Wesley Schuh Work Log

MILESTONE 1:

Wednesday, September 27, 2023

Met with the Ethans in class to discuss which processor type to use and which instructions we will need. We chose a load store processor (though other options are still on the table) and created a list of 16 instructions our processor will need to handle. We read further over milestone 1 and established a time to meet over the weekend with Garrett. [45 minutes]

Sunday, October 1, 2023

Met with everyone to finalize processor type and create design document. We eventually decided on a mix between accumulator and mem to mem. Scratch that, we're doing entirely memory to memory for efficiency purposes. We rewrote our instructions with memory to memory in mind. We started on the design document, with my specific roles being the abstract, the logical and verbose descriptions in the ISA table, and setting up the Github. Aside from the in-class meeting on Tuesday, we have planned our next meeting for Wednesday afternoon. [3 hours]

Monday, October 2, 2023

Individually reviewed design document to finalize and add my assignments from yesterday. I added the L instruction type and a description of what it does to the list of types since it was missing. I also added another code fragment and machine language translation for swap since the specifications imply multiple fragments. [30 minutes]

Tuesday, October 3, 2023

Met with everyone in class to make some final adjustments to design document. I confirmed my changes from yesterday. [30 minutes]

The plan for our next meeting is to:

1. Look over M2
2. Allocate instruction types for RTL descriptions
3. Take instruction types allocated to me, convert them into pseudocode, and convert the pseudocode into components [est 2 hours]