Wesley Schuh Work Log

MILESTONE 1:

Wednesday, September 27, 2023

Met with the Ethans in class to discuss which processor type to use and which instructions we will need. We chose a load store processor (though other options are still on the table) and created a list of 16 instructions our processor will need to handle. We read further over milestone 1 and established a time to meet over the weekend with Garrett. [45 minutes]

Sunday, October 1, 2023

Met with everyone to finalize processor type and create the design document. We eventually decided on a mix between accumulator and mem to mem. Scratch that, we're doing entirely memory to memory for efficiency purposes. We rewrote our instructions with memory to memory in mind. We started on the design document, with my specific roles being the abstract, the logical and verbose descriptions in the ISA table, and setting up the Github. Aside from the in-class meeting on Tuesday, we have planned our next meeting for Wednesday afternoon. [3 hours]

Monday, October 2, 2023

Individually reviewed design document to finalize and add my assignments from yesterday. I added the L instruction type and a description of what it does to the list of types since it was missing. I also added another code fragment and machine language translation for swap since the specifications imply multiple fragments. [30 minutes]

Tuesday, October 3, 2023

Met with everyone in class to make some final adjustments to design document. I confirmed my changes from yesterday. [30 minutes]

The plan for our next meeting is to:

1. Look over M2
2. Allocate instruction types for RTL descriptions
3. Take instruction types allocated to me, convert them into pseudocode, and convert the pseudocode into components [est 2 hours]

MILESTONE 2:

Wednesday, October 4, 2023

Attended milestone meeting with the team to get feedback on M1. [15 minutes]

Met with everyone during the lab period after the milestone meeting. We reviewed the feedback from the meeting and adjusted the design document accordingly. I specifically added a new code fragment (if…else), moved the instruction blocking section into the instruction section, and changed the logical description column of the ISA so Mem[sX] was used wherever just sX was incorrectly used. While translating the gcd function, we ran into a problem of having to constantly push and pop input arguments for procedure calls. Ethan H and I planned on meeting with Dr. Stamm later today to discuss this, as well as some more of the specifications of M2 in preparation for the meeting with the entire group tonight. [1.5 hours]

Met with Ethan H and Dr. Stamm to discuss procedure calling conventions and clarify RTL specifications. Dr. Stamm confirmed the initial hypothesis that pushing the arguments and ra onto the stack was the best solution. [10 minutes]

Met with everyone to finish M1 revisions and start work on M2. I formatted the headers in the design document to create a table of contents, then went through the list of Dr. Stamm's annotations to verify that we accounted for everything. We then distributed the RTLs amongst ourselves, with my two being BR and BRI. We plan to do our assigned RTLs on our own time, then meet this Sunday to trade and test. [45 minutes]

Sunday, October 8, 2023

Attempted to write my RTLs (BR and BRI) and corresponding components. I'm hesitant on my initial drafts because I closely followed the single cycle RTL examples even though our processor must use multicycle, and there are not many examples of memory to memory RTLs online. The team plans to meet tomorrow to trade our RTLs and test them. [1 hour]

Monday, October 9, 2023

Met with everyone to complete most of M2. We collectively reviewed our RTLs to create a multicycle table and fill in the shared cycles. We then each added the cycles for our assigned RTLs (BR and BRI for me). Additionally, we put together a component description table and started naming conventions for modules, inputs, outputs, and

such. We then all took a general look at the RTLs as a test of sorts, but we are planning more thorough testing in the design document at some point in the next two days. My assignments before our next meeting in class on Wednesday are to document the machine and assembly language changes with Ethan H and work testing some of the RTLs in accordance with the new format individually. [2 hours]

Tuesday, October 10, 2023

Individually created an RTL testing table and assigned some conventions to inputs and outputs for testing. I filled in the A instruction in the RTL testing table as a template for the team to look at tomorrow to make sure my conventions are correct. If everything looks good, we will fill out the rest of the testing table tomorrow. I modified the instruction formats to place s1 before s2/imm (and made note of such in the language change log) as that made the most sense to Ethan H and I. [30 minutes]

Wednesday, October 11, 2023

Met with everyone in class to work more on M2. We collectively filled out the RTL testing table, with my specific tests being A and AI. I noticed that because of our swapping of s1 and s2/imm in the instruction formats, most machine code translations are now incorrect. I will correct these later today. [45 minutes]

Individually modified machine code translations so that they match our latest instruction format. In doing so, I noticed the order of the arguments for branch instructions was incorrectly listed as s1, s2/imm, dest instead of dest, s1, s2/imm, so I also fixed those. [45 minutes]

My tasks going into milestone 3 are:

1. Draw datapath with Ethan H
2. Write components and corresponding tests in Verilog (remains to be seen which ones) [est 4 hours]

MILESTONE 3:

Thursday, October 12, 2023

Attended milestone meeting with the team to get feedback on M2. [15 minutes]

Met with everyone during the class period after the milestone meeting. We reviewed the feedback from the meeting and adjusted the design document accordingly. I specifically modified the machine code translations of the code fragments by removing the 0x to clarify the blocking of the values. I also created a table for the ALU component which gives ALUOp instructions corresponding to certain 3-bit codes, giving meaning to the "op" in A op B. [30 minutes]

Friday, October 13, 2023

Crafted a rough draft of our datapath with Ethan H. Does it look good? Absolutely not. Does it work? Going through the RTLs, it looks like it should. If not, the solution is probably to add another mux somewhere. I built the datapath using an application called Lucidchart after we wrote our initial draft on paper, which was very helpful in making the datapath presentable. We have yet to add a control and associated signals. [1 hour]

Sunday, October 15, 2023

Tweaked the datapath by combining our many memory components into just two, one for reading and one for writing. I also put in the control signals, which now includes flags for each register determining whether or not to write to them. [30 minutes]

Monday, October 16, 2023

Met with everyone to discuss our progress and what to do next for this milestone. After talking with the team, we decided each ALU in our datapath could be condensed into one, so I adjusted the datapath accordingly. We also figured out we could combine our two current memory components into one in a way that should work after going through our RTLs. Ethan H and I also wrote descriptions for all the control signals. [1 hour]

Tuesday, October 17, 2023

Wrote the iterative implementation plan with Ethan H. We wrote a mix of testing the components in groups and then testing the components based on the RTL specifications. Our plan specifies everything we could think of besides muxes and

control signals for the muxes and other components. We thought the muxes were self explanatory and descriptions of each flag have already been put in the design document. We also had a pleasant discussion regarding which colors of the rainbow were best. We agreed that green and purple are the best two colors, but not necessarily in that order. [1.5 hours]

Wednesday, October 18, 2023

Met with everyone in class to have a brief discussion of what has been done this milestone, and what is still needed before the milestone is due. We have come up with an interesting special feature of the processor, the specifications of which I cannot disclose at this time. [20 minutes]

My tasks going into milestone 4 are:

1. Specify control units (implement control) with Ethan H
2. Create control truth table and FSM
3. Implement stage 3 of the integration plan
4. Lab 7

MILESTONE 4:

Thursday, October 19, 2023

Attended milestone meeting with the team to get feedback on M3. Dr. Stamm is on team purple > green, and it hurts. [15 minutes]

Met with everyone during the class period after the milestone meeting. I modified the design document to include values for the control signals which are more than one bit. We started on the other topics we were assigned for this milestone and planned on finishing them on our own time. [30 minutes]

Sunday, October 12, 2023

Worked through lab 7. Remains to be seen if it works how I think it works. [2 hours]

We modified the JA type to include a cycle where Mem[A] is loaded into A as the datapath does not support PC = Mem[A]. We also updated the datapath to include a flag for writing to the PC similar to the other write register flags, and added a mux for the value going into register A to support A = PC + 1 in the SP type. [1 hour]

Monday, October 23, 2023

Met with everyone to review our progress in the milestone. I took the FSM and made it look nice with Lucidchart, while also adding the signals that have been changed since the first draft of the FSM. Looking over the lab, I don't think I implemented the connected control memory tests how I probably should have since it does not look like the memory.txt does anything when it has the different instructions. I plan to modify it and show it to Dr. Stamm in class tomorrow (maybe). Garrett has earned my trust as he has common sense and sees that $12 contains so much more than the $6 and is the superior option. The Ethans both chose $6 (hivemind). I wonder if the third Ethan would pick the same. [1.5 hours]

Tuesday, October 24, 2023

Modified the lab testbench, and I'm pretty sure that it performs how it's supposed to. I suppose Dr. Stamm will be the judge of that. I will most likely have to show it some time Wednesday or later. [1 hour]

I finally updated the blocking of the datapath in the iterative implementation plan since it was recommended in the last milestone meeting. I added somewhat of a control unit design implementation plan as well since it feels very similar to the lab. Also, today brings sad news. Garrett has betrayed me and joined the $6 side, even though the $12 is *clearly* a better deal. I fear I will die on this hill alone. [2 hours]

My tasks going into milestone 5 are:

1. Finish lab 7
2. Implement control and testbench
3. Modify FSM if necessary [est 6 hours]

MILESTONE 5:

Wednesday, October 25, 2023

Update: The lab does NOT perform how it is supposed to. Turns out datain has no purpose in the lab, so we were panicking over nothing. We made some minor changes like incrementing the PC instead of hardcoding it for each instruction. Ethan and I checked in the lab for the group after making these revisions. [1 hour]

Friday, October 27, 2023

Garrett wanted to work on memory, so I walked through the lab with him and showed him how to store values in memory from a text file and view memory in ModelSim. We made some minor changes to the memory unit to fit the specifications of our project, like changes the input and output names to match our naming conventions and changing data and address widths. [1 hour]

Sunday, October 29, 2023

Updated the control unit design in the design document to have a plan going into designing the actual control unit. I then actually implemented the control unit and a testbench in Verilog. It is very messy, but I think it works. At least, it does with my testbench. [2 hours]

🎃 Tuesday, October 31, 2023 🎃

Had to update the FSM in the design document since Garrett found a few incorrect signals when integrating the control with previous stages. I also updated the control testbench with the new values for the signals and adjusted some timings since control was changed to where the control signals are set first on the rising edge and then the state changes on the falling edge. [1 hour]

Wednesday, November 1, 2023

Met with everyone in class to finish requirements for milestone 5, which included running relPrime. Garrett had a working version ahead of time, yet it was not running for the rest of us. We tracked the error to state_7, which had a state input for the control which we had previously removed. After fixing this, relPrime ran great. What did not run great, however, was compiling the project in Quartus. It compiles very slowly with certain address widths for memory. We spent some time trying to improve this, which

eventually led Garrett to make some significant changes for the better to memory. [2 hours]

My tasks going into milestone 6 are:

1. Work on evaluating the performance of our design
2. Make any minor changes to implementation or design document with team if necessary [est 5 hours]

MILESTONE 6:

Monday, November 6, 2023

Met with everyone in class to keep working on the milestone. I spent most of the time in class today planning how to format the final design document, and made a note to make changes to the blocking on the iterative implementation plan as the current ms paint sketches look rough. [1 hour]

Tuesday, November 7, 2023

Met with everyone in class to keep working on the milestone. The Ethans and I worked on the assembler and made some minor changes, including changing some words which were incorrectly regarded as memory addresses into labels. Input and output theoretically work in the assembler as well, though they are handled in a weird way. They are memory addresses, but are handled like labels. It's best not to think about it. I plan on testing it more at some point later. [1 hour]

Wednesday, November 8, 2023

Met with everyone in class to keep working on the milestone. We created a slides presentation and made a basic outline, and we will most likely work on it more Thursday/Friday. [1 hour]

My tasks going into milestones 7/8 are:

1. Write final, well-formatted design document with team
2. Work on and practice presentation with team [est 5 hours]

Sunday, November 12, 2023

Worked on final presentation and final design document with the team. We ran through the presentation a few times to verify that we all know what we're doing for tomorrow. [3 hours]