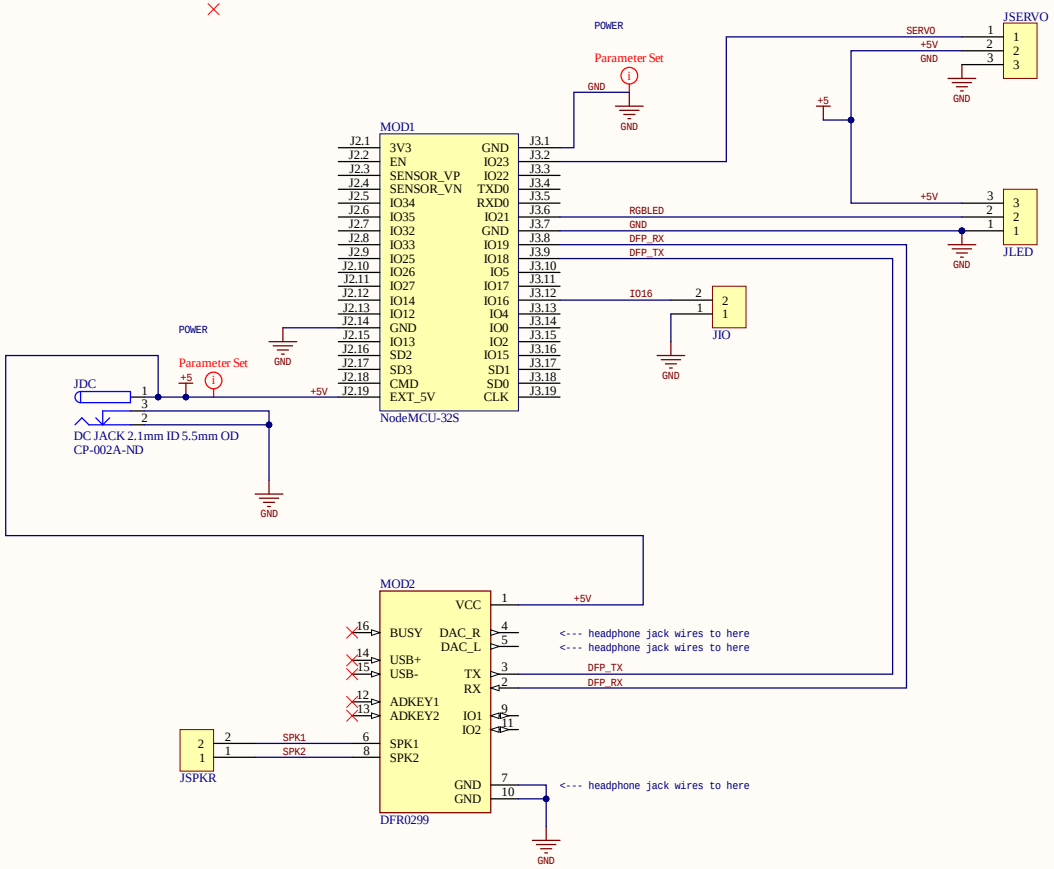
Release History

Version	Release Date	Comment
beta0-draft	00/00	Initial Version



[No Variations]

Title			ToyBuilder Labs 2736 E Walnut St Pasadena, California 91107
Size: B	Number:	Revision:	
Date: 4/14/2022	Time: 6:36:18 PM	Sheet 1 of 1	+1 (626) 808-4010
File: C:\Users\joech\Dropbox\work\altium\tbl examples\esp32-dfplayer\esp32-dfplayer\esp32-dfplayer.SchDoc			

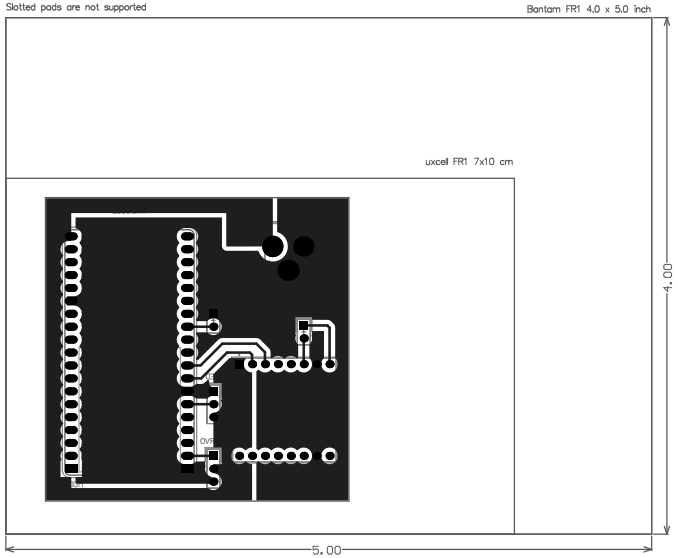
NOTE TO DESIGNERS

Tooling data (starting place -- adjust/update as needed)
1/32 Bit = 31.25 mil. Real world size = 33 mil
15deg 3 flute stub = 7.1 mil. Real world size = 8 mil
P2E-D1/32 (2 flute flat) = 31.25 mil. Real world size = 33 mil

Recommended clearance: 10 mil
Minimum clearance: 8 mil

Do not pour un-needed poly. Let CNC workflow create isolation milling.

Slotted pads are not supported



Layer	Name	Material	Thickness	Constant	Gerber	Board Layer Stack
1	Top Layer	CF-004	0.035mm		GTL	
	Dielectric 1	Core-043	1.499mm	4.3		
2	Bottom Layer	CF-004	0.035mm		GBL	

检查制造说明中的重要细节。(CN)
제작 노트에서 중요한 세부 사항을 확인하십시오. (KO)
Überprüfen Sie wichtige Details in den Fertigungshinweisen. (DE)

Check important details in fabrication notes. (EN)

必须具有 UL 标志，有关详细信息，请参见注释。 (CN)
UL 표시가 필요합니다. 자세한 내용은 참고 사항을 참조하십시오. (KO)
UL-Kennzeichnung erforderlich. Einzelheiten finden Sie in den Hinweisen. (DE)

UL Marking Required. See notes for details. (US/GB)

Client Name: Client Unassigned
Project Name: Project Unassigned

File: esp32-dfplayer.PcbDoc
Rev: beta0

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. Board Dimension: mm x mm
2. Total Thickness: 1.6 mm +/- 10%
3. Board Material: FR-4, Tg130+
4. Copper Layers: 2, Weight: 1 oz
5. Soldermask Layers: Both, Color: Green (LPI preferred)
6. Legend Layers: Both, Color: White. (LPI preferred)
7. Finish: ENIG or HASL
8. Fabricate PCB According to IPC-6012 Class 1
9. 1.5 mm (0.06") maximum radius on any inside corner.

SPECIAL REQUIREMENTS:

VENDOR NOTES:
10. Route board shape and any cut outs per Board Outline layer.
11. Place Manufacturer Mark and Date Code on bottom
12. Boards must pass visual inspection per IPC-A-600 Class 1

Engineering Contact: joseph@toybuilderlabs.com

'Multilayer Composite Print'
'Multilayer Composite Print'

ToyBuilder LABS

Not in version control

Notes: (unless otherwise specified)
1. Mils are the controlling dimensions for the drawings and supplied data. Millimeters dimensions are for reference only.
2. Fabricate PCB in accordance with IPC-6012, Class 2; per IPC-6011.
3. Materials:
   1. Laminate and Prepreg (B-stage) to be in accordance with IPC-4101/126.
   2. Copper foil to be in accordance with IPC-4562. Please see stackup for finished copper thickness.
4. All holes shall be located within 0.2 (0.008) Diameter of True Position. Layer to layer registration shall be within 0.125 (0.005).
5. Finish:
   1. All exposed conductive pattern areas not covered with solder mask or other plating shall be plated with Electroless Nickel/Immersion Gold (ENIG) per IPC-4552.
   2. Apply liquid photo imageable solder mask (color green) per IPC-SM-840, class H, to both sides of the board over bare copper. Via holes covered with solder mask do not need to be plugged. Only solder mask images that are the same size as the component pads may be enlarged, and shall not be enlarged beyond 0.08 (0.003) per side or 0.15 (0.006) overall. All other solder mask images shall not be enlarged. Tent all vias.
6. Marking:
   1. Board part number and revision letter is rendered in etch on the top side of the board. Revision letter should be identical to this drawing.
   2. UL recognized vendor mark and date code shall be rendered in etch on the bottom side of the board.
   3. Silkscreen shall be white, permanent, organic, non-conductive ink. No ink to appear on component pads.
7. Finished PCB to be subject to 100% continuity and isolation electrical test. Test fixtures to be generated from IPC-D-356 formatted netlist data, cross-referenced to gerber extracted netlist data.
8. Tolerances:
   1. Warp or twist of board shall not exceed 1%.
   2. Conductor widths and spacing shall be within 0.03 (0.001) of gerber data.
   3. Remove all burrs and break sharp edges 0.4 (0.015) maximum.
   4. Surface Mount Pad plating must be flat to a maximum of 0.08 (0.003) above board surface.
   5. 1.5 (0.06) maximum radius on any inside corner.
9. Thieving:
   1. Supplier may add thieving to compensate for low copper density areas.
   2. The following guidelines must be adhered to in order to maintain electrical and mechanical integrity of the design:
      1. Thieving to fiducial spacing 200 mil minimum.
      2. Thieving to non-plated through holes 200 mil minimum.
      3. Thieving to all other features 100 mil minimum.
      4. There shall be no exposed thieving in any areas free of solder mask.

https://www.analog.com/media/en/technical-documentation/evaluation-documentation/hmc7043-fab-drawing.pdfa

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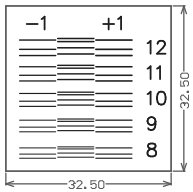

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Client Name: Client Unassigned
Project Name: Project Unassigned

File: Othermill Calibrator.PcbDoc
Rev: beta0

NOTES:
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Board Stack Report