

# Tyler Neal

## Embedded Software Engineer

Chesterfield, MI, 48047 | +1 810-278-2749 | [tylernel.dev@gmail.com](mailto:tylernel.dev@gmail.com) | [github.com/tp-neal](https://github.com/tp-neal) | [linkedin.com/in/tyler-neal-dev](https://linkedin.com/in/tyler-neal-dev)

## SUMMARY

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Recent graduate from Michigan Technological University specializing in embedded systems and firmware development. Proven ability to design, build, and debug complex C/C++ projects on bare-metal and RTOS platforms, from initial circuit design to final firmware implementation. Seeking a role as an Embedded Software Engineer to solve challenging problems in robotics, IoT, or automotive systems.

## EDUCATION

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**Bachelor's of Science in Computer Science**, Major GPA: 3.43  
*Michigan Technological University*

2020 – 2024  
*Houghton, MI*

## PROJECTS

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**RTOS-Based Self-Balancing Robot** | C, FreeRTOS, PID Control, STM32, ARM Cortex-M

June 2025 – August 2025

- Developed real-time firmware in C for a two-wheeled self-balancing robot on an STM32 microcontroller.
- Implemented a PID (Proportional-Integral-Derivative) control loop to maintain the robot's upright balance by modulating motor speed based on sensor feedback.
- Engineered a sensor fusion algorithm using a complementary filter to combine accelerometer and gyroscope data from an MPU6050 IMU for an accurate pitch estimate.
- Architected a multithreaded system using FreeRTOS, employing mutexes and semaphores to ensure thread-safe data sharing between sensor acquisition and control logic tasks.

**Bare-Metal "Simon Says" Game** | C, Bare-Metal, STM32, ARM Cortex-M

May 2025 – June 2025

- Developed a "Simon Says" memory game on an STM32L476RG microcontroller, programming directly against hardware registers in C without the use of HAL or vendor libraries.
- Engineered peripheral drivers from scratch for GPIO pin configuration, SysTick timer for precise millisecond delays, and ADC for generating a random seed from pin noise.
- Configured the system clock by enabling the PLL to scale the HSI oscillator to 80MHz through direct register manipulation.

**Multi-Layer Cache Simulator** | **Research Project** | C, Spec95

March 2024 – April 2024

- Designed and implemented a multi-layer (L1, L2, L3) direct-mapped write-back trace-based cache simulator in C
- Analyzed cache hit/miss rate, and memory access time using trace-based simulation with the Spec95 benchmark suite; validating trace files up to 6.15GB.
- Authored a technical paper detailing simulator design, performance metrics, and cache management techniques.

## TECHNICAL SKILLS

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**Embedded Development:** C, C++, Bare-Metal & RTOS (FreeRTOS) Programming, ARM Cortex-M, STM32

**Hardware & Protocols:** I2C, UART, GPIO, PWM, ADC

**Software & Tools:** Git, GDB, Make, Valgrind, Linux, Bash

**Other Languages:** Python, C#, Java, JavaScript, SQL