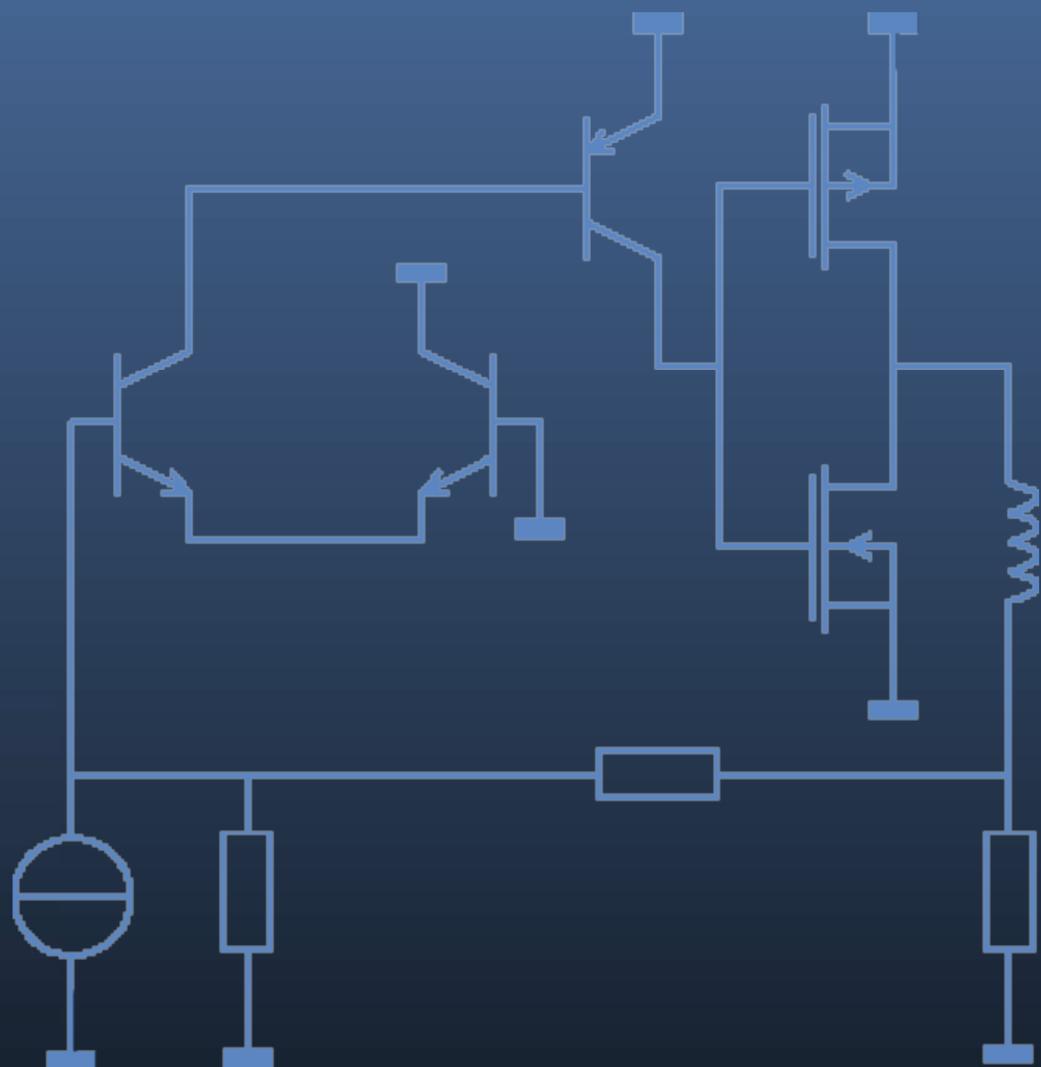


GRADIENT AMPLIFIER DESIGN



D.H. de Gans

Gradient Amplifier Design

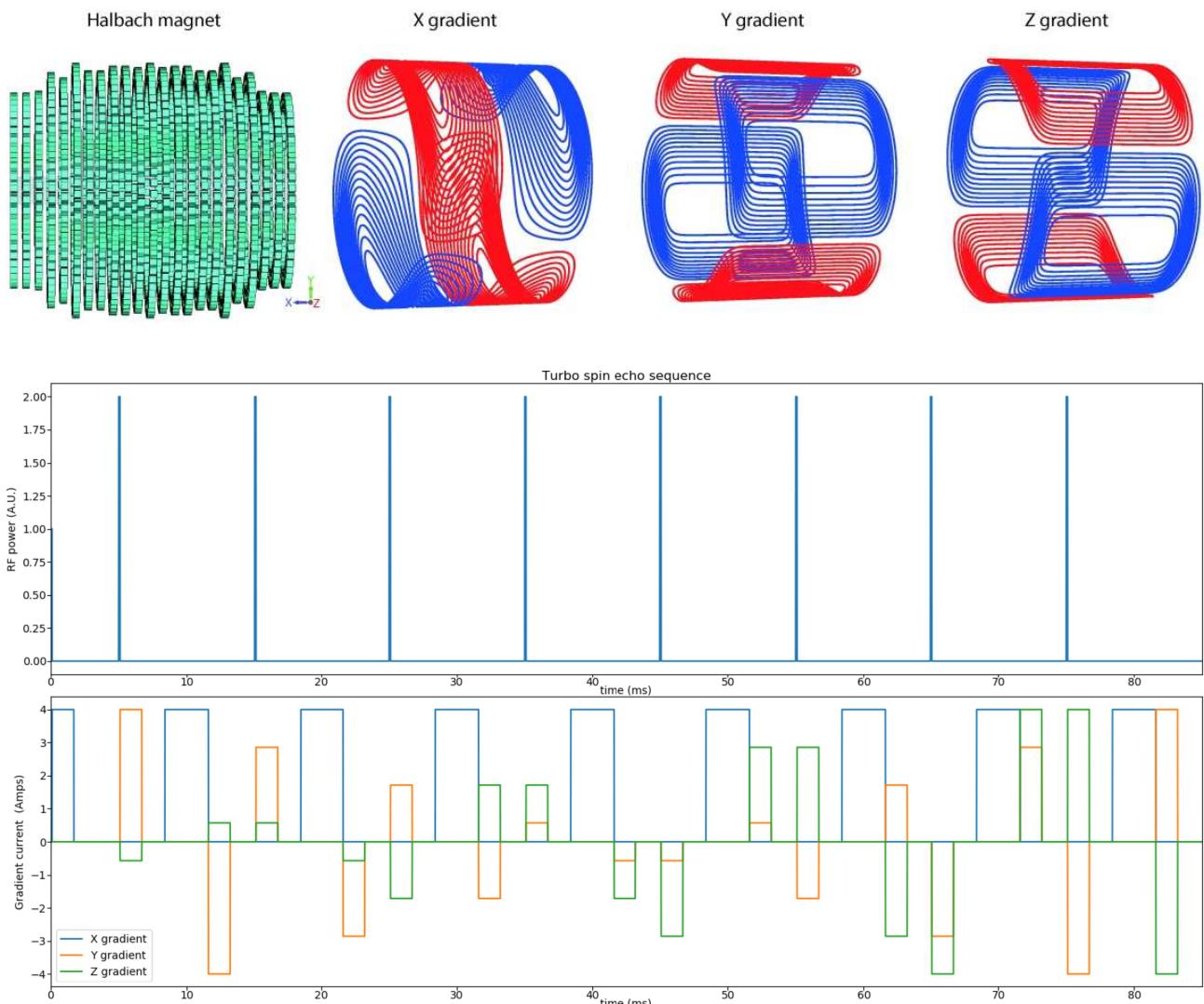
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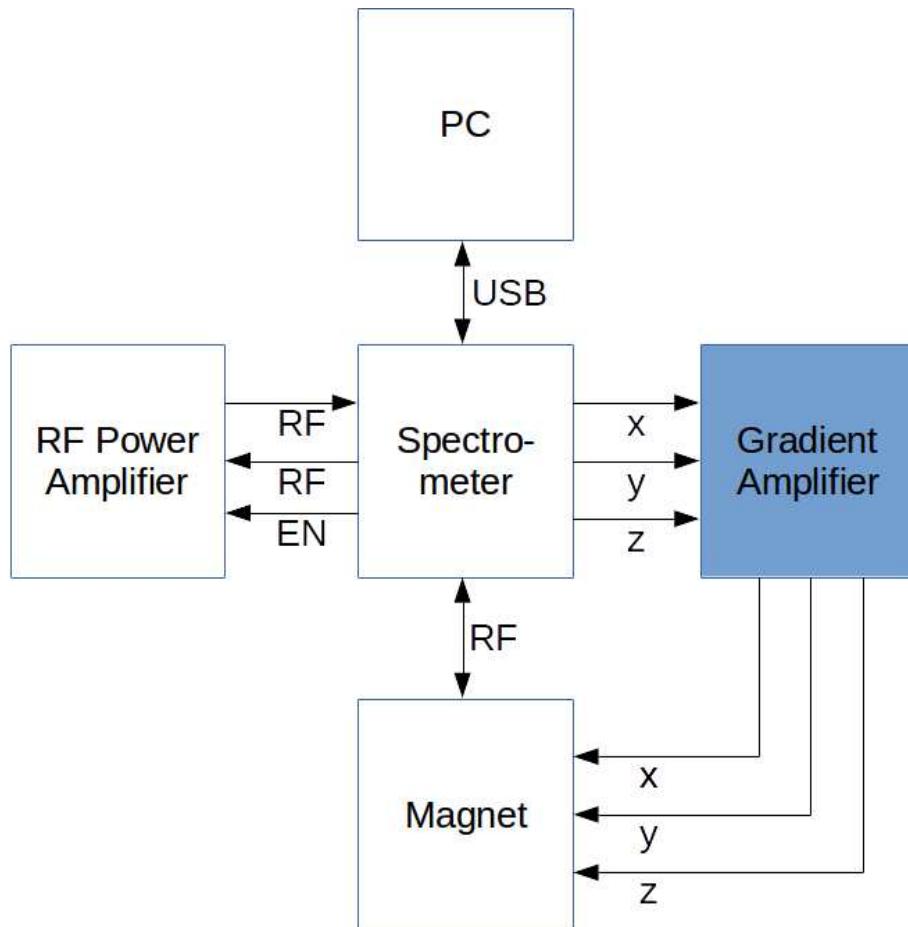
1 Specifications

- $I_{LOAD} = \pm 15A$
- duty cycle 30% per channel
- battery powered
- $V_{in} = \pm 10V$
- low noise current and EMI especially between 0,5MHz ... 5MHz
- $L = 20\mu H \dots 300\mu H$ ($180\mu H$)
- $ESR = 0,4\Omega$ $C_{PAR} = 130pF$
- $t_r = 50\mu s$, $B = 7kHz$
- $R_{SOURCE} = 200\Omega$
- overload protection



The typical driving pattern for all three outputs is a square pulse sequence that increases in amplitude during the measurement as the gradient needs to be stronger.

2 Place in the MRI system



Central in the low field MRI system is the spectrometer that controls the electronics. The gradient amplifier delivers current to the three gradient coils to produce magnetic fields in addition to the static magnetic field.

The spectrometer has BNC connectors to connect to both amplifiers and the magnet's RF coil. This means that all signals are single ended.

The magnet has banana plugs to connect the gradient amplifier to the gradient coils.

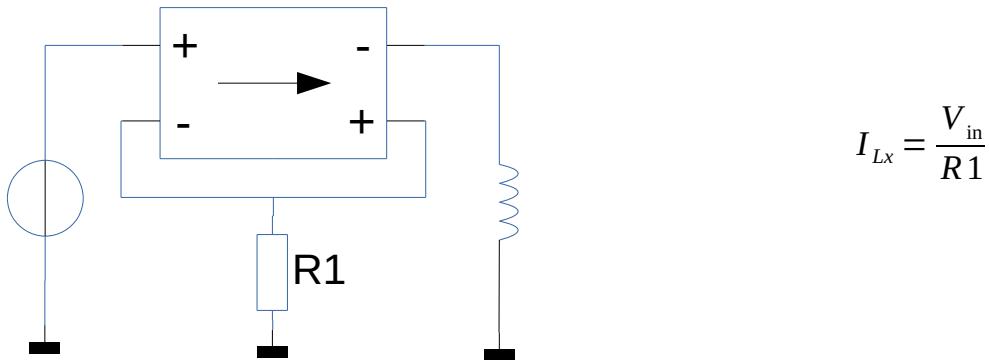
Since the gradient coils are directly located around the RF coil of the magnet, intrinsic noise and EMI can easily couple into the RF coil and distort very weak MR signal.

3 Circuit Design

3.1 Feedback Network At ∞ and Loop Gain

It is not possible to measure the magnetic field and use that for feedback. Since the magnetic field is proportional to the current through the coils it makes sense to design a current output amplifier to have the best control over the magnetic field.

The signals going to the gradient amplifier are single ended voltage pulses with a range of -10V to 10V. The most suitable nullor configuration for this is the following.

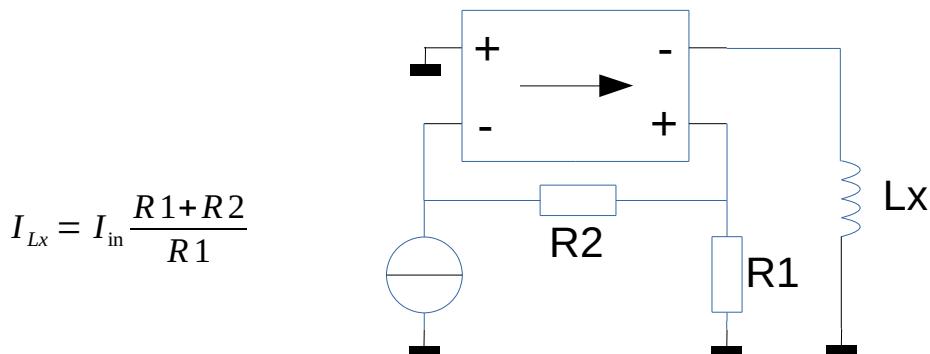


This results in a feedback resistor of $R_1 = \frac{V_{in}}{I_{out}} = \frac{10V}{15A} = 0,66\Omega$ which is not a practical choice for two reasons:

1. It would produce over 150W of power dissipation in the feedback resistor.
2. The required voltage span with R_1 and the load combined is more than double of that of the load alone.

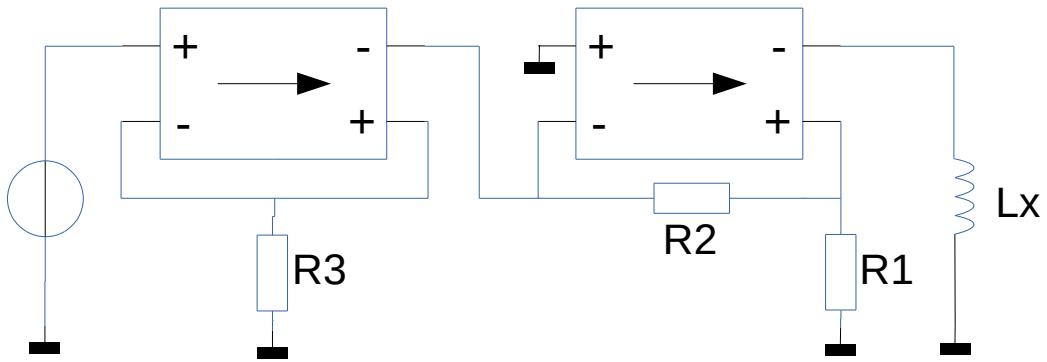
The solution in the first design was to attenuate the input signal by 20dB while adding 20dB gain in the feedback path. This way R_1 can be reduced to 1/100 of the normal value, but it also introduces at least one extra dominant pole in the loop that has to be compensated for to maintain stability.

A current amplifier is able to solve the dissipation problem in the feedback resistor.



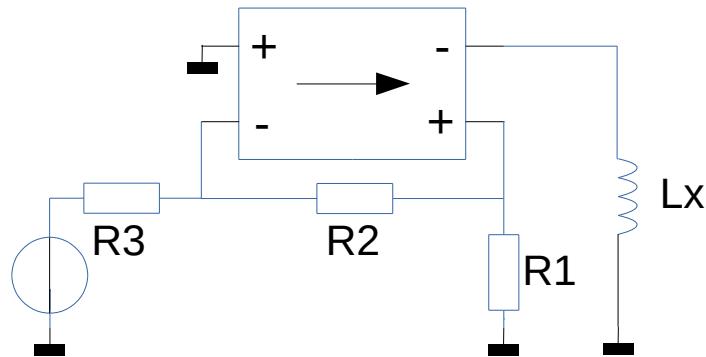
R_1 can be made arbitrarily small now since it's the combination of R_1 and R_2 that determine the transfer function. I_{Lx} is independent of the load as far as the available voltage range allows it of course.

The input voltage will have to be converted to a current first, making it a two stage amplifier.

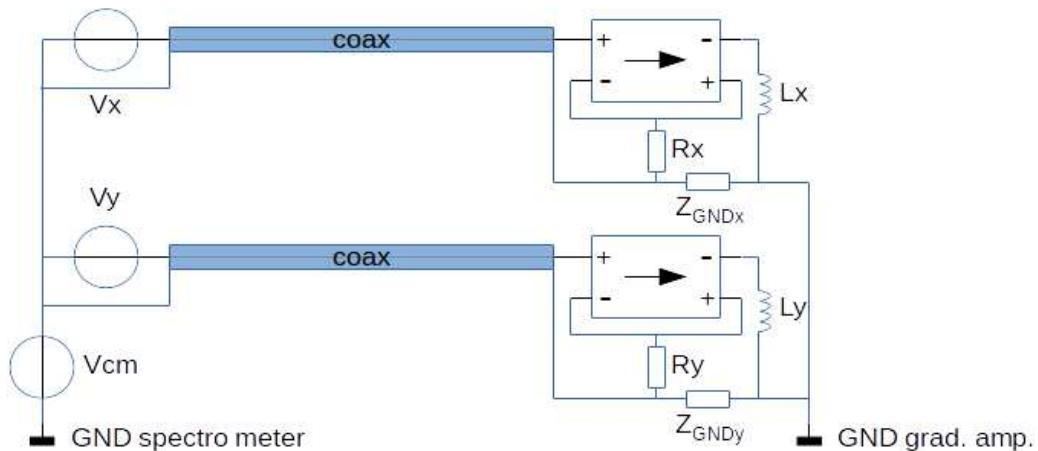


This configuration doesn't load the source which makes the amplifier independent of the source impedance. To make the input robust against high voltage spikes a series resistor and clamping diodes could be added at the cost of increased noise.

An alternative could be to leave out the first nullor and connect R3 directly between the input voltage source and the inverting input of the second nullor. This simplifies the design and increases robustness against high voltage spikes at the cost of reduced independence of the source impedance.



High currents will flow in the three gradient amplifier outputs. This will lead to practically unavoidable voltage rise of the local GND. Directly coupling the GND's of the input sources to the GND's of each channel will cause significant currents in the shields of the coax cables which is very undesirable. The voltage over the shielding because of these currents will add to the desired driving voltage making the output currents dependent of each other.



This drawing shows how the spectrometer and two channels of the gradient amplifier would be connected if no care was taken about isolation of the inputs. If a current is flowing through Rx there will be a current division between the path through Z_{GNDx} and the two coax cables with Z_{GNDy} in series. This causes a parasitic voltage at the input of channel y.

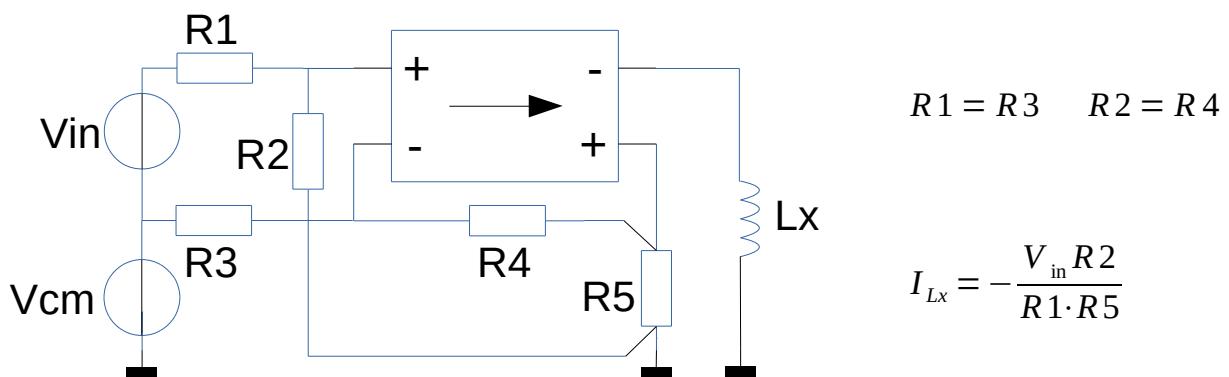
A second problem that this drawing reveals is that if both GNDs are connected to each other then high currents can flow through the shields of the coax cables as a result of a common mode voltage. This would cause all outputs to produce currents because of voltage drop in the shields of the cables. Having a battery powered gradient amplifier could prevent this loop.

- Isolation of the GNDs is absolutely necessary to keep control over the path that the current takes and to prevent a GND loop current through the amplifier circuit. In the ideal situation no current flows through the coax cables' inner conductor and shield. A single star point will connect the three GNDs together.

When a difference amplifier at the input is used as an isolation barrier between the single ended spectrometer voltage output and the gradient amplifier this has four big advantages

1. Isolation of the GND's of the spectrometer and the amplifier
2. Suppression of common mode voltage.
3. Greatly improves robustness against large voltage spikes at the input.
4. Makes it possible to produce a steering voltage relative to the local GND at R5.

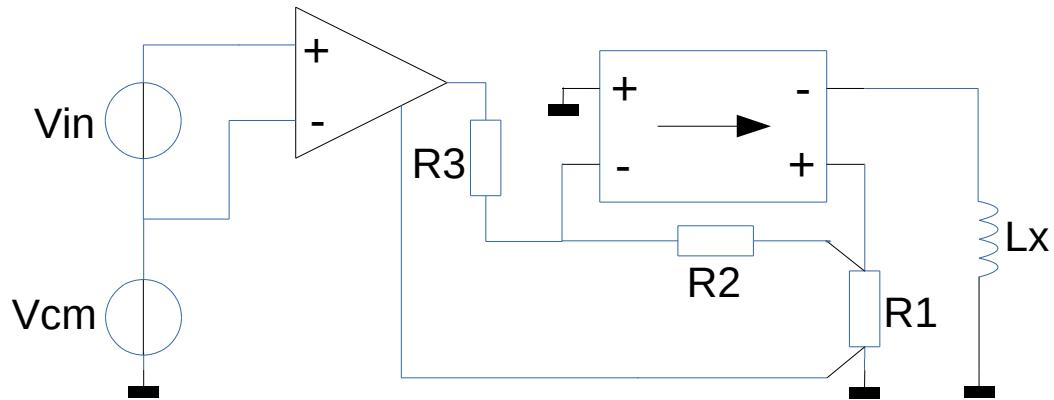
Especially the last point is of great importance since the high current will likely lift the voltage of the GND per channel locally. Since all three channels are driven from a common ground at the spectrometer this would otherwise result in cross coupling between the x, y, and z channel.



The common mode rejection ratio of this amplifier depends on how well resistors R1,R3 and R2,R4 match. The series resistance of Vin adds to R1 so to balance the input resistors R3 has to be increased with the same resistance (200Ω in this case). Choosing higher values for R1 to R4 decreases the influence of the resistance of the source.

For 1% gain error caused by $R_s=200\Omega$, R1 and R3 must be $20k\Omega$. R5=5mΩ as practical lower limit. R2 and R4 will be 150Ω to get 15A @10V or 180Ω to compensate for loss in gain and to have some margin. R2 and R4 dominate the noise caused by the feedback network which is a good thing. This brings the noise current density at the output to $488nA/\sqrt{Hz}$.

An instrumentation amplifier doesn't load the source, has better CMRR, and has all of the advantages of the difference amplifier except for the extreme robustness. Extra input resistors and clamping diodes are required to achieve this.



$$I_{Lx} = V_{in} \frac{R1+R2}{R1 R3} \quad L \approx G \cdot R1$$

When $R1$ is chosen to be $5\text{m}\Omega$ as a practical lower limit this will produce $1,1\text{W}$ @ 15A and a maximum voltage of 75mV . $R3:R2 = 130:1$, so $R3$ could be $13\text{k}\Omega$ and $R2$ 100Ω or even $1,3\text{k}\Omega$ and 10Ω . $R2$ will be the dominant noise source which can be significantly lower than in the difference amplifier situation depending on the choice of $R2$. At 10Ω the output noise current density is $81\text{nA}/\sqrt{\text{Hz}}$ which is an improvement of $15,5\text{dB}$ compared to the previous topology. To reach 1% gain error because of limited loop gain G needs to be at least 20kA/V or if the nullor is a CCCS $H > 200\text{k}$.

- This topology will perform better in noise rejection from outside and also produce less intrinsic noise than the difference amplifier. The gain is independent of the source resistance but an extra input filter is required to reach the same robustness against voltage spikes. The extra resistance of the input filter will add negligible noise.

Shielding of the cable is also an issue that needs to be considered. A shielded twisted pair can provide better shielding than a coax cable that is used until now. The equivalent circuit for the feedback network is the following:

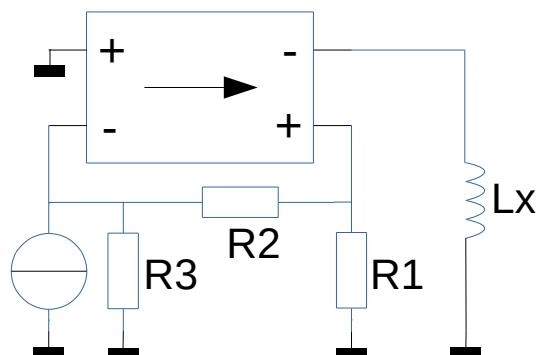
$$R1 = 5\text{m}\Omega$$

$$R2 = 10\Omega$$

$$R3 = 1,3\text{k}\Omega$$

$$L > 100$$

$$At\infty = 1,54 \text{ A/V}$$



3.2 Nullor Design

3.2.1 Noise, Drift & Offset

Noise drift and offset can all be seen as added unwanted voltage and current sources throughout the amplifier. When the input stage has a high gain all these effects are mainly determined by the input stage. This part of the design therefore is about the input stage.

Feedback resistor R1 is very low and the offset voltage and its drift are present with about unity gain across this resistor. Small voltage deviations at the input have a large consequence for the output current because of this. The offset voltage of a BJT is lower than for a FET since for a FET it's proportional to $V_{ov}/2$ and for a BJT to V_T . Offset voltage V_{os} of a BJT is determined by the equality if I_s , I_c and temperature.

The influence of I_c and I_s is given by $V_{os} = \frac{kT}{q} \ln \left(\frac{I_{c1}}{I_{c2}} \cdot \frac{I_{s2}}{I_{s1}} \right)$

Voltage drift is proportional to the offset voltage by $\frac{dV_{os}}{dT} = \frac{V_{os}}{T}$

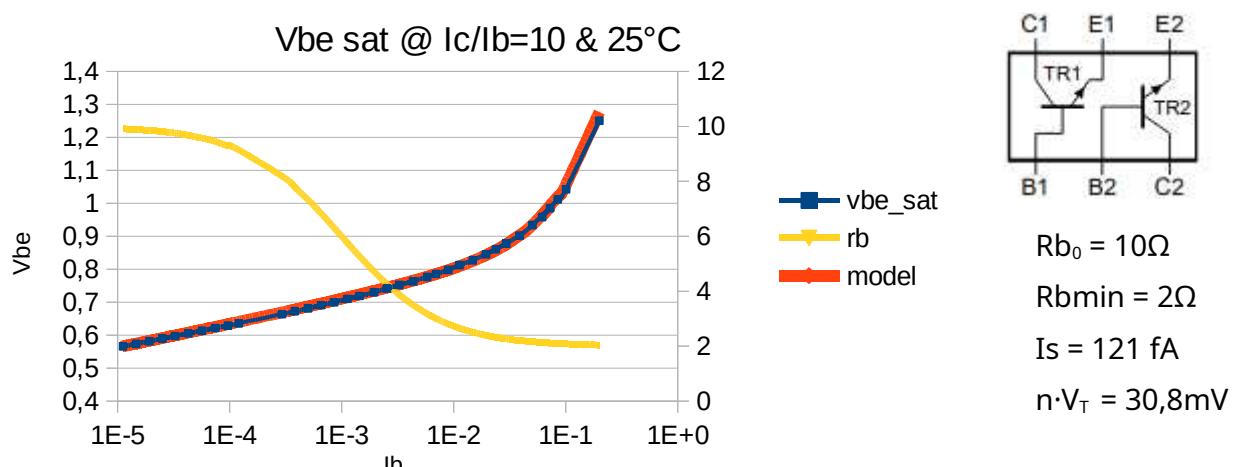
This means that an amplifier with low offset voltage also has low drift and also that it pays off to have an offset correction. However the correction should have the same temperature coefficient otherwise it could make it worse.

- V_{BE} drifts with $-2\text{mV}/^\circ\text{C}$ which is 2 or 3 orders of magnitude higher than the drift caused by I_c and I_s mismatch, so thermal matching is critical.
- These dependencies call for a matched dual transistor in a single package for the differential pair at the input.
- Thin film or metal film resistors should be used where temperature stability and excess noise matter.

BCM56DS dual matched NPN SOT457 (complementary with BCM53DS)

Rb @ 15mA	Hfe @ 15mA, 1V	f _T @ 15mA, 5V	Ic max	Vceo	Cob @ 1V	ΔV _{BE} max	Rth @ std. footprint
9 Ω	130	120 MHz	1 A	80 V	10 pF	2 mV	463 °C/W

Rbmin. was estimated from the Vbe sat curve below. Rb is from the spice model at 15mA.



The lower limit for the output noise as determined by the feedback network is $81\text{nA}/\sqrt{\text{Hz}}$. This is almost entirely set by: $\text{In} = \text{Vn}_{100\Omega} / 5\text{m}\Omega$. The input stage of the nullor will be designed now. This will determine the total noise behavior together with the feedback network.

- BJTs have a better noise performance at low source resistances and low frequencies than FETs. The choice for a BJT as the input device is obvious because the impedance as seen at the input from the amplifier is about 10Ω and the required bandwidth less than 10kHz .

The optimum collector current for a single CE stage is $I_{C_{opt}} = \frac{V_T \sqrt{h_{FE}}}{R_b + R_s}$

which results in 15mA for the BCM56DS.

input noise voltage sources for a differential stage:

$$\text{Ib1: } v_n^2 = \frac{2qI_c}{h_{FE}}(R_s + R_b) \quad 7,01\text{E-22}$$

$$\text{Ib2: } v_n^2 = \frac{2qI_c}{h_{FE}}R_b \quad 3,32\text{E-22}$$

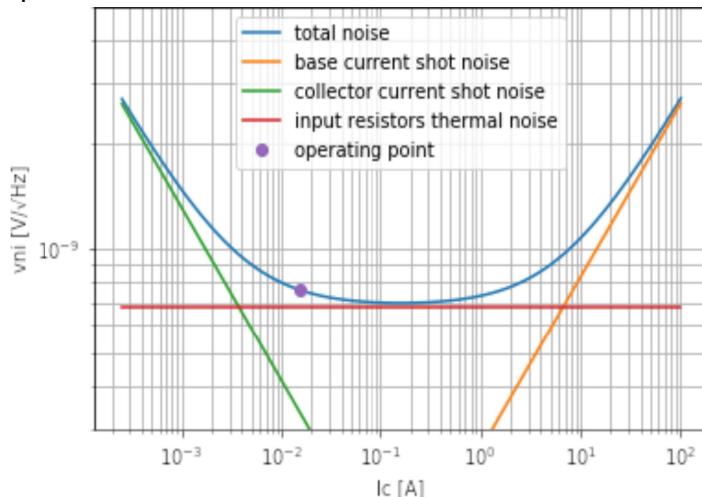
$$\text{Ic1,2: } v_n^2 = \frac{2qI_c}{\left(\frac{g_m}{2}\right)^2} \quad 5,71\text{E-20 (twice)}$$

$$R_{BB1,2}: \quad v_n^2 = 4kTR_B \quad 1,49\text{E-19 (twice)}$$

$$\text{Rs: } v_n^2 = 4kTR_S \quad 1,66\text{E-19} + \\ 5,79\text{E-19} \rightarrow 0,76\text{nV}/\sqrt{\text{Hz}}$$

The contribution of R_s , the parallel combination of R_2 and R_3 , is the dominant contribution to the total noise together with the R_{BB} . So the noise will be mainly determined by these.

The voltage gain from input to R_1 is practically 1. This input noise voltage over the $5\text{m}\Omega$ feedback resistor results in $152\text{nA}/\sqrt{\text{Hz}}$ at the output. That's only 1,9 times higher than the minimum obtainable noise from the feedback network alone. The input referred noise of the current amplifier is $76\text{pA}/\sqrt{\text{Hz}}$.



This plot shows the chosen bias point as a trade off between noise and collector current. At the cost of increased noise the bias current could be lowered a bit to reduce dissipation.

3.2.2 Distortion

If the output stage of a feedback amplifier has high gain then all previous stages operate more linearly because of the small signal amplitude. The distortion is mostly determined by the output stage then.

The output current of $\pm 15A$ requires a device that has high power gain. A power BJT has a lower h_{FE} which means that driving the output stage requires a significant current. A FET doesn't have this problem but only at low frequencies. Cgs of a power FET is in the nF range, so this is something to consider.

The load is inductive which means that current can be driven back into the output when the signal changes rapidly. MOSFETs have built in parasitic diodes that can redirect this current back to the power supply. This diode can handle the current that the MOSFET itself can handle, so no extra diode are required.

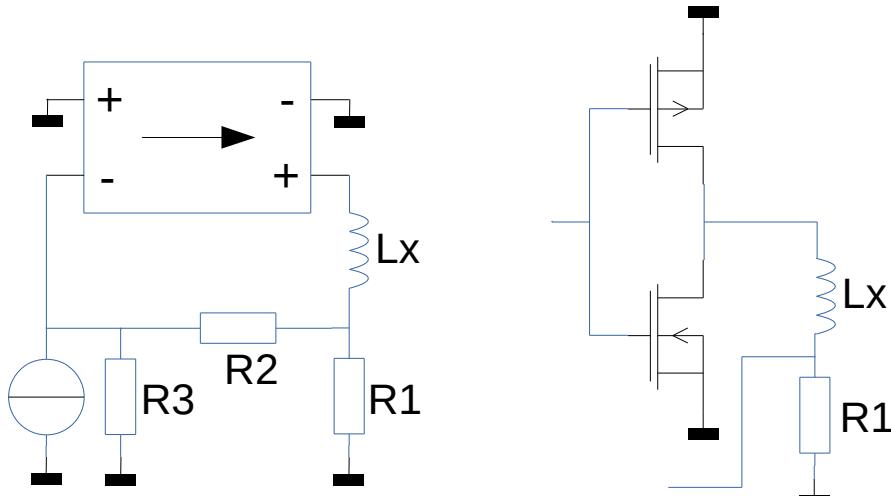
- The configuration with FETs with the highest gain is the CS stage. Since the amplifier has to be able to sink and source 15A two FETs will be required. Class A is not practical because that would waste a lot of power, so the output stage will be biased in class AB. A CS stage also matches best with the current output functionality of the amplifier.

MOSFET	I_{D25}	V_{DS}	k	$R_{DS\ ON}$	$R_{TH\ -JC}$	V_{TH}	C_{ISS}	C_{RSS}
IXTH90P10P	-90A	-100V	-16,9A/V ²	25mΩ	0,27K/W	-3,9V	5,8nF	510pF
IXTH96N20P	96A	200V	24,5A/V ²	24mΩ	0,25K/W	5,1V	4,8nF	270pF

$$I_D = \frac{1}{2} k (V_{GS} - V_{TH})^2$$

Parameter k is not given in MOSFET datasheets and was extracted from the $I_D(V_{GS})$ plot as well as V_{TH} that goes with it.

To get 15A out of the PFET and NFET a ΔV of 1,33V and 1,11V is required respectively at their gates. With a rise time of 50 μ s a drive current of less than 1mA is needs to be driven into the gates.

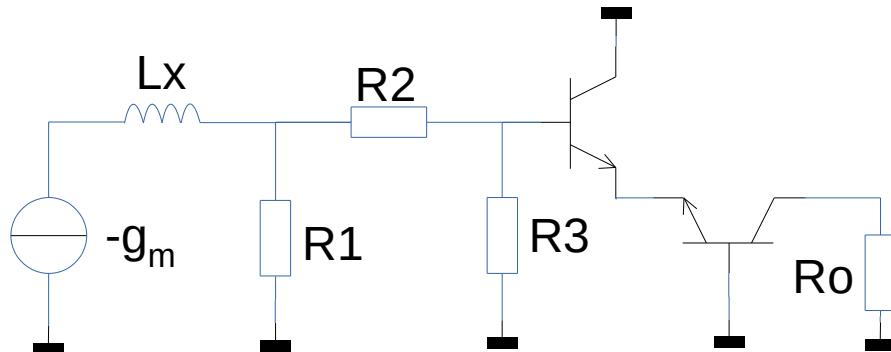


- By placing L_x in series with R_1 the output stage biasing, later in the design, becomes simpler.

3.2.3 Loop Gain

For the MOSFETs $g_m = \sqrt{2kI_D} \rightarrow 22,5_{(\text{PMOS})}$ and $27,1_{(\text{NMOS})}$ @ maximum current.

The minimum g_m depends on the bias current of the MOSFETs, so this can be chosen now. The loop gain of the current design with a differential input stage and the MOSFET output stage will be evaluated to determine the already available loop gain.

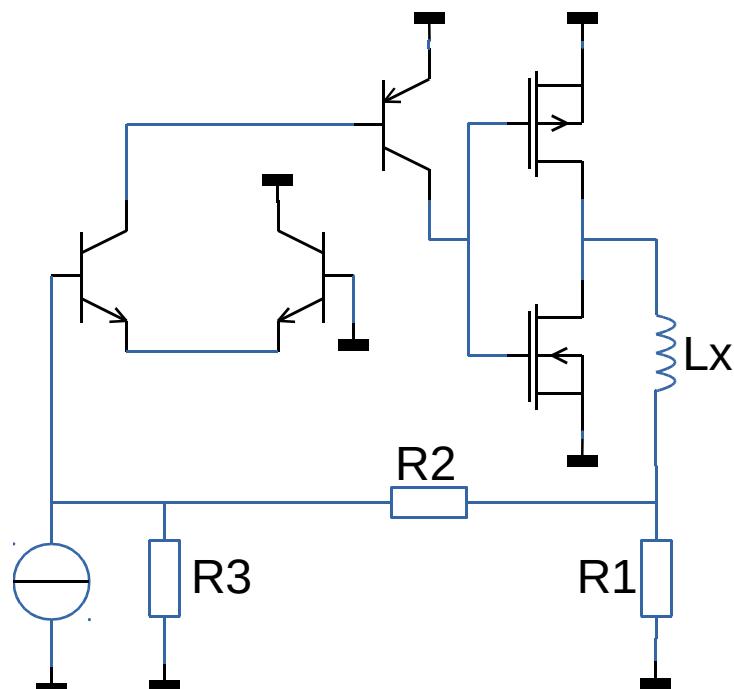


$$L \approx -g_m \cdot \frac{R_1}{R_1 + (R_2 + R_3 // 2h_{IE})} \cdot \frac{R_3}{R_3 + 2h_{IE}} \cdot h_{FE} \cdot R_o$$

R_o is the parallel resistance of a biasing current source and is estimated to be $1\text{k}\Omega$. This leaves g_m as the only unknown, and is calculated to be 41. This is even higher than the maximum value that will be reached, so

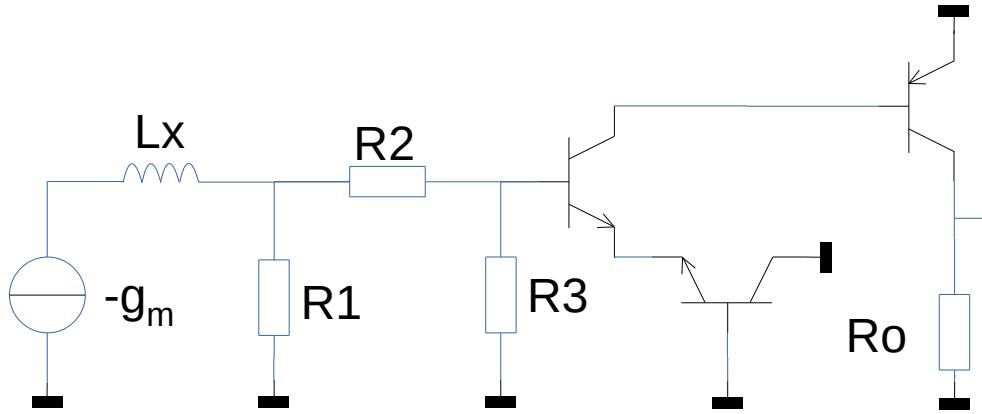
- An extra gain stage will be added between the input and output stage. This will be a BJT CE stage since this adds the most gain.

The gain stage needs to deliver at least 1mA to the gates so a bias current of 5mA should be enough. Now the loop gain for zero output current can be set to 100 by the bias current of the MOSFETs of the output stage.



BJT	R _b	H _{FE} @ 5mA	f _T @ 5mA	I _c max	V _{CEO}	C _{ob} @ 10V
50C02CH npn	29Ω	600	230MHz	500mA	50V	1,5pF
50A02CH pnp	28Ω	390	320MHz	500mA	50V	3,7pF

Both these transistors can be used for gain or as current source etc. at various places in the design.



At zero output current the g_m 's of both MOSFETs contribute about equally to the gain.

$$L \approx -g_m \cdot \frac{R_1}{R_1 + (R_2 + R_3 // 2h_{IE})} \cdot \frac{R_3}{R_3 + 2h_{IE}} \cdot h_{FE_N} \cdot h_{FE_p} \cdot R_o$$

10,7μ	0,65	350	390	2k5
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R_o is the combined resistance of the biasing and the r_o of the pnp transistor and will probably be about 2,5kΩ. The loop gain without the MOSFETs is about 2370, so there is easily enough loop gain now. If during the bias design some of the loop gain is lost, it will probably not be a problem.

Since g_m of a MOSFET changes with the square root of the drain current, biasing can put a limit to the change in loop gain between zero and maximum output current.

The maximum allowed drop in gain is 27,5dB to stay above a loop gain of 100.

$I_{BIAS} = \frac{I_{Dmax}}{400}$ will limit the change in loop gain to 20dB. This sets the bias current to 38mA

and the minimum combined g_m at 2,3.

3.2.4 Biasing

The bias current of each stage has been determined. The next step is to set or choose the voltages over the devices and the power supply.

Biasing results from previous steps		
Amplifier stage	currents	voltages
DV input stage	$I_{C1,2} = 15\text{mA}$	$V_{B1,2} = 0\text{V}$, $V_{E1,2} = -0,65\text{V}$, $V_{CE1} = V_{CE2}$
Gain stage	$I_C = 5\text{mA}$	- *
Output stage	$I_D = 38\text{mA}$	$V_{D1,2} = 0\text{V}$

The goal of biasing is to put the active devices in a state where they can deliver the performance that is required by the design. This means the currents that determine the noise, slew rate and loop gain and the voltages to keep the devices in their linear range.

Two main techniques can be used in biasing:

- feedback
- feedforward

Feedback can be over all stages multiple stages or locally. Since the amplifier needs to operate from DC it's not possible to use filtering in the feedback network to differentiate between the gain setting and biasing.

Feedforward can be implemented by setting V_{GS} or I_B by a trimmer and correct for temperature drift. The large spread of both V_{TH} and H_{FE} makes it impossible to use predetermined settings. Aging might require retrimming. The behavior depends on how well the temperature correction works and how much the drain or collector current may vary without problems. This is less favorable than feedback.

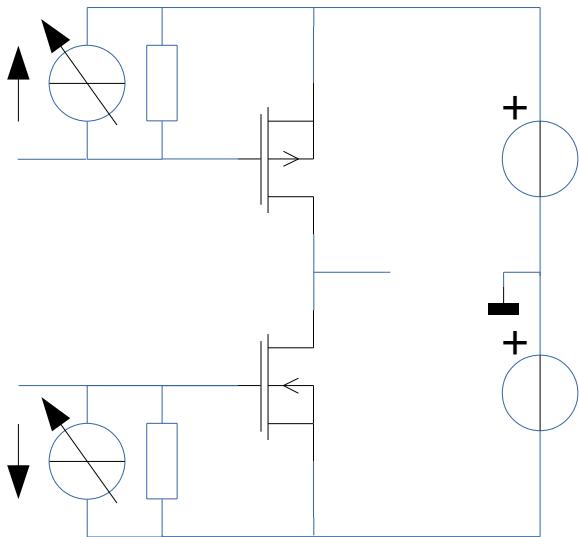
Starting from the output where the signal amplitude is the highest. The goal is to get enough voltage range to deliver current to the gradient coil and guarantee a minimum g_m with the bias current.

Having feedback on the I_D bias current is preferred but is difficult to achieve in this case. The current can range over a factor 400. A small sense resistor is required to keep its dissipation low at maximum current. A sense resistor of about $5\text{m}\Omega$ would be practical, but at 38mA only $190\mu\text{V}$ is available as feedback signal. However the same goes for the current amplifier feedback.

The bias current doesn't need to be accurate. A range of $40\text{mA} \dots 250\text{mA}$ would be acceptable. The other option is feedforward biasing of the MOSFETs by setting V_{GS} of each FET. This can best be done relative to the power supplies as the sources are connected to them. Voltage fluctuations will have no influence this on the biasing this way.

* The importance of equal V_{CE} and I_C in the differential stage wasn't recognized here which led to a dependence of the gain stage on the supply voltage.

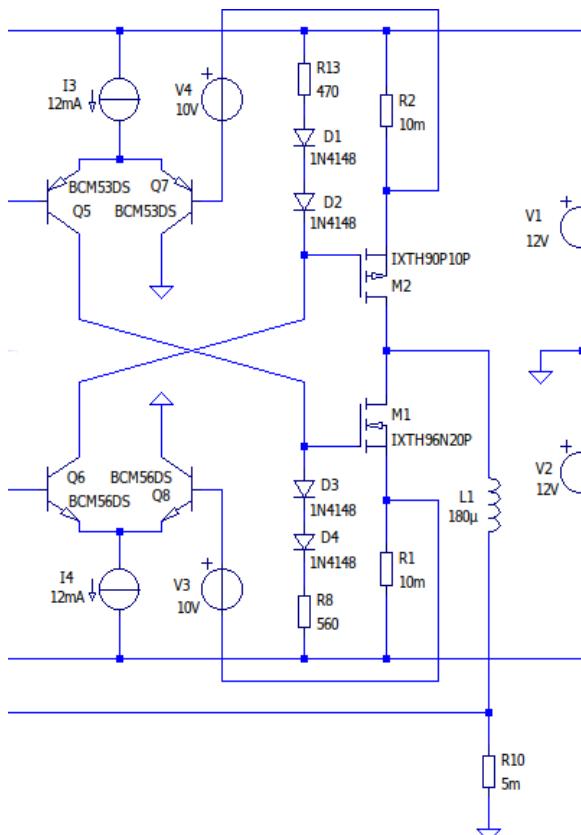
V_{GS} can be made by running a current through a resistor parallel to G-S or by a voltage source with a series resistor at the same location. These are equivalent of course. Temperature compensation can be implemented by using diodes or an NTC.



The supply voltage required to meet the specification for the slew rate of 15A in 50 μ s at 180 μ H is ± 54 V. A lot of power would be dissipated and the power supplies must be able to deliver 3 x 810W. This makes the design expensive and hard to keep cool. ± 15 V is a more practical supply voltage or a bit lower for battery power. The result is a longer rise time for large steps.

The current sources could be the collector outputs of two CE gain stages in stead of a single one. V_{GS} is about 5V and the earlier chosen bias current for the gain stage is 5mA, which makes the GS-bias resistors 1k Ω .

- ➔ Cross coupling the MOSFETs stabilizes the bias current at the cost of reduced linearity. When current is flowing in one of the MOSFETs the other ones current will be proportionally reduced until it reaches zero.



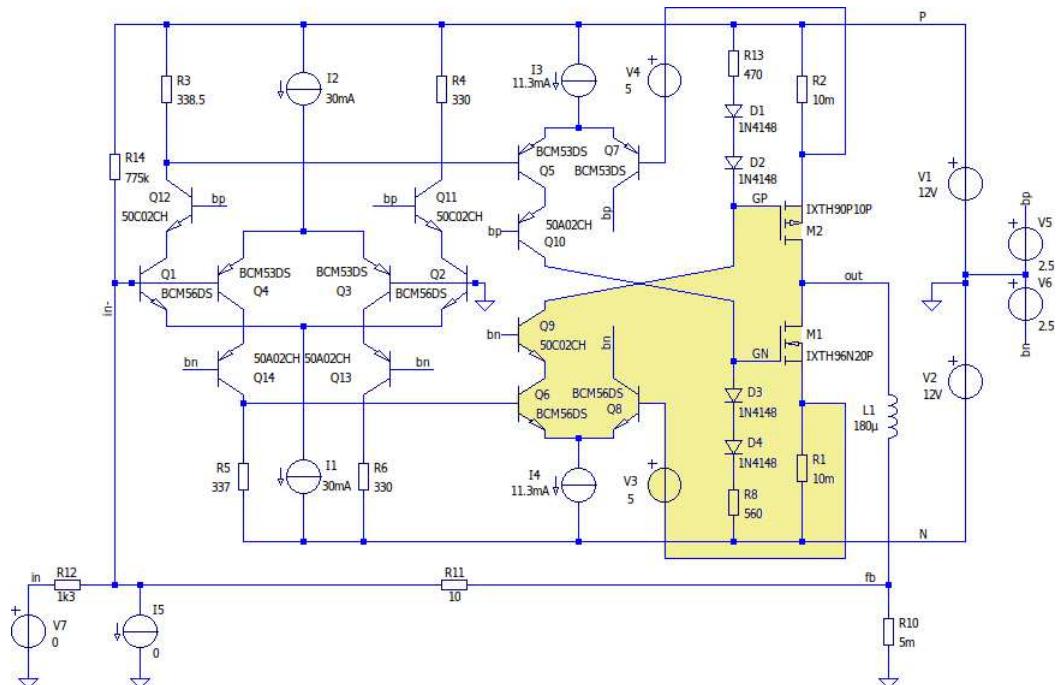
A differential stage is chosen to drive the MOSFETs in stead of a common emitter stage. This halves the loop gain but it also reduces the sensitivity to temperature changes of the collector current.

The gate resistors have been about halved to make it less likely that the dV/dt at the output will turn on both MOSFETs at the same time. This lower resistance requires more current for the same voltage, but by adding two diodes in series this is partly compensated.

- ➔ The diodes also add $-4\text{mV}/^\circ\text{C}$ feedforward temperature compensation which is about right for the MOSFETs. Thermally coupling them to the 10m Ω sense resistors implements indirect thermal feedback too.

Current sources I_3 , and I_4 should be temperature independent or else the sum of the currents should remain constant to prevent the class AB bias point from drifting. In the last case 10% change of current is no problem, but when only one current source drifts it should be less than 1%.

Higher bias voltages V_3 , V_4 reduce the dissipation in the transistors, but also require higher precision or relative stability. Maybe extra resistors or CB stages should be used instead of a high reference voltage. A 10V reference should stay within 1mV drift for acceptable change in the quiescent point. This is 10^{-4} or 20°C temperature change at $5\text{ppm}/^\circ\text{C}$. Opposite drifts of the voltage sources cancel here too, but it's unlikely to happen. At 5V reference voltage the acceptable change still is 1mV but then 40°C temperature change is allowed at the same drift rate.



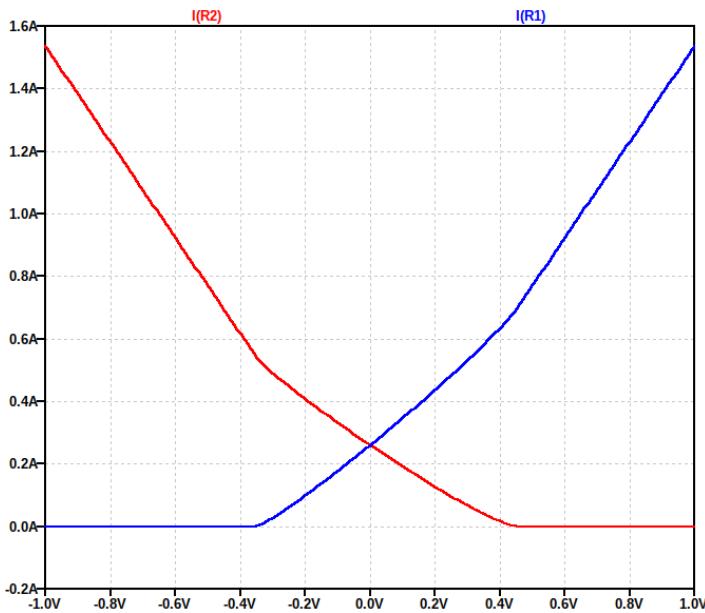
→ A double differential input stage takes care of driving both halves of the gain stage. Offset trimming is done by R_3 and R_5 which also sets the quiescent current for the MOSFETs. When both halves of the amplifier are active this should reduce the noise by 30%.

The colored area acts as a voltage controlled current amplifier when both FETs are active. The

input voltage is across R_5 . R_1 is the feedback resistor. Its loop gain is only about 1 so it doesn't accurately set the desired current but that is taken care of by the outer loop. At zero output all of the current through M_2 is going through M_1 because of the outer loop. When M_2 is turned off because the outer loop does so, the local feedback loop is broken and M_1 is not controlled by V_{R_5} anymore. A mirrored loop is formed with the PNP transistors of the gain stage. This means that the quiescent current through the FETs is set by V_{R_5} and V_{R_3} .

Having a larger V_{R_5} means that the absolute voltage drift over temperature is larger. This drift is coupled to R_1 . Lowering V_{R_5} makes the quiescent point less sensitive to temperature mismatch. So maybe an even lower reference voltage should be used.

This plot shows how the current through the FETs vary with V_{in} . Around 0V when both FETs are conducting the influence of the cross coupled current control is visible.

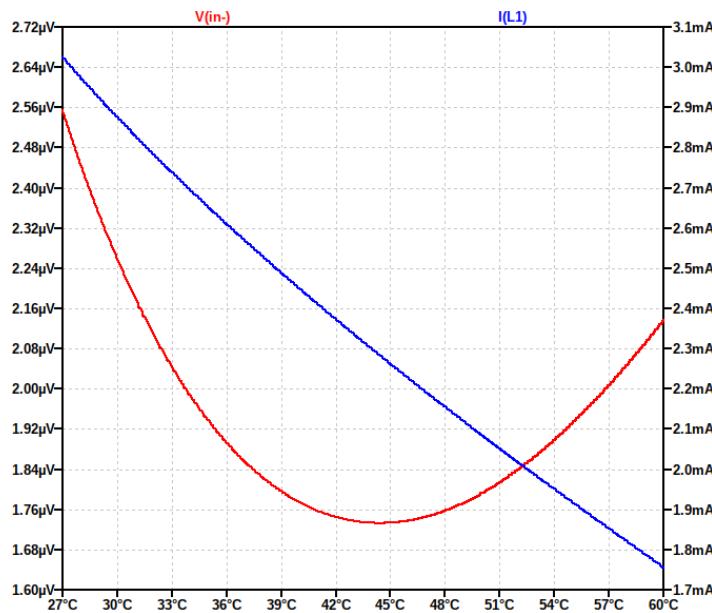


Both the center point and the quiescent current are set by trimming R3 and R5. In this case it could have been tuned to a bit lower current but this shows the cross coupling effect more clearly.

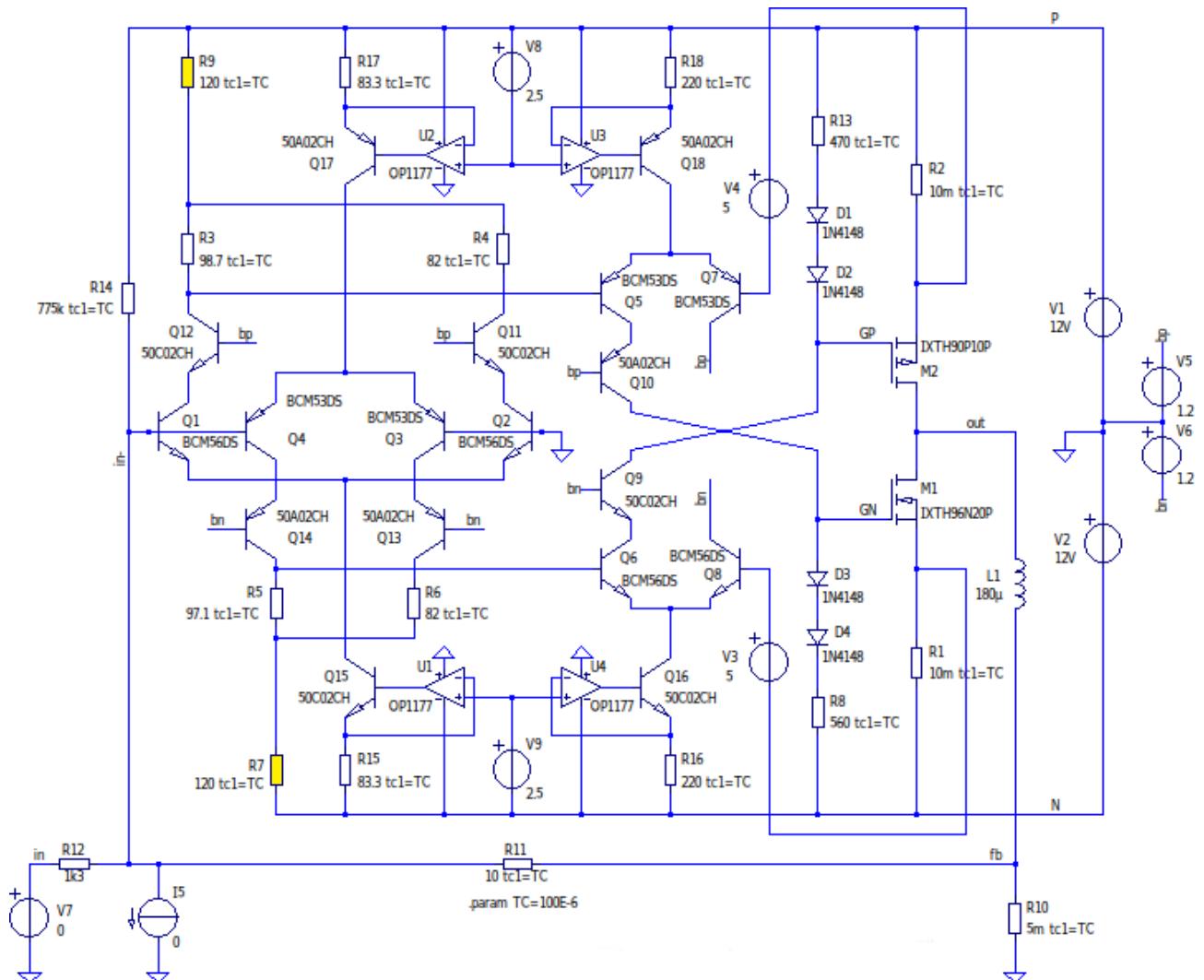
Stability of current sources I_1, I_2 is critical for the input offset voltage and the output current it causes. It helps if both currents drift the same way, but that increases the quiescent current of the MOSFETs rapidly. 0,1% drift is just acceptable.

- Temperature changes should be symmetrical at both sides of the input stage. This only helps if the temperature coefficients are equal. So the trimming potentiometer should be carefully chosen.

The highest sensitivity to temperature differences is from the input transistors that form the actual DV stage. A change of 0,1°C is already enough for 0,7A extra quiescent current in the MOSFETs. As mentioned before in 3.2.1 this causes input offset voltages of 2 or 3 orders higher magnitude per ΔT between the positive and negative input transistors than would occur when both transistors undergo the same ΔT . This was a reason for two matched transistors in a single package. Extra care should be given to the thermal design of the PCB.



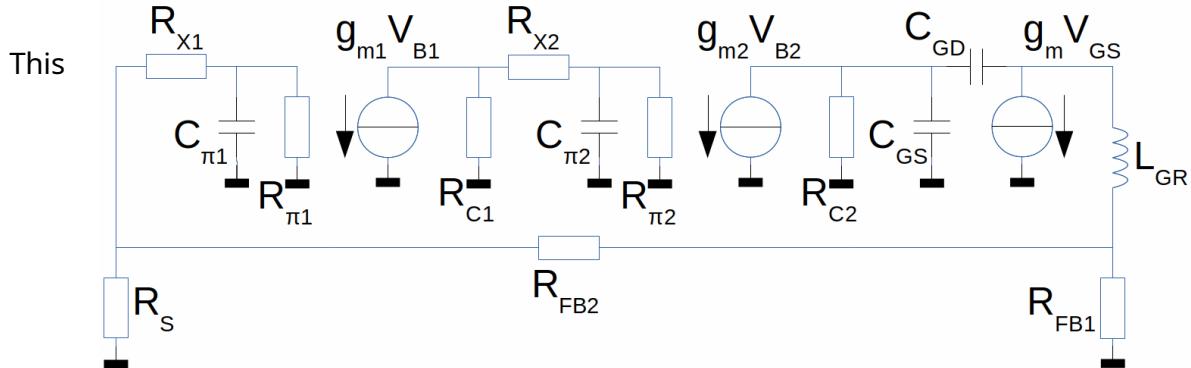
After trimming of the input offset voltage the drift of the output current becomes very low in a simulation where all components have an equal temperature.



V_5, V_6 have been lowered to 1,2V to reduce the temperature rise of the input transistors. R_7 , and R_9 create a constant voltage drop to make the quiescent current of the MOSFETs less sensitive to unequal temperatures, and therefore I_C , of the input transistors. This way V_5, V_6 don't have to be lowered even more. 100 ppm/ $^{\circ}\text{C}$ resistors seem good enough for temperature stability. This means that the TC of the trimmers can match that of the fixed resistors since these are typically 100ppm/ $^{\circ}\text{C}$. However the drift is $\pm 100\text{ppm}/^{\circ}\text{C}$, and could be opposite for the trimmer and the fixed resistors

- Using components with a better temperature stability is preferred.
- Thermal performance is something to consider in the layout
- The maximum range of the trimmer should be kept small to reduce its absolute contribution to the drift.

3.2.5 Frequency Compensation



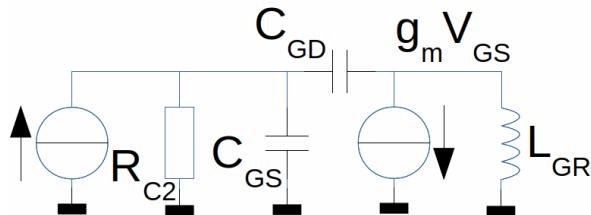
simplified model of the uncompensated amplifier still captures the important elements that determine the frequency behavior. The gradient coil which is actually an LCR combination will be modeled as a pure inductance. The differential input and gain stages are each represented by a single BJT model but with half the C_π and double the R_π for the gain stage. The input stage consists of 4 BJTs in 2 parallel pairs.

A single MOSFET is active at a time, so one or the other should be used here. The C_μ 's of the BJTs have been left out to keep the model simple since their influence is limited by the CB stages that follow the differential amplifier stages.

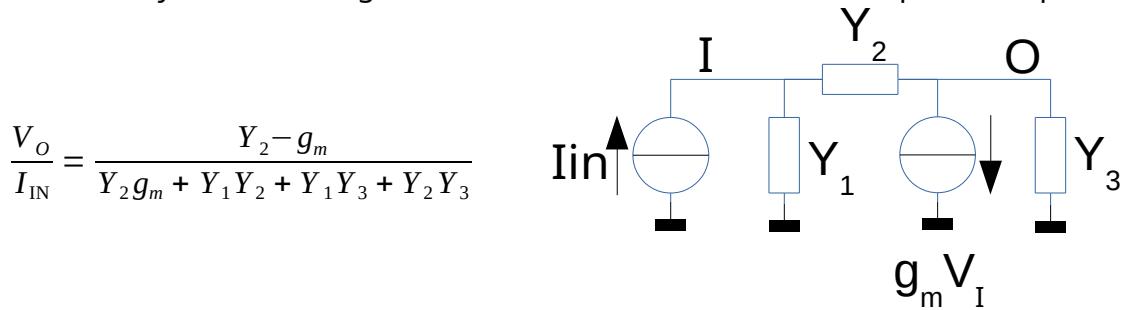
$$R_\pi = \beta \frac{kT}{qI_C} \quad C_\pi = \frac{qI_C}{2\pi f_T kT} \quad g_{m1,2} = \frac{1}{2} \frac{qI_C}{kT} \quad g_m = \sqrt{2kI_D}$$

R_{x1}	9Ω	R_{x2}	18Ω
$C_{\pi 1}$	795pF	$C_{\pi 2}$	160pF
$R_{\pi 1}$	217Ω	$R_{\pi 2}$	1,1kΩ
β_1	130	β_2	130
R_{C1}	100Ω	R_{C2}	500Ω
		L_{GR}	180μH; 0,4Ω; 130pF
C_{GS}	5nF	R_{FB1}	5mΩ
C_{GD}	500pF	R_{FB2}	10Ω
g_m	25	R_s	1,3kΩ

Starting with the transfer function of the output stage, this is the part that matters.



Breaking the circuit down into admittances gives a universal transfer function that can be relative easily altered for a gradient coil with series resistance and parallel capacitance.

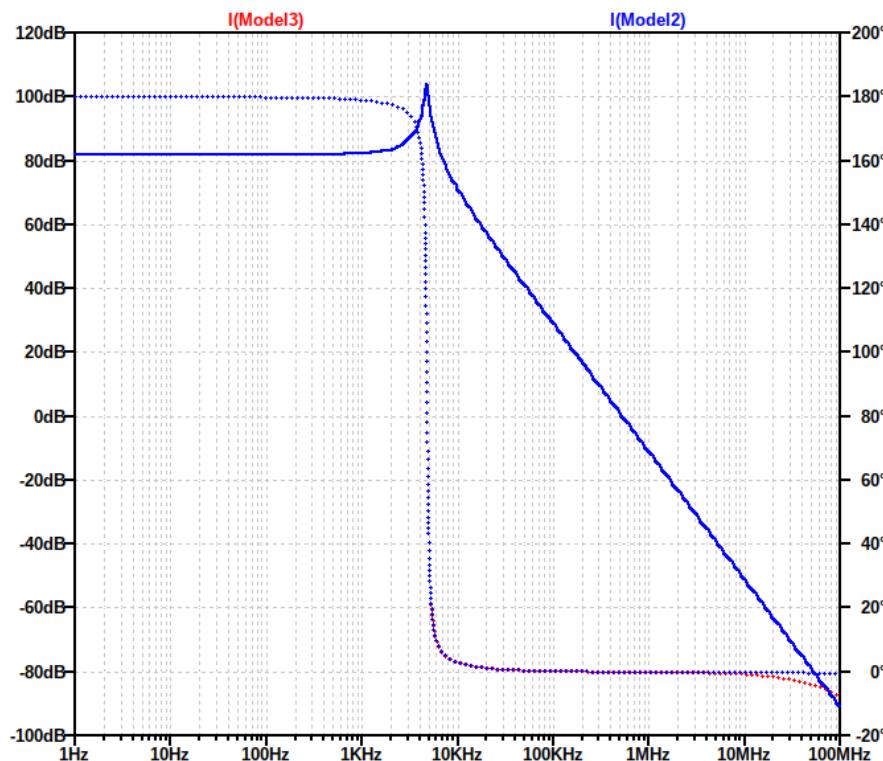


For an ideal gradient coil without resistance and capacitance this becomes:

$$\frac{V_o}{I_{IN}} = \frac{s C_{GD} - g_m}{s C_{GD} g_m + \left(\frac{1}{R_{C2}} + s C_{GS} \right) s C_{GD} + \left(\frac{1}{R_{C2}} + s C_{GS} \right) \frac{1}{sL} + \frac{C_{GD}}{L}}$$

$$\frac{I_o}{I_{IN}} = \frac{s^2 [R_{C2} L C_{GD}] - s [R_{C2} L g_m]}{s^3 [C_{GS} C_{GD} R_{C2} L] + s^2 [C_{GD} L (g_m R_{C2} + 1)] + s [R_{C2} (C_{GD} + C_{GS})] + 1} \cdot \frac{1}{sL}$$

The third order term is very small and only becomes relevant at very high frequencies. This is shown in the plot below with the 3rd order model in red and the 2nd order in blue.



The peaking in the loop gain because of LC resonance isn't something to worry about too much. It adds loop gain and therefore accuracy. However the phase change it causes is 180° because of the two poles, so at least one compensating zero is required for stability. These poles are the dominant poles of the loop.

$$H_o(s) = \frac{I_o}{I_{IN}} = \frac{s[R_{C2}C_{GD}] - R_{C2}g_m}{s^2[C_{GD}L(g_mR_{C2}+1)] + s[R_{C2}(C_{GD}+C_{GS})] + 1} \quad (\text{2nd order output stage model})$$

$$P_{1,2} = \frac{-R_{C2}(C_{GD}+C_{GS}) \pm \sqrt{[R_{C2}(C_{GD}C_{GS})]^2 - 4C_{GD}L(g_mR_{C2}+1)}}{2C_{GD}L(g_mR_{C2}+1)} \quad P_{1,2} = -0,2 \pm j4,7 \text{ kHz}$$

$$Z_1 = \frac{g_m}{C_{GD}} \quad Z_1 = 8 \text{ GHz}$$

The zero is in the right half of the s-plane but too far away from the poles to cause problems.

Continuing through the feedback network to the input stage by inspection.

$$H_I(s) = -\frac{1}{s[C_{\pi 1} \cdot (R_{\pi 1} / (R_{X1} + (R_{FB2} / R_S))) + 1]} \cdot \frac{R_{FB1}}{R_{FB1} + R_{FB2} + (R_S / (R_{X1} + R_{\pi 1}))} \cdot \frac{R_S}{R_S + R_{X1} + R_{\pi 1}} \cdot \frac{\beta_1}{2}$$

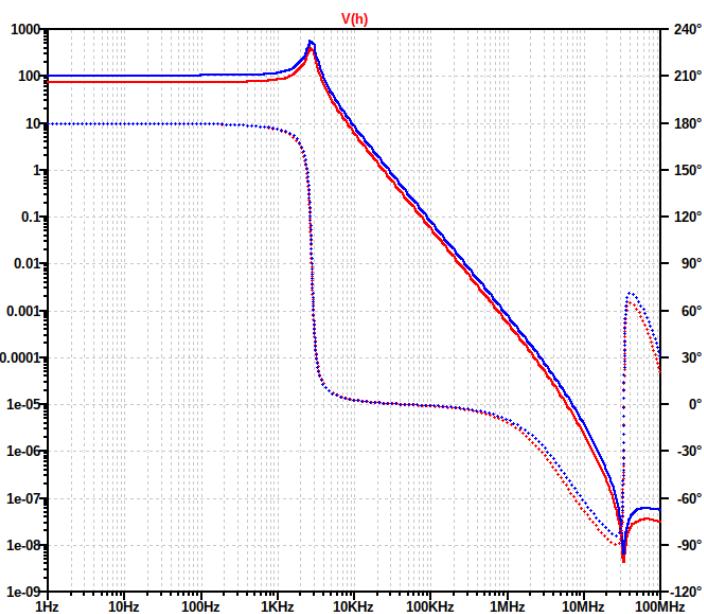
$$P_3 = -11,5 \text{ MHz}$$

And in the same way onto the gain stage.

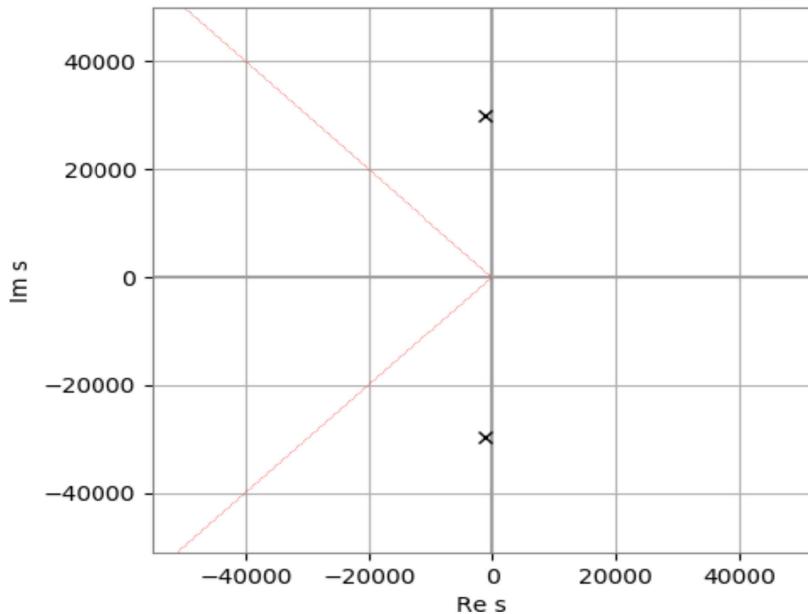
$$H_G(s) = -\frac{1}{s[C_{\pi 2} \cdot (R_{\pi 2} / (R_{X2} + R_{C1})) + 1]} \cdot \frac{R_{C1}}{R_{C1} + R_{X2} + R_{\pi 2}} \cdot \frac{\beta_2}{2}$$

$$P_4 = -9,3 \text{ MHz}$$

Filling in $s=0$ in the cascaded transfer functions $H_I H_G H_O$ results in the loop gain $L = -91$. This is lower than the intended 100 at minimum output current, but it's the result of previously made choices about thermal stability and anticipated insensitivity to high dV/dt that could turn on the MOSFETs and cause short circuiting of the power supply. Later on in the design when this is investigated it can be seen if the loop gain can be increased a bit by increasing the gate-source resistors. This would mean an iteration step.



This is a spice simulation of the open loop transfer of the biased amplifier from the previous design step. The settings that were used:
 $I_o = \pm 15A$, $L = 180\mu\text{H}$, $\text{ESR} = 0,4\Omega$
This shows that P_3 and P_4 aren't dominant poles and can be ignored in the frequency compensation. Only $P_{1,2}$ need to be considered.



These are the relevant poles that need to be moved in a better position.

For a range of $10\mu\text{H} < L < 1\text{mH}$ with varying ESR too the important thing is stability and not so much the location of the poles. Therefore at the extreme of 1mH and no ESR, Butterworth position will be designed so that for lower L values the amplifier will behave more like a first order system.

The real and imaginary part must be made equal at $L = 1\text{mH}$ for Butterworth poles. The preferred way to do this is by a phantom zero. This moves the poles without the zero showing up in the closed loop transfer.

When the forward path A is defined as the dominant transfer of the open loop

$$A = \frac{91}{as^2 + bs + 1} \quad \text{with} \quad a = C_{GD} L (g_m R_{C2} + 1) \quad \text{and} \quad b = R_{C2} (C_{GD} + C_{GS})$$

And the phantom zero in the feedback path $B = \tau_z s + 1$

Then the closed loop transfer of the amplifier becomes.

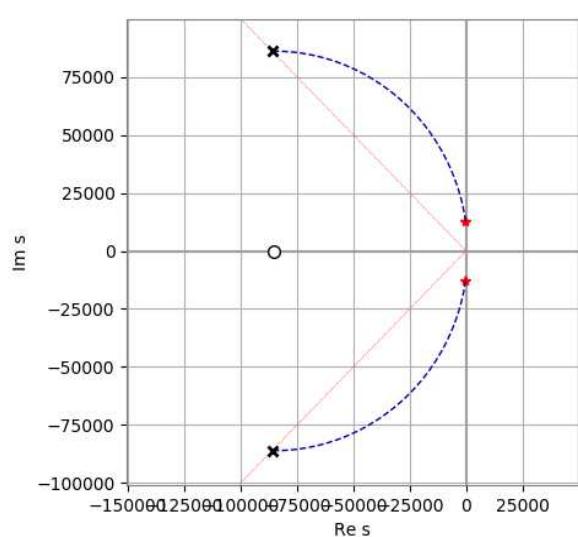
$$H_{CL} = \frac{91}{as^2 + (b + 91\tau_z)s + 92}$$

$$\begin{aligned} &-2.129e-14 s^2 + 0.001065 s + 90.61 \\ &1.475e-24 s^4 + 1.931e-16 s^3 + 6.251e-09 s^2 + 0.001067 s + 91.61 \end{aligned} \quad @ \text{gain} = 1.0$$

Time constant τ_z can then be found by

$$\tau_z = \frac{\sqrt{2 \cdot 92a} - b}{91} \quad \tau_z = 11.75\mu\text{s}$$

- The best implementation of the phantom zero is an inductor in series with R_{FB1} because a lot of attenuation can be undone over there. Also high frequency noise will have a lower gain because of that inductor.



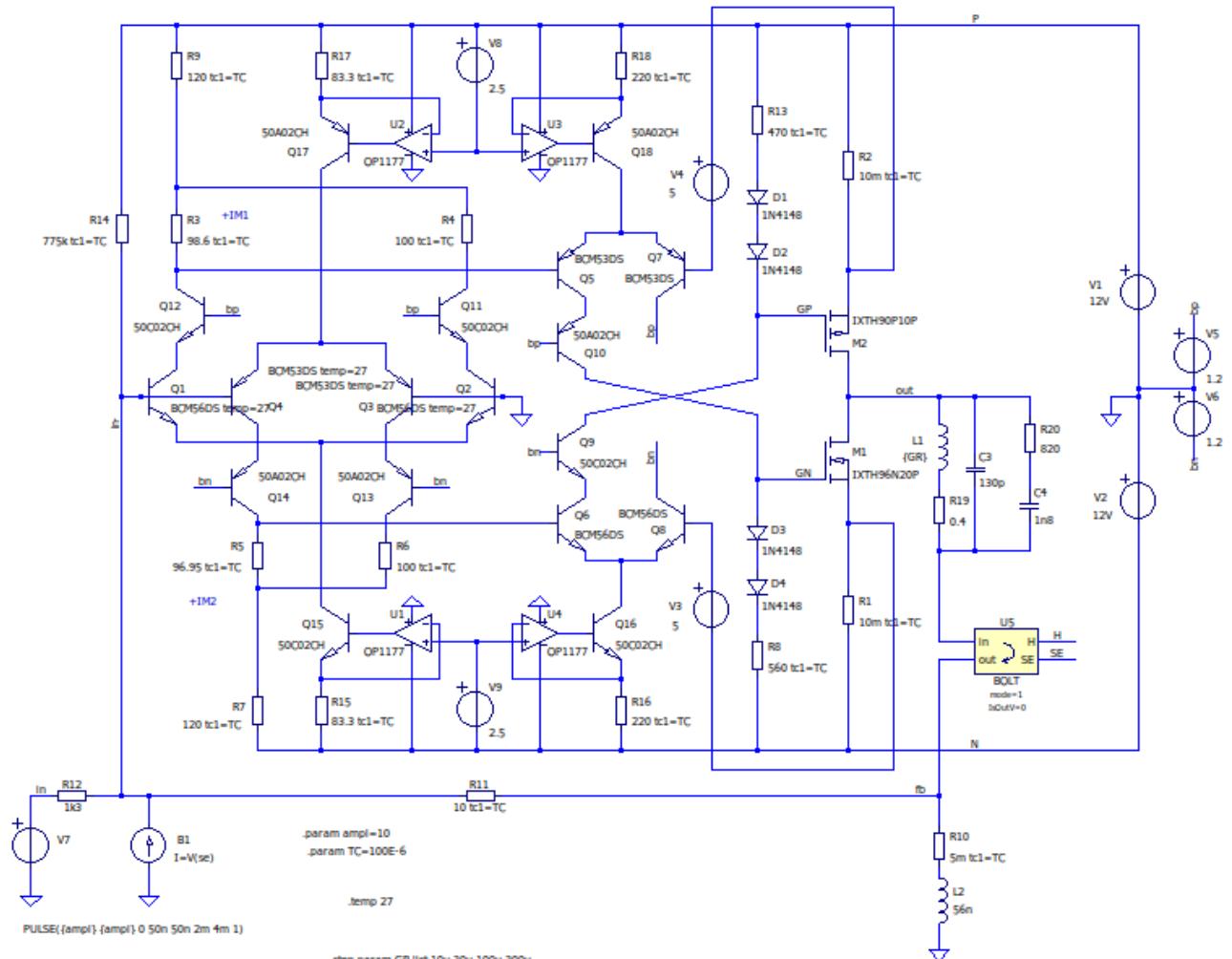
Finally the self resonance of the gradient coil with parasitic parallel capacitance needs to be damped. This can be done by a parallel damping resistor.

$$R_{damp} = \sqrt{\frac{L}{2C}}$$

And to prevent DC current through R_{damp} a blocking capacitor should be placed in series such that at a decade lower frequency than the resonance frequency it starts to have influence.

$$C_{block} \geq \frac{10}{2\pi f_{res} R_{damp}}$$

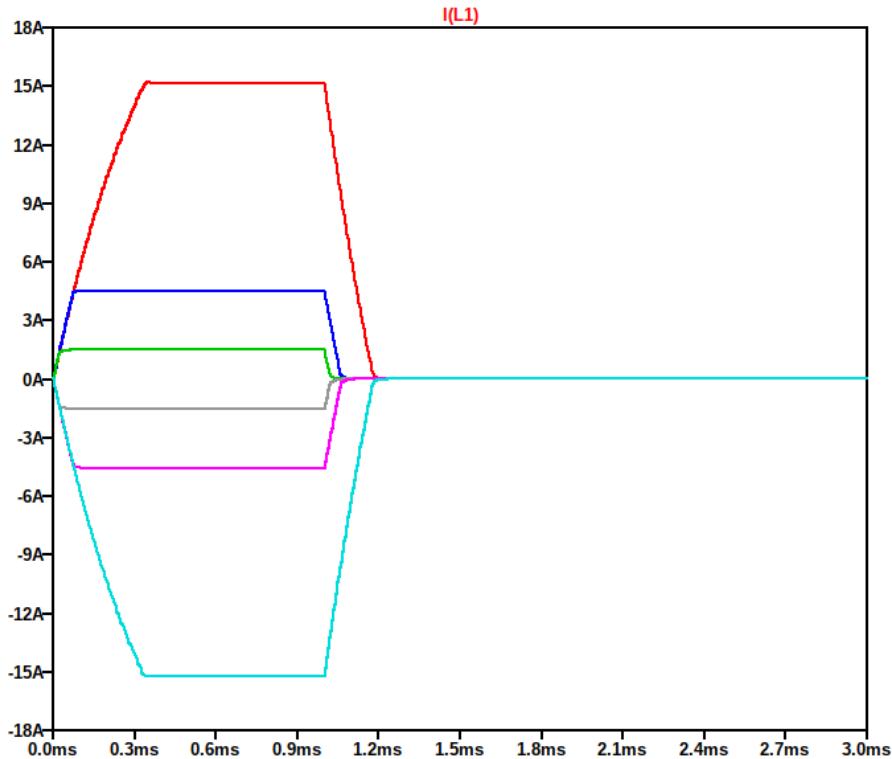
The dominant parallel capacitance comes from the C_{oss} of the MOSFETs and not just C_3 in this circuit. $\rightarrow R_{damp} = 200\Omega$, $C_{block} = 100nF$.



$L_2 = 64nH$ creates the phantom zero. R_{20} and C_4 is the damper for self resonance. U_5 is a tool that can break the loop to measure the loop gain.

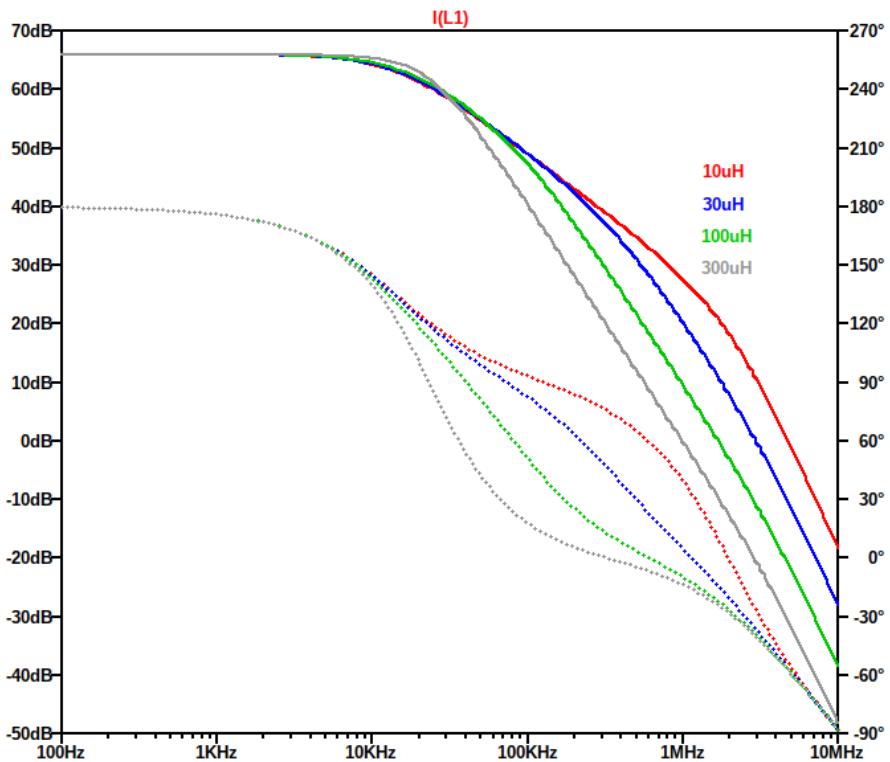
3.2.6 Verification by Simulation

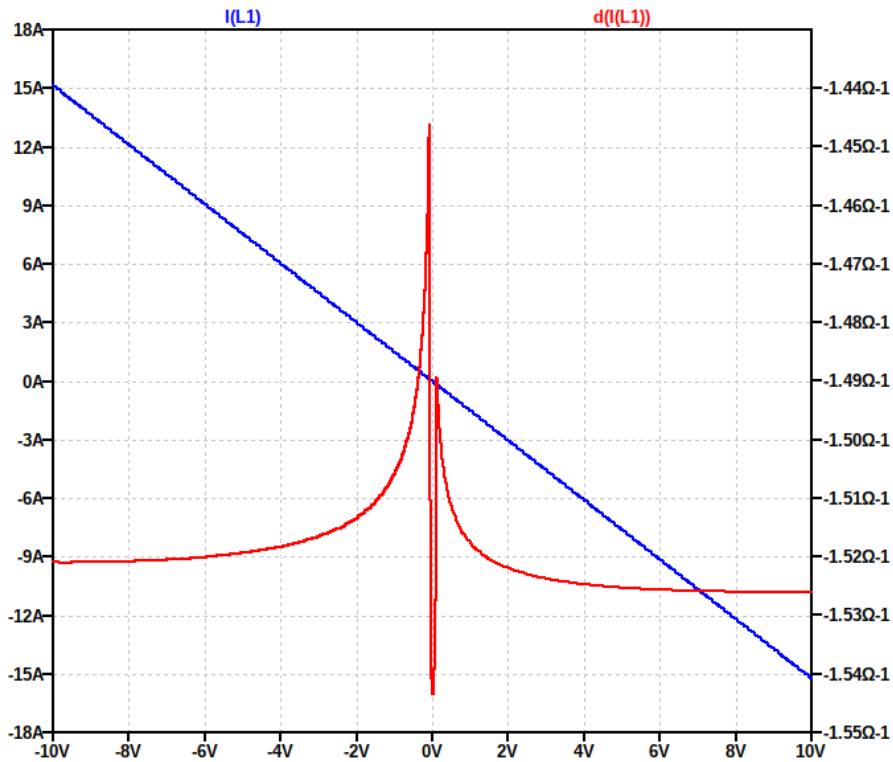
This is the closed loop frequency behavior of the amplifier with frequency compensation for several gradient coil inductances.



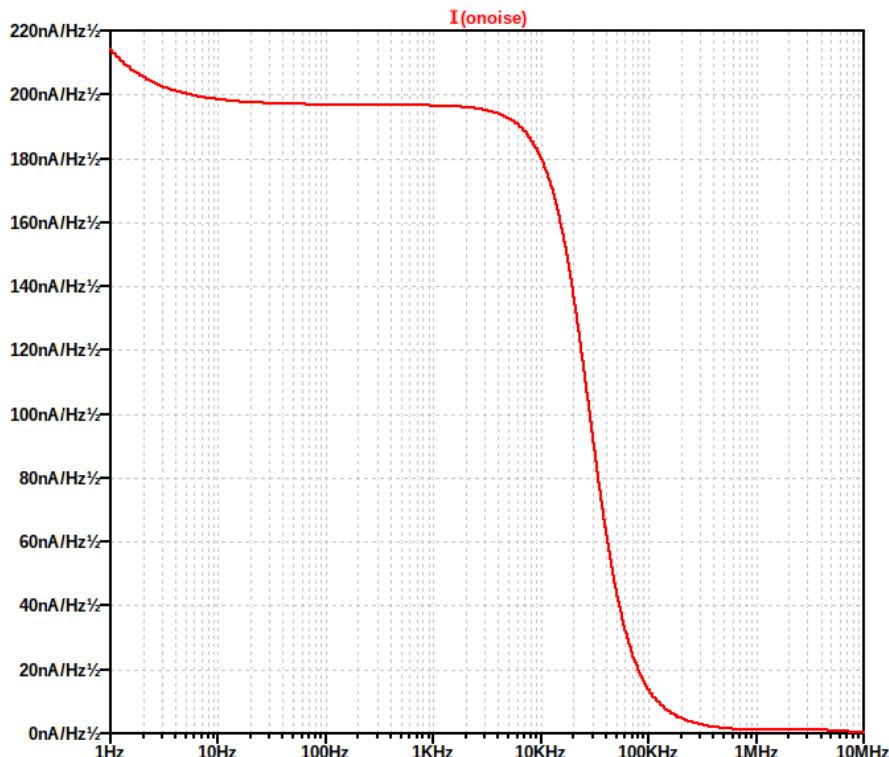
To add more attenuation for high frequencies a capacitor of 150nF and a series damping resistor of $0.1 \dots 1\Omega$ can be placed in parallel with RF_2 .

The step response for $180\mu\text{H}$ shows that the slew rate dominates the pulse shape for larger steps.



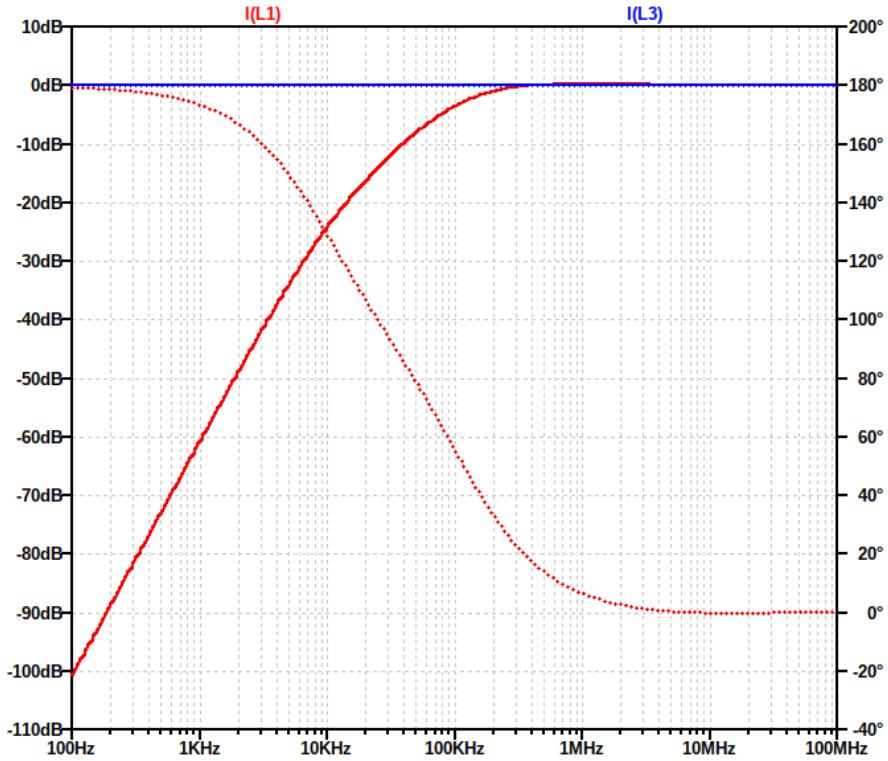


Linearity decreases near 0V input voltage as expected because of reduced loop gain.

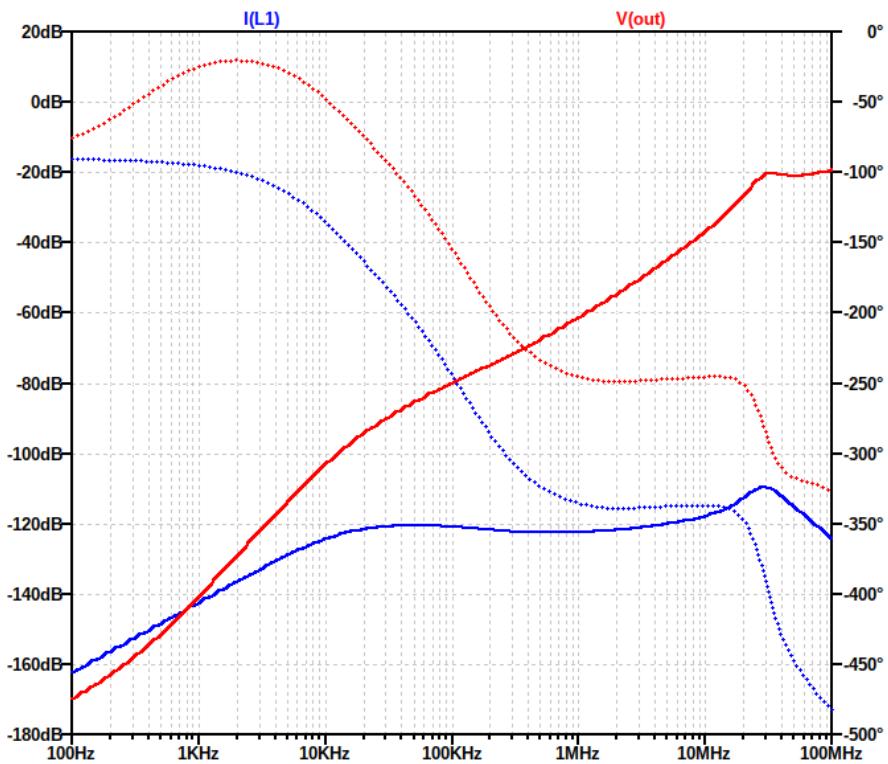


0,4nA/ $\sqrt{\text{Hz}}$ @ 2MHz (inductive part). The almost 200nA/ $\sqrt{\text{Hz}}$ is notably more than the expected 152nA/ $\sqrt{\text{Hz}}$ and is caused by the op-amp noise of the current sources of the DV stages. Noise of the voltage reference sources isn't even included and can easily dominate. More attention needs to go to the bias current sources.

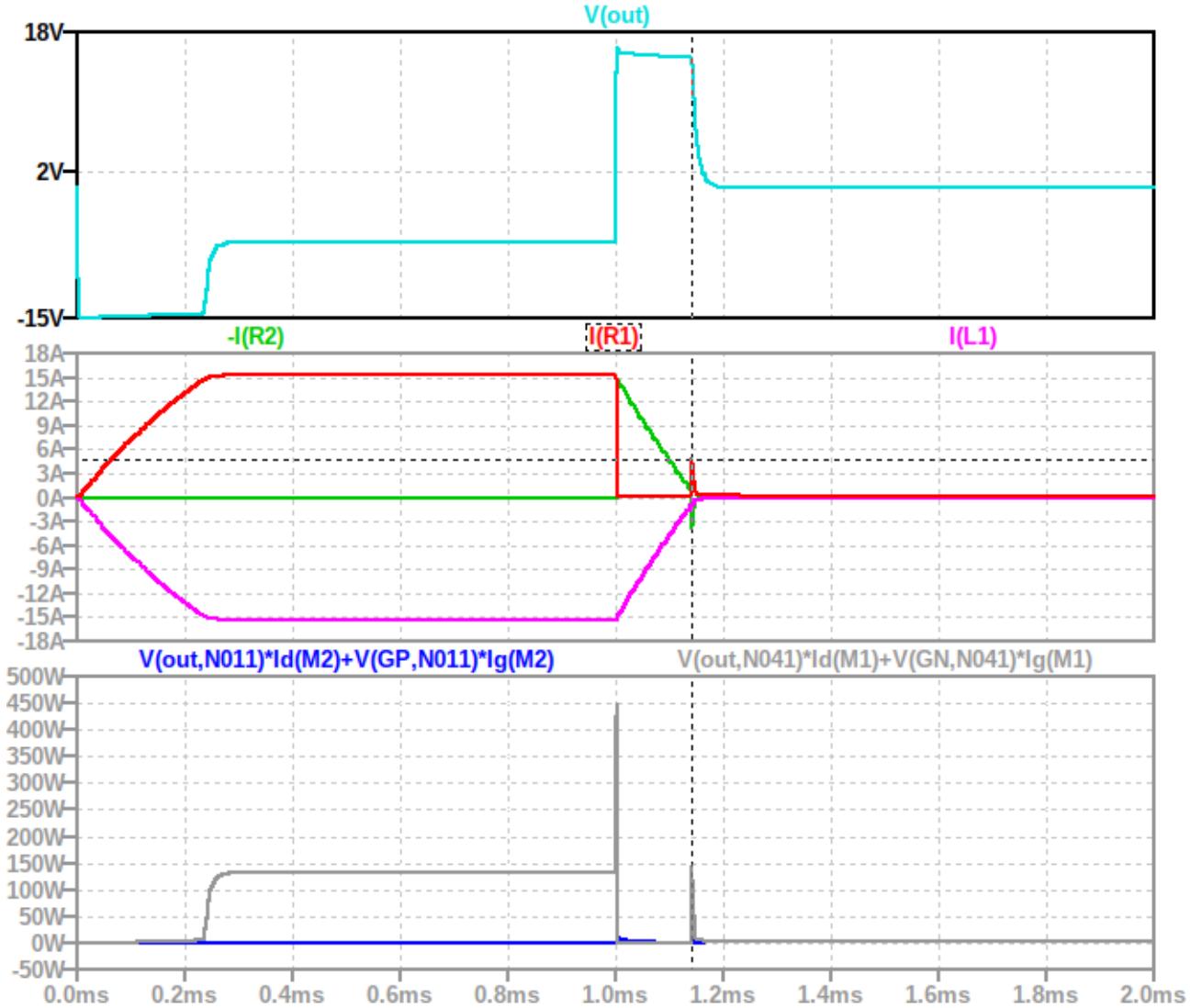
The coupling factor between the gradient coils was measured to be almost zero, but if the coils would couple this would lead to the following suppression. L3 couples to L1 with $k=1$. Of course once the output is clipping the isolation will drop.



The capacitance between the gradient coils was measured to be 700pF which is remarkably high. Introducing a voltage coupling via 700pF to the output of the amplifier results in the following suppression.



The output stage has the risk that both MOSFETs are switched on simultaneously because of a high dV/dt at the drains. This happens when current is flowing back into the power supply and then stops, shown at the position of the cursor. At that moment the output voltage suddenly changes to another value which causes a current through the C_{GD} of both FETs. This current turns into a voltage by the driving impedance at the gates of the FETs.



R1 and R2 are the current sense resistors in series with the FETs. L1 is the gradient coil. At the position of the cursor a short current spike occurs. The amplitude is limited by the design of the output stage which suppresses this.

The bottom grey plot shows the power dissipation of the N-FET M1. The larger spike at $t=1\text{ms}$ is $593\mu\text{J}$ and happens because the output voltage changes from -6V to $+15\text{V}$ while current keeps flowing through M1. Then once the body diode of P-FET M2 starts to conduct the current flow starts to change from M1 to M2. After a while when the current through L1 approaches zero another power spike occurs which is from the earlier described dV/dt . The energy content of that pulse is $597\mu\text{J}$ which is equal to the other pulse.

3.2.7 Revisit of the Input Stage Design

Simulation shows that biasing seems not to be completely independent of the noise as assumed in the noise design step, both for intrinsic noise and drift. Some bias noise sources in the amplifier produce so much noise that the gain of the first stage is not sufficient any more. This requires a second look at the input stage design to:

- Reduce the noise contribution of the biasing
- Improve temperature drift due to incorrect biasing
- Maybe increase gain.

The shot noise in the collector currents is $i_n = \sqrt{2qI_c}$ and at 15mA per BJT gives 100pA/ $\sqrt{\text{Hz}}$ combined. The bias current source should stay below that noise level if possible.

Having just a resistor between the emitters of the DV stage and the power supply would be a great solution for noise.

$$R_{BIAS} = \frac{12V}{30mA} = 400\Omega \text{ which results in } i_n = \sqrt{\frac{4kT}{R}} = 6,4 \text{ pA}/\sqrt{\text{Hz}}$$

However that would make it sensitive to power supply voltage variations. For this reason a current source is required for isolation.

The 83,3Ω resistor that converts the 2,5V reference voltage into 30mA also converts the input noise voltage of the op-amp into a noise current. This sets the limit on the noise voltage to a few nV/ $\sqrt{\text{Hz}}$. Voltage references produce a lot more noise than this, so a low pass filter should limit the noise bandwidth at the input of the op-amp.

The dependence on temperature of the input stage is as follows: $T\uparrow, \beta\uparrow, I_B\downarrow, I_C\uparrow$. This means that the current source at the emitters should compensate for the change of I_B instead of trying to create very constant bias current sources for the DV stage as it was concluded before. See: [Stability of current sources](#)

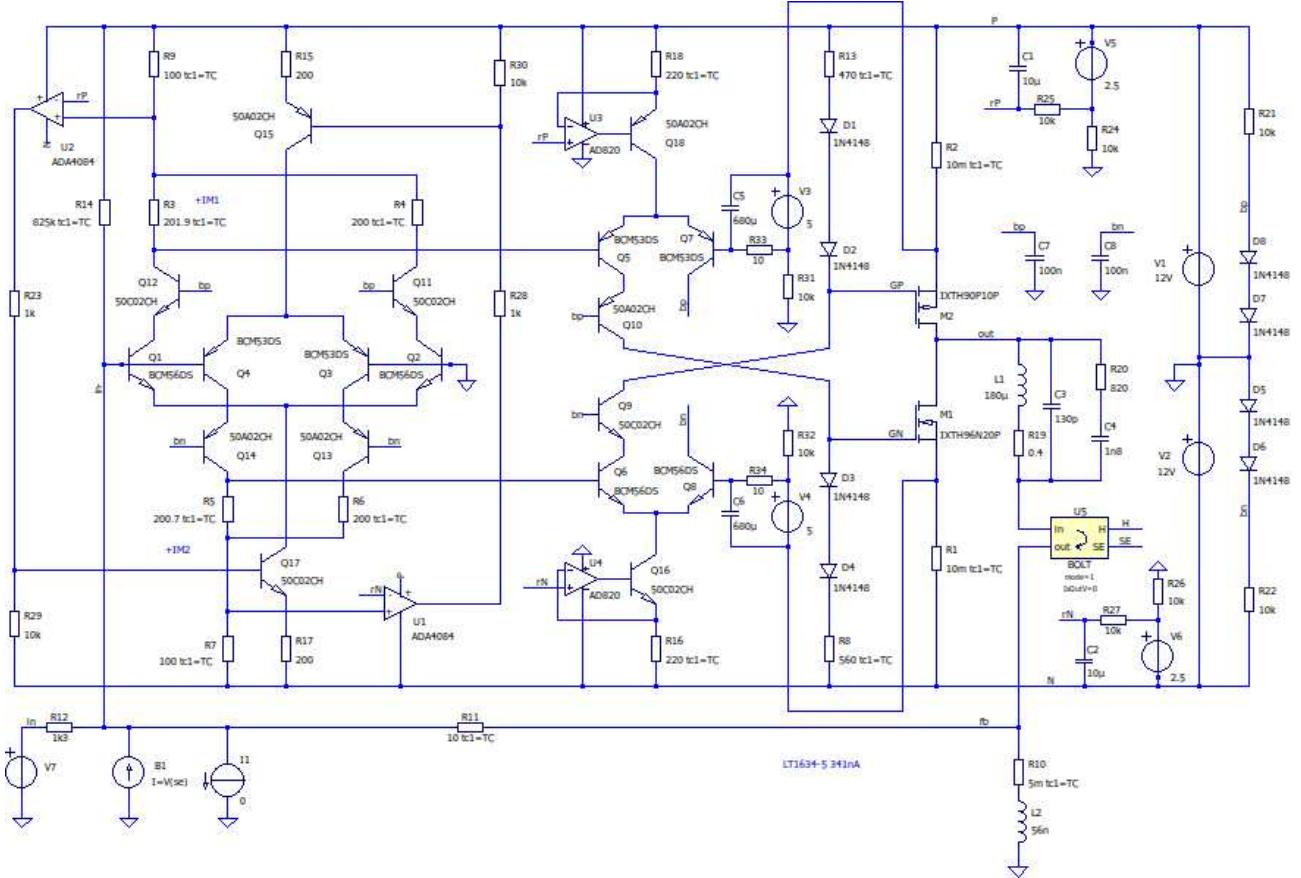
- Therefore the combined collector current should be controlled instead of the emitter current. There is already a resistor present in the DV stage that can be used for this purpose. This makes the output voltage of the DV stage a lot better defined.

A suitable op-amp for this purpose: ADA4084-1, -2, -4

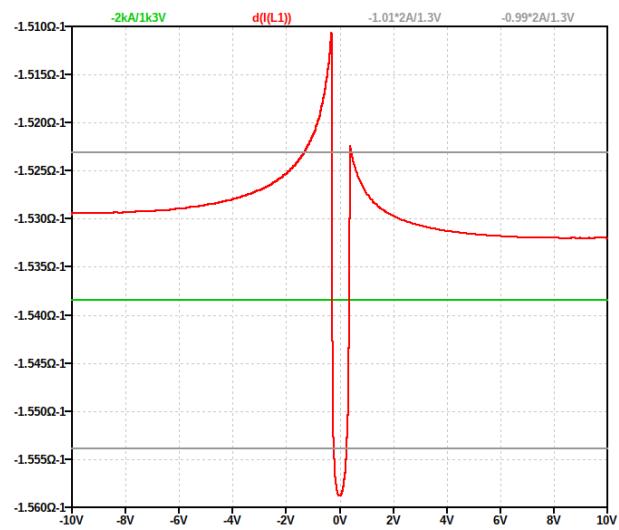
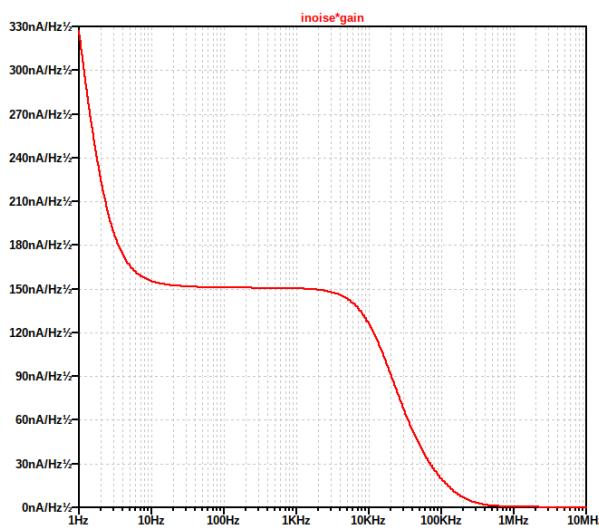
V _{sup}	V _{os}	V _{ni}	V _i range	V _o range	BW	I _{sc}
±3V .. ±15V	20µV typ	3,9nV/ $\sqrt{\text{Hz}}$	±V _{sup}	V _n +0,3 .. V _p -1	13,9MHz	±30mA

When the three collector resistors have equal temperature coefficients and their temperature is coupled then the feedback current source also creates insensitivity to change of the resistances.

- Then there is the noise of the voltage references at the MOSFETs. A LM4040 produces about 300nV/ $\sqrt{\text{Hz}}$. This is present at the input of the gain stage and is so much that after dividing that by the gain of the input stage it still dominates all of the other noise sources. Low pass filtering must take care of this.



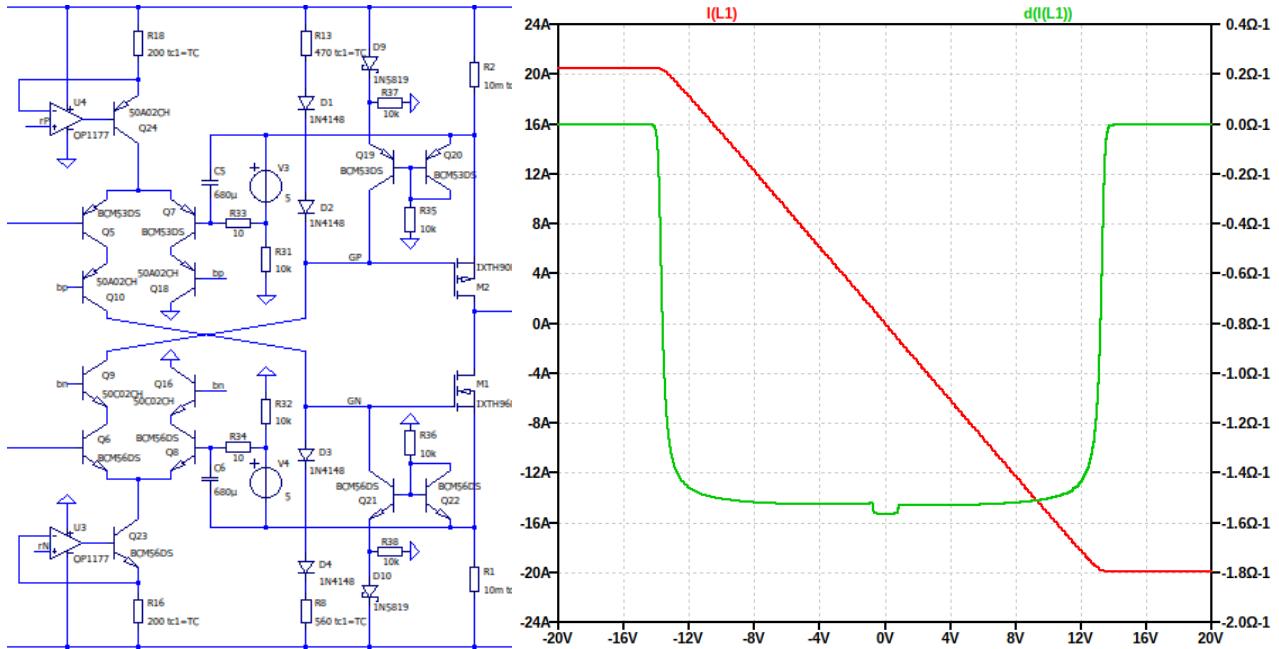
The modified input stage now has active bias control to correct for changing base currents and collector resistances over temperature. The shunt voltage references are filtered to reduce their noise contribution. The lower input noise of the op-amp brings the output noise of the amplifier to the expected level. Linearity has improved too, but the gain still is more than 1% off near the zero crossing. More loop gain is required to solve that. However, it will be left like this.



3.3 Robustness

3.3.1 Overload Protection: Current Limit

The current through each FET is measured at the $10\text{m}\Omega$ source resistors. When that voltage becomes too large a BJT will limit the V_{GS} . A Schottky diode is used as a 0,2V reference to set the current limit at 20A.



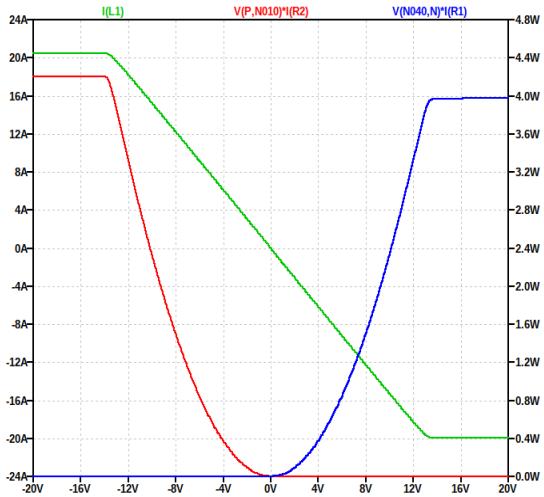
Two CB transistors have been added to improve the temperature stability of the gain stage by keeping both V_{CE} more equal. This helps to keep the quiescent current of the MOSFETs more constant*. The plot on the right shows the output current and its slope against the input voltage.

The current limit doesn't disable the amplifier so it will continue operating when the current drops to a normal level. When too much heat is produced a temperature alarm will disable the amplifier and a restart is required before it can operate again.

* During testing it was found that the ΔV_{BE} was still significantly influencing the MOSFETs bias current. This was because of an imbalance of I_C in each branch of the differential gain stage which causes one BJT to heat up more than the other when the supply voltage changed. Balancing I_C makes them heat up equally. Also the CB bias voltages should have been referenced to the supplies instead of to GND. That would make the dissipated power independent of the supply voltage.

3.3.2 Overload Protection: Temperature Alarm

To prevent overheating due to long periods of high current a temperature alarm will be added. The temperature of the $10\text{m}\Omega$ resistors is used as an indication of the current. Two temperature sensors can be placed near these resistors.



The dissipated power in the $10\text{m}\Omega$ resistors is 2.25W at 15A . The heat that is produced will be transferred to two thermistors that will produce a voltage change.

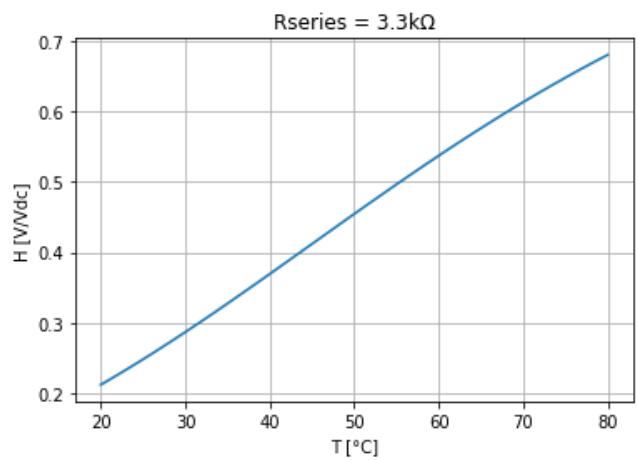
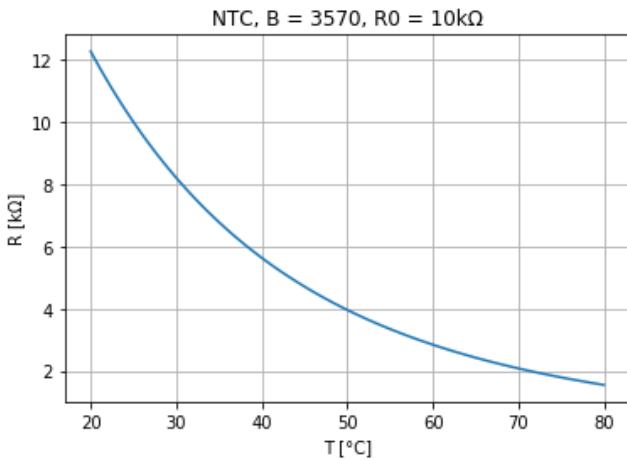
- When the alarm temperature is reached the amplifier will be disabled. The user will have to enable the amplifier before it is possible to use it again. The MOSFETs and resistors must cool down first.

The mathematical model for an NTC

$$\frac{1}{T} = \frac{1}{T_0} + \frac{1}{B} \ln \frac{R}{R_0} \quad \text{or} \quad R = R_0 e^{B \left(\frac{1}{T} - \frac{1}{T_0} \right)} \quad \text{where } T \text{ is in [K]}$$

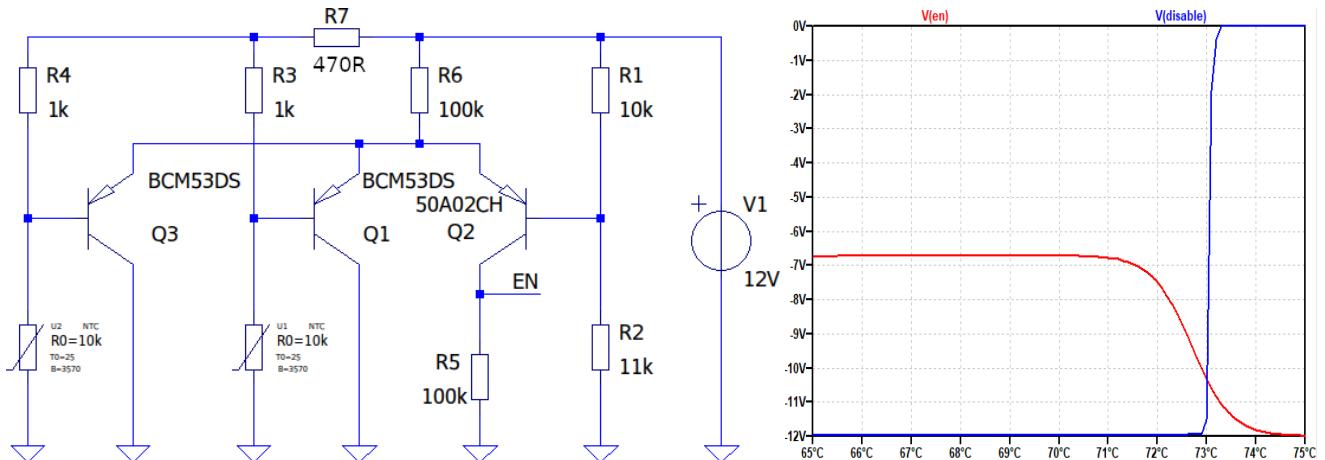
with parameters

B	R ₀	T ₀
3570K	10kΩ	25°C + 273K



The left plot shows how the resistance changes with temperature. The plot on the right is the transfer function of a voltage divider with the NTC connected to a supply voltage and the fixed resistor to GND.

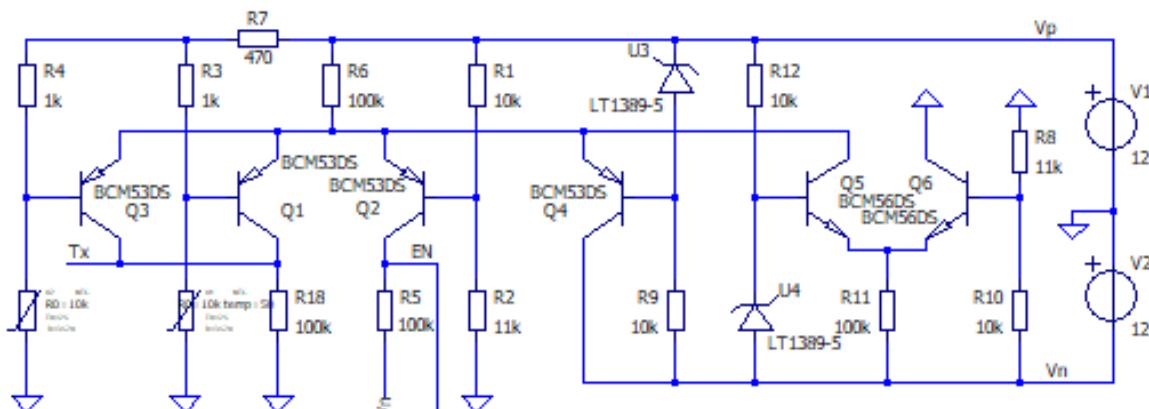
Both source resistors will be monitored. The first one that reaches the maximum temperature will trip the alarm and disable the amplifier. The NTCs will have a thermal coupling with the MOSFETs directly.



This circuit measures two temperatures with NTCs and compares the resulting voltage with the reference that is set by R1 and R2. When one NTC is heated up that will lower the threshold temperature a bit for the other by R7. The EN output goes to zero above the threshold temperature of 72°C. When only one NTC is heated the threshold will be about 2°C higher. More NTCs could be added to this circuit as long as the GND stays isolated from the other amplifiers' GND.

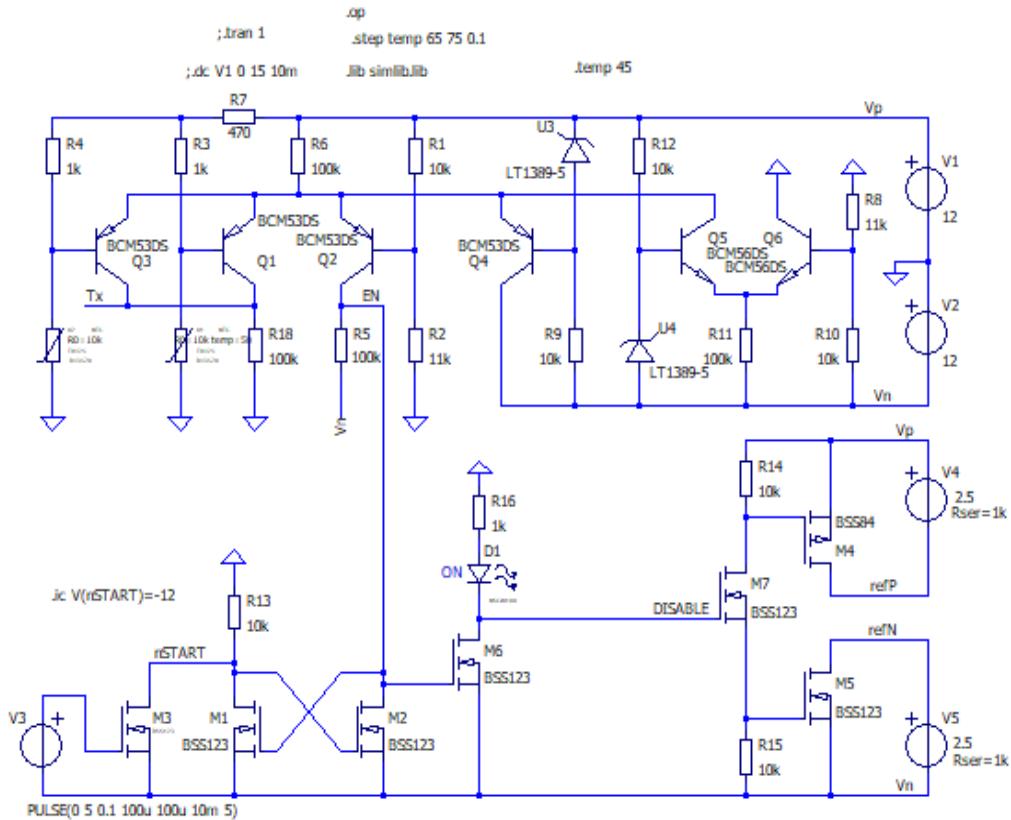
3.3.3 Under Voltage Lock Out

When the voltage of either the positive or negative power supply drops below 10,5V this will also disable the amplifier until the user enables it when the supply voltage is higher than $\pm 10,5V$.

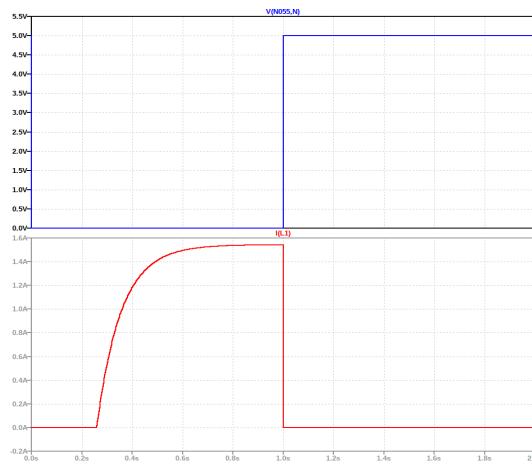


Everything right from Q4 is the UVLO detection for the positive and negative supply voltage. The left part of the circuit is the temperature alarm of one of the channels. Voltage Tx can be used to signal which channel tripped the temperature alarm.

3.3.4 Amplifier Disable



Disabling functionality has been added with $M_{4,5,7}$ that switch off the 2,5V bias voltages of the amplifiers. After enabling the reference voltage rises slowly and creates a soft start for the output stage biasing. A central logic circuit will disable all 3 amplifiers simultaneously when one of them generates a temperature alarm or under voltage lock out.



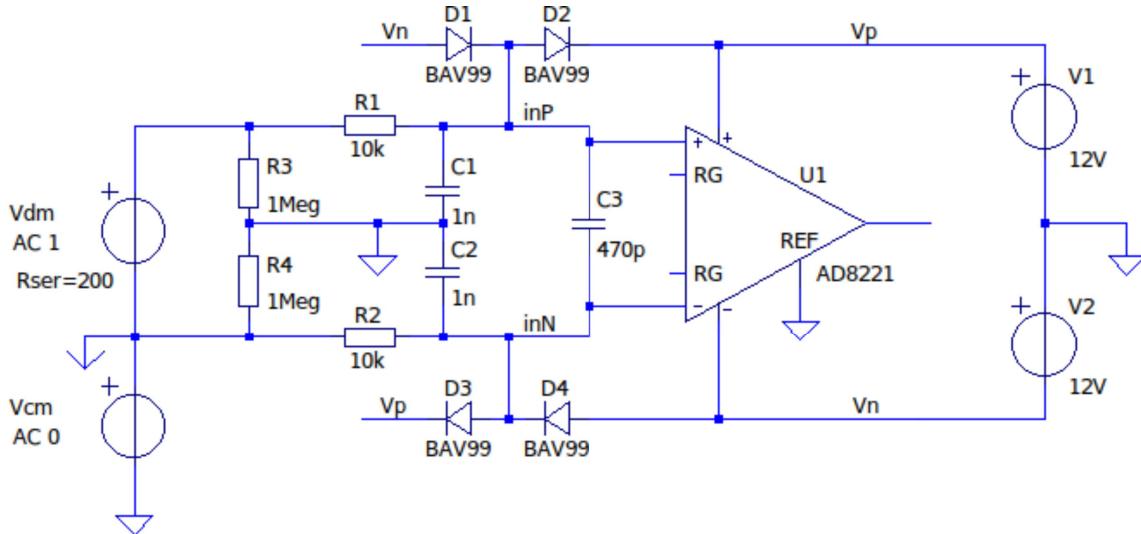
The blue signal is the disable signal. Disabling happens immediately unlike starting.

A bi-stable flip flop with $M_{1,2}$ forms the memory for an alarm. The amplifiers can be started by shorting V_{DS} of M_1 . In this case M_3 takes care of that but it will be replaced by a push button.

- Starting is only possible when all temperatures are below the threshold and the supply voltages are higher than 10,5V. The disable part of the circuit is part of each of the channels.

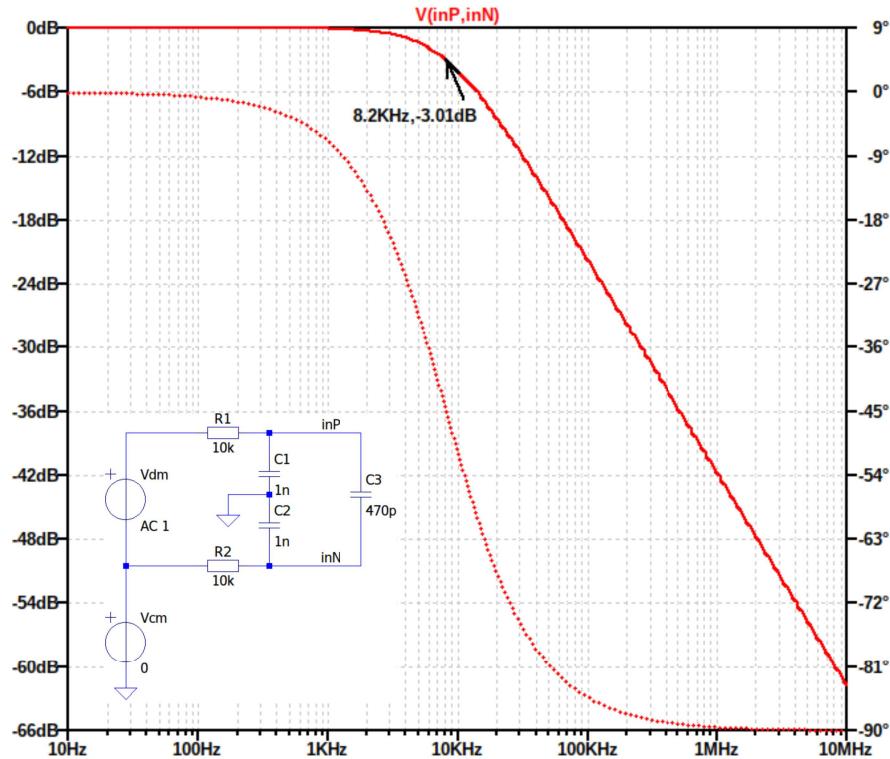


3.3.5 Input Protection



As decided in the topology design a differential amplifier will form the input of the gradient amplifier. The disadvantage over a difference amplifier structure is the reduced robustness. A voltage clamp and filtering are added to improve that. Two resistors connect the inputs to GND in case no cable is connected at the input or when the GND of the spectrometer is not connected to the gradient amplifier.

It's also possible to add spark gaps in the PCB layout for extra ESD protection.

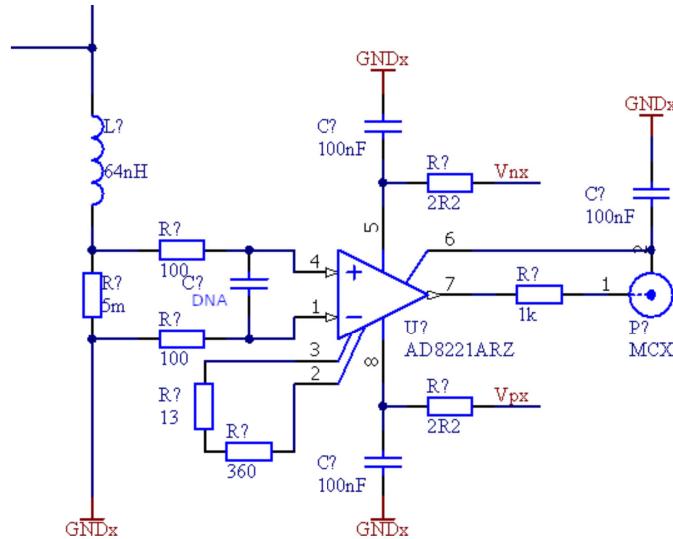


Differential input signals are low pass filtered from 8.2kHz. Common mode attenuation depends very much on the equality of the filter components but also on the source impedance. Although this is known to be 200Ω it was chosen not to correct for this in the circuit because when the signal source is replaced by one with another source resistance the user would have to modify the circuit. When the common mode rejection needs to be improved an external resistor should be added by the user to match the inputs.

4 Monitoring

4.1 Gradient Coil Current

The feedback current is measured as an indication of the current through the coil. The feedback current includes the current through the parasitic capacitance and the parallel damper circuit. So only in the static situation does the measured current represent the magnetic field. However the dynamic effects are relatively small and for monitoring purposes it is good enough.



Feedback resistor R_{FB1} of $5\text{m}\Omega$ is connected to GND in stead of the inductor to minimize the common mode voltage at the input of the AD8221.

The gain of the AD8221 is $G = 1 + \frac{49,4\text{k}\Omega}{R_G}$ and will be set such that the output voltage

matches the input voltage of the gradient amplifier. This results in an output voltage of 10V at 15A which makes the gain 133,3. Two resistors in series of 13Ω and 360Ω form the required R_G very accurately.

An important point is Isolation of the GNDs between the three amplifiers because that would make it possible for the current to flow in an unwanted, unintended path.

- For this reason the AD8221 monitoring outputs will not be referenced to their own GND but to the enclosure GND. This way when multiple monitoring channels are connected to an oscilloscope it will not couple the local GNDs.

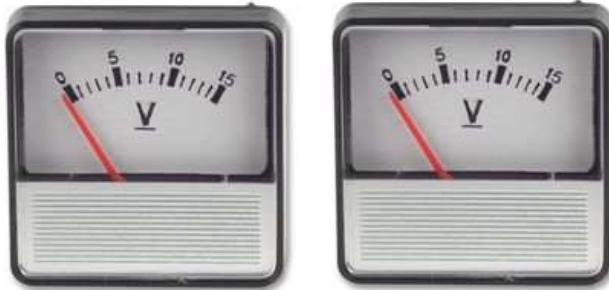
Extra filtering is added to limit the measurement bandwidth approximately to that of the amplifier.

A resistor at the output will prevent instability in case of capacitive loading of the monitor and make the output robust against ESD together with the built in diodes of the AD8221.

4.2 Temperature Alarm Indication

Per channel a single LED will indicate when the P or N FET is running too hot to show the user what channel caused a problem and to signal when the amplifier is ready for use again.

4.3 Supply Voltage



Two SD506/0-15V analog voltage meters will be placed in the front panel to show the supply voltages.

5 Power Supply

5.1 External Power Supply

The amplifier is intended to be battery powered and works on a supply voltage of $\pm 10V$ to $\pm 15V$ with a maximum total current of 45A. The idea is to keep the batteries outside of the enclosure to be able to quickly replace them when they are discharged. This also makes it possible to use a mains powered power supply. By keeping the power supply external no design modifications are required inside the amplifier when a model is unavailable or even obsolete.

Circular MIL spec connectors which can handle the maximum current will be used to connect the power supplies to the amplifier. The Amphenol MS3102A22-22P and MS3106B22-22S connectors are suitable for the application, easy to use and not expensive compared to other high current connectors. The same connectors could be used for charging the batteries.



Short cables should be used to reduce the voltage drop between the voltage source and the amplifier and also reduce EMI in both directions. Coolflex45 (WI-M-10-XX-*) silicone cables AWG 10 could be used. It is also possible to use shielded cable but that seems less practical since the cable will be short and has to split to two power supplies. Two shielded cables might be easier then.

5.1.1 Battery Power

An advantage of powering the gradient amplifier by batteries is the low noise level and the isolation from the mains net which prevents loops in the cabling.

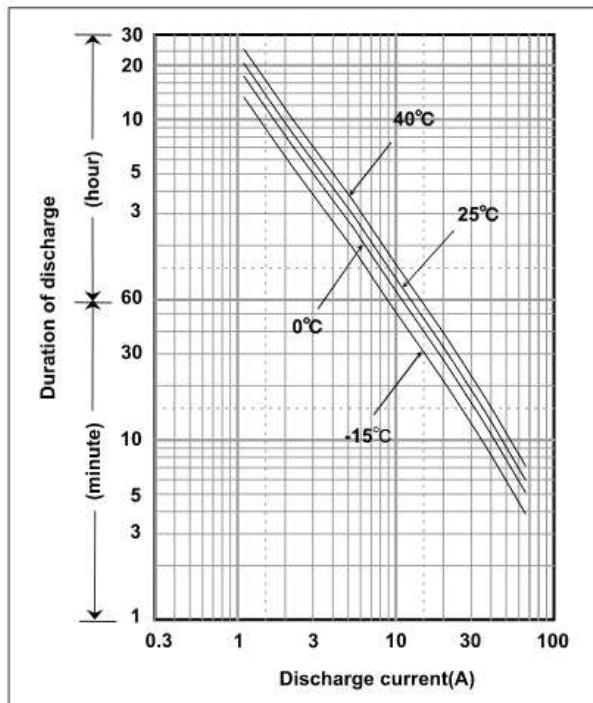
Two battery types that could possibly be used are:

type	V [V]	C [Ah]	$V_{CUT\ OFF}$ [V]	R [mΩ]	m [kg]	technology
LC-XC1222P	12	22	10,5 @1,1-4,4A	12	6,55	Lead Acid
NPC24-12	12	24	10,5 @ 0,4C	?	9,0	Lead Acid

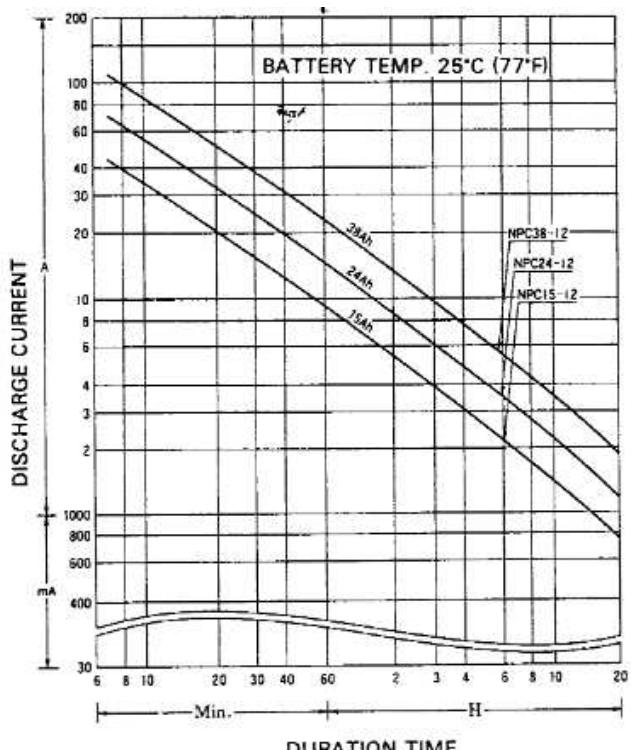


A disadvantage is the varying voltage as the batteries drain. This was taken into account in the biasing step of the design by making the biasing relative to the relevant supply rail.

Duration of discharge vs Discharge current



LC-XC1222P



NPC24-12

At a 3A average discharge current these batteries last about 5 or 6 hours. The under voltage lock out will disable the amplifiers when the batteries are drained. The threshold voltage needs to be 10,5V.

5.1.2 Switch Mode Power Supply

A SMPS is a good alternative to power the gradient amplifier. It only depends on the availability of mains power, gives constant output voltage and usually have built in protection against overload conditions. Linear power supplies would produce less noise, especially in the higher frequency regions, but these are far less available and otherwise probably very expensive for the required amount of power. Medical grade power supplies even have a very low leakage current for extra safety.

When the power supply is equipped with a constant current limiting overload protection this would result in a very effective protection in combination with the amplifiers' UVLO. As soon as the decoupling capacitors are discharged below the threshold voltage of 10,5V it will disable itself.

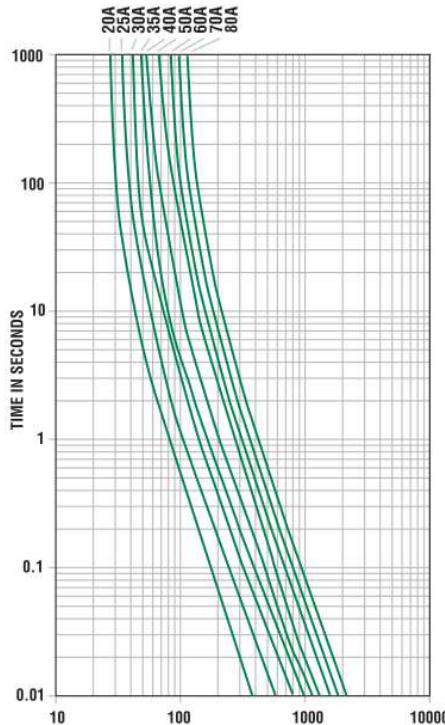
Two suitable models which are both medical grade:

Model	#outputs	V _{OUT} [V]	I _{MAX} [A]	Ripple [mVpp]	CL [% I _{MAX}]
TPP 450-115-M	1	15 (adj. 8%)	30	300	115-150
MSP-450-15	1	15	30	150	105-135



5.2 Fuse

Though the amplifier has a current limiter, thermal protection and an under voltage lock out, a fuse is an absolute must when the amplifier is powered from batteries. The type ATO Blade that is used in cars was chosen for its wide availability. Two fuses will protect the positive and negative power supply which will be mounted on the back panel of the amplifier for easy access.



The 20A fuse seems like a safe choice for the application. Each channel will be on with a limited duty cycle of about 1/3 and at most two channels will draw current from the same power supply at the same time. In case of a failure the batteries will be saved.



When a fuse blows while there is a large current flowing through the gradient coils that energy needs to go somewhere. Suppose that just before the fuse blew the maximum current of 15A was running in all three gradient coils of 1mH each. The total energy that needs to be moved is:

$$E_{GR} = \sum_{n=1}^3 \frac{1}{2} L_n I_n^2$$

Which gives 0,34J in this case. In the beginning just after a fuse breaks the capacitors will discharge. When the UVLO disables the amplifier and there is still current running in the coils, this current will continue as a charge current into the other supply voltage.

When the opposite fuse is blown and the UVLO disables the amplifier, then the remaining gradient energy will go to the decoupling capacitors. If the voltage is allowed to rise up to 18V it is possible to calculate the required capacitance.

$$C = \frac{2 \cdot E_{GR}}{V_{MAX}^2 - V_{START}^2}$$

The worst case situation is when V_{START} is 15V which results in a 6,9mF decoupling capacitance. This is a very acceptable value. Alternatively an anti parallel diode could be placed at the fuses to conduct current back to the power supply when a fuse blows but there seems no need for that.

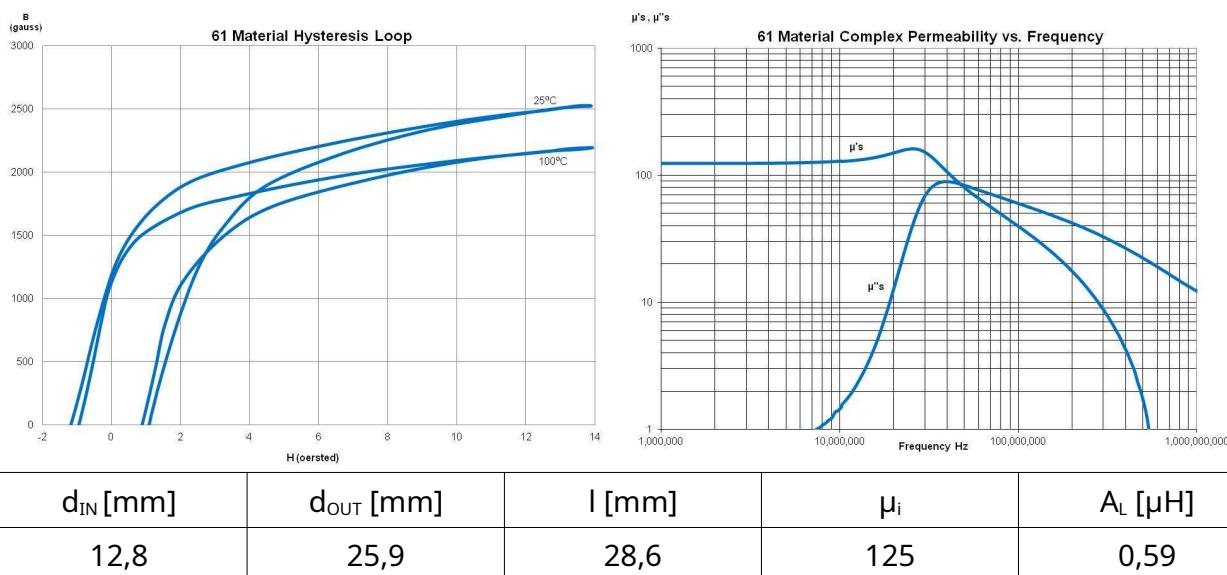
5.3 Filtering

An LC-filter on the supply voltage can filter out higher frequency noise to the amplifier but also keep most of the fast changing current inside the amplifiers' enclosure. A ferrite cylinder around the power cable can provide the inductance while keeping a low series resistance.

The magnetic core should not saturate at the maximum current of 45A. For a cylinder with diameter d the magnetic field is given by:

$$B(d) = \frac{4 \cdot 10^{-7} \mu_i I}{d}$$

A suitable core for this is the Fair-Rite 2661102002



The maximum magnetic field in the ferrite core is 176mT (1760 gauss) near the inner diameter and 86,9mT at the outer diameter. These are very acceptable values. The A_L was measured for a single turn as intended for the application, but can also be calculated.

$$L = \frac{\Phi}{I} = \frac{BA}{I} = \frac{\mu_0 \mu_i l}{2\pi} \int_{r_{IN}}^{r_{OUT}} \frac{1}{r} dr = \frac{\mu_0 \mu_i l}{2\pi} \ln \left(\frac{d_{OUT}}{d_{IN}} \right)$$

This results in $0,50\mu$ H which is slightly lower than the measured value.

The minimum capacitance as determined in the fuse section is 6,9mF. The maximum RMS current in the situation where all three channels generate the same sine wave is 15,9A.

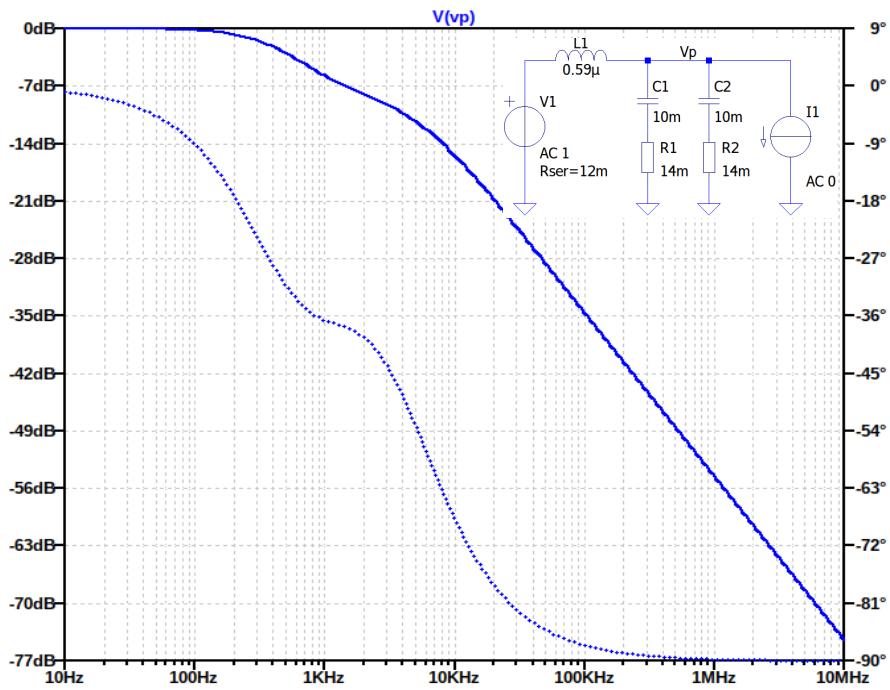
KEMET ALS30A103DE063



Two of these capacitors in parallel per supply voltage can handle that current and also equals the maximum load capacitance of one of the selected switch mode power supplies.

10mF, 63V, 14mΩ, 10,8A

D = 36mm, L = 82mm

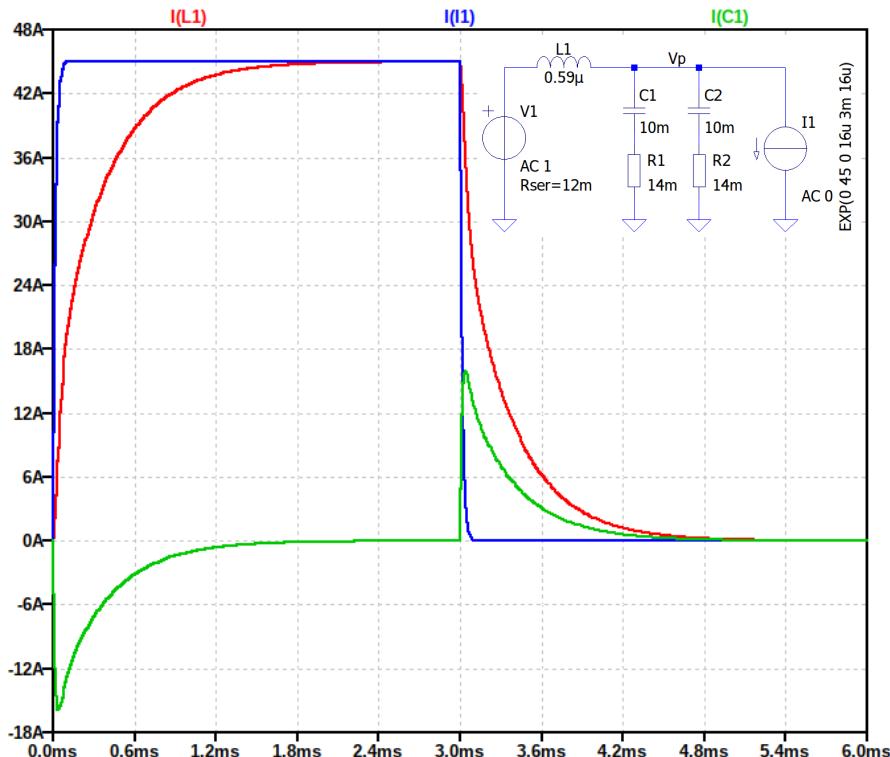


Bode plot of the attenuation of input noise on the power supply.

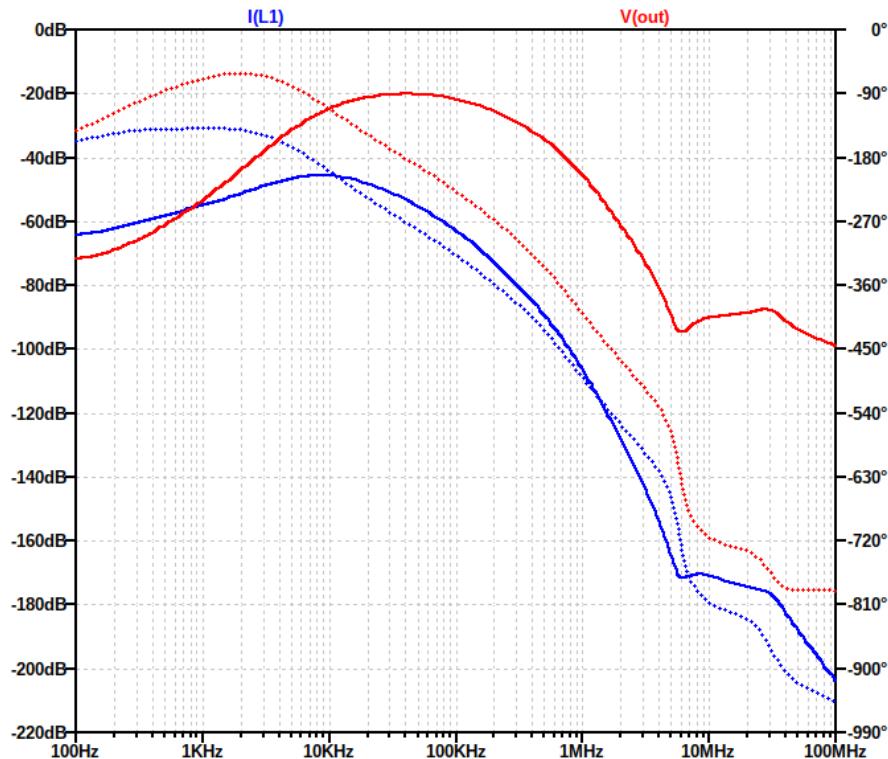
LC filters can cause ringing when there is not enough damping and thereby even increase the amount of noise for a certain frequency. The minimum series damping resistance can be found with:

$$R_{DAMP} = \sqrt{\frac{2L}{C}}$$

which results in 7.7mΩ or more. The battery has 12mΩ and the capacitors 7mΩ series resistance. So no ringing is expected even if the battery has less series resistance.



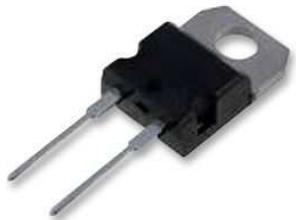
The simulated power supply rejection ratio with this filter plus the amplifier is shown below.



5.4 Reverse Polarity Protection

Since the batteries can be disconnected from the amplifier at either end of the cable, there is a risk of reconnecting them in reverse polarity by mistake.

- The decoupling capacitors could be damaged from reversed polarity and to prevent this one anti parallel diode will be placed at the decoupling capacitors per supply voltage.



MBR40250G

250V, 40A, TO220 Schottky diode

The soft start circuit that limits the charge current to the capacitors during start up should also limit the current when the polarity is reversed. The under voltage lock out will prevent the amplifier from being enabled.

No extra signaling will be added. The voltage meters in the front panel will indicate something is wrong with the power supply in that case.

5.5 Soft Start

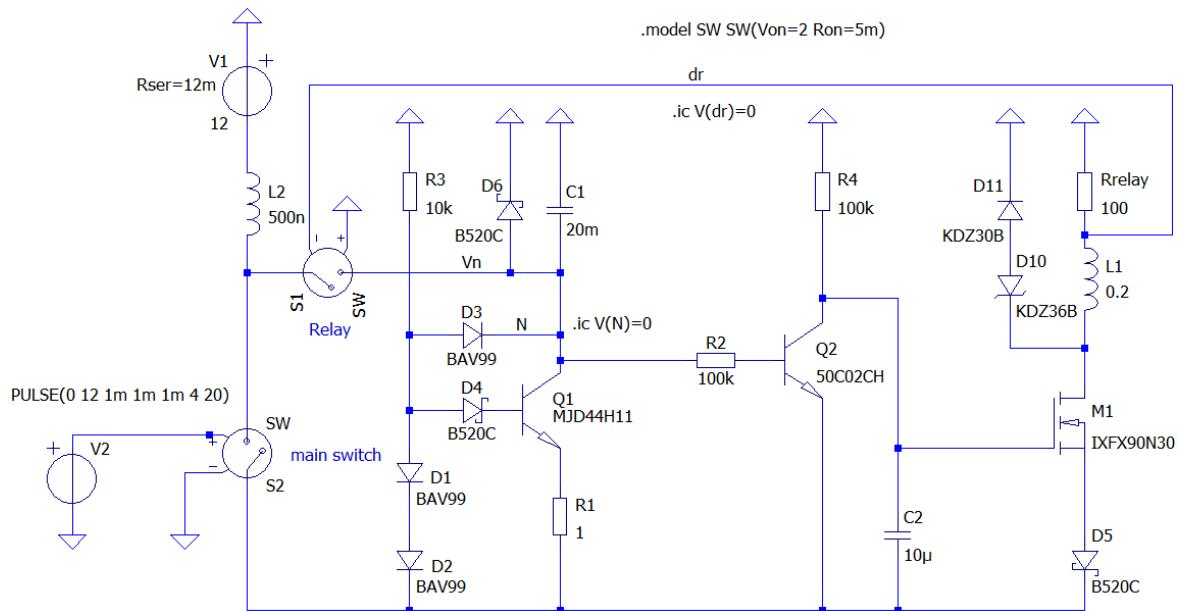
Since batteries have no current limit other than the few mΩ of internal resistance an inrush current limit circuit will be added. This circuit fully charges the large decoupling capacitors at an acceptable current before the power switch closes. This soft start prevents the fuse from blowing up immediately at power up and it protects the capacitors.

During the charging of the capacitors the under voltage lock out prevents the amplifier from being started when the start button is pushed.

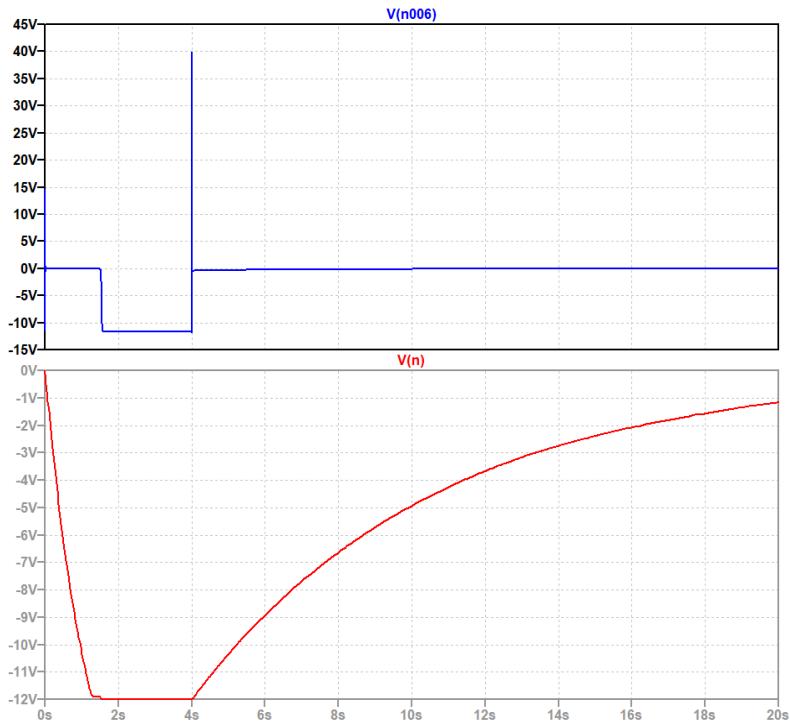
The very high operating current will flow through a relay which closes after the capacitors have been fully charged. This creates a bypass around the soft start circuit. Industrial applications often use contactors for this purpose, but these are quite expensive. Instead automotive relays will be used which are considerably cheaper and widely available.



These relays also require less power to operate than contactors. A parallel TVS diode will be placed to prevent sparking when the controlling switch opens. Most of them have only one switch either SPDT or SPST, so two of them will be required to switch both power supplies.



This soft start circuit charges C1 with a limited current of about 350mA when the main switch is closed. Q2 acts as a comparator to detect when C1 is almost fully charged. Then after a delay time determined by R4, C2, D5 and M1 the relay is switched on. D5 prevents reverse currents in case of wrong power supply polarity and D6 protects C1 int that case from reversed polarity. When C1 is charged and the power is switched off D3,4 prevent Q1 from being enabled in reverse mode* by keeping $V_{BC} < 0,6V$. During normal charging of C1 these diodes will limit the saturation voltage of Q1 slightly though. A similar but opposite circuit can be used for the other polarity.



* During testing it was found a reverse current still occurred but because $V_{EB\ ZENER}$ of Q1 after switching off the supply voltage. This conducted a current from the relay to the emitter to the now forward biased CB diode.

6 EMI / ESD

Measures that have already been implemented in the circuit design:

- Low pass filtering and voltage clamps at the control inputs.
- Series resistance and a voltage clamp at the monitoring outputs.
- Voltage clamps by the intrinsic MOSFET diodes at the amplifier outputs.
- Decoupling capacitors including a damping resistor to damp parasitic LC resonance.
- Low pass filtering at the power entries with sufficient damping.
- Separate GNDs per channel to prevent unintended current paths.

6.1 Cabling

6.1.1 Power Supply

The separate GNDs of the three amplifiers will only be coupled to each other at the 20mF decoupling capacitors. This star point is also the point where the metal enclosure is connected to GND.

The + and – terminal of each power supply must have their own cable to keep the resistance low, so at least four cables are required both inside and outside of the enclosure. The loop area between each set of cables should be minimized to reduce the inductance and thereby the magnetic flux. Twisting of the wires is preferred, but they should at least be bundled per power supply. Short current spikes from the positive to the negative power supply can occur during zero crossings which is why the two bundles of power cables should also be kept close to each other. Though most of this spike current will be taken care off by the decoupling capacitors.

6.1.2 Inputs

The differential inputs will guarantee channel isolation by design. No part of the enormous output current can flow through the input cables and thereby cause local feedback, either positive or negative, or even cross couple to the other channels. Since the inputs can't connect the GNDs of the three channels to the GND of the spectrometer this leaves the common mode voltage at the input undefined. Resistors of $1\text{M}\Omega$ at each input terminal are the only parts that form a DC connection between the GND of the spectrometer and the gradient amplifier. Somewhere along the path from the spectrometer to the PCB of the amplifier the GNDs must be coupled to define the common mode voltage.

The outputs of the spectrometer have BNC connectors connected to their common GND so to make the cabling easier these connectors will also be used for the amplifier. A shielded multicore cable connection is preferred but that would be more difficult to construct for BNC connectors. The choice for either insulated or non insulated BNC connectors should be made now. Both have their advantages and disadvantages.

BNC type choice	Insulated BNC	Non Insulated BNC
Advantages	<ul style="list-style-type: none"> A single connection between the GNDs of the SM and GA can be made which can ultimately be a continuous shield around the coax cables. 	<ul style="list-style-type: none"> The coax shield connects well with the enclosure to keep noise and ESD spikes out. A GND connection is guaranteed both at the input and between the SM and GA.
Disadvantages	<ul style="list-style-type: none"> Noise and ESD spikes on the coax shield will enter the enclosure. A separate GND cable and extra connector are required. The GND cable could be forgotten which makes the GA vulnerable for large CM voltages. 	<ul style="list-style-type: none"> Multiple coax cables form GND loops in which a changing magnetic field can induce shield currents and differential voltages. The shielding still continues into the enclosure which is unavoidable with coax cables.

→ The non insulated BNC will be used at the input of the gradient amplifier. This defines the common mode input voltage halfway the input signal, since the source is single ended, plus the voltage of the local GND plane of that channel.

A gas discharge tube will be placed directly between the BNC terminals to further improve ESD resilience.



2051-09-SM-RPLF

$V_{BD} = 90V$, size 2051

The cable inside the enclosure that connects the BNC to the PCB mount MCX is:

415-0015-M1.0 , 90° MCX Plug to 90° MCX Plug, RG178, 50Ω, 1 m, White, OD 1,85mm

These can be cut in half to connect one side to the BNC connector. This cable should run close to the walls of the enclosure to minimize the magnetic coupling area.

For extra common mode filtering these ferrite beads will be placed around the cable.



74270020

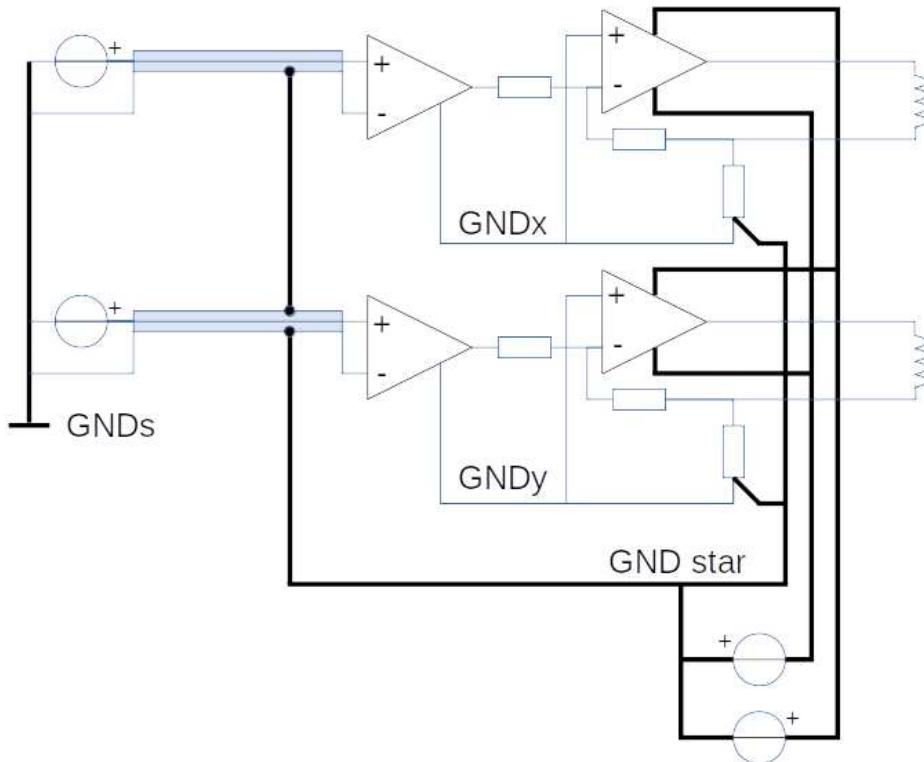
Ferrite Bead, Tubular, 108 ohm, WE-SAFB Series, -108 ohm, ± 25%

L = 7,5mm, OD = 7,5mm, ID = 2,4mm

measured:

$L = 478\text{nH}$, $R_s = 315\text{m}\Omega$ @ 300kHz

$L = 370\text{nH}$, $R_s = 690\text{m}\Omega$ @ 1MHz



This simplified schematic shows the power supply and grounding scheme for two channels of the gradient amplifier. The third one is of course similar but is not shown here. Starting at the left is the spectrometer with output voltages relative to GNDs. These connect to the gradient amplifier through coaxial cables which have their shields connected to the enclosure. GND star is the common point for GNDx, GNDy, the enclosure and the batteries. The two batteries are shown on the bottom right.

The important design philosophy behind this is that (high) currents from one channel should not be able to influence the output current of another or even itself. This could happen via local GND coupling in two ways:

1. If high current can flow through the local GNDx,y,z plane to GND star.
2. If high current can flow through the shield of a coax cable.

Both these situations result in a voltage drop in a GND and then results in a change of the output current. The first case is the most critical one since every mV voltage drop in a local GND results in 200mA output current. In the second case it only results in 1,5mA/mV which makes the advantage of an insulated BNC small compared to a non insulated one.

The fork structure in the local grounds combined with the Kelvin contacts at the current sense resistor make the output current insensitive to the current of any channel. Differential amplifiers at the input and the monitoring output (not shown here) prevent possible compromise of this structure.

High currents could still exist in the coax shields if a magnetic field couples with the loop they form or if the enclosure is connected to an earth potential which is different from the earth potential of the spectrometer. This is the consequence of using non insulated BNCs and can be reduced by minimizing the coupling area the cables make and by using a single earth point.

6.1.3 Amplifier Outputs

A PCB mount screw connector was chosen to connect the gradient coils. No high current cables are required inside the enclosure because of this, they are easy to use and take up very little board space compared to other types of high current connectors.



MSTB 2.5 HC/ 2-GF – 1923979 , 2 Way PCB Header

MSTB 2.5 HC/ 2-STF – 1912074 , Pluggable Terminal Blocks 5mm pitch Plug 24-12 AWG Screw

However shielding is not present on these connectors. To solve that M3 tapped holes will be added underneath the screw connectors to make it possible to use shielded cables and connect them to the enclosure.

6.1.4 Monitoring Outputs



The monitoring outputs will be connected to GND at the front panel of the enclosure, but this doesn't connect the separate GNDs to each other. This is because the AD8221 reference terminal is a sense input. The monitoring output voltage is superimposed on top of this sensed GND voltage. The same type BNC connector and cable will be used as for the inputs of the amplifier with the same gas discharge tubes and ferrite beads.

6.2 Shielding

Noise that is present on the GND of a channel is coupled through the feedback network to the gradient coil. Especially high frequency content of a few MHz, which is in the measurement bandwidth of the MRI RF coil, should be avoided. This can come from intrinsic noise or from external noise sources. The enclosure should also give some shielding in both directions. At 3MHz the wave length is 100m, so no extreme shielding measures are required for the enclosure which matters a lot in the price.



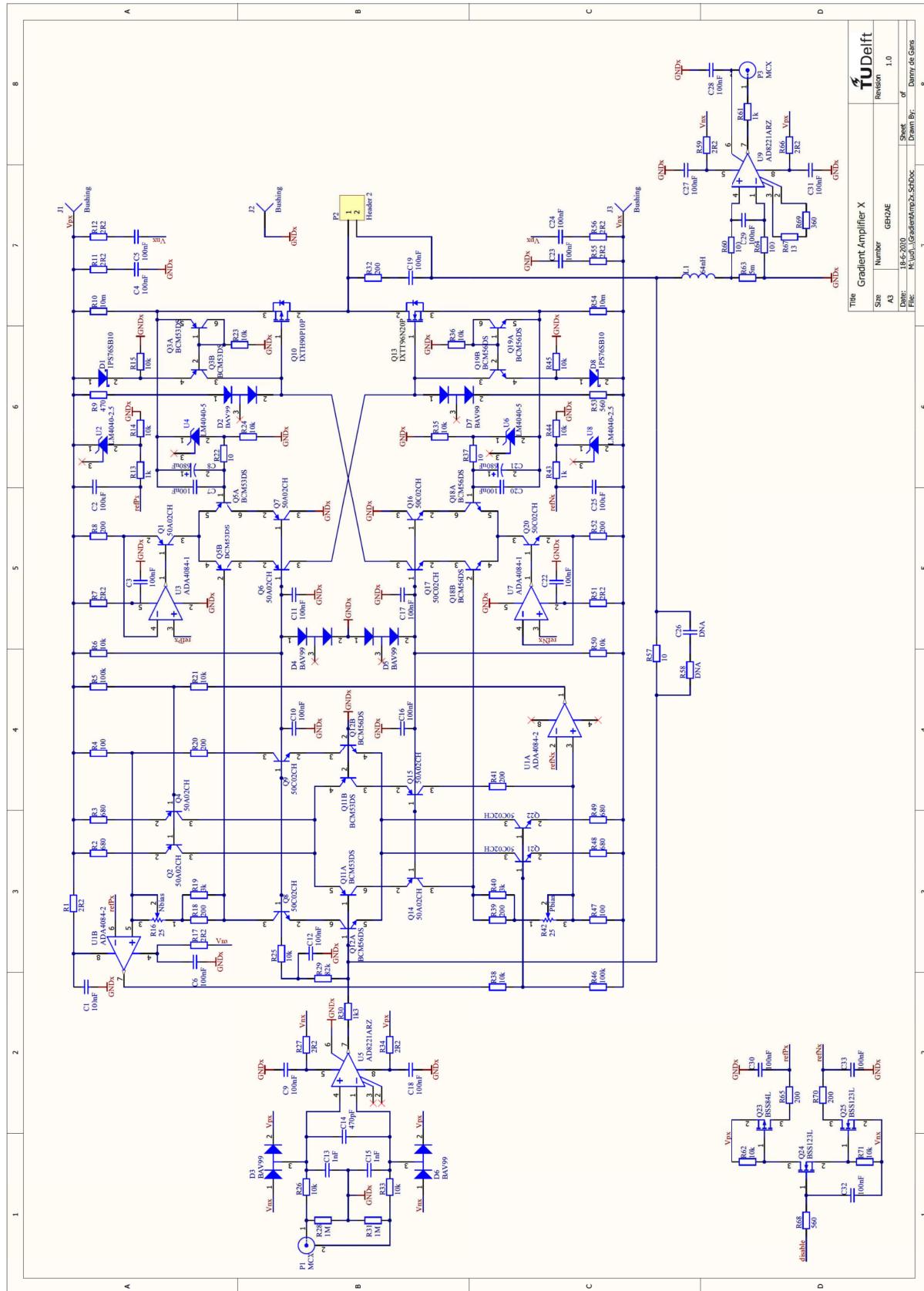
24563-133 , 19" Subrack, EuropacPro, Kit, Unshielded, 3U, 84, 295mm, 133mm, 427mm, 11.61"

The front panels and cover plates will make a good electrical contact with the rest of the enclosure.



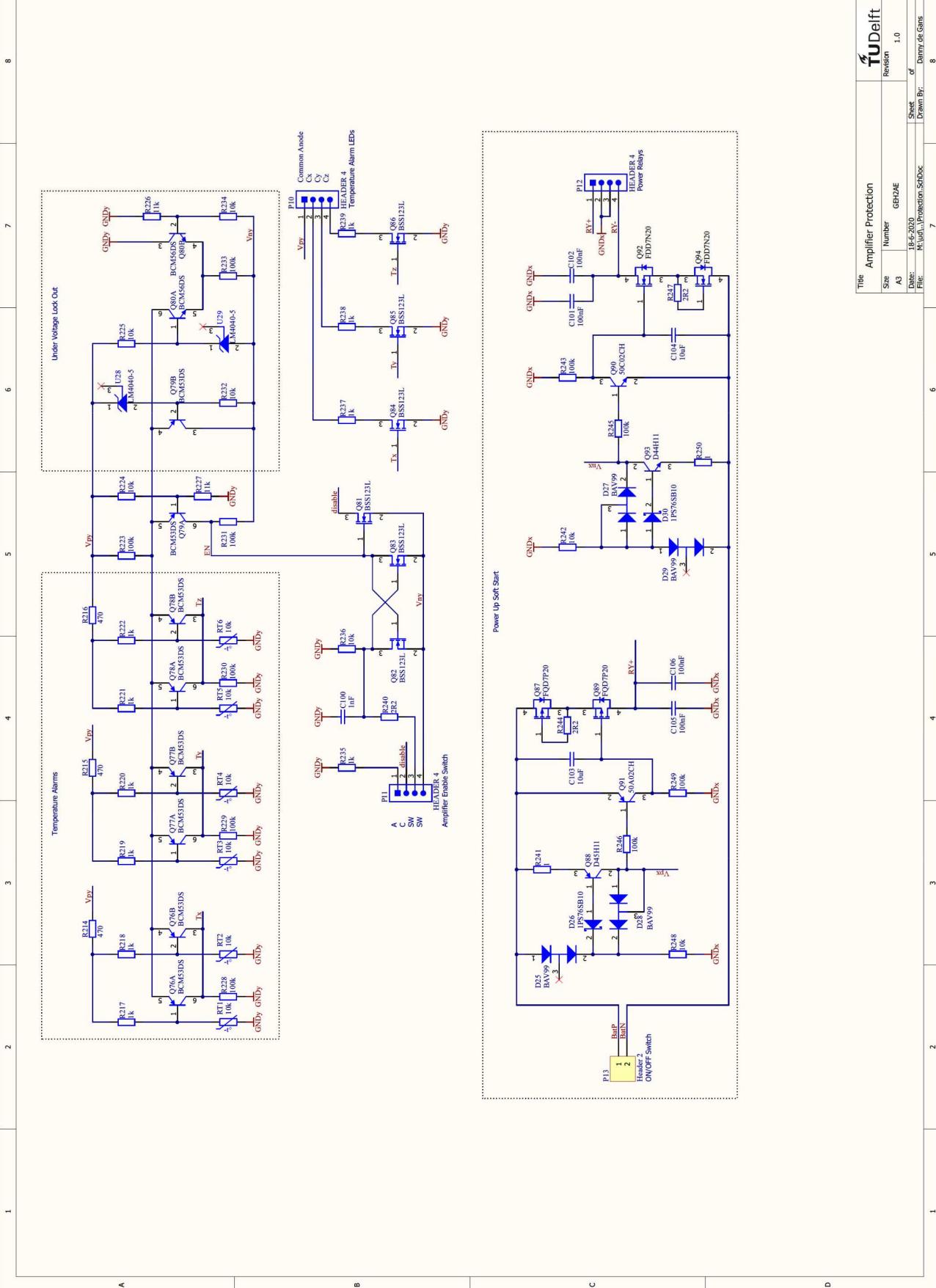
4mm banana sockets will be placed to be able to connect to other shielding parts of the system.

7 Circuits for PCB Layout



Identical for Channel X, Y and Z

Title Gradient Amplifier X		TU Delft	
A3	GB24E	Revision 1.0	Date 18-6-2020
Ref:	Rev. A	Sheet 7 of 8	Drawn By Danny de Gans



8 PCB Design

The circuit diagram is the starting point for the PCB design. However it is a simplification of reality and the only information it contains for the designer are the net list which tells what should be connected to each other and the footprints of the components. Important general information that is not captured in the schematic is:

- Sensitivity of a net or component to other parts of the circuit or even from outside. This could be because of electromagnetic, conductive or even thermal coupling.
- If a net is likely to produce noise because of high dV/dt or dI/dt .
- High voltage and -current nets.
- Characteristic impedance.
- Dimensions or even shape of the board outline.
- Heat dissipation of components.

These points result in acceptable copper dimensions and clearances and rough guide lines for the layout of the components and also where to place measures like shielding in the form of a ground plane or guard ring.

8.1 Tracks

8.1.1 Parasitic Components

The wires of the circuit schematic do not have resistance, inductance, capacitance and time delay. This means they have zero length. Trying to keep PCB traces as short as possible is therefore a good rule when implementing a schematic on a circuit board. Components should be placed in such a layout that minimizes the length of copper traces.

Copper Trace	Increasing Length	Increasing Width
R	↑	↓
L	↑	↓
C	↑	↑
t_{DELAY}	↑	-

This table again shows that it's always a good idea to keep traces short. The trace width depends on which parasitic component does the most damage. Often you want to keep traces narrower than wider because the capacitance is more likely to degrade performance and out of practical considerations, because narrow traces can pass more easily underneath components. These mentioned parasitic components create a loading effect throughout the circuit.

Mutual inductance and capacitance arise when magnetic and electric flux of a track couples to another. So now there are also parasitic transformers and coupling capacitors. These inject voltages and currents to other parts of the circuit and create unintended feedback loops that could even lead to an unstable amplifier.

Ways to cope with that are

- Creating less flux that could couple
- Keeping distance
- Minimize the mutual coupling area
- Shielding

Finally for high frequency designs it is important to keep the dimensions of the circuit well below the wave length for the lumped element approach to hold and work with transmission lines where this can not be met.

The board material is FR4 which has an ϵ_r of 4,3. A four layer build up has layer thicknesses of 0,36mm – 0,71mm – 0,36mm. This results in a capacitance to the ground plane of 106fF/mm^2 and 36fF/mm^2 depending on the layer.

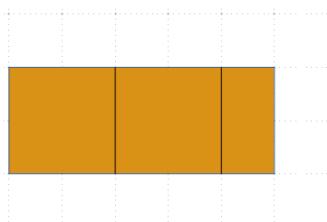
The resistance of a copper track is

$$R = \rho \frac{l}{A} \quad \text{with } \rho = 17\text{n}\Omega\text{m}$$

for a square part of trace the width is equal to the length so

$$R_{\square} = \rho \frac{l}{l \cdot h} = \frac{\rho}{h} = 0,5\text{m}\Omega/\square \quad \text{for } 35\mu\text{m thick copper.}$$

This means that every square piece of the trace will produce 109mW at 15A, and to minimize heat production these traces should consist of the least amount of squares possible.



This PCB trace for example is made of 2,5 squares, so its resistance is 1,25mΩ. The dimensions don't even matter.

To reduce the resistance of high current tracks it is possible to make tracks in the solder mask that are coated with solder by the hot air leveling step of the PCB manufacturer or during assembly.

8.1.2 Current Density

Copper can handle a maximum current density of $j = 400\text{A/mm}^2$ at 85°C before electro migration and diffusion destroy the connection. For 15A and $35\mu\text{m}$ copper thickness these tracks should be at least 1mm wide.

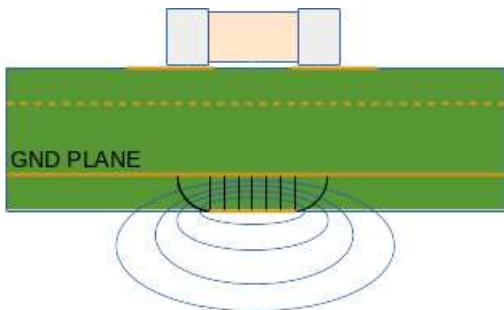
8.2 Ground Plane

The ground plane in this design is there to provide a low impedance return path for high frequency currents, provide electrical and magnetic shielding and spread out heat.

8.2.1 Shielding

Traces and components can have capacitive or inductive coupling with other traces or parts. It's the flux that couples ($d\Psi_E/dt$ and $d\Phi_B/dt$), so to prevent flux linkage from disturbing to sensitive parts of the circuit three things can be done in the layout of the PCB:

- minimize the area where E + M flux can couple (surface area and $\cos(\varphi)$)
- keeping distance
- redirect E + M flux by shielding
- reduce flux production by using short wide tracks close to each other (low L) for high dI/dt and short narrow tracks (low C) for high dV/dt sources.



A ground plane can be used to redirect E and M flux. The inner layers have a standard copper thickness of 35 μ m. The skin depth is given by:

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}}$$

with $\rho_{Cu} = 17[n\Omega m]$ and $\mu = 4\pi \cdot 10^{-7}[H/m]$

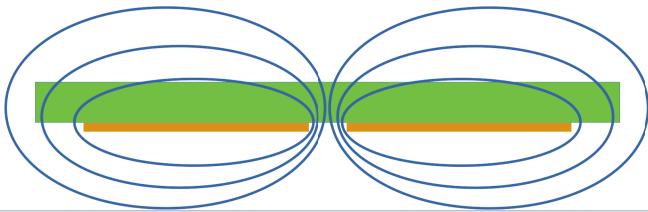
The magnetic field reduces by 63% per δ . If 28 is assumed to be thick enough for shielding then the GND plane becomes effective above 14MHz for a single layer and 3,5MHz for two layers of shielding.

- The bandwidth of the gradient amplifier is about 10kHz so the GND plane will only work as an electric shield and have almost no effect on the magnetic field formed by the 15A output current.

The magnetic field lines see 18 copper for 10kHz when the magnetic field is under an angle of 3° with the GND plane.

The GND plane can shield the high $d\Psi_E/dt$ coming from the wide track of the output of the amplifier that also has high dV/dt when a MOSFET starts or stops conducting current back into the power supply.

- By placing the GND plane at inner layer 1 the coupling capacitance between the output and the GND plane is 66% lower than if it were placed at inner layer 2. This makes it harder for the output current to flow through the local GND plane which was mentioned in the grounding design philosophy in 6.1.2.



Heat sink

This sketch shows the magnetic field of the large gradient coil current running through wide copper traces at the bottom of the PCB. Most of this field is oriented parallel to the PCB except between the traces. At that location the magnetic flux is the highest and loops of copper traces in the horizontal plane will induce a voltage. Loops in the neighboring channel are almost perpendicular to the magnetic field and will also couple but with less flux density.

Suppose the two high current tracks have:

$$w = 2\text{cm}, l = 8\text{cm}, d = 1\text{mm}$$

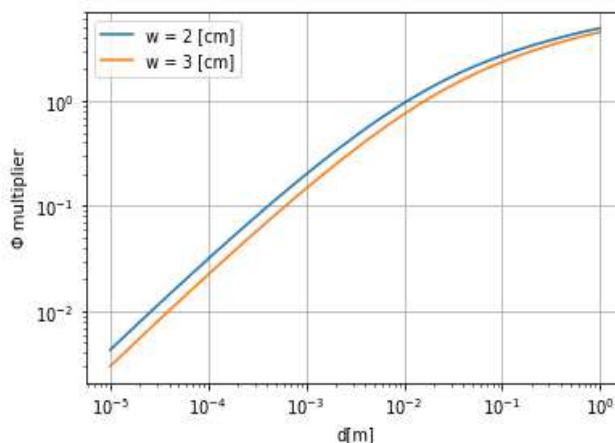
The magnetic field of a current carrying copper strip in the same plane at distance s is:

$$B = \frac{\mu_0 I}{2\pi w} \ln\left(\frac{w+s}{s}\right)$$

The total magnetic flux between two equal parallel strips on the same layer is

$$\Phi_B = 2 \int_0^d \frac{\mu_0 I l}{2\pi w} \ln\left(\frac{w+s}{s}\right) ds = \frac{\mu_0 I l}{\pi w} \left(d \ln\left(\frac{d+w}{d}\right) + w \ln\left(\frac{d+w}{w}\right) \right)$$

At 30V and 180 μ H the dI/dt becomes 167kA/s which results in a $V_{loop} = d\Phi/dt = 1\text{mV}$ for a loop that captures all of the flux. The formula shows that to reduce magnetic flux the distance between the tracks should be as small as possible and the width as large as possible.



8.2.2 Heat Spreading

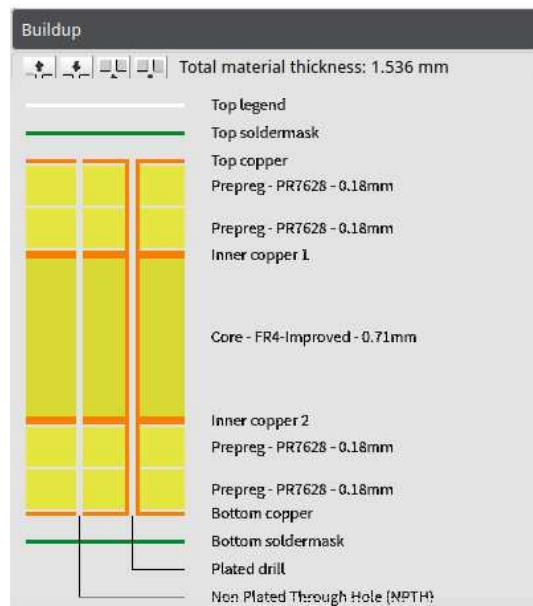
Temperature drift at the input stage causes the output current to drift. This was addressed in 3.2.1, 3.2.4 and 3.2.7 where measures were taken to minimize temperature effects. It would also help if the change in temperature across the surface and in time was minimized. The bottom layer already has large areas with copper because of the high current tracks. A GND plane closely underneath the components at inner layer 1 will also help to spread out the heat and reduce local hot spots. Creating copper fills at the top layer would help too if there is any space for it.

8.3 Build Up

The build up of the PCB will have four layers with the following purposes per layer:

1. placement of most components for easy access and routing
2. GND layer which is isolated per channel
3. routing of power and normal traces
4. high power components with wide copper tracks

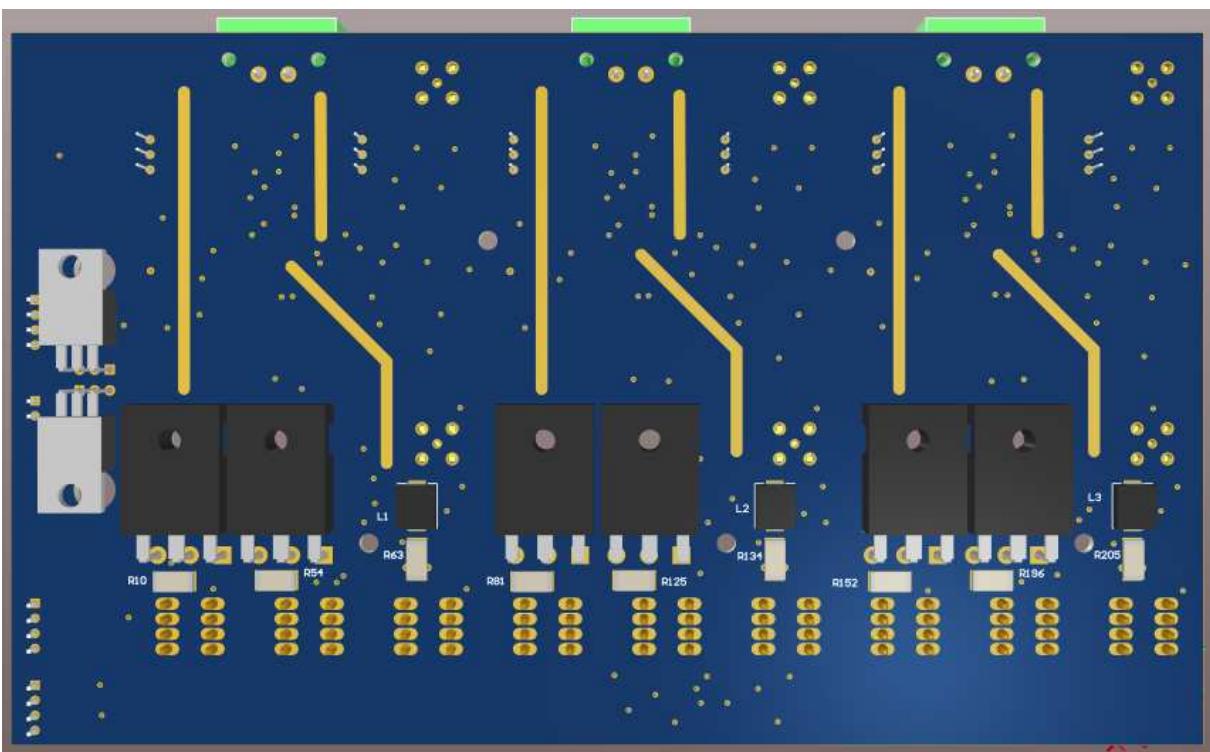
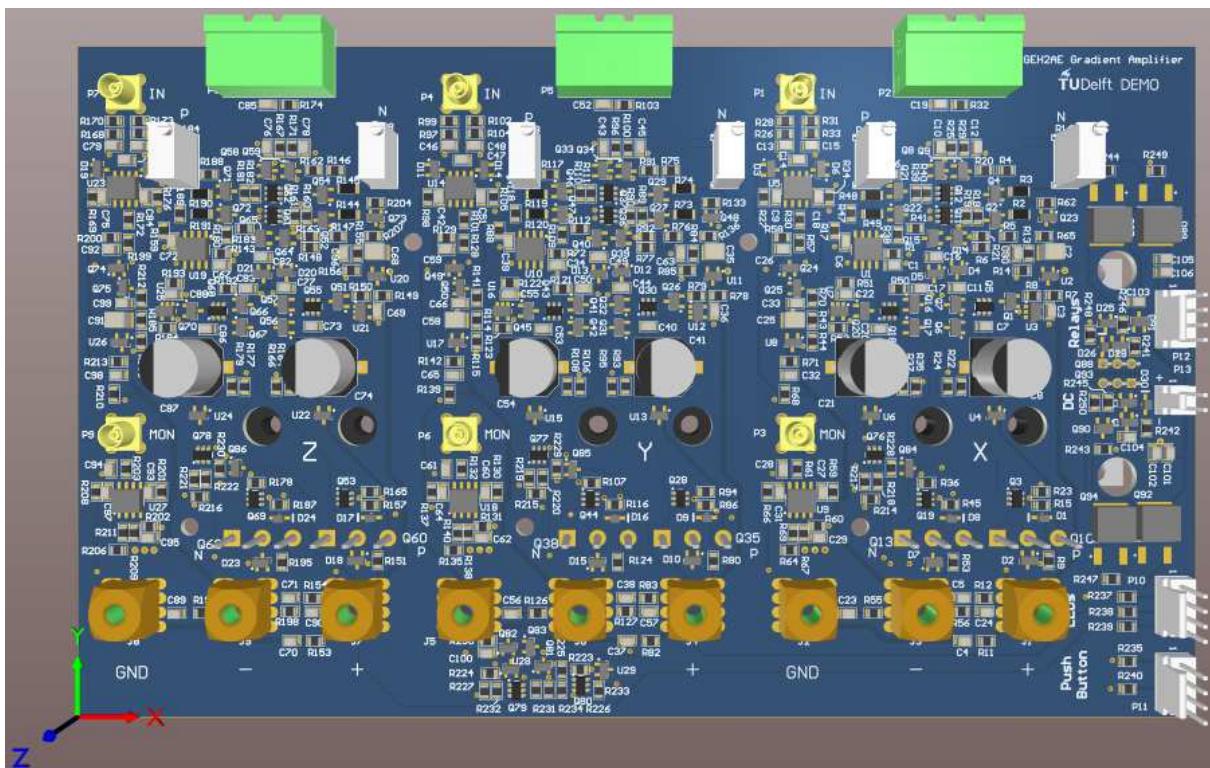
Top and bottom layer will be standard 35 μm copper.



8.4 Key Points for the Layout

- Thermal matching of the input stage
- GND plane on layer2 for thermal stability and optimal heat spreading
- Kelvin contact for GND at the positive input of the differential input stage
- text at trimmers for M1,2
- spreading of heat from the CB stages and try to keep the DV stage at a constant temperature
- thermal coupling of the 5V and 2,5V reference voltages of the same power rail.
- Coupling of the local GND plane at the Kelvin contact of the current sense resistor
- Decoupling capacitor locations

8.5 Layout details



The board is 1,56mm x 200mm x 120mm and contains 3 channels plus the protection circuits.

The input stage of an amplifier is at the top in the Y direction as noted in the first picture. The MOSFETs of the output stage are near the power bushings. This layout makes it possible to have very short power connections and have only two high current output traces cross the length of the board in stead of three supply traces.

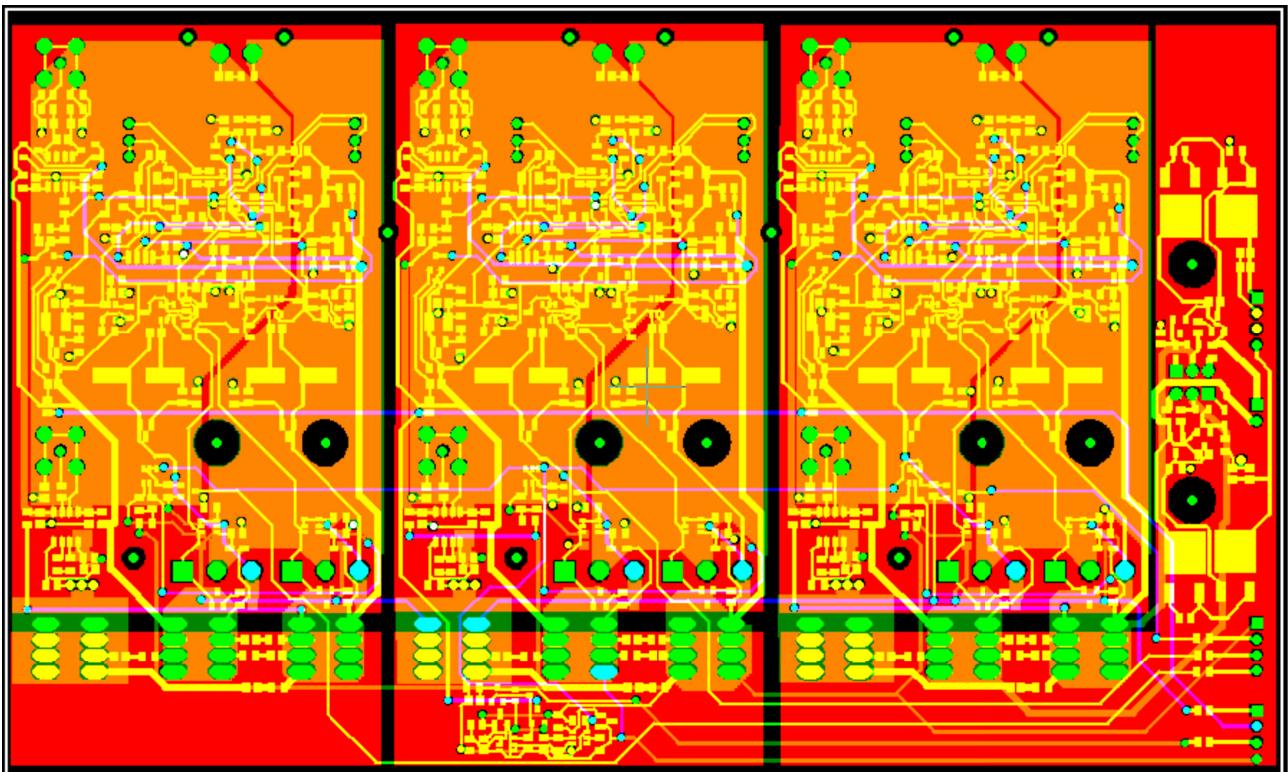
Holes in the PCB make it possible to mount the PCB directly onto a heat sink with the power transistors located between the board and the heat sink.

Solder mask openings in the bottom layer form traces that will have extra thickness after HAL to reduce the resistance even more. This allows the 'active' output trace to be made narrower to reduce the parasitic capacitance to the GND plane. It also compensates for under plating.

Below the Y channel in the center is where the disabling circuit is located. The two connectors that belong to it are at the bottom right corner of the PCB.

A 2cm strip at the right of the PCB contains the soft start circuit to slowly charge the large capacitors. The + and - of the power supply enter at the 2 pin IDT connector and the charge current flows out of the channel X bushings to the capacitors.

Three large parallel vias create a Kelvin contact from the feedback sense resistor to the channels' local GND plane. This is the common GND to which all of the amplifier is referenced. This GND layer is located at inner layer 1 and covers almost the entire area of a channel.

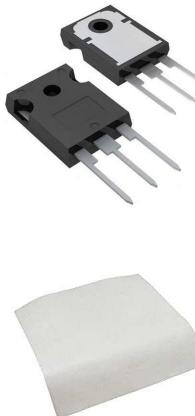


At the bottom layer a separate trace is made for a Kelvin contact to the frequency compensation inductor in the feedback network. Since the feedback current is 2000 times smaller than the output current even a small impedance in the widest track of the PCB would still result in more voltage drop than in a separate relatively long trace with very little current.

9 Enclosure Design

9.1 Cooling

The thermal resistance R_{TH-JC} of the P MOSFETs is 0,27°C/W and for the N MOSFET 0,25°C/W. Both MOSFETs can operate up to a junction temperature of 150°C.



Together with R_{TH-CS} and R_{TH-S} these thermal resistances determine the temperature rise for the dissipated power in the TO247 packages. Most MOSFETs have the drain connection at the tab on the back side for optimal cooling. This means that it has to stay electrically insulated from the heat sink. This increases the thermal resistance because the electrically insulating layer also forms a thermal barrier.

R_{TH-CS} is the thermal resistance between the TO247 package and the heat sink. One of the best insulating pads for this purpose is the Sil-Pad 2000 which has a thermal conductivity k of 3,5W/m·K and a thickness L of 0,38mm.

$$R_{TH} = \frac{L}{k \cdot A}$$

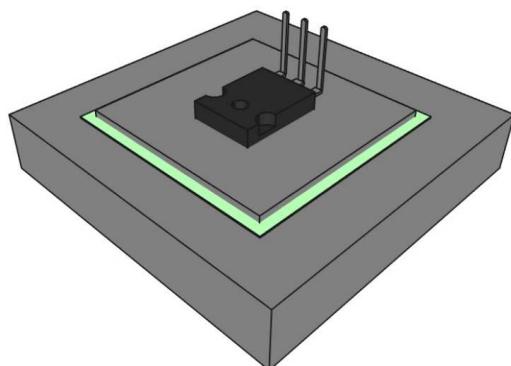
With the dimensions of the TO247 package of 21mm x 16mm this results in a thermal resistance R_{TH-CS} of 0,32°C/W. This thermal resistance is still slightly higher than the R_{TH-JC} and should be made as low as possible.

One of the best non insulating thermal contact methods is by using thermal grease between the package and the heat sink. A thermal conductivity of 10W/m·K is possible which results in negligible R_{TH-CS} when applied in a very thin layer.

- When the heat is spread out over a larger area than the TO247 package by using thermal grease and a metal plate and then couples through the thermal insulating pad, this will significantly reduce the overall thermal resistance while maintaining electrical insulation.



An aluminium heat spreader about six times larger than the TO247 package reduces R_{TH-CS} to only 0,05°C/W.



The maximum amount of heat that is produced in a MOSFET depends on the supply voltage and the gradient coil resistance.

$$P_{PEAK} = \frac{V_{SUP}^2}{4 R_{GR}} \quad \text{at} \quad I_{PEAK} = \frac{V_{SUP}}{2 R_{GR}}$$

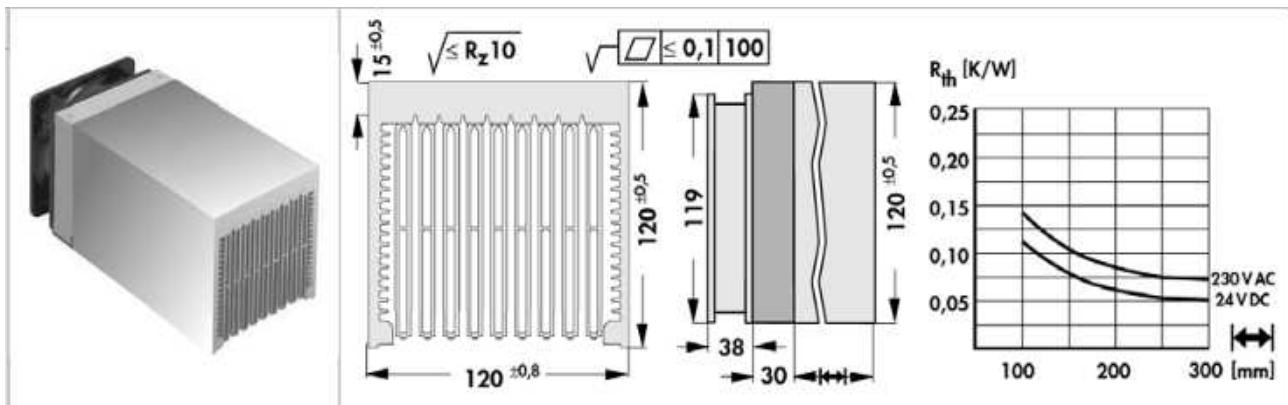
At 15V supply voltage and 0,4Ω coil resistance I_{PEAK} would be 18,75A which is higher than the maximum current of 15A, but if the input voltage is 12,5V it could happen. In that extreme case 141W of heat is produced. Under normal conditions when the maximum input voltage is 10V it would be 135W. When a 12V battery is used it drops to 90W maximum. If the combined $R_{TH,JC}$ is 0,3°C/W this results in a temperature rise ΔT between the junction and the heat sink of 40,5°C at 135W.

Three amplifiers produce heat that needs to be removed by a single heat sink. If the ambient temperature is 30°C then a total power of 3x135W should result in less than 150-30-41 = 79°C.

- This means that the heat sink should have a thermal resistance of less than 0,2°C/W which is possible with forced air cooling.

Especially the heat sinks that have an air chamber between the fan and the heat sink have a very low thermal resistance.

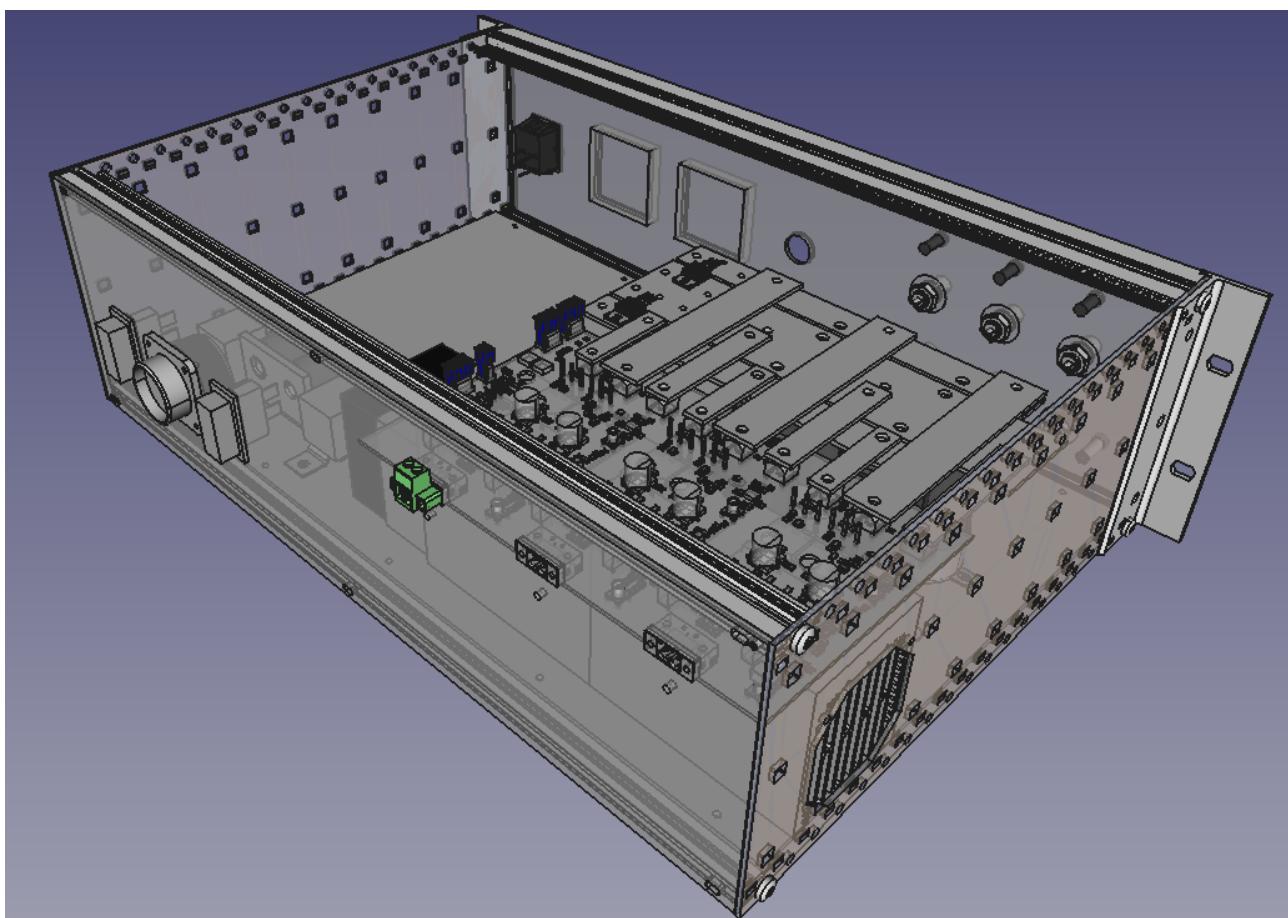
Fischer LA V series heat sinks

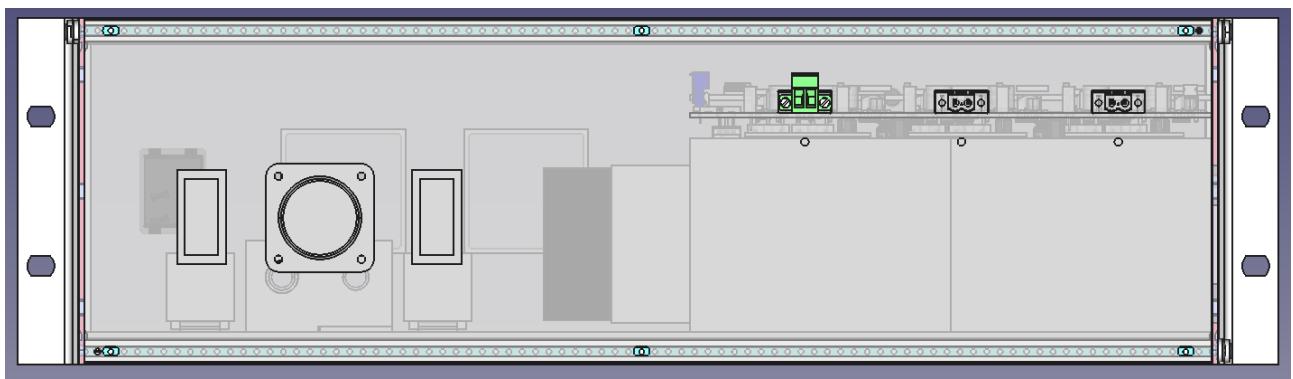
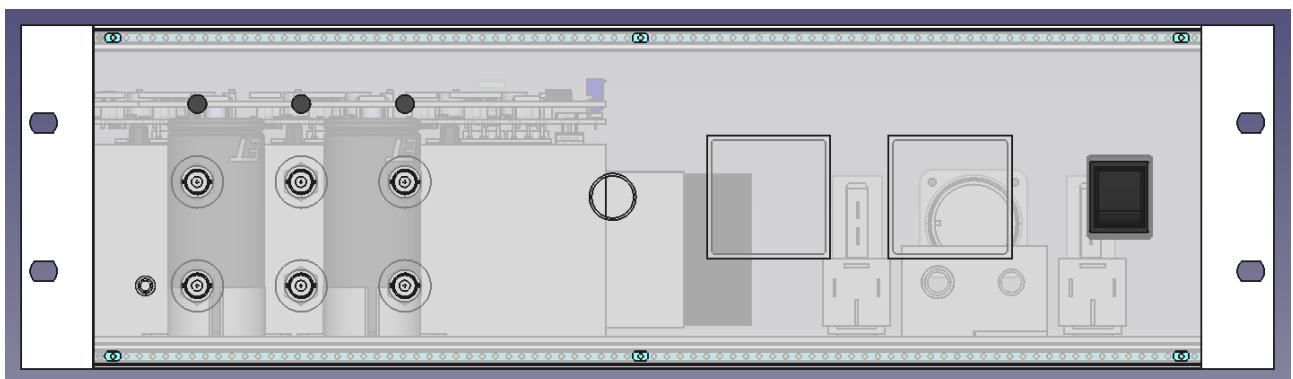
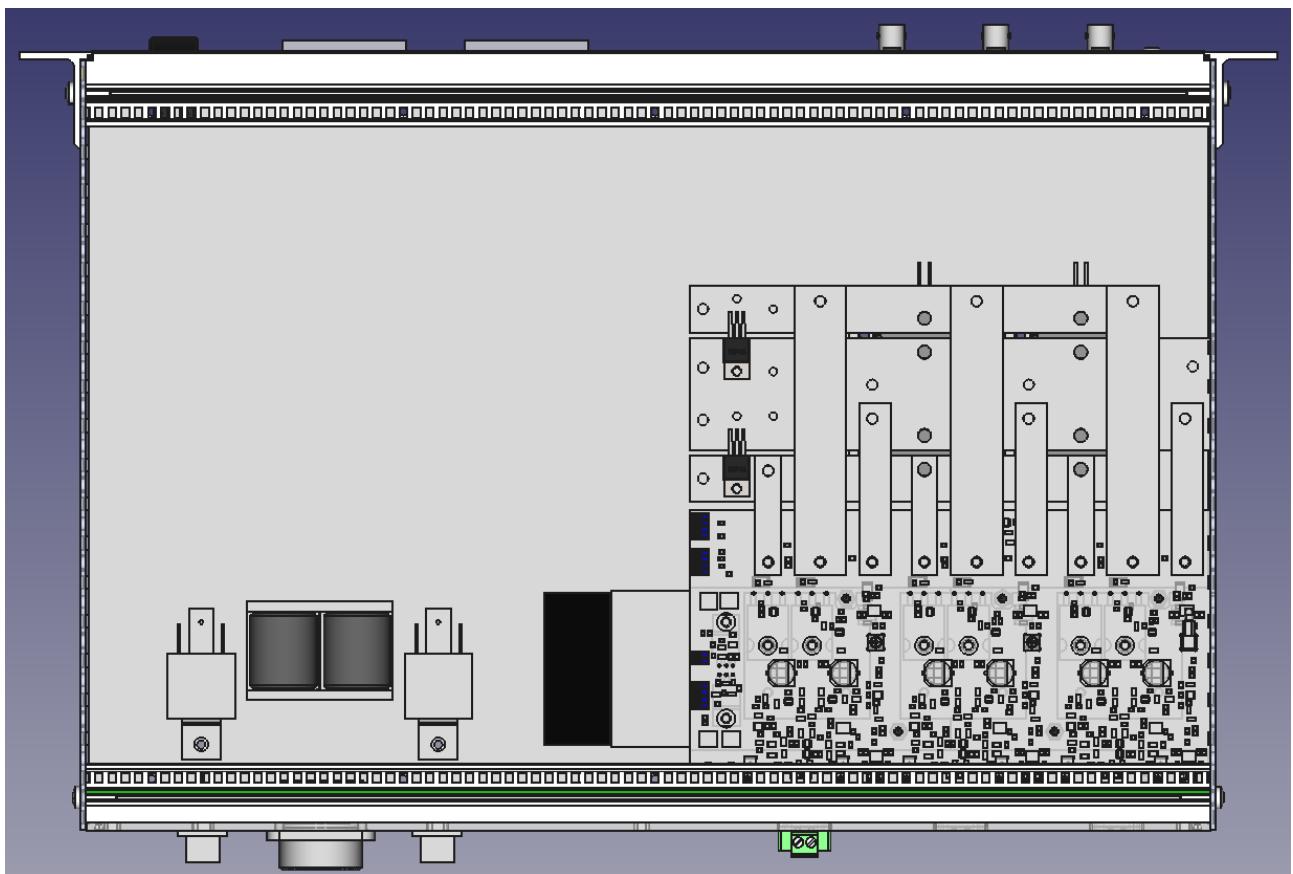


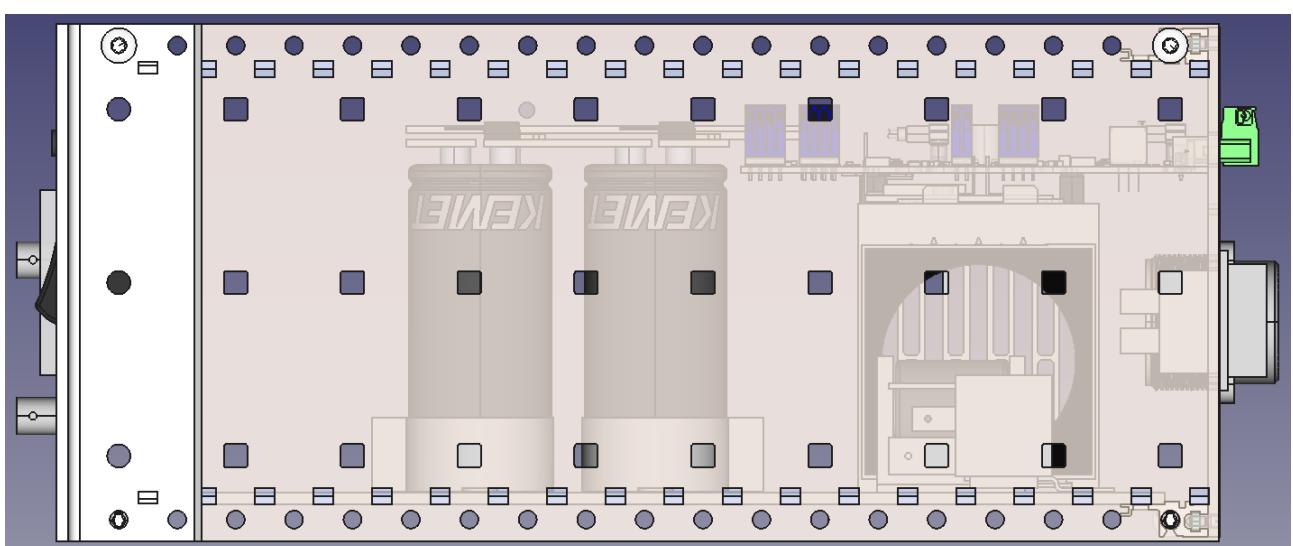
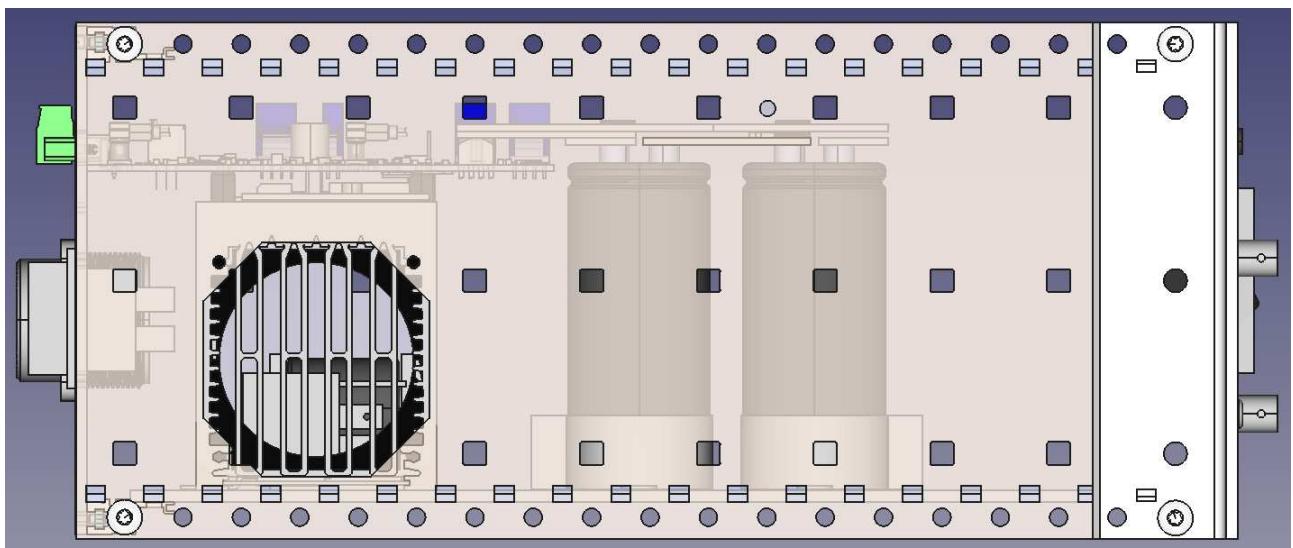
9.2 Construction and Layout

Important points to consider in the layout and construction:

- The decoupling capacitors must be close to the supply terminals of the PCB to reduce the parasitic inductance.
- The air flow of the heat sink should not be blocked and hot air must leave the enclosure directly. The decoupling capacitors should stay cool.
- The electronics should be easily accessible for testing, measuring, offset trimming or even repair.
- The input and monitoring BNC connectors will be located on the front panel such that the cable length inside the enclosure and the space between the connectors is minimized up to a practical level.
- The gradient coil screw connectors on the PCB should stick through the back panel.
- Parasitic cable inductances should be kept low to minimize magnetic stray fields and mutual inductances.
- The power supply connector will be placed on the back panel.
- A short and wide aluminium strip or corner molding maybe should connect the star point GND at the decoupling capacitors to the enclosure. All parts of the enclosure must be electrically well connected. This defines the GND of the BNC connectors.







10 Testing and Lessons Learned

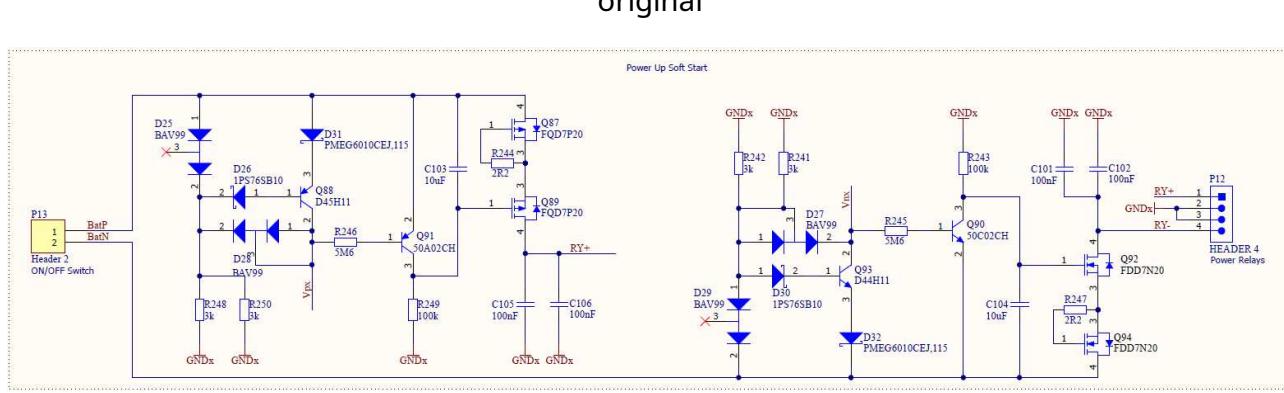
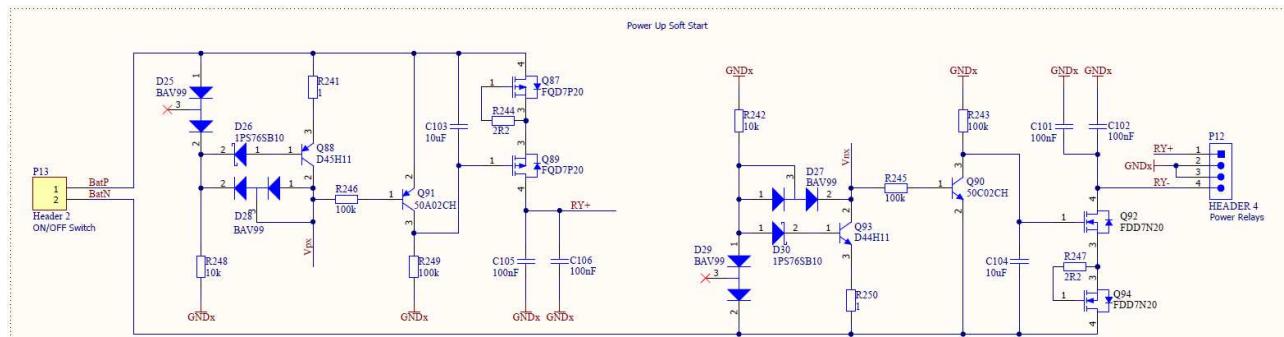
10.1 Supply

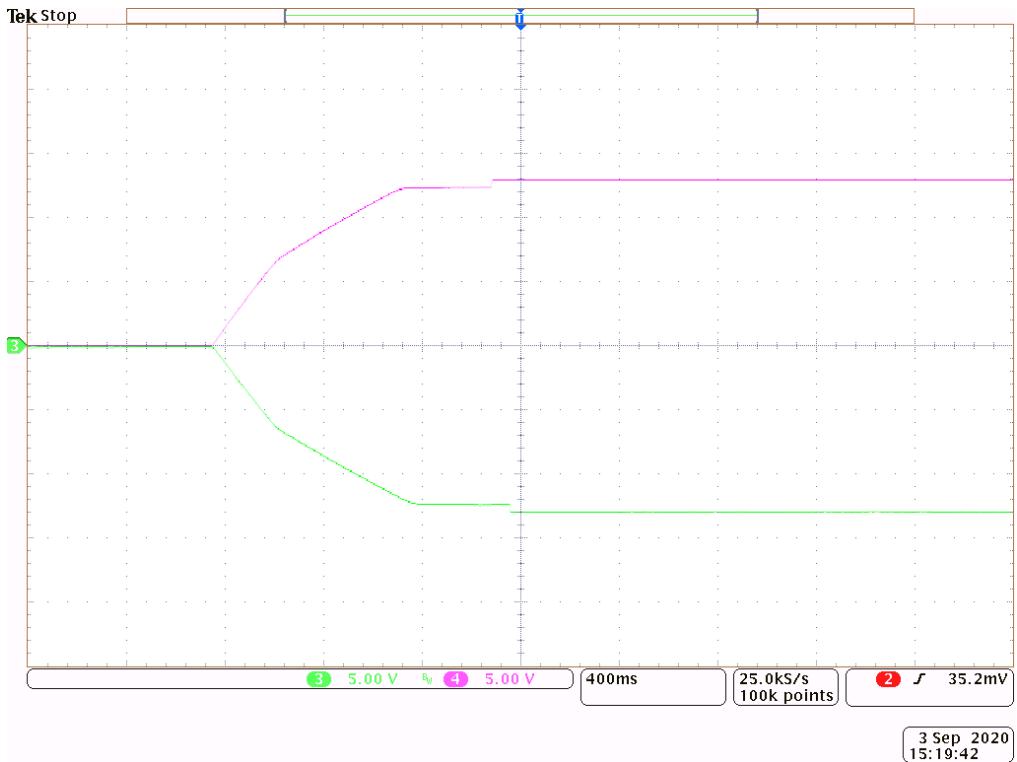
10.1.1 Soft Start Circuit

The D4xH11 transistors can operate in reverse mode after switching off the supply switch. This was anticipated but happened still in a different way. This prevents the relays from switching off. When $V_{EB} > V_{EBzener}$ a reverse current starts to flow from emitter to collector (in the NPN case) which is easily capable of keeping the relay powered via the relay coil itself. Especially the negative supply soft start was sensitive to this. But for high enough supply voltage the positive soft start could also show this effect. To prevent reverse current through Q88, Q93 the 1Ω resistors R241 and R250 were replaced by schottky diodes.

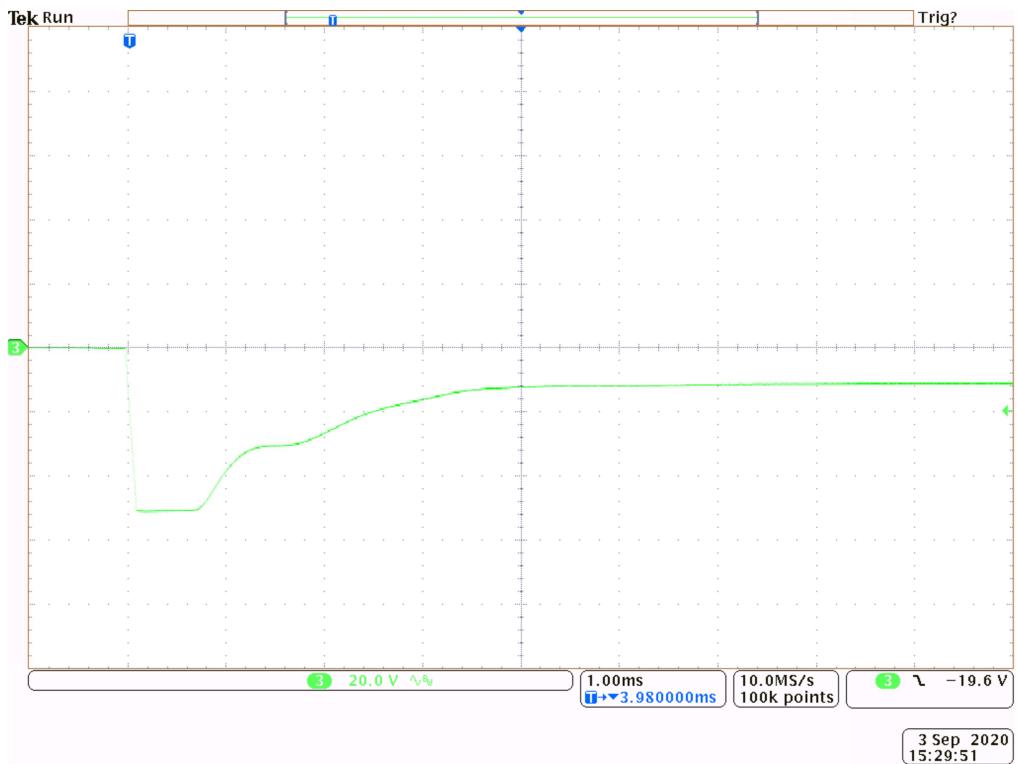
- Reverse currents become possible when after switching off the supply voltage the V_{CE} depends on another current path that could pull the voltage up over the V_{EB} zener voltage. This was not accurately modeled in spice and therefore overlooked in simulation too.

Also the charging current for the capacitors was too low. When the fan starts up it draws 130mA @24V and the total was about 350mA. The threshold for switching on the relays was never made because of this bias current. The solution was to lower the base resistor of the power transistors to 1,5kΩ for more current and increase the base resistor of Q90 and Q91 to 5,6MΩ to make it easier to switch off.





The slope reduces after the voltage across the fan is high enough to start it up. The relays switch on about 400ms after reaching the maximum charge voltage.

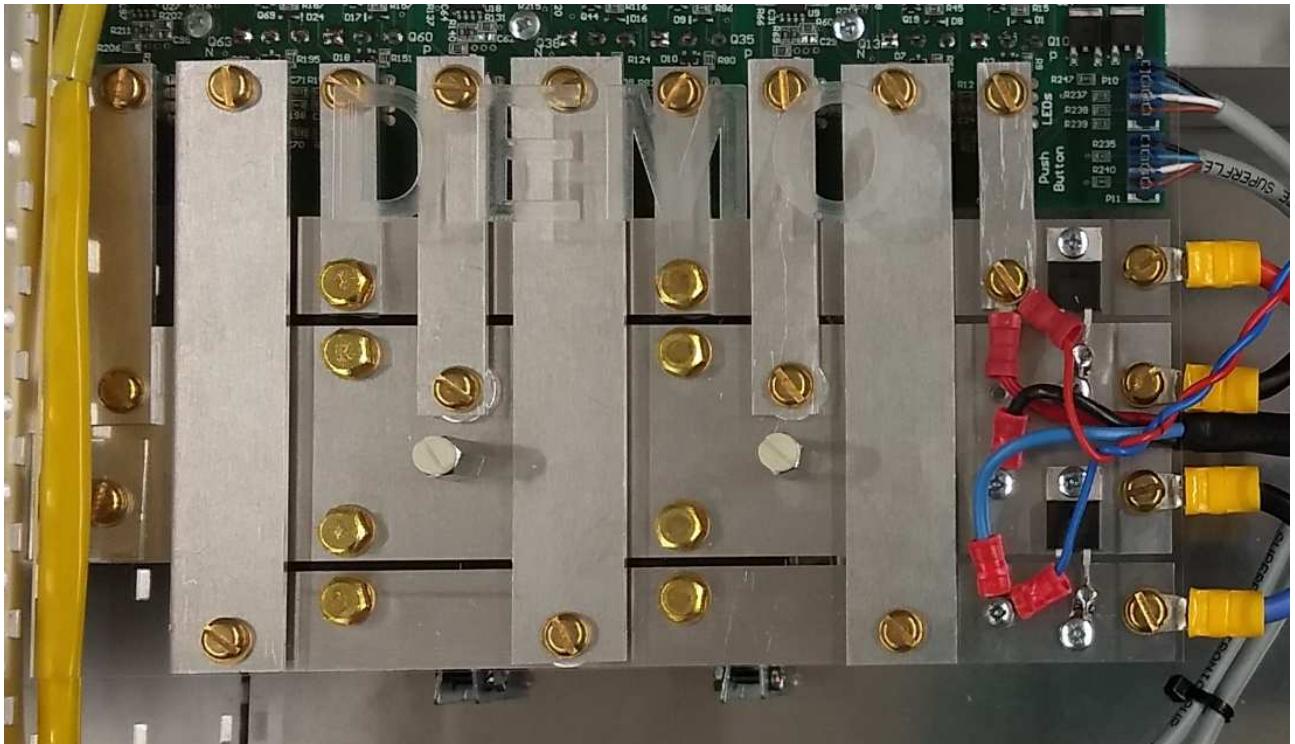


At powering down the voltage across the relay coil jumps about 50V down from 13V to -37V and is clamped by the TVS diode P6KE39CA at its terminals. This AC plot shows only the step. The relays switch off immediately after the main switch is switched off.

$$V23134-J1052-D624 \text{ 12V } ++1912; \quad L_{\text{relay}} = 202\text{mH}, R_{\text{relay}} = 98\Omega (\text{@}50\text{Hz})$$

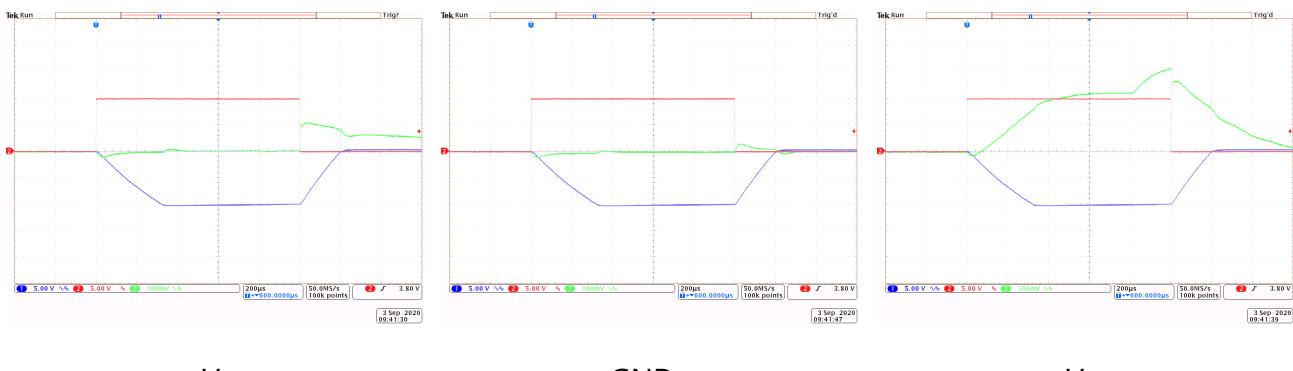
10.1.2 Supply Voltage Ripple

There was a significant contact resistance between the aluminium capacitor plates and the strips that connect to the PCB.



It seemed that the aluminum spacer rings of 2,5mm thick did not result in a low contacts resistance, even after flattening their surfaces. Originally RVS screws were used which did not help a lot in the contact resistance. After replacing them by brass screws the contact resistance dropped to 14,6mΩ.

→ Brass screws help in making low resistance connections



Vp

GND

Vn

These measurements show -15A pulses; Vin (Red), Iout (Blue), Vripple (Green). The power supply had a 10A current limit which is why at the end of the pulse the voltage drop increases.

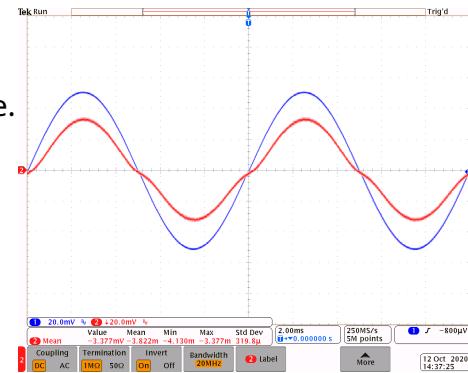
10.1.3 Under Voltage Lock Out

The thresholds where the alarm trips were measured to be at 10,50V as intended.

10.2 Biasing

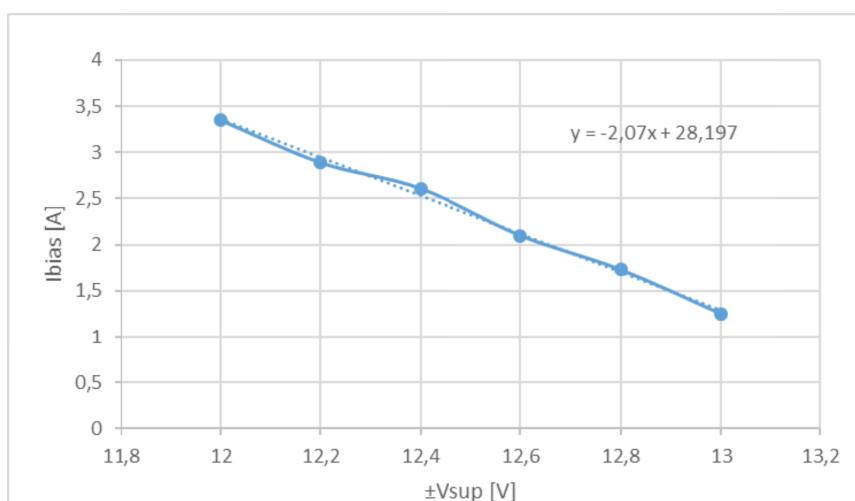
10.2.1 Procedure

- Use a power supply of $\pm 13,0V$ with the current limit set at about 5A
- Connect a coil to the output of an amplifier (or all 3)
- Enable the amplifiers with the push button on the front panel.
- Apply a sinusoidal input signal of 100Hz, 100mVpp
- It takes about 5 minutes after power up before the biasing is completely settled. So adjusting before then is less accurate.
- Measure the input signal and the monitoring output with an oscilloscope. Invert the monitoring output to make it easier to compare the signals.
- When the signal on the monitoring output shows cross over distortion increase the bias current by turning the potentiometer clockwise. The left potmeter of a channel labeled 'P' influences the positive half of the sine wave. (negative for the inverted signal). Adjust until the two signals match.
- The DC output current, measured with a multimeter in series with the coil, should be balanced to 0mA by adjusting both potmeters such that the extra current from the power supply is about 0,2A. When all amplifiers are unbiased the supply current is about 0,35A so after biasing all the amplifiers it will be 0,95A or slightly more.

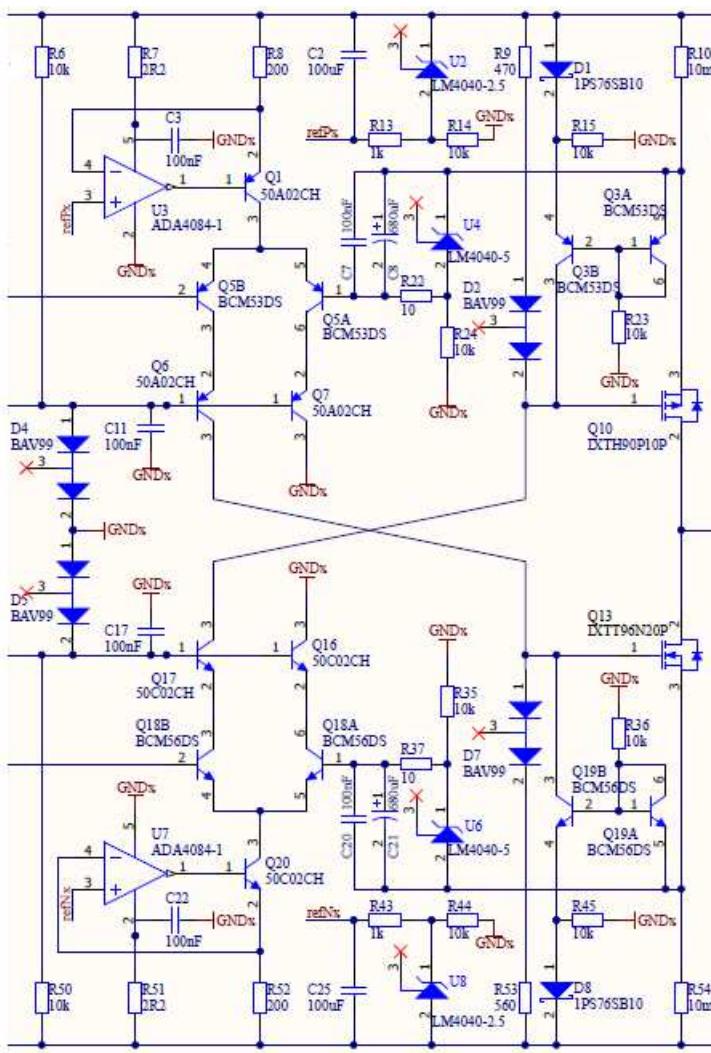


10.2.2 Supply Voltage Influence

Fully charged batteries gave a supply voltage of $\pm 13,05V$ after letting them rest for a few minutes after charging. It was noticed that the bias current increased as the supply voltages drop.



This was not expected since the biasing is made relative to the supply voltages to prevent this. Also simulation didn't show this effect.



The dependence on the supply voltage came from the way the CB stages, Q6,7,16,17, get their bias voltage. It is made by D4 and D5 and is about $\pm 1,2V$ referenced to GND. These voltages are required at the input stage and conveniently reused at the gain stage.

The latter was a mistake because when the supply voltages change so do V_{CE} of Q5 and Q18. These are configured as differential stages with matched dual transistors to become independent of V_{BE} as function of temperature.

The problem that is created now is that as V_{CE} changes with the supply voltage, at constant collector current, so does the dissipated power in each transistor. When the total bias current of the differential stage is unequally distributed this causes one transistor to heat up more than the other. This ΔT results in a ΔV of $-2mV/K$ across the terminals of the DV stage.

This offset voltage is present at the $10m\Omega$ sense resistors which convert it to $-0,2A/K$ change in bias current in the MOSFETs.

It doesn't matter so much for the output current since that is controlled by the feedback loop, but it does mean that the largest positive offset will determine the bias current.

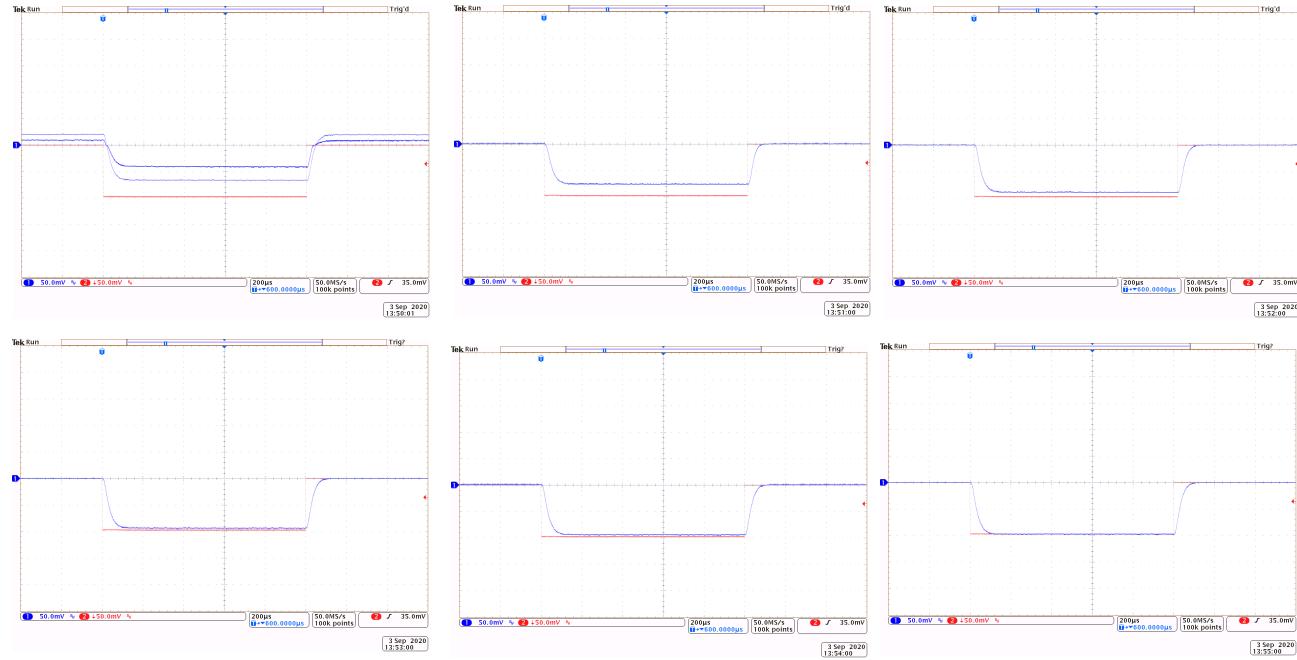
The total bias current of the gradient amplifiers decreases with $2A/V_{DC}$. Each amplifier draws on average $0,66A/V_{DC}$ less current which equals a change of ΔT of $3,3^{\circ}C/V_{DC}$ supply voltage.

A solution would be to make the bias voltage for the CB transistors relative to the supply rails like all other biases voltages and have no change in power at all in the DV stage and balance the currents for even better temperature performance.

Since changing the bias voltages to be relative to the supply rails means a change in the circuit topology it was chosen to only balance the differential stages to minimize the bias drift.

- It was overlooked that for the differential gain stage equal power dissipation and therefore temperature of each transistor is critical for the bias current stability since the feedback resistance of the voltage to current amplifier is very low. After all this bias feedback makes the gain stage an input stage too for low output current.
- The PCB temperature at the input stage also seems to influence the bias current which might be the reason why it takes about 5 minutes to settle after power up.

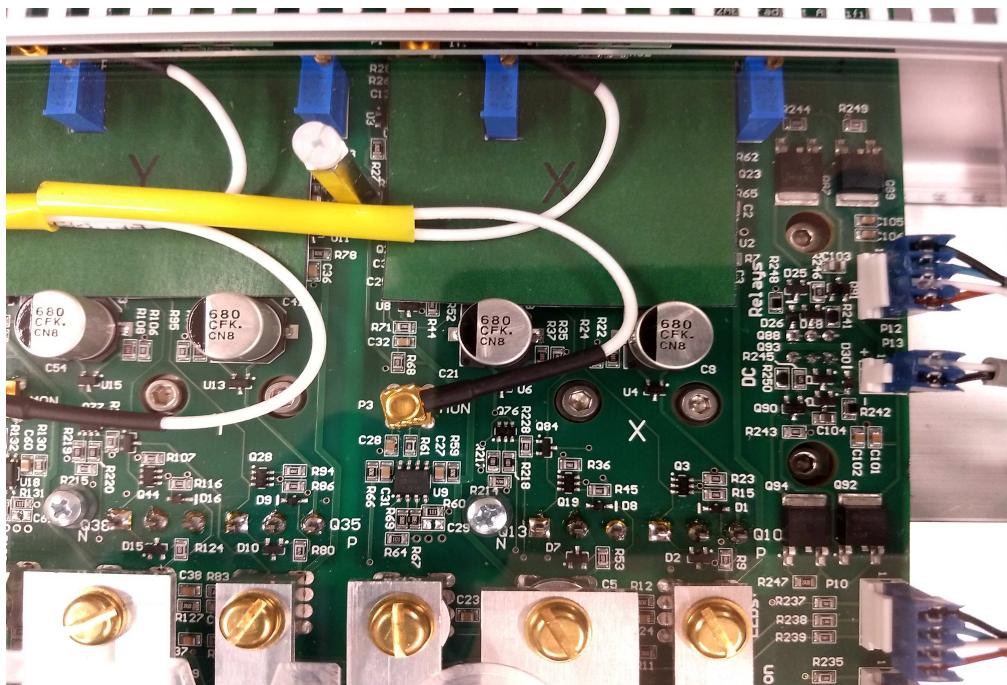
Immediately after powering up the amplifiers need about 3 minutes to settle.



Measurements from immediately after powering up and 5x 1 minute intervals.

10.2.3 Temperature influence

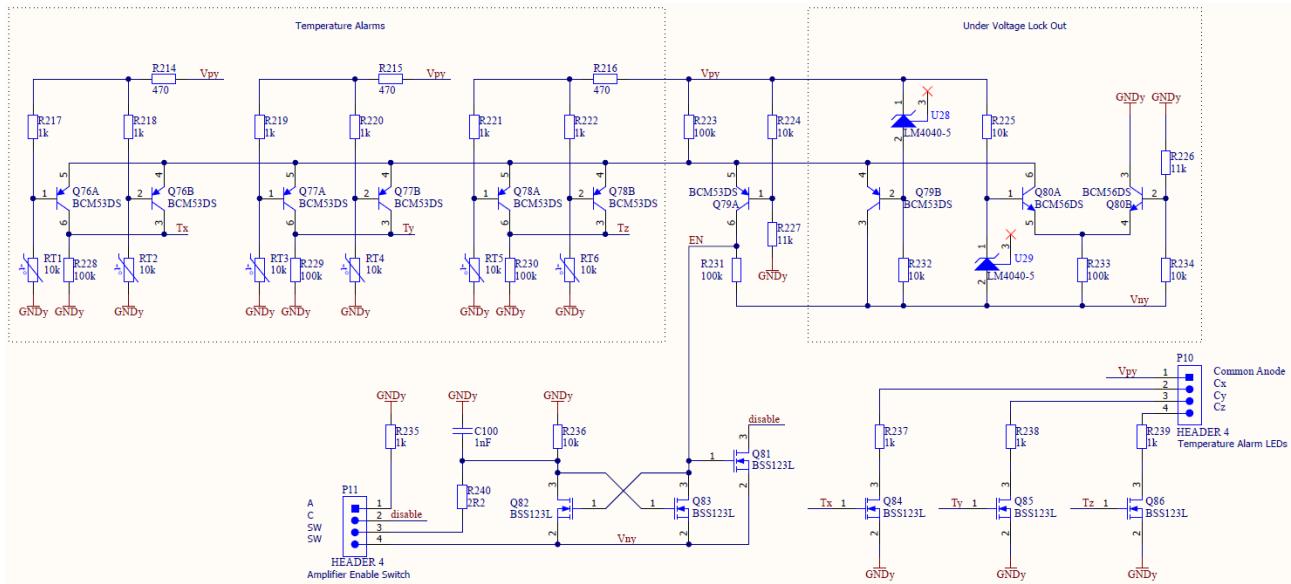
Temperature fluctuations also have influence on the biasing as was expected in the design stage. A perspex cover was placed to reduce air swirls. This turned out to be effective but even more improvement was made by placing paper covers directly over the input- and gain stage. **This made the bias current very stable.**



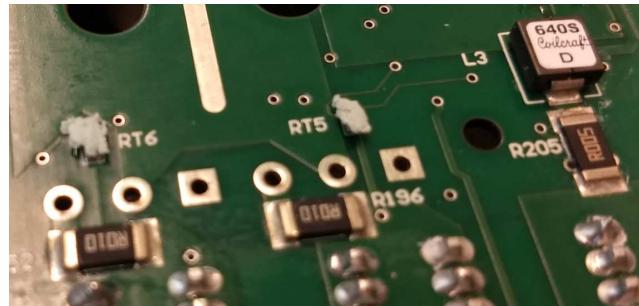
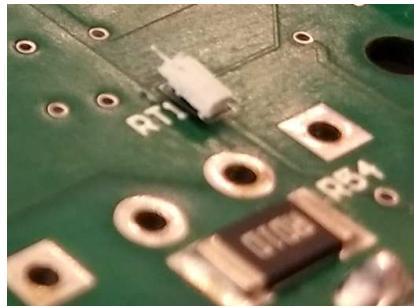
10.3 Thermal Behavior

10.3.1 Temperature Alarms

A test was done with the fan disconnected and 180W dissipation in channel X. All thermistors showed a drop in their voltage which means that all of them were thermally coupled to the MOSFETs. After 5 minutes or so the temperature alarm tripped and it disabled the amplifier. The indication LED was already indicating a high temperature just before the alarm tripped.



Making this coupling between the MOSFETs and thermistors was a bit difficult to do with the thermal pad that also isolates the heat spreader from the heat sink.



10.3.2 Heat Spreaders

The heat spreaders seem very effective as it took about 5 minutes before the temperature alarm tripped. The 4 screws were tightened with 0,75Nm to distribute the pressure equally, reach optimum thermal resistance with the MOSFETs and make all heat spreaders equally.

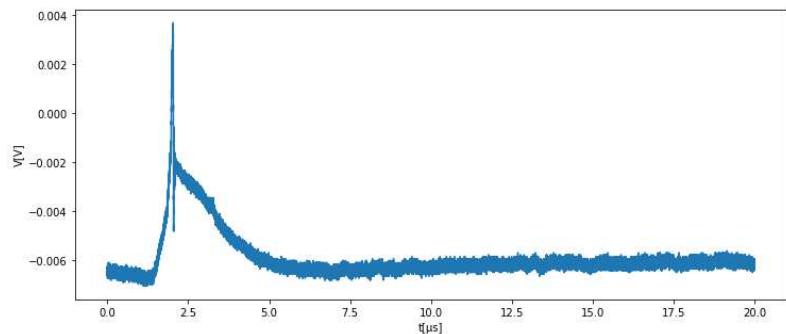
The electrical capacitance of each plate to the heat sink after tightening was $C = 192\text{pF} \pm 2\text{pF}$ @1MHz



The graphite thermal paste between the MOSFETs and the heat spreader should not create an electrical contact to the heat sink through the screw hole. This was checked with a multimeter.

10.3.3 EMI from the Fan

A ferrite ring core was placed near the fan as a common mode choke. Also its wires are connected to the big capacitors to create filtering instead of connecting them to the PCB first.

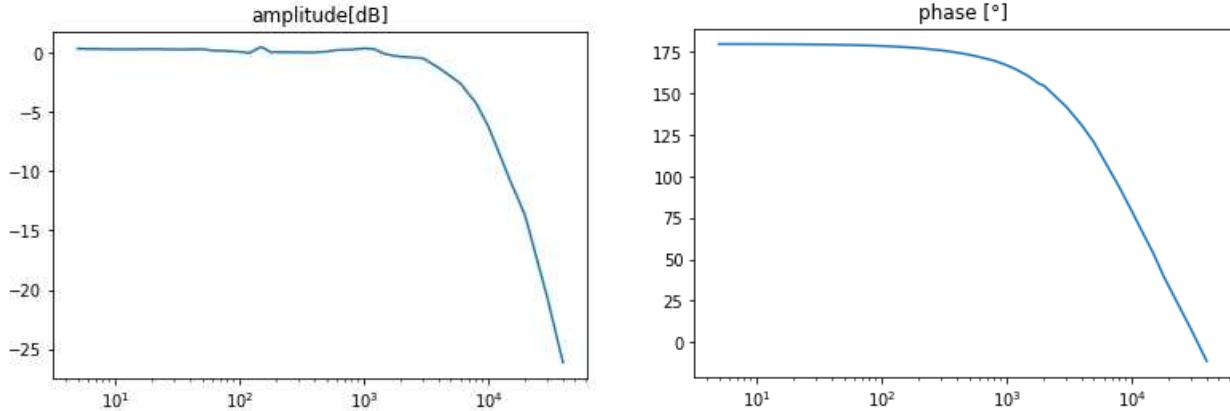


The measurement shows the signal that was picked up by the RG58 coax cable with the shielding stripped from 2 cm at the end. At the location of the PCB it was very well suppressed because of the distance and electrical shielding from the heatsink.

10.4 Transfer

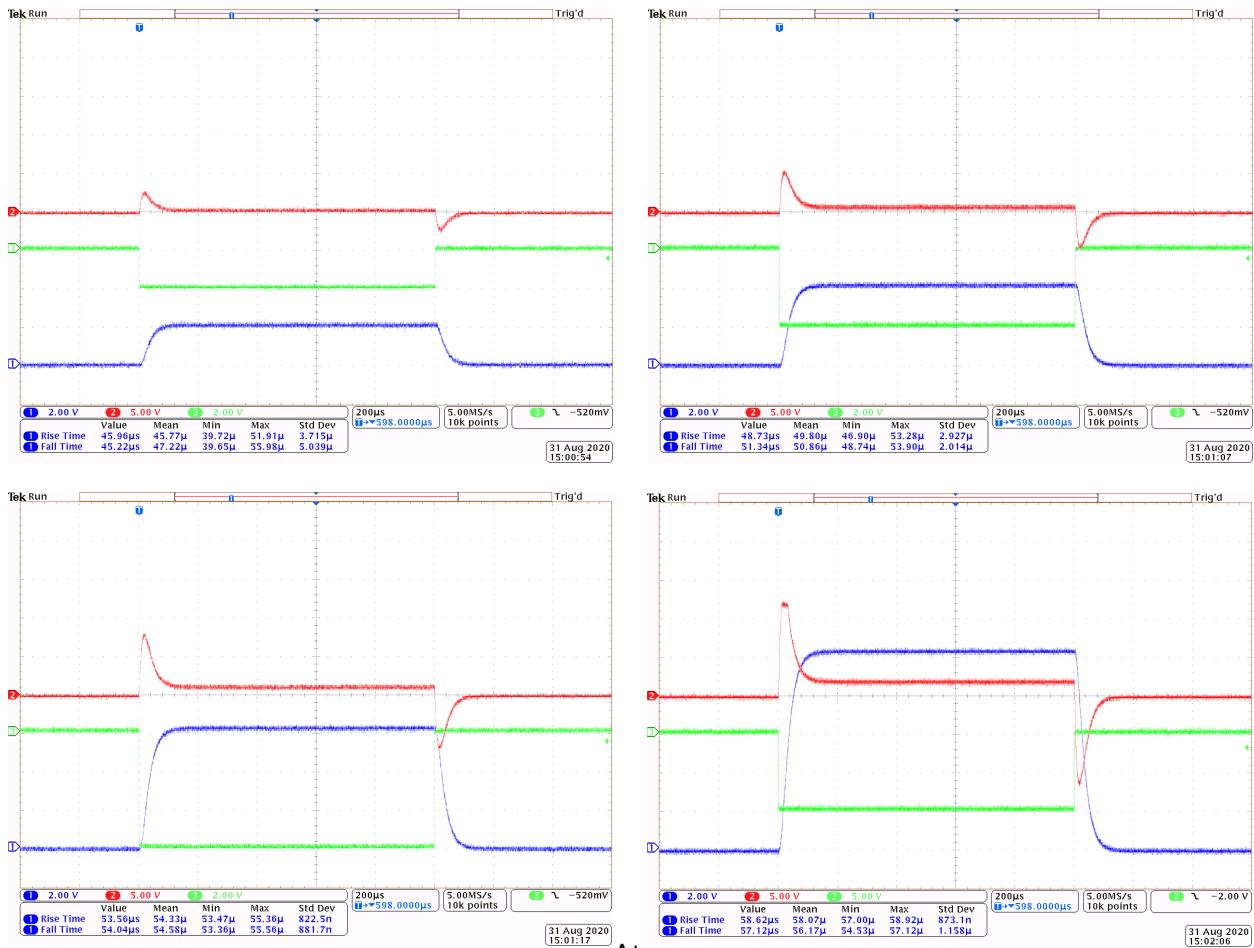
10.4.1 Bode Plot

This bode plot was measured on the monitoring output with a $36\mu\text{H}$ load inductance on the amplifier.



10.4.2 Step Response

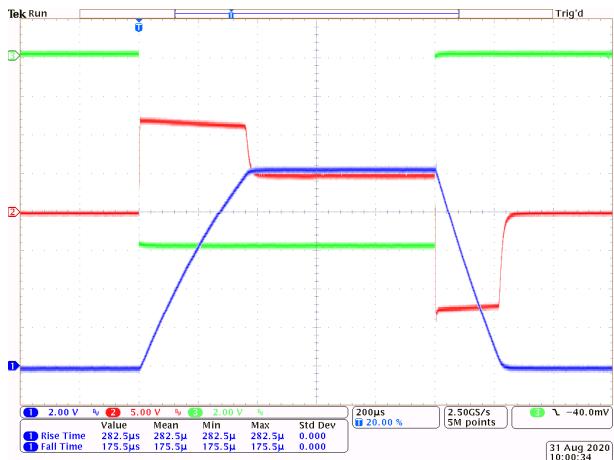
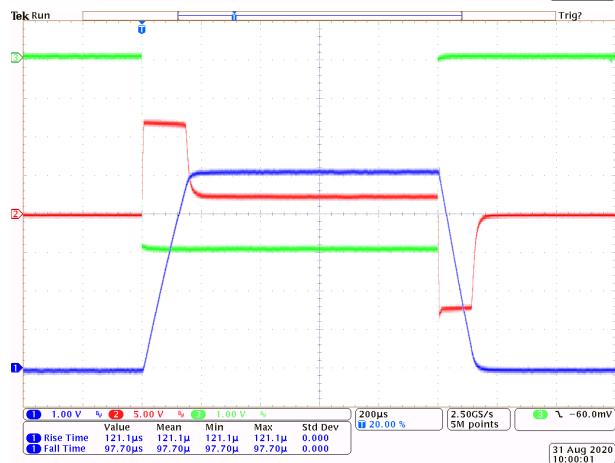
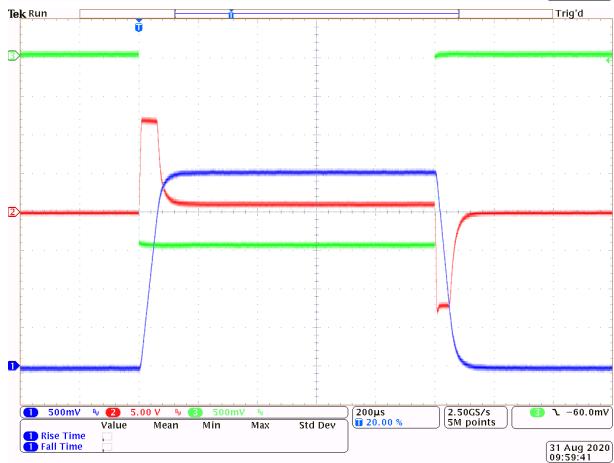
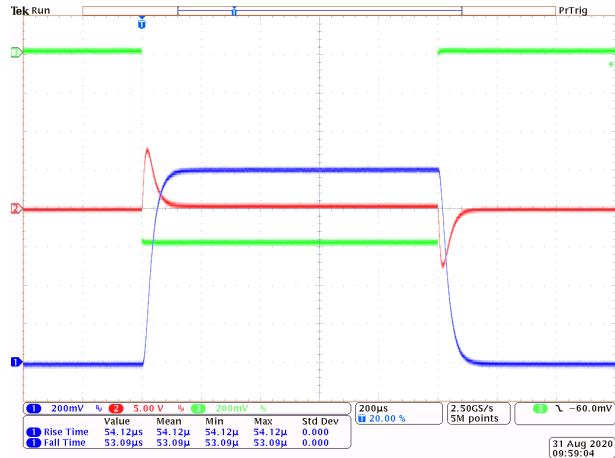
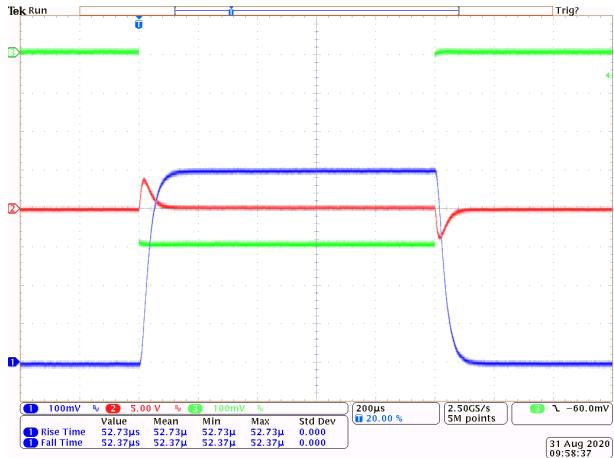
$36\mu\text{H}$ load inductance + $152\text{m}\Omega$



At

a 15A step the output starts to limit the slew rate because of clipping to the supply rail.

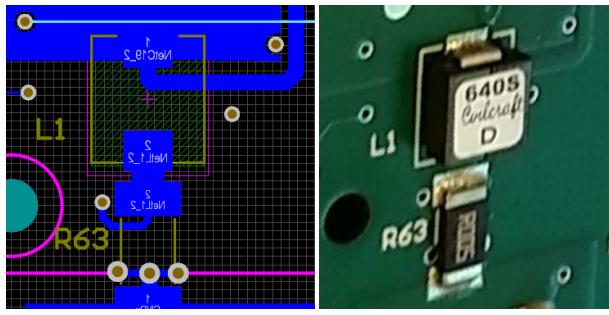
213 μ H + 316m Ω



Stable operation was shown between the range of 36 μ H to 213 μ H. Other coils were not available.

10.4.3 Static Transfer

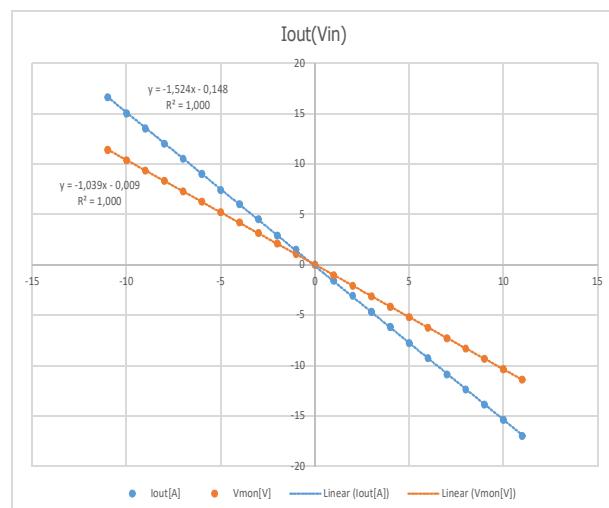
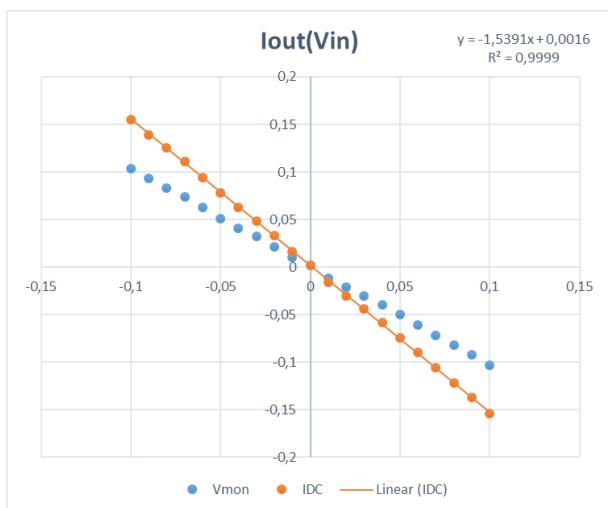
Small and large current static transfer were measured with a multimeter and the monitoring output. A gain correction was made because the gain was 10% too low.



It seems that even though the parasitic resistance of the inductor is specified as 0,123mΩ and Kelvin contacts are made in the PCB layout, the total parasitic series resistance adds up to 0,5mΩ (10% of the 5mΩ resistor).

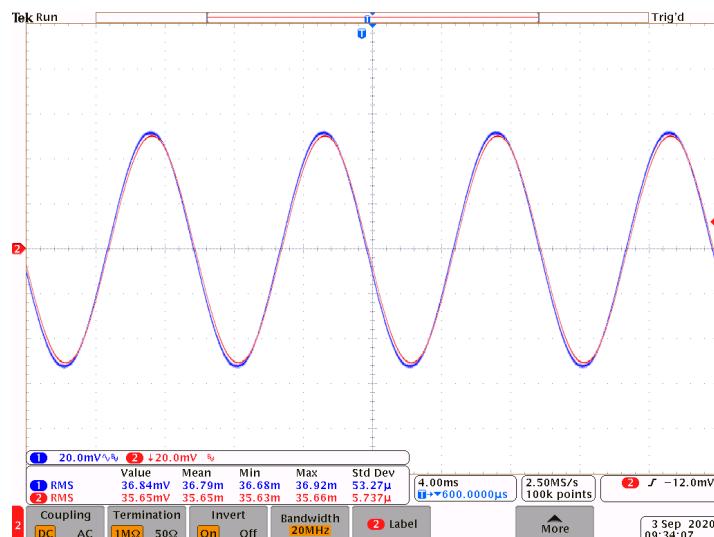
This might be explained by the trace that connects L1 and R63 together with the solder joints.

The solution is to lower the resistor that converts the input voltage to a current from 1,3kΩ to 1,15kΩ. This results in the following transfer.



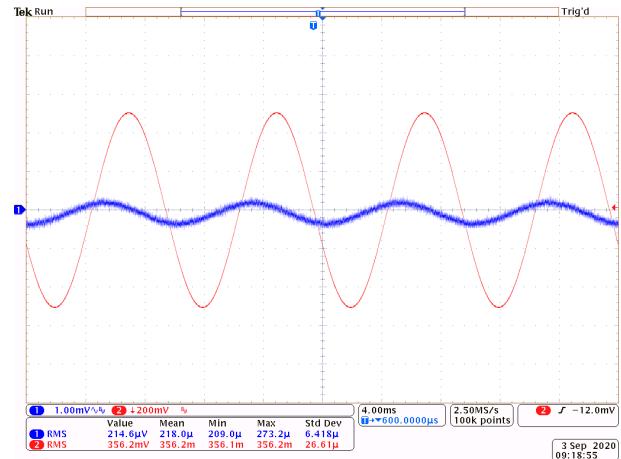
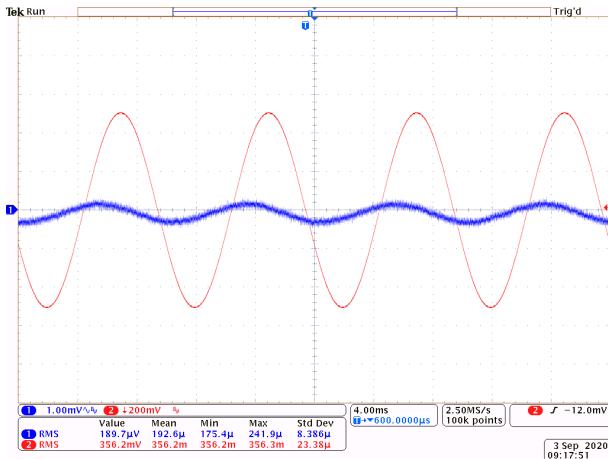
10.4.4 Small Signal

100Hz 150mA-pp small signal response: input (Blue), monitoring output (Red)



10.4.5 Cross Coupling

Cross coupling with uncoupled coils



XY -65dB

XZ -64dB

When all three coils are wound on top of each other to deliberately create worst case coupling the amplifiers showed unstable behavior by low amplitude high frequency oscillations.



→ It turned out that the negative output terminal was sensitive to current injection. This could be either capacitive or inductive. The feedback loop would compensate for this and create a coupling back to the other coils.

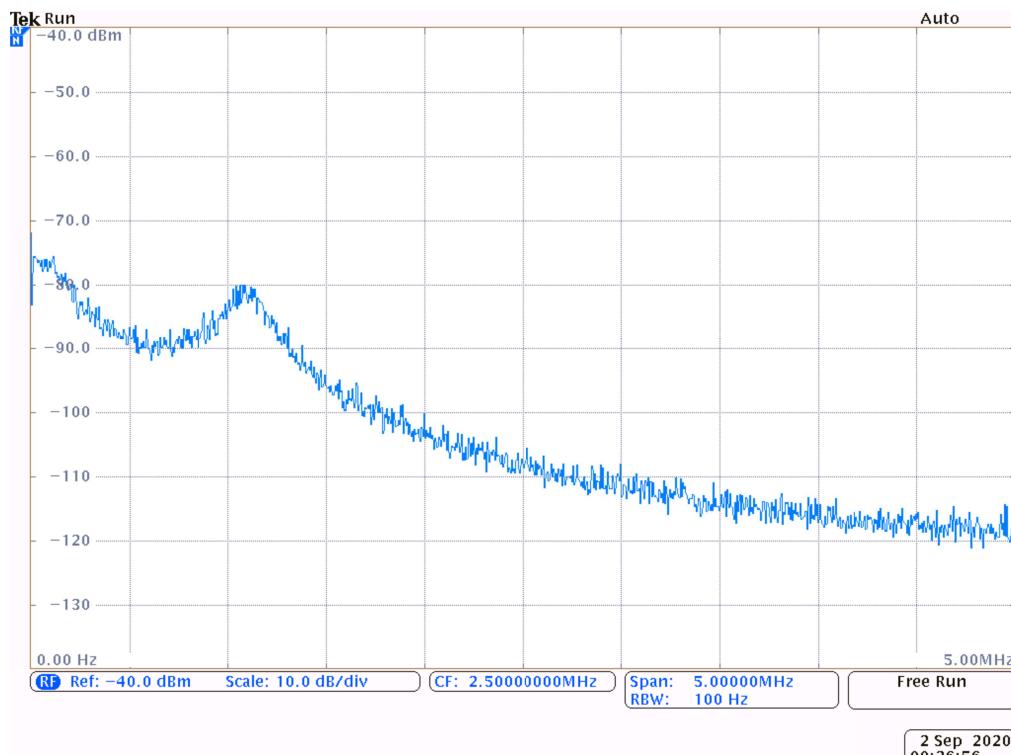
To solve this the bandwidth of the feedback network was limited with a 100nF capacitor to GND at the input of the amplifiers. The modified feedback network is shown below.



10.5 Noise

Noise can not be measured with the monitor output since the AD8221 that measures the voltage across the $5\text{m}\Omega$ feedback resistor, produces too much noise itself to be able to do that. A current probe was used but also produced more noise by itself than required for the measurement. No successful low frequency current noise measurement was made.

The output voltage noise was measured instead of trying to measure the current noise. At 2MHz this is especially important for the coupling to the RF coil of the MRI. The coil that was used is $149\mu\text{H}$ and $250\text{m}\Omega$. The noise floor of the oscilloscope is -120dBm in 100Hz and the input resistance was 50Ω .

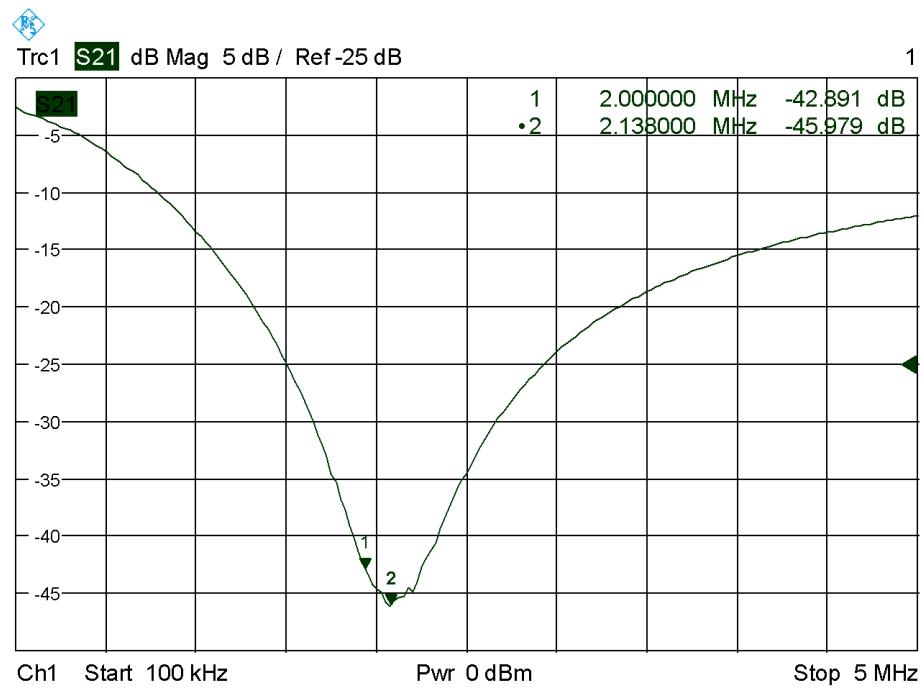
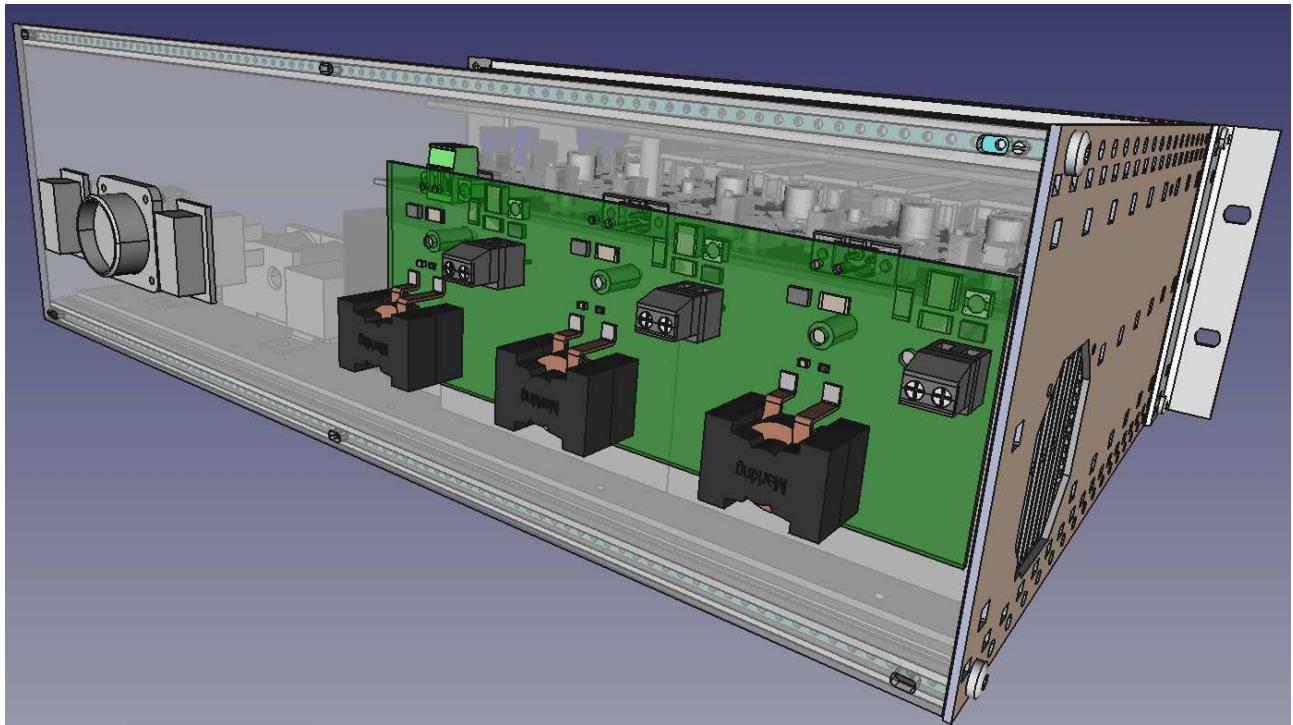


At 2MHz the noise is about -103dBm in 100Hz resolution bandwidth. Divided by 100 this results in -123dBm in 1Hz. The minimum thermal noise power $kT_B = -174\text{dBm}$ in 1Hz so it is 51dB above that. This proved to be a problem for the MRI setup because the shielding between the gradient coils and the RF coil was significantly less than that.

- The importance of having both low noise output current and -voltage was underestimated. The focus was mainly on the noise current because it was assumed that the electrical shielding could easily be very effective, making voltage noise less relevant. This turned out not to be the case.

The inductance at the output of the current amplifier gives it a high voltage gain for the input noise at higher frequencies. A way to avoid this is by adding a notch filter to the output that blocks the noise at 2MHz where the MRI is operating.

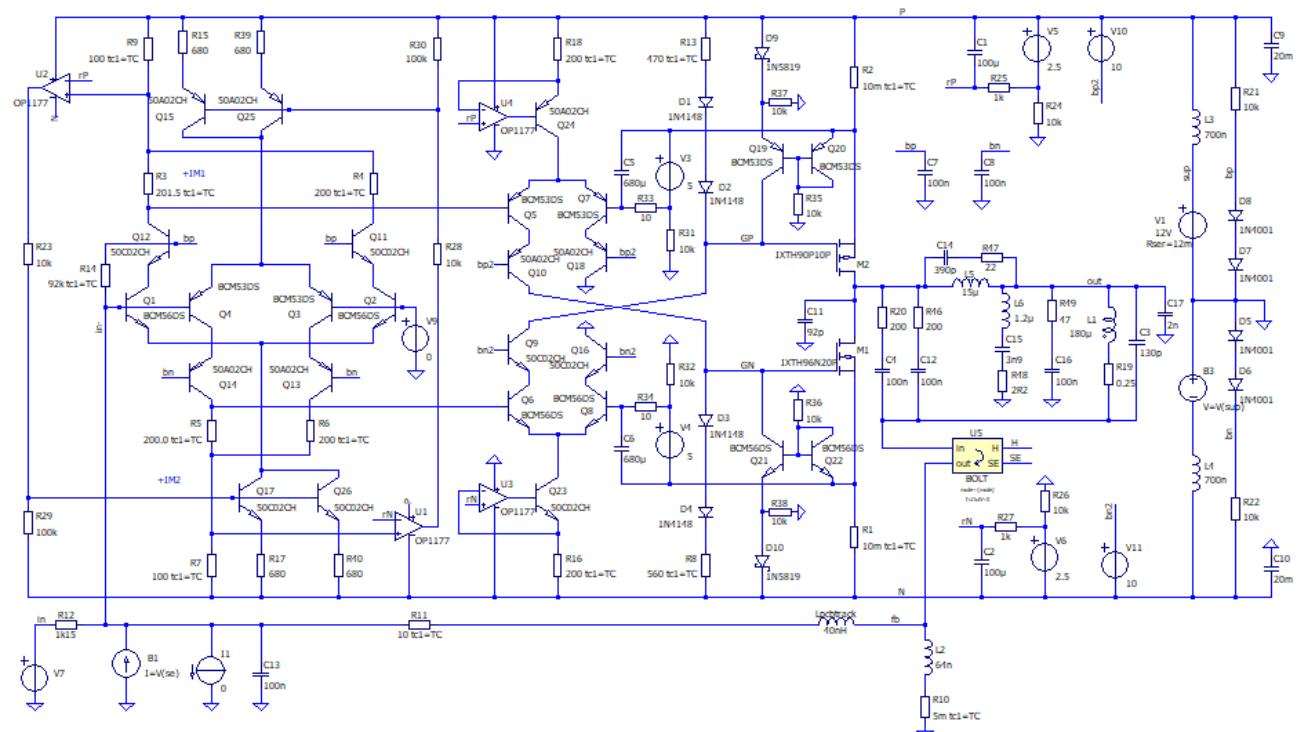
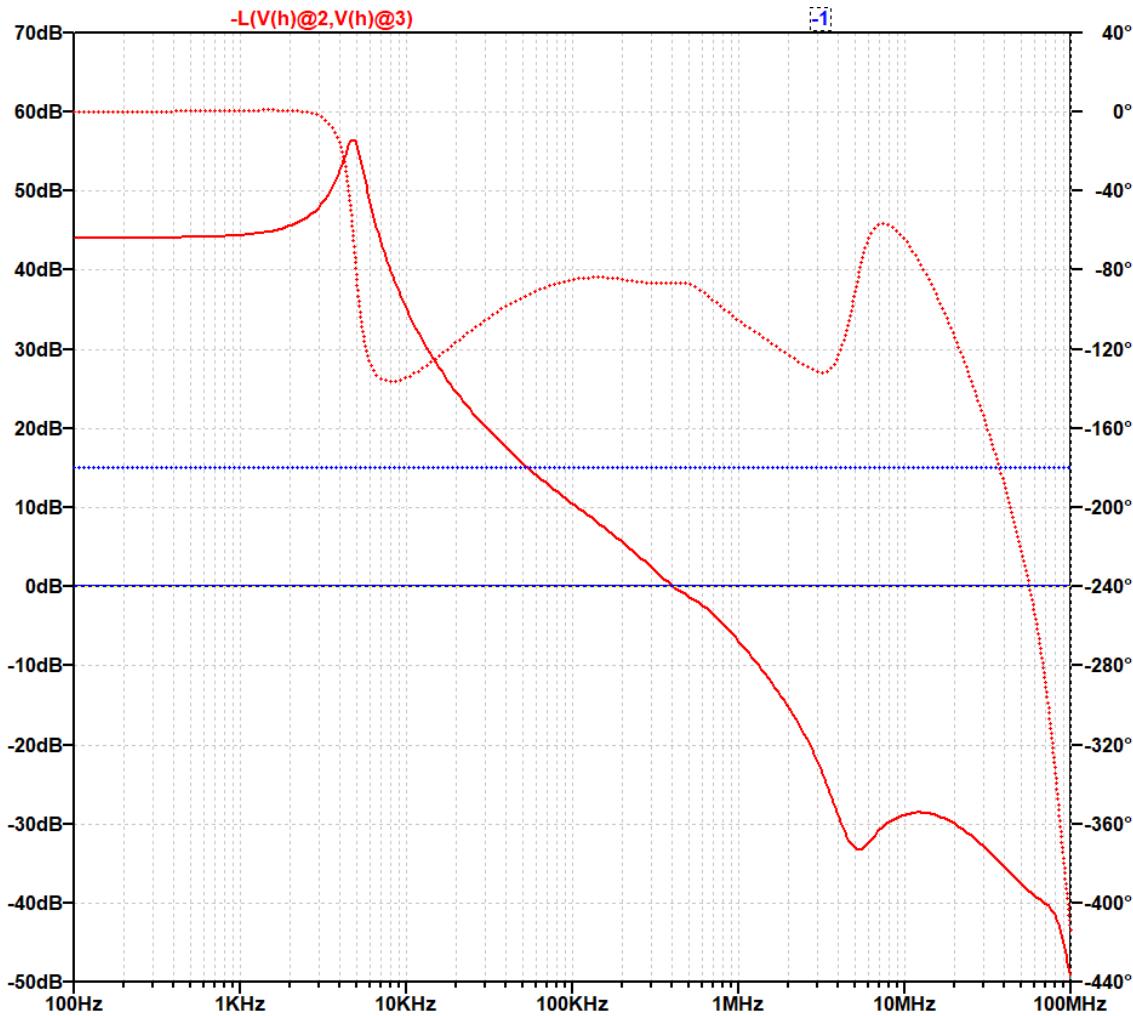
This filter was designed built and tested. It can be mounted directly on the back of the Gradient Amplifier. It is designed to have no influence on the stability of the amplifier.



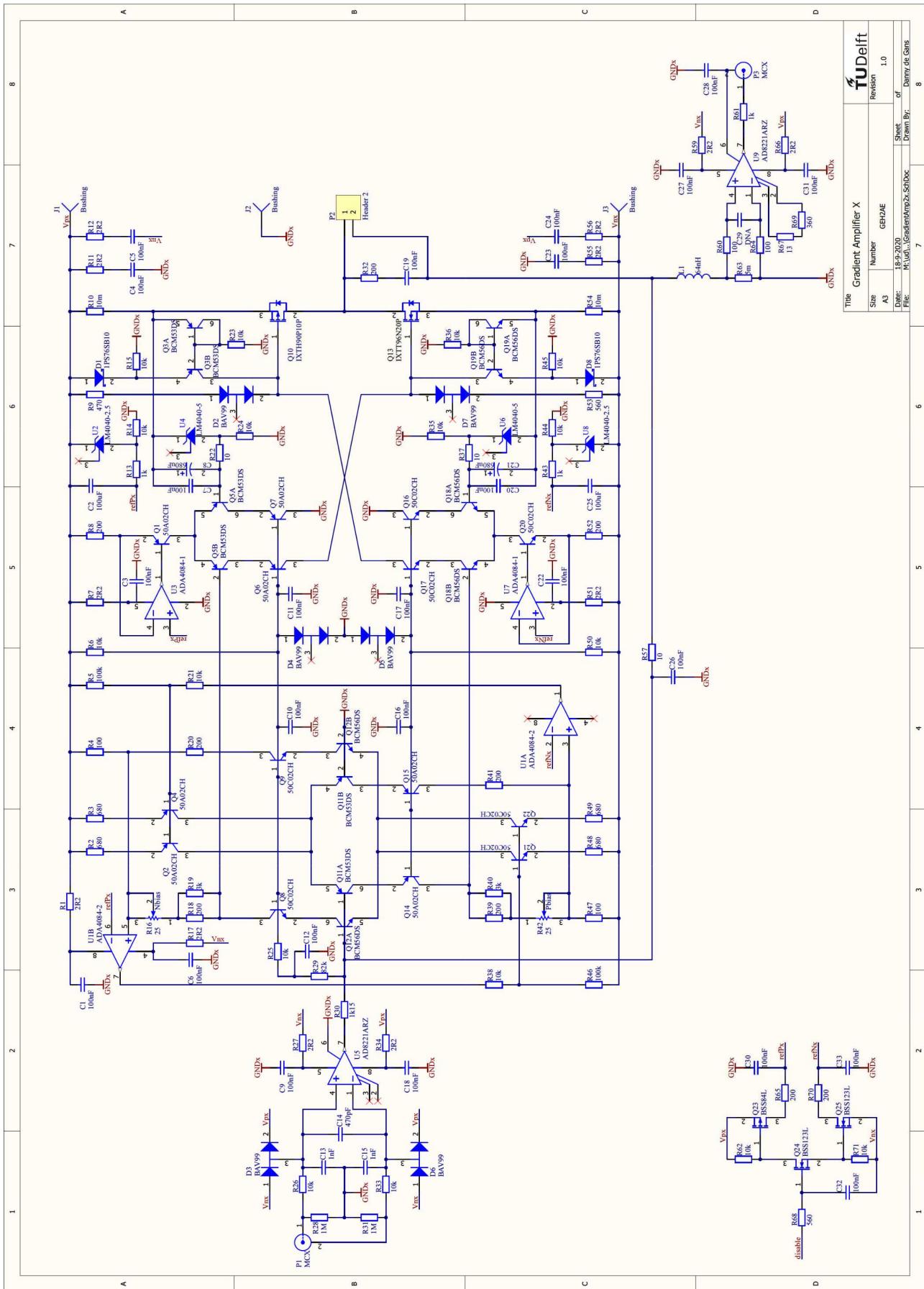
Date: 11.SEP.2020 17:33:32

Together with the shielding this should remove the EMI from the gradient coils to the RF coil completely.

Loop gain of the finalized design including filter at -1.4A output current as simulated with the Rosenstark method (the yellow block in the circuit below).



11 Final Circuits



Title Gradient Amplifier X		TU Delft Revision 1.0	
Size A3	Number GEHAE	Size A3	Number GEHAE
Date: 18-9-2020	File: H:\Uitd.\Gradiant\mp2\SchDoc	Date: 18-9-2020	File: H:\Uitd.\Gradiant\mp2\SchDoc
Drawn By: D.H. de Gans	Sheet of 8	Drawn By: D.H. de Gans	Sheet of 8

