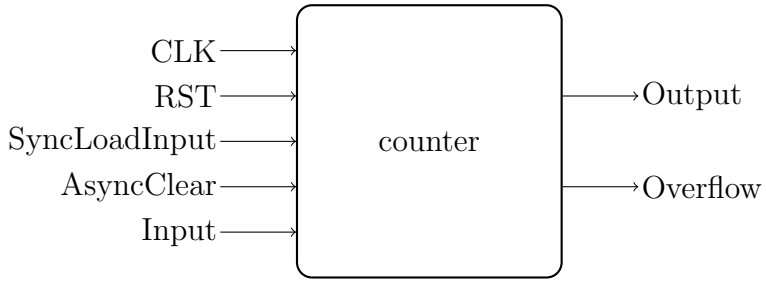
# Counter

Your task is to program the behavior of an entity called “counter”. This entity is declared in the attached file “counter.vhdl” and has the following properties:

- Input: CLK with type std_logic
- Input: RST with type std_logic
- Input: SyncLoadInput with type std_logic
- Input: AsyncClear with type std_logic
- Input: Input with type std_logic_vector of length 6
- Output: Overflow with type std_logic
- Output: Output with type std_logic_vector of length 6




Do not change the file “counter.vhdl”.

The “counter” entity shall increment the Output vector on every rising edge of the CLK signal. The input RST shall act as synchronous reset, the initial value of Output after reset shall be “000000”. When the input SyncLoadInput is set to ‘1’ then the Output vector shall be set to the value of the Input vector at the rising edge of the CLK signal. When the input AsyncClear is set to ‘1’ then the Output vector shall be set to “000000” immediately. When the Output vector changes from “111111” to “000000”, then the Overflow signal shall be set to ‘1’ until the next rising edge of the CLK signal. In all other cases the Overflow signal shall be ‘0’.

This behavior has to be programmed in the attached file “counter_beh.vhdl”.

To turn in your solution write an email to vhdl-dis+e384@tuwien.ac.at with Subject “Result Task 3” and attach your behavior file “counter_beh.vhdl”.

Good Luck and May the Force be with you.