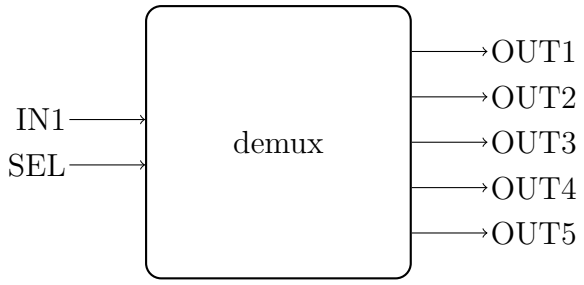
# Demux

Your task is to program the behavior of an entity called “demux”. This entity is declared in the attached file “demux.vhdl” and has the following properties:

- Input: IN1 with type std_logic_vector of length 7
- Input: SEL with type std_logic_vector of length 3
- Outputs: OUT1, OUT2, OUT3, OUT4, OUT5 with type std_logic_vector of length 7




Do not change the file “demux.vhdl”!

The “demux” entity shall demultiplex an input signal IN1 to the outputs OUT1 – 5 according to a select signal SEL. When SEL equals “000” the input IN1 shall be sent to output OUT1. When SEL equals “001” then IN1 shall be sent to OUT2, and so on and so forth as depicted in Table 1. When an output is not selected, then all its output bits shall be set to 0. When SEL selects no output then all outputs shall be set to 0.

| SEL | 000 | 001 | 010 | 011 | 100 |
|---|---|---|---|---|---|
| selected output | OUT1 | OUT2 | OUT3 | OUT4 | OUT5 |

Table 1: Selected output depending on SEL

This behavior has to be programmed in the attached file “demux_beh.vhdl”.

To turn in your solution write an email to vhdl-dis+e384@tuwien.ac.at with subject “Result Task 1” and attach your file “demux_beh.vhdl”.

Good Luck and May the Force be with you.