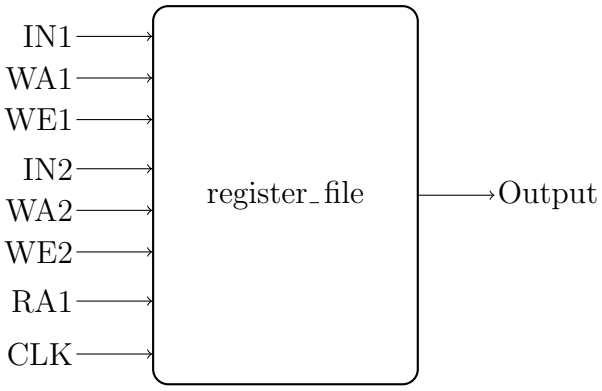
Register File

Your task is to program the behavior of an entity called “register_file”. This entity is declared in the attached file “register_file.vhdl” and has the following properties:

- Input: IN1 with type std_logic_vector of length 16
- Input: WA1 and RA1 with type std_logic_vector of length 3
- Input: WA2 with type std_logic_vector of length 3
- Input: WE1, WE2 and IN2 with type std_logic
- Input: CLK with type std_logic
- Output: Output with type std_logic_vector of length 16



Do not change the file “register_file.vhdl”.

The “register_file” entity shall contain 8 registers which have to be 16 bit wide each. The input data for registers 1 to 7 comes from the input IN1 and is written to the register specified by the write address WA1 only if the write enable bit WE1 is set to ‘1’. The write address WA2 is used to access the lower 7 bits of the register 0 seperately. The input data for the register 0 comes from the input IN2 and shall only be written if the write enable bit WE2 is ‘1’. The output of the entity is the content of a register selected by the read address RA1. See Figure 1 for a structural representation of this register file.

Changes of input signals shall become effective at a rising edge of the input CLK signal.

In a situation when the write address WA1 is identical with the read address RA1 and WE1 is ’1’, then the currently input data IN1 shall be passed through at the next rising edge of the input CLK signal to the Output. On the contrary, for special register 0, if a simultaneous read and write (WE2 is ’1’) from this register occurs, then the input data

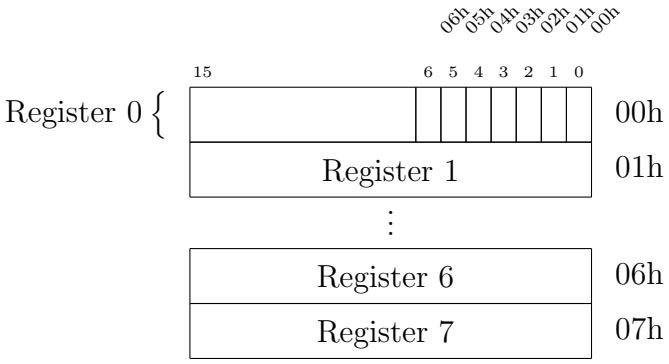


Figure 1: The layout of the register file. Addresses are given as a hexadecimal representation of the binary value.

IN2 shall be bypassed immediately to the Output (at the appropriate bit position specified by WA2).
This behavior, described above, has to be programmed in the attached file "register_file_beh.vhdl".

To turn in your solution write an email to vhdl-dis+e384@tuwien.ac.at with Subject "Result Task 4" and attach your file "register_file_beh.vhdl".

Good Luck and May the Force be with you.