Projet ECE_5RO07_TA
MPSOC

MULTIPROCESSOR SYSTEM ON CHIP

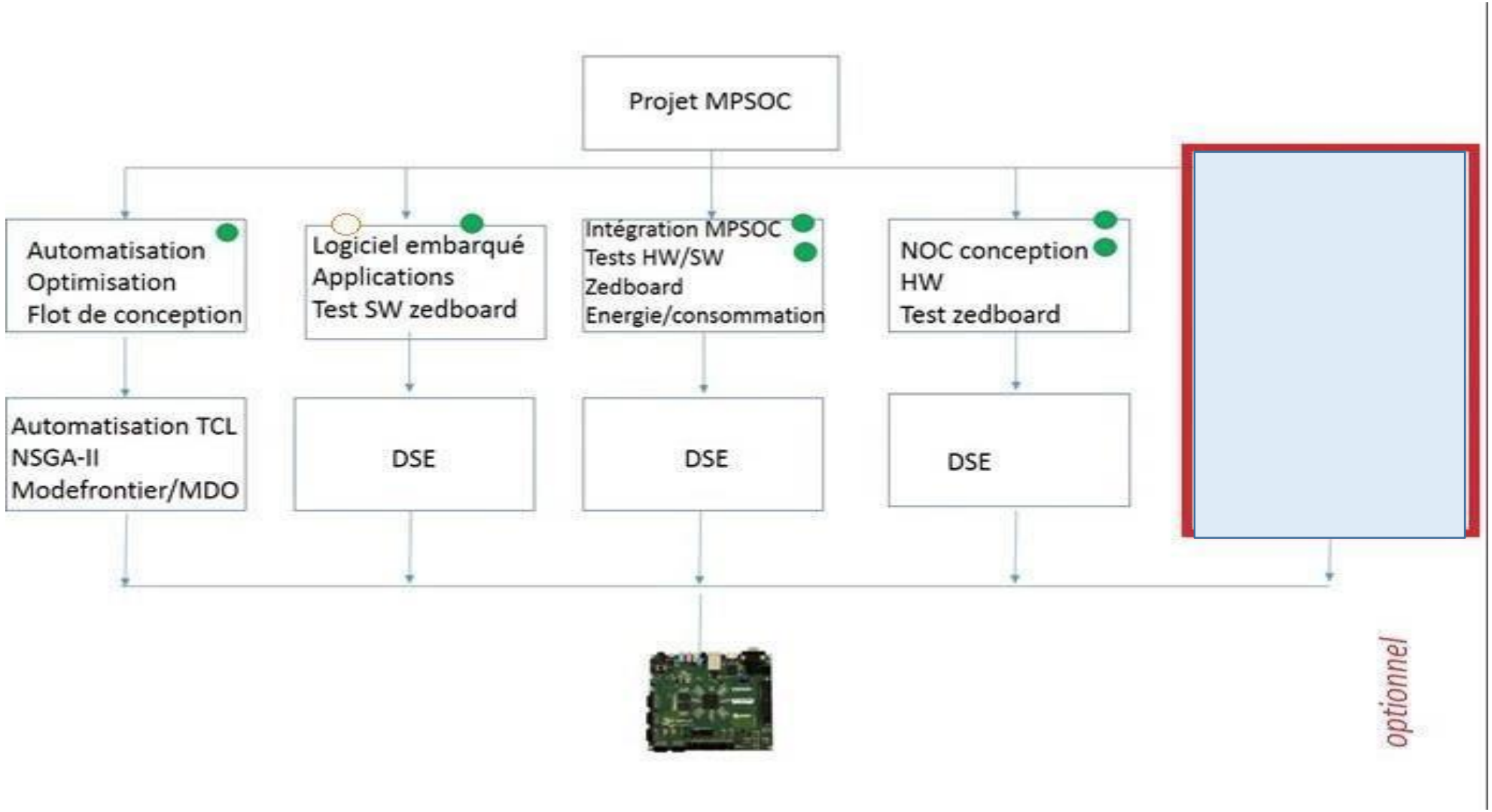
MPSOC for AI and Robotics Applications

Objectif: concevoir un système embarqué multicoeur hétérogène pour applications robotiques à base de NOC (Network-on-Chip)

Contraintes: Performance (P) Maximale, Ressources ® FPGA minimales Consommation Energétique (E) minimale

<Max(P), Min (R) , Min(E)>

Groupe – organisation 4/5 élèves



élève

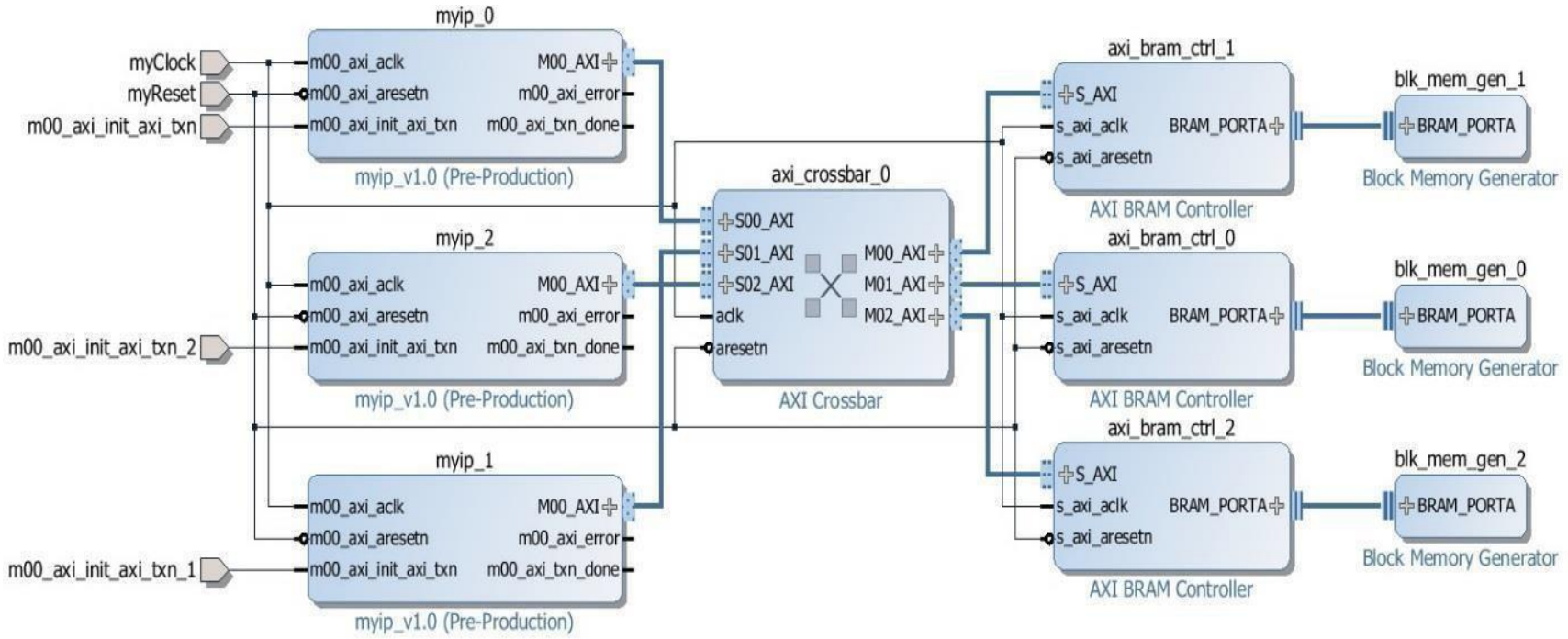
Livrables projet

Group mid-project presentation	Nov 19th 2024	Présentation powerpoint 20 mns + 10 mns questions
Group Presentation	Dec 12th 2024	Group presentation powerpoint 20 mns + 10 mns question
Group project validation	Dec 10h 2024	Board execution
Group Report	Jan 6th 2025	2 pts penalty/day - +5pts/week in advance
Group project	Dec 10th 2024	2 pts penalty/day

Full projects files (C/C++ codes, Vivado Projects, TCL, etc…) should be submitted for board validation on **Dec 9th 2024** through collaborative website (google drive, etc…).

The project evaluation represent 100% of your ROB307 course final grade.
The project will be based on a group grade of 40 % and an individual grade of 60 %.

Q1. Network on chip (NOC) 3x3

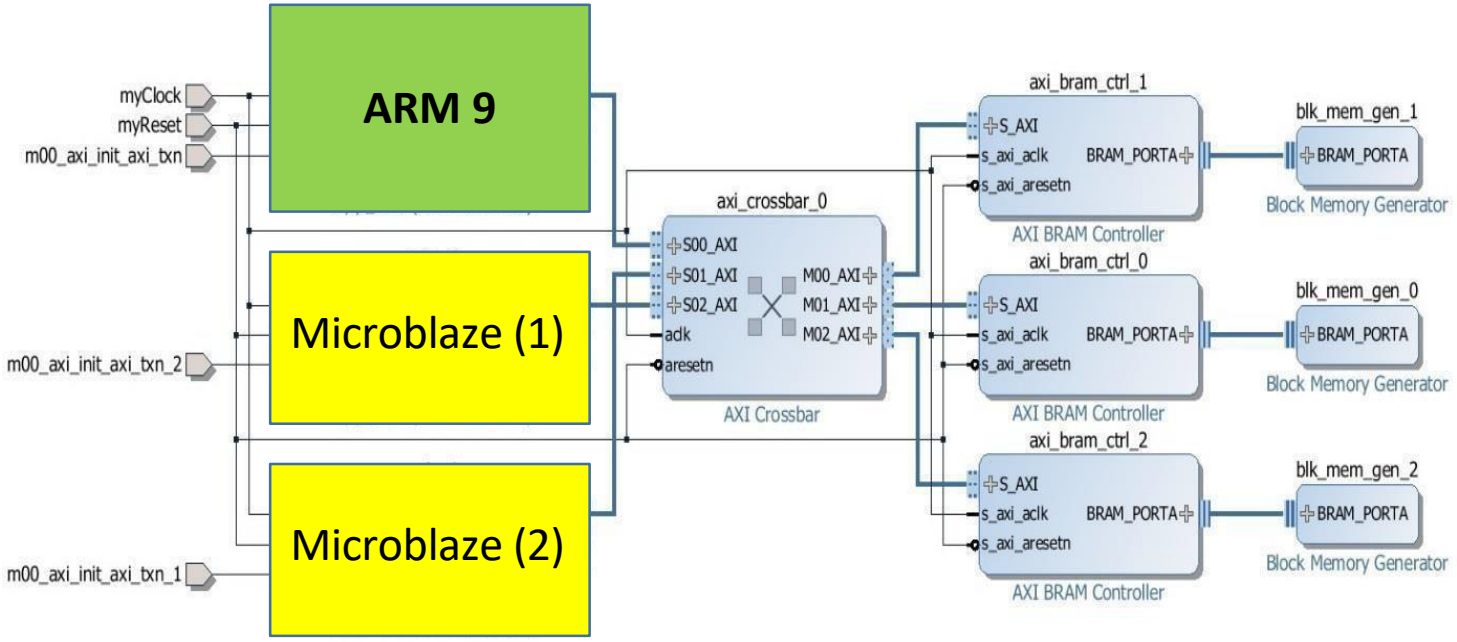


Exemple:
https://drive.google.com/drive/folders/1MIse0ENNUip1Cd_axxJYRaN9nohlsSbK?usp=sharing

Q1. Network on chip (NOC) 3x3

- Q1.1 Téléchargez l'exemple de NOC 3x3. Testez et validez le NOC en utilisant des générateurs de traffic et la simulation
- Q1.2 Analysez la latence et la bande passante de votre NOC par simulation
- Q1.3 Implémentez le NOC sur Zynq et donnez les informations d' implémentations. Explorez les options du NOC et leurs implémentations.
- Q1.4 donnez les informations de placement et routage. Proposez des améliorations.
- Q1.5 Testez and validatez le NOC sur la zedboard.
- Consultez la documentation
    - AXI Traffic Generator v3.0 LogiCORE IP Product Guide Vivado Design Suite PG125 February 11, 2019
    - AXI Interconnect v2.1 LogiCORE IP Product Guide Vivado Design Suite PG059 Dec. 20, 2017

Q2. Multicoeur 3 cœurs : 1 ARM 2 Microblaze v.1



https://www.xilinx.com/support/documentation/sw_manuals/xilinx2019_1/ug984-vivado-microblaze-ref.pdf

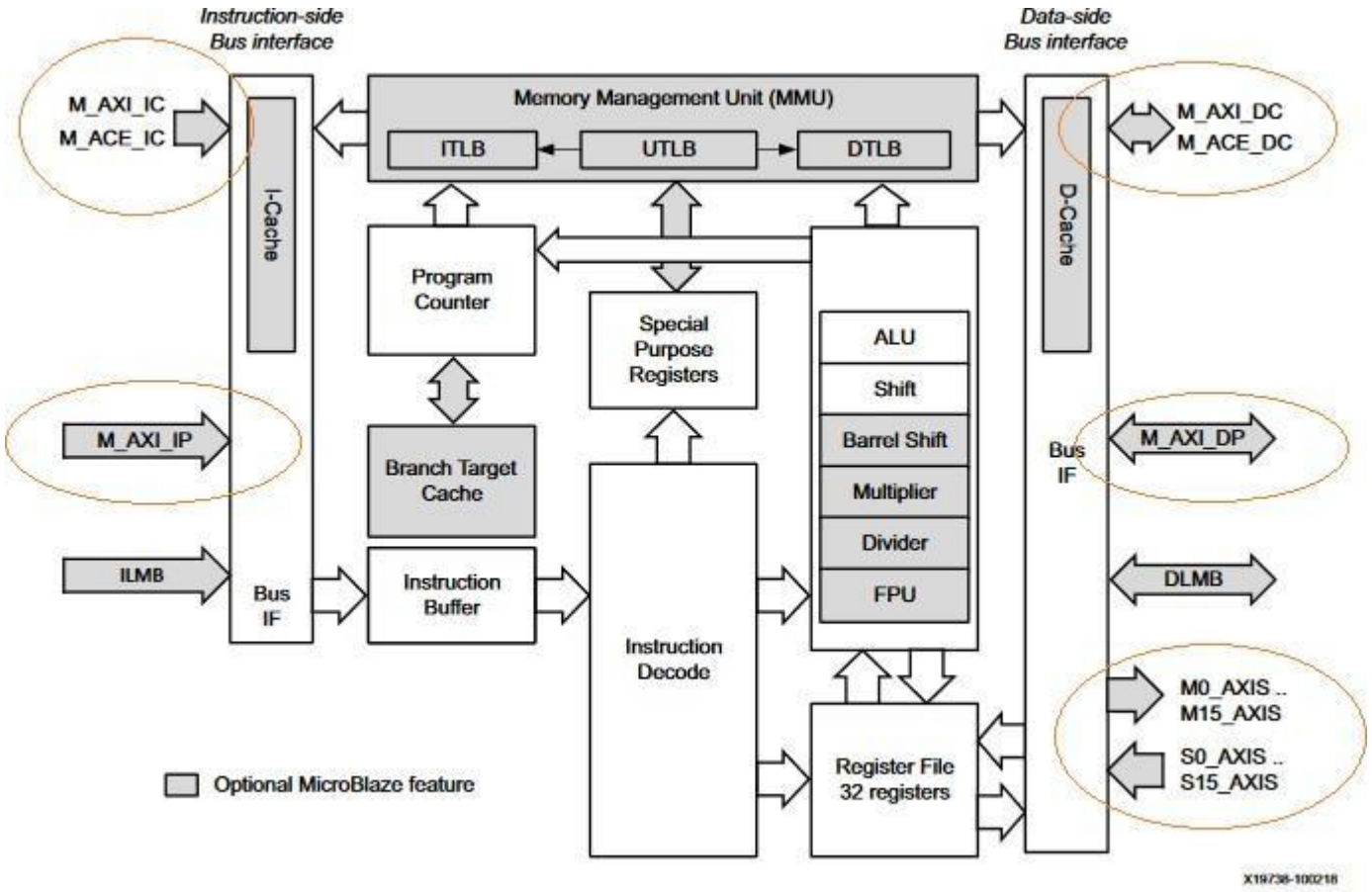
Q2. Multicoeur 3 cœurs : 1 ARM 2 Microblaze

- Q2.1 connectez le processeur ARM au NOC 3x3
- Q2.2 connectez deux processeurs Microblaze sans aucune option *(MMU, Barrel shifter, multiplier, divider, FPU, BTC, Icache, Dcache)* à l'exception de l'interface AXI au NOC 3x3

- Exemple: Vous trouverez ici :
- https://drive.google.com/drive/folders/1oRC-9zudnHiB4oMfo1yCGa0NvrwzLI7Z?usp=sharing

un exemple d'implémentation Vivado/SDK d'un microblaze et d'un ARM.

Q2. Multicoeur 3 cœurs : 1 ARM 2 Microblaze



MicroBlaze Core Block Diagram

Microblaze interface signals

- **M_AXI_DP:** Peripheral Data Interface, AXI4-Lite or AXI4 interface
- **M_AXI_IP:** Peripheral Instruction interface, AXI4-Lite interface

- **M0_AXIS..M15_AXIS:** AXI4-Stream interface master direct connection interfaces
- **S0_AXIS..S15_AXIS:** AXI4-Stream interface slave direct connection interfaces
- **M_AXI_DC:** Data-side cache AXI4 interface
- **M_ACE_DC:** Data-side cache AXI Coherency Extension (ACE) interface
- **M_AXI_IC:** Instruction-side cache AXI4 interface
- **M_ACE_IC:** Instruction-side cache AXI Coherency Extension (ACE) interface
- **Core: Miscellaneous signals for: clock, reset, interrupt, debug, trace**
- **ILMB:** Instruction interface, Local Memory Bus (BRAM only)
- **DLMB:** Data interface, Local Memory Bus (BRAM only)

Q2. Multicoeur 3 cœurs : 1 ARM 2 Microblaze

- Q2.3 effectuer une synthèse placement routage. Donnez les informations de placement et routage. Quelle est la fréquence d'horloge du multicoeur ?
- Q2.4 Proposez des améliorations de fréquence d'horloge avec un système multi-horloge pour les IPs de votre multicoeur

Configurations Microblaze (1/3)

Table 2-1: **Configurable Feature Overview by MicroBlaze Version**

Feature	MicroBlaze versions					
	v9.3	v9.4	v9.5	v9.6	v10.0	v11.0
Version Status	deprecated	deprecated	deprecated	deprecated	deprecated	preferred
Processor pipeline depth	3/5	3/5	3/5	3/5	3/5/8	3/5/8
Local Memory Bus (LMB) data side interface	option	option	option	option	option	option
Local Memory Bus (LMB) instruction side interface	option	option	option	option	option	option
Hardware barrel shifter	option	option	option	option	option	option
Hardware divider	option	option	option	option	option	option
Hardware debug logic	option	option	option	option	option	option
Stream link interfaces	0-16 AXI	0-16 AXI	0-16 AXI	0-16 AXI	0-16 AXI	0-16 AXI
Machine status set and clear instructions	option	option	option	option	option	option
Cache line word length	4, 8	4, 8	4, 8, 16	4, 8, 16	4, 8, 16	4, 8, 16
Hardware exception support	option	option	option	option	option	option
Pattern compare instructions	option	option	option	option	option	option
Floating-point unit (FPU)	option	option	option	option	option	option

Configurations Microblaze (2/3)

Table 2-1: **Configurable Feature Overview by MicroBlaze Version *(Cont'd)***

Feature	MicroBlaze versions					
	v9.3	v9.4	v9.5	v9.6	v10.0	v11.0
Disable hardware multiplier[1]	option	option	option	option	option	option
Hardware debug readable ESR and EAR	Yes	Yes	Yes	Yes	Yes	Yes
Processor Version Register (PVR)	option	option	option	option	option	option
Area or speed optimized	option	option	option	option	option	option
Hardware multiplier 64-bit result	option	option	option	option	option	option
LUT cache memory	option	option	option	option	option	option
Floating-point conversion and square root instructions	option	option	option	option	option	option
Memory Management Unit (MMU)	option	option	option	option	option	option
Extended stream instructions	option	option	option	option	option	option
Use Cache Interface for All I-Cache Memory Accesses	option	option	option	option	option	option
Use Cache Interface for All D-Cache Memory Accesses	option	option	option	option	option	option
Use Write-back Caching Policy for D-Cache	option	option	option	option	option	option
Branch Target Cache (BTC)	option	option	option	option	option	option

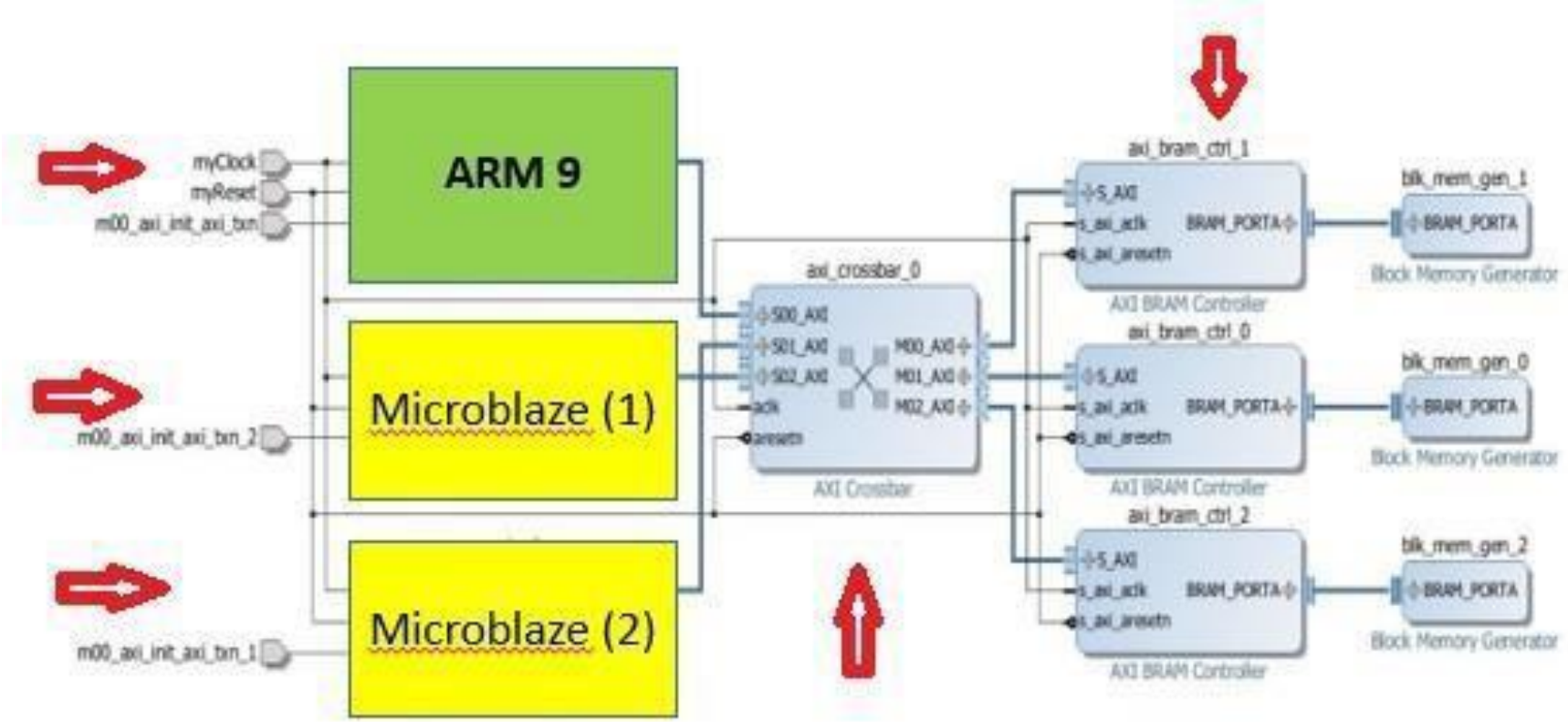
Configurations Microblaze (3/3)

Streams for I-Cache	option	option	option	option	option	option
Victim handling for I-Cache	option	option	option	option	option	option
Victim handling for D-Cache	option	option	option	option	option	option
AXI4 (M_AXI_DP) data side interface	option	option	option	option	option	option
AXI4 (M_AXI_IP) instruction side interface	option	option	option	option	option	option
AXI4 (M_AXI_DC) protocol for D-Cache	option	option	option	option	option	option
AXI4 (M_AXI_IC) protocol for I-Cache	option	option	option	option	option	option
AXI4 protocol for stream accesses	option	option	option	option	option	option
Fault tolerant features	option	option	option	option	option	option
Force distributed RAM for cache tags	option	option	option	option	option	option
Configurable cache data widths	option	option	option	option	option	option
Count Leading Zeros instruction	option	option	option	option	option	option
Memory Barrier instruction	Yes	Yes	Yes	Yes	Yes	Yes
Stack overflow and underflow detection	option	option	option	option	option	option
Allow stream instructions in user mode	option	option	option	option	option	option

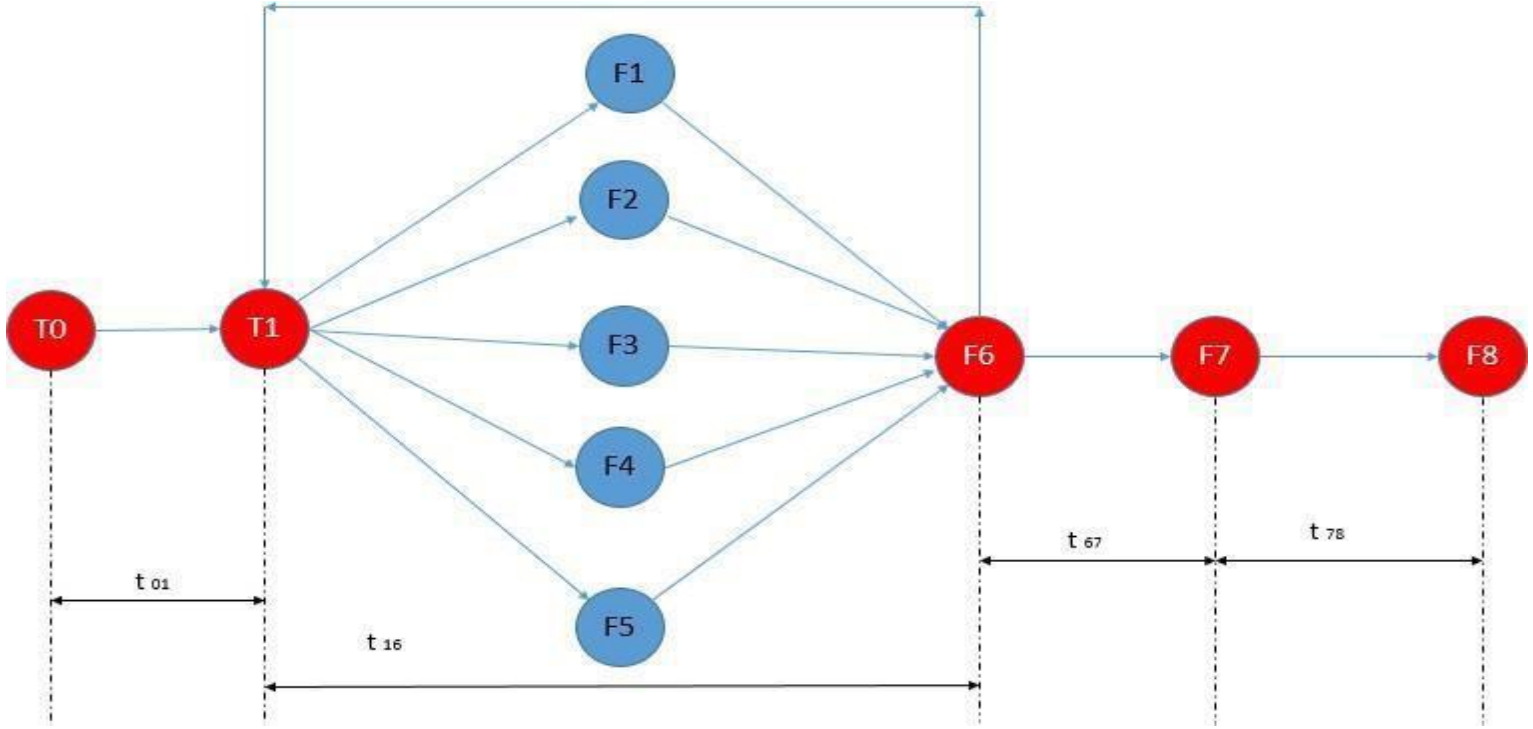
Q2. Multicoeur 3 cœurs : 1 ARM 2 Microblaze

- Q2.4 Explorations options Microblaze: modifiez les configurations du processeur Microblaze en faisant varier *(Barrel shifter, multiplier, divider, FPU, BTC, Icache, Dcache)*
- Effectuez une synthèse placement routage du multicoeur avec les différentes configurations des 2 Microblaze. Donnez les informations de placement et routage et fréquences d'horloge.
- Conservez l'ensemble des différents projets Vivado associés à ces différentes versions du multicoeur pour l'évaluation de performances logiciel.

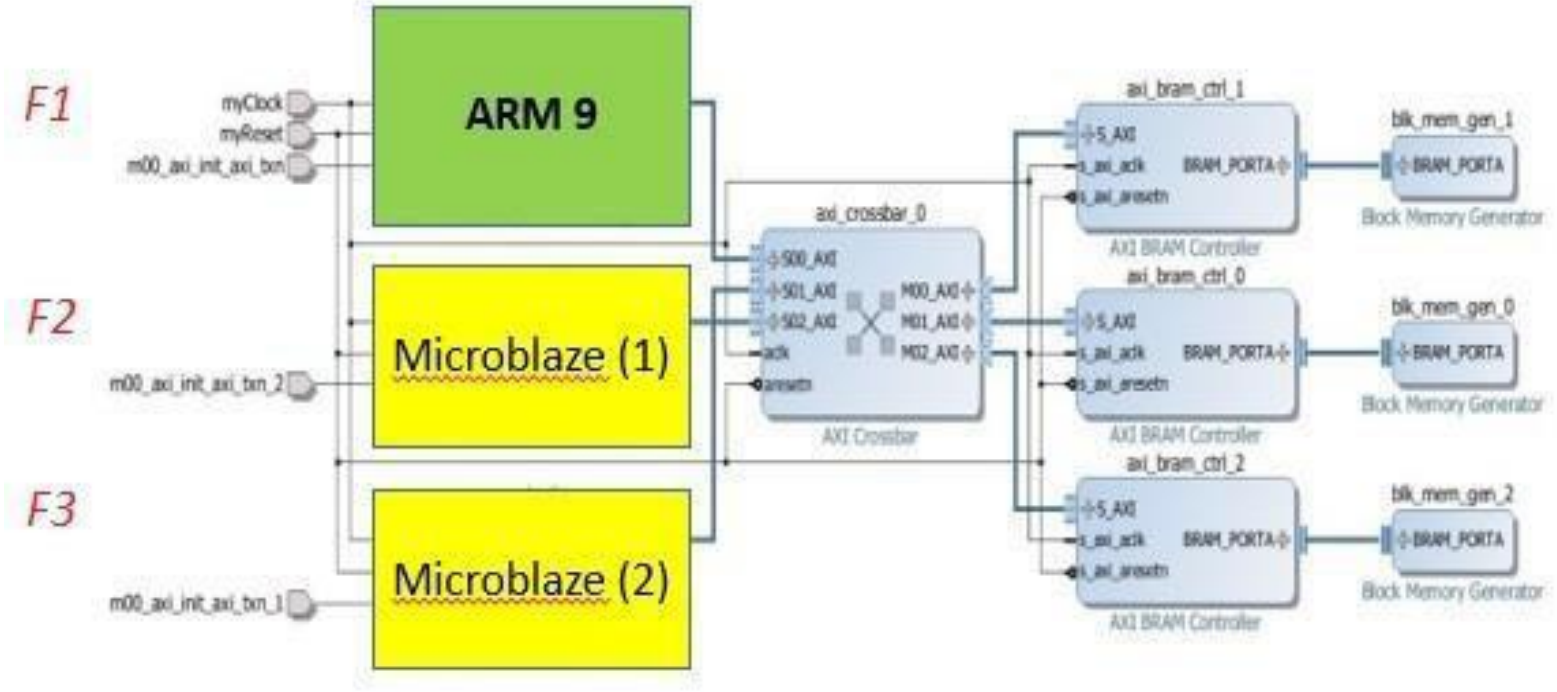
Multicoeur multi-horloges



Q3. programmation



3 programmes F1, F2 et F3 s'exécutant séparément sur chaque processeur



Evaluation de performances

- Evaluez les performances en temps d'exécution
- Étendre le multicoeur à 5 cœurs (1 ARM + 4 MB)
- Rajoutez des accélérateurs matériels HLS

- Comparez

Evaluation énergétique

- Evaluez la consommation énergétique de vos implémentations
- Étendre le multicoeur à 5 cœurs (1 ARM + 4 MB)

Exploration automatisée <P, R, E>

Proposez une méthode d'exploration multiobjective automatisée de l'espace de conception pour le MPSOC prenant en compte les contraintes et générant un front de Pareto 3D sur la base de l'execution

Lire l'article

Machine learning based fast and accurate High Level Synthesis design space exploration: From graph to synthesis

Question optionnelle: LLM + Vivado

Stanford University

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June 26-27 2025, Stanford, CA

https://iclad.ai/

Proposez la génération automatique de MPSOC par LLM

references

- https://www.xilinx.com/support/documentation/ip_documentation/axi_interconnect/v2_1/pg059-axi-interconnect.pdf
- https://www.xilinx.com/support/documentation/boards_and_kits/ug669_ml605_sp605_hw_tutorial_axi.pdf


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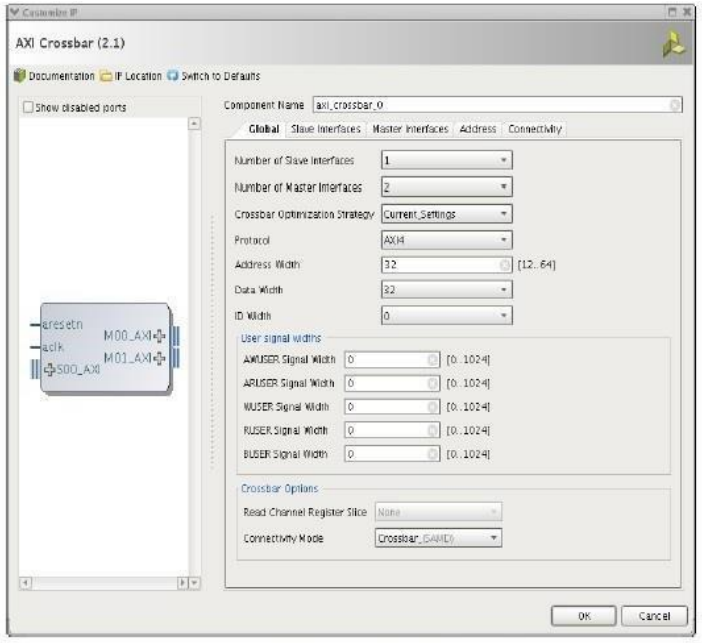
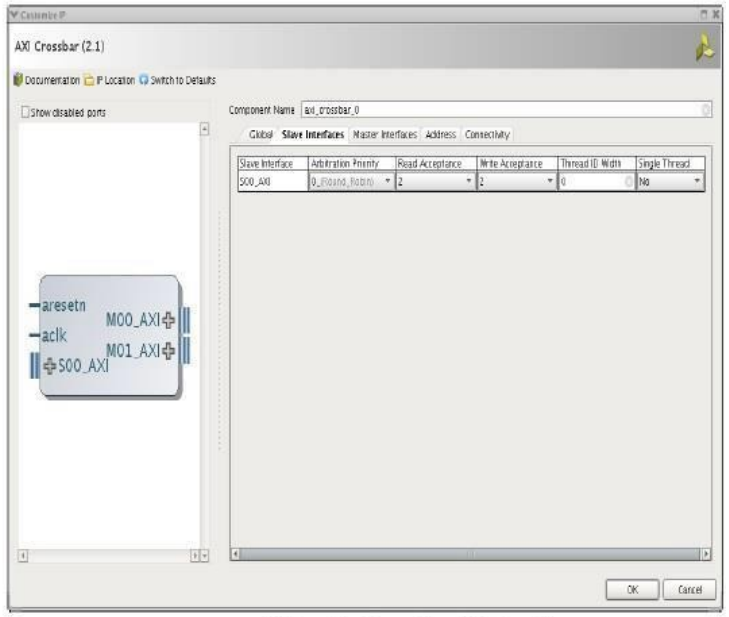
IP PARIS

AXI crossbar - configuration



AXI Crossbar Core – Global Tab

AXI Crossbar Core — Slave Interface Tab



AXI Crossbar Core – Slave Interface Tab

AXI Crossbar Core — Master Interface Tab

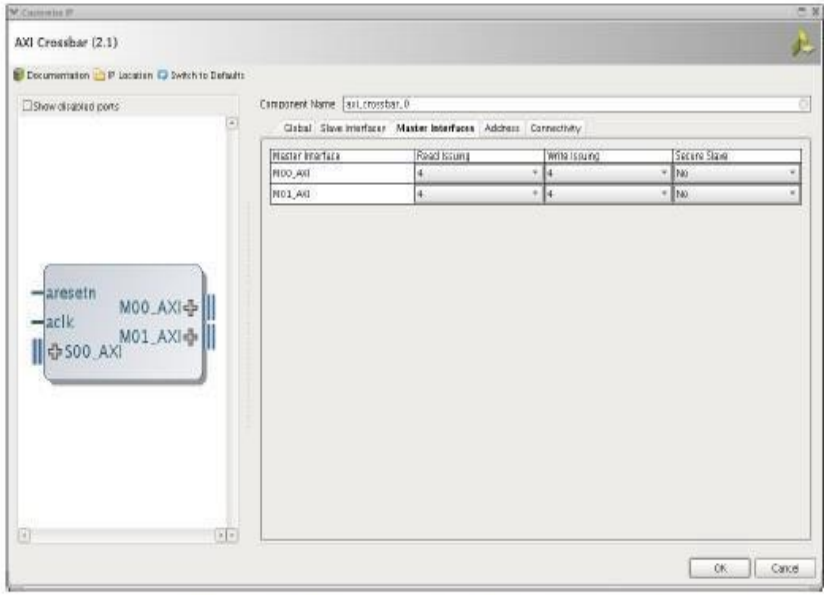
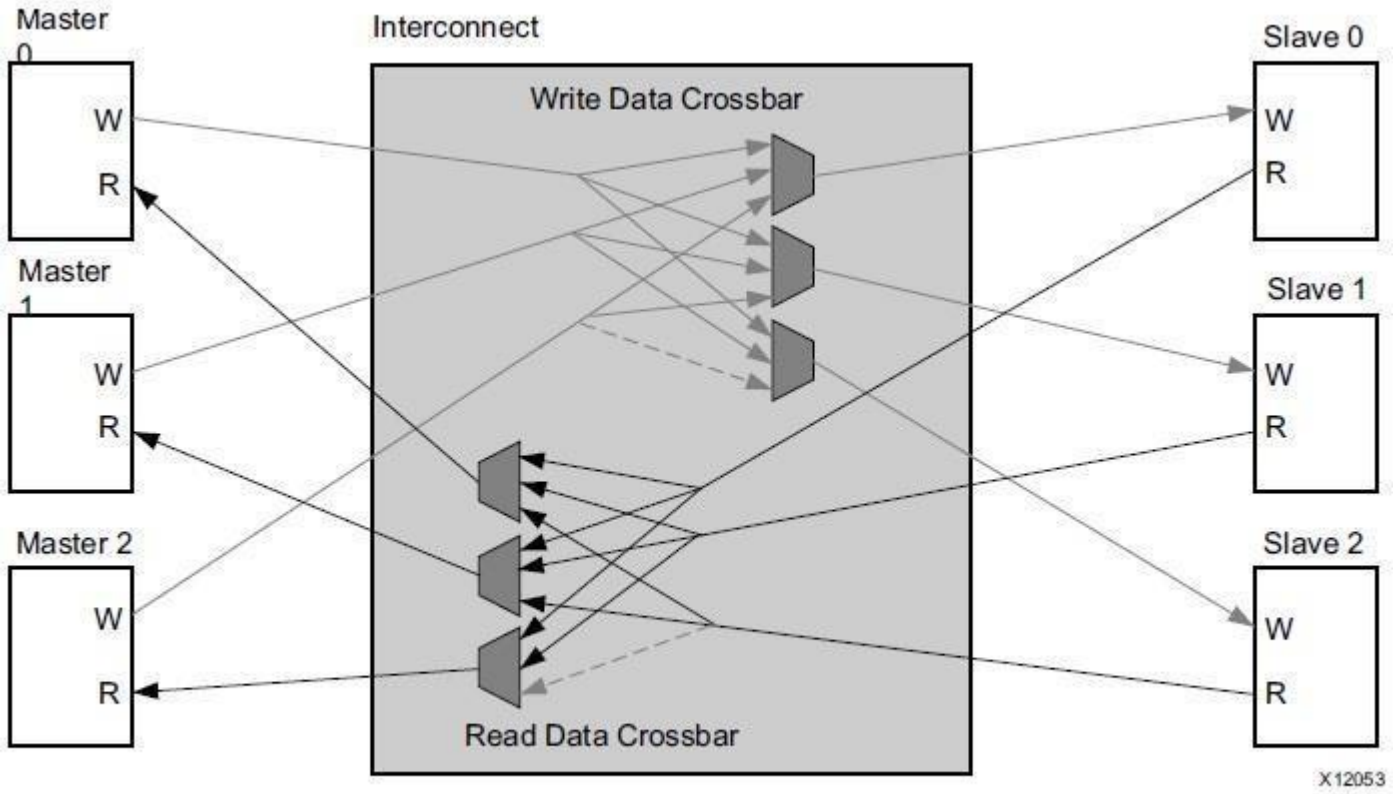


Figure 4-7: AXI Crossbar Core -- Master Interface Tab

AXI Crossbar



Sparse Crossbar Write and Read Data Pathways

Arteris – Network on Chip

Exemple d’entreprises https://www.arteris.com/customers