

ICS Homework 4

崔士强 PB22151743

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T1

1. 0101 011 010 1 00100
2. 0101 011 010 1 01100
3. 0101 011 010 1 11111
4. We can not acquire 0100 0000 by sign-extending a 5-bit number.

T2

T3

1. LDR R2, R1, #0
STR R2, R0, #0
2. MAR <- SR
MDR <- Memory[MAR]
MAR <- DR
Memory[MAR] <- MDR

T4

0101 011 001 000 011
0101 100 010 000 100

T5

Addressing modes: immediate, register, PC-relative, indirect, Base+offset.

Category	Instructions	Addressing modes
Operate	ADD	register, immediate
	NOT	register
	LEA	register, PC-relative
Data movement	LDR	register, Base+offset
Control	JMP	register

T6

1. AND
2. AND R3, R3, #0
3. NOT R1, R7
ADD R1, R1, #1
ADD R1, R1, R6
- 4.
5. ADD R1, R1, #0

T7

JMP: 2 accesses (One for the instruction and another for the address stored in BaseR)

ADD: 3 accesses (One for the instruction and two for the operands)

LDI: 3 accesses (One access to fetch the LDI instruction itself. Another access to fetch the address from memory. A third access to fetch the actual data from the location specified by the address.)

T8

1. x70A4
2. Suppose the instruction is at memory address x3010
1110 1100 0011 1101

T9

In all 16 bits of the value in R5, there are 4 bits which are 1.