2023 ICS 期中考试

B2, B3, B4

汤皓宇

2023 年 12 月 1 日

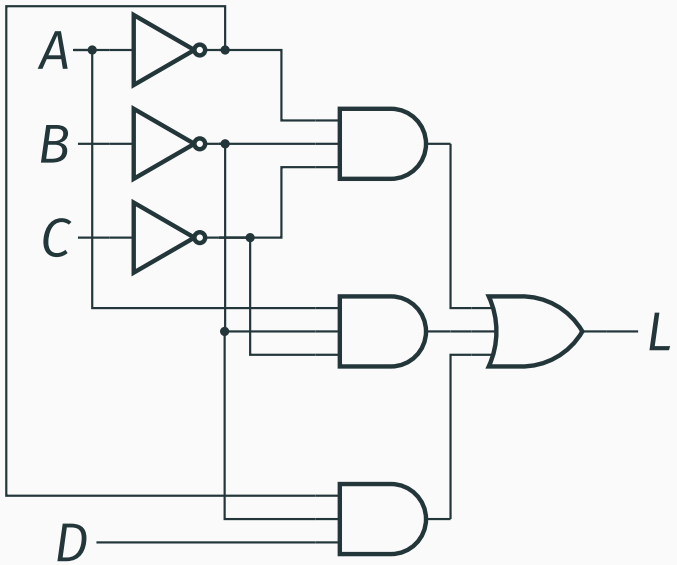
总体情况

- B2, B3, B4 部分主要考察组合与时序电路、状态机的知识。
- 对组合电路中一些运算的规律掌握不是很熟练，比如摩根律、结合律、排中律、双重否定律等。
- 画逻辑电路图时出现遗漏符号的问题。
- 对时序电路的分析不太熟练。
- 状态机的绘制容易出现遗漏、不标状态转移条件等问题。

B2

B2 (1)

Please write the logic expression for the circuit below.



答案

简记 $X\,Y, X+Y, \overline{X}$ 分别表示 X AND Y, X OR Y, NOT X.

$$
\begin{aligned}
L &= \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,D \\
&= \overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,D \\
&= \overline{B}(\overline{C} + \overline{A}\,D)
\end{aligned}
$$

B2 (2) 出题人思路

$$
\begin{aligned}
L &= \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,D \\
&= \overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,D \\
&= \overline{B}(\overline{C} + \overline{A}\,D)
\end{aligned}
$$

Rewrite the expression using only NOT and NAND.

答案

三输入与非门可以使用记号 $NAND(X, Y, Z)$ 或者直接 $\overline{XYZ}$，注意 $NAND$ 没有结合律。

$$
\begin{aligned}
L &= \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,D \\
&= \overline{\overline{\overline{A}\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,D}} \\
&= \overline{\overline{\overline{A}\,\overline{B}\,\overline{C}}\;\overline{\overline{A}\,\overline{B}\,\overline{C}}\;\overline{\overline{A}\,\overline{B}\,D}}
\end{aligned}
$$

B2 (2) 非预期解

$$
\begin{aligned}
L &= \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,D \\
&= \overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,D \\
&= \overline{B}(\overline{C} + \overline{A}\,D)
\end{aligned}
$$

Rewrite the expression using only NOT and NAND.

答案 1

$$
\begin{aligned}
L &= \overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,D \\
&= \overline{\overline{\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,D}} \\
&= \overline{\overline{\overline{B}\,\overline{C}}\;\overline{\overline{A}\,\overline{B}\,D}}
\end{aligned}
$$

答案 2

$$
\begin{aligned}
L &= \overline{B}(\overline{C} + \overline{A}\,D) \\
&= \overline{\overline{\overline{B}\,\overline{\overline{C} + \overline{A}\,D}}} \\
&= \overline{\overline{B}\,\overline{\overline{C}\,\overline{\overline{A}\,D}}}
\end{aligned}
$$

B2 (2) 只使用二输入门

答案

$$
\begin{aligned}
L &= \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,D \\
&= \overline{\overline{A}\,\overline{B}\,\overline{C}} + A\,\overline{\overline{B}\,\overline{C}} + \overline{\overline{A}\,\overline{B}}\,D \\
&= \overline{\overline{\overline{A}\,\overline{B}\,\overline{C}}\;\overline{A\,\overline{\overline{B}\,\overline{C}}}} + \overline{\overline{A}\,\overline{B}}\,D \\
&= \overline{\overline{\overline{A}\,\overline{B}\,\overline{C}}\;\overline{A\,\overline{\overline{B}\,\overline{C}}}\;\overline{\overline{A}\,\overline{B}}} + D \\
&= \overline{\overline{\overline{A}\,\overline{B}\,\overline{C}}\;\overline{A\,\overline{\overline{B}\,\overline{C}}}\;\overline{\overline{A}\,\overline{B}}}\;D \\
&= NAND(NOT(\\
&\quad NAND(NAND(NOT(NAND(NOT(A), NOT(B))), NOT(C)), \\
&\quad\quad NAND(A, NOT(NAND(NOT(B), NOT(C))))) \\
&), NAND(NOT(NAND(NOT(A), NOT(B))), D))
\end{aligned}
$$

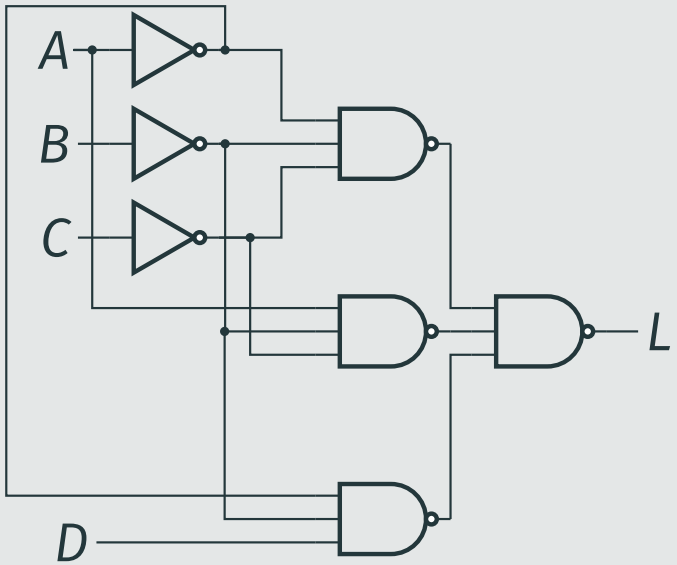
B2 (3)

$$L = \overline{\overline{\overline{A}\,\overline{B}\,\overline{C}}\;\overline{A\,\overline{B}\,\overline{C}}\;\overline{\overline{A}\,\overline{B}\,D}}$$

Draw the logic diagram implemented using only NOT gates and NAND gates.

答案

其他的表达式对应的逻辑电路图也对，这里只给出一种。



B3

B3 公式推导

Use only **NOT** gates and **2-input NOR** gates to draw a logic circuit diagram for expression $L = A\,\overline{B} + \overline{A}\,C$.

答案

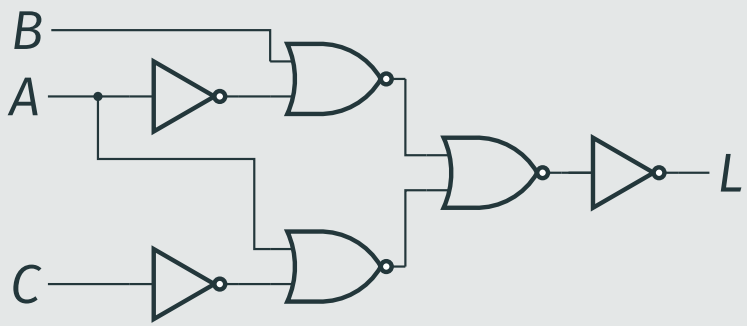
$$
\begin{aligned}
L &= A\,\overline{B} + \overline{A}\,C \\
&= \overline{\overline{A\,\overline{B}}\;\;\overline{\overline{A}\,C}} \\
&= \overline{\overline{A} + B + A + \overline{C}}
\end{aligned}
$$

B3 画图

$$L = \overline{\overline{\overline{A} + B} + \overline{A + \overline{C}}}$$

Use only **NOT** gates and **2-input NOR** gates to draw a logic circuit diagram for expression $L = A\,\overline{B} + \overline{A}\,C$.

答案



B4

B4(1)

Please explain why state machines must be implemented using sequential circuits and cannot be realized with only combinational circuits.

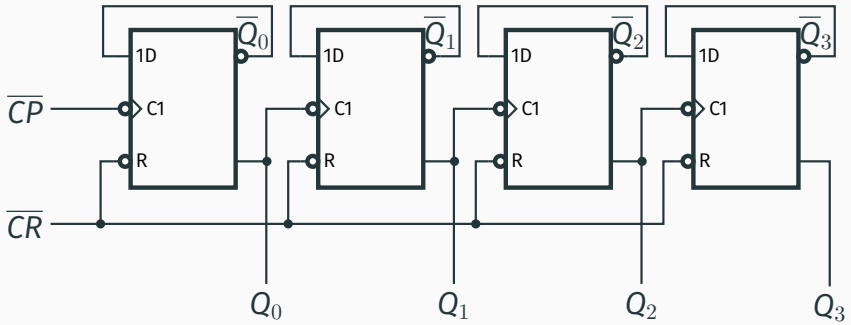
答案

状态机的输出不止和当前的输入有关，也与之前的输入有关，因此需要使用时序电路来存储之前的状态；而组合电路不能保存之前的状态，输出只和输入有关。

B4(2)

D-trigger, is a type of digital storage element in digital circuits. It has three inputs: a data input (D), clear input (R) and a clock input (CLK). When the clear signal (R) is asserted, it forces the output (Q) to be *'0'*. The clock input determines when the data input should be sampled. When clock signal rising edge occurs, it will make Q = D.

Your job: Describe what the following sequential circuit does in **one sentence**. Assume that the output $Q_0Q_1Q_2Q_3$ is initially *0000*.



答案

在时钟 CP 下降沿到来时，输出 $Q_3Q_2Q_1Q_0$ 会增加 1，且可以循环。

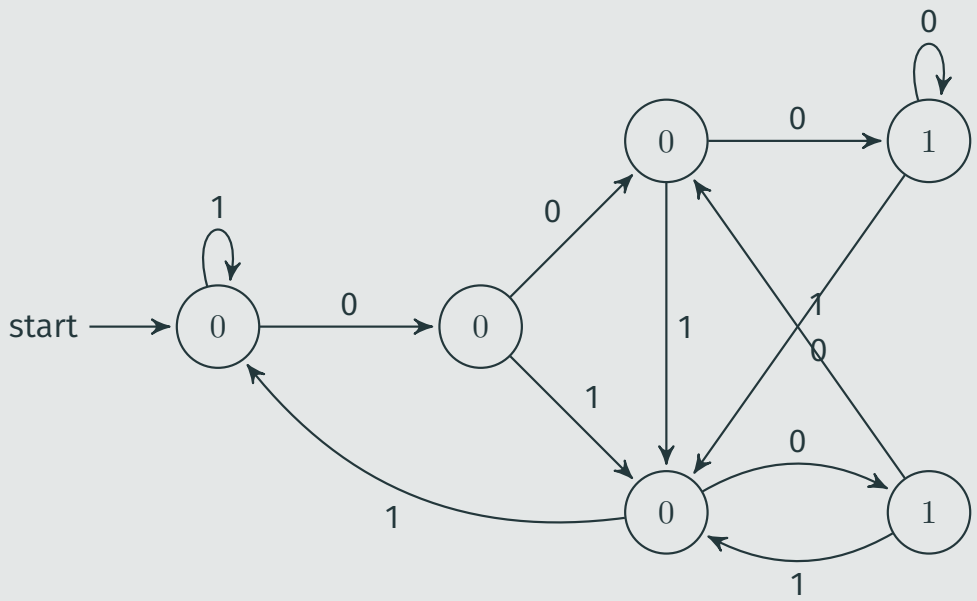
B4(3)

Design a Finite State Machine (FSM) that recognizes patterns of *"000"* and *"010"* in an input string and outputs *1* when either pattern is detected.

For example, given a string *00001000*, it will produce *00110101*.

答案

每个状态都需要考虑所有的可能输入，即每个状态会有两条出边。

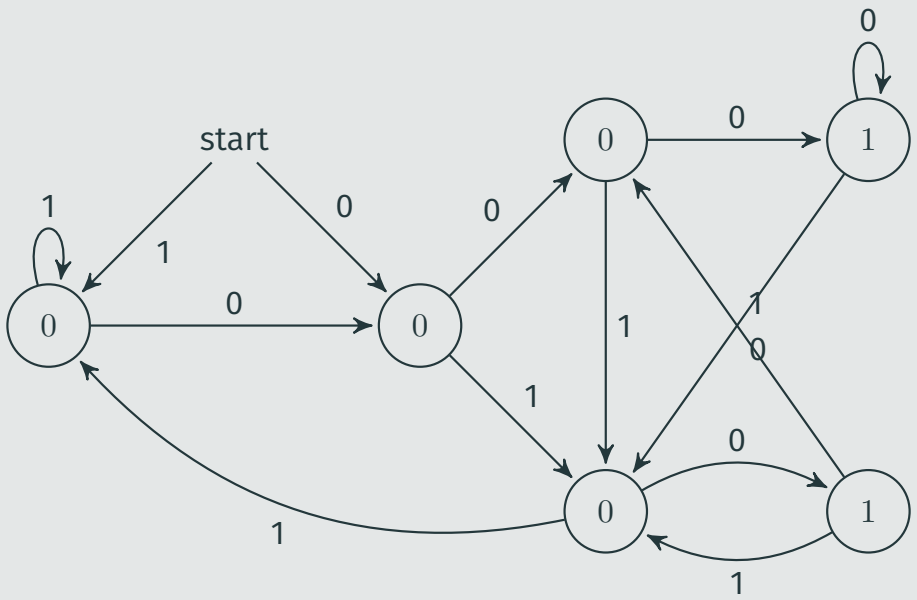


B4(3) 另一种

Design a Finite State Machine (FSM) that recognizes patterns of *"000"* and *"010"* in an input string and outputs *1* when either pattern is detected.

For example, given a string *00001000*, it will produce *00110101*.

答案



Questions?

谢谢大家