



MICRO PROCESSORS AND INTERFACING (EEE F241)

**BIRLA INSTITUTE OF TECHNOLOGY AND
SCIENCE, PILANI
K.K. BIRLA GOA CAMPUS**

DESIGN ASSIGNMENT ON BUILDING AN IC TESTER

SUBMITTED TO DR. K.R. ANUPAMA

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BATCH NO::81

OBJECTIVE:

Design a Microprocessor based Tester to test the logical functioning of the following chips: (i) 7400 (ii) 7402 (iii) 7410 The IC to be tested will be inserted in a 14 pin ZIF socket. The IC number is to be entered via a keyboard. The keyboard has keys 0-9, backspace, enter and test. The user places the IC in the ZIF socket closes it - then enters the IC No, followed by enter key. The IC No. is displayed on the 7-segment display. The testing will start once the user presses test key. After Test the result PASS/FAIL must be displayed on the 7-segment display. Design the necessary hardware and write the necessary ALP for implementing.

DESIGN SPECIFICATIONS

P3-IC TESTER :Design a Microprocessor based Tester to test the logical functioning of the following chips: (i) 7400 (ii) 7402 (iii) 7410

- The IC to be tested will be inserted in a 14 pin ZIF socket.
- The IC number is to be entered via a keyboard. The keyboard has keys 0-9, backspace, enter and test. The user places the IC in the ZIF socket closes it - then enters the IC No, followed by enter key.
- The IC No. is displayed on the 7-segment display. The testing will start once the user presses test key.
- After Test the result PASS/FAIL must be displayed on the 7-segment display.
- Design the necessary hardware and write the necessary ALP to implement this task.

- 8253 Timer is used to create the delay of 20 ms
- PNP BJTs are being used to enable the display one by one to show the result of test and IC number
- The system generates to selector o/p at PC4 and PC5 of 8255(2) depending upon IC number entered

7402-00

7410-01

7400-10

- Demuxes are connected to the possible input pins of ICs through ZIF. Demux uses selector inputs to decide which signal should go to which pin of ZIF based on IC number entered

- Mux is connected to the possible output pins of given ICs through ZIF. Output of the MUX goes to PB0 to PB3.
- These O/P generated at O/P pins of ZIF(decided by IC number entered) are taken as I/P through MUX and are compared against the stored truth table for corresponding set of I/Ps.
- The use of MUX and DEMUX is based on the idea that each gate of the IC can be checked simultaneously by giving same set of signals as input.
- For 7400 and 7402 I/P set is (I1,I2){which can be given to all four gates simultaneously} and output set is (O1,O2,O3,O4). For 7410, it's (I1,I2,I3) and (O1,O2,O3).
- Testing the ICs other than 7400, 7402, 7410 and damaged ICs gives O/P as FAIL on the 7 segment Display.
- If the IC is working, the Display shows PASS

ASSUMPTIONS IN DESIGN

1. The first key pressed is always a digit (backspace is never pressed in the beginning).
2. Only test key is pressed after the enter key

COMPONENTS USED:

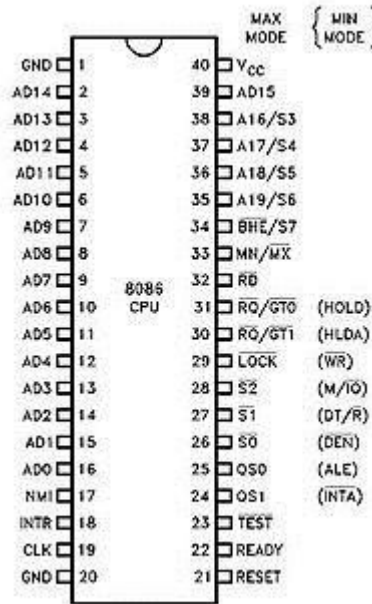
1. 8086 Microprocessor
2. 2N2905-Low power BJT
3. 8255A (Programmable Peripheral Interface with 24 I/O lines) -2 NOS
4. 74LS138 (3:8 Decoder) - 3 NOS
5. 74LS245 (Octal Bus transceivers with tristate output) -2 NOS
6. 74LS373 (Octal D-Type transparent latches with 3 state outputs) -3 NOS
7. 2732 (16K (4Kx4) EPROM) -4 NOS
8. 6116 (4K (2Kx2) Static RAM) -2 NOS

9. 7400 (Quadruple 2-input positive NAND gates)
10. 7402 (Quadruple 2-input positive NOR gates)
11. 7410 (Triple 3-input positive NAND gates)
12. 7-Segment Anode Display
13. SW-SPDT (Interactive SPDT switch (Momentary Action))
14. Resistances-10K, 150 ohms, 1.5K-Quantity 4 each
15. 74153-Dual 1 of 4 line Multiplexer
16. 74LS139-Dual 1 of 4 Demultiplexer
17. 8253 - Programmable Interval Timer

PIN OUTS OF COMPONENTS USED

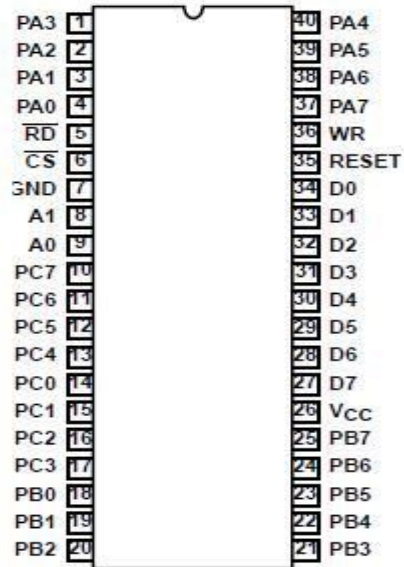
8086

Microprocessor Quantity-1



8255A

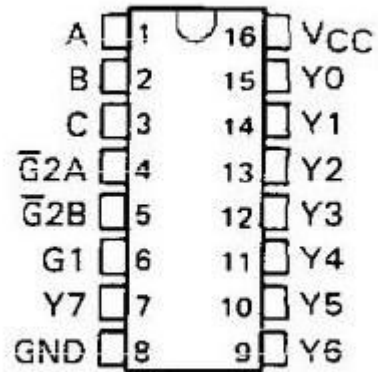
Microprocessor Programmable Peripheral Interface Quantity-2



Decoder Buffer

74LS138 74LS245

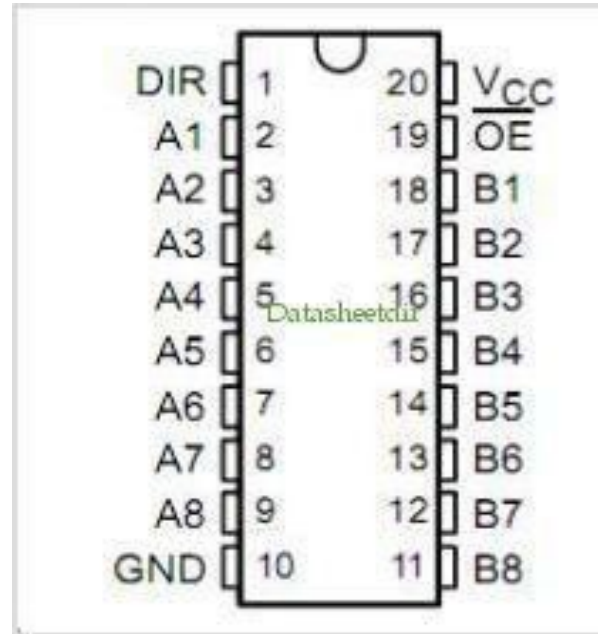
Quantity-3



Decoder Buffer

74LS245

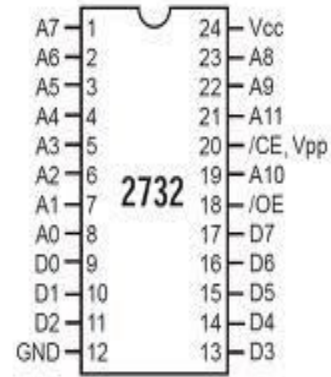
Quantity-1 Quantity-2



ROM

2732

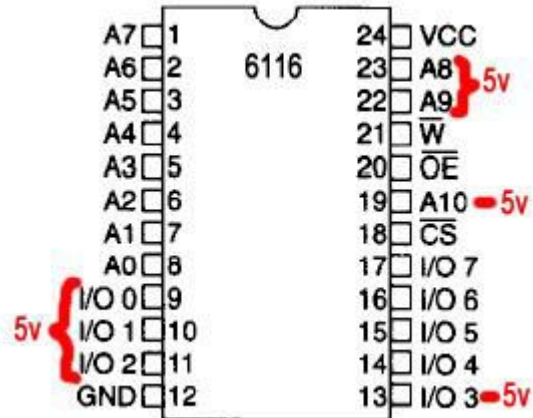
Quantity-4



RAM

6116

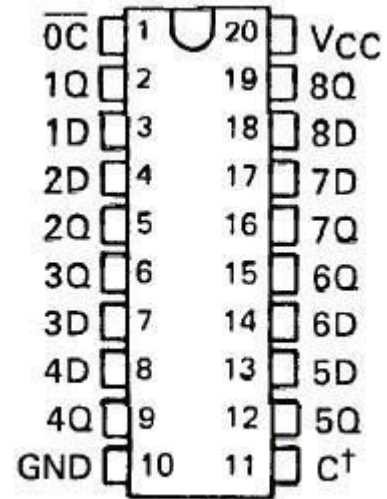
Quantity-2



Latch

74LS373

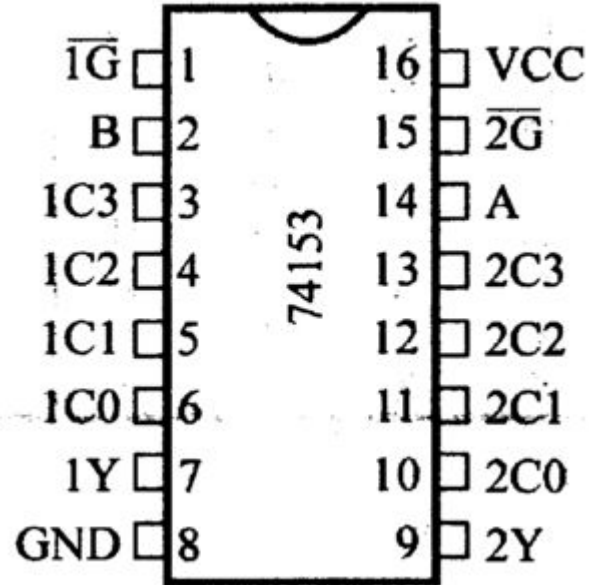
Quantity-3



Dual 4 line to 1 line Multiplexer

74153

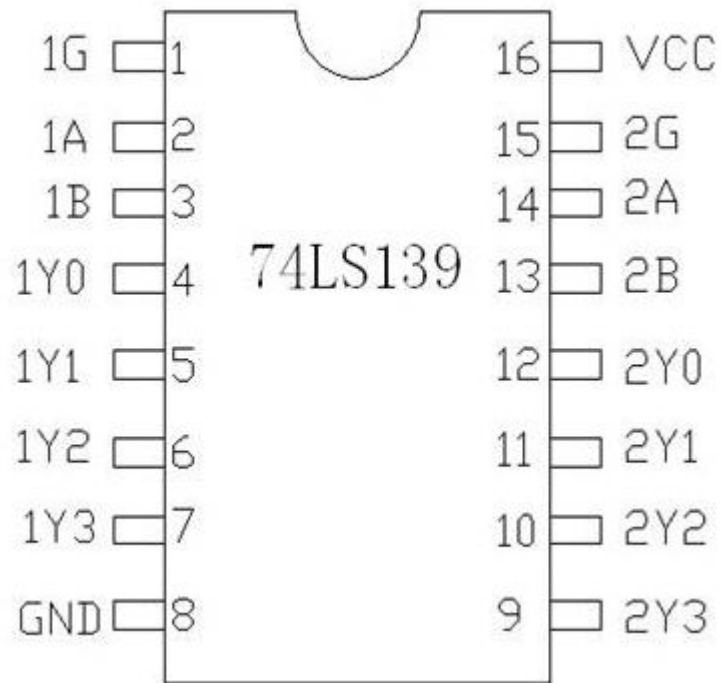
Quantity-2



Dual 1 of 4 Demultiplexer

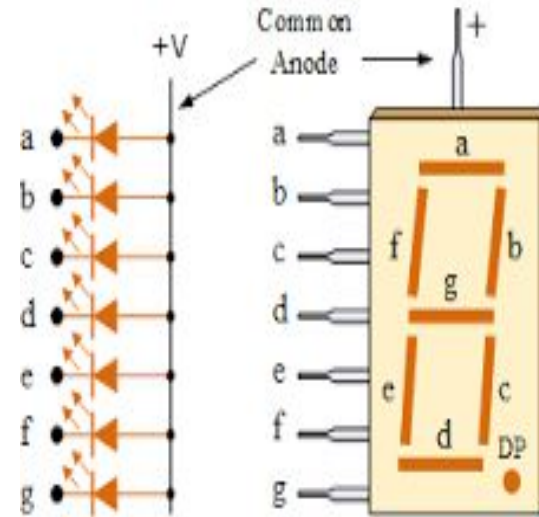
74LS139

Quantity-2



7 Segment Anode Display

Quantity-4



Bipolar Junction Transistor

2N2905

Quantity-4



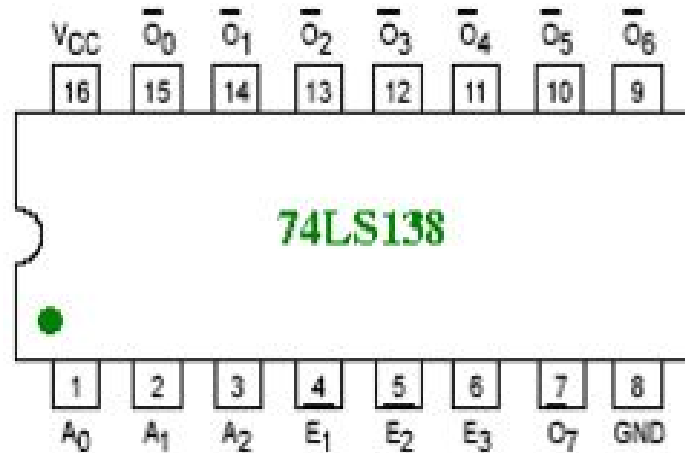
Pin Configuration

1. Emitter
2. Base
3. Collector

3 Line to 8 line Decoder

74LS138

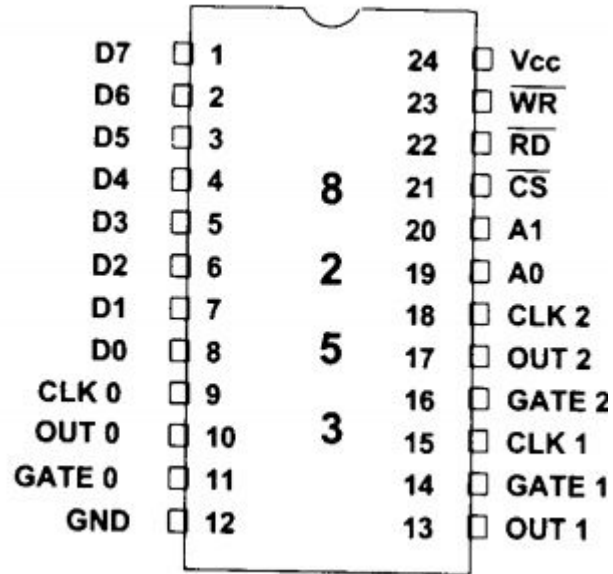
Quantity-1



Timer

8253

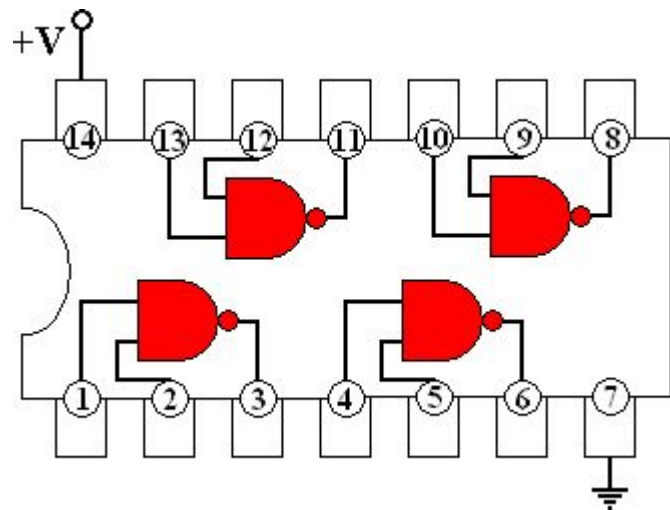
Quantity-1



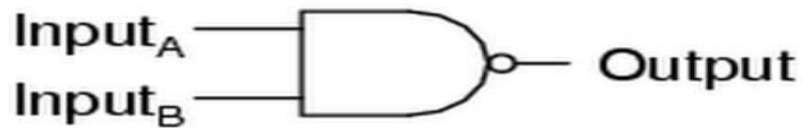
IC's TO BE TESTED

IC-7400

2 Input NAND Gate IC



NAND gate

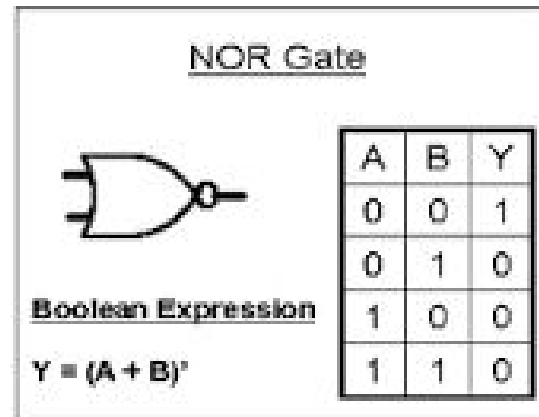
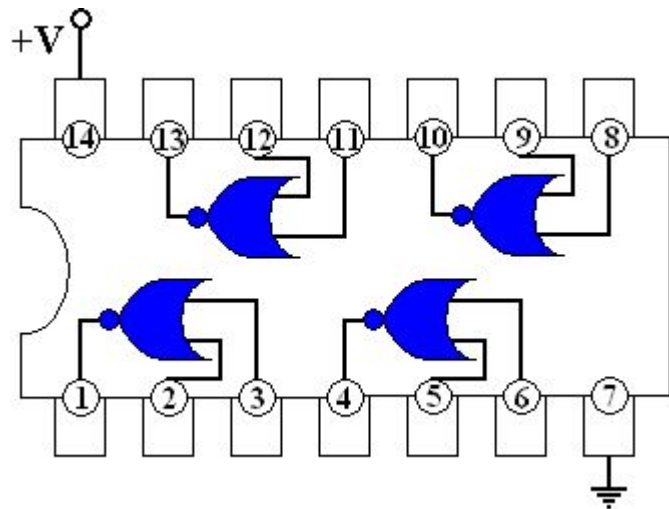


A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

IC's TO BE TESTED

IC-7402

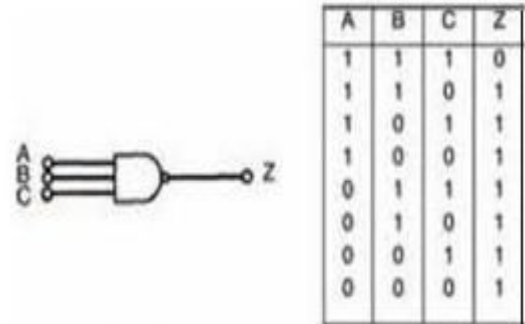
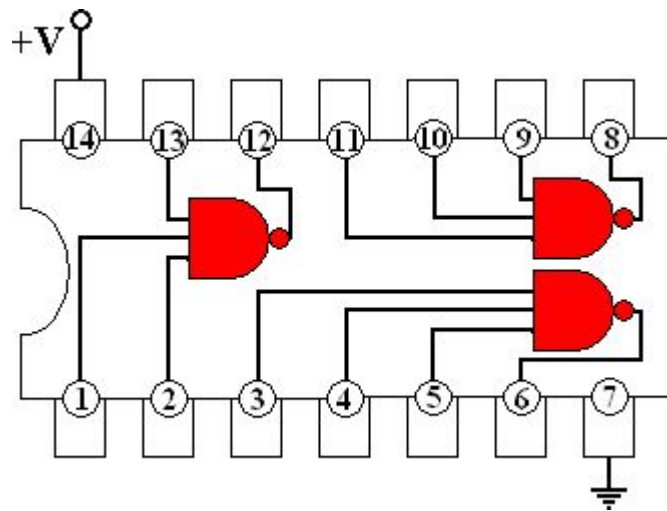
2 Input NOR Gate IC



IC's TO BE TESTED

IC-7410

3 Input NAND Gate IC



MEMORY INTERFACING

Memory Requirements:

In proteus 7 minimum ROM chip available is 4K and minimum RAM chip available is 2k. We need to interface :

8K ROM starting at 00000H

4K RAM starting at 02000H

8K ROM starting at FE000H

No of Chips:

2732 ROM ($\text{Size of ROM} = 32/8 = 4\text{K}$) x4

6116 RAM ($\text{Size of RAM} = 16/8 = 2\text{K}$) x2

MEMORY ALLOCATION

Memory Allocation:

ROM1E - 00000H, 00002H, 00004H.....01FFEh

ROM1O - 00001H, 00003H, 00005H.....01FFFh

RAM1E - 02000H, 02002H, 02004H.....02FFEh

RAM1O - 02001H, 02003H, 02005H.....02FFFh

ROM2E - FF000H, FF002H, FF004H.....FFFFEh

ROM2O - FF001H, FF003H, FF005H.....FFFFFh

ROM1: 00000H-01FFFH

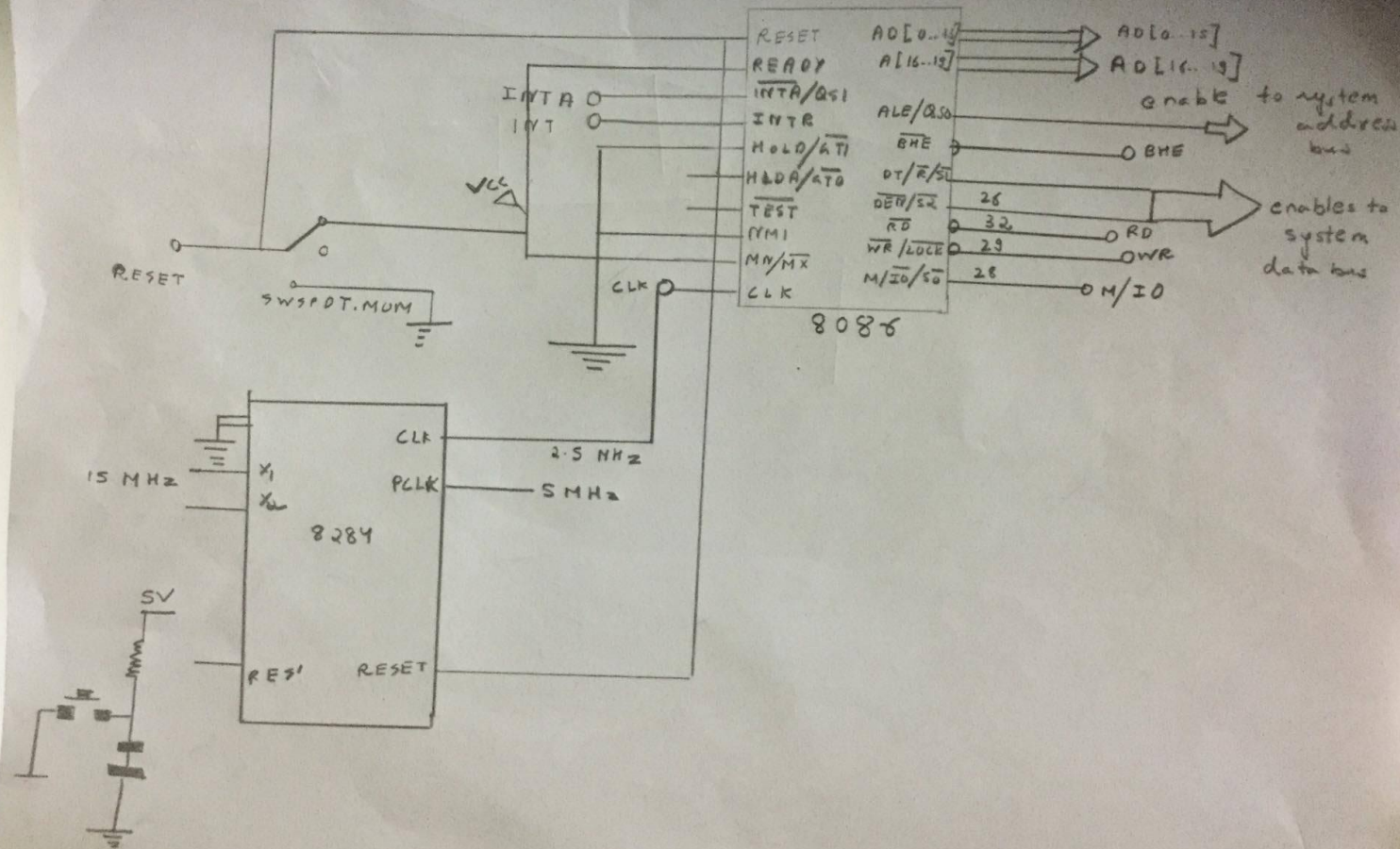
A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	...	A0
0	0	0	0	0	0	0	0	0	0	0	...	0
0	0	0	0	0	0	0	1	1	1	1	...	1

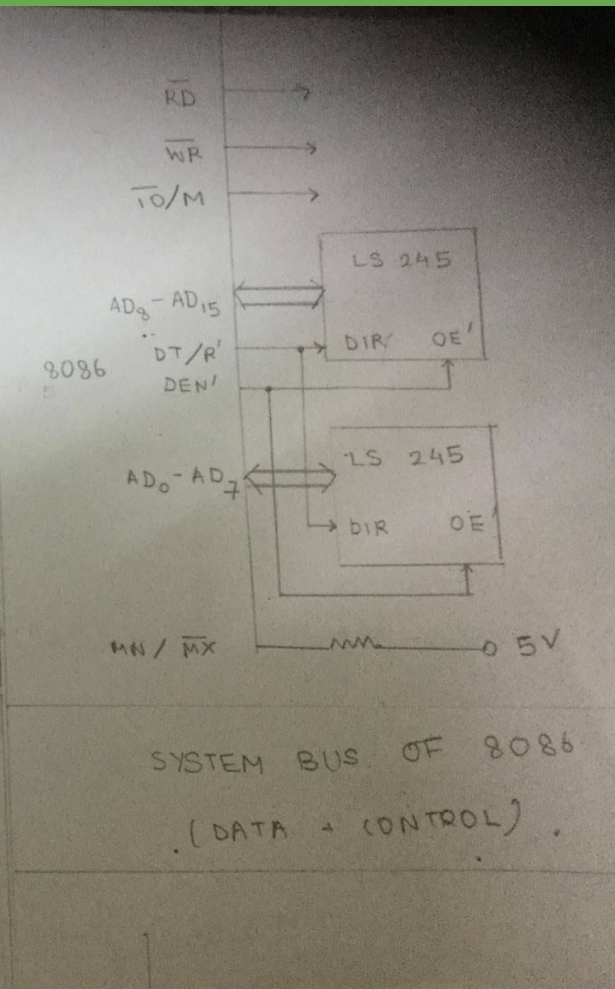
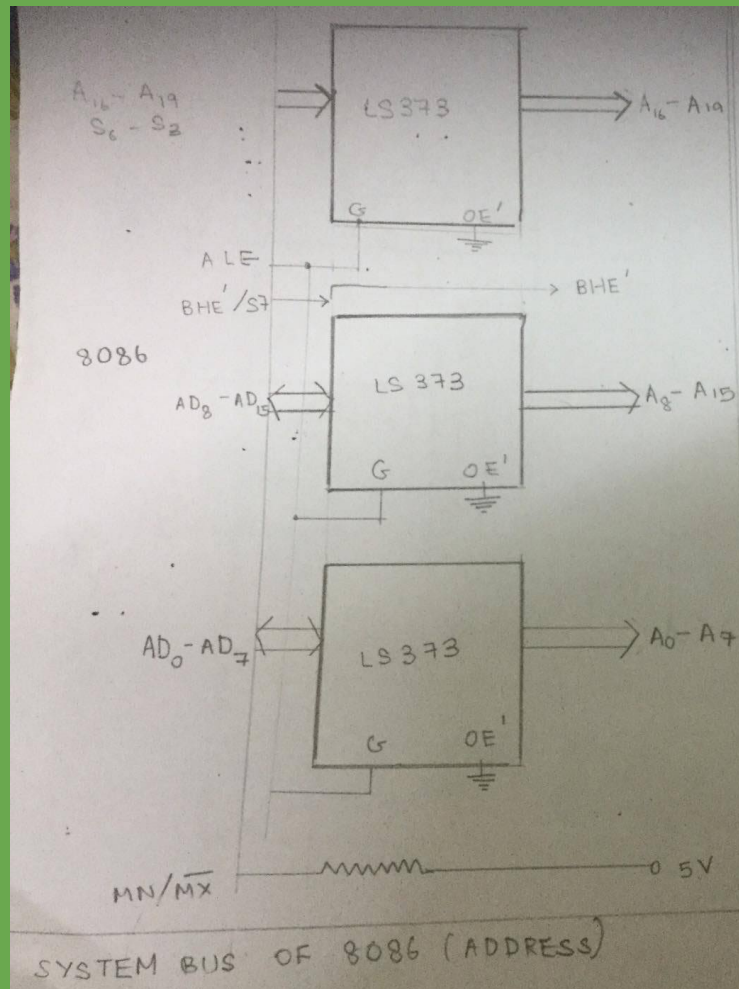
ROM1: FE000H-FFFFFFH

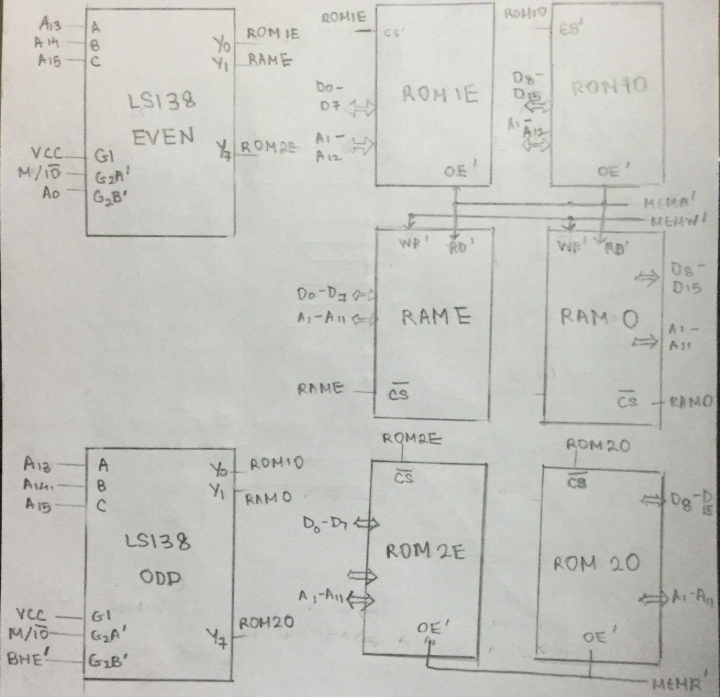
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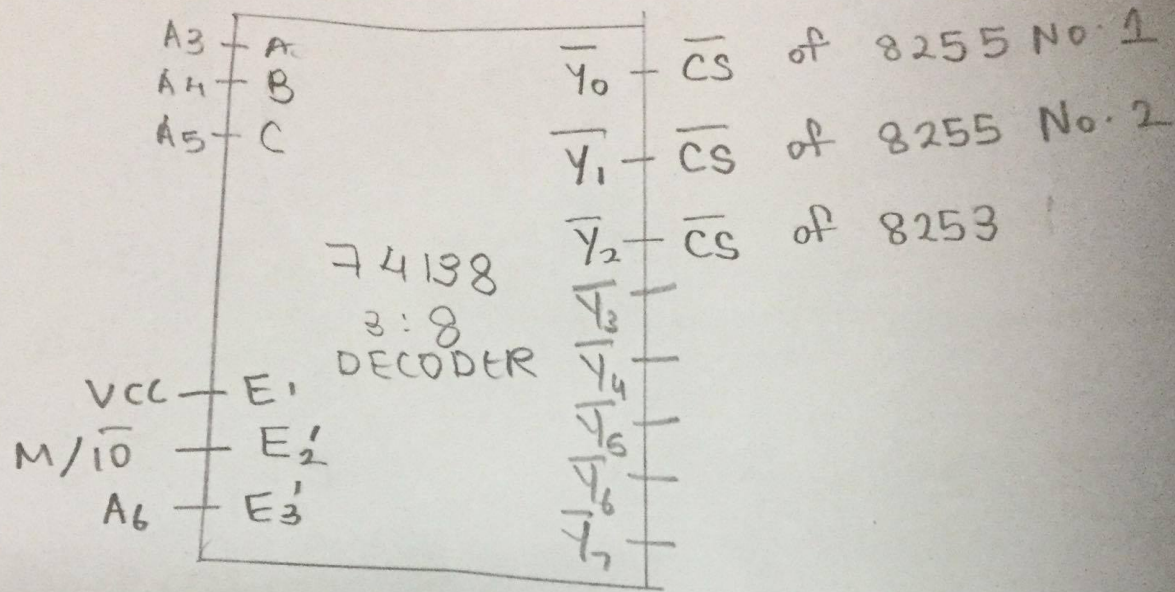
RAM : 02000-02FFFH

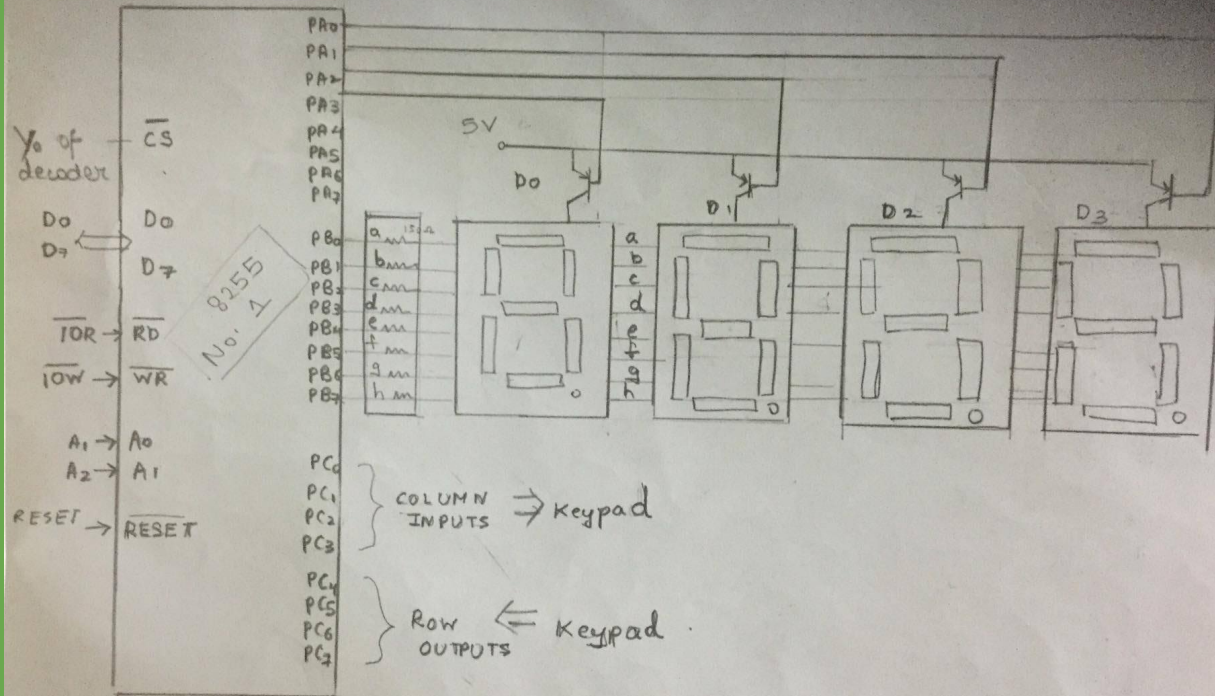
A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	...	10
0	0	0	0	0	0	1	0	0	0	0	...	0
0	0	0	0	0	0	1	0	1	1	1	...	1



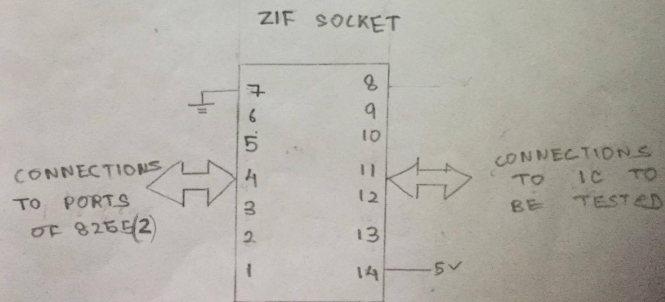
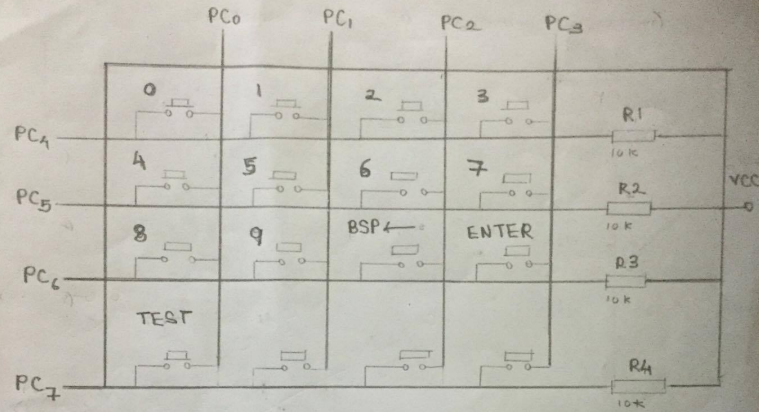


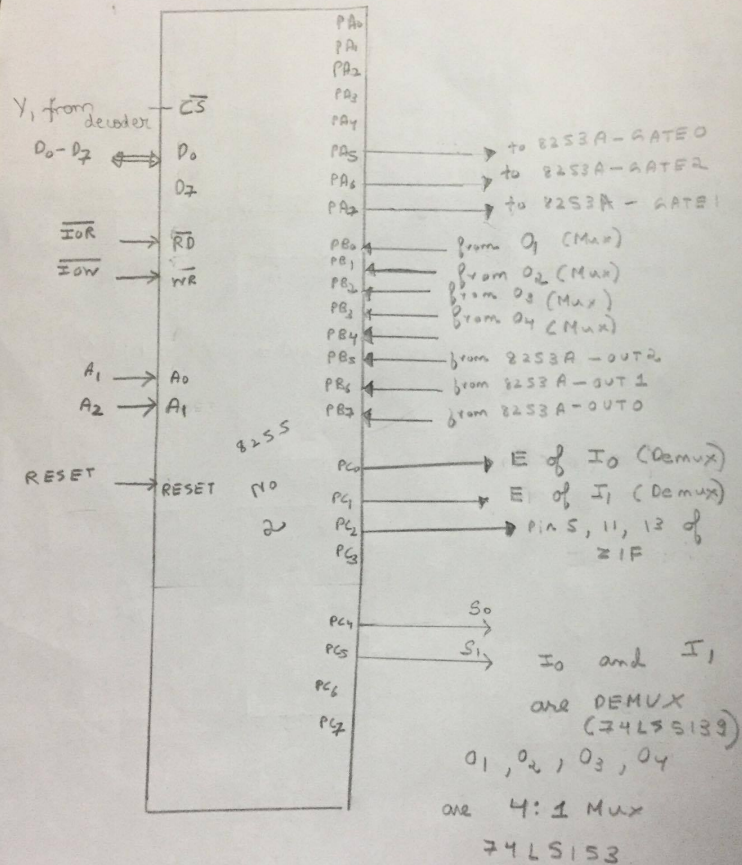






(to 8255(1))





84:90 9107-82-4

Inputs are classified as I_1, I_2 and I_3 (I_3 is only for 7410)

O/p are classified as O_1, O_2 , and O_3 and O_4 (O_4 is for 7400 and 7402)

Pins of 2ett →

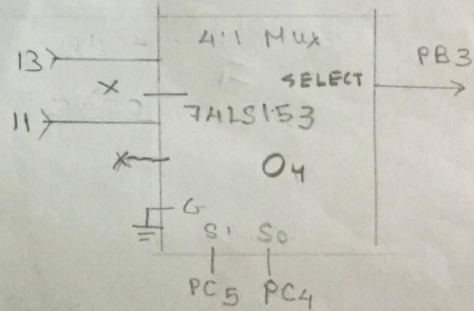
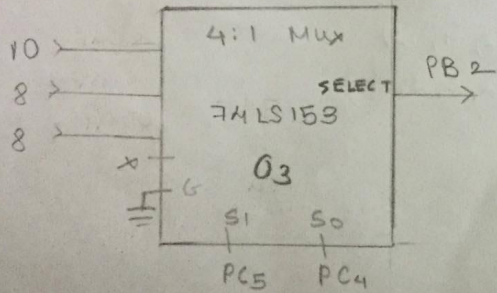
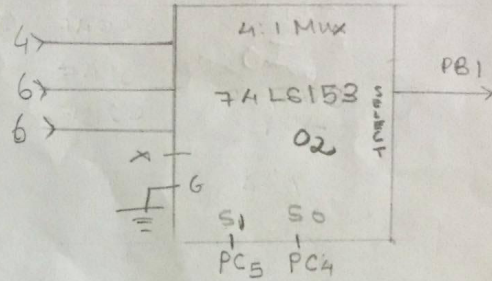
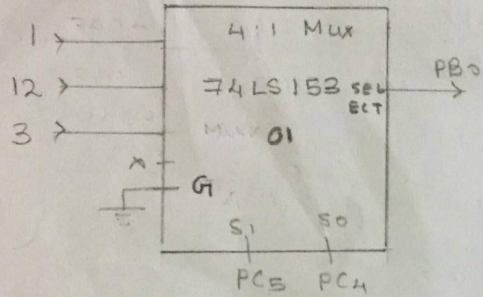
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
7402	O_1	I_1	I_2	O_2	I_1	I_2	G	I_1	I_2	O_3	I_1	I_2	O_4	V
7410	I_1	I_2	I_1	I_2	I_3	O_2	G	O_3	I_1	I_2	I_3	O_1	I_3	V
7400	I_1	I_2	O_1	I_1	I_2	O_2	G	O_3	I_2	I_1	O_4	I_2	I_1	V

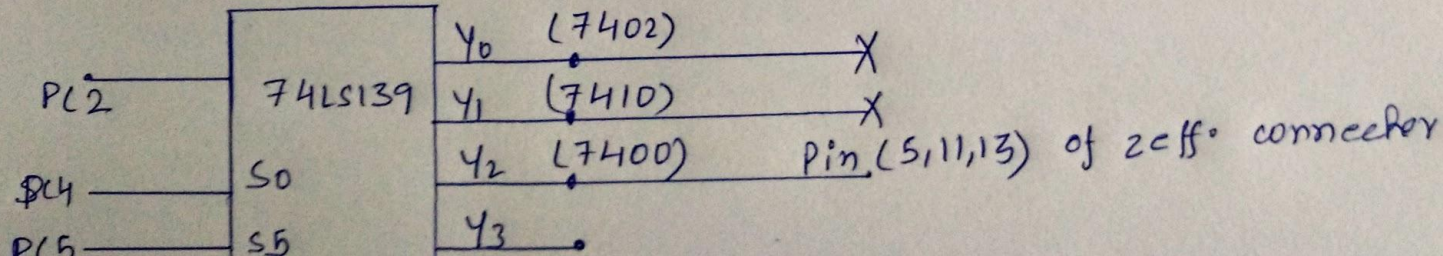
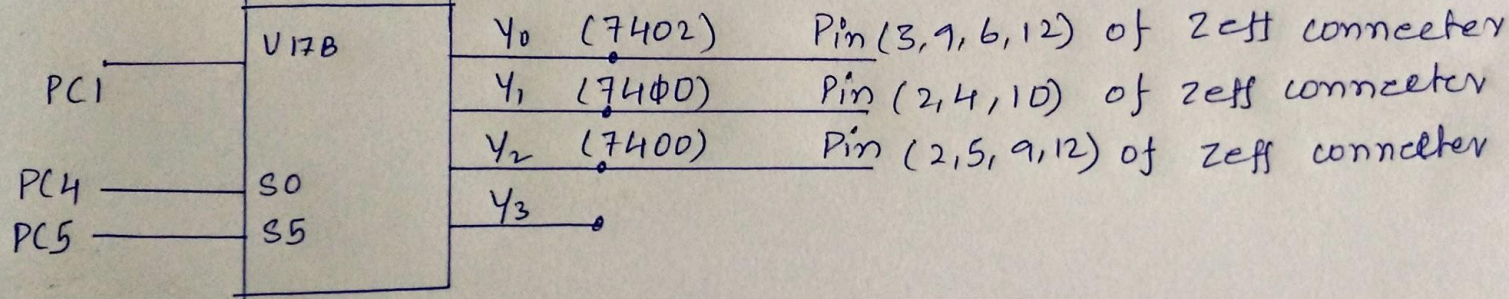
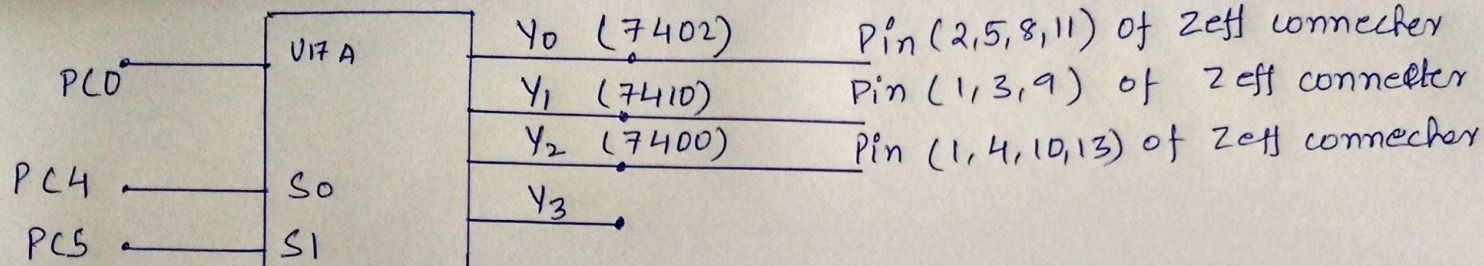
G: GND

V: Vcc

OUTPUT

MULTIPLEXING





8086 with 8284 clock generator

