MPSL2019

Lab3

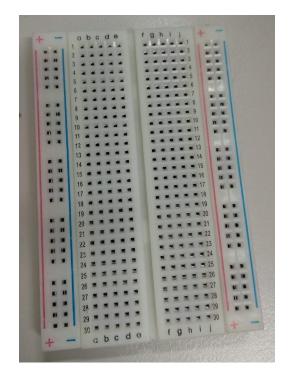
Components of lab

- Breadboard
- 4DIP Switch
- 1K Ω Network Resistor *1
- LED *4
- 220 Ω resistor *4





Breadboard



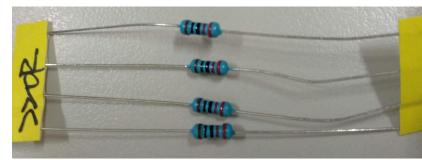
1k Ω Network resistor





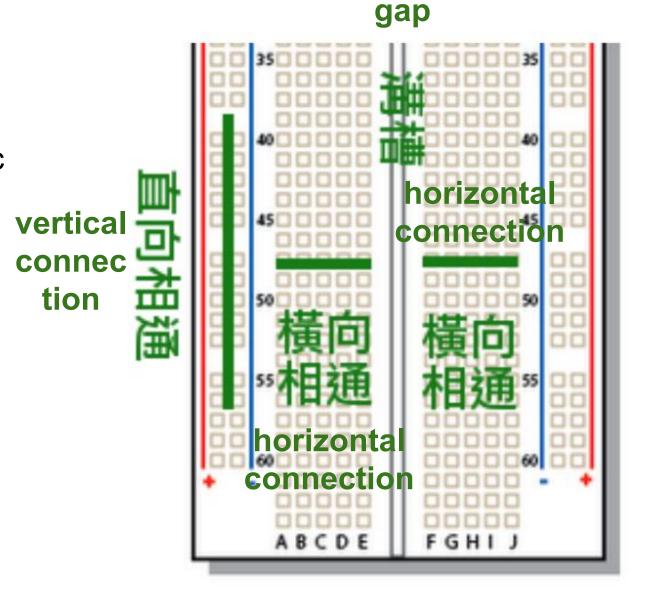
220 Ω resistor *4





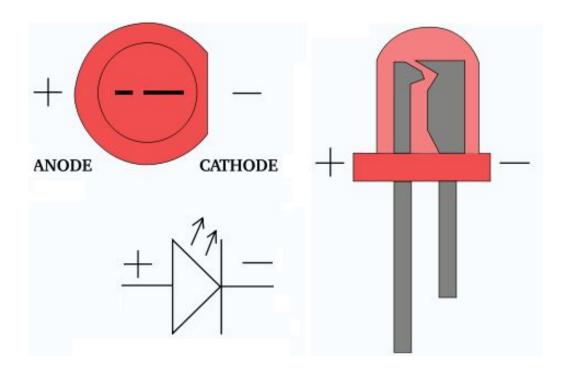
Breadboard

- Easy to connect electronic components
- Please be careful when plugging and unplugging

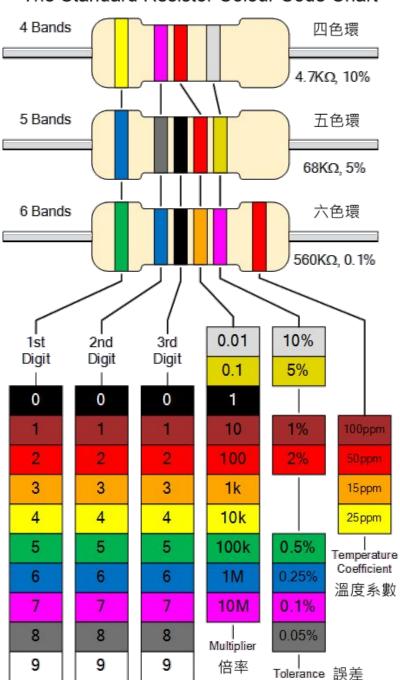


Resistor and LED

- mark resistor value by colour code
- the long pin of LED is positive (+)



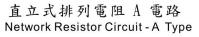
電阻色碼表 The Standard Resistor Colour Code Chart

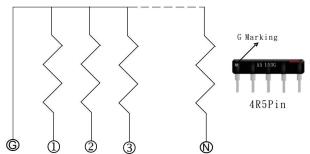


Network resistor 排列電阻

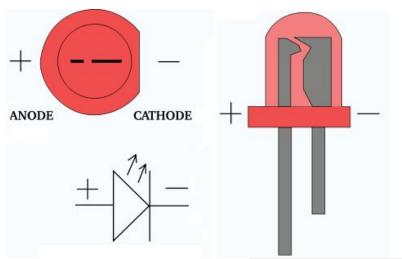
- many resistors in it
- mark resistor value by number, e.g : $102=10*10^2$ = 1K Ω

network resistor naming				
circuit type	number of pins	resistor value	difference	
 A: all resistors share one pin (leftmost) B: each resistor has its own independent pin 	4 ~ 14	three-digital first and second digital are valid number and third digital is number of zero after valid number	 F: ±1% G: ±2% J: ±5% 	





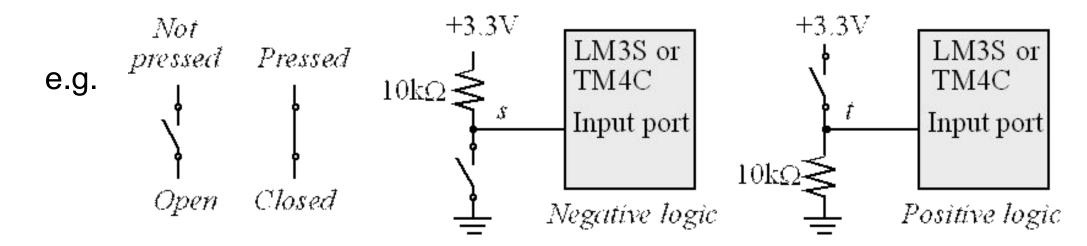
Our network resistor name is "A 102 J". The "A" means all resistors share one pin. 102 means 1K Ω



排阻命名方法			
第一部分電路類型	第二部分引 腳數	第三部分阻值	第四部分 誤差
A-所有電阻共用一端,公共端從左端(第1引腳)引出B-每個電阻有各自獨立引腳,相互間無連接C-各個電阻首尾相連,各連接到均有引出腳D-所有電阻共用一端,公共端從中間引出E、F、G、H、I-內部連接較複雜,不常用,此次略去	4~14	3位數字(第1、2 位為有效數,第3 位為有效數後面0 的個數,如102表 示1000Ω)	F-±1%G- ±2%J- ±5%

Negative logic and Positive logic

- logic can mean to the logical level received by the CPU when a component "action" or "trigger"
- Positive logic or Active High
 - When component actions, CPU receives High level ("1")
- Negative logic or Active Low
 - When component actions, CPU receives Low level ("0")



Hardware Sketch

http://fritzing.org/