
ECE 483 FINAL PROJECT

Low Dropout Regulator Design

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1 Overall Design Approach

Given the specification, the two essential requirements that affect the amplifier design are the DC line regulation $\leq 500\mu\text{V}/\text{V}$ and the DC load regulation $\leq 50\mu\text{V}/\text{mA}$. Therefore, for the line regulation, $L_R \approx \frac{1}{\beta A_{EA0}} \leq 500\mu\text{V}/\text{V} = 5 \times 10^{-4}\text{V}/\text{V}$, and $\beta A_{EA0} \geq 2000$. Then for the load regulation, $LD_R \approx \frac{r_{dsp}}{1+A_{EA0}g_{mp}r_{dsp}\beta} \approx \frac{r_{dsp}}{A_{EA0}g_{mp}r_{dsp}\beta} = \frac{1}{g_{mp}A_{EA0}\beta} \leq 50\mu\text{V}/\text{mA} = 0.05\text{V}/\text{A}$, and $g_{mp} \geq 10\text{mS}$.

For the pass PMOS, other than the load regulation, a $V_{dsat} \leq 1.8 \times 0.9 - 1.4 = 0.22\text{V}$ at $I_L = 20\text{mA}$ is required to keep the pass element in saturation. To satisfy this, the pass PMOS dimension was determined to be $\frac{1999.98\mu\text{m}}{0.18\mu\text{m}}$ by simulation. $g_{mp} \geq 10\text{mS}$ was also satisfied by this dimension across all conditions.

Based on the above analysis, a $V_{REF} = 0.9\text{V}$ was chosen along with a folded-cascode OTA with both PMOS and NMOS differential inputs to increase the gain. $A_{EA0} \geq 3200$ (70.1dB) was required to meet the specifications. A folded-cascode OTA with a $A_{EA0} \approx 3400$ (70.6dB) was made to serve as the error amplifier.

However, it was later found that a smaller β would be more favorable when stabilizing the amplifier, and a higher gain was hence necessary. We decided to modify the topology to a folded-triple-cascode OTA with both PMOS and NMOS differential inputs. A $V_{REF} = 0.75\text{V}$ was chosen since this was the minimum voltage for the NMOS differential input to work well. In this case, $A_{EA0} \approx 56000$ (95dB). The amplifier worked well across all specified conditions, and performance requirements were satisfied. V_{REF} could actually be lower for higher stability while the gain may still high enough to meet the specifications, but we kept it at 0.75V to have good line and load regulations. A design with only the PMOS differential input was also conceived, but it would require larger PMOS sizes that would bring the secondary pole to a lower frequency, offsetting the benefit brought by a lower β value. Thus, the former amplifier was kept as the final design. The quiescent current for the error amplifier is approximately $270\mu\text{A}$ which is reasonable.

The pass element dimension was kept at $\frac{1999.98\mu\text{m}}{0.18\mu\text{m}}$ to make sure that it is in saturation across all conditions. $R_{F1} + R_{F2} = 2k\Omega$ was chosen for stability and moderate quiescent current. A table of resistance values for $V_{OUT} = 1.0\text{V}$ and $V_{OUT} = 1.4\text{V}$ can be found below. A miller compensation capacitor of 15pF was added so that the loop gain phase margin is at least 45° .

Table 1: R_{F1} and R_{F2} Values

V_{out}	β	R_{F1}	R_{F2}
1.0V	0.75	500Ω	1500Ω
1.4V	0.536	928.57Ω	1071.43Ω

2 Complete Design

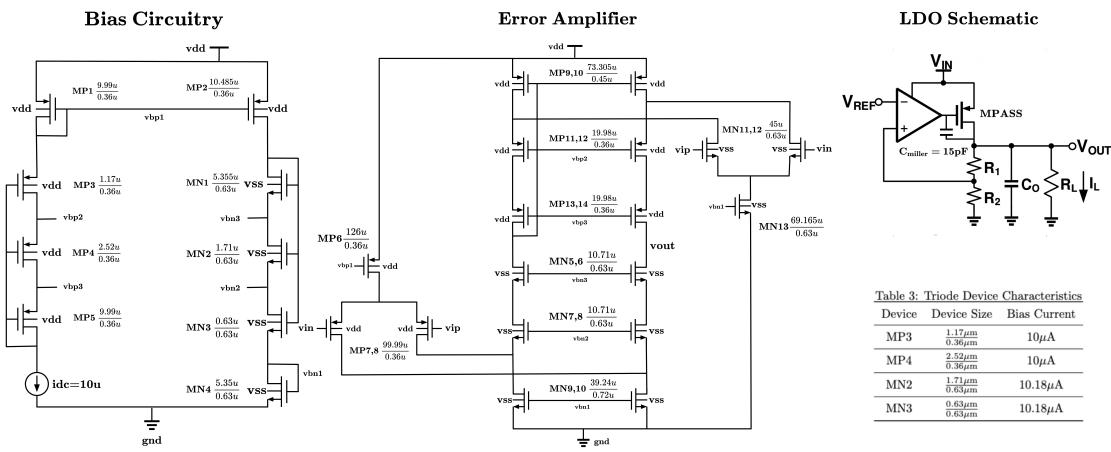


Figure 1: Complete LDO Design and Transistors Characteristics at $V_{OUT} = 1.4\text{V}$ and $I_L = 20\text{mA}$

Table 2: Saturated Device Characteristics				
Device	Device Size	Bias Current	g_m	Δ
MP1	$0.99\mu\text{m} \times 0.36\mu\text{m}$	$10\mu\text{A}$	$162.1\mu\text{s}$	95.54mV
MP2	$10.48\mu\text{m} \times 0.36\mu\text{m}$	$10.18\mu\text{A}$	$165.9\mu\text{s}$	95.50mV
MP5	$9.99\mu\text{m} \times 0.36\mu\text{m}$	$10\mu\text{A}$	$161.7\mu\text{s}$	104.8mV
MN1	$5.355\mu\text{m} \times 0.63\mu\text{m}$	$10\mu\text{A}$	$178.2\mu\text{s}$	95.38mV
MN4	$5.355\mu\text{m} \times 0.63\mu\text{m}$	$10\mu\text{A}$	$172\mu\text{s}$	90.44mV
MP6	$126\mu\text{m} \times 0.36\mu\text{m}$	$123.2\mu\text{A}$	2.011mS	95.58mV
MP7	$9.99\mu\text{m} \times 0.36\mu\text{m}$	$61.62\mu\text{A}$	1.139mS	82.13mV
MP8	$9.99\mu\text{m} \times 0.36\mu\text{m}$	$61.62\mu\text{A}$	1.139mS	82.13mV
MP9	$73.305\mu\text{m} \times 0.45\mu\text{m}$	$66.89\mu\text{A}$	1.001mS	104.6mV
MP10	$73.305\mu\text{m} \times 0.45\mu\text{m}$	$66.89\mu\text{A}$	1.001mS	104.6mV
MP11	$19.98\mu\text{m} \times 0.36\mu\text{m}$	$5.113\mu\text{A}$	$105.5\mu\text{s}$	63.79mV
MP12	$19.98\mu\text{m} \times 0.36\mu\text{m}$	$5.113\mu\text{A}$	$105.6\mu\text{s}$	63.77mV
MP13	$19.98\mu\text{m} \times 0.36\mu\text{m}$	$5.113\mu\text{A}$	$108.4\mu\text{s}$	63.33mV
MP14	$19.98\mu\text{m} \times 0.36\mu\text{m}$	$5.113\mu\text{A}$	$108.5\mu\text{s}$	62.89mV
MN5	$10.71\mu\text{m} \times 0.63\mu\text{m}$	$5.113\mu\text{A}$	$113\mu\text{s}$	58.23mV
MN6	$10.71\mu\text{m} \times 0.63\mu\text{m}$	$5.113\mu\text{A}$	$113.1\mu\text{s}$	58.36mV
MN7	$0.71\mu\text{m} \times 0.63\mu\text{m}$	$5.113\mu\text{A}$	$109.4\mu\text{s}$	59.76mV
MN8	$39.24\mu\text{m} \times 0.72\mu\text{m}$	$66.74\mu\text{A}$	1.091mS	93.77mV
MN9	$39.24\mu\text{m} \times 0.72\mu\text{m}$	$66.74\mu\text{A}$	1.091mS	93.77mV
MN10	$39.24\mu\text{m} \times 0.72\mu\text{m}$	$66.74\mu\text{A}$	1.091mS	93.77mV
MN11	$45\mu\text{m} \times 0.63\mu\text{m}$	$61.77\mu\text{A}$	1.147mS	80.99mV
MN12	$4.5\mu\text{m} \times 0.63\mu\text{m}$	$61.78\mu\text{A}$	1.147mS	80.99mV
MN13	$69.165\mu\text{m} \times 0.63\mu\text{m}$	$123.5\mu\text{A}$	2.103mS	90.12mV
MPASS	$1999.98\mu\text{m} \times 0.18\mu\text{m}$	20.7mA	189.8mS	179.8mV

3 Performance Summary

Table 4: Performance Summary

Design Parameter	Specification	Simulated Performance
Input Voltage	$1.8V \pm 10\%$	$1.62V \sim 1.98V$
Output Voltage	$1.0V \sim 1.4V$	$1.0V \sim 1.4V$
Load Current	$0.5mA \sim 20mA$	$0.5mA \sim 20mA$
DC Load Regulation ($0.5mA - 20mA/20mA - 0.5mA$); $V_{out} = 1V$	$\leq 50\mu V/mA$	$0.344\mu V/mA / 0.155\mu V/mA$
DC Load Regulation ($0.5mA - 20mA/20mA - 0.5mA$); $V_{out} = 1.4V$	$\leq 50\mu V/mA$	$0.745\mu V/mA / 0.446\mu V/mA$
DC Line Regulation ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1V$	$\leq 500\mu V/V$	$32.795\mu V/V / 35.21\mu V/V$
DC Line Regulation ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1.4V$	$\leq 500\mu V/V$	$28.35\mu V/V / 58.55\mu V/V$
Quiescent current ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1V$	Minimum	$0.777mA / 0.777mA$
Quiescent current ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1.4V$	Minimum	$0.977mA / 0.977mA$
PSR (@ $F_{in} = 1kHz/F_{in} = 1MHz$); $V_{out} = 1V$	—	$-81.4dB / -21.4dB$
PSR (@ $F_{in} = 1kHz/F_{in} = 1MHz$); $V_{out} = 1.4V$	—	$-78.4dB / -18.4dB$
Worst-Case PSR ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1V$	—	$2.163dB@12.85MHz / 1.617dB@39.27MHz$
Worst-Case PSR ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1.4V$	—	$1.432dB@11.730MHz / 1.002dB@37.52MHz$
DC Loop Gain ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1V$	—	$114.1dB / 109.9dB$
DC Loop Gain ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1.4V$	—	$112.7dB / 108.3dB$
Loop-Gain UGF ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1V$	—	$9.548MHz / 10.53MHz$
Loop-Gain UGF ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1.4V$	—	$7.571MHz / 7.781MHz$
Loop-Gain Phase Margin ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1V$	—	$45.39^\circ / 74.37^\circ$
Loop-Gain Phase Margin ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1.4V$	—	$57.51^\circ / 78.36^\circ$
Loop-Gain Gain Margin ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1V$	—	$11.42dB / 11.82dB$
Loop-gain Gain Margin ($I_L = 0.5mA/I_L = 20mA$); $V_{out} = 1.4V$	—	$14.15dB / 14.54dB$
Output Noise	—	$1.436 \times 10^{-9} V^2$

4 Simulated Results

4.1 Loop-Gain AC Response

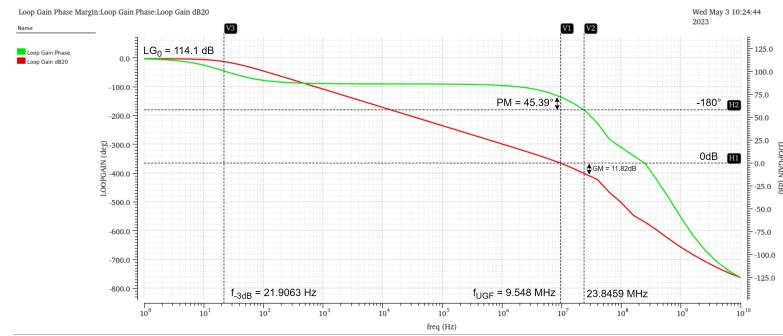


Figure 2: Loop-Gain AC Response for $V_{OUT} = 1.0V$, $I_L = 0.5\text{mA}$

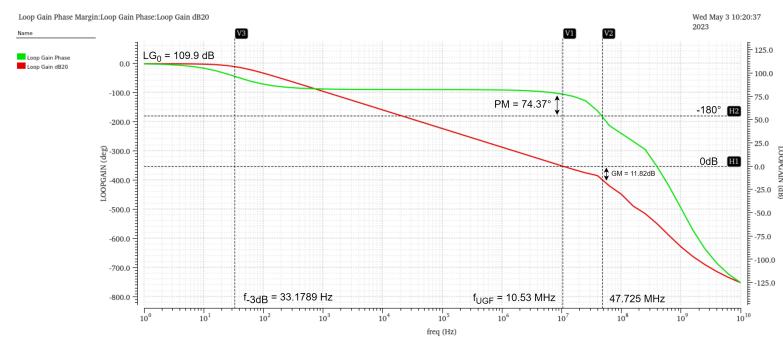


Figure 3: Loop-Gain AC Response for $V_{OUT} = 1.0V$, $I_L = 20\text{mA}$

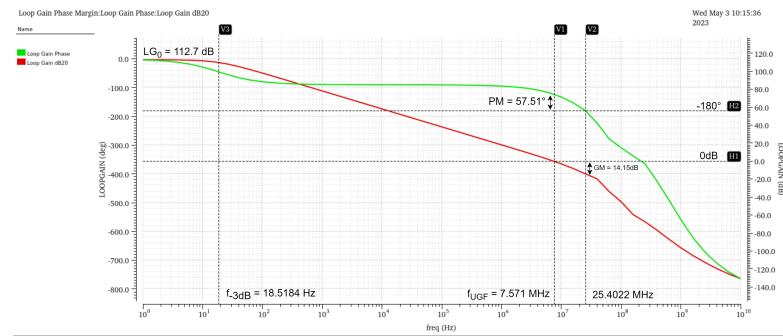


Figure 4: Loop-Gain AC Response for $V_{OUT} = 1.4V$, $I_L = 0.5\text{mA}$

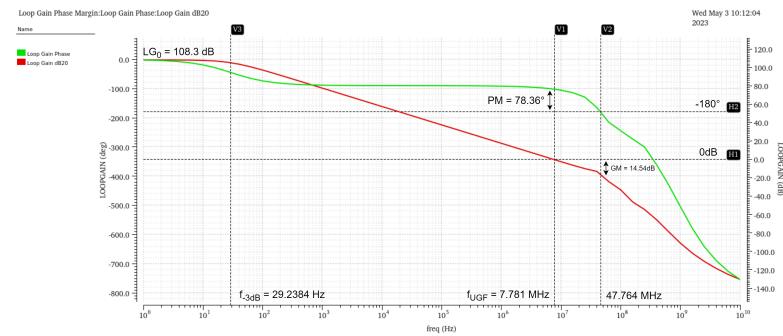


Figure 5: Loop-Gain AC Response for $V_{OUT} = 1.4V$, $I_L = 20\text{mA}$

4.2 DC Load and Line Regulation Response

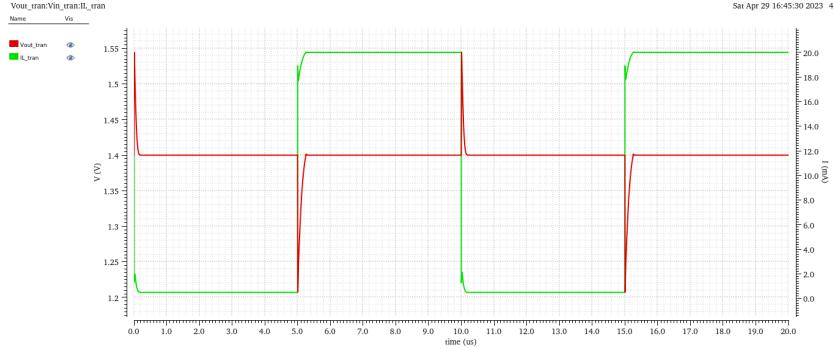


Figure 6: Load Regulation Response for $V_{OUT} = 1.4V$

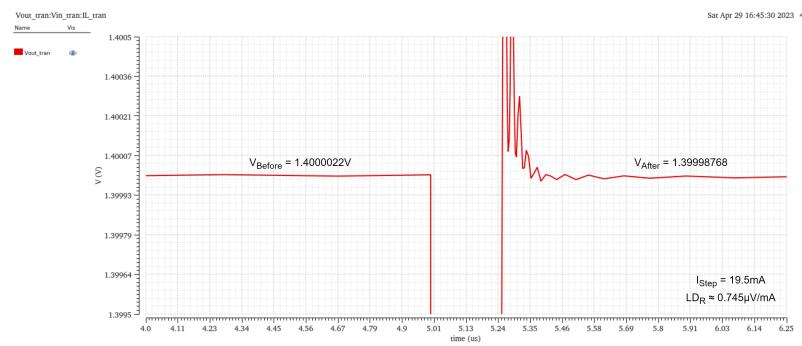


Figure 7: Zoomed-In Load Regulation Response for $V_{OUT} = 1.4V$, Stepping from 0.5mA to 20mA

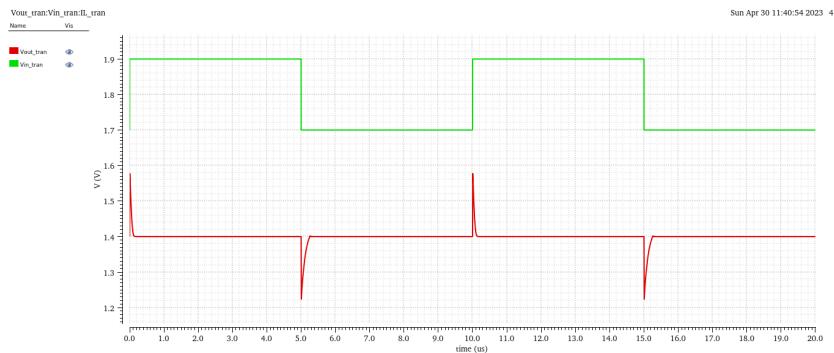


Figure 8: Line Regulation Response for $V_{OUT} = 1.4V$, $I_L = 20mA$

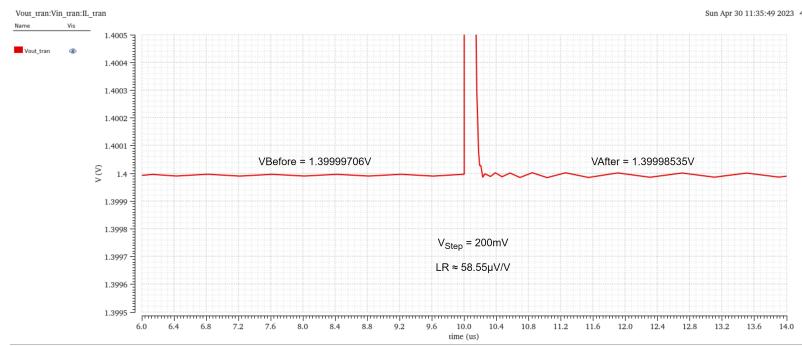


Figure 9: Zoomed-In Line Regulation Response for $V_{OUT} = 1.4V$, $I_L = 20mA$

4.3 Power Supply Rejection (PSR)

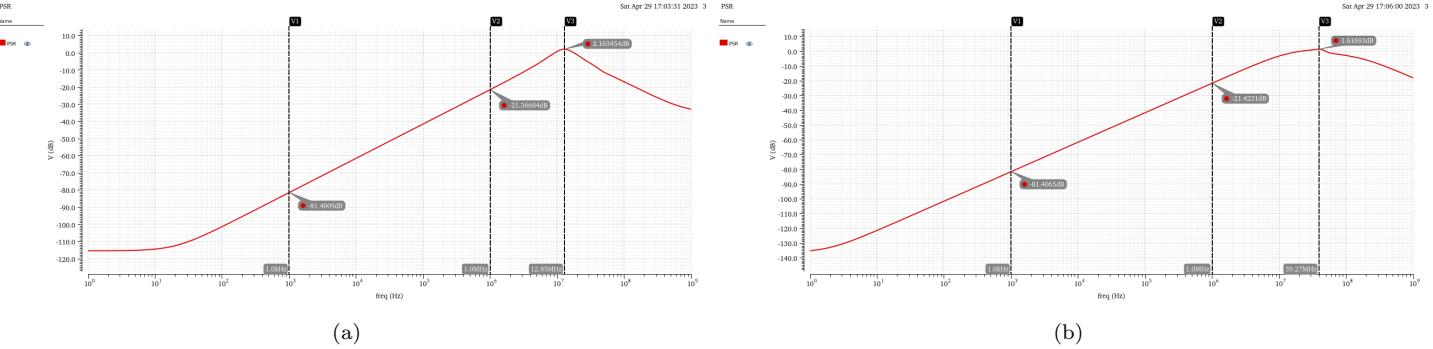


Figure 10: (a) PSR for $V_{OUT} = 1.0V$, $I_L = 0.5\text{mA}$ (b) PSR for $V_{OUT} = 1.0V$, $I_L = 20\text{mA}$

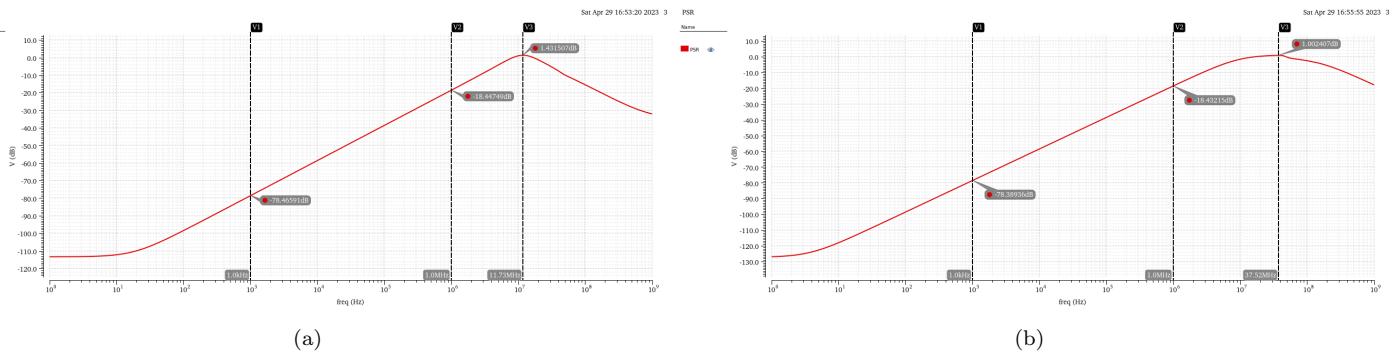


Figure 11: (a) PSR for $V_{OUT} = 1.4V$, $I_L = 0.5\text{mA}$ (b) PSR for $V_{OUT} = 1.4V$, $I_L = 20\text{mA}$

4.4 Output Noise

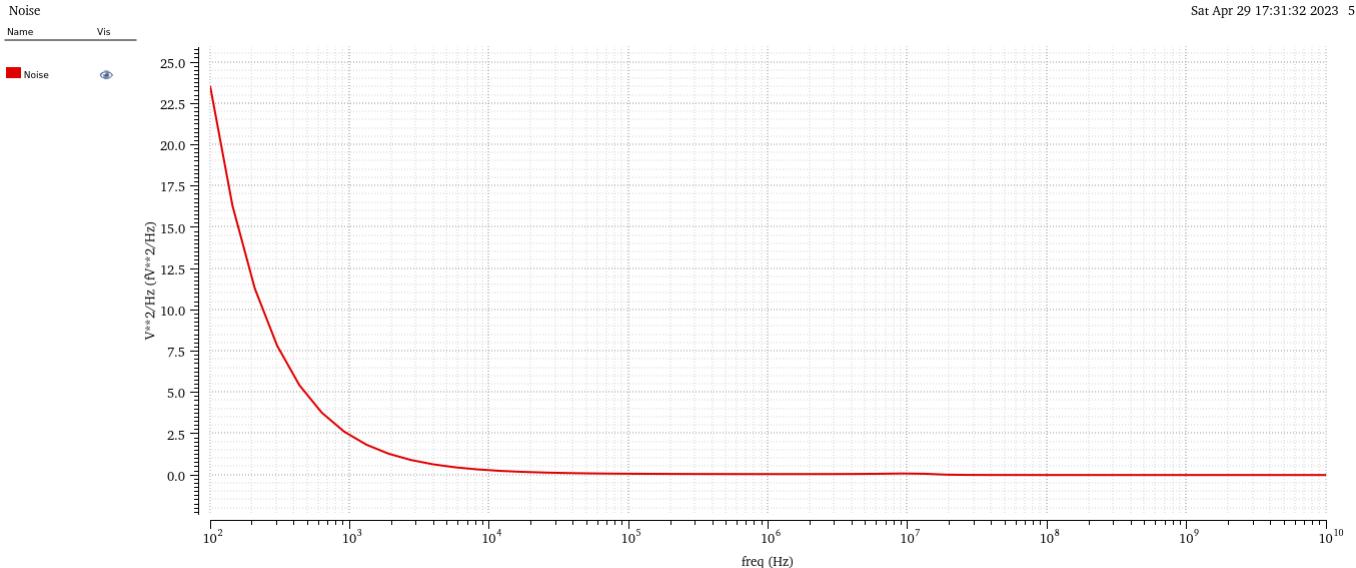


Figure 12: Output Noise Squared