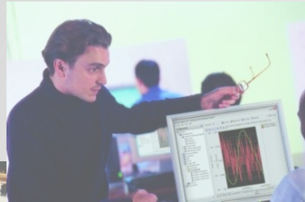


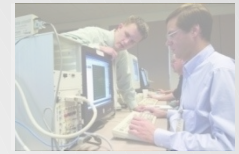


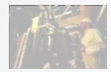

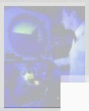


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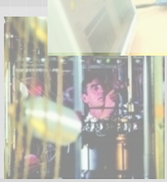
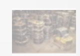



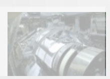

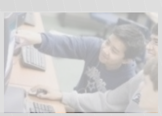


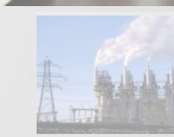
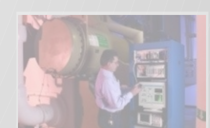

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LabVIEW 2010

Hands-on Session For Current User

Zileriu Vlad
Sales Manager Romania
National Instruments

Exercises for Today's Session

Improved Performance

- Inlining

Tools for Distributed Measurement Systems

- Web Services
- HTTP(s) Nodes

Large Application Development

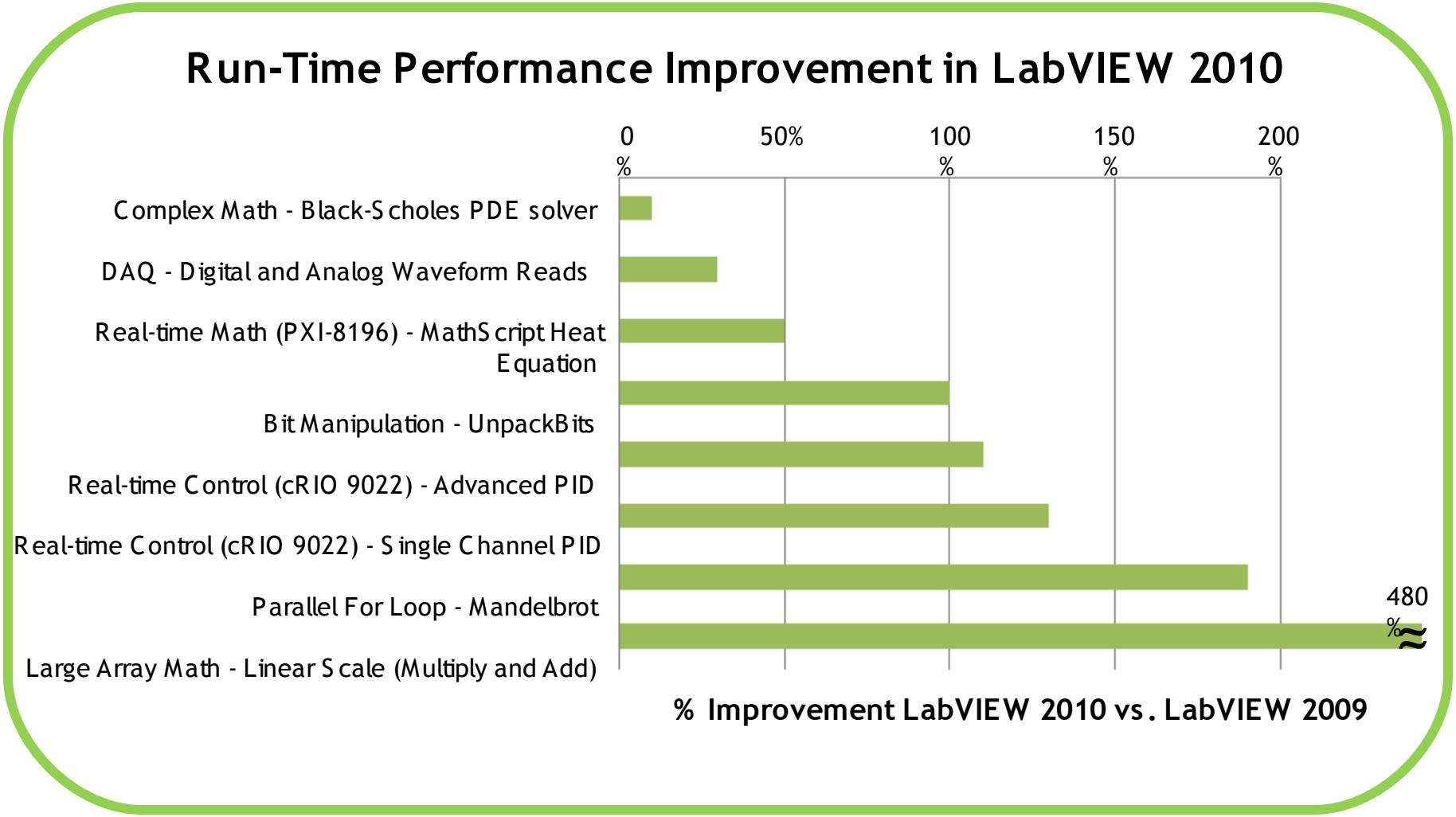
- Packed Project Libraries

Target-to-Host Data Transfer

- Network Streams

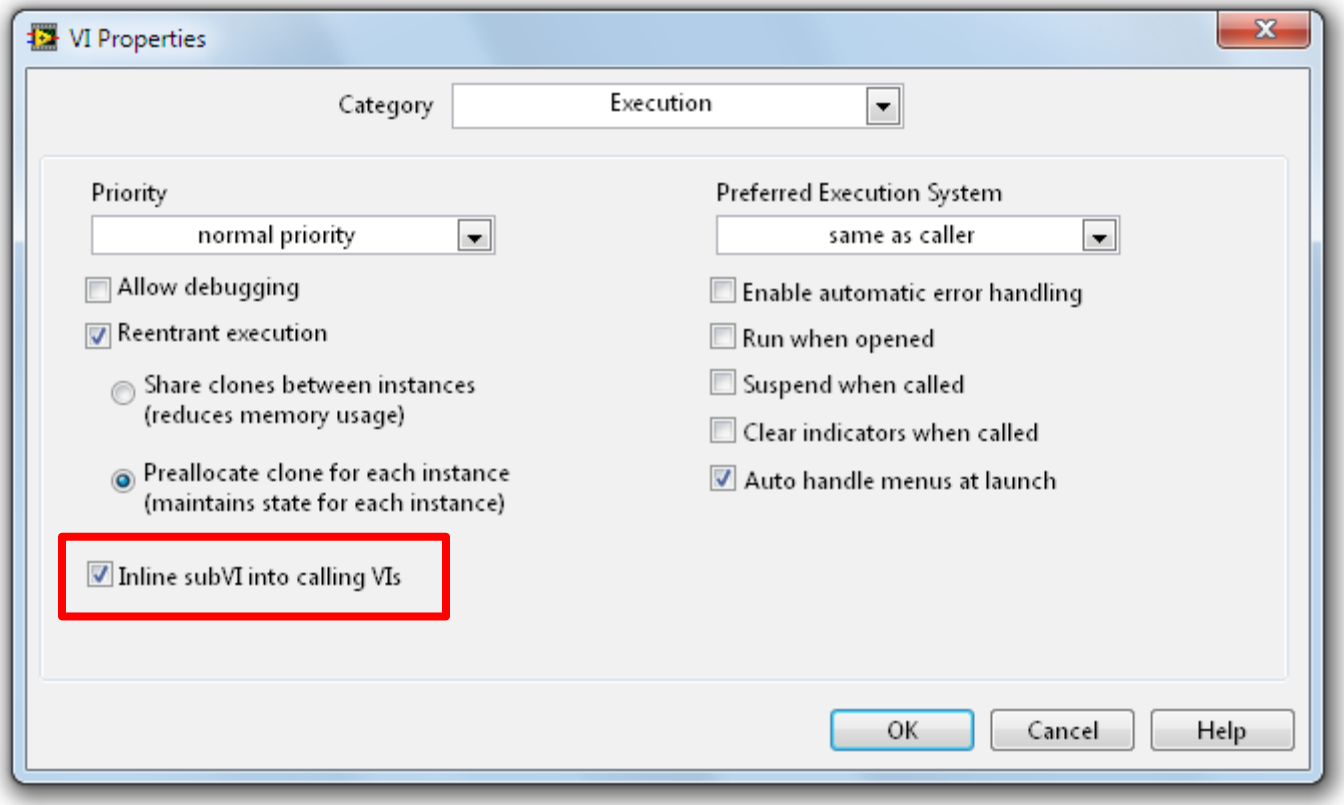
Improved Performance

LabVIEW 2010 Performance Metrics



SubVI Inlining

Maintain Code Modularity With Minimum Overhead



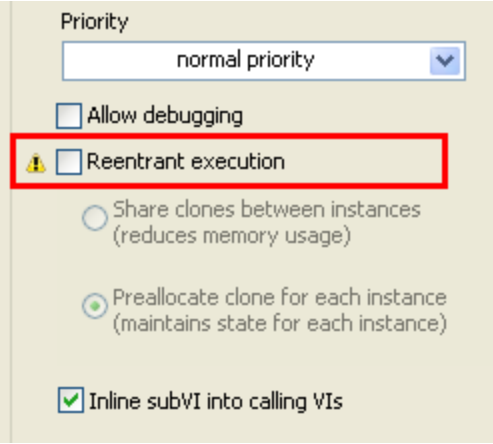
Removes all subVI call overhead

Automatically updates callers when callee's code changes

SubVI Inlining

Maintain Code Modularity With Minimum Overhead

- Debugging Not Allowed
- Reentrant Execution
- Automatic Error Handling Disabled
- Look for Exclamation Marks



Exercise:
Inline Benchmark

New Distributed Measurement Systems

Networking in LabVIEW

Remote monitoring and control is a common requirement

Multiple technologies and factors to consider

LabVIEW Web Services Background

Invoke VIs over the web

- URL selects the VI and specifies input terminal values
- Easily return output terminal values
- Optionally return data of any type using Web Services VI palette

Uses RESTful software architecture

Windows, PharLap, VxWorks

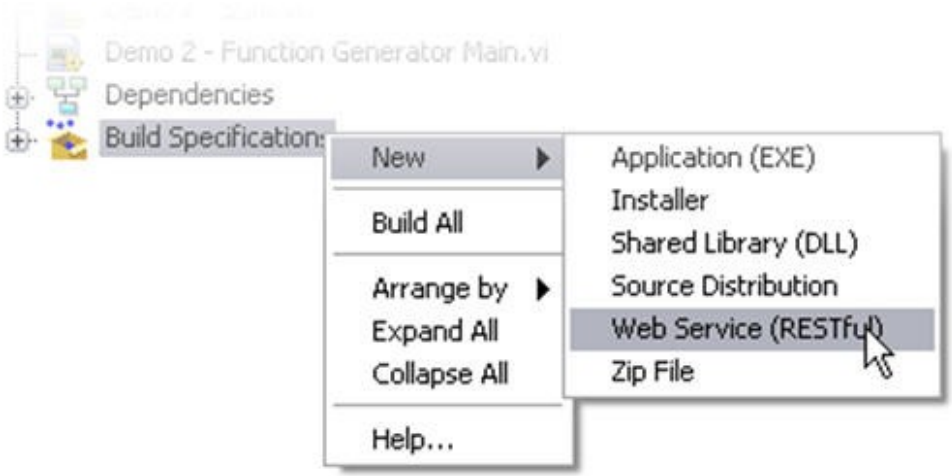
Based on LabVIEW's new embedded web server

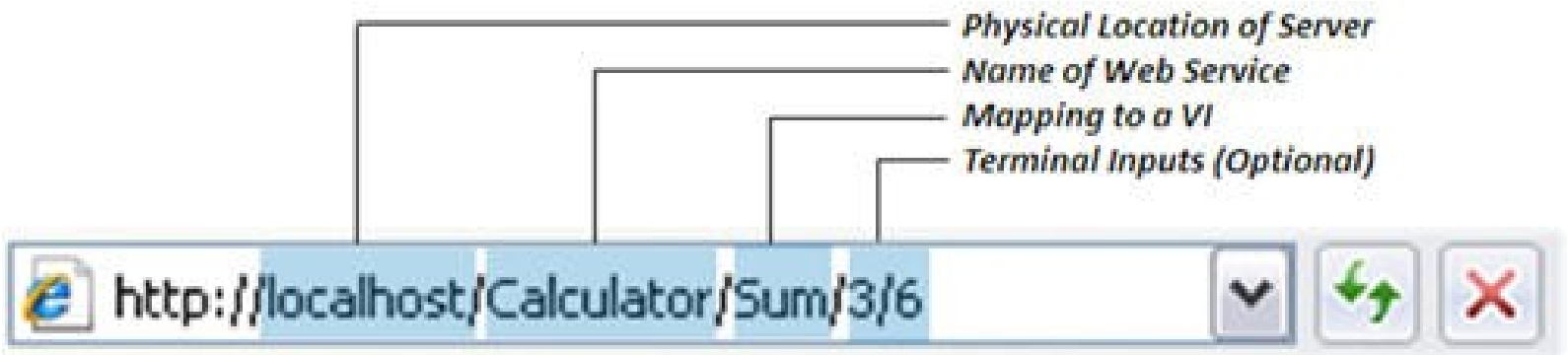
Server-side only

Invoking a VI Using Web Services

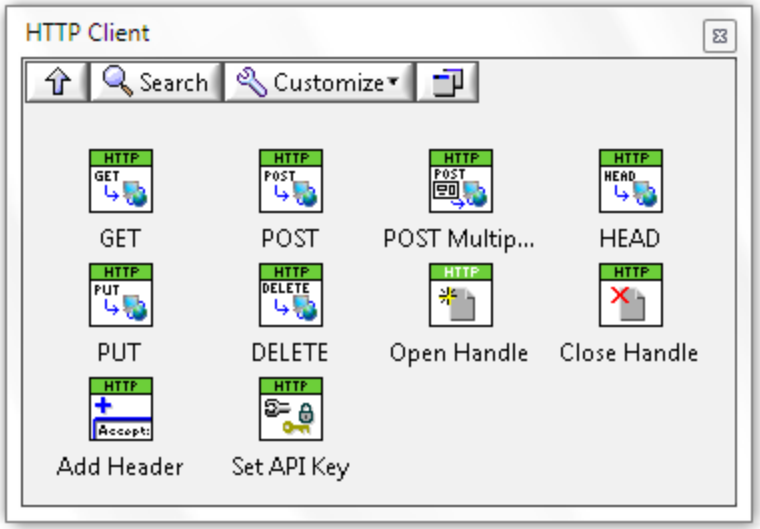
Deploy VIs from Build Specifications

Invoke VI via URL Web Request





HTTP(S) Nodes

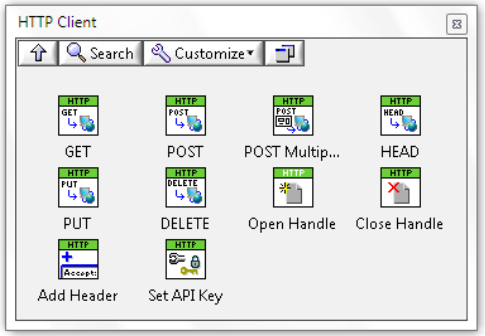


Use the new **HTTP Client VIs** to build a LabVIEW web client

Interact with servers, Web pages, and Web services

Works with LabVIEW or 3rd-party Web services

HTTP(S) Nodes



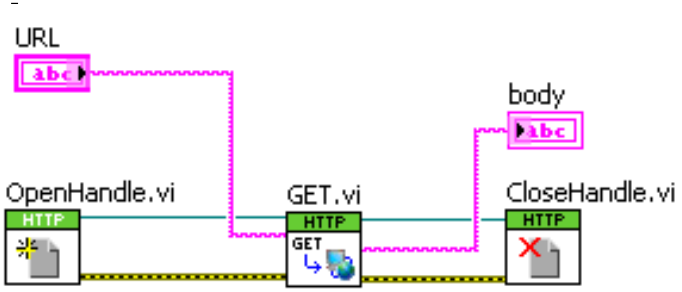
Open/Close Handle - To Establish Communication

HEAD - To Retrieve Header of the Document

GET - To Retrieve The Resource from the Server

POST - To Send Data to the Server

Easy to Create Web Client Appl

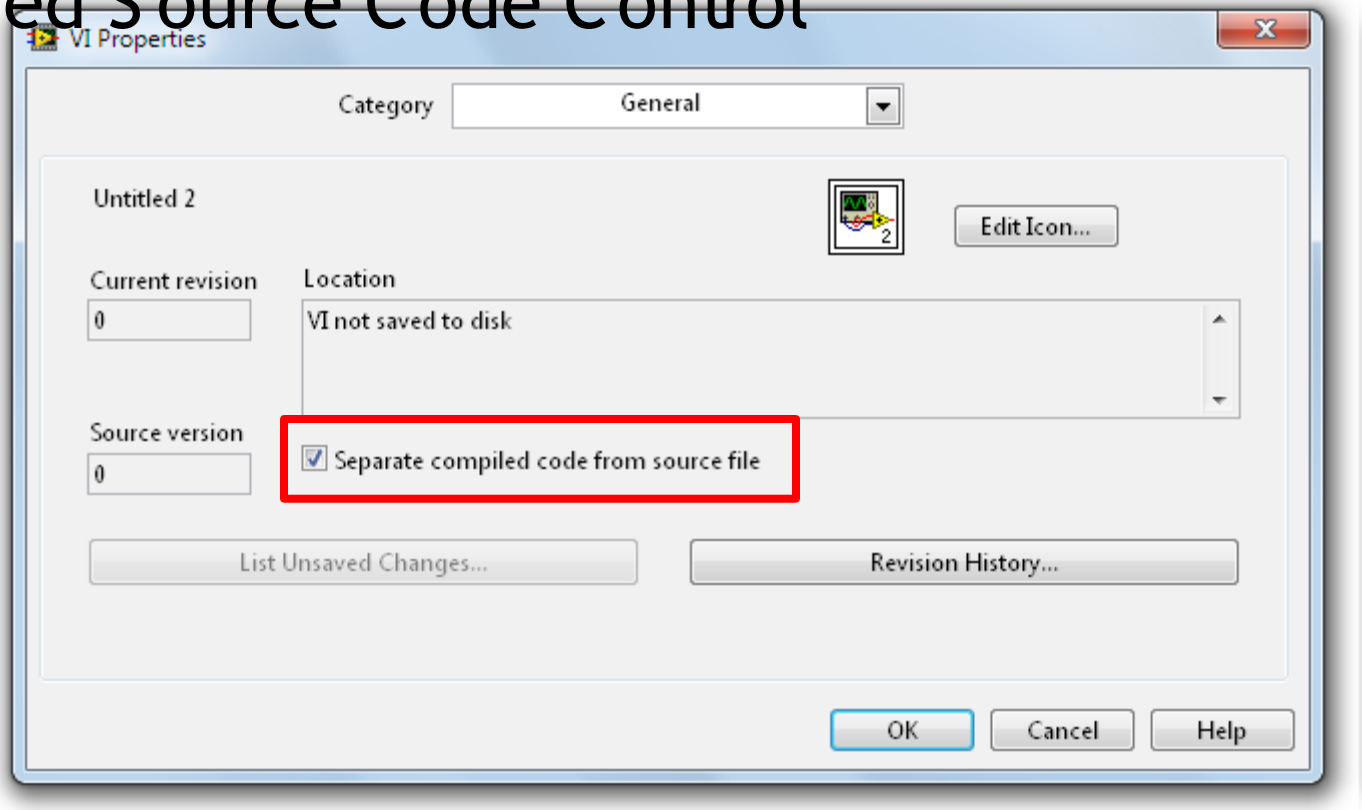


Exercise:
Web Services and HTTP nodes

Large Application Development

Separate Compiled Code From Source File

Improved Source Code Control



Eliminate the need to re-save and re-submit files to source code control unless the graphical source code has been changed by the developer

Packed Project Libraries

Distribute and Reuse LabVIEW Code Easily

- Deploy the VI hierarchy with a single file
- Shorter build times for calling VIs
- Simplified code deployment
- .lvlibp file type

Example	# Source VIs	EXE Build Time	# VIs Built Into PPL	EXE Build Time	Build Time Improvement
Agilent 34401 Acquire and Graph - SW Triggered.vi	53	6.3 s	22	5.15 s	18.2%
E-Mail Notification.vi	102	8.66 s	68	5.82 s	32.8%
Update Weather Data.vi	71	12.97 s	46	5.48 s	57.8%
Custom Example	1000	53.93 s	999	15.94 s	70.4%

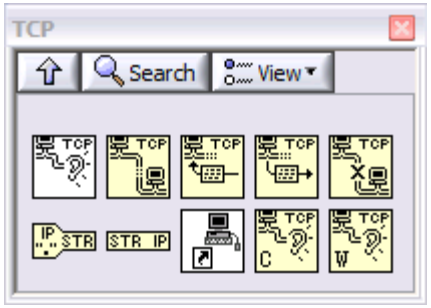
Exercise:
Packed Project Libraries

Target-to-Host Data Transfer

Network Connectivity Options in LabVIEW

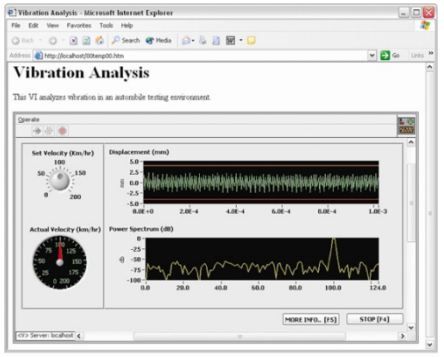
TCP/IP and UDP

Define low-level communication protocols



Remote Front Panels

Quickly embed a front panel in a browser



Shared Variables

Quickly develop distributed systems through drag-and-drop configuration

Network Streaming in LabVIEW

Based on TCP

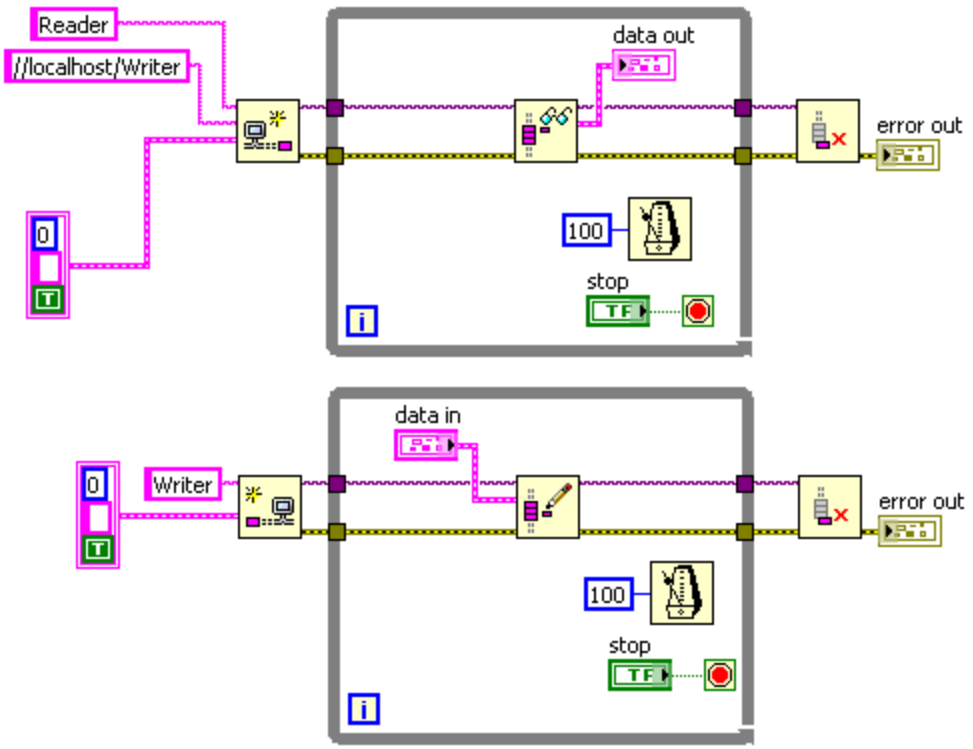
High throughput

Queues-like Experience

Easy to program

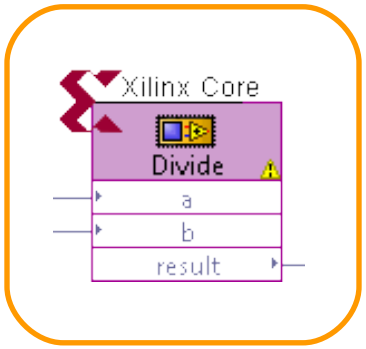
Adaptive Data Type

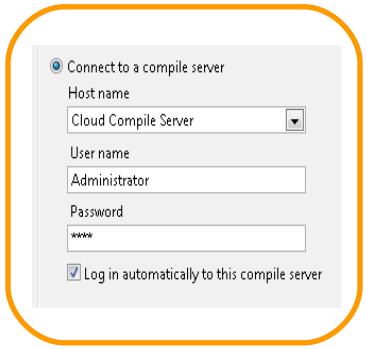
No need to type cast

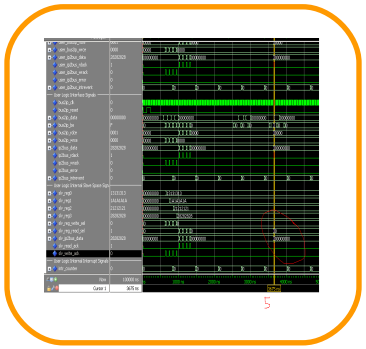


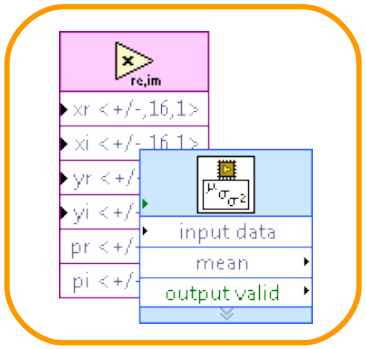
Exercise:
Data Transfer with Network Streaming

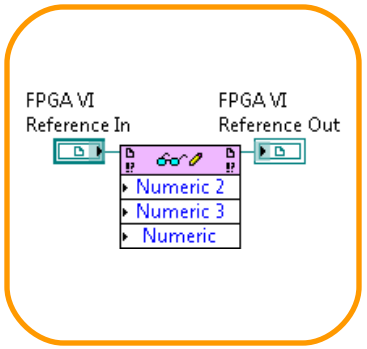
LabVIEW 2010 FPGA Module











IP Integration Node - Directly import Xilinx .xco files or your own VHDL easily

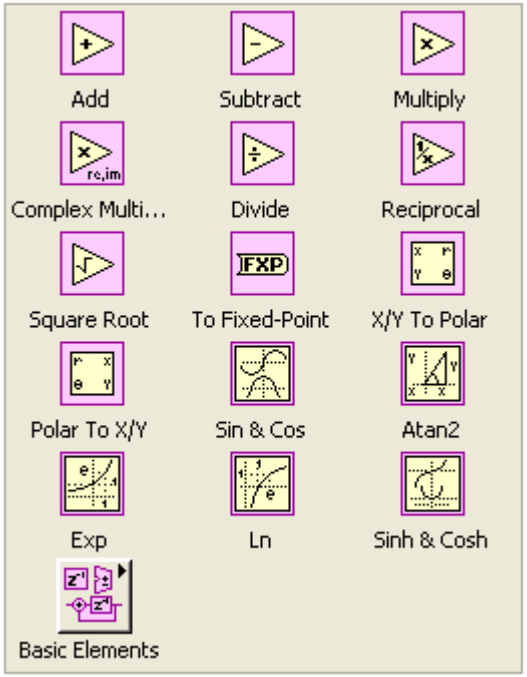
New Compilation Flow - Earlier Compilation Estimates and Build Specifications

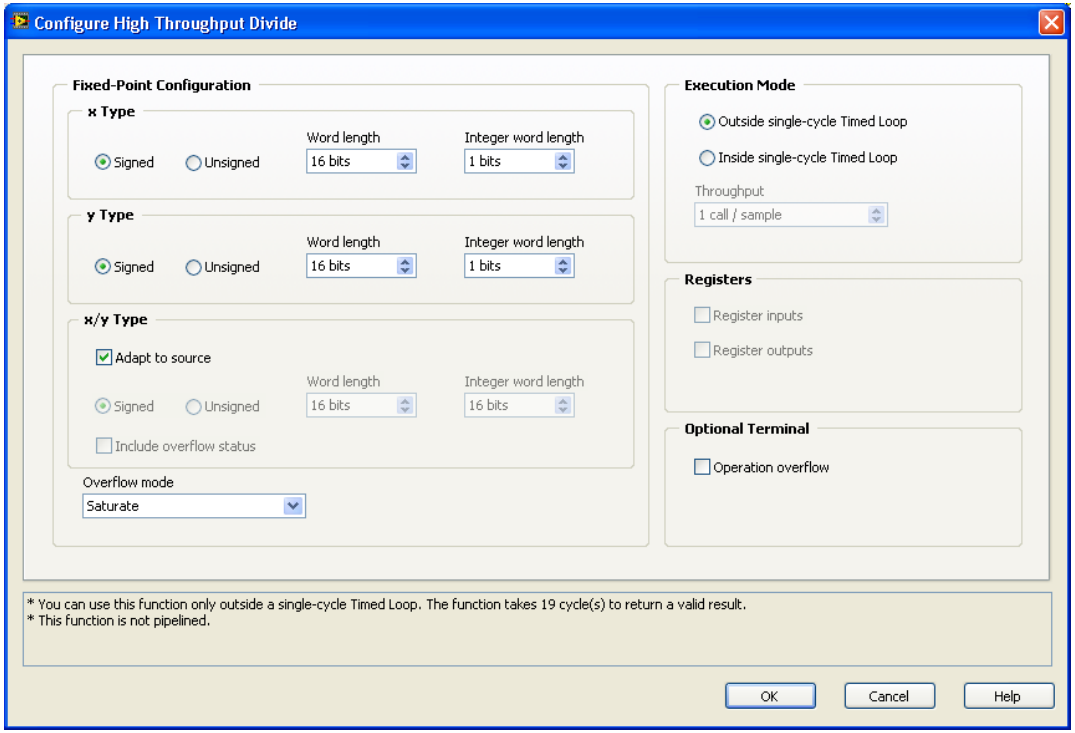
Cycle-Accurate Simulation - Use ModelSim for Cycle-Accurate Simulation

More IP Blocks - New IP for Statistics, Complex Multiplication, and More

Host Improvements – New Dynamic reference for Host VI reuse

FPGA Module - High-Throughput Math

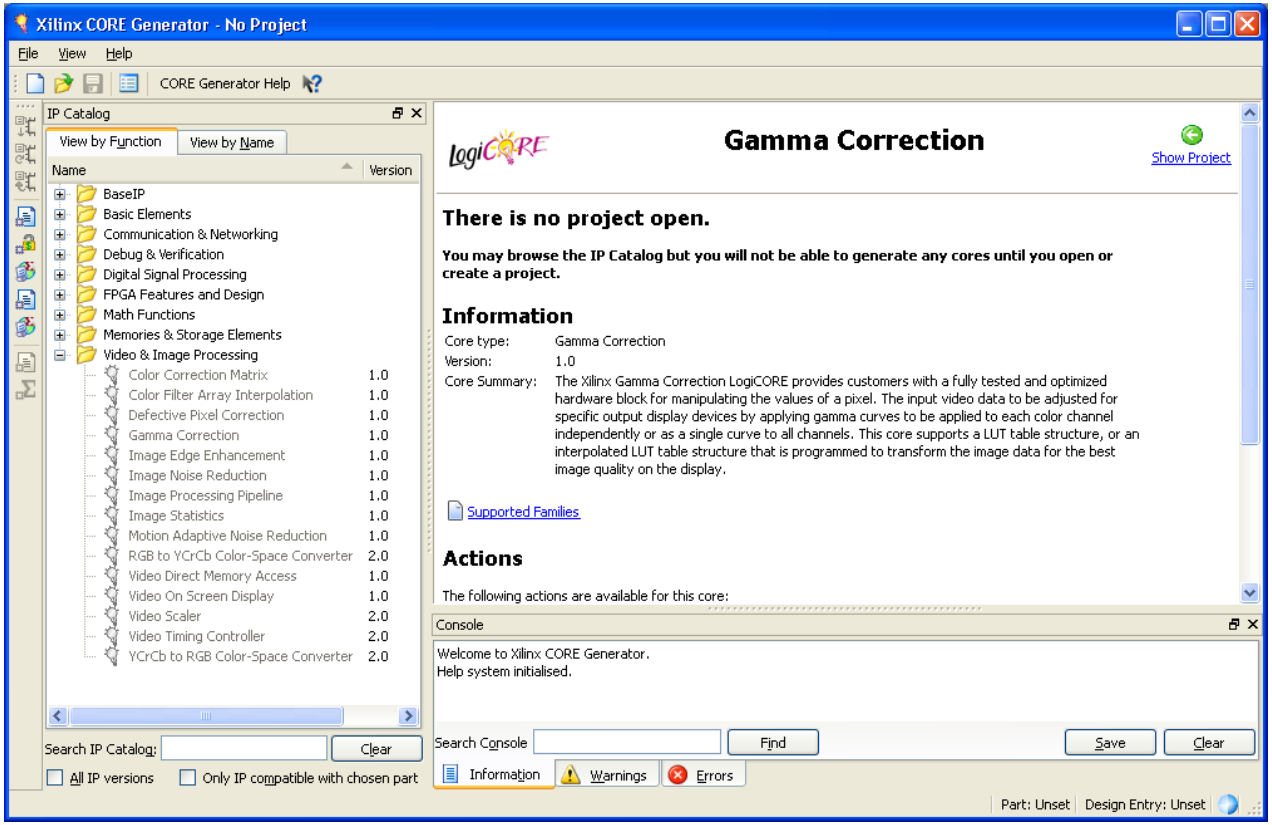




Numerous Mathematical Functions

Execution within one clock cycle (with pipelining)

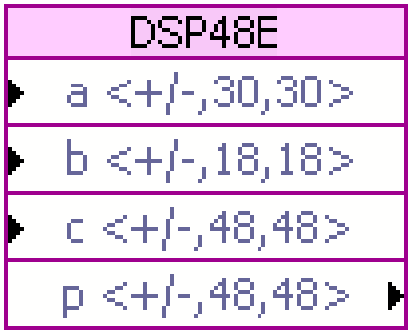
FPGA Module – Additional IP Sources

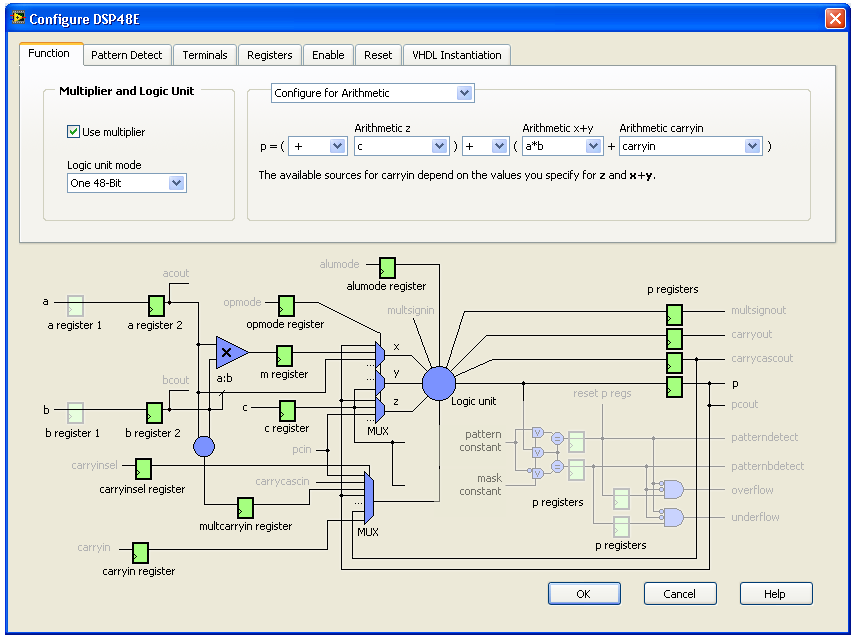


www.ni.com/ipnet - Library of FPGA VIs

Xilinx Core Generator – Wizard-based IP Creator

FPGA Module - (Advanced) DSP48E





Lowest-level FPGA Usage

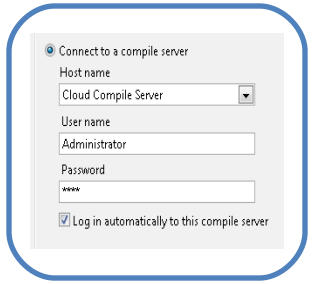
Fastest Throughput (even 550MHz)

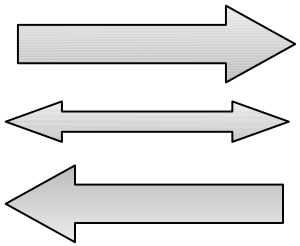
Wizard-based Configuration

Requires Familiarity with Virtex-5 FPGA XtremeDSP Design Considerations User Guide

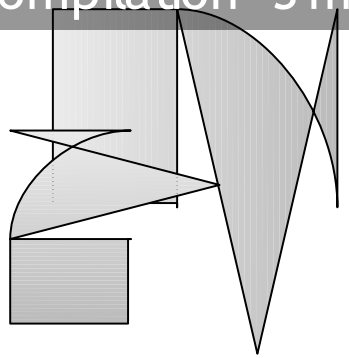
LabVIEW 2010 FPGA Compilation

LabVIEW FPGA Compile Farm Toolkit





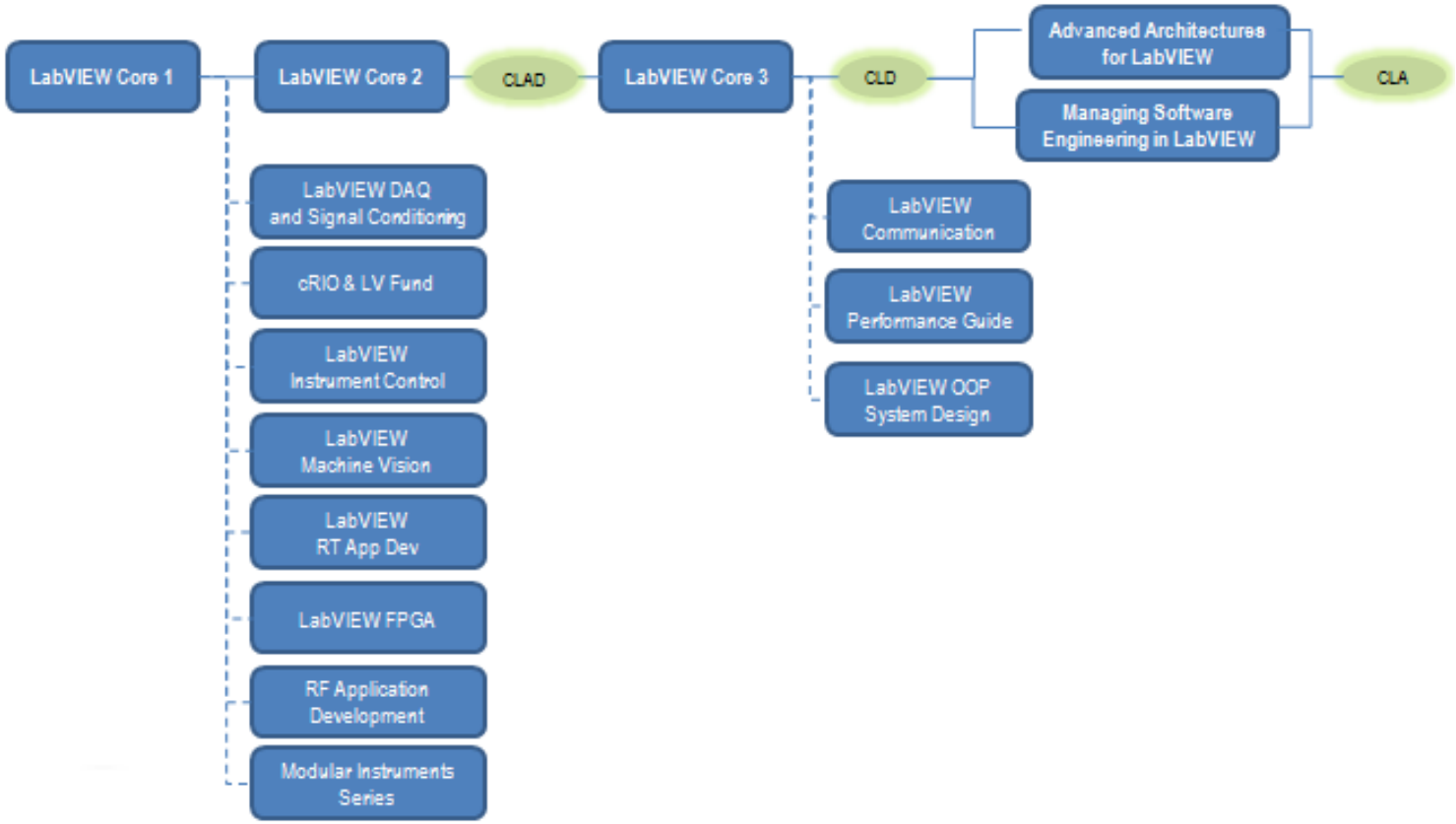
Compilation "Smart" Server



LabVIEW FPGA Development

Compilation Workers

LabVIEW Training and Certification Path



ni.com/romania/training

Training and Certification Membership Program

Flat rate training program with

- unlimited access to all scheduled courses for one or two years,
- personalized training programs,
- option to retake all courses,
- skill validation with professional credentials,
- and money-back satisfaction guarantee.

Thank you for your attention!