BCM47765

Contact Sales

Second Generation Dual-Frequency GNSS chip

Currently Viewing:

Overview

Overview

The Broadcom BCM47765 is the latest Broadcom sensor hub microcontroller with integrated GNSS. The BCM47765 includes many sensor hub and GNSS innovations. The synergistic benefits of combining multiple ICs (sensor hub and GNSS) into one IC and manufacturing in 28-nm technology include low system-level power consumption and a smaller PCB footprint with fewer BOM components than multiple-IC solutions. The BCM47765 sensor hub includes a dual-processor architecture (Arm CM4+CM0) that ensures each task is handled in the most power-efficient manner. The BCM47765 simultaneously supports GPS, GLONASS, NAVIC, BeiDou, Galileo, SBAS, and QZSS in both the L1/ B1/E1 and L5/E5a/B2a frequency bands.

This industry-first dual-band capability provides the most accurate positioning available in the market today. The BCM47765 achieves system-level performance benefits from tightly integrating the sensor and GNSS signals. Measurements from sensors such as accelerometers, gyroscopes, magnetometers, and others are fused with GNSS measurements to provide a highly accurate, cross-calibrated output to applications while helping to maintain a lower system power profile. Cross calibration is achieved by using sensor measurements to aid GNSS for small movements and by using GNSS to calibrate sensor measurements, the latter having inherent drift that accumulates over time and larger movements.

Benefits

- Highest levels of navigation performance
- Industry-leading accuracy
- Supports HDGPS (High-Definition GPS) Broadcom technology
- Highest levels of urban multipath mitigation
- New multipath scanner hardware block
- Very low GNSS and sensor hub power consumption
- Small PCB footprint (saves 50% board space over discrete sensor hub + GNSS solutions)
- Optional on-chip PVT calculations
- Robust anti-spoofing behavior through hardware RPM (Receiver Power Monitoring) for L1 and L5

Features

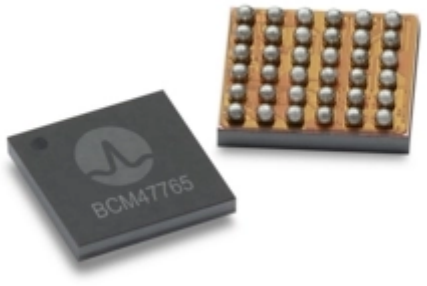
- GNSS subsystem functions and interfaces including the following:
  - A massively parallel search engine with separate tracking engines
  - Internal LNAs and adjustable gain to support external LNA operation with a noise figure better than 3.5 dB across process, voltage and temperature – Standards support for AGPS applications, including

Applications

- Smartphones
- Tablets
- Mobile accessories
- Wearables
- Digital cameras

GSM/UMTS/LTE (3GPP 44.031, 44.035, 25.331, and 36.355)
- Excellent transmit blocker performance allowing for a single filter on the BOM
- Enhanced autonomous acquisition: multiday, multi-constellation long-term orbit (LTO) data accelerates the acquisition of satellite signals.
- Synchronization pulse input enables the BCM47765 to be synchronized to an external timing reference or to provide precise GNSS time to another device
- A GNSS location library API with protocol engines for control-plane (RRLP and RRC) and user-plane (SUPL) interfaces
- Autonomous, MS-based, MS-assisted, and enhanced autonomous GNSS operation. Enhanced autonomous operation includes LTO data for the GPS, GLONASS, Galileo and BDS constellations
- Time-stamped GNSS data and a multisecond data buffer
- Supports geofencing, sensor batching, sensor fusion, and sensor navigation
- Arm-based 32-bit Cortex-M4F (CM4) CPU:
  - Single-precision Floating Point Unit (FPU)
  - Memory Protection Unit (MPU)
  - 1.125 MB internal SRAM (single-cycle access at full speed)
  - Accelerated Single Instruction Multiple Data (SIMD) and Digital Signal Processing (DSP) functions
  - 1.25 Dhrystone MIPS/MHz with an operating frequency up to 150 MHz
- Arm-based Cortex
  - M0 (CM0) operating at up to 75 MHz with 32 KB RAM to offload the CM4 and save power
- 1 MB ROM (includes the bootloader)
- High-speed system interface (to an applications processor):
  - Serial streaming SPI slave (up to 50 MHz)
  - Alternate UART system interface supports rates up to 3.2 Mb/s
- Peripheral DMA (PDMA) channels for increased peripheral communications speed
- Up to 49 programmable GPIOs
- I2S master/slave interface
- Pulse Density Microphone (PDM) input
- Interfaces to a host applications processor and to sensors:
  - SPI: Two master ports for peripherals (normal, dual, quad, up to 50 MHz) and one slave port for host communication.
  - UART: Four ports for host and peripheral communication
  - BSC: One I2C compatible port
- Integrated 12-bit, 2-channel ADC
- Timers:
  - A watchdog timer
  - A Real-time Clock (RTC) (42 bits, 32.768 kHz)
  - Two general purpose 32-bit microsecond timers
  - A 48-bit microsecond counter for better resolution timestamps than the RTC can provide
- Serial Wire Debug (SWD)
- One-Time Programmable (OTP) memory programmed in manufacturing contains the following unique information:
  - Wafer lot
  - Wafer number
  - Wafer X-Y coordinates

- Automatic Test Equipment (ATE) version number



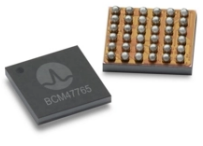
Lifecycle Status

Active

Specifications

Specification	Value
Lifecycle	Active
Distributor Inventory	No

Previously Viewed



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