
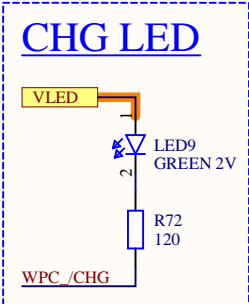
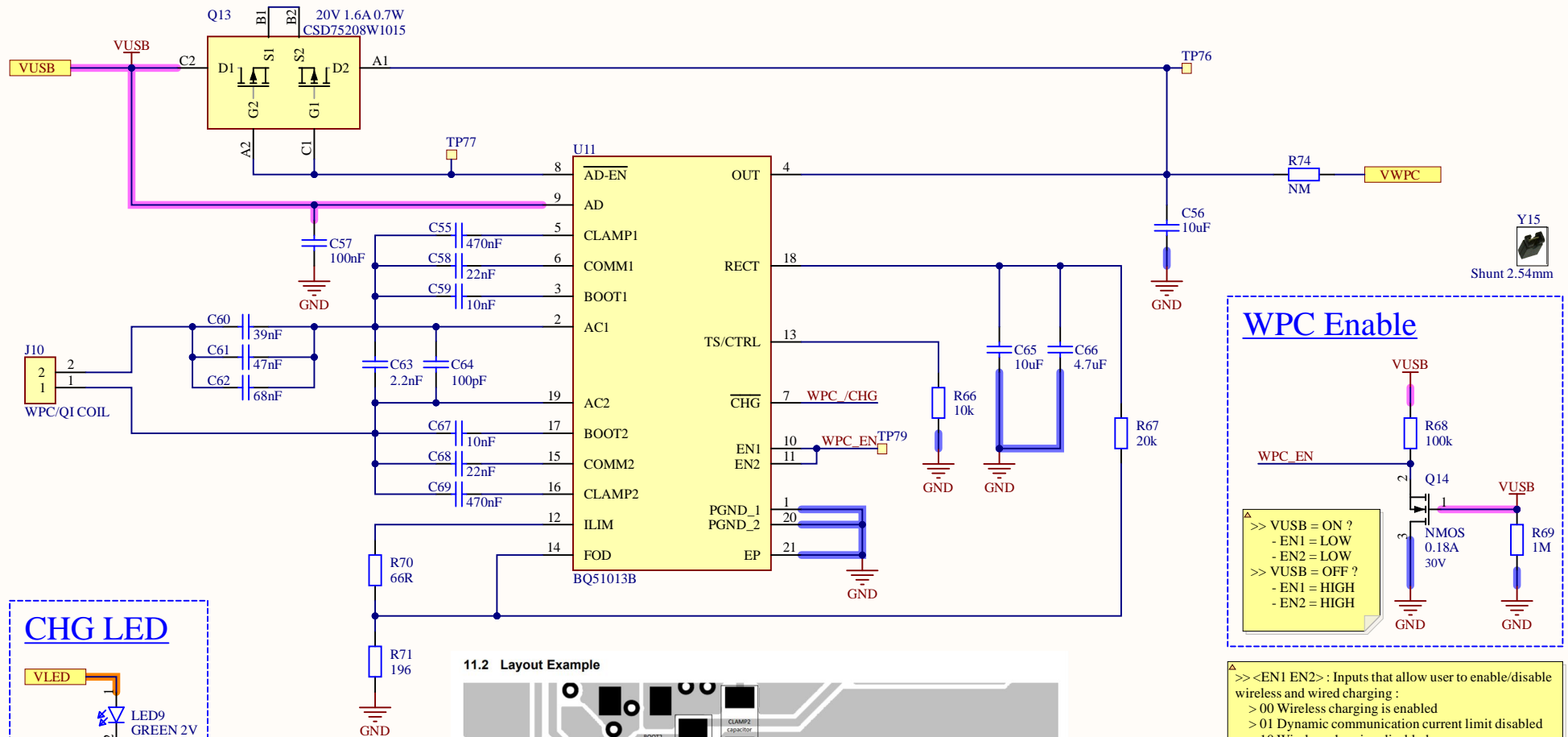


Title <i>LTEWatch</i>			MSE HES-SO HEVS	
Size: A4	Number: 1	Revision: 1.0		
Date: 09/02/2023	Time: 01:40:59	Sheet 1 of 6	<i>Tristan Traiber</i>	
File: C:\Users\Tristan_Traiber\Documents\GitHub\TM2_Hardware\Altium\Final\LTEWatch\LTEWatch.SchDoc				



$R_{ILim} = R70 + R71 = 262 \text{ Ohm}$
 $K_{ILim/I_{Max}} = 262/1 = 262 \text{ Ohm}$
 $R70 = 262 - R_{FOD} = 262 - 196 = 66 \text{ Ohm}$

11.2 Layout Example

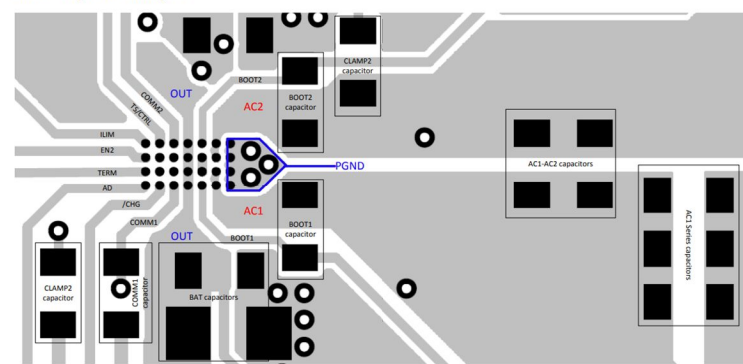
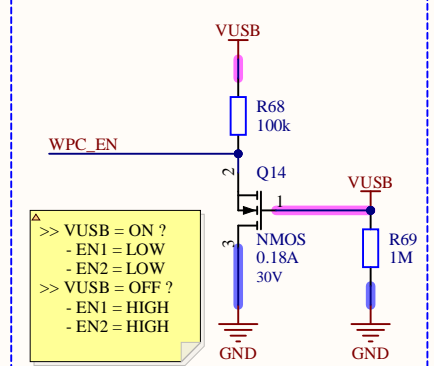


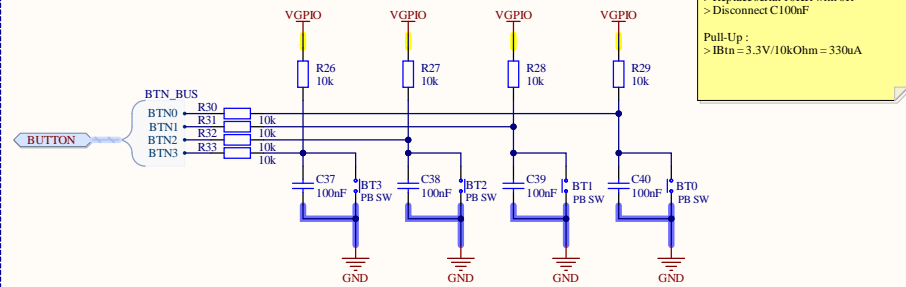
Figure 41. bq51003 Layout Schematic

WPC Enable

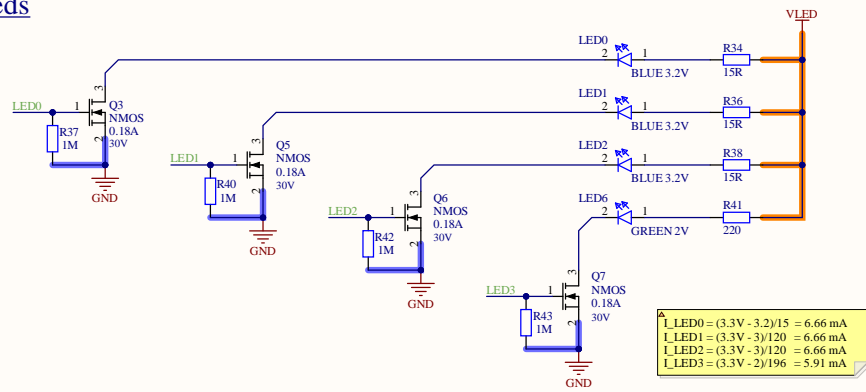


- >> <EN1 EN2> : Inputs that allow user to enable/disable wireless and wired charging :
- > 00 Wireless charging is enabled
 - > 01 Dynamic communication current limit disabled
 - > 10 Wireless charging disabled
 - > 11 Wireless charging disabled.

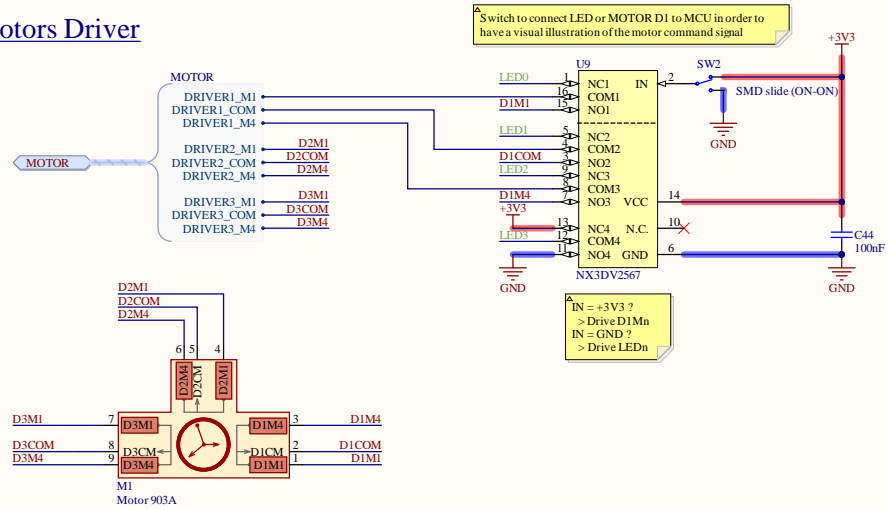
Buttons & Switches



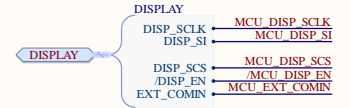
Leds



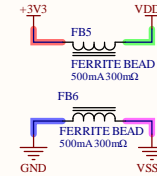
Motors Driver



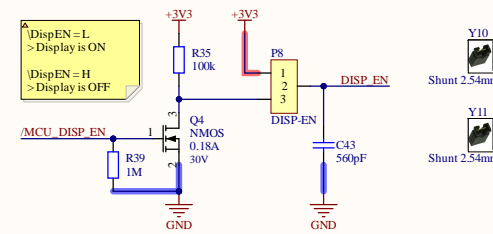
Display Interface



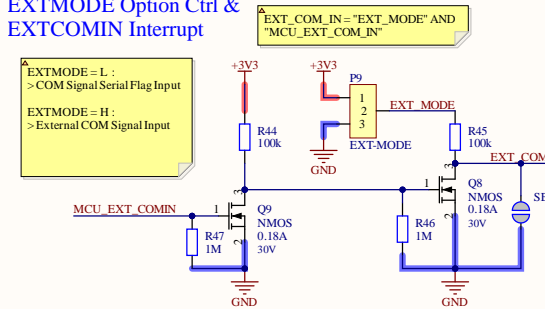
Filter Power Supply and GND



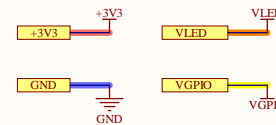
Display Enable Ctrl



EXTMODE Option Ctrl & EXTCOMIN Interrupt



Power Supply



4. Input Terminal names and function

4-1) Input Terminal

Table 4

No.	Code	I/O	Voltage	Signal name	Remark
1	SCLK	I	0/3.0 (V)	Serial clock signal	
2	SI	I	0/3.0 (V)	Serial input signal	
3	SCS	I	0/3.0 (V)	Chip select signal	
4	EXTCOMIN	I	0/3.0 (V)	COM inversion polarity input pin	
5	DISP	I	0/3.0 (V)	Display ON/OFF switching signal	4-2
6	VDDA	I	3.0(V)	Power source for Analog	
7	VDD	I	3.0(V)	Power source for Logic	
8	EXTMODE	I	0/3.0 (V)	COM inversion mode switch terminal	4-1
9	VSS	I	0(V)	Logic ground	
10	VSSA	I	0(V)	Analogue ground	

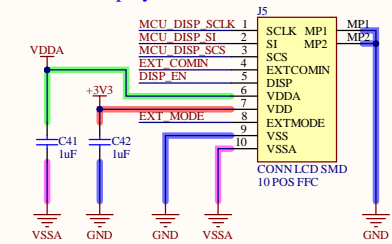
[Remark 4-1] "H"=EXTCOMIN signal enabled, "L"=Serial input flag enabled.

When "H", connect EXTMODE to VDD and when "L" to VSS.

[Remark 4-2] ON/OFF for LCD display only. Memory data is maintained.

When "H", displays with memory data, and when "L", displays all white with memory data maintained.

On Board Display Interface



Nice!View Connector

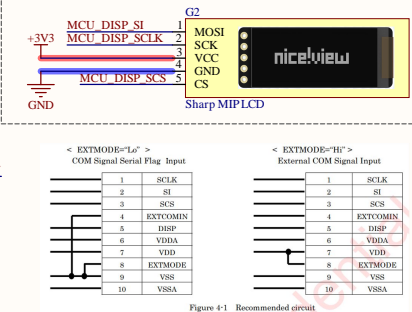
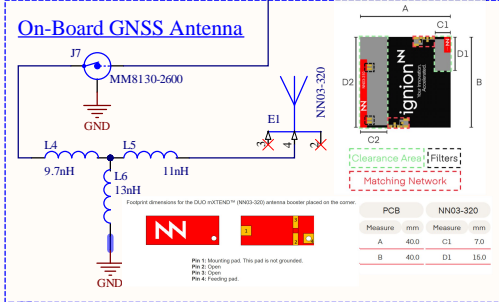
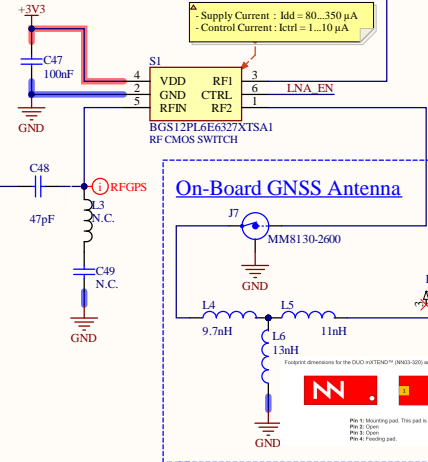
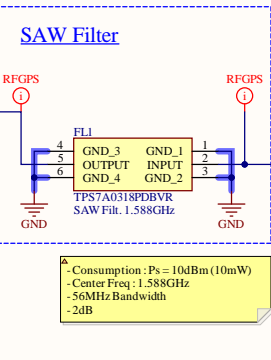
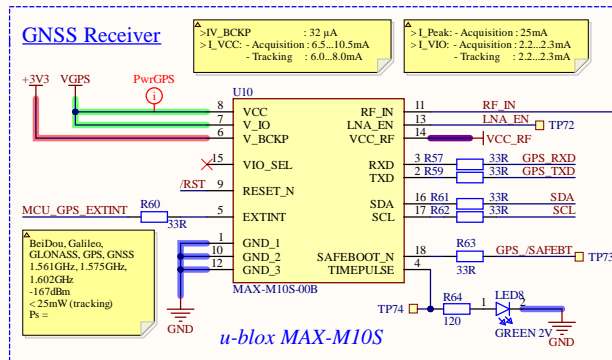
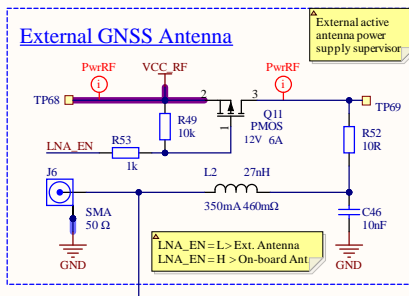
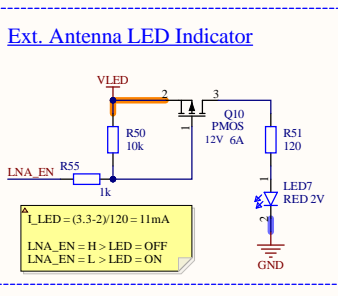
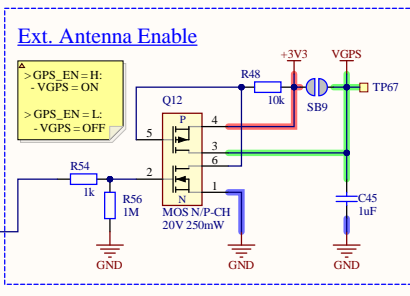
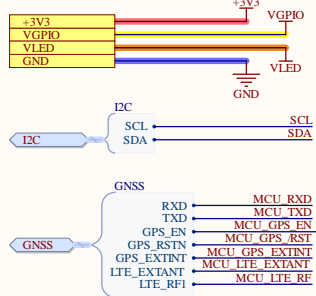


Figure 4-1 Recommended circuit



[illegible]