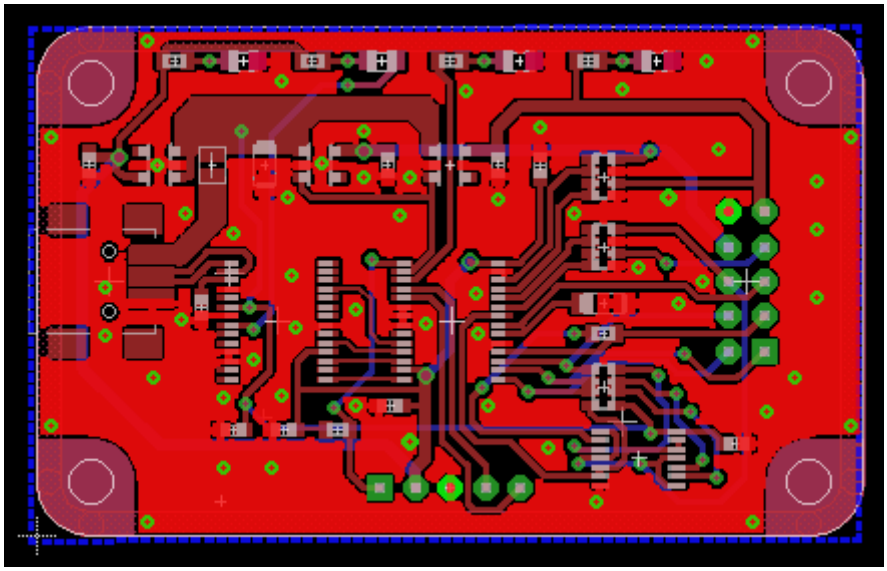
Dangerous Prototypes — Open source hardware projects

HOW-TO: Polygons and ground fills for PCBs in Eagle

DP July 18, 2012 44 Comments

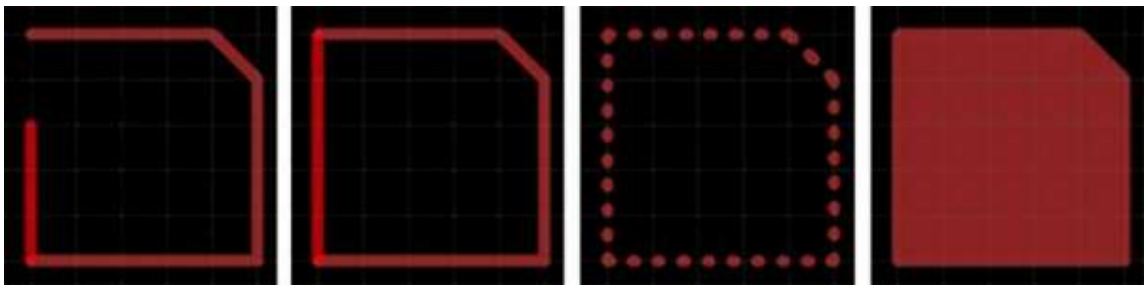


In Eagle polygons are used to make big copper areas on a PCB that aren't necessarily traces. We use them all the time to fill blank space on a PCB with copper connected to ground. Less frequently we use them to make large power traces such as with the **ATX Breakout Board**. Here's some notes on how to use and customize polygons in Cadsoft Eagle.

How to use

Open Eagle and start a new schematic and PCB. Go to the board so we can lay down a polygon.

- Click 'polygon' icon  located in the toolbar
- In the top menu bar make sure the top (red) or bottom (blue) copper layer is selected



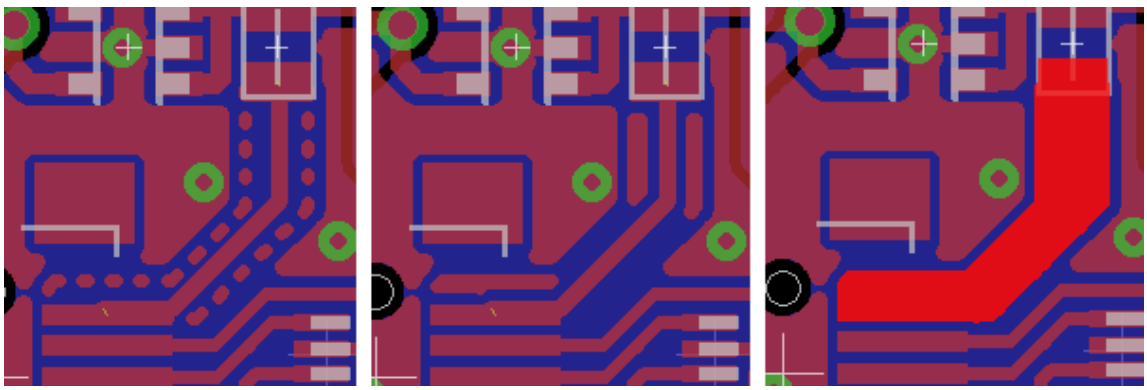
Route the polygon in the shape you want it. Make sure to close it at the starting point or you'll have problems **generating gerbers later**.

A polygon with a dashed line will appear (picture 3).

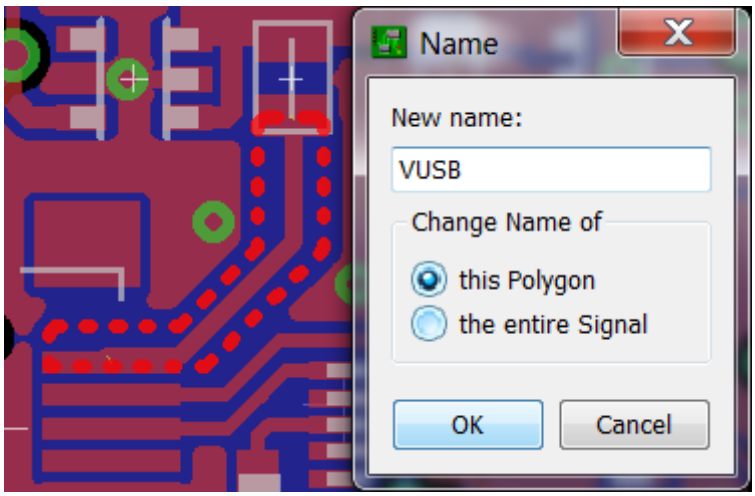
Click the 'Ratsnest' icon  , and the polygon will fill with a solid copper area.

This will now be a solid copper area on your final PCB. Next we'll look at a few ways to customize it.

Polygon Name

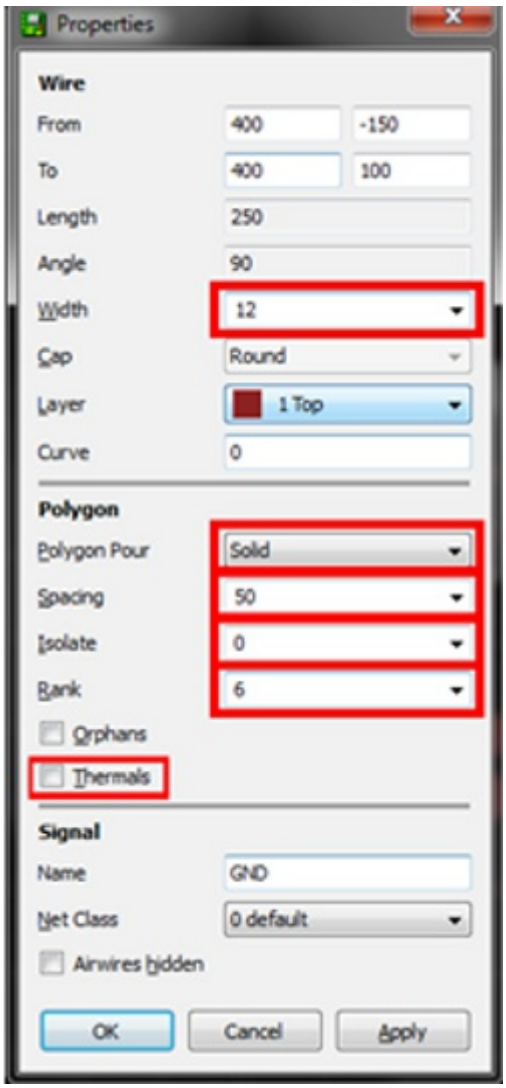


Sometimes it's useful to make the polygon part of an existing trace or electrical net. For example if you wanted to beef up a power trace.



To connect the polygon to the ‘net’ you want, right click on it’s edge, and select ‘Name’. Here make sure ‘This Polygon’ is selected, and type in the net name you want it to connect to. Hit ‘Ok’.

Polygon properties

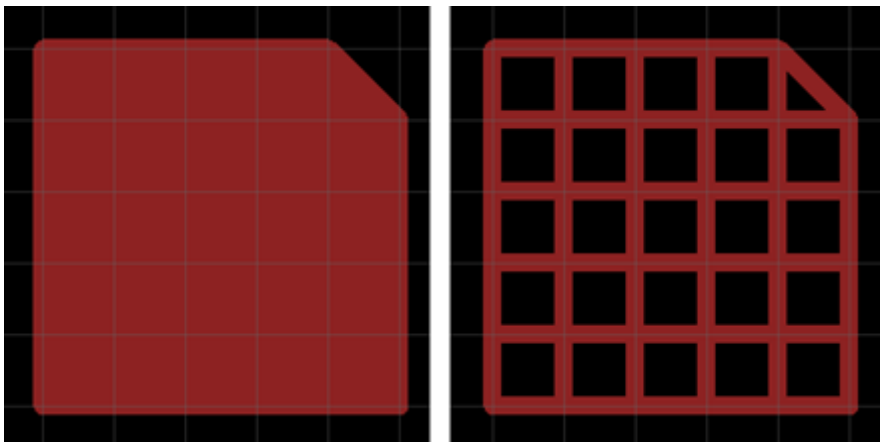


Right click on the edge of a polygon and select properties. This opens the ”Polygon properties” menu. From here you can customize the polygon.

Width

This is the width of the polygon’s perimeter when you draw it on the board. It also affects some properties below.

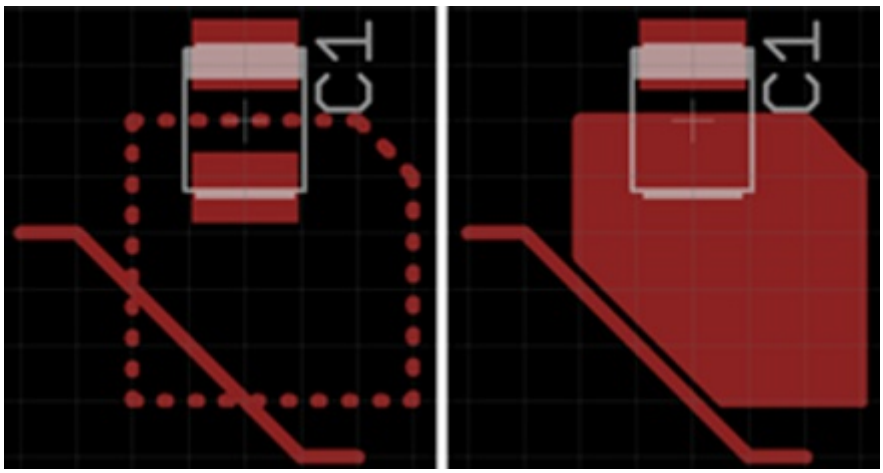
Pour



Here you can select between two versions of fill for inside the polygon, solid or hatched.

Hatched line widths are adjusted in the ”width” property. Line spacing is adjusted in the ”Mesh Distances” property. We only use the solid fill option in our projects.

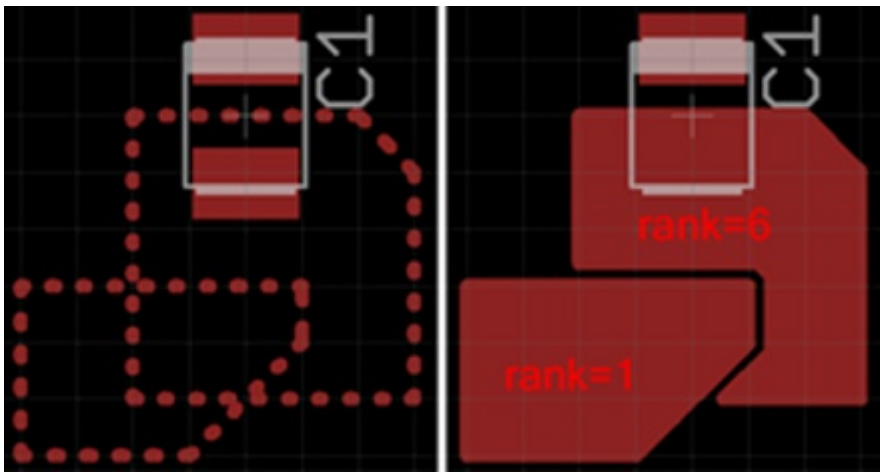
Isolate



This is the clearance between the polygon and neighboring objects, such as other traces, pins, and other polygons.

Don’t torture your board house here. Low isolation values lead to PCBs with **electrical faults from under-etching**. Leave as much room as you can.

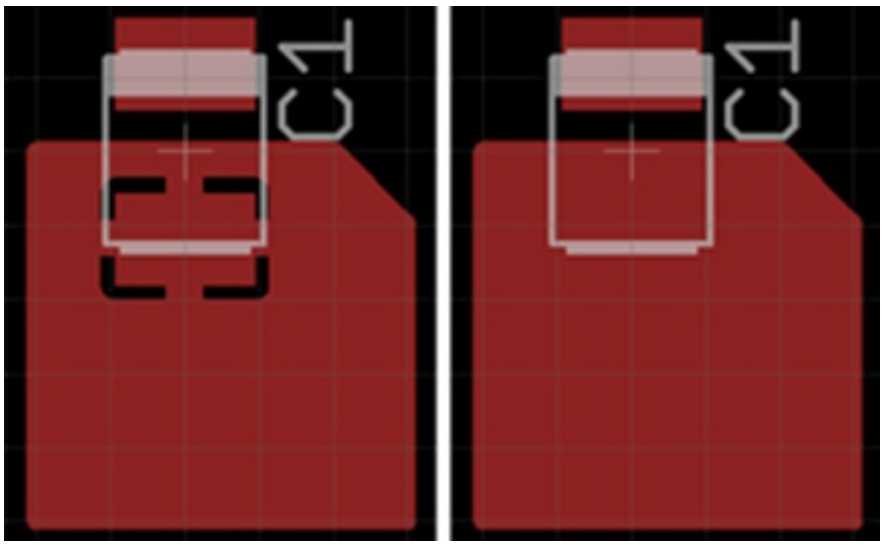
Ranks



Rank determines if one polygons if above or below an overlapping polygon.

Assigning a lower rank to one polygon will make that polygon dominate the other as seen in the pic above. When using a ground fill over the entire board it is important for it to have the highest rank so other polygons can be drawn.

Thermals



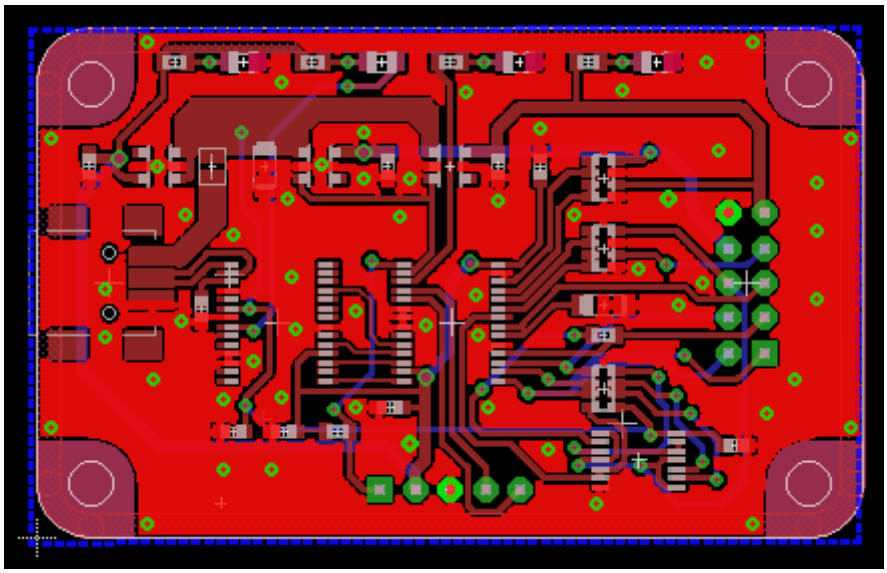
With thermals on, a pin will connect to the polygon through small traces extending from the pin center in 4 directions. Thermals make soldering easier, the part heats faster because the heat is not dissipated as quickly.

Disable thermals will make a solid pour trough the pin/pad. We usually use thermals. We only turn it off on high power traces that require more conductivity

between the pad and the polygon.

Uses

Ground planes



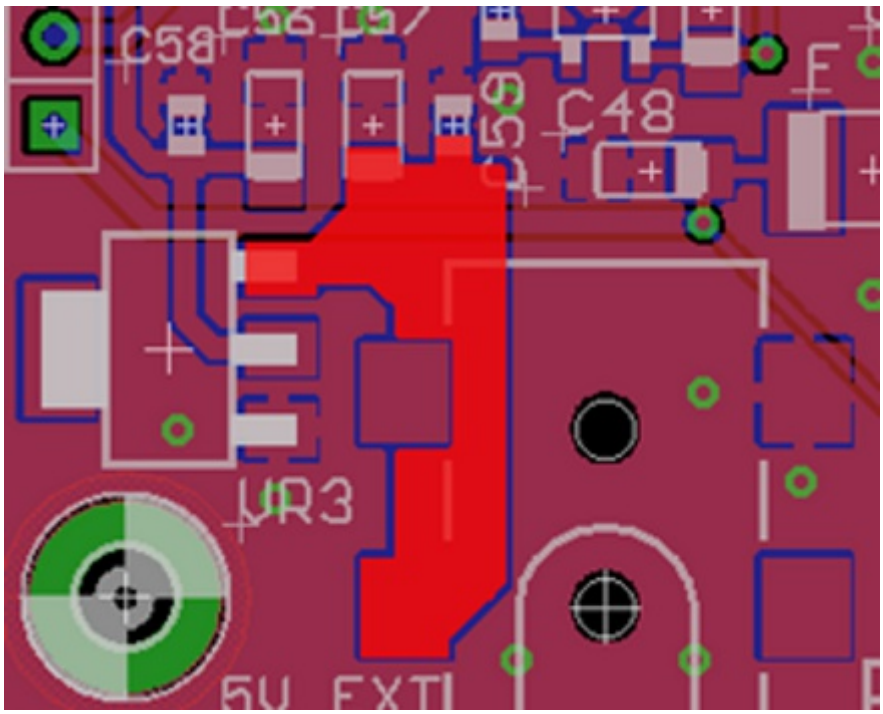
Ground planes fill-up the empty spaces of a PCB with copper connected to ground. The ground plane connects all the ground pins on a PCB automatically, which usually makes routing easier. It can also reduce electrical noise on the board.

Filling the board with a ground plane is the first thing we do when designing a PCB.

1. Draw a polygon
2. Give it the same name as the ground connections on your schematic, usually ”GND”
3. Click the ratnest button to refresh the ratnest after adding parts or traces

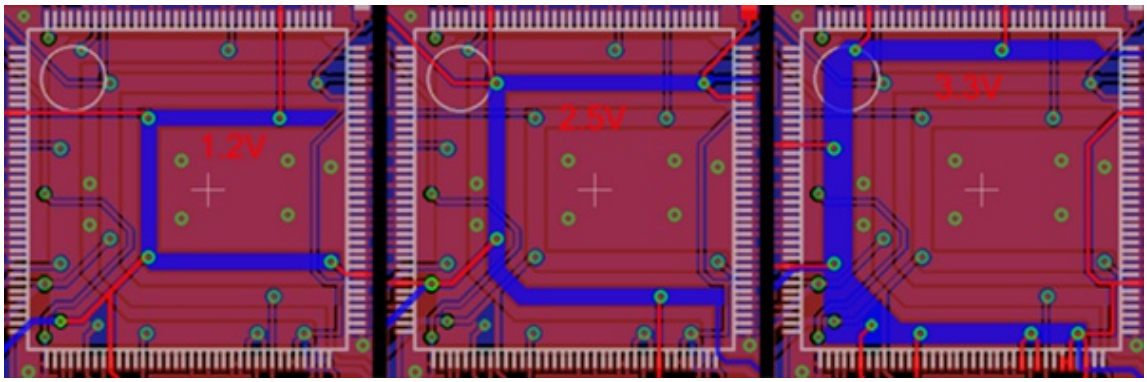
Any parts placed in the ground plane with pins names GND will automatically connect.

Power planes



Power planes are no different than ground planes, they just carry a power supply instead of ground. We use these for fat power traces where the board will carry a lot of current.

Power distribution for multiple voltage powered chip



Multiple supply polygons, good for power distribution especially on CPLD and FPGA chips.

Although a normal traces can be used here, concentric C shaped polygons provide both a power supply access, and give you more freedom with it’s shape.

Join the Conversation

44 Comments

Mats

July 18, 2012 at 5:30 pm

Is there really any difference in the number of shorts between two regular traces spaced at 8mils compared to a trace next to a ground fill with 8 mils distance? I've read it before in other texts that you should have like 14 or 16 mils isolation for ground fills even if the rest of the board is routed 7/7 or 8/8.

To me it seems a bit like an urban legend. Much like the famed "acid-traps" that apparently occurs when tracks connect/bend at 90 degrees or less angles (that would be Acute angles if I remember my math and English classes correctly).

rsdio

July 18, 2012 at 8:53 pm

I'm going to guess: Could it be that it's not shorts but signal issues instead? Perhaps placing signals very close to ground will result in some stray capacitance that affects the signal shape, so 14 or 16 mils might reduce the capacitance by 1.75 to 2 times. But I don't know how significant such tiny capacitances might be.

I have read that ground places under SMD chips can seriously create unexpected and undesired capacitance … to the point that some op-amp data sheets recommend defeating the ground plane under the SMD pads for critical or sensitive input pins. I'm not sure how much a parallel trace would have this effect as compared to parallel plates like an SMD pad over a ground plane.

Alan

July 18, 2012 at 8:39 pm

What are HATCHED polygons for?

Niklas

July 18, 2012 at 8:51 pm

Hatched polygons are often found on boards with capacitive touch buttons. The hatched pattern creates less capacitance due to smaller area.

Alan

July 18, 2012 at 9:00 pm

Thanks!

Mats

July 19, 2012 at 3:55 am

I've seen old boards that was wave-soldered (basically dipped into molten tin) that had its ground fills becoming all bubbly and wrinkled. Possibly from gasses released from the board getting trapped under the large copper area. A hatched fill would reduce this.

Probably this is not an issue with modern manufacturing techniques using FR4 laminate and reflow soldering.

And most laser printers produce a better result when doing printing a hatched area compared to a completely filled area when doing homebrew PCBs.

Niklas

July 19, 2012 at 8:42 am

The amount of copper should be balanced between the board layers to reduce warping. Perhaps not a big issue with 5×5 cm boards or hand soldered homebrew but it is for larger boards and production panels.

The term "FR4" can vary quite a lot between different manufacturers. We had a PCB supplier that used different manufacturers depending on volume and time, ie prototypes and mass production. The prototype boards were quite stiff, which was good for this 300×200 mm 4 layers board. The boards for mass production were

much softer and tended to sag about 5 mm, even at room temperature, with all the components soldered to it.

Just a guess from my side, but was it not more popular with hatched polygons in the 1990s? Almost like it was a new feature in the ECAD software that he designers wanted to show of with.

Niklas

July 18, 2012 at 8:48 pm

Try to keep all polygons as intact as possible instead of just stitching with a single via. Do a rough layout and then move traces and vias, repour and try to get connections between polygons of the same net. Sometimes it is also worth the penalty of added vias to change the routing layer for a few segments just to keep the polygons more intact.

Look at the top row of components on the featured layout. The second pair of 0603s has a via that breaks the surrounding polygon. Move that via up a bit and perhaps also the via between the 0603s and then repour. The continue to do that for the rest of the board. Long and narrow copper areas that are not connected in both ends can also come loose and cause problems.

Through hole pads can also be trimmed to be more rectangular and sometimes with the holes off center, just to increase the spacing between the pads. Then the polygon might fit in between. With 10 mils trace and space you can have pads with up to 70 mils in diameter. Make sure that the copper around the drilled hole (annular ring) is within your manufacturers capabilities.

Adrian

July 18, 2012 at 9:21 pm

ANOTHER Eagle article ?

Come on, this thing is just a teaser for the commercial version and has lots of limitations. It’s free so you’ll invest the time in learning it and won’t want to bother with something else when you hit the limits.

There are other good packages around, KiCad especially. How about some articles on that ?

Filip

July 18, 2012 at 9:28 pm

We use Eagle, so unfortunately we can't write about KiCad ourselves.. This tutorial was made to help people learning Eagle….W'll look for some KiCad articles online, and make posts about them, from time to time, but DangerousPrototypes only uses Eagle at this time, limited as it is… If and when we switch, we'll surely share any insights we learn along the way.

Unfortunately right now we don;t have the time to switch to another ECAD, as that would probably involve porting all our projects, and libraries to it, and we just don't have the time for such a massive undertaking…

Adrian

July 18, 2012 at 9:37 pm

Yes, I can understand that you wouldn't want to switch – that confirms my point !

But thank you for offering to point out the alternatives, I'm sure that's worthwhile.

rsdio

July 18, 2012 at 10:07 pm

I purchased a full, 3-seat license for Eagle and have designed several commercial products with it. Also, I know many professionals who use Eagle, some who pay and some who live with the limitations. Eagle is a very viable CAD program – it isn't perfect, but there isn't any out there that are perfect.

Nix

July 19, 2012 at 11:58 am

I've been using different CAD programs starting with Protel 99, P-Cad2008. I like Eagle mostly because it saves me a lot of time with nice parts library organization which I didn't

or still don't like in other CAD. Most projects I do in Eagle also some BGA routing etc. I noticed that all CAD programs are actually the same in base for me. I just got used to Eagle and it is easier for me to use. Sometimes I miss some features that for an eg. Altium Designer has but… everything can be done with Eagle. Matter of taste! :)

m

November 11, 2012 at 6:40 pm

I put on my chip a keep out "square" on the layer "tKeepOut" as there are exposed testing points there. I want my ground pour to go around this, is this the right way to accomplish this, or are there better alternatives? How can I check it will work, is generating a gerber the best/only way?

rsdio

November 11, 2012 at 8:35 pm

If your ground pour is on the Bottom layer, then copy your tKeepOut square and change its later to bRestrict. If your ground pour is on the Top later, then use tRestrict. The keepout deals with physical placement, while restrict controls copper generation and is useful for both traces and pours.

m

November 12, 2012 at 5:18 am

Thank you.

iulian

January 15, 2013 at 4:32 pm

How can i increase the distance between the tracks and mask determined by the polygon ?

vimark

January 15, 2013 at 6:16 pm

Hi iulian,

You can change the “Isolate” value. see Polygon properties picture above, to vary the isolation distance between mask and traces.

iulian

January 15, 2013 at 9:38 pm

thanks for the tip … but i found out want i wanted to know : i managed to enlarge the isolation gap from Drc/clearance/wire ; i changed the “wire” value and that did the trick . Thank you for your help anyway !

vimark

January 16, 2013 at 3:23 am

No problem, that DRC trick will do too.

eaglistlite

March 5, 2013 at 10:34 am

1. When polygon is created in eagle6.4.0 lite and 6.2.0 lite is created, it calculates correctly. Any layer.
2. When the same polygon is renamed into a some wire name from schematic, it does not calculate anymore at all. Any layer.
3. There is some 12mils limitation somewhere in the programe regarding width of polygone wires that cold not be found… Any layer.

How about that?

Jeremyvnc

July 26, 2013 at 3:11 pm

The width of the polygon wires are set by the trace width that you draw it with. If you draw the line and your trace width is 40mils the box will have an outline of 40 mils. I

usually use the same or smaller trace width for drawing the polygon as the isolation value that I use (usually 16 mils). The width can be changed in the polygon properties.

rsdio

July 26, 2013 at 7:32 pm

You can even set the polygon width to 0 for the most intricate shapes. However, the Design Rule Check will fail since 0 is less than whatever minimum trace width you might have specified. In those case, I either increase the polygon width or approve the DRC failures individually.

Jeremyvnc

July 26, 2013 at 3:18 pm

Here's a problem I'm seeing. I like doing hatch pours mostly because that is like my signature but also for signal capacitance. However, in EagleCAD 6.4, after I change to hatch and go back to change the spacing, anything other than the 50mil spacing now crashes Eagle. I normally do 24mil spacing (gives nice texture). Has anyone else experienced this?

Also, I noticed that there is a new pour type called "cutout." It seems to make a negative pour (ie no copper). Might be a good idea to update your article for this.

rsdio

July 26, 2013 at 7:30 pm

I'm running Eagle 5, and have never had a crash with any setting. However, I don't use hatch. The only variation I use is whether isolated copper is filled or skipped.

Jeremyvnc

August 1, 2013 at 5:57 pm

I also used 5.4 before this and never saw an issue. It is only with the recent 6.4 release that this crash has cropped up.

Sean

August 26, 2013 at 6:47 pm

I can make ground fills in Eagle using Ratsnest. Cool. How do i turn the ground fill display off please so I can continue routing?

rsdio

August 27, 2013 at 7:04 pm

That's a good question. If you autoroute, it will take precedence over the ground fill. If you are manually routing then you can just place traces over the ground fill and then run ratsnest again to have Eagle recalculate the ground fill around your traces.
If you want to completely get rid of the visual indicator of the fill, you can close the file and reopen it. You could also use the rip tool to rip up ground, but that could easily cause problems if you do it wrong.

Ahmad

October 31, 2014 at 9:36 pm

In board editor go to options
select set
toggle between the settings tab to "Misc"

uncheck ratsnet process polygon.

then whenever you click on rats net the polygon wont fill.

hope this answer ur querry..

bb

January 21, 2015 at 9:20 am

perfect thanks!

Mick M

August 27, 2013 at 9:14 pm

Hi;
" How do i turn the ground fill display off please so I can continue routing?"

What I do is grab one outer edge of the ground fill polygon and move it outside the dimension layer.

This kills the fill. (ratsnest will re-display it).
I leave it outside so that I can move it again if I "ratsnest".
You only have to move it a tiny amount.

Sometimes I want to manually do a gnd, like when 7805 TO-220 makes a big hole.
I draw fat traces over the hole, and name it "GND"
Ratsnest will show if the new GND is big enough, moving the outside lets you go back and change it.

Mick M

Staffan C
August 24, 2017 at 10:02 am

Move a side or a corner a small distance. This un-pours the polygon, however changes its shape.
Then do Z ("undo"), and you will get back the shape before the move.

Thomas
September 14, 2013 at 12:44 pm

How do i mix thermals vias with non thermal vias for groundplane interconnections?

I'm tying to have my components connected to the groundplane with thermals(ON), and i I would like to add somme via with thermals(OFF) for top and bottom layer groundplane interconnections.

But the only way i have been able to do this is by drawing a second rank small polygon around each interconnection via, witch is a lot off work.

Mark
February 23, 2014 at 10:44 pm

Hi Thomas,
Way late for a reply, but… I just found that if you go to Edit / Design Rules / Supply, then click Generate Thermals for vias, you have a lot more control over thermals for vias. Good luck!

Muhammad
December 14, 2013 at 3:47 pm

Every time i use the poylgon tool there is some copper islands and necks in between the traces, how could i remove them?

Jeremy
December 14, 2013 at 8:12 pm

In properties for the polygon, uncheck “keep orphans” that will get rid of the islands. As for the necks, you can change your clearance or add polygons in the restrict layer.

Muhammad
December 15, 2013 at 2:32 pm

I already did that and it didn’t work, i don’t know why !!!

rt
July 30, 2014 at 9:52 am

For a single sided pcb, should there be a grd copper pour for both the top layer and bottom layer?

rt
July 30, 2014 at 9:54 am

For a single sided pcb, should there be a grd copper pour for both the top and bottom layer?

nasiruddin

April 24, 2016 at 6:57 pm

sir i want to cut the gnd in pieces with ratness