3.2

a. Z=A

b. Z retains its previous value

c. Yes.

3.31 8\*8=64bytes

3.33

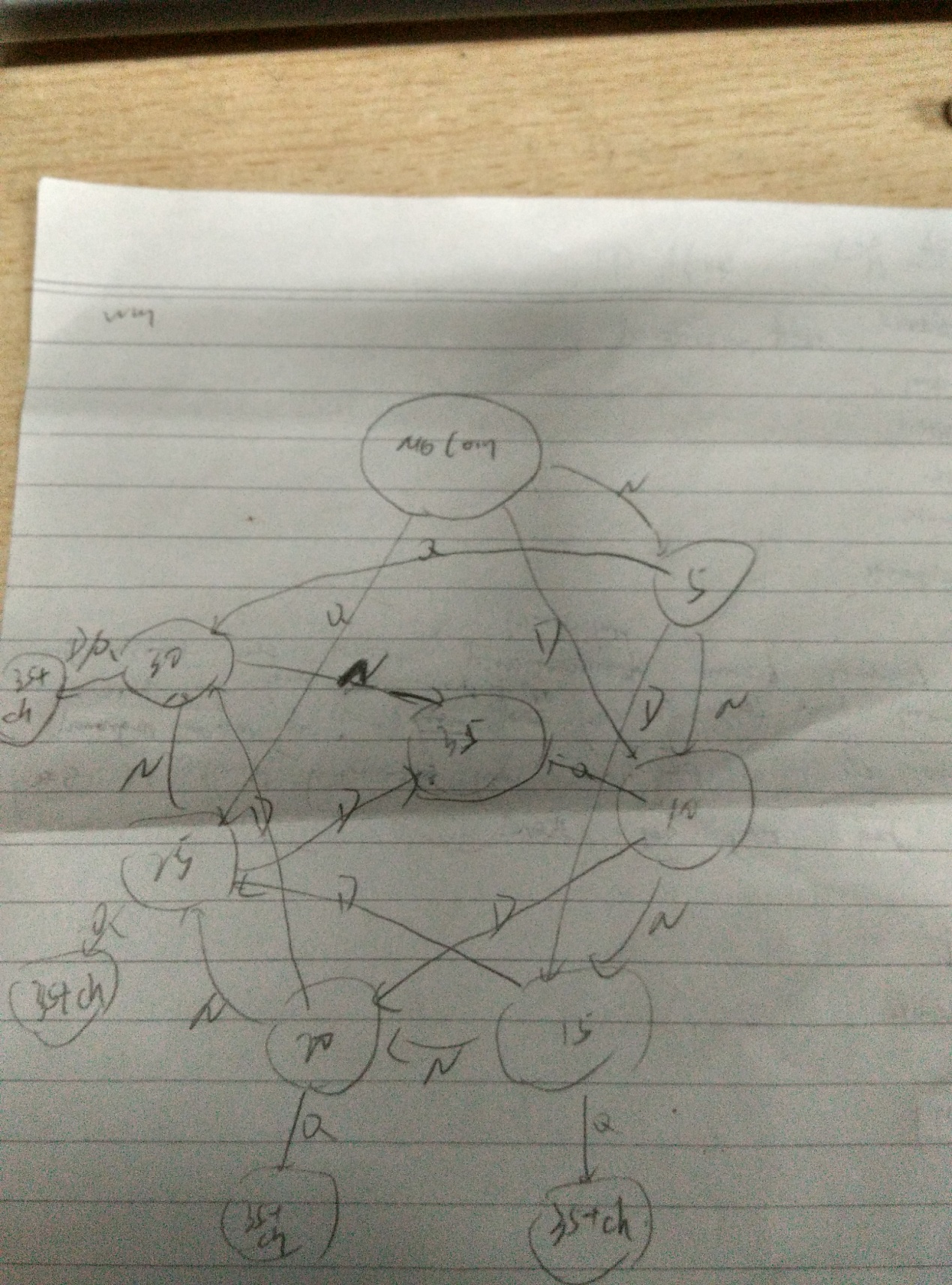
a. A[1:0]=11 WE=0

b. 6

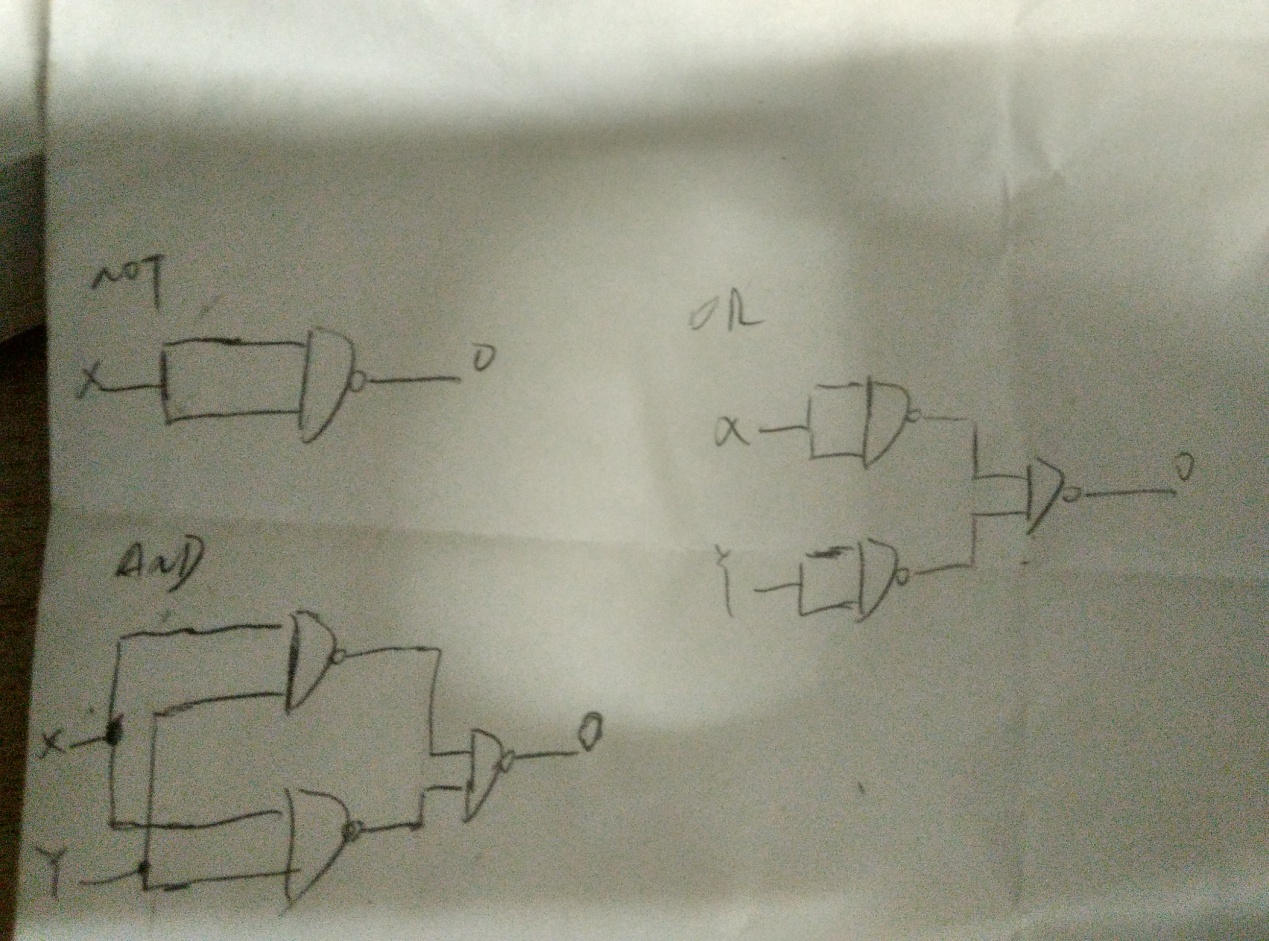
The addressability of the memory will remain unchanged.

c.2^6-60=4

3.41



3.44



5.2 The MDR is 64 bits, but the statement tells nothing about MAR.

5.7 15

5.25

(0000) 3000 0011000000000000 ( 1) .ORIG x3000

(3000) 5260 0101001001100000 ( 2) AND R1 R1 #0

(3001) 5482 0101010010000010 ( 3) AND R2 R2 R2

(3002) 0201 0000001000000001 ( 4) BRP po

(3003) 0E02 0000111000000010 ( 5) BRNZP sec

(3004) 56C3 0101011011000011 ( 6) po AND R3 R3 R3

(3005) 0C0A 0000110000001010 ( 7) BRNZ outp1

(3006) 5482 0101010010000010 ( 8) sec AND R2 R2 R2

(3007) 0801 0000100000000001 ( 9) BRN na

(3008) 0E02 0000111000000010 ( 10) BRNZP tri

(3009) 56C3 0101011011000011 ( 11) na AND R3 R3 R3

(300A) 0607 0000011000000111 ( 12) BRZP outp2

(300B) 98FF 1001100011111111 ( 13) tri NOT R4 R3

(300C) 1921 0001100100100001 ( 14) ADD R4 R4 #1

(300D) 1A84 0001101010000100 ( 15) ADD R5 R2 R4

(300E) 0803 0000100000000011 ( 16) BRN outp2

(300F) 0200 0000001000000000 ( 17) BRP outp1

(3010) 1242 0001001001000010 ( 18) outp1 ADD R1 R1 R2

(3011) 0E02 0000111000000010 ( 19) BRNZP stop

(3012) 1243 0001001001000011 ( 20) outp2 ADD R1 R1 R3

(3013) 0E00 0000111000000000 ( 21) BRNZP stop

(3014) F025 1111000000100101 ( 22) stop TRAP x25

5.33 R5 has exactly 5 “ones” of the lower 8 bits.

5.34 The Register file and the ALU in figure 5.18 implement the NOT instruction, alongwith NZP and the logic which goes with it.

5.40 The signal A indicates whether the instruction in IR is a BR instruction.