

# TRAN DUC ANH

## DIGITAL IC DESIGN

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### CAREER OBJECTIVE

A motivated **RTL Design & SoC Engineer** with hands-on experience in digital hardware design using **Verilog/SystemVerilog, FPGA** development, and **ASIC design** fundamentals. Seeking an internship opportunity in Ho Chi Minh City to apply strong knowledge in RTL design, SoC architecture, and familiar with memory access optimization, hardware-based **memory acceleration** techniques and basic **DSP**

### EDUCATION

#### HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY - VNU-HCMUT

2023 - 2027

##### Computer Engineering (CE)

2023 – Present (3rd-year student)

Expected Graduation Date: 06/2027

GPA: 3.5/4.0 (8.3/10)

### SKILLS

SKILLS	Analyze problems logically, identify root causes, and propose effective solutions, while effectively tutoring and mentoring others to understand complex concepts
TOOLS	Vivado, Vitis HLS, Vitis Embedded, STM32 CubeIDE, Altium Design, Proteus, MATLAB, PSpice, Visual Studio Code, Petalinux, OpenLane, Klayout
PROGRAMMING LANGUAGE/HDL	Verilog/SystemVerilog, C, C++, Assembly, TCL scripts

### PROJECTS

#### RTL-to-GDSII Flow & RISC-V System Integration on Linux ([https://github.com/tranducanh-ut/RISCV\\_SINGLE\\_CYCLE](https://github.com/tranducanh-ut/RISCV_SINGLE_CYCLE))

- Designed and integrated AXI4-Lite interface for memory-mapped control between RISC-V CPU and custom IP
- Implemented RTL-to-GDSII ASIC flow using OpenLane and SkyWater 130nm PDK and display the layout by Klayout
- Configured and customized Petalinux for RISC-V(RV32I)-based system that can use ARM CPU to control IP blocks
- Generated BOOT image, device tree, and Linux kernel for embedded system

#### True Random Number Generator (TRNG) Design ([https://github.com/tranducanh-ut/TRNG\\_RISC\\_V\\_pico](https://github.com/tranducanh-ut/TRNG_RISC_V_pico))

- Designed true random number generator using flip-flop metastability with 3 members
- An open-source RISC-V RV32IM core was used and configured in combination with a TRNG module.
- Built FPGA system in Vivado and software in Vitis Embedded to transfer data from Arty z7 to STM32
- A custom-designed UART was integrated to facilitate data transmission to PuTTY for the other two team members.

### CERTIFICATES AND AWARDS

IELTS Academic (6.0)

Altium Designer - PCB schematic & layout design

Microsoft Office Specialist: Excel and Powerpoint

Academic Encouragement Scholarship – Level 3 & OISP Scholarship (three times)

Study Buddy Program – Academic Tutor

