SCB68155
Interrupt Handler

Preliminary Specification

Microprocessor Products

DESCRIPTION

The Signetics SCB68155/8X824 is an asynchronous interrupt handler for VMEbus and VERSAbus™ systems. Up to 14 interrupts are prioritized by the SCB68155/8X824 to one of seven levels and are output on the interrupt priority level lines ($\overline{IPL0}$ – $\overline{IPL2}$). The SCB68155/8X824 prioritizes the interrupts in the following manner: local bus requests over system bus requests with the non-maskable interrupt ($\overline{NMI}$) considered the highest priority local interrupt ($\overline{NMI}$ over $\overline{IRQ7}$, then $\overline{LRQ6}$ – $\overline{LRQ1}$ over $\overline{IRQ6}$ – $\overline{IRQ1}$).

The local interrupt requests can be programmed to be either active high or low, and either edge or level sensitive. The system bus interrupt requests are always active low and level sensitive. The non-maskable interrupt is always negative edge triggered.

During a local interrupt acknowledge sequence, two modes of response are available: vectored mode or device-supplies-the vector mode.

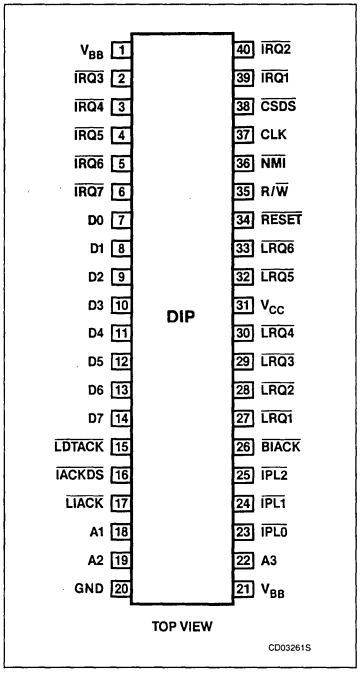
For system bus responses, the SCB68155/8X824 works with a bus requester (for example, the Signetics SCB68175/8X821 Bus Master or SCB68172 VMEbus Controller), to acquire a status/ID byte (interrupt vector) from the system.

The SCB68155/8X824 was designed primarily for interface to the VMEbus. For more information regarding the protocol definitions, proper use, and application of this device, refer to the VMEbus Specification Manual.

FEATURES

- **Asynchronous interrupt handler for VMEbus and VERSAbus systems**
- **Receives and prioritizes non-maskable, six local and seven system bus interrupts**
- **Interrupts may be polled in lieu of real time operation**
- **Programmable local interrupt response**
- **Works with the SCB68175/8X821 to acquire status/ID byte (vector) during bus interrupt acknowledge**
- **Complete device status, including last interrupt acknowledged**
- **High speed bipolar technology**

PIN CONFIGURATION



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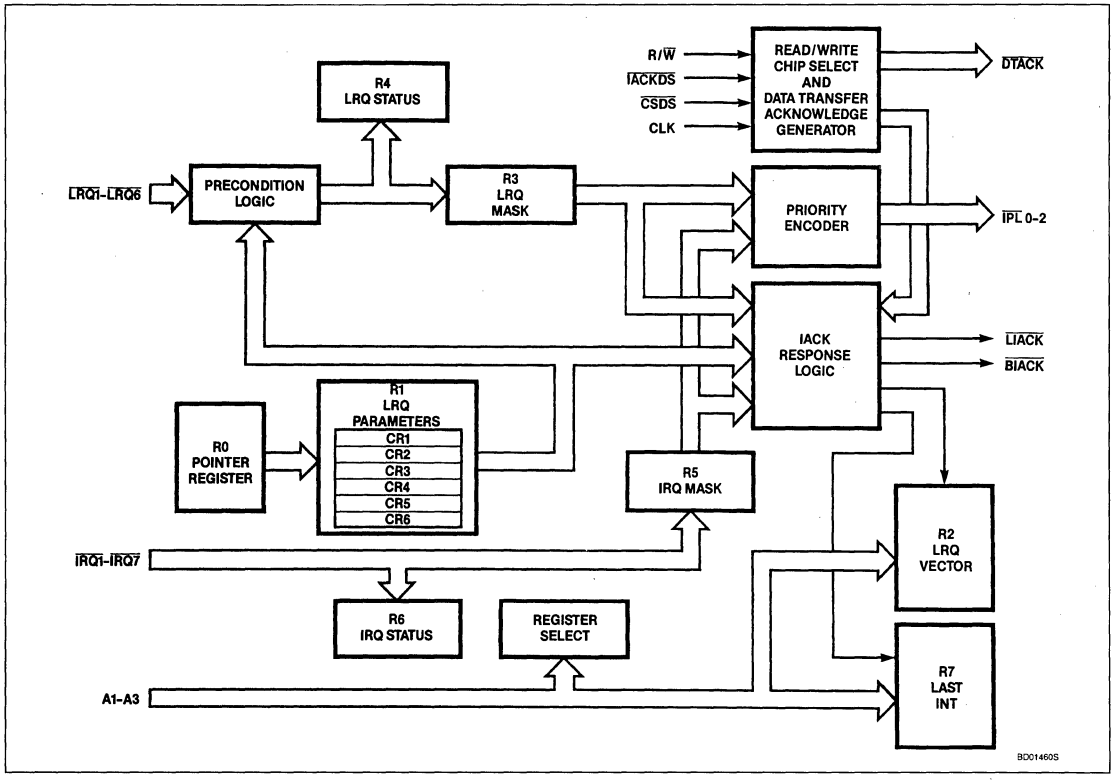
Interrupt Handler | SCB68155

ORDERING CODE

PACKAGES	V_{CC} = 5V ± 5%, T_A = 0°C to 70°C
Ceramic DIP	SCB68155CAI40
Plastic DIP	SCB68155CAN40

BLOCK DIAGRAM



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PIN DESCRIPTION

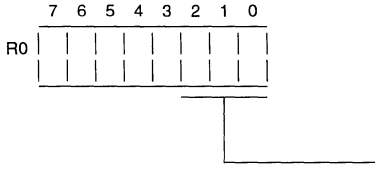
MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
V_{BB}	1, 21	I	**Supply Voltage:** Supply voltage for internal gates.
$\overline{IRQ1}$ – $\overline{IRQ7}$	39, 40, 2 – 6	I	**Bus Interrupt Request:** Active low inputs for bus generated interrupts.
D0 – D7	7 – 14	I/O	**Bus Data:** Three state local data bus.
$\overline{LDTACK}$	15	O	**Local Data Transfer Acknowledge:** Active low, open collector output. Indicates that valid data is available on the local data bus during interrupt acknowledge cycle or data transfer cycle.
$\overline{IACKDS}$	16	I	**Interrupt Acknowledge:** Active low interrupt acknowledge input from the local master. This signal must be qualified by the local master's data strobe prior to input.
$\overline{LIACK}$	17	O	**Local Interrupt Acknowledge:** Active low interrupt acknowledge totem pole output to the local interrupting devices.
A1 – A3	18, 19, 22	I	**Address Lines:** Address inputs from local master.
GND	20	I	**Ground**
$\overline{IPL0}$ – $\overline{IPL2}$	23 – 25	O	**Interrupt Priority Level:** Active low totem pole outputs to the local master. The priority level of the interrupt request is encoded on these outputs.
$\overline{BIACK}$	26	O	**Bus Interrupt Acknowledge:** Active low interrupt acknowledge totem pole output to the system bus.
$\overline{LRQ1}$ – $\overline{LRQ6}$	27 – 30, 32, 33	I	**Local Interrupt Request:** User can define the active state of these inputs.
V_{CC}	31	I	**Supply Voltage:** +5V power supply.
$\overline{RESET}$	34	I	**Reset:** Active low input reset.
R/$\overline{W}$	35	I	**Read/Write:** This signal specifies the data transfer cycle to be either read or write.
$\overline{NMI}$	36	I	**Non – Maskable Interrupt:** Active low highest priority interrupt.
CLK	37	I	**Clock:** Clock input (typically CPU clock).
$\overline{CSDS}$	38	I	**Chip Select:** Active low chip select input for register I/O. This input must be qualified by the local master's data strobe prior to input.

REGISTERS

The SCB68155/8X824 contains eight internal registers (R0 – R7) accessible to the local master. There are also six sub-registers contained in register R1. Register R0 specifies which sub-register is to be accessed in R1. Register R2 stores the interrupt vector for vectored mode responses. Register R3 and R5 are the interrupt mask registers for the local and system bus interrupts respectively. Registers R4 and R6 are the status registers for local and bus interrupts respectively, allowing all interrupts to be polled. Register R7 can be read by the local master to determine the last interrupt acknowledged.

All data transfers between the SCB68155/8X824 and the local master are done using the local data bus (D0 – D7), address bus (A1 – A3), a chip select ($\overline{CSDS}$) and a read/write (R/$\overline{W}$) input.

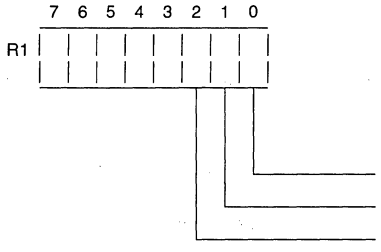
Register R0 – A3A2A1 = 000



Pointer register (write only).
Bit 0 – 2 of R0 specify which control sub-register CR1 – CR6 during an access of R1. During register I/O, bits 7 – 3 will read as 0.

B2 – B1 – B0	
000 – none	100 – CR4
001 – CR1	101 – CR5
010 – CR2	110 – CR6
011 – CR3	111 none

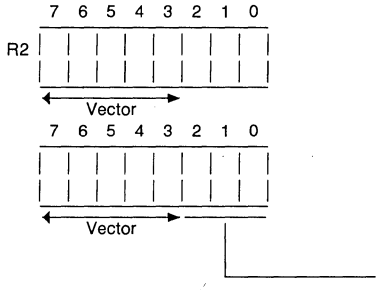
Register R1 – A3A2A1 = 001



Control registers CR1 – CR6 (read or write).
These six registers program the function of the local interrupt requests ($\overline{LRQ1}$ – $\overline{LRQ6}$). (CR1 programs $\overline{LRQ1}$, CR2 programs $\overline{LRQ2}$, etc). During register I/O, bits 7 – 3 will be read as 0.

$\overline{LRQn}$ active state (high/low)	(1 = active high)
$\overline{LRQn}$ edge/level sensitive	(1 = edge sensitive)
$\overline{LRQn}$ vector enable	(1 = enabled)

Register R2 – A3A2A1 = 010

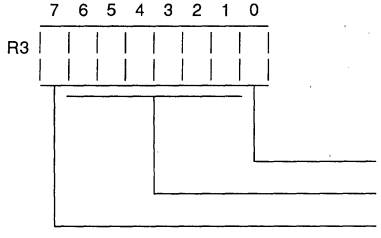


LRQ vector (read or write).
Bits 7 – 3 of this register are the top five bits of the local interrupt vector. During register I/O, bits 2 – 0 will be read as zeros.

LRQ vector output during local interrupt acknowledge (If vector enable = 1).

	100 – $\overline{LRQ4}$
001 – $\overline{LRQ1}$	101 – $\overline{LRQ5}$
010 – $\overline{LRQ2}$	110 – $\overline{LRQ6}$
011 – $\overline{LRQ3}$	111 – $\overline{NMI}$

Register R3 – A3A2A1 = 011

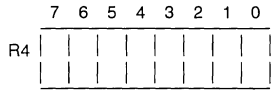


LRQ mask (read or write).
This register allows the user to mask local interrupts. It also enables vectored response for $\overline{NMI}$.

$\overline{NMI}$ Vector enable	(1 = active high)
$\overline{LRQ}$ 1 – 6 mask	(1 = interrupt enabled)
$\overline{NMI}$ mask	(1 = $\overline{NMI}$ enabled)

Bit 1 = $\overline{LRQ1}$	Bit 5 = $\overline{LRQ5}$
Bit 2 = $\overline{LRQ2}$	Bit 6 = $\overline{LRQ6}$
Bit 3 = $\overline{LRQ3}$	Bit 7 = $\overline{NMI}$

Register R4 – A3A2A1 = 100

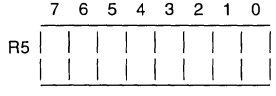


LRQ mask (read only).
Local interrupts can be polled through this register. During register I/O, bit 0 will be read as a 0.

Bit 1 = $\overline{LRQ1}$
Bit 2 = $\overline{LRQ2}$
Bit 3 = $\overline{LRQ3}$
Bit 4 = $\overline{LRQ4}$
Bit 5 = $\overline{LRQ5}$
Bit 6 = $\overline{LRQ6}$
Bit 7 = $\overline{NMI}$

$\overline{LRQ}$ status (1 = interrupt pending)
$\overline{NMI}$ status (1 = interrupt pending)

Register R5 – A3A2A1 = 101

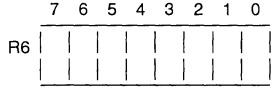


IRQ mask (read or write).
This register allows the user to mask system bus interrupts. During register I/O, bit 0 will be read as a 0.

Bit 1 = $\overline{IRQ1}$
Bit 2 = $\overline{IRQ2}$
Bit 3 = $\overline{IRQ3}$
Bit 4 = $\overline{IRQ4}$
Bit 5 = $\overline{IRQ5}$
Bit 6 = $\overline{IRQ6}$
Bit 7 = $\overline{IRQ7}$

(1 = interrupt enabled)

Register R6 – A3A2A1 = 110

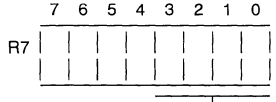


IRQ status (read only).
System bus interrupts can be polled through this register. During register I/O, bit 0 will be read as 0.

Bit 1 = $\overline{IRQ1}$
Bit 2 = $\overline{IRQ2}$
Bit 3 = $\overline{IRQ3}$
Bit 5 = $\overline{IRQ5}$
Bit 6 = $\overline{IRQ6}$
Bit 7 = $\overline{IRQ7}$

$\overline{IRQ}$ status (1 = interrupt pending)

Register R7 – A3A2A1 = 111



Last interrupt acknowledged (read only).
This register can be read by the local CPU to determine the last interrupt acknowledged. During register I/O, bits 7 – 4 will be read as 0.

0000 – none
0001 – $\overline{IRQ1}$
0010 – $\overline{IRQ2}$
0011 – $\overline{IRQ3}$
0100 – $\overline{IRQ4}$
0101 – $\overline{IRQ5}$
0110 – $\overline{IRQ6}$
0111 – $\overline{IRQ7}$
1000 – none
1001 – $\overline{LRQ1}$
1010 – $\overline{LRQ2}$
1011 – $\overline{LRQ3}$
1100 – $\overline{LRQ4}$
1101 – $\overline{LRQ5}$
1110 – $\overline{LRQ6}$
1111 – $\overline{NMI}$

FUNCTIONAL OPERATION

Typical Configuration

The SCB68155/8X824 can handle interrupts from 14 sources: seven bus interrupt requests generated on the $\overline{IRQ1}$ – $\overline{IRQ7}$ inputs, six local interrupt sources generated on the $\overline{LRQ1}$ – $\overline{LRQ2}$ inputs, and one non-maskable interrupt which may originate locally or from the system (such as the system's AC fail signal). All interrupts are encoded to one of seven levels and output on the $\overline{IPL0}$ – $\overline{IPL2}$ lines. Table 1 shows how the SCB68155/8X824 encodes the interrupts.

$\overline{BIACK}$ is the bus interrupt acknowledge signal which is asserted during a bus interrupt acknowledge sequence. $\overline{BIACK}$ can be used to get the associated bus requester (for example, the Signetics SCB68175/8X821 or SCB68172), to acquire an interrupt vector from the system bus. Figure 1 shows a typical SCB68155/8X824-SCB68175/8X821 system configuration.

$\overline{LIACK}$ is the local interrupt acknowledge signal which is asserted during a local interrupt acknowledge sequence. Figure 2 shows a typical configuration for the SCB68155/8X824.

Non-Maskable Interrupt (NMI)

The highest priority interrupt request is the non-maskable interrupt ($\overline{NMI}$). It is an active low, negative edge-triggered interrupt. $\overline{NMI}$ is considered by the SCB68155/8X824 to be the highest priority local interrupt, however, the user is not restricted to having it represent a local device. When the local master responds to an $\overline{NMI}$, bit 7 in the LRQ status register R4 is cleared to 0.

Both vectored and device-supplies-the-vector modes are available with $\overline{NMI}$. However, it is recommended that the SCB68155/8X824's response to an $\overline{NMI}$ be a vectored mode interrupt acknowledge.

Local Interrupts

The SCB68155/8X824 can handle interrupts generated by local devices through its six local interrupt request lines ($\overline{LRQ1}$ – $\overline{LRQ6}$). The local interrupt requests are prioritized with $\overline{LRQ6}$ being the highest priority, and $\overline{LRQ1}$ the lowest priority.

The response of the SCB68155/8X824 to an acknowledge of a local interrupt can be selected by means of the SCB68155/8X824's R1 register. Pointer register R0 points to one of the six control sub-registers when accessing register R1. The six control registers (CR1 – CR6) in register R1 define the functions of the six local interrupt requests ($\overline{LRQ1}$ – $\overline{LRQ6}$).

Control Register 'n' Bit 0
Selects local interrupt requests 'n' ($\overline{LRQn}$), to be either low or high. Bit 0 = 1 defines active state to be high.

Control Register 'n' Bit 1
Selects local interrupt request 'n', to be either edge or level sensitive. Bit 1 = 1 defines LRQ1 to be edge sensitive. Two modes of operation for a local interrupt response are possible; vectored mode and device-supplies-the-vector mode. In vectored mode, the SCB68155/8X824 supplies the interrupt vector to the local CPU and asserts $\overline{LDTACK}$ to complete the transfer. In the device-supplies-the-vector mode, the local interrupting device supplies its own interrupt vector and asserts $\overline{LDTACK}$ to complete the transfer.

Control Register 'n' Bit 2
Selects either vectored mode or device-supplies-the-vector mode response. Bit 2 = 1 enables vectored mode operation for $\overline{LRQn}$. The vector register R2 allows the user to program the five most significant bits (bits 7 – 3) of the interrupt vector supplied in vectored mode. During a vectored local interrupt acknowledge cycle, the upper five bits of the vector register are concatenated with a 3-bit interrupt level (address lines A3 = B2 of the vector, A2 = B1 and A1 = B0). This forms the unique vector for the local interrupt request level being acknowledged.

The local interrupt request mask register R3 allows the user to selectively enable local interrupt requests by setting appropriate bits in the register.

The current state of the local interrupt requests can be determined by the local master by reading the local interrupt status register R4.

Local Interrupt Acknowledge

An interrupt acknowledge, by the local CPU, is signified by the assertion of the interrupt acknowledge input ($\overline{IACKDS}$). The SCB68155/8X824 responds by reading the three address lines (A1 – A3) to determine what level is being acknowledged. If a local interrupt is the highest priority interrupt pending on the level acknowledged, the SCB68155/8X824 will respond as though it is programmed for that level.

If vectored mode is programmed, the SCB68155/8X824 will assert the local interrupt acknowledge ($\overline{LIACK}$) and place the interrupt vector on the local data bus. To complete the transfer of the vector to the local CPU, the SCB68155/8X824 asserts the local data transfer acknowledge signal ($\overline{LDTACK}$).

If device-supplies-the-vector mode is programmed, the SCB68155/8X824 asserts the local interrupt acknowledge signal ($\overline{LIACK}$). The interrupting device is then allowed to place its own vector on the local data bus and assert $\overline{LDTACK}$.

When a local interrupt is acknowledged by the local master, the appropriate bit in the LRQ status register R4 is cleared to 0.

Bus Interrupts

The VMEbus specification defines a maximum of seven interrupt levels. The SCB68155/8X824 can handle seven system bus interrupts through its $\overline{IRQ1}$ – $\overline{IRQ7}$ lines. Bus interrupt request are active low level sensitive, and prioritized with $\overline{IRQ7}$ being the highest priority and $\overline{IRQ1}$ the lowest priority. The bus mask control register R5 allows the user to selectively enable bus interrupt requests by setting appropriate bits in the register. The local CPU can read the bus interrupt status register R6 to determine the current state of the bus interrupt requests.

Bus Interrupt Acknowledge

The local CPU asserts the interrupt acknowledge signal ($\overline{IACKDS}$) to signify an interrupt acknowledge. The SCB68155/8X824 responds by reading the interrupt level on A1 – A3 to determine what level is being acknowledged. If a local interrupt is not pending on the level acknowledged, and that bus level is not masked, the SCB68155/8X824 will assert bus interrupt acknowledge ($\overline{BIACK}$). If that bus level is masked, the SCB68155/8X824 will not respond to the interrupt acknowledge by the local master.

Part of the interrupt acknowledge sequence for a bus interrupt consists of acquiring a vector (status/ID byte) from the system bus. The bus signals required to acquire this vector are available with a bus controller. The

Table 1. SCB68155/8X824 Interrupt Level Encoding

INTERRUPT REQUEST LEVEL	INTERRUPT PRIORITY LEVEL OUTPUTS		
	$\overline{IPL2}$	$\overline{IPL1}$	$\overline{IPL0}$
$\overline{NMI}$, $\overline{IRQ7}$	0	0	0
$\overline{LRQ6}$, $\overline{IRQ6}$	0	0	1
$\overline{LRQ5}$, $\overline{IRQ5}$	0	1	0
$\overline{LRQ4}$, $\overline{IRQ4}$	0	1	1
$\overline{LRQ3}$, $\overline{IRQ3}$	1	0	0
$\overline{LRQ2}$, $\overline{IRQ2}$	1	0	1
$\overline{LRQ1}$, $\overline{IRQ1}$	1	1	0
None	1	1	1

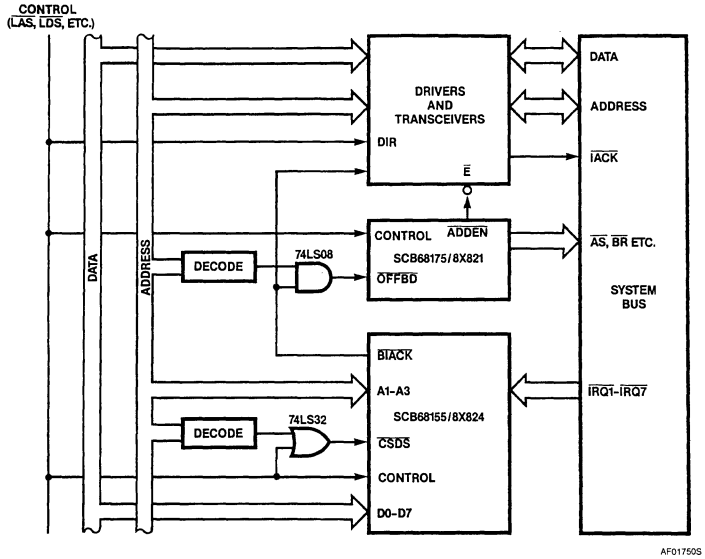


Figure 1. SCB68155/8X824-SCB68175/8X821 Typical System Configuration

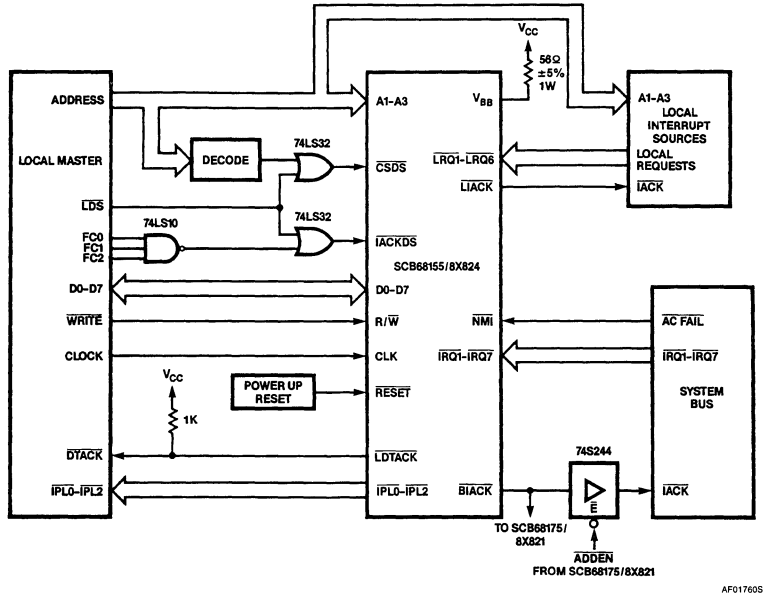


Figure 2. Typical SCB68155/8X824 Local Master Configuration

Signetics SCB68175/8X821 bus controller can be used by the SCB68155/8X824 to acquire the vector (status/ID byte), thereby eliminating the need for the SCB68155/8X824 to duplicate this bus control function. Because most interrupts are serviced by boards that already have the SCB68175/8X821, a one-chip addition of the SCB68155/8X824 gives that board complete interrupt handling capability.

Since the SCB68155/8X824 is an asynchronous device, it is possible for a local interrupt request to be asserted during acknowledgement of a bus interrupt on the same level. The SCB68155/8X824 passes all local interrupt requests through transparent latches which close during each interrupt acknowledge cycle. All possibility of contention is therefore eliminated.

Reset

When $\overline{\text{RESET}}$ is asserted, the SCB68155/8X824 drives $\overline{\text{LDTACK}}$, $\overline{\text{LIACK}}$, $\overline{\text{BIACK}}$ and $\overline{\text{IPL0}}$ – $\overline{\text{IPL2}}$ all high. The D0 – D7 I/O pins go to three-state and all internal registers are cleared.

2

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
Supply voltage[3]	−0.5 to +7.0	V
Input voltage[3]	−0.5 to +5.5	V
Voltage applied to output in off-state[3]	−0.5 to +5.5	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{CC}	Supply voltage		4.75	5.25	V
V_{BB}	Supply voltage		1.35	1.65	V
I_{CC}	V_{CC} supply current	$V_{CC} = 5.25V$		65	mA
I_{BB}	V_{BB} supply current	$V_{BB} = 1.65V$		190	mA
I_{IL}	Input low current	$V_{CC} = 5.25V$, $V_{BB} = 1.65V$, $V_{IL} = 0.4V$		−20	μA
I_{IH}	Input high current	$V_{CC} = 5.25V$, $V_{BB} = 1.65V$, $V_{IH} = 2.7V$		20	μA
I_{OS}	Short circuit output current except $\overline{LDTACK}$	$V_{CC} = 5.25V$, $V_{OUT} = 0V$[6]	−15	−100	mA
V_{OL}	Output low voltage	$V_{CC} = 4.75V$, $V_{BB} = 1.35V$, $I_{OL} = 8mA$		0.6	V
V_{OH}	Output high voltage except $\overline{LDTACK}$	$V_{CC} = 4.75V$, $V_{BB} = 1.35V$, $I_{OH} = -3mA$	2.5		V
I_I	Input leakage current	$V_{CC} = 5.25V$, $V_{IN} = 5.25V$		100	μA
I_{CEX}	Open collector leakage current $\overline{LDTACK}$	$V_{CC} = 4.75V$, $V_{OUT} = 4.25V$		100	μA
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IN} = -10mA$	−1.5		V
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on + 150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient for ceramic package (116°C/W for plastic package).
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 3ns maximum and output voltages are checked at 0.8V and 2.0V.
6. At any time, no more than one output should be connected to ground.
7. t_{TST} is always greater than or equal to t_{DTH}.
8. These parameters are guaranteed at the values listed; these values were determined by characterization procedures. All other tabular entries are taken directly from simulation results run at a range of operation frequencies; these values are not tested or guaranteed.

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5]

PARAMETER		LIMITS		UNIT
		Min	Max	
Register read (see figure 3)				
t_{RWS}	R/$\overline{W}$ to $\overline{CSDS}$ low set-up time	10		ns
t_{IAKS}	$\overline{IACKDS}$ high to $\overline{CSDS}$ low set-up time	10		ns
t_{ADRS}	A1 – A3 valid to $\overline{CSDS}$ low set-up time	30		ns
t_{DTV}	$\overline{CSDS}$ low to D0 – D7 set-up time		89	ns
t_{ACCR}	$\overline{CSDS}$ low to $\overline{LDTACK}$ low read access time		$2t_{CKPD} + 116$[8]	ns
t_{RWH}	$\overline{CSDS}$ high to R/$\overline{W}$ high hold time	0		ns
t_{ADRH}	$\overline{CSDS}$ high to A1 – A3 valid hold time	0		ns
t_{DTH}	$\overline{CSDS}$ high to D0 – D7 valid hold time	0	79	ns
t_{TST}[7]	$\overline{CSDS}$ high to D0 – D7 three state	0	80	ns
t_{ACK}	$\overline{CSDS}$ high to $\overline{LDTACK}$ high time	0	66	ns
t_{CSH}	$\overline{CSDS}$ high time	10		ns
t_{DTCS}	$\overline{LDTACK}$ low to $\overline{CSDS}$ high	0		ns
Register write (see figure 4)				
t_{RWS2}	R/$\overline{W}$ low to $\overline{CSDS}$ low set-up time	10		ns
t_{IAKS}	$\overline{IACKDS}$ high to $\overline{CSDS}$ low set-up time	10		ns
t_{ADRS}	A1 – A3 valid to $\overline{CSDS}$ low set-up time	30		ns
t_{DS}	D0 – D7 valid to $\overline{CSDS}$ low set-up time	0		ns
t_{ACCW}	$\overline{CSDS}$ low to $\overline{LDTACK}$ low write access time		$2t_{CKPD} + 116$[8]	ns
t_{RWH2}	$\overline{CSDS}$ high to R/$\overline{W}$ low hold time	0		ns
t_{ADRH}	$\overline{CSDS}$ high to A1 – A3 valid hold time	0		ns
t_{DH}	$\overline{CSDS}$ high to D0 – D7 valid hold time	0		ns
t_{ACK}	$\overline{CSDS}$ high to $\overline{LDTACK}$ high time	0	66	ns
t_{CSH}	$\overline{CSDS}$ high time	100		ns
t_{DTCS}	$\overline{LDTACK}$ low to $\overline{CSDS}$ high time	0		ns
Vector mode (see figure 5)				
t_{CSS}	$\overline{CSDS}$ high to $\overline{IACKDS}$ low set-up time	10		ns
t_{PDL}	$\overline{IACKDS}$ low to $\overline{LIACK}$ low propagation time	t_{CKPD}	$2t_{CKPD} + 68$	ns
t_{DAV}	$\overline{IACKDS}$ low to D0 – D7 vector valid		103	ns
t_{ACCV}	$\overline{IACKDS}$ low to $\overline{LDTACK}$ low (vector access time)	t_{AKPD}	$t_{ACKPD} + 116$[8]	ns
t_{IKH}	$\overline{IACKDS}$ high time	100		ns
t_{DAH}	$\overline{IACKDS}$ high to D0 – D7 valid hold time	0	111	ns
t_{TRST}[7]	$\overline{IACKDS}$ high to D0 – D7 three state	0	115	ns
t_{IKDT}	$\overline{IACKDS}$ high to $\overline{LDTACK}$ high	0	81	ns
t_{PHD}	$\overline{IACKDS}$ high to $\overline{LIACK}$ high propagation delay	0	42	ns
t_{DTIK}	$\overline{LDTACK}$ low to $\overline{IACKDS}$ high time	0		ns
t_{ADRS}	A1 – A3 valid to $\overline{IACKDS}$ low set-up time	0		ns
t_{ADRH}	$\overline{IACKDS}$ high to A1 – A3 valid hold time	0		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		LIMITS		UNIT
		Min	Max	
Device supplies the vector mode (see figure 6)				
t_{CSS}	$\overline{CSDS}$ high to $\overline{IACKDS}$ low set-up time	10		ns
t_{PDL}	$\overline{IACKDS}$ low to $\overline{LIACK}$ low propagation time delay	t_{CKPD}	$2t_{CKPD} + 68$	ns
t_{IKH}	$\overline{IACKDS}$ high time	100		ns
t_{PDH}	$\overline{IACKDS}$ high to $\overline{LIACK}$ high propagation delay	0	42	ns
t_{ADS}	A1 – A3 valid to $\overline{IACKDS}$ low set-up time	0		ns
t_{ADH}	$\overline{IACKDS}$ high to A1 – A3 valid hold time	0		ns
Bus interrupt acknowledge (see figure 7)				
t_{CSS}	$\overline{CSDS}$ high $\overline{IACKDS}$ set-up time	10		ns
t_{PDL2}	$\overline{IACKDS}$ low to $\overline{BIACK}$ low propagation delay	t_{CKPD}	$2t_{CKPD} + 68$	ns
t_{IKH}	$\overline{IACKDS}$ high time	100		ns
t_{PDH2}	$\overline{IACKDS}$ high to $\overline{BIACK}$ high propagation delay	0	50	ns
t_{ADS}	A1 – A3 valid to $\overline{IACKDS}$ low set-up time	0		ns
t_{ADH}	$\overline{IACKDS}$ high to A1 – A3 hold time	0		ns
Reset timing (see figure 8)				
t_{RST}	$\overline{RESET}$ low time	120		ns
Clock timing (see figure 9)				
t_{CKPD}	Clock period	100		ns
t_{CKH}	Clock high	50		ns

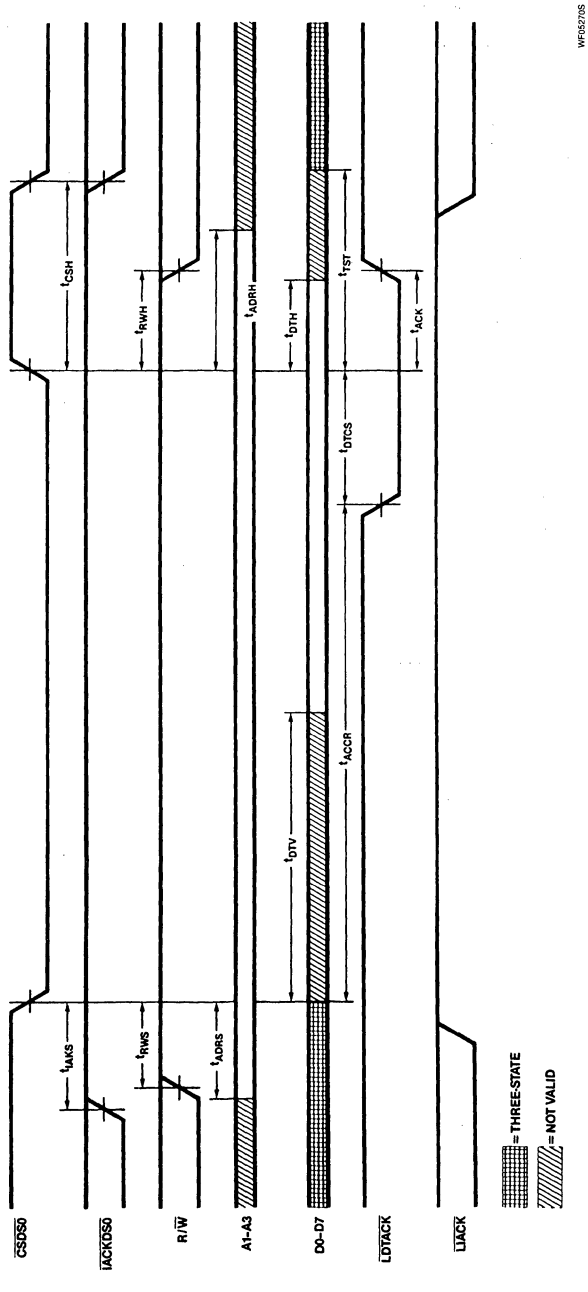


Figure 3. Register Read

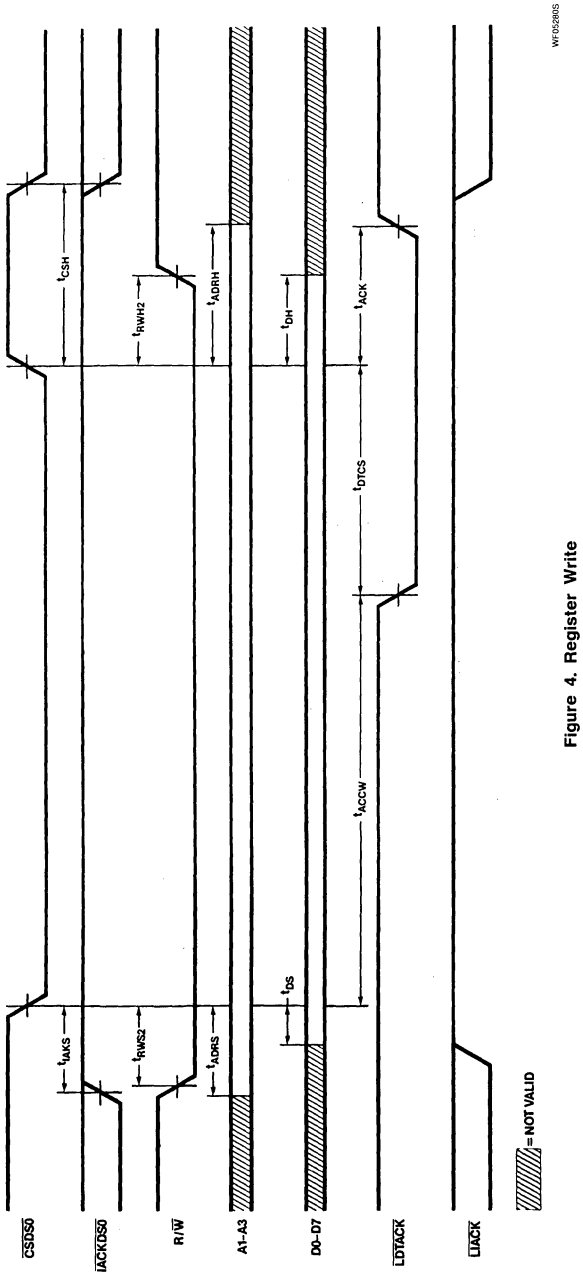


Figure 4. Register Write

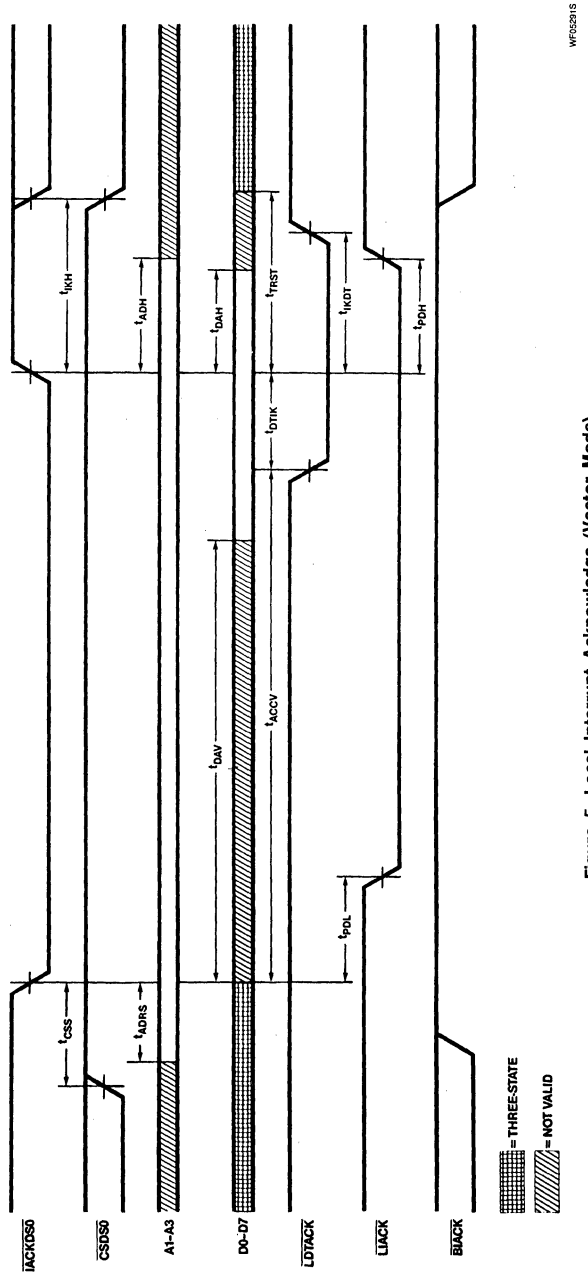


Figure 5. Local Interrupt Acknowledge (Vector Mode)

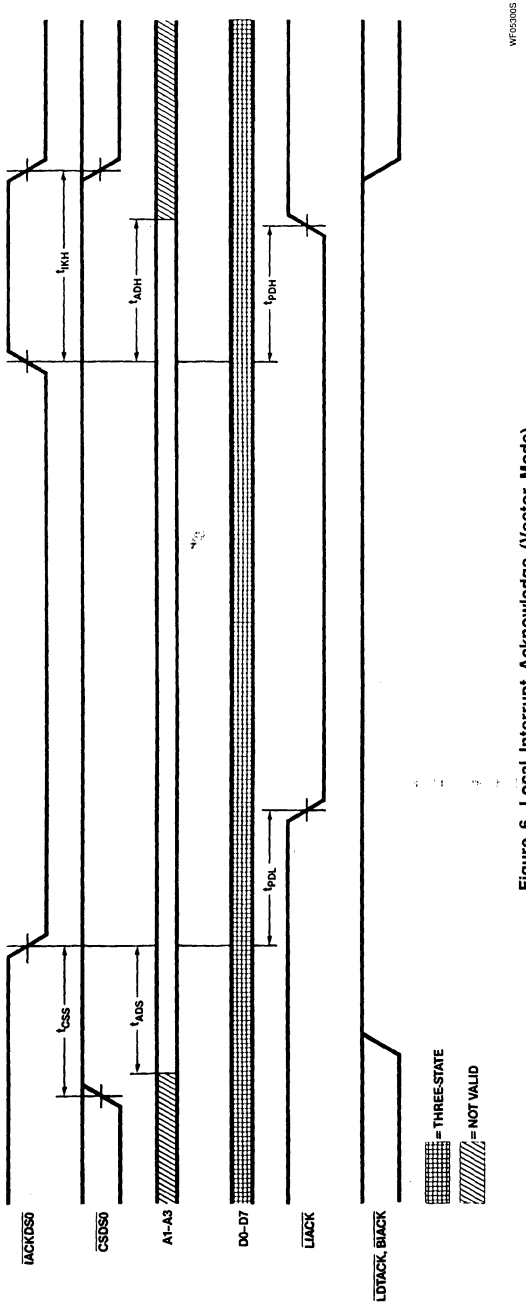


Figure 6. Local Interrupt Acknowledge (Vector Mode)

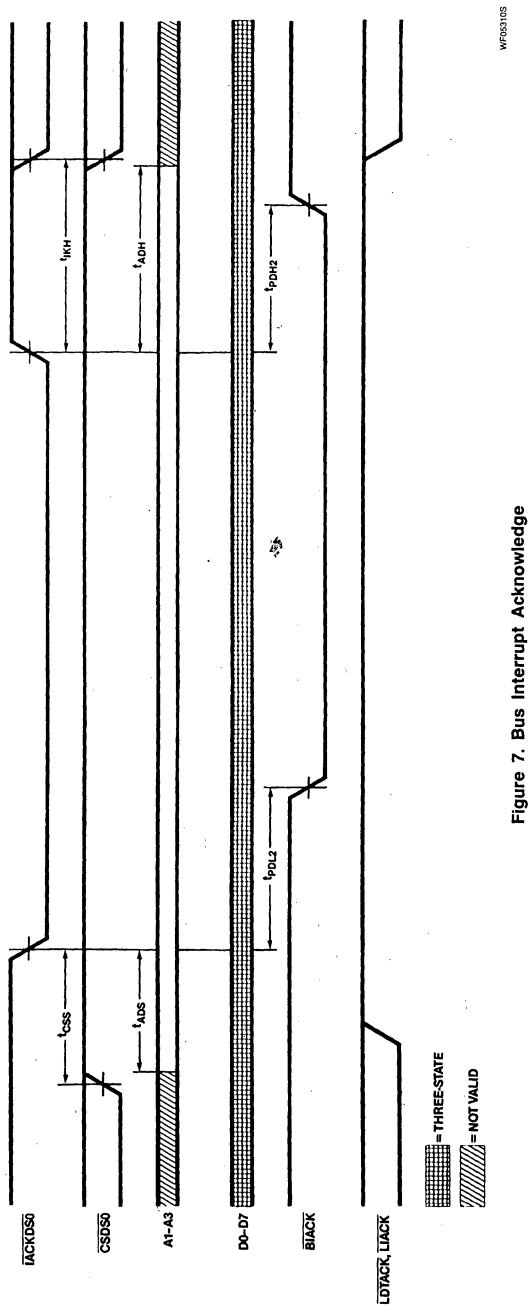


Figure 7. Bus Interrupt Acknowledge

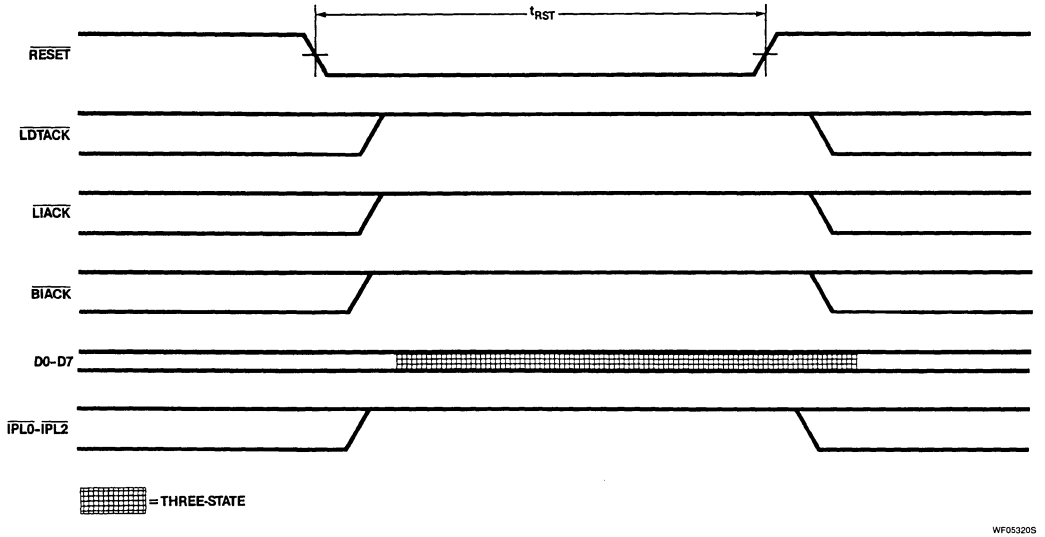


Figure 8. Reset

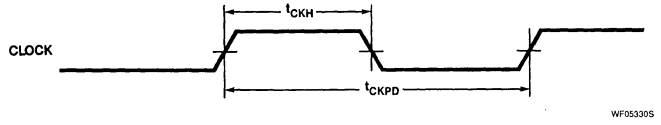


Figure 9. Clock