PRELIMINARY

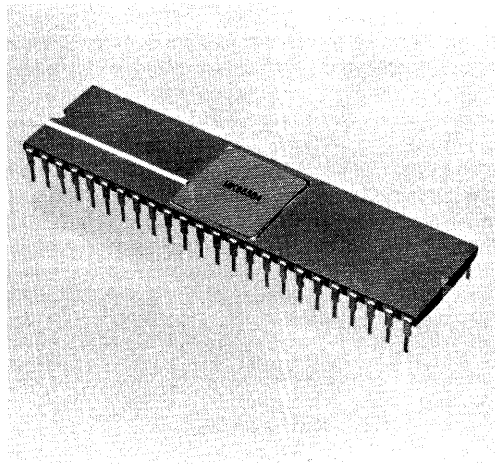
# SERIAL INPUT/OUTPUT CONTROLLER MK68564



## FEATURES

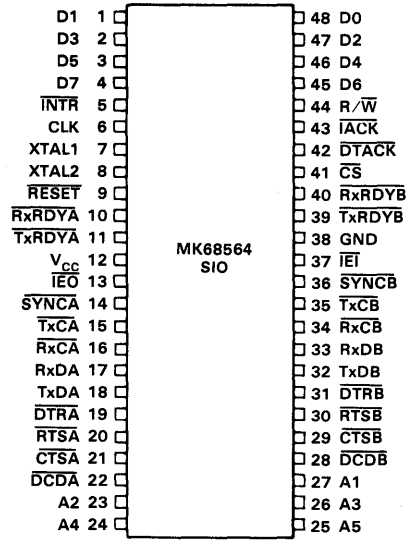
- ☐ Compatible with MK68000 CPU
- ☐ Compatible with MK68000 Series DMA's
- ☐ Two independent, full-duplex channels
- ☐ Two independent baud rate generators
  - Crystal oscillator input
  - Single-phase TTL clock input
- ☐ Directly addressable registers (all control registers are read/write)
- ☐ Data rate in synchronous or asynchronous modes
  - 0-1 M bits/second with 5.0 MHz system clock rate
- ☐ Self-test capability
- ☐ Receive data registers are quadruply buffered; transmit data registers are doubly buffered
- ☐ Daisy-chain priority interrupt logic provides automatic interrupt vectoring without external logic
- ☐ Modem status can be monitored
  - Separate modem controls for each channel
- ☐ Asynchronous features
  - 5, 6, 7, or 8 bits/character
  - 1, 1½, or 2 stop bits
  - Even, odd, or no parity
  - x1, x16, x32, and x64 clock modes
  - Break generation and detection
  - Parity, overrun, and framing error detection
- ☐ Byte synchronous features
  - Internal or external character synchronization
  - One or two sync characters in separate registers
  - Automatic sync character insertion
  - CRC-16 or CRC-CCITT block check generation and checking
- ☐ Bit synchronous features
  - Abort sequence generation and detection
  - Automatic zero insertion and deletion
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - Valid receive messages protected from overrun
  - CRC-CCITT block check generation and checking

**MK68564**
**Figure 1**



## PIN DESCRIPTION

**Figure 2**



## GENERAL DESCRIPTION

The MK68564 SIO is a dual-channel, Serial Input/Output Controller, designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller; however, within that role, it is systems software configurable so that it may be optimized for any given serial data communications application.

The MK68564 is capable of handling asynchronous protocols, synchronous byte-oriented protocols (such as IBM Bisync), and synchronous bit-oriented protocols (such as HDLC and IBM SDLC). This versatile device can also be used to support virtually any serial protocol for applications other than data communications (cassette or floppy disk interface, for example).

The MK68564 can generate and check CRC codes in any synchronous mode and may be programmed to check data integrity in various modes. The device also has facilities for modem controls in each channel. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O.

## SIO PIN DESCRIPTION

| | |
|---|---|
| GND: | Ground. |
| $V_{CC}$: | +5 volts (±5%). |
| $\overline{CS}$: Chip Select | Input active low. $\overline{CS}$ is used to select the MK68564 SIO for access to the internal registers. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time. |
| R/$\overline{W}$: Read/Write | Input. R/$\overline{W}$ is the signal from the bus master, indicating whether the current bus cycle is a read (high) or write (low) cycle. |
| $\overline{DTACK}$: Data Transfer Acknowledge | Output, active low, tri-stateable. $\overline{DTACK}$ is used to signal the bus master that data is ready or that data has been accepted by the MK68564 SIO. |
| A1-A5: Address Bus | Inputs. The address bus is used to select one of the internal registers during a read or write cycle. |
| D0-D7: Data Bus | Bidirectional, tri-stateable. The data bus is used to transfer data to or from the internal registers during a read or write cycle. It is also used to pass a vector during an interrupt acknowledge cycle. |
| CLK: Clock | Input. This input is used to provide the internal timing for the MK68564 SIO. |
| $\overline{RESET}$ Device Reset | Input, active low. $\overline{Reset}$ disables both receivers and transmitters, forces TxDA and TxDB to a marking condition, forces the modem controls high, and disables all interrupts. With the exception of the status registers, data registers, and the vector register, all internal registers are cleared. The vector register is reset to "0FH". |
| $\overline{INTR}$ Interrupt Request | Output, active low, open drain. $\overline{INTR}$ is asserted when the MK68564 SIO is requesting an interrupt. $\overline{INTR}$ is negated during an interrupt acknowledge cycle or by clearing the pending interrupt(s) through software. |
| $\overline{IACK}$ Interrupt Acknowledge | Input, active low. $\overline{IACK}$ is used to signal the MK68564 SIO that the CPU is acknowledging an interrupt. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time. If interrupts are not used then $\overline{IACK}$ should be pulled high. |
| $\overline{IEI}$ Interrupt Enable In | Input, active low. $\overline{IEI}$ is used to signal the MK68564 SIO that no higher priority device is requesting interrupt service. |
| $\overline{IEO}$ Interrupt Enable Out | Output, active low. $\overline{IEO}$ is used to signal lower priority peripherals that neither the MK68564 SIO nor another higher priority peripheral is requesting interrupt service. |
| XTAL1 XTAL2 Baud Rate Generator Inputs | Inputs.A crystal may be connected between XTAL1 and XTAL2, or XTAL1 may be driven with a TTL level clock. When using a crystal, external capacitors must be connected. When driving XTAL1 with a TTL level clock, XTAL2 must be allowed to float. |
| $\overline{RxRDYA}$ $\overline{RxRDYB}$ Receiver Ready | Outputs, active low. Programmable DMA output for the receiver. The $\overline{RxRDY}$ pins pulse low when a character is available in the receive buffer. |
| $\overline{TxRDYA}$ $\overline{TxRDYB}$ Transmitter Ready | Outputs, active low. Programmable DMA output for the transmitter. The $\overline{TxRDY}$ pins pulse low when the transmit buffer is empty. |
| $\overline{CTSA}$ $\overline{CTSB}$ Clear to Send | Inputs, active low. If Tx Auto Enables is selected, these inputs enable the transmitter of their respective channels. If Tx Auto Enables is not selected, these inputs may be used as general purpose input pins. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals. |

| | |
|---|---|
| $\overline{DCDA}$<br>$\overline{DCDB}$<br>Data Carrier Detect | Inputs, active low. If Rx Auto Enables is selected, these inputs enable the receiver of their respective channels. If Rx Auto Enable is not selected, these inputs may be used as general purpose input pins. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals. |
| RxDA<br>RxDB<br>Receive Data | Inputs, active high. Serial data input to the receiver. |
| TxDA<br>TxDB<br>Transmit Data | Outputs, active high. Serial data output of the transmitter. |
| $\overline{RxCA}$<br>$\overline{RxCB}$<br>Receiver Clocks | Input/output. Programmable pin, receive clock input, or baud rate generator output. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals. |
| $\overline{TxCA}$<br>$\overline{TxCB}$<br>Transmitter Clocks | Input/output. Programmable pin, transmit clock input, or baud rate generator output. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals. |
| $\overline{RTSA}$<br>$\overline{RTSB}$<br>Request to Send | Outputs, active low. These outputs follow the inverted state programmed into the RTS bit. When the RTS bit is reset in the asynchronous mode, the output will not change until the character in the transmitter is completely shifted out. These pins may be used as general purpose outputs. |
| $\overline{DTRA}$<br>$\overline{DTRB}$<br>Data Terminal Ready | Outputs, active low. These outputs follow the inverted state programmed into the DTR bit. These pins may also be used as general purpose outputs. |
| $\overline{SYNCA}$<br>$\overline{SYNCB}$<br>Synchroníz-ation | Input/output, active low. The $\overline{SYNC}$ pin is an output when Monosync, Bisync, or SDLC mode is programmed. It is asserted when a sync/flag character is detected by the receiver. The $\overline{SYNC}$ pin is a general purpose input in the Asynchronous mode and an input to the receiver in the External Sync mode. |

## MK68564 ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −25°C to +100°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . −.3 V to +7 V
Power Dissipation . . . . . 1.5 Watt

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 5%, GND = 0 Vdc, $T_A$ = 0 to 70°C)

| CHARACTERISTIC | SYM | MIN | MAX | UNIT |
|---|---|---|---|---|
| INPUT HIGH VOLTAGE ALL INPUTS | $V_{IH}$ | GND + 2.0 | $V_{CC}$ | V |
| INPUT LOW VOLTAGE ALL INPUTS | $V_{IL}$ | GND −0.3 | GND +0.8 | V |
| POWER SUPPLY CURRENT OUTPUTS OPEN | $I_{LL}$ | | 190 | mA |
| INPUT LEAKAGE CURRENT ($V_{IN}$ = 0 to 5.25) | $I_{IN}$ | | ±10 | μA |
| THREE-STATE (OFF STATE) INPUT CURRENT $0 < V_{IN} < V_{CC}$ $\overline{DTACK}$, D0-D7, $\overline{SYNC}$, $\overline{TxC}$, $\overline{RxC}$, $\overline{INTR}$ | $I_{TSI}$ | | 20<br>±10 | μA<br>μA |
| OUTPUT HIGH VOLTAGE ($I_{LOAD}$ = −400 μA, $V_{CC}$=MIN) $\overline{DTACK}$, D0-D7 ($I_{LOAD}$ = −150μA, $V_{CC}$=MIN) ALL OTHER OUTPUTS (EXCEPT XTAL2 & $\overline{INTR}$)* | $V_{OH}$ | GND+2.4 | | V |
| OUTPUT LOW VOLTAGE ($I_{LOAD}$=5.3 mA, $V_{CC}$=MIN) $\overline{INTR}$, $\overline{DTACK}$, D0-D7 ($I_{LOAD}$=2.4 mA, $V_{CC}$=MIN) ALL OTHER OUTPUTS (EXCEPT XTAL2)* | $V_{OL}$ | | 0.5 | V |

*XTAL2 SPECIAL
$\overline{INTR}$ (OPEN DRAIN)

### CAPACITANCE

$T_A$=25°C, f=1 MHz unmeasured pins returned to ground.

| CHARACTERISTIC | SYM | MAX | UNIT | TEST CONDITION |
|---|---|---|---|---|
| Input Capacitance $\overline{CS}$, $\overline{IACK}$ | $C_{IN}$ | 15 | pf | Unmeasured pins returned to ground |
| ALL OTHERS | | 10 | pf | |
| Tri-state Output Capacitance | $C_{OUT}$ | 10 | pf | |

**AC ELECTRICAL CHARACTERISTICS**
($V_{CC}$=5.0 Vdc±5%, GND=0 Vdc, $T_A$=0 to 70°C)

| NUMBER | PARAMETER | 3.0 MHz | | 4.0 MHz | | 5.0 MHz | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| 1 | CLK Period | 330 | 1000 | 250 | 1000 | 200 | 1000 | ns | |
| 2 | CLK Width High | 145 | | 105 | | 80 | | ns | |
| 3 | CLK Width Low | 145 | | 105 | | 80 | | ns | |
| 4 | CLK Fall Time | | 30 | | 30 | | 30 | ns | |
| 5 | CLK Rise Time | | 30 | | 30 | | 30 | ns | |
| 6 | $\overline{CS}$ Low to CLK High (Setup Time) | 0 | | 0 | | 0 | | ns | 1 |
| 7 | A1-A5 Valid to $\overline{CS}$ Low (Setup Time) | 0 | | 0 | | 0 | | ns | |
| 8 | DATA Valid to $\overline{CS}$ Low (Write Cycle) | 0 | | 0 | | 0 | | ns | |
| 9 | $\overline{CS}$ Width High | 50 | | 50 | | 50 | | ns | 1 |
| 10 | $\overline{DTACK}$ Low to A1-A5 Invalid (Hold Time) | 0 | | 0 | | 0 | | ns | |
| 11 | $\overline{DTACK}$ Low to DATA Invalid (Write Cycle Hold Time) | 0 | | 0 | | 0 | | ns | |
| 12 | $\overline{CS}$ High to $\overline{DTACK}$ High (Delay) | | 60 | | 55 | | 50 | ns | |
| 13 | CLK High to $\overline{DTACK}$ Low | | 325 | | 320 | | 295 | ns | |
| 14 | R/$\overline{W}$ Valid to $\overline{CS}$ Low (Setup Time) | 0 | | 0 | | 0 | | ns | |
| 15 | $\overline{DTACK}$ Low to R/$\overline{W}$ Invalid (Hold Time) | 0 | | 0 | | 0 | | ns | |
| 16 | CLK Low to DATA Out | | 550 | | 450 | | 450 | ns | |
| 17 | $\overline{CS}$ High to DATA Out Invalid (Hold Time) | 0 | | 0 | | 0 | | ns | |
| 18 | $\overline{CS}$ High to $\overline{DTACK}$ High Impedance | | 110 | | 105 | | 100 | ns | |
| 19 | $\overline{DTACK}$ Low to $\overline{CS}$ High | 0 | | 0 | | 0 | | ns | |
| 20 | DATA Valid to $\overline{DTACK}$ Low | 70 | | 70 | | 70 | | ns | |
| 21 | $\overline{IACK}$ Width High | 50 | | 50 | | 50 | | ns | 1 |
| 22 | $\overline{IACK}$ Low to CLK High (Setup Time) | 0 | | 0 | | 0 | | ns | 1 |
| 23 | CLK Low to $\overline{INTR}$ Disabled | | 410 | | 410 | | 410 | ns | 2 |
| 24 | CLK Low to DATA Out | | 330 | | 330 | | 330 | ns | 2 |
| 25 | $\overline{DTACK}$ Low to $\overline{IACK}$ High | 0 | | 0 | | 0 | | ns | |
| 26 | $\overline{IACK}$ High to $\overline{DTACK}$ High | | 60 | | 55 | | 50 | ns | |
| 27 | $\overline{IACK}$ High to $\overline{DTACK}$ High Impedance | | 110 | | 105 | | 100 | ns | |
| 28 | $\overline{IACK}$ High to DATA Out Invalid (Hold Time) | 0 | | 0 | | 0 | | ns | |
| 29 | DATA Valid to $\overline{DTACK}$ Low | 195 | | 195 | | 195 | | ns | 2 |
| 30 | CLK Low to $\overline{IEO}$ Low | | 220 | | 220 | | 220 | ns | 3 |

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**AC ELECTRICAL CHARACTERISTICS (Cont.)**
($V_{CC}$=5.0 Vdc±5%, GND=0 Vdc, $T_A$=0 to 70°C)

| NUMBER | PARAMETER | 3.0 MHz | | 4.0 MHz | | 5.0 MHz | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| 31 | $\overline{IEI}$ Low to $\overline{IEO}$ Low | | 140 | | 140 | | 140 | ns | 3 |
| 32 | $\overline{IEI}$ High to $\overline{IEO}$ High | | 190 | | 190 | | 190 | ns | 4 |
| 33 | $\overline{IACK}$ High to $\overline{IEO}$ High | | 190 | | 190 | | 190 | ns | 4 |
| 34 | $\overline{IACK}$ High to $\overline{INTR}$ Low | | 200 | | 200 | | 200 | ns | 5 |
| 35 | $\overline{IEI}$ Low to CLK Low (Setup Time) | 10 | | 10 | | 10 | | ns | |
| 36 | $\overline{IEI}$ Low to $\overline{INTR}$ Disabled | | 500 | | 425 | | 425 | ns | 6 |
| 37 | $\overline{IEI}$ Low to DATA Out Valid | | 225 | | 225 | | 225 | ns | 6 |
| 38 | DATA Out Valid to $\overline{DTACK}$ Low | 55 | | 55 | | 55 | | ns | 6 |
| 39 | $\overline{IACK}$ High to DATA Out High Impedance | | 150 | | 120 | | 90 | ns | |
| 40 | $\overline{CS}$ High to DATA Out High Impedance | | 150 | | 120 | | 90 | ns | |
| 41 | $\overline{CS}$ or $\overline{IACK}$ High to CLK Low | 100 | | 100 | | 100 | | ns | 7 |
| 42 | $\overline{TxRDY}$ or $\overline{RxRDY}$ Width Low | | 3 | | 3 | | 3 | CLK Period | 8,10 |
| 43 | CLK High to $\overline{TxRDY}$ or $\overline{RxRDY}$ Low | | 300 | | 300 | | 300 | ns | |
| 44 | CLK High to $\overline{TxRDY}$ or $\overline{RxRDY}$ High | | 335 | | 300 | | 300 | ns | |
| | $\overline{IACK}$ High to $\overline{CS}$ Low or $\overline{CS}$ High to $\overline{IACK}$ Low (not shown) | 50 | | 50 | | 50 | | ns | 1 |
| 45 | $\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ Pulse Width High | 200 | | 200 | | 200 | | ns | |
| 46 | $\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ Pulse Width Low | 200 | | 200 | | 200 | | ns | |
| 47 | $\overline{TxC}$ Period | 1320 | DC | 1000 | DC | 800 | DC | ns | 9 |
| 48 | $\overline{TxC}$ Width Low | 180 | DC | 180 | DC | 180 | DC | ns | |
| 49 | $\overline{TxC}$ Width High | 180 | DC | 180 | DC | 180 | DC | ns | |
| 50 | $\overline{TxC}$ Low to TxD Delay (X1 Mode) | | 300 | | 300 | | 300 | ns | |
| 51 | $\overline{TxC}$ Low to $\overline{INTR}$ Low Delay | 5 | 9 | 5 | 9 | 5 | 9 | CLK Period | 10 |
| 52 | $\overline{RxC}$ Period | 1320 | DC | 1000 | DC | 800 | DC | ns | 9 |
| 53 | $\overline{RxC}$ Width Low | 180 | DC | 180 | DC | 180 | DC | ns | |
| 54 | $\overline{RxC}$ Width High | 180 | DC | 180 | DC | 180 | DC | ns | |
| 55 | RxD to $\overline{RxC}$ High Setup Time (X1 Mode) | 0 | | 0 | | 0 | | ns | |
| 56 | $\overline{RxC}$ High to RxD Hold Time (X1 Mode) | 140 | | 140 | | 140 | | ns | |
| 57 | $\overline{RxC}$ High to $\overline{INTR}$ Low Delay | 10 | 13 | 10 | 13 | 10 | 13 | CLK Period | 10 |
| 58 | $\overline{RxC}$ High to $\overline{SYNC}$ Low Delay (Output Modes) | 4 | 7 | 4 | 7 | 4 | 7 | CLK Period | 10 |

## AC ELECTRICAL CHARACTERISTICS (Cont.)

($V_{CC}$=5.0 Vdc±5%, GND=0 Vdc, $T_A$=0 to 70°C)

| NUMBER | PARAMETER | 3.0 MHz | | 4.0 MHz | | 5.0 MHz | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| 59 | $\overline{\text{RESET}}$ Low | 1 | | 1 | | 1 | | CLK Period | 10 |
| 60 | XTAL 1 Width High (TTL in) | 145 | | 100 | | 80 | | ns | |
| 61 | XTAL 1 Width Low (TTL in) | 145 | | 100 | | 80 | | ns | |
| 62 | XTAL 1 Period (TTL in) | 330 | 2000 | 250 | 2000 | 200 | 2000 | ns | |
| 63 | XTAL 1 Period (Crystal in) | 330 | 1000 | 250 | 1000 | 200 | 1000 | ns | |

NOTES:

1. This specification only applies if the SIO has completed all operations initiated by the previous bus cycle, when $\overline{CS}$ or $\overline{IACK}$ was asserted. Following a read, write, or interrupt acknowledge cycle, all operations are complete within two CLK cycles after the rising edge of $\overline{CS}$ or $\overline{IACK}$. If $\overline{CS}$ or $\overline{IACK}$ is asserted prior to the completion of the internal operations, the new bus cycle will be postponed.
2. If $\overline{IEI}$ meets the setup time to the falling edge of CLK, 1½ cycles following the clocking in of $\overline{IACK}$.
3. No internal interrupt request pending at the start of an interrupt acknowledge cycle.
4. Time starts when first signal goes invalid (high).
5. If an internal interrupt is pending at the end of the interrupt acknowledge cycle.
6. If Note 2 timing is not met.
7. If this spec is met, the delay listed in note 1 will be one CLK cycle instead of two.
8. Ready signals will be negated asynchronous to the CLK, if the condition causing the assertion of the signals is cleared.
9. If $\overline{RxC}$ and $\overline{TxC}$ are asynchronous to the System Clock, the maximum clock rate into $\overline{RxC}$ and $\overline{TxC}$ should be no more than one-fifth the System Clock rate. If $\overline{RxC}$ and $\overline{TxC}$ are synchronized to the falling edge of the System Clock, the maximum clock rate into $\overline{RxC}$ and $\overline{TxC}$ can be one-fourth the System Clock rate.
10. SIO Clock (CLK) Cycles as defined in Parameter 1.

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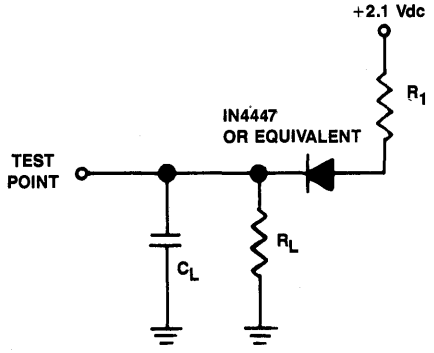
## OUTPUT TEST LOAD

**Figure 3**




for all outputs except $\overline{DTACK}$, D0-D7, $\overline{INTR}$, XTAL2

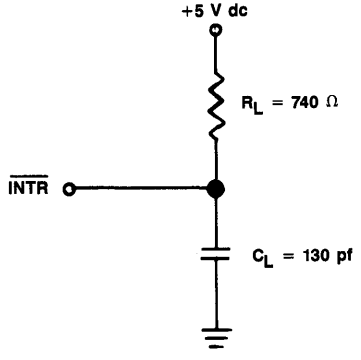
$C_L$ = 130 pf
$R_L$ = 16K Ω
$R_1$ = 450 Ω

for $\overline{DTACK}$, D0-D7

$C_L$ = 130 pf
$R_L$ = 6K Ω
$R_1$ = 200 Ω

## $\overline{INTR}$ TEST LOAD

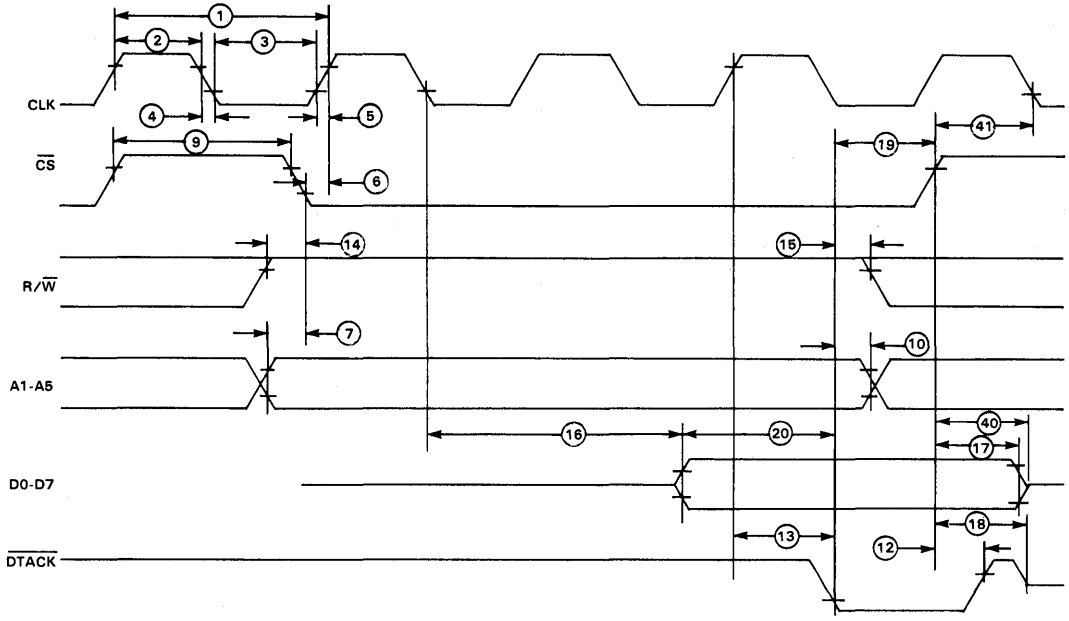
**Figure 4**




**NOTE:**
XTAL2 output test load is a cyrstal.

## READ CYCLE

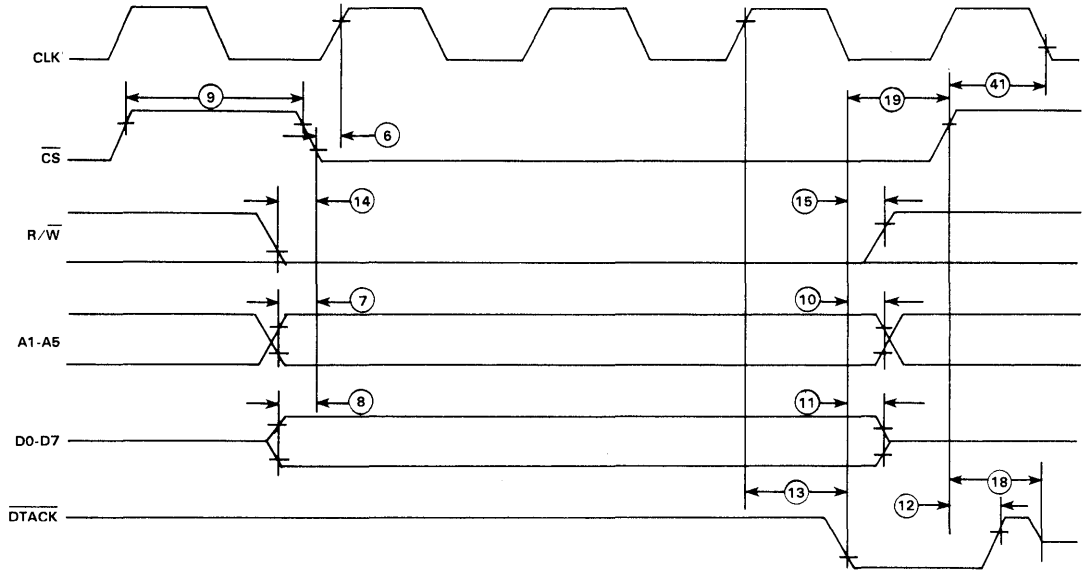
**Figure 5**




**NOTE:**
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

## WRITE CYCLE

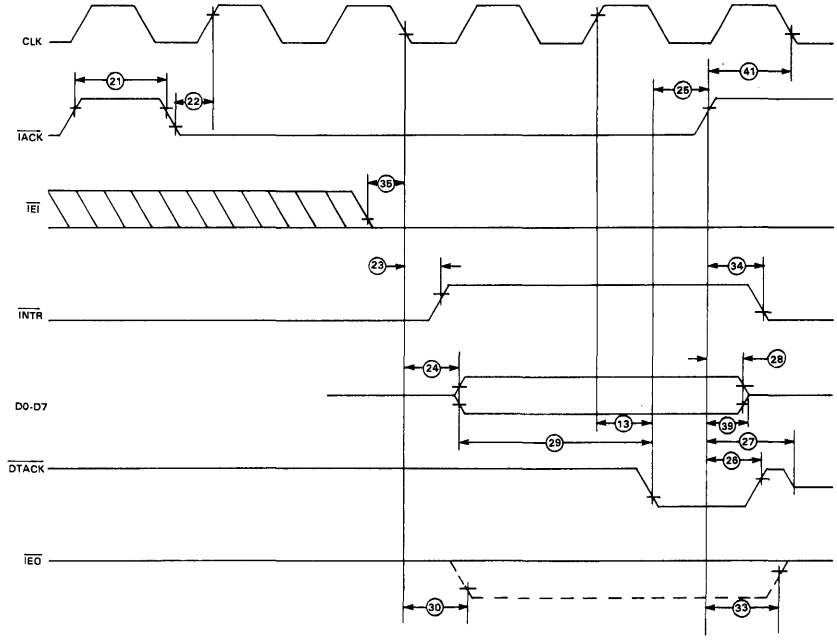
**Figure 6**




**NOTE:**
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

## INTERRUPT ACKNOWLEDGE CYCLE ($\overline{IEI}$ LOW)

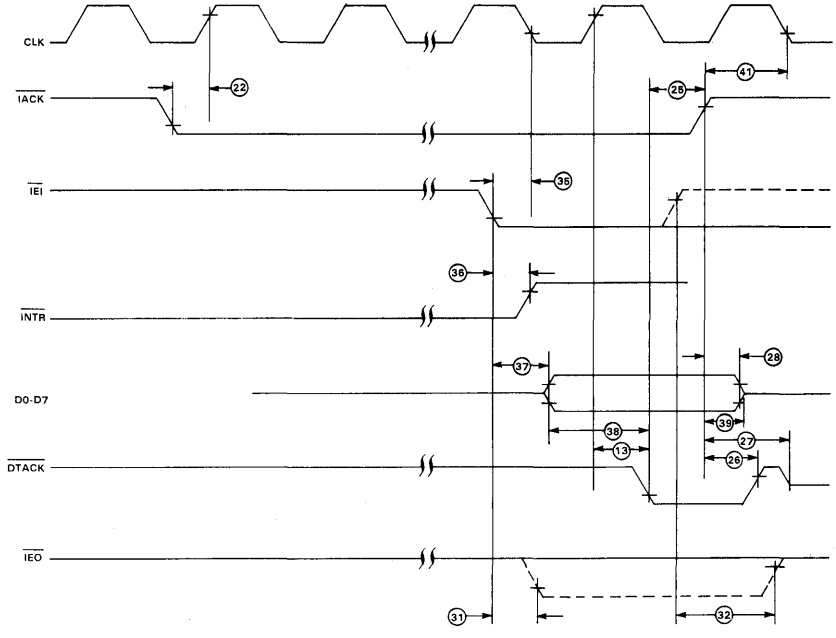
**Figure 7**




**NOTE:**
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

## INTERRUPT ACKNOWLEDGE CYCLE ($\overline{IEI}$ HIGH)

**Figure 8**




**NOTE:**
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

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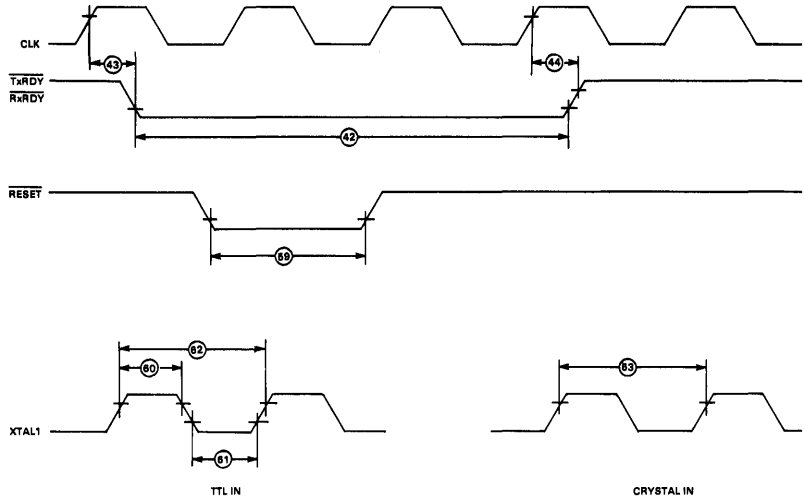
## DMA INTERFACE TIMING

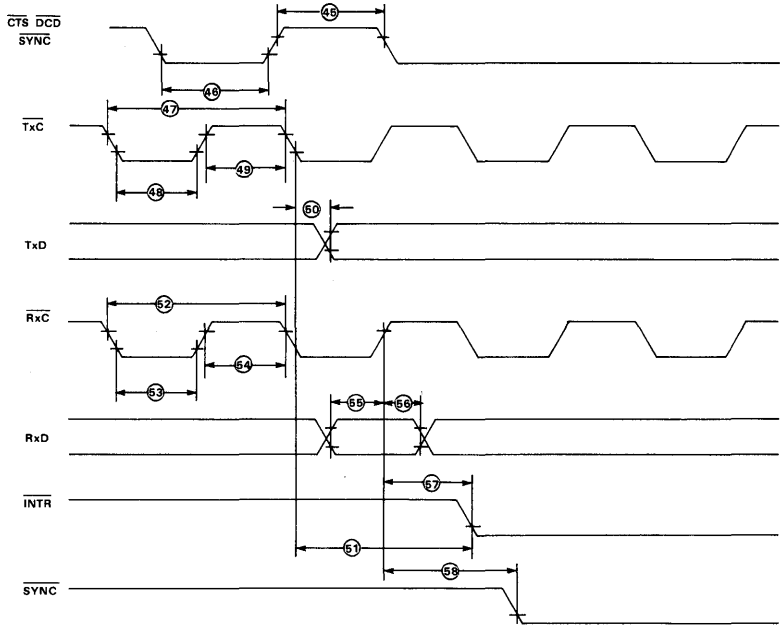
**Figure 9**




**NOTE:**
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

## SERIAL INTERFACE TIMING

**Figure 10**




**NOTE:**
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

## MK68564 ORDERING INFORMATION

| PART NO. | PACKAGE TYPE | MAX. CLOCK FREQUENCY | TEMPERATURE RANGE |
|---|---|---|---|
| MK68564N-03 | Plastic | 3.0 MHz | 0° to 70°C |
| MK68564N-04 | Plastic | 4.0 MHz | 0° to 70°C |
| MK68564N-05 | Plastic | 5.0 MHz | 0° to 70°C |