THOMSON
COMPONENTS

MOSTEK

TECHNICAL
MANUAL

MK68590
CONTROLLER FOR ETHERNET LOCAL AREA NETWORK

TABLE OF CONTENTS

SECTION PAGE

Chapter 1
General Description

Chapter 2
Programming Specifications

Chapter 3
Functional Specifications

Chapter 4
Electrical Specifications

LIST OF ILLUSTRATIONS

CHAPTER 1
GENERAL DESCRIPTION

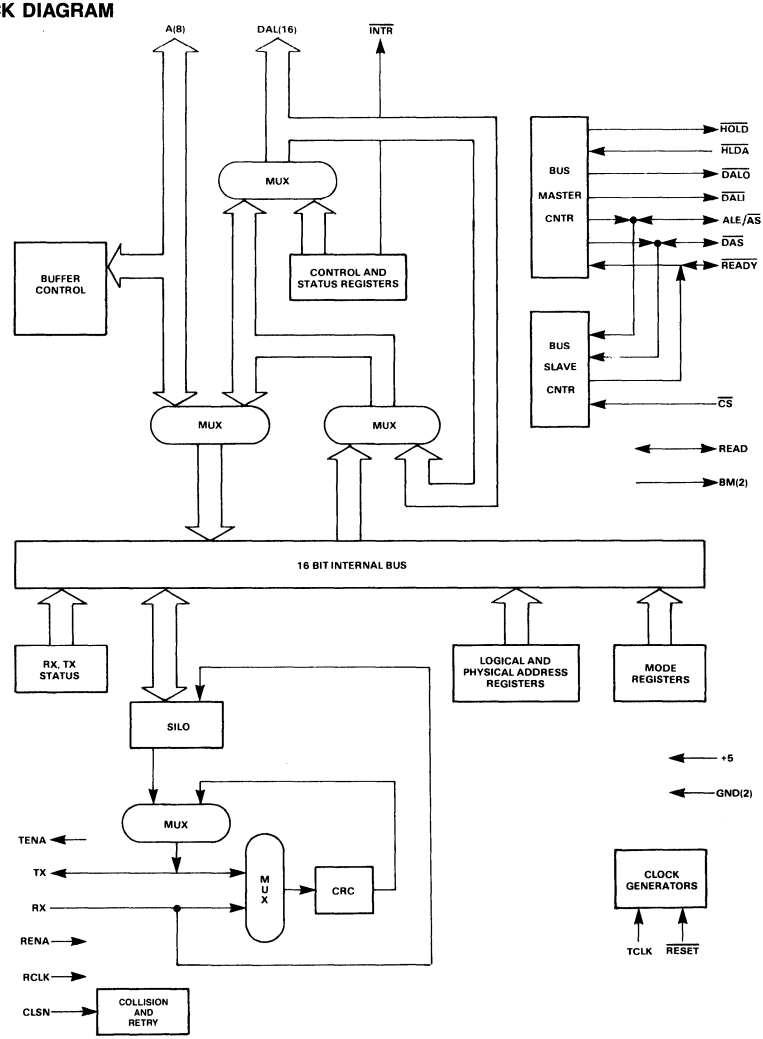
1.0 INTRODUCTION

1.1 OVERVIEW

The MK68590 LANCE (Local Area Network Controller for Ethernet) is a 48-pin VLSI device designed to simplify greatly the interfacing of a microcomputer or a minicomputer to an Ethernet Local Area Network. This chip is intended to operate in a local environment that includes a closely coupled memory and microprocessor. The LANCE uses scaled N-channel MOS technology and is compatible with several microprocessors. A block diagram of the chip is shown in Figure 1.

LANCE is a trademark of Mostek Corporation.

LANCE BLOCK DIAGRAM
Figure 1

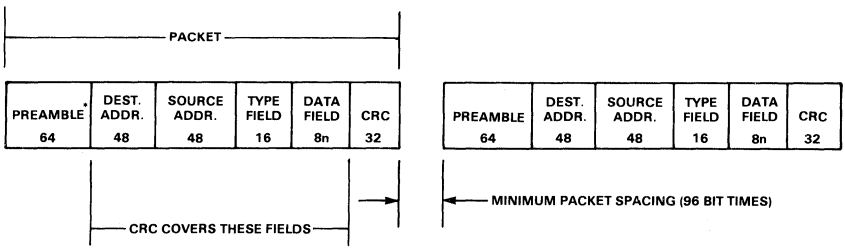


1.2 FUNCTIONAL CAPABILITIES

The Local Area Network Controller for Ethernet (LANCE) interfaces to a microprocessor bus characterized by time multiplexed address and data lines. Typically, data transfers are 16 bits wide, but byte transfers occur if the buffer memory address boundaries are odd. The address bus is 24 bits wide.

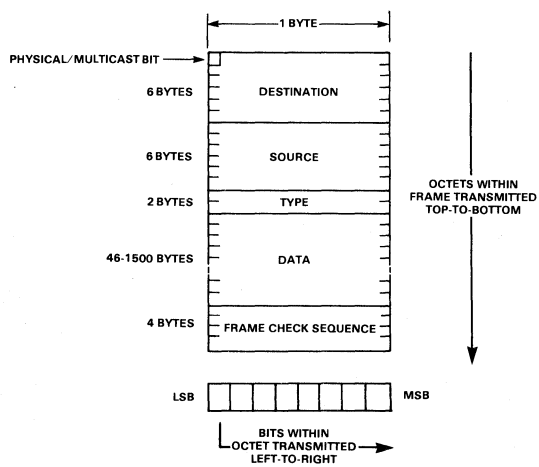
The Ethernet packet format consists of a 64-bit preamble, a 48-bit destination address, a 48-bit source address, a 16-bit type field, and a 46 to 1500 byte data field terminated with a 32-bit CRC as shown in Figure 2 and Figure 3. The variable widths of the packets accommodate both short status, command and terminal traffic packets, and long data packets to printers and disks (1024 byte disk sectors for example). Packets are spaced a minimum of 9.6 μsec apart to allow one node time enough to receive back-to-back packets.

ETHERNET AND LANCE PACKET FORMAT
Figure 2



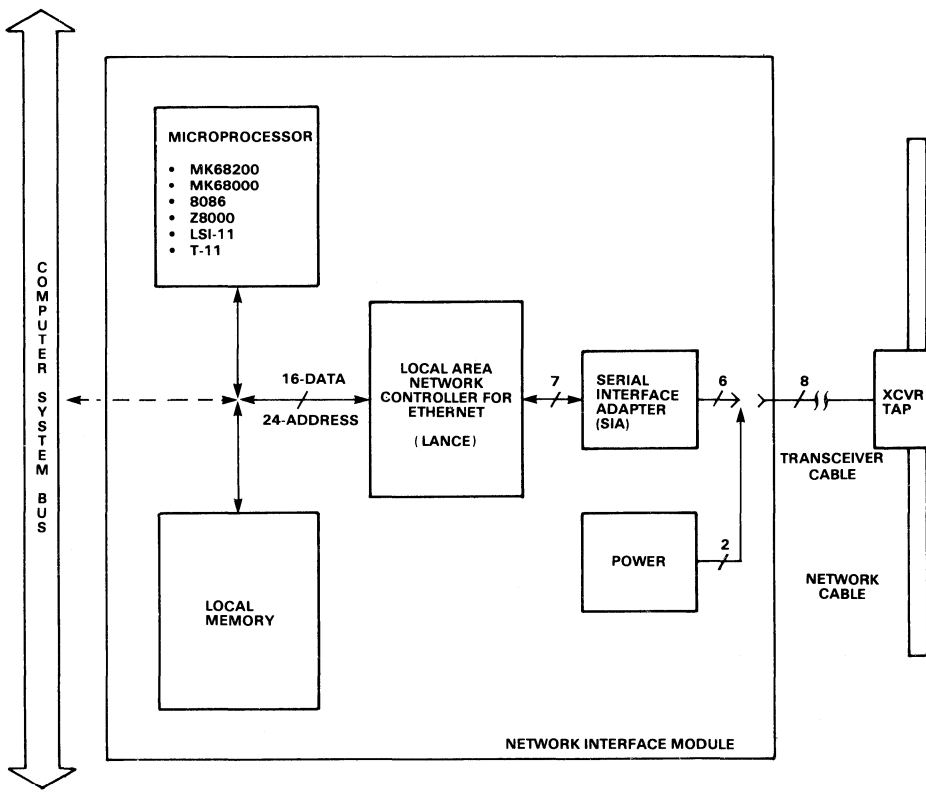
*Last Byte is Start of Frame Synchronization Byte--10101011

ETHERNET AND LANCE PACKET BIT TRANSMISSION SEQUENCE
Figure 3



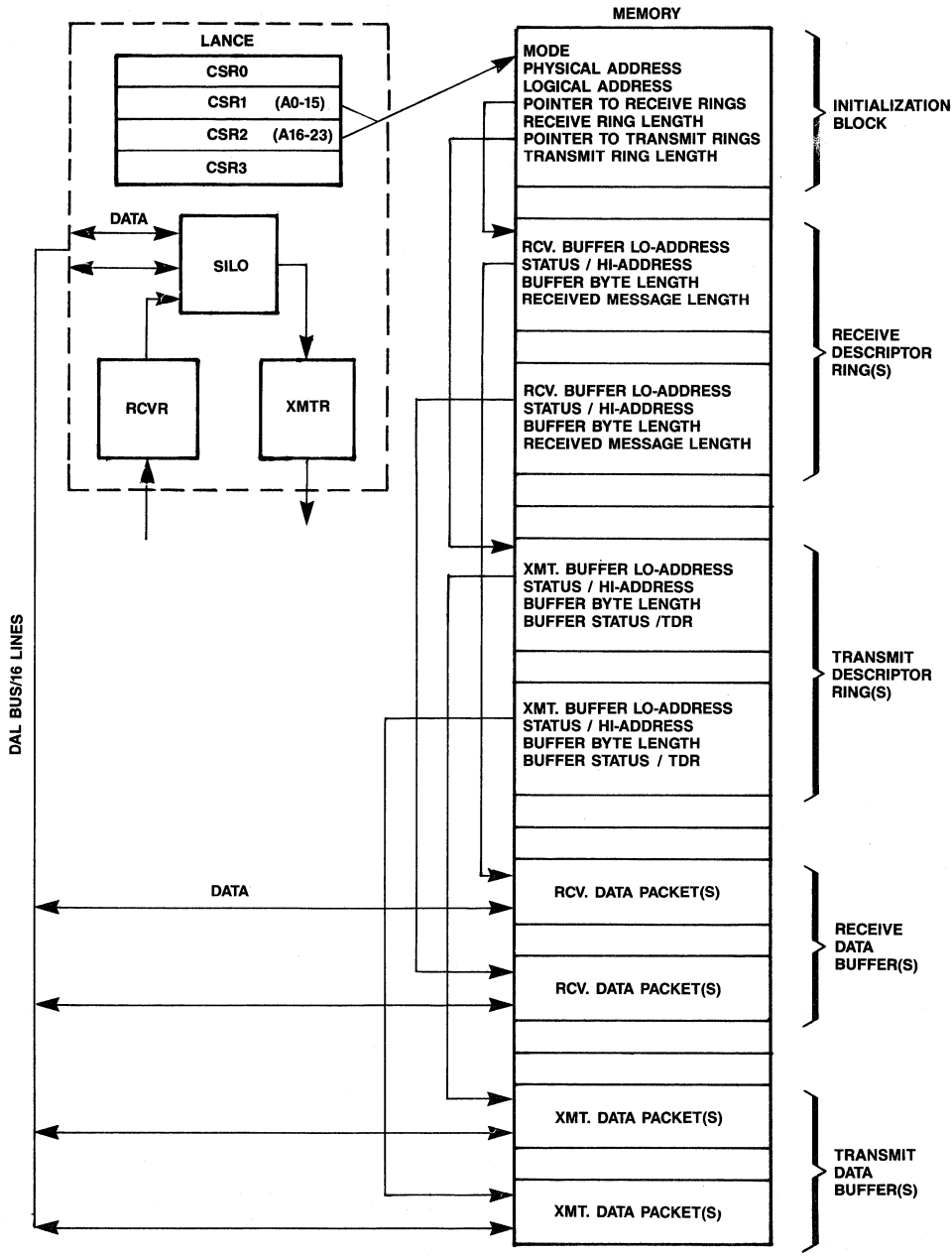
The LANCE is intended to operate in a minimal configuration that requires close coupling between local memory and a processor. Figure 5 shows the relationship between the chip and local memory. The local memory provides packet buffering for the chip and serves as a communication link between the chip and the processor. During initialization, the control processor loads into LANCE the starting address of the initialization block plus the operating mode of the chip via two control registers. It is only during this initial phase that the host processor talks directly to LANCE. All further communications are handled via a DMA machine under microword control contained within the LANCE. Figure 4 is a block diagram of the LANCE and SIA device used to create an Ethernet interface for a computer system.

ETHERNET LOCAL AREA NETWORK SYSTEM BLOCK DIAGRAM
Figure 4



LANCE CONCEPTUAL VIEW

Figure 5



1.3 FUNCTIONAL DESCRIPTION

1.3.1 SERIAL DATA HANDLING

The basic operation of the chip set to provide the Ethernet interface is as follows. In the transmit mode (since there is only one transmission path, Ethernet is a half duplex system), the LANCE reads data from a transmit buffer by using Direct Memory Access (DMA) and appends the preamble, sync pattern (two ones after alternating ones and zeros in the preamble), and calculates and appends the complement of the 32-bit CRC. The first eight words of the transmit buffer must contain the destination address, source address, and type field as detailed in the Ethernet specification. In the receive mode, the destination address, source address, type, data, and CRC fields are transferred to memory via DMA cycles. The CRC is calculated as the data and transmitted CRC are received. At the end of the packet, if this calculated CRC does not agree with a constant, an error bit is set and in RMD1 of the receiver descriptor rings. In the receive mode, packets will be accepted by the LANCE under four modes of operation. The first mode is a full comparison of the 48-bit destination address in the packet with the node address that was programmed into the LANCE during an initialization cycle. There are two types of logical address. One is a group type mask where the 48-bit address in the packet is put through a hash filter in order to map the 48-bit physical addresses into 1 of 64 logical groups. This mode can be useful if sending packets to all of one type of a device simultaneously or the network (i.e. sending a packet to all file servers or all printer servers). The second logical address is the broadcast address where all nodes on the network receive the packet. The last receive mode of operation is the so called "promiscuous mode" in which a node will accept all packets on the network cable regardless of their destination address.

1.3.2 COLLISION DETECTION AND IMPLEMENTATION

The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear network cable before transmitting, Ethernet handles collisions in a predetermined way. Should two transmitters attempt to seize the network cable at the same time, they will collide, and the data on the network cable will be garbled. LANCE is constantly monitoring the CLSN (Collision) pin. This signal is generated by the transceiver when the signal level on the network cable indicates the presence of signals from two or more transmitters. If LANCE is transmitting when CLSN is asserted, it will continue to transmit the preamble, (normally collisions will occur while the preamble is being transmitted) then will "jam" the network for 32 bit times (3.2 microseconds). This jamming ensures that all nodes have enough time to detect the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm defined in the Ethernet specification to minimize the probability of the colliding nodes having multiple collisions with each other. After 16 abortive attempts to transmit a packet, LANCE will report a RTRY error due to excessive collisions and step over the transmit buffer. During reception, the detection of a collision causes that reception to be aborted. Depending on when the collision occurred, LANCE will treat this packet as an error packet if the packet has an address mismatch, as a runt packet (a packet that has less than 64 bytes), or as a legal length packet with a CRC error. Extensive error reporting is provided by the LANCE through a microprocessor interrupt and error bits in a status register. The following are the significant error conditions: CRC error on received data; transmitter on longer than 1518 bytes; missed packet error (meaning a packet on the network cable was missed because there were no empty buffers in memory), and memory error, in which the memory did not respond (handshake) to a memory cycle request.

1.3.3 BUFFER MANAGEMENT

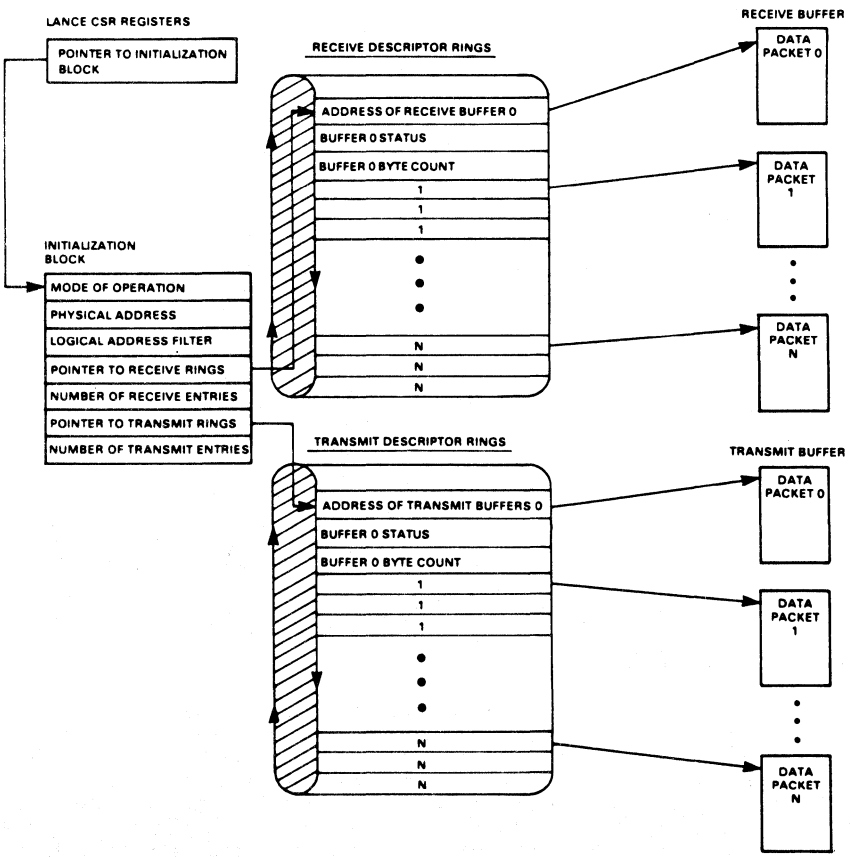
A key feature of the LANCE and its on board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings, as shown in Figure 6. There are separate descriptor rings to describe transmit and receive operations. Up to 128 tasks may be queued up on a descriptor ring awaiting execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the length of the data buffer. Data buffers can be chained or cascaded in order to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor

rings in a "look ahead manner" to determine the next empty buffer in order to chain buffers together or to handle back to back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer. The minimum buffer size is 64 bytes for receive buffers and 100 bytes for transmit buffers.

1.3.4 MICROPROCESSOR INTERFACE

The parallel interface of the LANCE has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the following: MK68000, Z8000, 8086, LSI-11, T-11, and MK68200. (The MK68200 is a 16-bit single chip microcomputer being sampled by Mostek with an architecture modeled after the MK68000). The LANCE has a wide 24-bit linear address space when it is in the Bus Master Mode, allowing it to DMA directly into the entire address space of the above microprocessors. No segmentation or paging methods are used within the LANCE, and as such the addressing is closest to that used by the MK68000 but is compatible with the others. When the LANCE is a bus master, a programmable mode of operation allows byte addressing either by employing a Byte/Word control signal, much like that used on the 8086 or the Z8000, or by using an Upper Data Strobe/Lower Data strobe much like that used on the MK68000, LSI-11, and MK68200 microprocessors. A program-

LANCE MEMORY MANAGEMENT
Figure 6

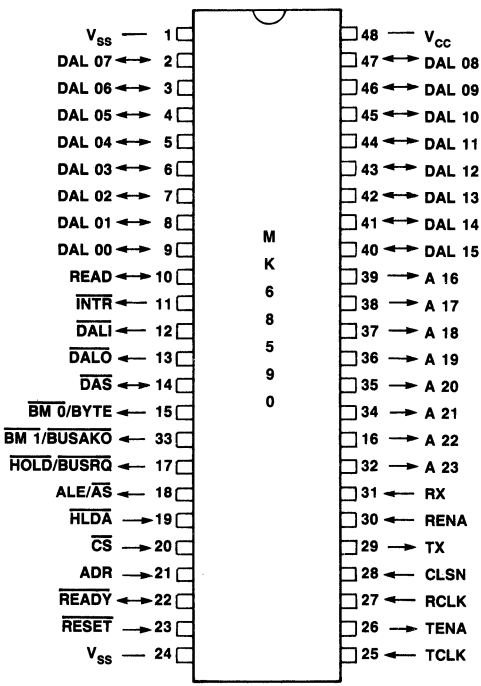


mable polarity on the Address Strobe signal eliminates the need for external logic. The LANCE interfaces with both multiplexed and demultiplexed data buses and features control signals for address/data bus transceivers.

Interrupts to the microprocessor are generated by the LANCE upon completion of its initialization routine, the reception of a packet, the transmission of a packet, transmitter timeout error, a missed packet, or a memory error.

The cause of the interrupt is ascertained by reading the control status register (CSR0). Bit (06) of CSR0, INEA, enables or disables interrupts to the microprocessor. In a polling mode, BIT (07) of CSR0 is sampled to determine when an interrupt causing condition occurred.

LANCE PIN ASSIGNMENT
Figure 7



1.3.5 PIN DESCRIPTION

DAL00-DAL15
(Data/Address Bus)
Input/Output Tri-State. Pins 2-9 and 40-47. The time multiplexed Address/Data bus. During the address portion of a memory transfer, DAL <15:00> contains the lower 16 bits of the memory address. The upper 8 bits of address are contained in A <23:16>. During the data portion of a memory transfer, DAL <15:00> contains the read or write data, depending on the type of transfer. The LANCE drives these lines both as a Bus Master and as a Bus Slave.

READ
Input/Output Tri-State. Pin 10. Read indicates the type of operation the bus controller is performing during a bus transaction. When it is a Bus Master, LANCE drives READ. Read is valid during the entire bus transaction and is tri-stated at all other times.

LANCE as Bus Slave:
High - The chip places data on the DAL lines.
Low - The chip takes data off the DAL lines.
LANCE as Bus Master:
High - The chip takes data off the DAL lines.
Low - The chip places data on the DAL lines.

$\overline{\text{INTR}}$
(Interrupt)
Output Open Drain. Pin 11. INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set: BABL, MISS, MERR, RINT, TINT OR IDON. Interrupt is enabled by CSR0 <6>, INEA = 1.

$\overline{\text{DALI}}$
(Data/Address Line In)
Output Tri-State. Pin 12. DAL IN is an external bus transceiver control line. LANCE drives $\overline{\text{DALI}}$ only while it is the Bus Master. When LANCE reads the DAL lines during the data portion of a READ transfer, $\overline{\text{DALI}}$ is asserted. $\overline{\text{DALI}}$ is not asserted during a WRITE transfer.

$\overline{\text{DALO}}$
(Data/Address Line Out)
Output Tri-State. Pin 13. DAL OUT is an external bus transceiver control line. LANCE drives $\overline{\text{DALO}}$ only when it is a Bus Master. When LANCE drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer, $\overline{\text{DALO}}$ is asserted.

$\overline{\text{DAS}}$
(Data/Strobe)
Input/Output Tri-State. Pin 14. Data Strobe defines the data portion of the bus transaction. By definition, data is stable and valid at the low to high transition of $\overline{\text{DAS}}$. When it is the Bus Master, LANCE drives this signal. At all other times, the signal is tri-stated.

$\overline{\text{BM0}}$, $\overline{\text{BM1}}$ or BYTE, $\overline{\text{BUSAK0}}$
(Byte Mask)
Output Tri-State. Pins 15 and 16 are programmable through CSR3.

CSR3<00> BCON = 0
PIN 15 = $\overline{\text{BM0}}$ (Output Tri-State)
PIN 16 = $\overline{\text{BM1}}$ (Output Tri-State)
Byte Mask <1:0> Indicates the byte(s) on the DAL to be read or written during this bus transaction. LANCE drives these lines only as a Bus Master. LANCE ignores the BM lines when it is a Bus Slave and assumes word transfers. Byte selection follows:

$\overline{\text{BM1}}$	$\overline{\text{BM0}}$	
LOW	LOW	Whole Word
LOW	HIGH	Byte <DAL 15:08>
HIGH	LOW	Byte <DAL 07:00>
HIGH	HIGH	None

CSR3<00> BCON = 1
PIN 15 = BYTE (Output Tri-State)
PIN 16 = $\overline{\text{BUSAKO}}$ (Output)

Byte selection occurs by using the BYTE line and DAL <00> latched during the address portion of the bus transaction. LANCE drives BYTE only as a Bus Master and ignores it when operating as a Bus Slave. Byte selection occurs as follows:

BYTE	DAL<00>	(During Address Portion)
LOW	LOW	WHOLE WORD
LOW	HIGH	ILLEGAL CONDITION
HIGH	LOW	LOWER BYTE
HIGH	HIGH	UPPER BYTE

$\overline{\text{BUSAKO}}$ is a bus request daisy chain output. If LANCE is not requesting the bus and it receives $\overline{\text{HLDA}}$, $\overline{\text{BUSAKO}}$ is driven low. If LANCE is requesting the bus when it receives $\overline{\text{HLDA}}$, $\overline{\text{BUSAKO}}$ remains high.

$\overline{\text{HOLD}}$/$\overline{\text{BUSRQ}}$
(Bus Hold Request)

Input/Output Open Drain. Pin 17. This pin is programmable through CSR3.

CSR3<00> BCON = 0
PIN 17 = $\overline{\text{HOLD}}$

LANCE asserts the $\overline{\text{HOLD}}$ request when it requires a DMA cycle regardless of the $\overline{\text{HOLD}}$ pin state. $\overline{\text{HOLD}}$ is held LOW for the entire bus transaction.

CSR3<00> BCON = 1
PIN 17 = $\overline{\text{BUSRQ}}$

LANCE asserts $\overline{\text{BUSRQ}}$ when it requires a DMA cycle if the prior state of the $\overline{\text{BUSRQ}}$ pin was high. $\overline{\text{BUSRQ}}$ is held low for the entire bus transaction.

ALE/$\overline{\text{AS}}$
(Address Latch Enable)

Output Tri-State. Pin 18. The active level of Address Strobe is programmable through CSR3. The address portion of a bus transfer occurs while this signal is at its asserted level. LANCE drives this signal while it is the Bus Master. At all other times, the signal is tri-stated.

CSR3<01> ACON = 0
PIN 18 = ALE

Address Latch Enable is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion. A slave device can use ALE to control a latch on the bus address lines. When ALE is high, the latch should be open and when ALE goes low, the latch should be closed.

CSR3<01> ACON = 1
PIN 18 = AS

As AS, the signal pulses low during the address portion of the bus transfer. The low to high transition of AS can be used by a slave device to strobe the address into a register.

$\overline{\text{HLDA}}$
(Hold Acknowledge)

Input. Pin 19. Hold Acknowledge is the response to $\overline{\text{HOLD}}$. When $\overline{\text{HLDA}}$ is low in response to LANCE's assertion of $\overline{\text{HOLD}}$, the LANCE is the Bus Master. $\overline{\text{HLDA}}$ should be deasserted after LANCE releases $\overline{\text{HOLD}}$.

$\overline{CS}$
(Chip Select)
Input. Pin 20. When low, $\overline{CS}$ indicates LANCE is the slave device for the data transfer. $\overline{CS}$ must be valid throughout the data portion of the transaction.

ADR
(Register Address Port Select)
Input. Pin 21. Address selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and the chip only uses it when $\overline{CS}$ is low.

ADR	PORT
LOW	Register Data Port
HIGH	Register Address Port

$\overline{READY}$
Input/Output Open Drain. Pin 22. When LANCE is a Bus Master, $\overline{READY}$ is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle. As a Bus Slave, LANCE asserts $\overline{READY}$ when it has put data on the DAL lines during a READ cycle or is about to take data off the DAL lines during a WRITE cycle. $\overline{READY}$ is a response to $\overline{DAS}$ and is negated after $\overline{DAS}$ is negated. $\overline{CS}$ and $\overline{DAS}$ must remain asserted until $\overline{READY}$ is asserted or $\overline{READY}$ will not be asserted.

$\overline{RESET}$
(Bus Reset Signal.)
Input. Pin 23. Causes LANCE to cease operation, clear its internal logic and enter an idle state with the STOP bit of CSR0 set.

TLCK
(Transmit Clock)
Input. Pin 25. A crystal-controlled 10 MHz clock. This clock is the primary LANCE clock as well as the Transmit clock. (A 0.01 % clock as specified in the Ethernet Specification.)

TENA
(Transmit Enable)
Output. Pin 26. A high level signal asserted with the transmit output serial bit stream, TX, to enable the external transmit logic.

RCLK
(Receive Clock)
Input. Pin 27. The 10 MHz clock that is synchronous with the received data and is used for transferring the received data into the LANCE.

CLSN
Collision)
Input. Pin 28. A logical input that indicates, when high, that a collision is occurring on the channel.

TX
(Transmit)
Output. Pin 29. Transmit Output Bit Stream.

RENA
(Receive Enable)
Input. Pin 30. A logical input that indicates, when high, the presence of data on the channel.

RX
(Receive)
Input. Pin 31. The input for the serial receive data. The data is synchronous with the receive clock.

A16-A23
(High-Order Address Bus)
Output, Three State pins 32 thru 39. Address bits <23:16> used in conjunction with DAL <15:00> to produce a 24-bit address. LANCE drives these lines only as a Bus Master.

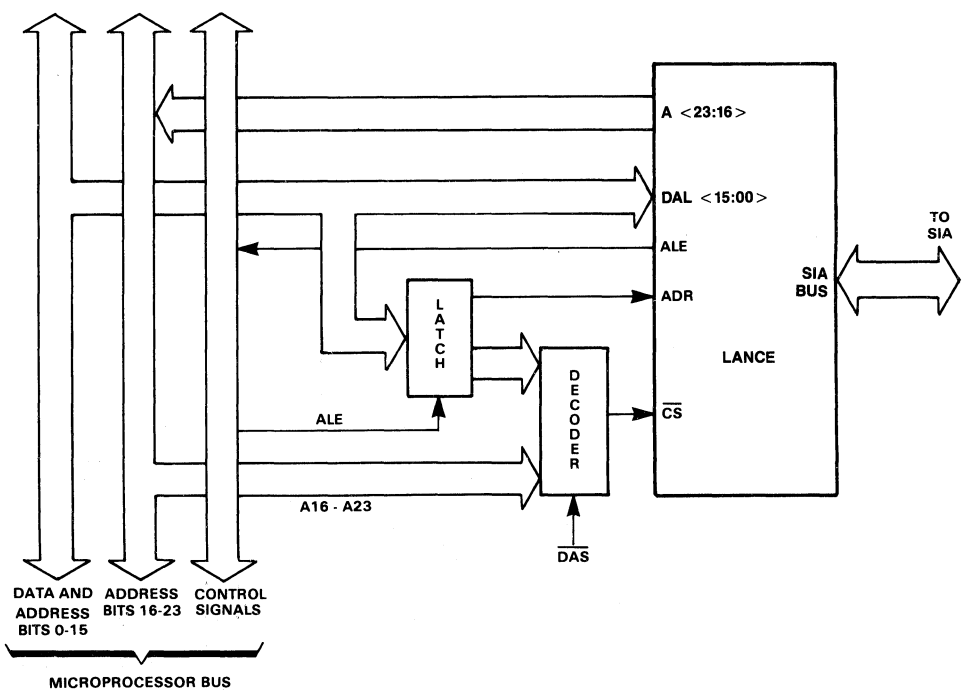
V_{CC}
Power supply pin 48. +5 VDC ±5%. It is recommended that a power supply filter be used between V_{CC} (Pin 48) and V_{SS} (Pins 1 and 24). This filter should consist of two capacitors in parallel having the values of 10μF and .047μF respectively.

V_{SS}
Ground pins 1 and 24. 0 VDC

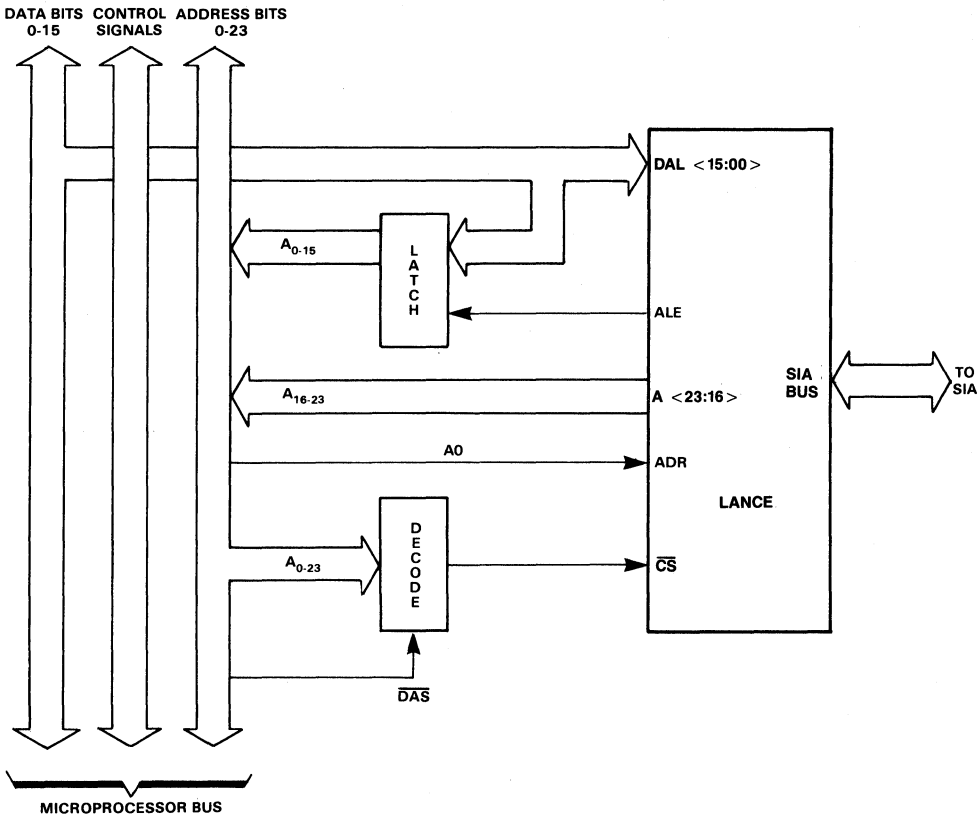
1.3.6 LANCE INTERFACE DESCRIPTION--BUS MASTER MODE

All data transfers from the LANCE in the Bus Master mode are timed by ALE, $\overline{DAS}$, and $\overline{READY}$. The automatic adjustment of the LANCE cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600 nsec in length and can be increased in 100 nsec increments. Figure 8 and Figure 9 show generalized interfaces to both multiplexed and demultiplexed bus microprocessors, and Figure 10, the Bus Master Timing modes.

MULTIPLEXED BUS INTERFACE
Figure 8



DEMULTIPLEXED BUS INTERFACE
Figure 9

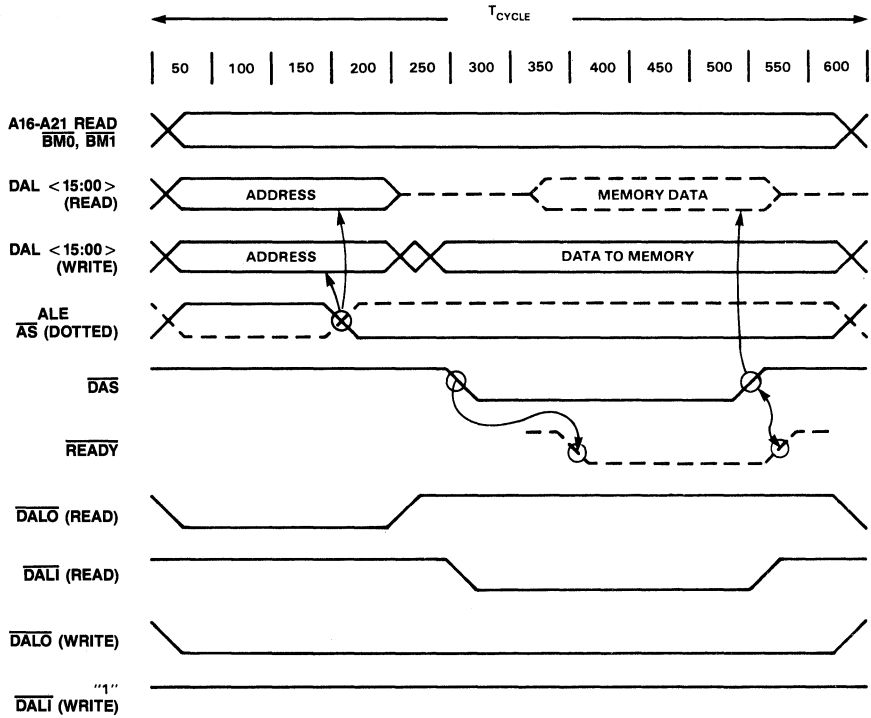


1.3.6.1 READ SEQUENCE

At the beginning of a read cycle, valid addresses are placed on DAL <15:00> and A <23:16>. The BYTE Mask signals ($\overline{BM0}$ and $\overline{BM1}$) become valid at the beginning of this cycle as does READ, indicating the type of cycle. The trailing edge of ALE or $\overline{AS}$ is used to strobe in the addresses A <15:00> into the external latches. Approximately a hundred nanoseconds later, DAL <15:00> go into a tristate mode. There is a fifty nanosecond delay to allow for transceiver turnaround, then $\overline{DAS}$ falls low to signal the beginning of the data portion of the cycle. At this point in the cycle, the LANCE waits for the memory device to assert $\overline{READY}$. Upon assertion of $\overline{READY}$, $\overline{DAS}$ makes a transition from a zero to a one, latching memory data. ($\overline{DAS}$) is low for a minimum of 200 nsec).

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, are used to control the bus transceivers. The $\overline{DALI}$ signal is used to strobe data toward the LANCE and the $\overline{DALO}$ signal is used to strobe data or addresses away from the LANCE. During a read cycle, $\overline{DALO}$ goes inactive before $\overline{DALI}$ goes active to avoid the "spiking" of the bus transceivers.

BUS MASTER TIMING
Figure 10



1.3.6.2 WRITE SEQUENCE

The write cycle begins exactly like a read cycle with the READ line remaining inactive. After ALE or AS pulse, the DAL <15:00> change from addresses to data. DAS goes active when the DAL <15:00> lines are stable. This data will remain valid on the bus until the memory device asserts READY. At this point, DAS goes inactive latching data into the memory device. Data is held for 75 nanoseconds after the deassertion of DAS.

1.3.7 LANCE INTERFACE DESCRIPTION--BUS SLAVE MODE

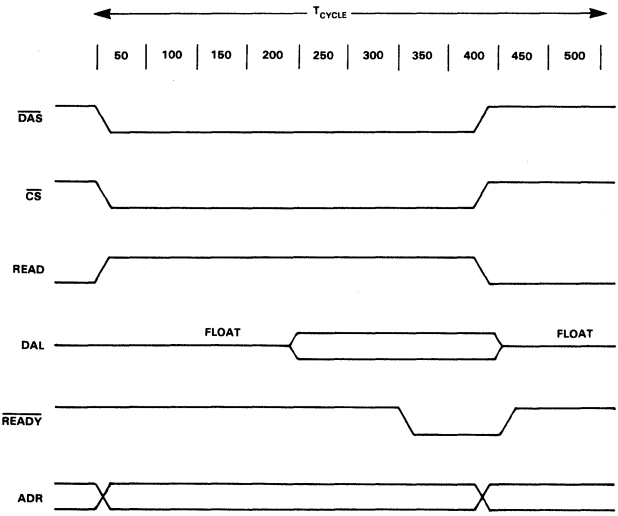
The LANCE enters the Bus Slave Mode whenever CS becomes active. This mode must be entered whenever writing or reading the four status control registers (CSR0, CSR1, CSR2, and CSR3) and the register address pointer (RAP). RAP and CSR0 may be read or written to at any time, but the LANCE must be stopped for CSR1, CSR2, and CSR3 to be written to or read.

1.3.7.1 READ SEQUENCE

CS, READ, and DAS are asserted at the beginning of a read cycle. ADR also must be valid at this time. (If ADR is a "1", the contents of RAP are placed on the DAL lines. Otherwise the contents of the CSR register addressed by RAP are placed on the DAL lines.) After the data on the DAL lines become valid, LANCE asserts READY. CS, READ, DAS, and ADR must remain stable throughout the read cycle. Refer to Figure 11.

BUS SLAVE READ TIMING FOR CSR0, RAP, AND CSR3

Figure 11



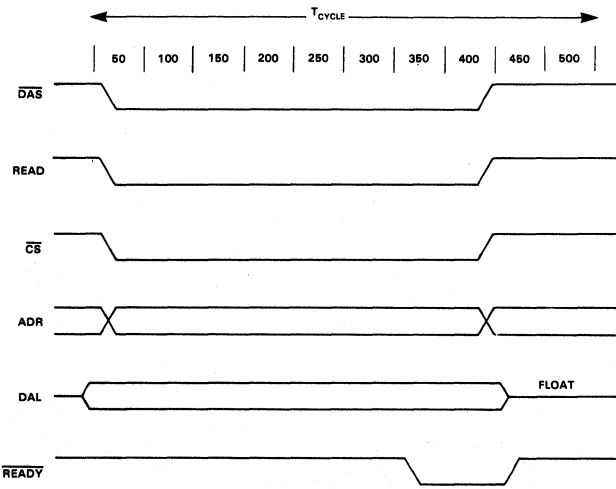
Timing for CSR1 and CSR2 are similar but the DELAY to READY becomes 1250 instead of 350 μs.

1.3.7.2 WRITE SEQUENCE

This cycle is similar to the read cycle, except that during this cycle, READ is not asserted. The DAL buffers are tristated which configures these lines as inputs. The assertion of READY by LANCE indicates to the memory device that the data on the DAL lines has been stored by LANCE in its appropriate CSR register. CS, READ, DAS, ADR, and DAL <15:00> must remain stable throughout the write cycle. Refer to Figure 12.

BUS SLAVE WRITE TIMING FOR CSR0, RAP, AND CSR3

Figure 12



Timing for CSR1 and CSR 2 are similar but the DELAY to READY becomes 1250 instead of 350 μs.

1.3.7.3 REFERENCE DOCUMENTS

The following documents provide a good overview and background for Ethernet. They can be requested from:

Ethernet
Xerox Office Systems Division
Dept. A
3333 Coyote Hills Rd.
Palo Alto, CA 94304

1. The Ethernet, a Local Area Network, Data Link Layer and Physical Layer Specifications--Version 2.0, November 1982.

2. John F. Shoch, An Annotated Bibliography on Local Computer Networks, October 1979.

3. The Ethernet Local Network: Three Reports, February 1980.

4. Internet Transport Protocols, Xerox System Integration Standard, December 1981.

5. Courier: The Remote Procedure Call Protocol, Xerox System Integration Standard, December 1981.

CHAPTER 2
PROGRAMMING SPECIFICATIONS

2.0 INTRODUCTION

2.1 PROGRAMMING SPECIFICATIONS

This section defines the Control and Status Registers and the memory data structures required to program the LANCE Ethernet Protocol Controller.

2.2 PROGRAMMING THE LANCE

The LANCE is designed to operate in an environment that includes close coupling with a local memory and a microprocessor (HOST). The LANCE is programmed by a combination of registers and data structures resident within the LANCE and in memory. There are four Control and Status Registers (CSR's) within the LANCE which are programmed by the HOST device. Once enabled, the LANCE has the ability to access external buffer memory locations to acquire additional operating parameters. LANCE has the ability to do independent buffer management as well as transfer data packets to and from an Ethernet. There are three memory structures accessed by LANCE, as follows:

1. Initialization Block - 12 words in contiguous memory starting on a word boundary. The initialization block is assembled by the HOST, and is accessed by LANCE. The initialization block contains the operating parameters necessary for device operation. The initialization block is comprised of:

    1. Mode of Operation (1 Word)
    2. Physical Address (3 Words)
    3. Logical Address Mask (4 Words)
    4. Location of Receive and Transmit Descriptor Rings (2 Words)
    5. Number of Entries in Receive and Transmit Descriptor Rings (2 Words)

2. Receive and Transmit Descriptor Rings - Two ring structures, one each for incoming and outgoing packets. Each entry in the rings is 4 words long. Each entry must start on a quadword boundary. The Descriptor Rings are comprised of:

    1. The address of a data buffer.
    2. The length of that buffer.
    3. Status information associated with the buffer.

3. Data Buffers - Contiguous portions of memory reserved for packet buffering. Data buffers may begin on arbitrary byte boundaries.

In general, the programming sequence of LANCE may be summarized as:

1. Programming the LANCE CSR's by a HOST device to locate an initialization block in memory.
2. LANCE loading itself with the information contained within the initialization block.
3. LANCE accessing the Descriptor Rings for packet handling.

2.3 CONTROL AND STATUS REGISTERS

There are four Control and Status Registers (CSR's) resident within LANCE. The CSR's are accessed through two bus addressable ports, an address port (RAP), and a data port (RDP).

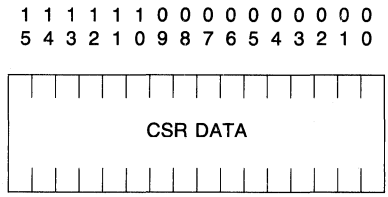
2.3.1 ACCESSING THE CONTROL AND STATUS REGISTERS

The CSR's are read (or written) in a two step operation. The address of the CSR is written into

the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP. Once written, the address in RAP remains unchanged until rewritten. A discrete control input pin (ADR) is provided to distinguish the address port from the data port.

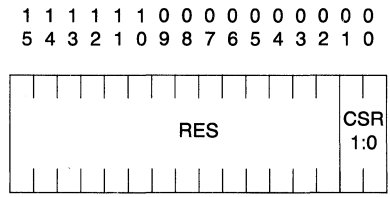
ADR Pin	Port
L	REGISTER DATA PORT (RDP)
H	REGISTER ADDRESS PORT (RAP)

2.3.1.1 REGISTER DATA PORT (RDP)



CSR DATA
Bits 15:00
Writing data to the RDP loads data into the CSR selected by RAP. Reading the data from RDP reads the data from the CSR selected by RAP. CSR1, CSR2 and CSR3 are accessible only when the STOP bit of CSR0 is set. If an attempt to access CSR1, CSR2, or CSR3 is made without the STOP bit being set, LANCE does not respond to the bus transfer. LANCE will assert $\overline{\text{READY}}$, but no data will be transferred either into or out of these registers.

2.3.1.2 REGISTER ADDRESS PORT (RAP)



RES
Bits 15:02
Reserved and read as zeros.

CSR
Bits 01:00
CSR address select bits. READ/WRITE. Selects the CSR to be accessed through the RDP. RAP is cleared by Bus RESET.

CSR<1:0>	CSR
0	CSR0
1	CSR1
2	CSR2
3	CSR3

2.3.2 CONTROL AND STATUS REGISTER DEFINITION

2.3.2.1 CONTROL AND STATUS REGISTER 0 (CSR0)

RAP = 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	BABL	CERR	MISS	MERR	RINT	TINT	IDON	INTR	INEA	RXON	TXON	TDMD	STOP	STRT	INIT

ERR
Bit 15
(Error Summary) Error Summary is set by the 'OR' of BABL, CERR, MISS and MERR. ERR remains set as long as any of the error flags are true. ERR is read only, writing it has no effect. It is cleared by $\overline{\text{RESET}}$ or by setting the stop bit.

BABL
Bit 14
(Babble) BABL is a transmitter timeout error. It indicates that the transmitter has been on longer than the time required to send the maximum length packet. BABL will be set if the number of bytes transmitted exceeds 1518. When BABL is set, an interrupt will be generated if INEA = 1. BABL is READ/CLEAR ONLY and is set by LANCE and cleared by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

CERR
Bit 13
(Collision Error)
Collision Error indicates that the collision input to the chip failed to activate within 2 usec after a chip-initiated transmission was completed. Collision after transmission is a transceiver test feature. CERR is READ/CLEAR ONLY. The chip sets it and clears it by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

MISS
Bit 12
(Missed Packet) Missed Packet is set whenever a packet arrives and passes address recognition, but is lost because the receiver does not own a receive buffer. When MISS is set, an interrupt will be generated if INEA = 1. MISS is READ/CLEAR ONLY and is set by LANCE and cleared by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

MERR
Bit 11
(Memory Error) Memory Error sets when LANCE is the Bus Master and has not received READY within 25.6 μsec after asserting the address on the DAL lines. When a Memory Error is detected, the receiver and transmitter are turned off and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

RINT
Bit 10
(Receiver Interrupt) Receiver Interrupt is set after LANCE updates the last entry in the Receive Descriptor Ring for the completed packet. When RINT is set, an interrupt is generated if INEA = 1. RINT is READ/CLEAR ONLY and is set by LANCE and cleared by writing a "1" into the bit. Writing a "0" has no effect. RESET or setting the STOP bit clears it.

TINT
Bit 09
(Transmitter Interrupt) Transmitter Interrupt is set after LANCE updates the last entry in the Transmit Descriptor Ring for that completed packet. When TINT is set, an interrupt is generated if INEA = 1. TINT is READ/CLEAR ONLY and is set by LANCE and cleared by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

IDON
Bit 08
(Initialization Done) Initialization Done indicates that LANCE has completed the initialization procedure started by setting the INIT bit. When IDON is set, the chip has read the Initialization Block from memory and stored the new parameters. When IDON is set, an interrupt is generated if INEA = 1. IDON is READ/CLEAR ONLY and is set by LANCE and cleared by writing a "1" into the bit. Writing a "0" has no effect. $\overline{\text{RESET}}$ or setting the STOP bit clears it.

INTR
Bit 07
(Interrupt Flag) Interrupt Flag indicates that one or more of the following interrupt causing conditions has occurred: BABL, MISS, MERR, RINT, TINT, IDON. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ output pin will be low. INTR is READ ONLY, writing this bit has no effect. INTR is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit.

INEA
Bit 06
(Interrupt Enable) Interrupt Enable allows the INTR Output pin to be driven low when the Interrupt Flag is set. If INEA = 1 and INTR = 1 the INTR pin will be low. If INEA = 1 and INTR = 1 the INTR pin will be low. If INEA = 0 the INTR pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE set by writing a "1" into this bit and is cleared by writing a "0" into this bit or by $\overline{\text{RESET}}$ or by setting the STOP bit.

RXON
Bit 05
(Receiver On) Receiver On indicates that the receiver is enabled. RXON and IDON are set at the same time, if the DRX bit in the Mode Register is a "0". RXON is cleared by MERR or STOP being set or by RESET. RXON is READ ONLY, writing this bit has no effect. RXON is gated by the STRT bit; thus it will always be read as a "0" until STRT is set.

TXON
Bit 04
(Transmitter On) Transmitter On indicates that the transmitter is enabled. TXON and IDON are set at the same time, if the DTX bit in the Mode Register is "0". TXON is cleared by MERR, or STOP being set, a TRANSMIT UNDERFLOW, or by RESET. TXON is READ ONLY; writing this bit has no effect. TXON is gated by the STRT bit; thus it will always be read as a "0" until STRT is set.

TDMD
Bit 03
(Transmit Demand) When set, Transmit Demand causes LANCE to access the Transmit

Descriptor Ring without waiting for the polltime interval to elapse. (about 1.6 ms). TDMD need not be set to transmit a packet, it merely hastens LANCE's response to a Transmit Descriptor Ring entry insertion by the host. TDMD is WRITE WITH ONE ONLY and microcode clears it after it is used. It may read as a "1" for a short time after it is written because the LANCE microcode may have been busy when TDMD was set. It is also cleared by RESET or by setting the STOP bit. Writing a "0" in this bit has no effect.

STOP
Bit 02
(Stop) STOP disables LANCE from all external activity when set and clears the internal logic. Setting STOP is the equivalent of asserting Bus RESET. LANCE remains inactive and STOP remains set until the STRT or INIT bit is set. If STRT, INIT and STOP are all set together, STOP will override the other bits and only STOP will be set. STOP IS READ/WRITE WITH ONE ONLY and set by RESET. Writing a "0" to this bit has no effect.

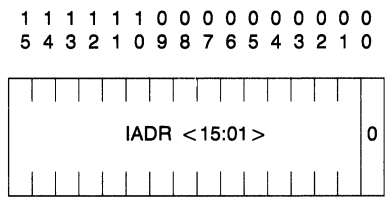
STRT
Bit 01
(Start) Start enables LANCE to send and receive packets, perform direct memory access and do buffer management. If STRT and INIT are set together, the INIT function will be executed first. STRT is READ/WRITE WITH ONE ONLY. Writing a "0" into this bit has no effect. STRT is cleared by RESET or by setting the STOP bit.

INIT
Bit 00
(Initialize) When set, Initialize causes LANCE to begin the initialization procedure and access the Initialization Block. If STRT and INIT are set together, the INIT function is executed first. INIT is READ/WRITE WITH "1" ONLY. Writing a "0" into this bit has no effect. INIT is cleared by RESET or by setting the STOP bit.

2.3.2.2 CONTROL AND STATUS REGISTER 1 (CSR1)

RAP = 1

READ/WRITE: Accessible only when the STOP bit of CSR0 is a ONE. Access at any other time will not be responded to by LANCE. READY will be asserted but no data will be transferred. CSR1 is unaffected by RESET.

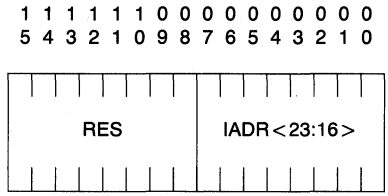


IADR
Bits 15:01
The low order 16 bits of the address of the first word (lowest address) in the Initialization Block. Bit 00 must be zero.

2.3.2.3 CONTROL AND STATUS REGISTER 2 (CSR2)

RAP = 2

READ/WRITE: Accessible only when the STOP bit of CSR0 is a ONE. Access at any other time will not be responded to by LANCE. READY will be asserted but no data will be transferred. CSR2 is unaffected by RESET.



RES
Bits 15:08
Reserved.

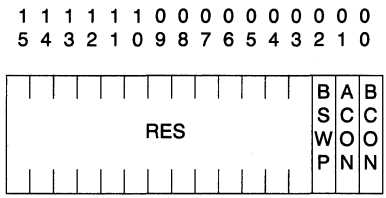
IADR
Bits 07:00
The high order 8 bits of the address of the first word (lowest address in the Initialization Block.

2.3.2.4 CONTROL AND STATUS REGISTER 3 (CSR3)

CSR3 allows redefinition of the Bus Master interface.

RAP = 3

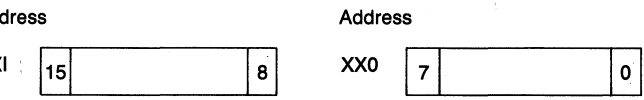
READ/WRITE: Accessible only when the STOP bit of CSR0 is a ONE. Access at any other time will not be responded to by LANCE. $\overline{\text{READY}}$ will be asserted but no data will be transferred. CSR3 is cleared by $\overline{\text{RESET}}$ or by setting the STOP bit in CSR0.



RES
Bits 15:03
Reserved/read as "0".

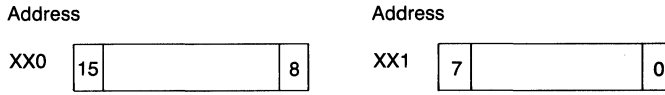
BSWP
Bit 02
(Byte Swap) Byte Swap allows LANCE to operate with memory organizations that have bits <07:00> at even addresses with bits <15:08> at odd addresses or vice versa.

With Byte Swap = 0:



This memory organization is used with the LSI 11 microprocessor and the 8086 microprocessor.

With Byte Swap = 1:



This memory organization is used with the MK68000, MK68200, and Z8000 microprocessors. Only data from SILO transfers are swapped. Initialization Block Data and Ring Descriptor entries are not swapped. BSWP is READ/WRITE and cleared by RESET or by setting the STOP bit in CSR0.

ACON
Bit 01
(ALE Control) ALE Control defines the assertive state of ALE/$\overline{AS}$ when LANCE is a Bus Master. ACON is READ/WRITE and cleared by $\overline{RESET}$ or by setting the STOP bit in CSR0.

ACON	ALE/$\overline{AS}$
0	ASSERTED HIGH (ALE)
1	ASSERTED LOW ($\overline{AS}$)

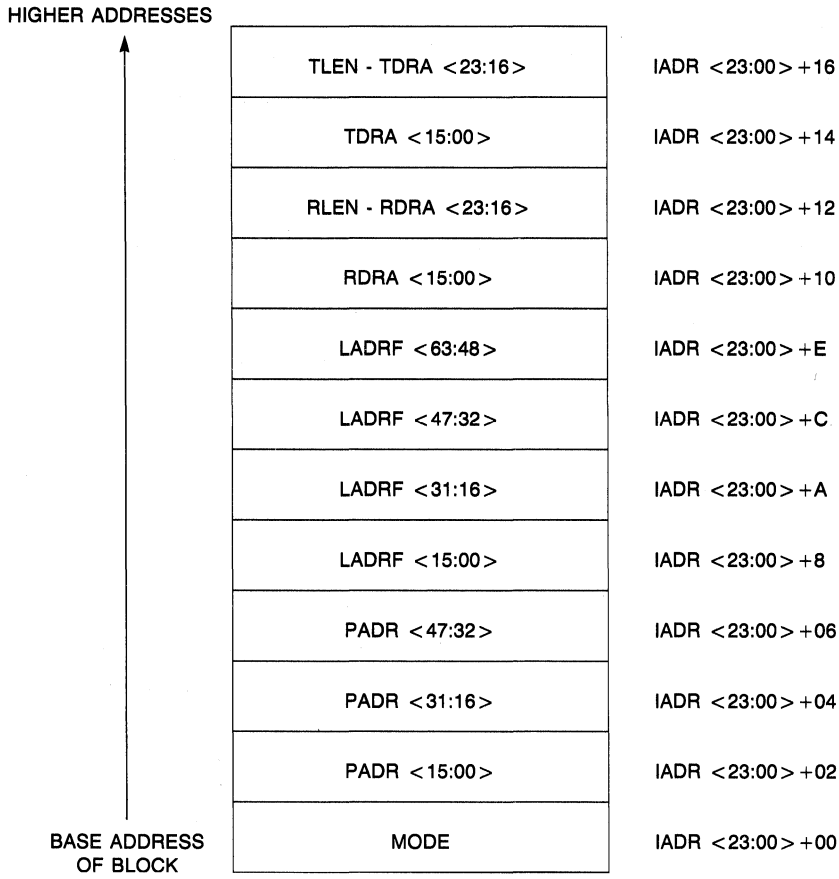
BCON
Bit 00
(Byte Control) Byte Control redefines the Byte Mask and Hold I/O Pins. BCON is READ/WRITE and cleared by $\overline{RESET}$ or by setting the STOP bit in CSR0.

BCON	I/O PIN 16	I/O PIN 15	I/O PIN 17
0	$\overline{BM1}$	$\overline{BM0}$	$\overline{HOLD}$
1	$\overline{BUSAKO}$	BYTE	$\overline{BUSRQ}$

2.4 INITIALIZATION

2.4.1 INITIALIZATION BLOCK

LANCE initialization includes the reading of the initialization block in memory to obtain the operating parameters. The following is a definition of the Initialization Block. The Initialization Block is read by LANCE when the INIT bit in CSR0 is set. The INIT bit should be set before or concurrent with the STRT bit to ensure proper parameter initialization and LANCE operation. After LANCE has read the Initialization Block, IDON is set in CSR0 and an interrupt is generated if INEA = 1.



2.4.1.1 MODE

The Mode Register allows alteration of LANCE's operating parameters. Normal operation is with the Mode Register clear.

IADR <23:00> +00

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PROM	RES								INTL	DRTY	COLL	DTCR	LOOP	DTX	DRX

PROM
Bit 15
(Promiscuous Mode) When PROM = 1, all incoming addresses are accepted. This bit must be set in internal loopback if a physical address is not used.

RES
Bits 14:07
(Reserved)

INTL
Bit 06
(Internal Loopback) Internal Loopback is used with the LOOP bit to determine where the loopback is to be done. Internal loopback allows LANCE to receive its own transmitted packet. Since this represents full duplex operation, the packet size would be limited by the SILO size, which is 48 bytes. However, a SILO full flag is generated after 32 bytes are loaded into the SILO. This limits the transmit buffer size to 32 bytes in internal or extended loopback. With transmit CRC enabled, the LANCE generates the 4-byte CRC code and appends it to the data. Thus, the receive buffer is filled with 36 bytes and the host CPU checks the CRC result. With transmit CRC disabled, the host CPU provides 4 bytes of CRC as part of the 32 bytes in the transmit buffer. The LANCE checks the CRC on reception and transfers only 28 bytes of "data" to the receive buffer. After each Internal Loopback packet, LANCE should be reinitialized.

INTL is only valid if LOOP = 1, otherwise it is ignored.

LOOP	INTL	LOOPBACK
0	X	NO LOOPBACK, NORMAL OPERATION
1	0	EXTERNAL
1	1	INTERNAL

DRTY
Bit 05
(Disable Retry) When DRTY = 1, LANCE attempts only one packet transmission If there is a collision on the first transmission attempt, a Retry Error (RTRY) is reported in Transmit Message Descriptor 3 (TMD3).

COLL
Bit 04
(Force Collision) This bit allows the collision logic to be tested. LANCE must be in internal loopback mode for COLL to be valid. If COLL = 1, a collision will be forced during the subsequent transmission attempt. This will result in 1 or 16 total transmission attempts with a retry error reported in TMD3. The number of attempts depends upon the state of DRTY (Bit (05).

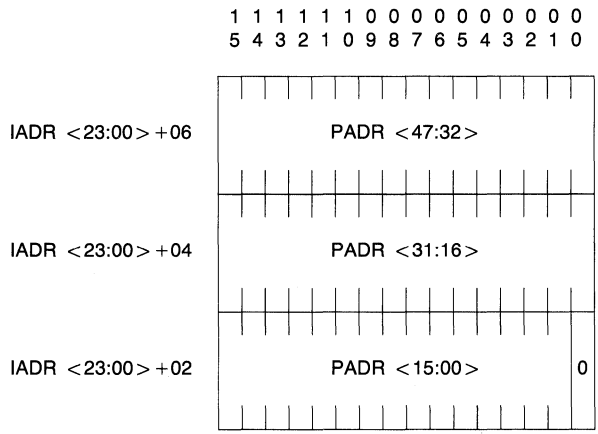
DTCR
Bit 03
(Disable Transmit CRC) When DTCR = 0, the transmitter generates and appends a CRC to the transmitted packet. When DTCR = 1, the CRC logic is allocated to the receiver and no CRC is generated and sent with the transmitted packet. During loopback, DTCR = 0 causes a CRC to be generated on the transmitted packet but the receiver will not perform a CRC check since the CRC logic is shared and cannot generate and check CRC at the same time. The generated CRC is written into memory with the data and can be checked by the host software. If DTCR = 1 during loopback the host software must append a CRC value to the transmit data. The receiver checks the CRC on the received data and reports any errors.

LOOP
Bit 02
(Loopback) Loopback allows LANCE to operate in full duplex mode for test purposes. The maximum packet size is limited to 36 bytes as described above for the INTL bit. During loopback, the runt packet filter is disabled because the maximum packet is forced to be smaller than the minimum size Ethernet packet (64 bytes). LOOP = 1 allows simultaneous transmission and reception for a message constrained to fit within the SILO. The chip waits until the entire message is in the SILO before serial transmission begins. The incoming data stream fills the SILO from behind as it is being emptied. Moving the received message out of the SILO to memory does not begin until reception has ceased. In loopback mode, transmit data chaining is not possible. Receive data chaining is allowed regardless of the receive buffer length. In normal operation, the receive buffers must be 64 bytes long, to allow time for buffer lookahead.

DTX
Bit 01
(Disable the Transmitter) Disable the Transmitter causes LANCE not to access the Transmit Descriptor Ring and therefore no transmissions are attempted. DTX disables TXON from being set when initialization is complete.

DRX
Bit 00
(Disable the Receiver) Disable the Receiver causes LANCE to reject all incoming packets and not access the Receive Descriptor Ring. DRX disables RXON from being set when initialization is complete.

2.4.1.2 PHYSICAL ADDRESS

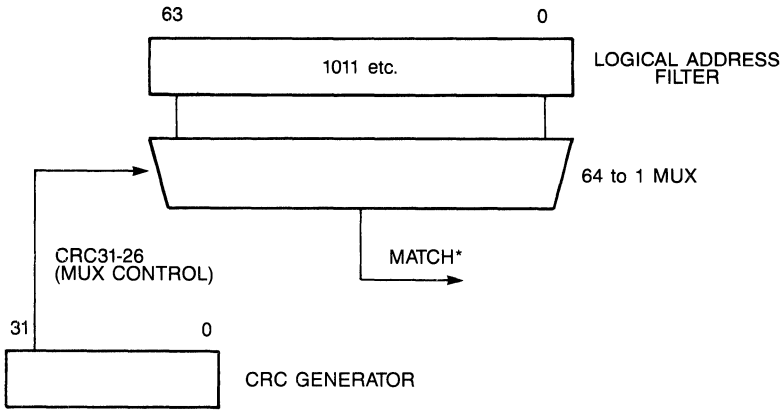


PADR
Bits 47:00
(Physical Address) Physical Address is the unique 48-bit physical address assigned to LANCE. PADR <0> must be zero.

2.4.1.3 LOGICAL ADDRESS FILTER

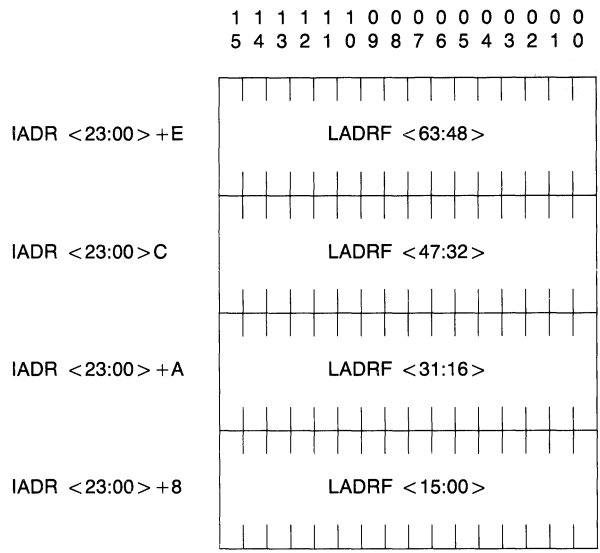
The Logical Address Filter is a 64 bit mask composed of four sixteen bit registers LADRF <63:00> in the initialization block that is used to accept incoming Logical Addresses. This is an imperfect filter that requires the host processor to do the final filtering. The first bit of the incoming address must be a "1" for either the Logical Address Filter or the Broadcast Address decode to be enabled. Otherwise the incoming address is a physical address and is compared against the contents of PADR <47:00> that was loaded through the Initialization Block.

All incoming data goes through the CRC Generator. In the case of a logical address, the six most significant bits of the CRC Generator are strobed into the Hash Register after the 48th bit of the logical address has gone through this circuitry. This 6-bit address then selects one of the 64 bits in the Logical Address Filter. If the mask bit selected is a "1", the address is accepted and the packet will be put into the current receive buffer space. The task of mapping a logical address to one of 64 bit positions is a tedious one that requires a simple computer program to generate the CRC codes for the addresses desired. The Ethernet CRC Polynomial is CRC-32, which is: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$. Figure 13 shows one such mapping. (This is one of 2^{26} possible mappings). Hash Address 00 will select bit 0 and Hash Address 63 will select bit 63.



* If MATCH = 1, the packet is accepted.
If MATCH = 0, the packet is rejected.

The Broadcast address, which is all ones, is decoded independent of the Logical Address Filter (Broadcast Address will also map to bit 47 of the Logical Address Filter). If the Logical Address Filter is loaded with all zeroes, all incoming logical addresses except Broadcast will be rejected.

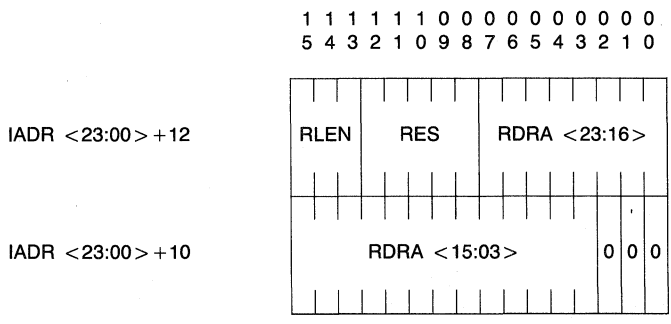


LADRF
Bits 63:00
The 64-bit mask used by LANCE to accept logical addresses.

MAPPING OF LOGICAL ADDRESS TO FILTER MASK
Figure 13

LAF REG BITS SET	LAF LOC. DEC.	DESTINATION ADDRESS ACCEPTED (HEX)	LAF REG. BITS SET	LAF LOC. DEC.	DESTINATION ADDRESS ACCEPTED (HEX)
0	0	FF FF FF FF FF 65	0	32	FF FF FF FF FF D1
	1	FF FF FF FF FF 55		33	FF FF FF FF FF F1
L	2	FF FF FF FF FF 15	L	34	FF FF FF FF FF B1
A	3	FF FF FF FF FF 35	A	35	FF FF FF FF FF 91
F	4	FF FF FF FF FF B5	F	36	FF FF FF FF FF 11
	5	FF FF FF FF FF 95		37	FF FF FF FF FF 31
0	6	FF FF FF FF FF D5	2	38	FF FF FF FF FF 71
	7	FF FF FF FF FF F5		39	FF FF FF FF FF 51
	8	FF FF FF FF FF DB		40	FF FF FF FF FF 7F
	9	FF FF FF FF FF FB		41	FF FF FF FF FF 4F
	10	FF FF FF FF FF BB		42	FF FF FF FF FF 1F
	11	FF FF FF FF FF 8B		43	FF FF FF FF FF 3F
	12	FF FF FF FF FF 0B		44	FF FF FF FF FF BF
	13	FF FF FF FF FF 3B		45	FF FF FF FF FF 9F
	14	FF FF FF FF FF 7B		46	FF FF FF FF FF DF
15	15	FF FF FF FF FF 5B	15	47	FF FF FF FF FF EF
0	16	FF FF FF FF FF 27	0	48	FF FF FF FF FF 93
	17	FF FF FF FF FF 07		49	FF FF FF FF FF B3
	18	FF FF FF FF FF 57		50	FF FF FF FF FF F3
	19	FF FF FF FF FF 77		51	FF FF FF FF FF D3
L	20	FF FF FF FF FF F7	L	52	FF FF FF FF FF 53
A	21	FF FF FF FF FF C7	A	53	FF FF FF FF FF 73
F	22	FF FF FF FF FF 97	F	54	FF FF FF FF FF 23
	23	FF FF FF FF FF A7		55	FF FF FF FF FF 13
1	24	FF FF FF FF FF 99	3	56	FF FF FF FF FF 3D
	25	FF FF FF FF FF B9		57	FF FF FF FF FF 0D
	26	FF FF FF FF FF F9		58	FF FF FF FF FF 5D
	27	FF FF FF FF FF C9		59	FF FF FF FF FF 7D
	28	FF FF FF FF FF 59		60	FF FF FF FF FF FD
	29	FF FF FF FF FF 79		61	FF FF FF FF FF DD
	30	FF FF FF FF FF 29		62	FF FF FF FF FF 9D
15	31	FF FF FF FF FF 19	15	63	FF FF FF FF FF BD

2.4.1.4 RECEIVE DESCRIPTOR RING POINTER



RLEN
Bits 15:13
(Receive Ring Length) Receive Ring Length is the number of entries in the Receive Ring expressed as a power of two.

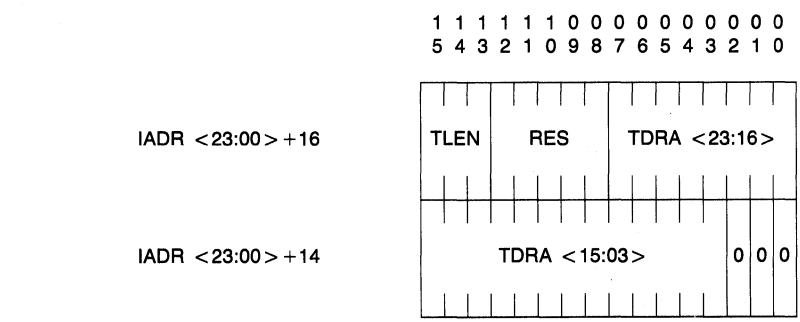
RLEN	NUMBER OF ENTRIES
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

RES
Bits 12:08
(Reserved)

RDRA
Bits 07:00 and 15:03
(Receive Descriptor Ring Address) Receive Descriptor Ring Address is the base address (lowest address) of the Receive Descriptor Ring.

RDRA
Bits 02:00
(Must Be Zeros) These bits are RDRA <02:00> and must be zeroes because the Receive Rings are aligned on quadword boundaries.

2.4.1.5 TRANSMIT DESCRIPTOR RING POINTER



TLEN
Bits 15:13
(Transmit Ring Length) Transmit Ring Length is the number of entries in the Transmit Ring expressed as a power of two.

TLEN	NUMBER OF ENTRIES
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

RES
Bits 12:08
(Reserved)

TDRA
Bits 07:00 and 15:03
(Transmit Descriptor Ring Address) This address is the base address (lowest address) of the Transmit Descriptor Ring.

Bits 02:00
(Must Be Zeros) These bits must be zeroes because the Transmit Rings are aligned on quadword boundaries.

2.5 BUFFER MANAGEMENT

Buffer Management is accomplished through message descriptors organized in ring structures in memory. Each message descriptor entry is four words long. There are two rings allocated for the LANCE:a Receive ring and a Transmit ring. The LANCE is capable of polling each ring for buffers either to empty or fill with packets to or from the channel. The LANCE is also capable of entering status information in the descriptor entry. When polling, LANCE is limited to looking one ahead of the descriptor entry with which it is currently working. The speed of the data stream restricts the receiver buffer size to a minimum of 64 bytes to avoid an overflow when chaining receive buffers. The location of the descriptor rings and their length are found in the initialization block, accessed during the initialization procedure by LANCE. Writing a "ONE" into the STRT bit of CSR0 will cause LANCE to start accessing the descriptor rings and enable it to send and receive packets. The LANCE communicates with a HOST device (probably a microprocessor) through the ring structures in memory. Each entry in the ring is either "owned" by LANCE or the HOST. There is an ownership bit (OWN) in the message descriptor entry. Mutual exclusion is accomplished by a protocol which states that each device can only relinquish ownership of the descriptor entry to the other device; it can never take ownership, and each device cannot change the state of any field in an entry after it has relinquished ownership. When chaining buffers, the minimum transmit buffer size is restricted to 100 bytes (to avoid mutual exclusion violations, which could occur following a collision). Otherwise, LANCE would access a buffer to which it had relinquished ownership (to reinitialize a transmission interrupted by a collision).

2.5.1 DESCRIPTOR RINGS

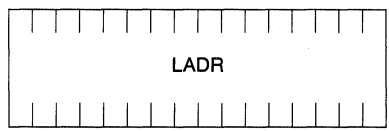
Each descriptor in a ring in memory is a 4 word entry. The following is the format of the receive and the transmit descriptors.

2.5.1.1 RECEIVE MESSAGE DESCRIPTOR ENTRY

2.5.1.1.1 RECEIVE MESSAGE DESCRIPTOR 0 (RMD0)

MEMORY ADDRESS: XXXXXXX0

1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0



LADR
Bits 15:00
The Low Order 16 address bits of the buffer pointed to by this descriptor. LADR is written by the Host and unchanged by LANCE.

2.5.1.1.2 RECEIVE MESSAGE DESCRIPTOR 1 (RMD1)

MEMORY ADDRESS: XXXXXXX2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OWN	ERR	FRAM	OFLO	CRC	BUFF	STP	ENP	HADR							

OWN
Bit 15
This bit indicates that either the Host owns the descriptor entry (OWN = 0) or LANCE owns it (OWN = 1). The chip clears the OWN bit after filling the buffer pointed to by the descriptor entry. The Host sets the OWN bit after emptying the buffer. Once the LANCE or Host relinquishes ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.

ERR
Bit 14
(Error Summary) Error Summary is the "OR" of FRAM, OFLO, CRC or BUFF. ERR is set by LANCE when it releases the buffer and is cleared by the Host.

FRAM
Bit 13
(Framing Error) Framing Error indicates that the incoming packet contained both a non-integer multiple of eight (8) bits and a CRC error. In internal loopback, whenever a CRC error occurs, FRAM will always be set. FRAM is set by LANCE when it releases the buffer and is cleared by the Host.

OFLO
Bit 12
(Overflow) Overflow error indicates that the receiver has lost all or part of the incoming packet due to an inability to store the packet in a memory buffer before the internal SILO overflowed. OFLO is set by LANCE when it releases the buffer and is cleared by the Host.

CRC
Bit 11
CRC indicates that the receiver has detected a CRC error on the incoming packet. CRC is set by LANCE when it releases the buffer and is cleared by the Host.

BUFF
Bit 10
(Buffer Error) Buffer Error is set either when LANCE has utilized all its allocated buffers or if the next status is not acquired in time while data chaining a received packet. BUFF is set by LANCE when it releases the buffer and is cleared by the Host. If a Buffer Error occurs, an Overflow Error also occurs because LANCE tries to acquire the next buffer until the SILO overflows.

STP
Bit 09
(Start of Packet) Start of Packet indicates that this is the first buffer used by LANCE for this packet. It is used for data chaining buffers. STP is set by LANCE when it releases the buffer and is cleared by the Host.

ENP
Bit 08
(End of Packet) End of Packet indicates that this is the last buffer used by LANCE for this packet. It is used for data chaining buffers. If both STP and ENP were set, the packet would fit into one buffer and there was no data chaining. ENP is set by LANCE when it releases the buffer and is cleared by the Host.

HADR
Bits 07:00
The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by LANCE.

2.5.1.1.3 RECEIVE MESSAGE DESCRIPTOR 2 (RMD2)

MEMORY ADDRESS: XXXXXXX4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	1	BCNT											

Bits 15:12
(Must Be Ones) This field is written by the Host and unchanged by LANCE.

BCNT
Bits 11:00
(Buffer Byte Count) Buffer Byte Count is the length of the buffer pointed to by this descriptor expressed as a two's complement number. This field is written by the Host and unchanged by LANCE. The minimum buffer size is 64 bytes.

2.5.1.1.4 RECEIVE MESSAGE DESCRIPTOR 3 (RMD3)

MEMORY ADDRESS: XXXXXXX6

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RES				MCNT											

RES
Bits 15:12
(Reserved) Read as zeroes.

MCNT
Bits 11:00
(Message Byte Count) Message Byte Count is the length in bytes of the received message. MCNT is valid only when ERR is clear and ENP is set. MCNT is written by LANCE and is cleared by the Host. In data chaining, RMD3 is only written to after the last buffer status is updated. Only the status word is updated for intermediate buffers in the data chain.

2.5.1.2 TRANSMIT MESSAGE DESCRIPTOR ENTRY

2.5.1.2.1 TRANSMIT MESSAGE DESCRIPTOR 0 (TMD0)

MEMORY ADDRESS: XXXXXXX0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LADR															

LADR
Bits 15:00
The Low Order 16 address bits of the buffer pointed to by this descriptor. LADR is written by the Host and unchanged by LANCE.

2.5.1.2.2 TRANSMIT MESSAGE DESCRIPTOR 1 (TMD1)

MEMORY ADDRESS: XXXXXXX2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OWN	ERR	RES	MORE	ONE	DEF	STP	ENP	HADR							

OWN
Bit 15
This bit indicates that either the Host owns the descriptor entry (OWN = 0) or LANCE owns it (OWN = 1). The host sets the OWN bit after filling the buffer pointed to by the descriptor. LANCE clears the OWN bit after transmitting the contents of the buffer. Both the Host and LANCE must not alter a descriptor entry after it has relinquished ownership.

ERR
Bit 14
(Error Summary) Error Summary is the "OR" of LCOL, LCAR, UFLO or RTRY. ERR is set by LANCE when it releases the buffer and is cleared by the Host.

RES
Bit 13
(Reserved) LANCE will write this bit with a "0".

MORE
Bit 12
MORE indicates that more than one retry was needed to transmit a packet. MORE is set by LANCE when it releases the buffer and is cleared by the Host.

ONE
Bit 11
ONE indicates that exactly one retry was needed to transmit a packet. ONE is set by LANCE when it releases the buffer and is cleared by the Host. ONE is not valid if LCOL in TMD3 is set.

DEF
Bit 10
(Deferred) Deferred indicates that LANCE had to defer while trying to transmit a packet. This condition occurs when the channel is busy when LANCE is ready to transmit. DEFER is set by LANCE when it releases the buffer and is cleared by the Host.

STP
Bit 09
(Start of Packet) Start of Packet indicates that this is the first buffer to be used by LANCE for this packet. It is used for data chaining buffers. STP is set by the Host and is unchanged by LANCE.

ENP
Bit 08
(End of Packet) End of Packet indicates that this is the last buffer to be used by LANCE for this packet. It is used for data chaining buffers. If both STP and ENP are set, the packet fits into one buffer and there is no data chaining. ENP is set by the Host and is unchanged by LANCE.

HADR
Bits 07:00
The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and is unchanged by LANCE.

2.5.1.2.3 TRANSMIT MESSAGE DESCRIPTOR 2 (TMD2)

MEMORY ADDRESS: XXXXXXX4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	1	BCNT											

ONES
Bits 15:12
(Must Be Ones) This field is set by the Host and unchanged by LANCE.

BCNT
Bits 11:00
(Buffer Byte Count) Buffer Byte Count is the usable length in bytes of the buffer pointed to by this descriptor expressed as a two's complement negative number. This is the number of bytes from this buffer that will be transmitted by LANCE. This field is written by the Host and unchanged by LANCE. The minimum buffer size is 100 bytes when chaining or 64 bytes when not chaining.

2.5.1.2.4 TRANSMIT MESSAGE DESCRIPTOR 3 (TMD3)

TMD3 is valid only if the ERR bit of TMD1 has been set by LANCE.

MEMORY ADDRESS: XXXXXXX6

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BUFF	UFLO	RES	LCOL	LCAR	RTRY	TDR									

BUFF
Bit 15
(Buffer Error) Buffer Error is set by LANCE during transmission when LANCE does not find the ENP flag in the current buffer and does not own the next buffer. BUFF is set by LANCE and cleared by the Host. If a Buffer Error occurs, an Underflow Error will also occur because LANCE tries to read memory data until the SILO is empty. Buffer Error is valid only if UFLO is set.

UFLO
Bit 14
(Underflow Error) Underflow Error indicates that the transmitter has truncated a message due to data late from memory. UFLO indicates that owing to a lack of data from memory, the SILO has emptied before the end of the packet was reached. UFLO is set by LANCE and is cleared by the Host.

RES
Bit 13
Reserved bit. LANCE writes this bit with a "0".

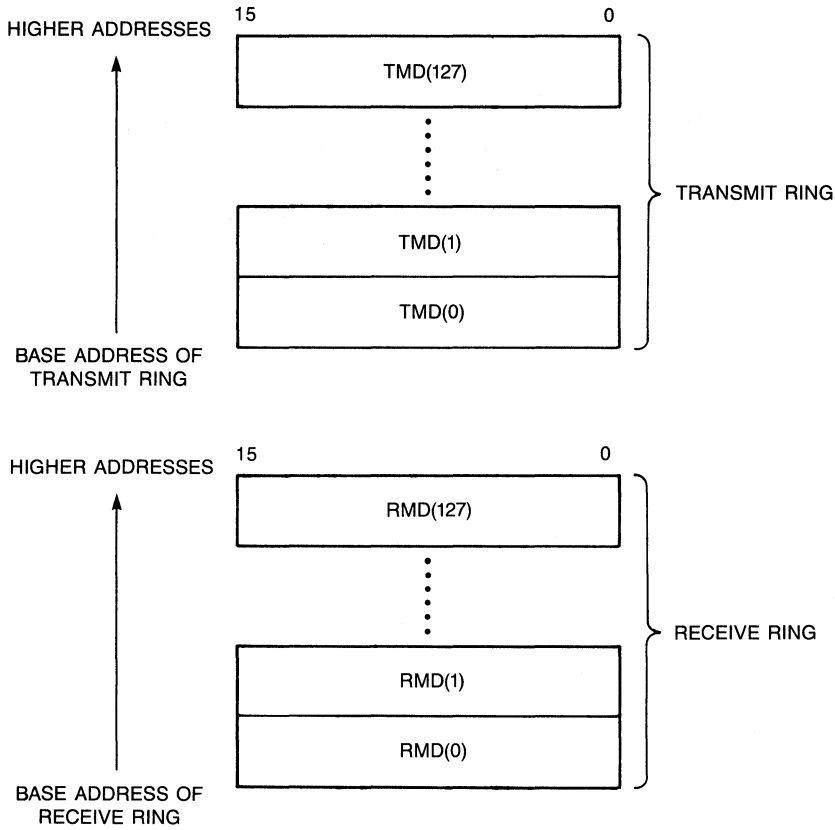
LCOL
Bit 12
(Late Collision) Late Collision indicates that a collision has occurred after the slot time of the channel has elapsed. LANCE does not retry on late collisions. LCOL is set by LANCE and is cleared by the Host.

LCAR
Bit 11
(Loss of Carrier) Loss of Carrier is set when the carrier presence (RENA) input to LANCE goes false during a LANCE-initiated transmission. LANCE does not retry upon Loss of Carrier. LCAR is set by LANCE and is cleared by the Host.

RTRY
Bit 10
(Retry Error) Retry Error indicates that the transmitter has failed in 16 attempts to successfully transmit a message due to repeated collisions on the medium. If DRTY = 1 in the MODE register, RTRY sets after 1 failed transmission attempt. RTRY is set by LANCE and is cleared by the Host.

TDR
Bits 09:00
(Time Domain Relectometry) Time Domain Reflectometry is an internal counter that counts system clocks from the start of a transmission to the occurrence of a collision. This value is useful in determining the approximate distance to a cable fault. The TDR value is written by LANCE and is valid only if RTRY is set.

DESCRIPTOR RINGS IN MEMORY



CHAPTER 3
FUNCTIONAL SPECIFICATIONS

3.0 INTRODUCTION

3.1 FUNCTIONAL DESCRIPTION

This section describes the logical elements used to implement the LANCE Ethernet Controller.

3.2 LOGIC

3.2.1 CLOCK

The LANCE has its clocks derived from a basic free running 10 MHz clock presented to the input pin TCLK. Refer to Section 4 for the clock specification. The microcycle is 200 nanoseconds long, or two basic clock ticks. The microcycle is the basic unit of time in the microsequencer and the control data path. Clock suppression is the act of selectively stretching the microcycle to allow a memory transfer to complete when the Chip is operating as a bus master. Clock suppression can only occur in those microcycles that contain an asserted USUPPRESS bit in the microword register.

3.2.2 MICROSEQUENCER

LANCE is controlled by an internal microprogram. Chained sequencing is used to advance the program address. Each microword contains the address of the next instruction plus any microbranch and trap information required in the program being executed. The microsequencer operates as a one level deep pipeline. As one micro-instruction is being executed, the next is being accessed. The basic microcycle is 200 nanoseconds long, but may be extended on 200 nanosecond boundaries to allow memory transfers to complete. During each microcycle, an address is formed to access the program store which is clocked into the microword register at the end of each cycle.

3.2.3 CONTROL DATA PATH

The Control Data Path contains the hardware necessary to build,control, and store the information required to do buffer management and to control the block transfers of data to and from the silo. The major components in this section of logic are a 24-bit adder, a data shuffler, a constant selector, and a static memory. In this memory resides twelve 24-bit Address Registers and ten 16 bit Status/ Byte Count Registers.

3.2.4 MESSAGE BYTE COUNT

The message byte count is contained in a 12-bit counter. The message byte count keeps track of the number of bytes entering or leaving the Silo under microprogram control for each transmission or reception. The value contained in the message byte count is written into memory through the MDR as part of the reception process. It is also used for the detection of runt packets on reception, and for the detection of babbling transmissions.

3.2.5 RING END FINDERS

The ring end finders, one each for the receive and transmit rings, determine whether the ring address pointers in the CDP RAM are at the end of the rings, and provide a microbranchable signal, which, when true, informs the microprogram to restore the pointers with the beginning address of the rings. The ring end finders are simply a pair of programmable modulo counters, the value of which is loaded at initialization time. The counters are independently incremented under microprogram control.

3.3 BUS CONTROL

3.3.1 BUS ADDRESS REGISTER

The Bus Address register (BA) is 27 bits wide. It is loaded directly from the Data Shuffler under control of a bit in the microword, ENA BA CLK, at the end of the microcycle. At the same time, the bus address is clocked, byte mask and read/write information, associated with the transfer is clocked into a three bit extension of the BA. Clocking of the BA initiates the bus transfer. The upper 8 bits of the BA drive A <23:16> directly. The lower sixteen bits of the BA are multiplexed onto DAL <15:00> during the address portion of the bus cycle when LANCE is the Bus Master. This is an internal register and is not directly addressable by the user.

3.3.2 MEMORY DATA REGISTER

The Memory Data register (MDR) buffers data transfers to and from the I/O bus. The MD is clocked at the end of the microcycle. It is enabled from the ENA MD CLK bit of the microword register. I/O bus data is synchronized to LANCE prior to loading the MDR.

3.3.3 BUS MASTER CONTROL

LANCE becomes a Bus Master for the purposes of acquiring data from the initialization block, buffer management, and the block move of data during the transmission or reception process. The Bus Master Control works in partnership with the microprogram. The microprogram is responsible for loading the BA and MDR for a write transaction, and loading the BA and unloading the MDR for a read transaction. Clocking the BA initiates the transfer. The microprogram also provides a clock suppress enable to stall selectively a microcycle until a memory transaction completes, thus providing synchronization between the microprogram and the Bus Master Control. During block transfer (DMA) of data, memory references overlap. LANCE performs up to 8 data transfers before relinquishing $\overline{\text{HOLD}}$. Refer to Chapter 4 for timing specifications.

3.3.4 MEMORY TIMEOUT

As a Bus Master, LANCE detects and recovers from non-existent memory errors. LANCE waits for a maximum of 25 microseconds for the assertion of $\overline{\text{READY}}$ after it asserts ALE. If LANCE does not receive $\overline{\text{READY}}$ within that time, it sets the MERR bit of CSR0, negates the RXON and TXON bits, and takes no further action unless either the $\overline{\text{RESET}}$ signal is asserted or the STOP bit of CSR0 is asserted.

3.3.5 BUS SLAVE CONTROL

The Bus Slave control is invoked when a memory transaction occurs and the $\overline{\text{CS}}$ pin is asserted. When this happens, it indicates that one of the four LANCE CSR's is being accessed. CSR0 provides visibility into LANCE and is accessed independently of the microprogram. CSR1 and CSR2 hold the address of the initialization block and are resident within the CDP RAM. Accessing CSR1 and CSR2 causes a microtrap for access. The microprogram issues the $\overline{\text{READY}}$ signal for CSR1 and CSR2. The Bus Slave Control independently returns $\overline{\text{READY}}$ for CSR0 and CSR3. CSR 3 allows the I/O pins to be programmed. CSR1, CSR2, and CSR3 are accessible only when the STOP bit of CSR0 is set. Refer to Chapter 4 for timing specifications.

3.3.6 DISCRETE USER APPARENT REGISTERS

Of the register ports and control and status registers, CSR0, CSR3, and RAP are read and written asynchronously from the parallel I/O bus. Refer to Section 2.3 for definitions of the register ports and control and status registers.

3.4 TRANSCEIVER DATA PATH

3.4.1 SERIAL DATA OUTPUT

Serial output data is presented at the TX Output pin by LANCE. The presence of the output

data stream is indicated by the assertion of the TENA level at the Output pin. TX and TENA are synchronous to the internal clock TCLK.

3.4.2 SERIAL DATA INPUT

Serial input data is presented to LANCE at the RX Input pin. The serial input data clock is presented at the RCLK Input pin. The presence of the input data stream is indicated by the assertion of the RENA at its Input pin. RX, RCLK, and RENA are asynchronous to the internal clock TCLK. RCLK is used by LANCE to clock in the input data stream. After the assertion of RENA, LANCE waits 800 nanoseconds before searching for the start bit. If LANCE detects a double ZERO prior to detecting a START bit, LANCE rejects the rest of the packet. Once the Start bit has been detected, LANCE frames the remaining bit stream into byte boundaries, synchronizes the bytes to the internal clock, and loads the Silo if not otherwise disabled.

3.4.3 SILO

The SILO provides buffer storage for the data being transferred between the parallel bus I/O pins and serial bus I/O pins. The capacity of the SILO is 48 bytes. The fall-through time of the SILO is 200 nanoseconds maximum. The SILO has the following capabilities:

1. SILO OPERATION - TRANSMISSION. Data is loaded into the SILO under microprogram control from the MDR. Data from the SILO goes to the serial output shift register.

2. SILO OPERATION - UNDERFLOW. Underflow occurs during Transmission when the output serial shift register requires data to continue an unbroken bit stream output, but data is not available at the output of the SILO, and the last data byte in the frame has been shifted out. Once the SILO has underflowed, the SILO locks out further reads and writes until cleared by the microprogram.

3. SILO OPERATION - RECEPTION. Data is loaded into the SILO from the serial input shift register during Reception. Data leaves the SILO under microprogram control. The destination is the MDR. Preamble is not loaded into the SILO.

4. SILO OPERATION - OVERFLOW. Overflow occurs during Reception when the SILO is filled and data needs to be transferred from the input serial shift register. Once the SILO has overflowed, the SILO locks out further reads and writes until cleared by the microprogram.

5. SILO OPERATION - RESTORE. During Reception, restoring the SILO refers to the action of discarding the 6 bytes of the destination address that have accumulated in the SILO after an address match has been tested and an address match has not occurred. The same action occurs if less than 6 bytes are received before the packet ends. Note that this is different from clearing the SILO since there may be residual data in the SILO from a previous reception which cannot be lost. During the Transmission process, restoring the SILO refers the action of discarding the accumulated Transmit bytes when bit stream transmission has not yet begun and the receiver becomes active.

6. SILO OPERATION - INDEXING. The SILO is capable of holding residual data from a received packet, and accepting data from a second packet. The SILO is able to mark the end of one packet and the beginning of another.

7. SILO OPERATION - CLEARING. The SILO is cleared as part of the recovery for overflow, underflow, and collision. SILO clearing is the action of flushing all data from the SILO unconditionally by clearing the address counters. The SILO is cleared by a discrete microprogram operation.

3.4.4 SILO - MEMORY BYTE ALIGNMENT

Memory buffers may begin and end on arbitrary byte boundaries. Parallel data is byte aligned between the SILO and the MDR. Byte alignment can be reversed by setting the Byte Swap (BSWP) bit in CSR3.

TRANSMISSION - WORD READ FROM EVEN MEMORY ADDRESS

BWSP = 0: SILO BYTE n gets MDR <07:00>
SILO BYTE n + 1 gets MDR <15:08>

BWSP = 1: SILO BYTE n gets MDR <15:08>
SILO BYTE n + 1 gets MDR <07:00>

TRANSMISSION - BYTE READ FROM EVEN MEMORY ADDRESS

BSWP = 0: SILO BYTE n gets MDR <07:00>

BSWP = 1: SILO BYTE n gets MDR <15:08>

TRANSMISSION - BYTE READ FROM ODD MEMORY ADDRESS

BWSP = 0: SILO BYTE n gets MDR <15:08>

BWSP = 1: SILO BYTE n gets MDR <07:00>

RECEPTION - WORD WRITE TO EVEN MEMORY ADDRESS

BSWP = 0: MDR <07:00> gets SILO BYTE n
MDR <15:08> gets SILO BYTE n + 1

BSWP = 1: MDR <15:08> gets SILO BYTE n
MDR <07:00> gets SILO BYTE n + 1

RECEPTION - BYTE WRITE TO EVEN MEMORY ADDRESS

BSWP = 0: MDR <07:00> gets SILO BYTE n
MDR <15:08> - don't care

BSWP = 1: MDR <15:08> gets SILO BYTE n
MDR <07:00> - don't care

RECEPTION - BYTE WRITE TO ODD MEMORY ADDRESS

BSWP = 0: MDR <07:00> - don't care
MDR <15:08> gets SILO BYTE n

BSWP = 1: MDR <15:08> - don't care
MDR <07:00> gets SILO BYTE n

3.4.5 CYCLIC REDUNDANCY CHECK

LANCE utilizes the 32-bit CRC function used in the Autodin-II network. Refer to the Ethernet Specification (section 6.2.4 Frame Check Sequence Field and Appendix C; CRC Implementation) for more detail. LANCE requirements for the CRC logic are the following:

1. TRANSMISSION - MODE <02> LOOP = 0, MODE <03> DTCRC = 0. LANCE calculates the CRC from the first bit following the Start bit to the last bit of the data field. The CRC value is inverted and appended onto the transmission in one unbroken bit stream.

2. RECEPTION - MODE <02> LOOP = 0. LANCE performs a check on the input bit stream from the first bit following the Start bit to the last bit in the frame. LANCE continually samples the state of the CRC check on framed byte boundaries, and, when the incoming bit stream stops, the last sample determines the state of the CRC error. Framing error (FRAM) is not reported if there is no CRC error.

3. LOOPBACK - MODE <02> LOOP = 1, MODE <03> DTRC = 0. LANCE generates and appends the CRC value to the outgoing bit stream as in Transmission but does not check the incoming bit stream.

4. LOOPBACK - MODE <02> LOOP = 1 MODE <03> DTRC = 1. LANCE performs the CRC check on the incoming bit stream as in Reception, but does not generate or append the CRC value to the outgoing bit stream.

3.5 TRANSMISSION

Serial transmission consists of sending an unbroken bit stream from the TX pin consisting of:

1. Preamble / Start bit: 64 alternating ONES and ZEROS terminating in two ONEs. The last ONE is the Start bit.

2. Data: The serialized byte stream from the Silo. Shifted out LSB first.

3. CRC: The inverted 32 bit polynomial calculated from the Data field. CRC is not transmitted if:

    1. Transmission of the Data field is truncated for any reason.

    2. CLSN becomes asserted any time during transmission.

    3. LANCE is in Loopback mode and CRC transmission is disabled (MODE <03> = 1 and MODE <02> = 1).

    4. Mode <03> DTCRC = 1 in a normal transmission mode.

Transmission is indicated at the I/O pin by the assertion of TENA with the first bit of the preamble and the negation of TENA after the last transmitted bit. LANCE starts transmitting the preamble when the following are satisfied.

1. There is at least one byte of data to be transmitted in the Silo.

2. The inter-packet delay has elapsed.

3. The backoff interval has elapsed, if a retransmission.

3.5.1 INTERPACKET DELAY

The interpacket delay is 9.6 to 10.6 microseconds including synchronization. The interpacket delay interval begins after the negation of the RENA signal, LANCE continuously monitors the RENA input pin to monitor or generate an interpacket delay. If LANCE is about to transmit (about to assert the TENA output pin) and RENA is asserted, the chip will not assert TENA until RENA has negated and the interpacket delay has elapsed. Whenever LANCE is about to transmit and is waiting for the interpacket delay to elapse, it will begin transmission immediately after the interpacket delay interval, independent of the state of RENA.

3.5.2 COLLISION DETECTION AND COLLISION JAM

Collisions are detected by monitoring the CLSN input pin. If CLSN becomes asserted during a Frame Transmission, TENA will remain asserted for at least 32 (but not more than 48) additional bit times (including CLSN synchronization). This additional transmission after collision

is referred to as COLLISION JAM. The bit pattern present at the TX output pin is unspecified during COLLISION JAM, but it may not be the 32 bit CRC value corresponding to the (partial) packet transmitted prior to the COLLISION JAM.

If CLSN becomes asserted during the reception of a packet, this reception is immediately terminated. Depending on the timing of collision detection, the following will occur. A collision that occurs within 6 byte times (4.8 microseconds) will result in the packet being rejected because of an address mismatch with the silo write pointer being reset. A collision that occurs within 64 byte times (51.2 microseconds) will result in the packet being rejected since it is a runt packet. A collision that occurs after 64 byte times will result in a truncated packet being written to the memory buffer with the CRC error bit being set in the Status Word of the Receive Ring.

3.5.3 COLLISION BACKOFF

When a transmission attempt has been terminated due to the assertion of CLSN, it is retried by LANCE up to 15 times until successful, or something else aborts the process (memory timeout). The scheduling of the retransmissions is determined by a controlled randomized process called "truncated binary exponential backoff." Upon the negation of the COLLISION JAM interval, LANCE calculates a delay before retransmitting. The delay is an integral multiple of the SLOT TIME. The SLOT TIME is 512 bit times. The number of SLOT TIMEs to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer in the range:

$$0 \leq r < 2^k \qquad \text{where } k = \min(n,10)$$

If all 16 attempts fail, LANCE sets the RTRY bit in the current Transmit Message Descriptor 3 in memory, and steps over the current transmit buffer.

3.5.4 COLLISION - MICROCODE INTERACTION

The microprogram uses the time provided by COLLISION JAM, INTERPACKET DELAY, and the backoff interval to restore the address and byte counts and start loading the Silo in anticipation of retransmission. It is important that LANCE be ready to transmit when the backoff interval elapses in order to utilize the channel properly.

3.5.5 TIME DOMAIN REFLECTOMETRY

LANCE contains a time domain reflectometry counter. The TDR counter is ten bits wide. It counts at a 10 MHz rate. It is cleared by the microprogram and counts upon the assertion of RENA during transmission. Counting ceases if CLSN becomes true. The counter does not wrap around, once all ONEs are reached in the counter, that value is held until cleared. The value in the TDR is written into memory by the microprogram through the MDR. TDR is used to determine the location of suspected cable faults. Transfer from TDR counter into MDR register occurs only if RTRY is set. Normally, when RTRY is not set, the value of TDR will be all zeros.

3.5.6 HEARTBEAT

During the INTERPACKET DELAY following the negation of TENA, the CLSN input is asserted by some Version 1 and all Version 2 transceivers as a self-test. If two microseconds of the INTERPACKET DELAY elapse without CLSN having been asserted, LANCE will set the CERR bit in CSR0 (bit <13>). This function is gated off in the internal loopback mode.

3.6 RECEPTION

Serial reception consists of receiving an unbroken bit stream on the RX I/O pin consisting of:

1. Preamble / Start bit: Two ONES occurring a minimum of 8 bit times after the assertion of RENA. The last ONE is the Start bit.

2. Destination Address: The 48 bits (6 bytes) following the Start bit.

3. Data: The serialized byte stream following the Destination Address. The last four complete bytes of data are the CRC. The Destination Address and the Data are framed into bytes and enter the Silo.

Reception is indicated at the I/O pin by the assertion of RENA and the presence of clock on RCLK while TENA is deasserted.

3.6.1 STATION ADDRESS DETECTION

The station address detect logic checks the destination address of the incoming packet to determine if the packet is addressed to this node. A packet will be accepted if at least one of the following is true:

1. Physical address match: The destination address of the packet exactly matches the physical address of the node.

2. Logical address match: The destination address of the packet is hashed using the CRC. The hash function is used to determine a logical address match.

3. Promiscuous mode: The node accepts all packets regardless of the destination address.

4. Broadcast Detection: The destination address of the packet is the Broadcast Address; all ones.

3.6.1.1 PHYSICAL ADDRESS REGISTER

The physical address register is 48 bits wide and contains the physical address of LANCE. The microprogram loads the physical address from the initialization block through three sequential memory transactions. If the first bit following the Start bit is a ZERO, LANCE will perform a physical address compare. The following 47 bits are compared, bit for bit, for an exact match. If they do not match, LANCE will reject the packet. Bit <00> of the physical address register corresponds to the first bit of the destination address field, and bit <47> of the physical address register corresponds to the last bit of the destination address field.

3.6.1.2 LOGICAL ADDRESS FILTER REGISTER

The logical address filter register is 64 bits wide. The microprogram loads the logical address filter from the initialization block through four sequential memory transactions. If the first bit following the Start bit is a ONE, LANCE will perform a logical address compare. After the last bit of the destination address is clocked into the CRC check logic, the value of CRC 31:26 is used as an index into the logical address filter register. If the bit selected in the register is not a ONE, the chip will reject the packet.

3.6.1.3 PROMISCUOUS MODE

If MODE <15> PROM = 1, LANCE will accept all packets, regardless of the destination address.

3.6.1.4 BROADCAST ADDRESS DETECTION

LANCE will always accept all packets sent to the Broadcast Address of all ones.

3.6.2 RUNT PACKET FILTRATION

If, after loading a buffer, the message byte count is less than 64 bytes, LANCE does not update the ring descriptor entry that pointed to the buffer. Instead LANCE retains the buffer information for use with the next incoming packet. An incoming message must be greater than 64 bytes to be considered a valid packet.

3.7 LOOPBACK

The normal operation of LANCE is as a half duplex device. However, to provide an on-line operational test of LANCE, a pseudo-full duplex mode is provided. In this mode, simultaneous transmission and reception of a loopback packet are enabled with the following constraints:

1. The packet length must be no longer than 32 bytes, exclusive of the CRC.

2. Serial transmission does not begin until the Silo contains the entire output packet.

3. Moving the input packet from the Silo to the memory does not begin until the serial input bit stream terminates.

4. CRC may be generated and appended to the output serial bit stream or may be checked on the input serial bit stream, but not both in the same transaction.

Loopback is controlled by bits <06,03:02> INTL, DTCR, and LOOP of the MODE register. Refer to Section 2.4.1.1 for detailed operation of this register.

3.8 MICROPROGRAM OVERVIEW

3.8.1 SWITCH ROUTINE

Upon power-up, the microprogram finds itself in a routine to evaluate the INIT, STRT, and STOP bits of CSR0. INIT and STRT are cleared and STOP is set by the hardware by $\overline{\text{RESET}}$. Setting either INIT or STRT through an I/O transfer to CSR0 clears STOP. Setting STOP through an I/O transfer clears INIT and STRT. After seeing STOP cleared, the microprogram tests the state of INIT. If set, it branches to the initialization routine, returns, and tests the state of STRT. If INIT is clear and STRT is set, the microprogram goes on to the Polling routine without going to the Initialization routine. If, while the STOP bit is set, an I/O transfer to CSR1 or CSR2 occurs, the microprogram traps to the CSR service routine.

3.8.2 INITIALIZATION ROUTINE

This routine is entered only from the switch routine upon the setting of the INIT bit. Its function is to load LANCE with the data from the initialization block in memory. The routine accesses the initialization block through the address loaded into the CDP RAM by a trap to CSR1 and CSR2 that should have occurred prior to the INIT bit being set. This routine simply sequentially reads the initialization block and stores the information away in the appropriate elements of LANCE. When done, the microcode returns to the switch routine.

3.8.3 POLLING ROUTINE

This routine is entered from:

1. The switch routine upon the setting of the STRT bit.

2. The receive routine after a packet has been received.

3. The transmit routine after a packet has been transmitted.

4. The transmit routine after a Transmission Abort occurs.

5. The memory error trap routine after the trap is serviced.

The routine begins by testing to see if the receiver is disabled, and, if not, tests the current receiver buffer ownership bit to see if it owns a buffer. If LANCE had not acquired a buffer previously, the microprogram goes to the receiver polling routine to acquire one. When the microprogram returns from the receive polling routine, or if LANCE had acquired a buffer previously, it tests

to see if the transmitter is disabled, and, if not, goes to the transmit polling routine to test if there is a buffer to be transmitted. When the microprogram returns from the transmit polling routine, the microprogram enters a timing loop, and repeats the routine upon timeout (above 1.6 ms). Setting the TDMD bit in CSR0 overrides the timing loop. This forces the microprogram to fall through the wait loop. The TDMD bit is cleared immediately after leaving the wait loop. Therefore, to be effective, TDMD should be set after a buffer has been inserted on the transmit ring.

During this routine, should the receiver become active, the microprogram traps to the receive routine.

3.8.4 RECEIVE POLLING ROUTINE

This routine is entered if the receiver is enabled, and LANCE needs a free buffer. The routine begins by the microprogram performing a memory transaction to get a buffer status word from the receive descriptor ring. After acquiring the word, it tests to see if it owns the buffer. If not, the microprogram returns to the polling routine. If it does, the microprogram proceeds to acquire two additional words to obtain the rest of the buffer address and byte count. It then returns to the polling routine with the three words stored in the CDP RAM. The trap to the receive routine is enabled in this routine.

3.8.5 RECEIVE ROUTINE

The receive routine is entered when the receiver is enabled and an incoming packet address has been detected as a match. The routine is divided into three sections of code, an initialization section, a buffer lookahead section, and a descriptor update section. In the initialization section, the microprogram first tests to see if it has acquired a free buffer. If not, it makes one attempt to get the status, address, and byte count from memory. LANCE backs up the address and byte count in the CDP RAM for runt packet recovery, and proceeds to the lookahead section. In the lookahead section, the microprogram tries to acquire an additional buffer by memory transactions with the ring buffer descriptors. If it acquires one, it stores it in the CDP RAM, and waits for byte count overflow or the frame to terminate. In this section the receive DMA trap is enabled. The descriptor update section is entered when byte count overflow has occurred or the message has ended. The code section begins with a test to determine if the message has completed, if data chaining needs to be done, or if a runt packet has been encountered. If a runt packet has been encountered, the microprogram restores the address and byte count and goes to the polling routine. If the incoming message has terminated, the microprogram writes the message length into the ring descriptor entry, writes the status information into the ring descriptor entry, puts the next buffer status information it acquired in the lookahead code in the current buffer status area of the CDP RAM, advances the ring pointer, and goes to polling. If the byte count has overflowed, but the message has not ended, chaining is required. The microprogram releases the buffer by writing the status information into the ring descriptor entry, puts the next buffer status information it acquired in the lookahead code in the current buffer status area of the CDP RAM, advances the ring pointer, and returns to the lookahead code section.

3.8.6 RECEIVE DMA ROUTINE

The Receive DMA routine is entered whenever there are 16 or more bytes of data in the SILO for transfer to memory during receive. The routine is also entered when there are less than 16 bytes in the SILO and the receiver has gone inactive. This is to allow the SILO to empty at the end of reception. Once entered, the Receive DMA routine transfers 16 bytes of data to memory by doing 8 word transfers. These transfers are done on a single memory bus acquisition. This means that LANCE will arbitrate through the HOLD-HOLD ACKNOWLEDGE sequence and then keep HOLD asserted for the duration of 8 transfers. The READY signal from the bus slave device controls the individual word transfers.

If the memory buffer starts on an odd address boundary, the first transfer is 1 byte rather than 1 word (2 bytes). This routine is also used to transfer less than 16 bytes at the end of a reception depending upon the packet size, buffer addresses and data chaining.

NOTE:
DMA (direct memory access) is performed each time LANCE initiates a memory transfer. However, in this document, DMA refers only to those transfers between the SILO and Bus memory.

This routine is entered through a microtrap in the lookahead section of the receive routine. The function of the routine is to move data out of the SILO to local memory. The trap is active when there are 16 or more bytes of data in the SILO and SILO overflow has not occurred or when the incoming message has terminated with data in the SILO. The routine pipelines the data through the Memory Data register while the address and byte counts are incremented in the control data path. A memory timeout will cause a trap. The routine is exited through the URETURN register to the code section that originally trapped to this routine.

3.8.7 TRANSMIT POLLING ROUTINE

The transmit polling routine is entered from the polling routine to determine if a message has been scheduled on the transmit descriptor ring. The routine begins by testing the status word of the ring descriptor entry. The routine tests the ownership of the ring buffer by reading the status word in the ring descriptor. If LANCE does not own the buffer, the microprogram returns to the polling routine. If it does own the buffer, this indicates that a message is to be transmitted, and the microprogram performs memory transactions to acquire and store the address and byte count of the buffer in the CDP RAM. It then goes to the transmit routine to allow transmission of the buffer. The receive active trap is enabled during this routine to allow for processing of an incoming packet and termination of the transmit process.

3.8.8 TRANSMIT ROUTINE

The transmit routine is entered from the transmit polling routine when the microcode finds a buffer that it owns, indicating that a message is scheduled to be transmitted. The routine is divided into three sections of code: an initialization section, a buffer lookahead section, and a descriptor update section. Upon entering the initialization section, the first thing the microprogram does is back up the buffer address and byte count in the event of a retry. It then enables the DMA engine to start filling the SILO and send the preamble. It then enters a wait loop until the transmitter is actually sending the bit stream. It then proceeds to the lookahead section. In the lookahead section, the microprogram tests to determine if the current buffer it is transmitting has been marked with the end of packet flag. If so, data chaining is not required. The microprogram enters a wait loop for byte count overflow. If the end of packet flag is not set, the microprogram attempts to obtain the next buffer descriptor status, address, and byte count before entering the wait loop. When byte count overflow does occur, the microprogram enters the descriptor update section. In the descriptor update section, the microprogram first determines if an error has occurred or, simply, if data chaining must be performed. If an error needs to be reported, an error status word is written into the ring descriptor prior to writing the status word containing the "OWN" bit which releases the buffer. If no error is to be reported, the single word containing the "OWN" bit is written. The microprogram returns to the polling section if the "ENP" flag is found. Otherwise the microprogram returns to the lookahead section.

3.8.9 TRANSMIT DMA ROUTINE

This routine is entered through a microtrap in the lookahead section of the transmit routine. The function of the routine is to move data out of local memory into the SILO. The trap is active when there are 16 or more free locations in the SILO and SILO underflow has not occurred. The routine pipelines the data through the Memory Data register while the address and byte counts are incremented in the Control Data Path. A memory timeout will cause a trap. After a maximum of eight (8) words have been transferred into the SILO, the routine is exited through the URETURN register to the code section that originally trapped to this routine.

3.8.10 COLLISION TRAP ROUTINE

This routine is entered when a collision has been detected while the transmitter is active. The buffer address and byte counts are restored and the microprogram proceeds to the transmit routine to reschedule the transmission. This is the rule if less than 15 retransmissions have occurred. If 15 retransmissions have occurred, the microprogram goes instead to the error reporting code in the descriptor update section.

3.8.11 CSR TRAP ROUTINE

The CSR trap routine is entered only during the switch routine when the STOP bit of CSR0 is set. The function of the routine is to allow the access of CSR1 and CSR2 through an I/O transaction. The routine determines which CSR is being accessed, read or written, moves the data between the MDR and the CDP RAM, and generates a $\overline{\text{READY}}$ signal. The routine is exited through the URETURN register.

3.8.12 MEMORY TIMEOUT TRAP ROUTINE

This trap is invoked whenever a memory transfer times out. The routine sets the STOP bit of CSR0 and returns the microprogram to the start of the switch routine.

3.8.13 RETRY TRAP ROUTINE

This routine is entered when a collision has been detected. The buffer address pointer is restored and the SILO is cleared to restore the READ and WRITE pointers. If there was a TX error, it indicates that 15 retransmissions have occurred (16 total attempts) or that the Disable Retry bit (DRTY) is set in the Mode register. The microprogram then writes the status into the transmit descriptor ring.

If there was no TX error, the byte count is restored and the microprogram returns to the start of the transmit routine to attempt another transmission.

3.8.14 DATA CHAIN

If Byte Count Equal 0 becomes true, it indicates that the receive buffer is full and the packet is not yet finished, which is the data chain case. The microprogram updates the receive status in the descriptor ring. It then checks the next OWN bit. If next OWN is false, which would be the case if there was only one buffer or if there was more than one buffer but the chip did not own the next one, the microprogram waits for RX Active to go false. This indicates that no more data is arriving from the Ethernet. When RX Active goes false, the current RX OWN bit is cleared because the ring entry has just been used for the updated receive status. The SILO is then cleared to restore the READ and WRITE pointers, RX Clear is issued and the microprogram returns to the Polling routine.

If LANCE owned the next buffer, the current receive buffer parameters in the CDP Ram are updated from the next receive buffer parameters that had previously been loaded into the CDP Ram. The microprogram then checks for the end of the ring and updates the address pointers accordingly. The microprogram then goes through the receive buffer lookahead microprogram once to try to acquire another receive buffer if one is available. The microprogram finally returns to the wait loop until either RX Done, SILO overflow or receive buffer overflow becomes true. When RX Done or SILO Overflow occurs, the microcode sets the RINT bit in CSR0. The flow from this point is the same as described elsewhere.

CHAPTER 4
ELECTRICAL SPECIFICATIONS

4.0 ELECTRICAL SPECIFICATIONS

This chapter provides tabular presentations for Absolute Maximum Ratings, DC Characteristics, Capacitance, and AC Timing Specifications. In addition, illustrations are provided for an Output Load Diagram and for Serial Link, Bus Master, and LANCE Bus Slave Timing Diagrams.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −25°C to +100°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −.7 V to +7 V
Power Dissipation ..... 2.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A=0°C to 70°C, V_{CC} = +5 V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{IL}		−0.5	+0.8	V
V_{IH}		+2.0	V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA		+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA	+2.4		V
I_{IL}	@ V_{in} = 0.4 to V_{CC}		±10	μA

CAPACITANCE

F=1 MHz

SYMBOL	PARAMETER	MIN	MAX	UNITS
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIOS	MIN (ns)	TYP (ns)	MAX (ns)
1	TCLK	T_{TCT}	TCLK period		99		101
2	TCLK	T_{TCL}	TCLK low time		45		55
3	TCLK	T_{TCH}	TCLK high time		45		55
4	TCLK	T_{TCR}	Rise time of TCLK		0		8
5	TCLK	T_{TCF}	Fall time of TCLK		0		8
6	TENA	T_{TEP}	TENA propagation delay after the rising edge of TCLK	CL = 50 pf			75
7	TENA	T_{TEH}	TENA hold time after the rising edge of TCLK	CL = 50 pf	5		

AC TIMING SPECIFICATIONS (CONTINUED)

T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
8	TX	T_{TDP}	TX data propagation delay after the rising edge of TCLK	CL=50 pf			75
9	TX	T_{TDH}	TX data hold time after the rising edge of TCLK	CL=50 pf	5		
10	RCLK	T_{RCT}	RCLK period		85		118
11	RCLK	T_{RCH}	RCLK high time		38		
12	RCLK	T_{RCL}	RCLK low time		38		
13	RCLK	T_{RCR}	Rise time of RCLK		0		8
14	RCLK	T_{RCF}	Fall time of RCLK		0		8
15	RX	T_{RDR}	RX data rise time		0		8
16	RX	T_{RDF}	RX data fall time		0		8
17	RX	T_{RDH}	RX data hold time (RCLK to RX data change)		5		
18	RX (See note)	T_{RDS}	RX data setup time (RX data stable to the rising edge of RCLK)		See Note		
19	RENA	T_{DPL}	RENA low time		120		
20	RENA	T_{RENH}	RENA Hold time after rising edge of RCLK		40		
21	CLSN	T_{CPH}	CLSN high time		80		
22	A/DAL	T_{DOFF}	Bus master driver disable after rising edge of $\overline{HOLD}$		0		50
23	A/DAL	T_{DON}	Bus master driver enable after falling edge of $\overline{HLDA}$		0		150
24	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (Bus master)		0		
25	$\overline{RESET}$	T_{RW}	RESET pulse width low		200		
26	A/DAL	T_{CYCLE}	Read/write, address/data cycle time		600		
27	A	T_{XAS}	Address setup time to the falling edge of ALE		75		
28	A	T_{XAH}	Address hold time after the rising edge of $\overline{DAS}$		35		
29	DAL	T_{AS}	Address setup time to the falling edge of ALE		75		
30	DAL	T_{AH}	Address hold time after the falling edge of ALE		35		
31	DAL	T_{RDAS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master read)		50		

NOTE: T_{RDS} (min) = T_{RCT} −25ns i.e. T_{RCT} = 100ns, then T_{RDS} (min) = 75 ns.

AC TIMING SPECIFICATIONS (CONTINUED)

T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

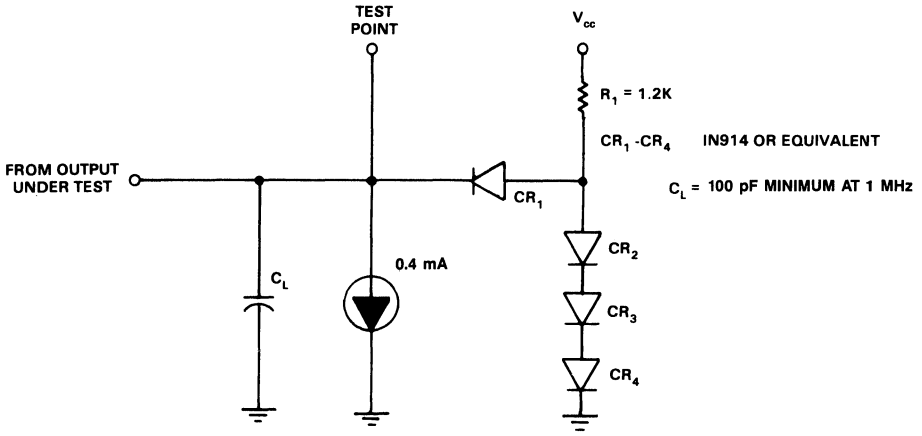
NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
32	DAL	T_{RDAH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
33	DAL	T_{DDAS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus master write)		0		
34	DAL	T_{WDS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master write)		200		
35	DAL	T_{WDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)		35		
36	DAL	T_{SDO1}	Data driver delay after the falling edge of $\overline{DAS}$ (Bus slave read)	(CSR 0,3, RAP)		400	
37	DAL	T_{SDO2}	Data driver delay after the falling edge of $\overline{DAS}$ (Bus slave read)	(CSR 1,2)		1200	
38	DAL	T_{SRDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)		0		35
39	DAL	T_{SWDH}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
40	DAL	T_{SWDS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
41	ALE	T_{ALEW}	ALE width high		120		150
42	ALE	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
43	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width low		200		
44	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		130
45	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (BUS master read)		15		
46	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	Taryd= 300 ns	75		250
47	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (Bus master read)		15		
48	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$(Bus master read)		135		
49	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
50	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (Bus master read)		55		
51	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of ALE (Bus master read)		110		
52	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (Bus master read)		35		
53	$\overline{DALO}$	T_{WDSI}	Delay from the rising edge of $\overline{DAS}$ to the rising edge of $\overline{DALO}$ (Bus master write)		35		

AC TIMING SPECIFICATIONS (CONTINUED)
T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

NO.	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN (ns)	TYP (ns)	MAX (ns)
54	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
55	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
56	ADR	T_{SAH}	$\overline{ADR}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
57	ADR	T_{SAS}	$\overline{ADR}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
58	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle time (600 ns)				80
59	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (Bus slave read)		75		
60	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus master)		0		
61	$\overline{READY}$	T_{SRO1}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 0,3, RAP)		600	
62	$\overline{READY}$	T_{SRO2}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 1,2)		1400	
63	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		35
64	READ	T_{SRH}	$\overline{READ}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
65	READ	T_{SRS}	$\overline{READ}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		

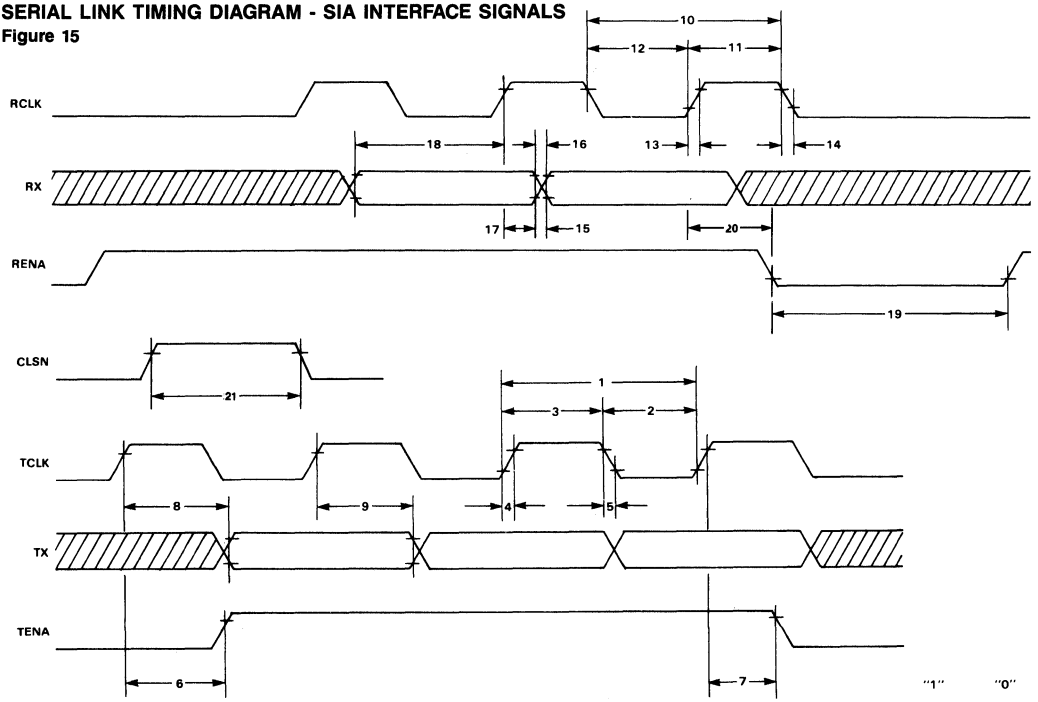
OUTPUT LOAD DIAGRAM

Figure 14



SERIAL LINK TIMING DIAGRAM - SIA INTERFACE SIGNALS

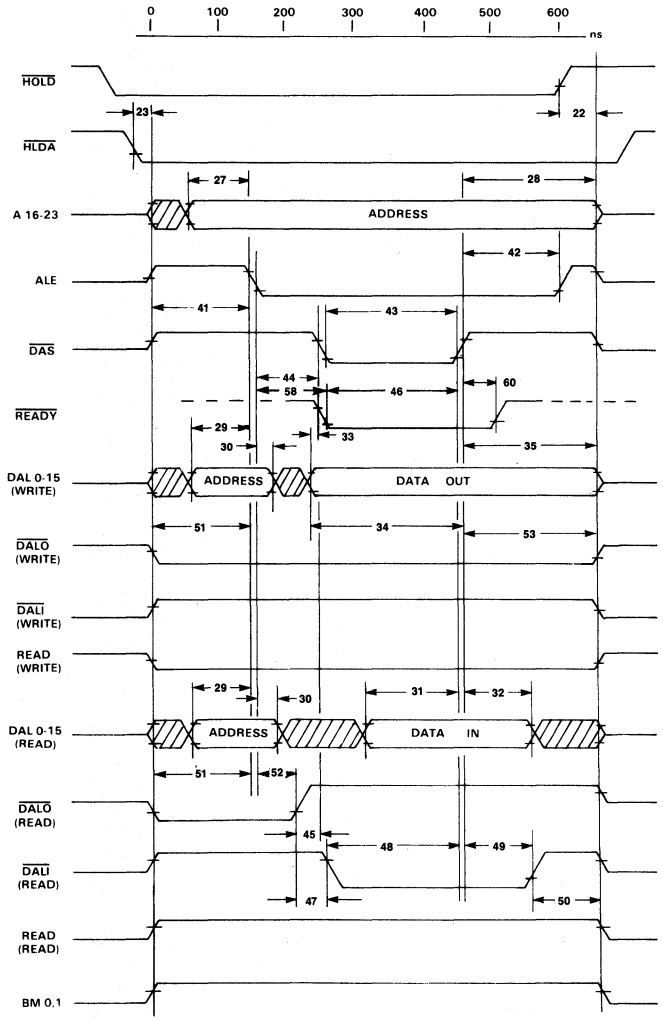
Figure 15



Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8V
FLOAT	V	0.5 V

BUS MASTER TIMING DIAGRAM
Figure 16



NOTE:
The Bus Master cycle time will increase from a minimum of 600 ns in 100 ns steps until the slave device returns $\overline{\text{READY}}$.

LANCE BUS SLAVE TIMING DIAGRAM
Figure 17