Signetics

SCB68154
Interrupt Generator

Preliminary Specification

Microprocessor Products

DESCRIPTION

The Signetics SCB68154/8X825 Interrupt Generator provides an interface between an interrupting device and a system bus such as the VMEbus or VERSAbus™. Figure 1 shows a typical configuration of the SCB68154/8X825. The SCB68154/8X825 has three primary functions:

1. Generates bus interrupt requests.
2. Resides in the interrupt acknowledge daisy-chain.
3. Allows a status/ID byte (interrupt vector) to be supplied to the system if needed.

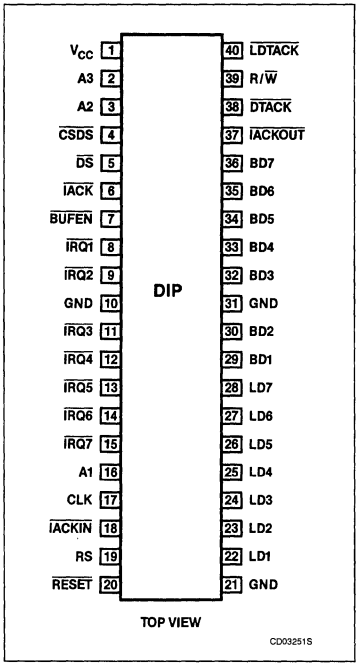
The SCB68154/8X825 has seven interrupt request levels, $\overline{IRQ7}$ – $\overline{IRQ1}$, which are selected by using the interrupt request register. The local master writes to the interrupt request register to generate an interrupt request on any interrupt request level. The interrupt request register may be read to determine if an interrupt has been acknowledged. If a level with an interrupt request pending is acknowledged, the SCB68154/8X825 will allow a status/ID byte to be supplied to the system. Seven bits of the status/ID byte come from the interrupt vector register with the user externally supplying the LSB. If the SCB68154/8X825 does not have an interrupt on the level acknowledged, the SCB68154/8X825 will pass the interrupt acknowledge on via the interrupt acknowledge daisy-chain output. The user can enable all interrupt request levels and clear all interrupt request levels by setting specific bits in the interrupt vector register.

The SCB68154/8X825 was designed primarily for interface to the VMEbus. For more information regarding the protocol definitions, proper use, and application of this device, refer to the VMEbus Specification Manual.

FEATURES

- **Interrupts generator for VMEbus and VERSAbus systems**
- **Generates 7 bus interrupt requests**
- **Two internal registers for system control**
- **Interrupt enable and interrupt clear bits**
- **Allows status/ID byte to be supplied during interrupt acknowledge**
- **High speed bipolar technology**
- **Single +5V supply**

PIN CONFIGURATION



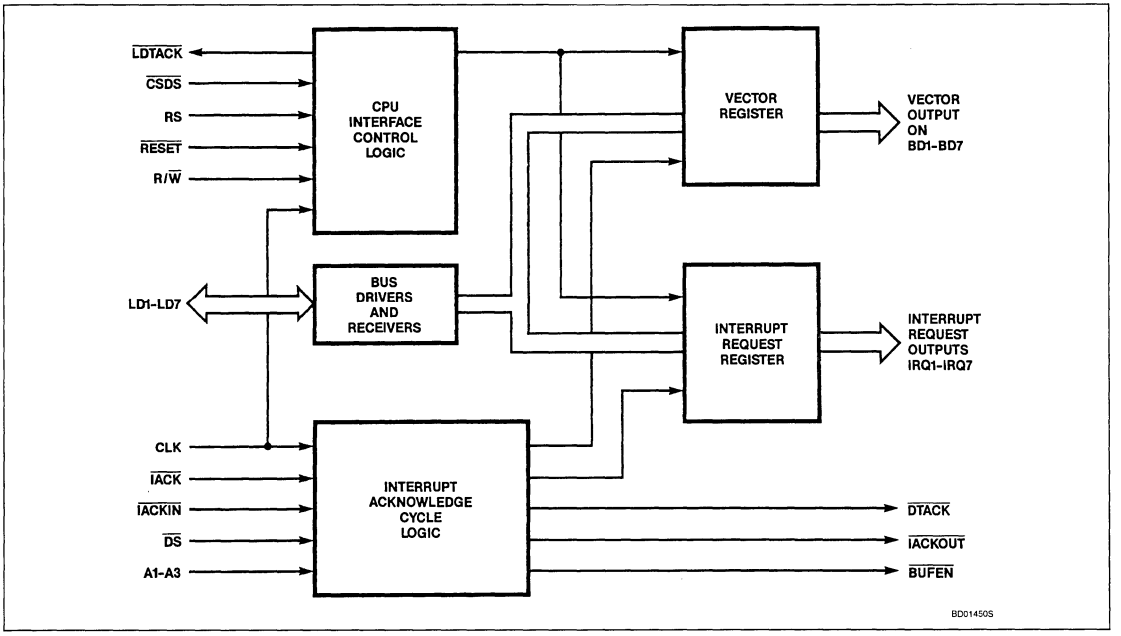
VERSAbus is a registered trademark of Motorola, Inc.

Interrupt Generator SCB68154

ORDERING CODE

PACKAGES	V_{CC} = 5V ± 5%, T_A = 0°C to 70°C
Ceramic DIP	SCB68154C2I40
Plastic DIP	SCB68154C2N40

BLOCK DIAGRAM



Interrupt Generator | SCB68154

PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
V_{CC}	1	I	**Supply Voltage:** + 5V power supply
A1 – A3	16, 3, 2	I	**Address Lines:** Address inputs from system bus. The internal level being acknowledged is encoded on these inputs. A1 is LSB.
$\overline{CSDS}$	4	I	**Chip Select:** Active low chip select input for register I/O. This input must be qualified by the local master's data strobe prior to input (see figure 1).
$\overline{DS}$	5	I	**Data Strobe:** Active low data strobe input from the system used to enable interrupt vector output.
$\overline{IACK}$	6	I	**Interrupt Acknowledge:** Active low interrupt acknowledge input from the system bus.
$\overline{BUFEN}$	7	O	**Buffer Enable:** Active low totem pole output to enable the data buffer required to drive the outputs of the bus data pins (BD1 – BD7).
$\overline{IRQ1}$ – $\overline{IRQ7}$	8, 9, 11 – 15	O	**Interrupt Request:** Active low totem pole system interrupt request output.
GND	10, 21, 31	I	**Ground**
CLK	17	I	**Clock:** Clock input (typically CPU clock).
$\overline{IACKIN}$	18	I	**Interrupt Acknowledge In:** Active low interrupt acknowledge daisy-chain input.
RS	19	I	**Register Select:** Register select input.
$\overline{RESET}$	20	I	**Reset:** Active low input resets all internal registers, $\overline{IACKOUT}$, and $\overline{IRQn}$.
LD1 – LD7	22 – 28	I/O	**Local Data:** Three state local data bus.
BD1 – BD7	29, 30, 32 – 36	O	**Bus Data:** Three state data pins used for vector output.
$\overline{IACKOUT}$	37	O	**Interrupt Acknowledge Out:** Active low totem pole interrupt acknowledge daisy-chain output.
$\overline{DTACK}$	38	O	**Data Transfer Acknowledge:** Active low, totem pole output. This signal indicates that valid data is available on the bus during interrupt acknowledge cycle.
R/$\overline{W}$	39	I	**Read/Write:** Register read/write input. This signal specifies the data transfer cycle in process is to be either read or write.
$\overline{LDTACK}$	40	O	**Local Data Transfer Acknowledge:** Active low, open collector, data transfer acknowledge output to the local bus.

FUNCTIONAL DESCRIPTION

Typical Configuration

The SCB68154/8X825 provides a vehicle for interprocessor communications on an intelligent peripheral controller board, or a CPU board as shown in Figure 1. The local data pins (LD1 – LD7) serve as a local data bus. This allows the local master to access the Interrupt Generator's two internal registers. During an interrupt acknowledge, the SCB68154/8X825 will allow for a status/ID byte to be supplied to the system. The SCB68154/8X825 supplies seven of the eight needed status/ID bits. The user is allowed to externally supply the least significant bit (LSB), typically the system address line A1 of the status/ID byte. The $\overline{IRQ1}$ – $\overline{IRQ7}$, $\overline{DTACK}$, and BD1 – BD7 outputs require external buffers to provide adequate drive to the system bus. $\overline{BUFEN}$ provides the output enable control for the data buffer that is required for BD1 – BD7.

Register Selection

The SCB68154/8X825 has two internal registers which can be programmed for system control. They are the interrupt vector register and the interrupt request register. Figure 2 shows the programming model. Both registers can be read from as well as written to. The interrupt vector register (register R0) is selected by the register select (RS) input equal to 0. Setting bit 1 of register R0 enables all interrupt levels for the SCB68154/8X825. Writing a 1 to bit 2 of register R0 resets all interrupt levels in the interrupt request register as well as the $\overline{IRQn}$ outputs. Subsequent interrupt requests will be honored. Bit 2 of R0 will always be read as 0. The high order bits, bits 7 – 3, of register R0 are the high order bits of the status/ID byte. The seven bit output of the status/ID byte are formed by concatenating the high order bits (bits 7 – 3) of register R0 with system bus address lines A3 and A2. Bus address lines A3 and A2 are output on BD2 and BD1 respectively.

The interrupt request register (R1) is selected by RS input equal to 1. Setting bit "n" in R1 will generate an interrupt on interrupt request level $\overline{IRQn}$. Any number (up to the maximum of seven) interrupt requests can be generated in a single access of R1.

The state of only those levels, which a 1 has been written to, is affected. Writing a 0 to any level does not change the current state of that level. For example, if $\overline{IRQ1}$ is currently asserted, writing a 0 to bit 1 of R1 does not de-assert $\overline{IRQ1}$, nor clear bit 1 in R1.

Note that interrupt requests on the same level are not stackable. To generate another interrupt request on a level currently asserted, the user must wait until that level has been acknowledged, before generating another interrupt request on that level.

Since interrupts are acknowledged independently of the local CPU, the interrupt vector register should not be modified while interrupts are pending. Any attempt to modify the interrupt vector register, while interrupts are

pending, could cause the status/ID byte to change while the interrupted master is reading it. This could cause the interrupted master to acquire an indeterminate vector. Therefore, the interrupt request register should be examined to make certain there are no interrupts pending before attempting to modify the interrupt vector register.

All data transfers between the local CPU and the SCB68154/8X825 are done using local data lines (LD1 – LD7), register select (RS), read/write (R/$\overline{W}$) and a chip select input ($\overline{CSDS}$). The SCB68154/8X825 supplies a local data transfer acknowledge ($\overline{LDTACK}$) to complete the transfer of data between the local CPU and itself.

Interrupt/Interrupt Acknowledge

The SCB68154/8X825 generates the maximum defined seven bus interrupts, on the $\overline{IRQ1}$ – $\overline{IRQ7}$ outputs, in a VMEbus or VERSAbus system. An interrupted master will acknowledge only a single level of the seven interrupt levels. To allow for multiple interrupters on the level acknowledged, VMEbus and VERSAbus systems use an interrupt acknowledge daisy-chain. The SCB68154/8X825 resides in this interrupt acknowledge daisy-chain.

When the system interrupt acknowledge ($\overline{IACK}$) is asserted, the interrupt acknowledge daisy-chain starts at the first slot in the system bus. The level being acknowledged is specified by the interrupted master on address lines A1 – A3. The system bus interface on the SCB68154/8X825 is initiated only if $\overline{IACK}$, interrupt acknowledge daisy-chain in ($\overline{IACKIN}$), and data strobe 0 (DS0) are all received asserted. If the system bus interface is initiated and the SCB68154/8X825 has an interrupt request on the level specified, it will not pass the daisy-chain signal on. It will, instead, clear the interrupt request level acknowledged, $\overline{IRQn}$, as well as the appropriate bit in the interrupt request register. It will also assert buffer enable ($\overline{BUFEN}$), place seven bits of the status/ID byte on the bus data outputs (BD1 – BD7) and assert data transfer acknowledge ($\overline{DTACK}$).

If the system bus interface is initiated, but the SCB68154/8X825 has no interrupt request on the level being acknowledged, it will pass the daisy-chain input ($\overline{IACKIN}$) on via the interrupt acknowledge out ($\overline{IACKOUT}$).

Arbitration

The system bus interface, as well as the local master interface, are independent processes. Either can be initiated at any time, without respect to the other. The SCB68154/8X825 will arbitrate between the processes, allowing proper system operation without any degradation in performance.

Reset

When $\overline{RESET}$ is asserted, the SCB68154/8X825 drives the outputs $\overline{IRQn}$ and $\overline{IACKOUT}$ high. It also resets the interrupt request and the interrupt vector registers.

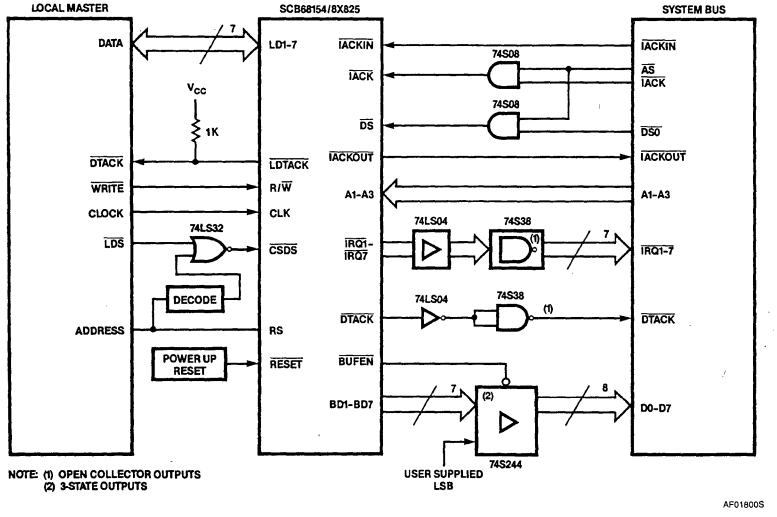


Figure 1. Typical Configuration

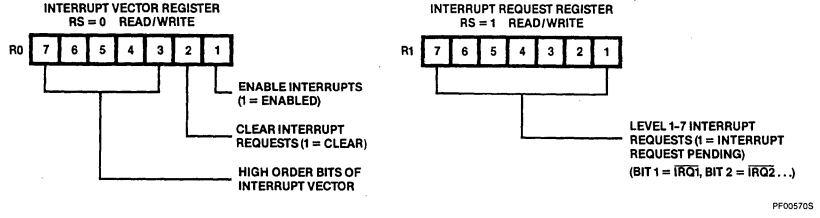


Figure 2. Programming Model

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
Supply voltage[3]	−0.5 to +7.0	V
Input voltage[3]	−0.5 to +5.5	V
Voltage applied to output in off-state[3]	−0.5 to +5.5	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5]

PARAMETER		TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{CC}	Supply voltage		4.75	5.25	V
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
I_{IL}	Input low current	$V_{CC} = 5.25V$, $V_{IL} = 0.4V$		−410	μA
I_{IH}	Input high current	$V_{CC} = 5.25V$, $V_{IH} = 2.7V$		20	μA
I_{OS}	Short circuit output current	$V_{CC} = 5.25V$, $V_{OUT} = 0V$ Other outputs not grounded	−15	−100	mA
I_{OZL}	High-Z low output current BD1 – BD7	$V_{CC} = 5.25V$, $V_{OL} = 0.5V$		−20	μA
I_{OZH}	High-Z high output current BD1 – BD7	$V_{CC} = 5.25V$, $V_{OH} = 2.5V$		20	μA
V_{OL}	Output low voltage			0.5	V
	$\overline{LDTACK}$	$V_{CC} = 4.75V$, $I_{OL} = 20mA$			
	All other outputs	$V_{CC} = 4.75V$, $I_{OL} = 8mA$			
V_{OH}	Output high voltage	$V_{CC} = 4.75V$, $I_{OH} = -400\mu A$	2.5		V
I_{CEX}	Open collector leakage current				
	$\overline{LDTACK}$	$V_{CC} = 4.75V$, $V_{OUT} = 4.75V$		100	μA
I_I	Input leakage current	$V_{CC} = 5.25V$, $V_{IN} = 5.25V$		100	μA
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IN} = -10mA$	−1.2		V
I_{CC}	Supply current	$V_{CC} = 5.25V$, $V_{IN} = 0V$		130	mA

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on + 150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient for ceramic package (116°C/W for plastic package).
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 3ns maximum and output voltages are checked at 0.8V and 2.0V.
6. If the falling edge of $\overline{IACKIN}$ occurs last, then t_{ADIK} is valid. If the falling edge of $\overline{DS}$ occurs last, then t_{ADDS} is valid. If the falling edges of $\overline{IACKIN}$ and $\overline{DS}$ occur simultaneously then either t_{ADDS} or t_{ADIK} is valid.
7. If the falling edge of $\overline{IACKIN}$ occurs last, then t_{IKBF} is valid. If the falling edge of $\overline{DS}$ occurs last, then t_{DSBF} is valid. If the falling edges of $\overline{IACKIN}$ and $\overline{DS}$ occur simultaneously then either t_{IKBF} or t_{DSBF} is valid.
8. If the falling edge of $\overline{IACKIN}$ occurs last, then t_{IRA1} is valid. If $\overline{DS}$ occurs last, then t_{IRA2} is valid. If the falling edges of both $\overline{IACKIN}$ and $\overline{DS}$ occur simultaneously then either t_{IRA1} or t_{IRA2} is valid.
9. True only if no request pending on levels being acknowledged. If the falling edge of $\overline{IACKIN}$ occurs last, then t_{DYO1} is valid. If the falling edge of $\overline{DS}$ occurs last then t_{DYO2} is valid. If the falling edges of both $\overline{IACKIN}$ and $\overline{DS}$ occur simultaneously then either t_{DYO1} or t_{DYO2} is valid.
10. If the rising edge of $\overline{IACK}$ occurs first, then t_{IDT} is valid. If the rising edge of $\overline{DS}$ occurs first then t_{DSDT} is valid. If the rising edges of both $\overline{IACK}$ and $\overline{DS}$ occur simultaneously, then either t_{IDT} or t_{DSDT} is valid.
11. If the rising edge of $\overline{IACK}$ occurs first then t_{ITST} is valid. If the rising edge of $\overline{DS}$ occurs first then t_{DTST} is valid. If the rising edges of both $\overline{IACK}$ and $\overline{DS}$ occur simultaneously then either t_{ITST} or t_{DTST} is valid.
12. If the rising edge of $\overline{IACK}$ occurs first, then t_{IBF} is valid. If the rising edge of $\overline{DS}$ occurs first then t_{DBF} is valid. If the rising edges of both $\overline{IACK}$ and $\overline{DS}$ occur simultaneously, then either t_{IBF} or t_{DBF} is valid.
13. If the rising edge of $\overline{IACK}$ occurs first then t_{IDTK} is valid. If the rising edge of $\overline{DS}$ occurs first then t_{DDTK} is valid. If the rising edges of both $\overline{IACK}$ and $\overline{DS}$ occur simultaneously, then either t_{IDTK} or t_{DDTK} is valid.
14. True only if no request pending on level being acknowledged. If the rising edge of $\overline{IACK}$ occurs first then t_{IOUT} is valid. If the rising edge of $\overline{DS}$ occurs first then t_{DOUT} is valid. If the rising edge of both $\overline{IACK}$ and $\overline{DS}$ occur simultaneously then either t_{IOUT} or t_{DOUT} is valid.
15. t_{TST} is always greater than or equal to t_{DTH}.
16. These parameters are guaranteed at the values listed; these values were determined either by system bench testing or by Signetics' characterization procedures. All other tabular entries are taken directly from simulation results run at a range of operational frequencies; these values are not tested or guaranteed.

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AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5]

PARAMETER		LIMITS		UNIT
		Min	Max	
Register read (see figure 3)				
t_{RSS}	RS valid to $\overline{CSDS}$ low set-up time	0		ns
t_{RWS}	R/$\overline{W}$ to $\overline{CSDS}$ low set-up time	0		ns
t_{DTV}	$\overline{LDTACK}$ low to LD1 – 7 valid	5.4	19.4	ns
t_{DTCS}	$\overline{LDTACK}$ low to $\overline{CSDS}$ high	0		ns
t_{RSH}	$\overline{CSDS}$ high to $\overline{RS}$ valid hold time	0		ns
t_{RWH}	$\overline{CSDS}$ high to R/$\overline{W}$ high hold time	0		ns
t_{DTH}	$\overline{CSDS}$ high to LD1 – 7 valid hold time	11.5	33.5	ns
t_{TST}[15]	$\overline{CSDS}$ high to LD1 – 7 three state	11.5	34.5	ns
t_{CSDT}[16]	$\overline{CSDS}$ high to $\overline{LDTACK}$ high	9.2	27.2	ns
t_{CSH}	$\overline{CSDS}$ high time	20		ns
t_{ACCR}	$\overline{CSDS}$ low to $\overline{LDTACK}$ low read access time	$t_{CKPD} \div 2 + 12.5$	$3t_{CKPD} \div 2 + 40.3$	ns
Register write (see figure 4)				
t_{RSS}	RS valid to $\overline{CSDS}$ low set-up time	0		ns
t_{RWS2}	R/$\overline{W}$ low to $\overline{CSDS}$ low set-up time	0		ns
t_{DS}	LD1 – LD7 valid to $\overline{CSDS}$ low set-up time	0		ns
t_{RSH}	$\overline{CSDS}$ high to RS valid hold time	0		ns
t_{RWH2}	$\overline{CSDS}$ high to R/$\overline{W}$ low hold time	0		ns
t_{DH}	$\overline{CSDS}$ high to LD1 – LD7 valid	0		ns
t_{CSDT}	$\overline{CSDS}$ high to $\overline{LDTACK}$ high	9.2	27.2	ns
t_{DTCS}	$\overline{LDTACK}$ low to $\overline{CSDS}$ high	0		ns
t_{IRQ}	$\overline{LDTACK}$ low to $\overline{IRQn}$ low	1.2	8.2	ns
t_{ACCW}	$\overline{CSDS}$ low to $\overline{LDTACK}$ low write access time	$t_{CKPD} \div 2 + 13.3$	$3t_{CKPD} \div 2 + 40.3$	ns
t_{CSH}	$\overline{CSDS}$ high time	20		ns
Interrupt acknowledge (see figure 5)				
t_{IKDS}	$\overline{IACK}$ low to $\overline{DS}$ low	0		ns
t_{ADDS}[6]	A1 – A3 valid to $\overline{DS}$ low set-up	0		ns
t_{ADIK}[6]	A1 – A3 valid to $\overline{IACKN}$ low set-up	0		ns
t_{IKBF}[7]	$\overline{IACKN}$ low to $\overline{BUFEN}$ low	$t_{CKPD} + 18.3$	$3t_{CKPD} \div 2 + 29.2$	ns
t_{DSBF}[7]	$\overline{DS}$ low to $\overline{BUFEN}$ low	$t_{CKPD} + 18.3$	$3t_{CKPD} \div 2 + 29.2$	ns
t_{IRA1}[8]	$\overline{IACKN}$ low to $\overline{IRQn}$ high	$t_{CKPD} + 12.5$	$3t_{CKPD} \div 2 + 29.2$	ns
t_{IRA2}[8]	$\overline{DS}$ low to $\overline{IRQn}$ high	$t_{CKPD} + 29.2$	$3t_{CKPD} \div 2 + 29.2$	ns
t_{DYO1}[9]	$\overline{IACKN}$ low to $\overline{IACKOUT}$	$t_{CKPD} + 11.2$	$3t_{CKPD} \div 2 + 29.2$	ns
t_{DYO2}[9]	$\overline{DS}$ low to $\overline{IACKOUT}$ low	$t_{CKPD} + 11.2$	$3t_{CKPD} \div 2 + 29.2$	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		LIMITS		UNIT
		Min	Max	
t_{BFBD}	$\overline{BUFEN}$ low to BD1 – BD7	3.2	38.2	ns
t_{BFDT}	$\overline{BUFEN}$ low to $\overline{DTACK}$ low	38.2	50	ns
t_{ADRH}	$\overline{DTACK}$ low to A1 – A3 valid hold time	0		ns
t_{DTDS}	$\overline{DTACK}$ low to $\overline{DS}$ high	0		ns
t_{DTIK}	$\overline{DTACK}$ low to $\overline{IACK}$ high	0		ns
t_{IDT}[10]	$\overline{IACK}$ high to BD1 – BD7 valid hold time	3.0	8.4	ns
t_{DSDT}[10]	$\overline{DS}$ high to BD1 – BD7 valid hold time	3.0	8.4	ns
t_{ITST}[11]	$\overline{IACK}$ high to BD1 – BD7 three state	3.0	9.1	ns
t_{DTST}[11]	$\overline{DS}$ high to BD1 – BD7 three state	3.0	9.1	ns
t_{DBF}[12]	$\overline{DS}$ high to $\overline{BUFEN}$ high	12.2	32.2	ns
t_{IBF}[12]	$\overline{IACK}$ high to $\overline{BUFEN}$ high	12.2	32.2	ns
t_{DDTK}[13]	$\overline{DS}$ high to $\overline{DTACK}$ high	12.2	32.2	ns
t_{IDTK}[13]	$\overline{IACK}$ high to $\overline{DTACK}$ high	12.2	32.2	ns
t_{IOUT}[14]	$\overline{IACK}$ high to $\overline{IACKOUT}$ high	6.2	17.2	ns
t_{DOUT}[14]	$\overline{DS}$ high to $\overline{IACKOUT}$ high	6.2	17.2	ns
t_{IAKH}	$\overline{IACK}$ high time	20		ns
t_{IINH}	$\overline{IACK}$ high to $\overline{IACKIN}$ high	0		ns
t_{IKIN}	$\overline{IACK}$ low to $\overline{IACKIN}$ low	0		ns
Reset timing (see figure 6)				
t_{RST}	$\overline{RESET}$ low time	51		ns
Clock timing (see figure 7)				
t_{CKH}[16]	Clock high	45		ns
t_{CKPD}	Clock period	90		ns

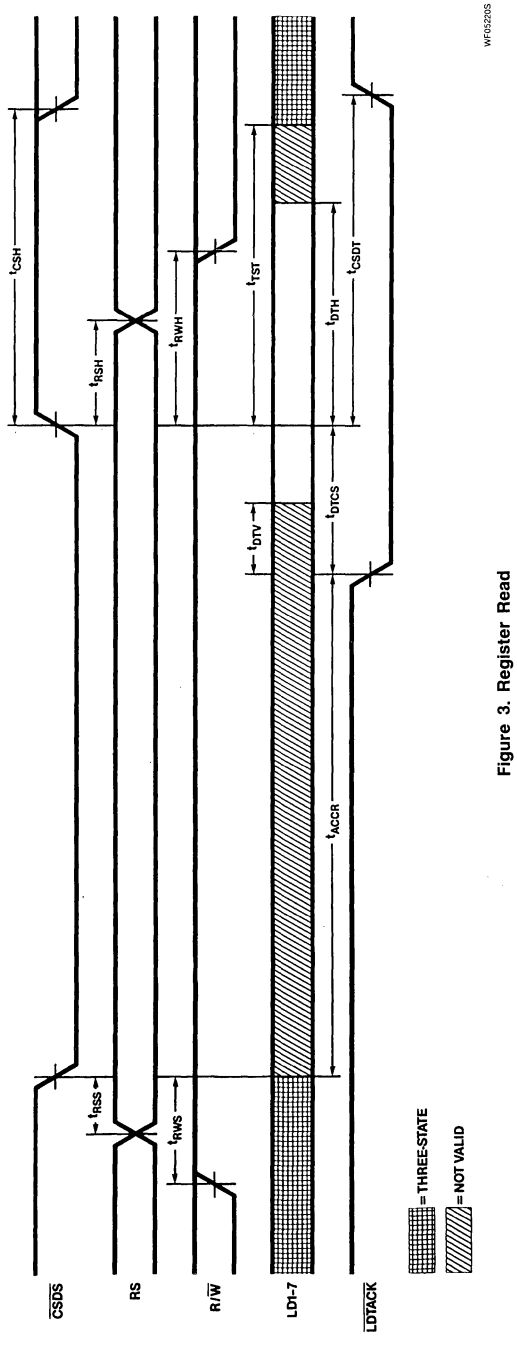

Figure 3. Register Read

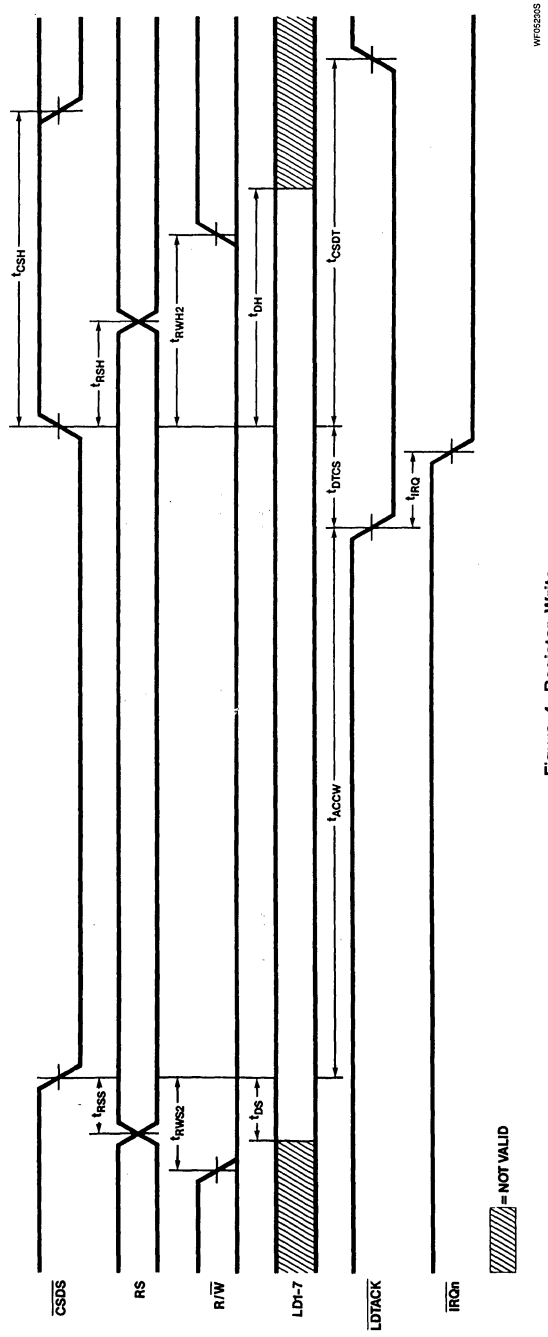

Figure 4. Register Write

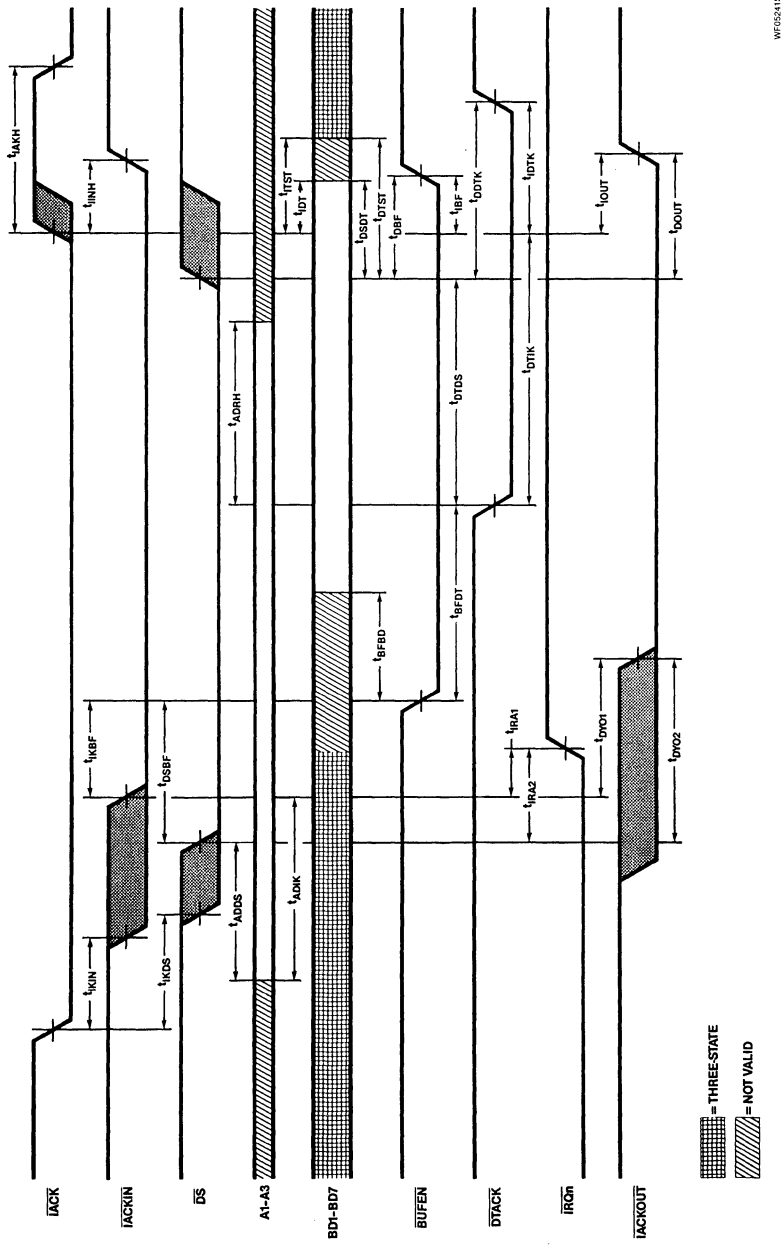

Figure 5. Interrupt Acknowledge

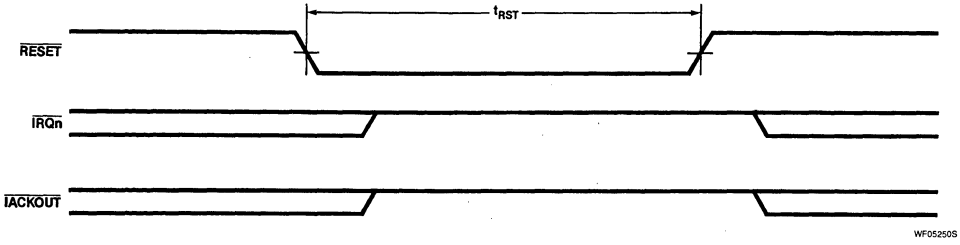

Figure 6. Reset Timing

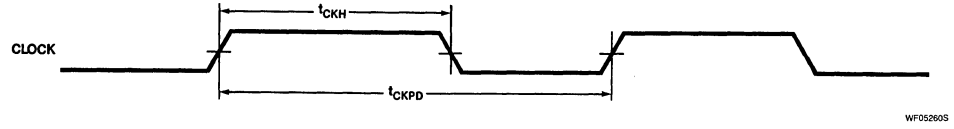

Figure 7. Clock Timing