MOSTEK®

MICROCOMPUTER COMPONENTS

# Local Area Network Controller For Ethernet

# MK68590



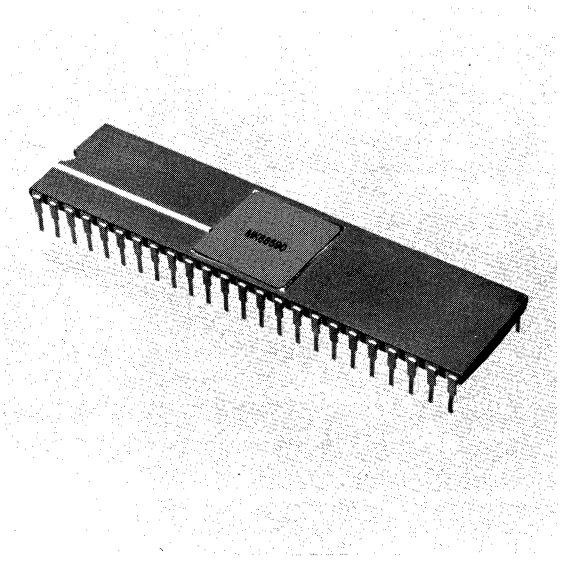
## FEATURES

- ☐ 100% compatible Ethernet serial port
- ☐ Data packets moved by block transfers over a processor bus (on-board DMA controller-24 bit linear address space)
- ☐ Buffer management
- ☐ Packet framing
- ☐ Preamble and CRC insertion
- ☐ Preamble stripping and CRC checking
- ☐ General 16 bit microprocessor bus interface compatible with popular processors (68000, 8086, Z8000, LSI-11)
- ☐ Cable fault detection
- ☐ Multicast logical address filtration
- ☐ Collision handling and retry
- ☐ Scaled N-channel MOS VLSI technology
- ☐ 48 pin DIP
- ☐ Single 5 volt power supply
- ☐ Single phase TTL level clock
- ☐ All inputs and outputs TTL compatible
- ☐ Completely compatible with companion Serial Interface Adapter (SIA) chip.

## INTRODUCTION

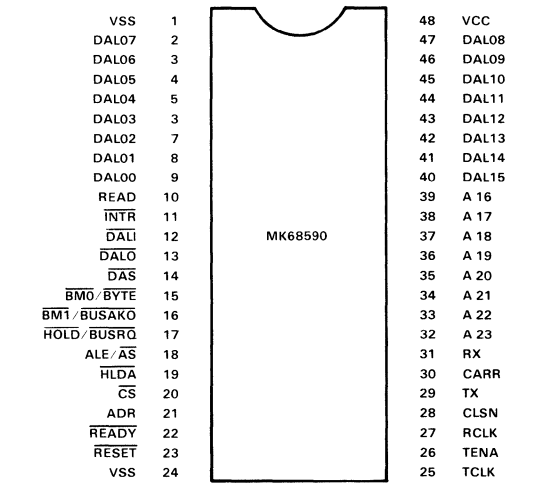
The MK68590-LANCE (Local Area Network Controller for Ethernet) is a 48 pin VLSI device designed to simplify greatly the interfacing of a microcomputer or a minicomputer to an Ethernet Local Area Network. This chip is intended to operate in a local environment that includes a closely coupled memory and microprocessor. The LANCE uses scaled N-channel MOS technology and is compatible with several microprocessors.

**MK68590**
**Figure 1**



## LANCE PIN DESCRIPTION

**Figure 2**



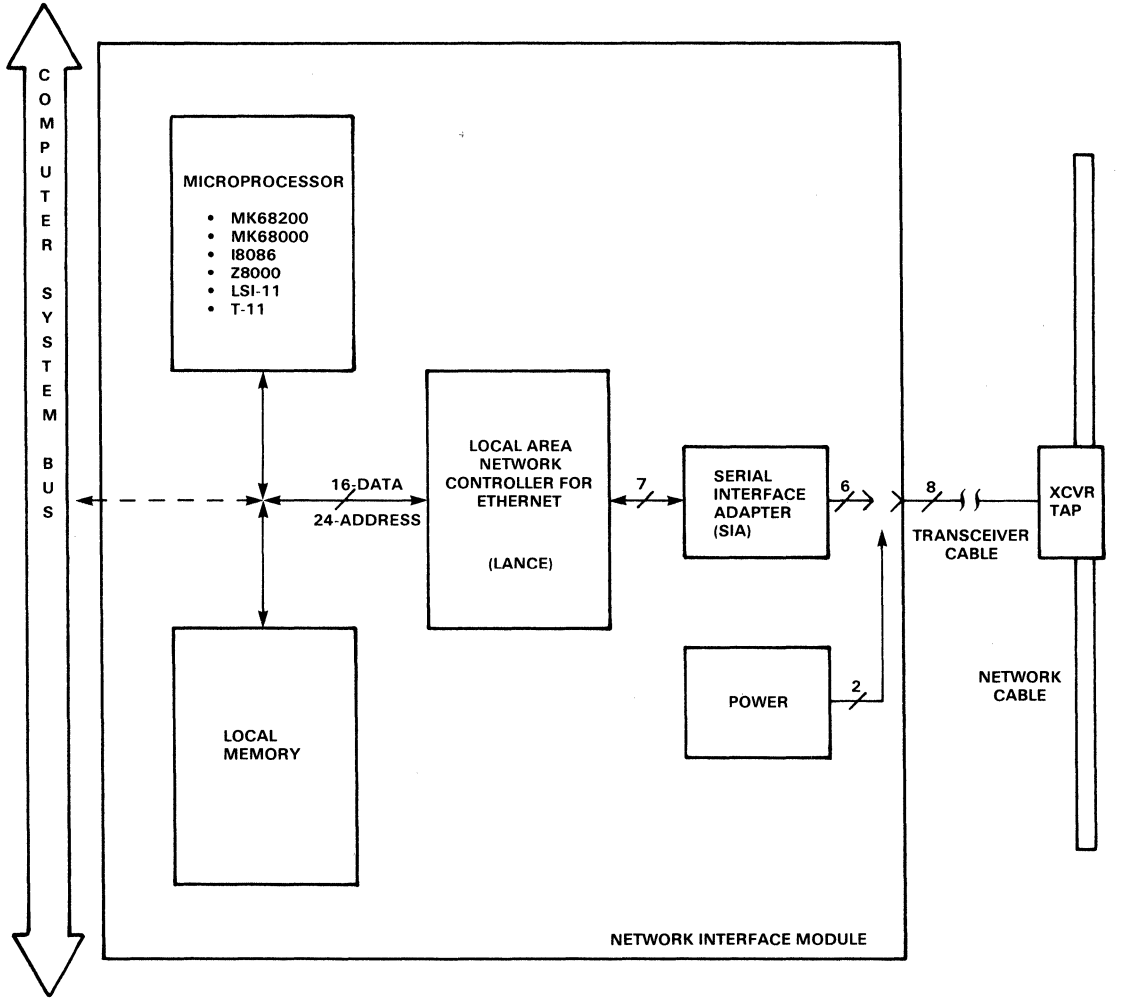
## FUNCTIONAL CAPABILITIES

The Local Area Network Controller for Ethernet (LANCE) interfaces to a microprocessor bus characterized by time multiplexed address and data lines. Typically, data transfers are 16 bits wide but byte transfers occur if the buffer memory address boundaries are odd. The address bus is 24 bits wide.

The Ethernet packet format consists of a 64 bit preamble, a 48 bit destination address, a 48 bit source address, a 16 bit type field, and from a 46 to 1500 byte data field terminated with a 32-bit CRC. The variable widths of the packets accommodate both short status, command and terminal traffic packets, and long data packets to printers and disks (1024 byte disk sectors for example). Packets are spaced a minimum of 9.6 $\mu$sec apart to allow one node time enough to receive back to back packets.

The LANCE is intended to operate in a minimal configuration that requires close coupling between local memory and a processor. The local memory provides packet buffering for the chip and serves as a communication link between the chip and the processor. During initialization, the control processor loads into LANCE the starting address of the initialization block plus the operating mode of the chip via two control registers. It is only during this initial phase that the host processor talks directly to LANCE. All further communications are handled via a DMA machine under microword control contained within the LANCE. Figure 3 is a block diagram of the LANCE and SIA device used to create an Ethernet interface for a computer system.

**ETHERNET LOCAL AREA NETWORK SYSTEM BLOCK DIAGRAM**
**Figure 3**



## PIN DESCRIPTION

DAL00-DAL15 DATA/ADDRESS BUS (INPUT/OUTPUT TRI-STATE) The time multiplexed Address/Data bus. These lines will be driven as a Bus Master and as a Bus Slave.

A16-A23 HIGH ORDER ADDRESS BUS (OUTPUT TRI-STATE) The additional address bits necessary to extend the DAL lines to produce a 24 bit address. These lines will be driven as a Bus Master only.

READ (INPUT/OUTPUT TRI-STATE) Indicates the type of operation to be performed in the current bus cycle. This signal will be driven by the LANCE when it is a bus master.

LANCE as a Bus Slave:

High - Data is placed on the DAL by the chip

Low - Data is taken off the DAL by the chip

LANCE as a Bus Master:

High - Data is taken off the DAL by the chip

Low - Data is placed on the DAL by the chip

$\overline{BM0}$, $\overline{BM1}$ or BYTE, $\overline{BUSAKO}$ BYTE MASK (INPUT/OUTPUT) Pins 15 and 16 are programmable through bit (00) of CSR3 (known as BCON). Asserting $\overline{RESET}$ clears CSR3.

If BCON = 0

I/O PIN 16 = $\overline{BM\ 1}$ (OUTPUT TRI-STATE)

I/O PIN 15 = $\overline{BM\ 0}$ (OUTPUT TRI-STATE)

BM0, BM1 Byte Mask. Indicates the byte(s) of a bus transaction to be read or written. The BM lines are ignored as a Bus Slave and assume word transfers only. The LANCE drives the BM lines only as a Bus Master. Byte selection is done as outlined in the following table:

| $\overline{BM\ 1}$ | $\overline{BM\ 0}$ | |
|---|---|---|
| LOW | LOW | Whole Word |
| LOW | HIGH | Upper byte |
| HIGH | LOW | Lower byte |
| HIGH | HIGH | None |

If BCON = 1

I/O PIN 16 = $\overline{BUSAKO}$ (OUTPUT)

I/O PIN 15 = BYTE (OUTPUT TRI-STATE)

BYTE An alternate byte selection line. Byte selection is done using the BYTE line and DAL (00) line, latched during the address portion of the bus transaction. BYTE is ignored as a Bus Slave as is $\overline{BM0}$, $\overline{BM1}$. There are two modes of ordering bytes depending on bit (02) of CSR 3, (known as BSWP). This programmable ordering of upper and lower bytes when using BYTE and DAL (00) as selection signals is required to make the ordering compatible with the various 16 bit microprocessors.

| BSWP = 0 | | BSWP = 1 | | |
|---|---|---|---|---|
| LOW | LOW | LOW | LOW | Whole Word |
| LOW | HIGH | LOW | HIGH | Illegal Condition |
| HIGH | HIGH | HIGH | LOW | Upper Byte |
| HIGH | LOW | HIGH | HIGH | Lower Byte |

$\overline{BUSAKO}$ The DMA daisy chain output

$\overline{CS}$ CHIP SELECT (INPUT). Indicates, when asserted, that the LANCE is the slave device of the data transfer. $\overline{CS}$ must be valid throughout the data portion of the bus cycle.

ADR REGISTER ADDRESS PORT SELECT (INPUT). Indicates, when $\overline{CS}$ is asserted, which of the two register ports is selected. ADR must be valid throughout the data portion of the bus cycle.

ADR

LOW Register Data Port.

HIGH Register Address Port.

ALE/$\overline{AS}$ ADDRESS LATCH ENABLE (OUTPUT TRI-STATE). Used to demultiplex the DAL lines and define the address portion of the bus cycle. This I/O pin is programmable through bit (01) of CSR3. As ALE, the signal transitions from a HIGH to a LOW during the address portion of the bus transaction and remains LOW during the entire data portion of the transaction. As $\overline{AS}$, the signal pulses LOW during the address

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portion of the bus transaction. The LANCE drives the ALE/$\overline{AS}$ line only as a Bus Master

CSR3 (01) ACON = 0

I/O PIN 31 = ALE

CSR3 (01) ACON = 1

I/O PIN 31 = $\overline{AS}$

$\overline{DAS}$ — DATA STROBE (INPUT/OUTPUT TRI-STATE). Defines the data portion of the bus transaction. $\overline{DAS}$ is driven only as a Bus Master.

$\overline{DALO}$ — DATA/ADDRESS LINE OUT (OUTPUT TRI-STATE). An external bus transceiver control line. $\overline{DALO}$ is asserted when the LANCE drives the DAL lines as a Bus Master.

$\overline{DALI}$ — DATA/ADDRESS LINE OUT (OUTPUT TRI-STATE). An external bus transceiver control line. $\overline{DALI}$ is asserted when the LANCE reads from the DAL lines as a Bus Master.

$\overline{HOLD}/\overline{BUSRQ}$ — BUS HOLD REQUEST (OUTPUT OPEN DRAIN). Asserted by the LANCE when it requires access to memory. $\overline{HOLD}$ is held LOW for the entire ensuing bus transaction. This bit is programmable through bit (00) of CSR3. Bit (00) of CSR3 is cleared when $\overline{RESET}$ is asserted.

CSR3 (00) BCON = 0
I/O PIN 17 = $\overline{HOLD}$ (OUTPUT OPEN DRAIN)
CSR3 (00) BCON = 1
I/O PIN 17 = $\overline{BUSRQ}$ (OUTPUT OPEN DRAIN)
$\overline{BUSRQ}$ will be asserted only if I/O PIN 17 is high prior to assertion.

$\overline{HLDA}$ — BUS HOLD ACKNOWLEDGE (INPUT). A response to $\overline{HOLD}$ indicating that the LANCE is the Bus Master. $\overline{HLDA}$ stops its response when $\overline{HOLD}$ ends its assertion.

$\overline{INTR}$ — INTERRUPT (OUTPUT OPEN DRAIN). An attention signal that indicates, when enabled, that one or more of the following events have occurred: a message reception or transmission has completed or an error has occurred during the transaction; the initialization procedure has completed, or a memory error has been encountered. $\overline{INTR}$ is enabled by programming register (CSR0).

RX — RECEIVE (INPUT). Receive Input Bit Stream.

TX — TRANSMIT (OUTPUT). Transmit Output Bit Stream.

TENA — TRANSMIT ENABLE (OUTPUT). Transmit Output Bit Stream Enable. A level asserted with the transmit output bit stream, TX, to enable the external transmit logic.

RCLK — RECEIVE CLOCK (INPUT). Normally a 10 MHz square wave synchronized to the Receive data and only present while receiving an input bit stream.

CLSN — COLLISION (INPUT). A logical input that indicates that a collision is occurring on the channel.

CARR — CARRIER (INPUT). A logical input that indicates that the presence of a carrier on the channel.

TLCK — TRANSMIT CLOCK (INPUT). Normally a freerunning 10 MHz clock.

$\overline{READY}$ — (INPUT/OUTPUT TRI-STATE). When the LANCE is a bus master, $\overline{READY}$ is an asynchronous acknowledgement from external memory that it will complete the data transfer. As a bus slave, the chip asserts $\overline{READY}$ when it has put data on the bus, or is about to take data off the bus. $\overline{READY}$ is a response to $\overline{DAS}$. $\overline{READY}$ negates after $\overline{DAS}$ negates.

$\overline{RESET}$ — (INPUT). Bus reset signal. Causes the LANCE to cease operation and enter an idle state.

VCC — Power supply pin. +5 VDC ±5%

VSS — Ground. 0 VDC

## FUNCTIONAL DESCRIPTION

### SERIAL DATA HANDLING

The basic operation of the chip set to provide the Ethernet interface is as follows. In the transmit mode (since there is only one transmission path, Ethernet is a half duplex system), the LANCE reads data from a transmit buffer by using Direct Memory Access (DMA) and appends the preamble, sync pattern (two ones after alternating ones and zeros in the preamble), and calculates and appends the complement of the 32-bit CRC. In the receive mode, the destination address, source address, type, data, and CRC fields are transferred to memory via DMA cycles. The CRC is calculated as the data and transmitted CRC is received. At the end of the packet, if this calculated CRC does not agree with a constant, an error bit is set and an interrupt is generated to the microprocessor. In the receive mode, packets will be accepted by the LANCE under four modes of operation. The first mode is a full comparison of the 48 bit destination address in the packet with the node address that was programmed into the LANCE during an initialization cycle. There are two types of logical address. One is a group type mask where the 48 bit address in the packet is put through a hash filter in order to map the 48 bit physical addresses into 1 of 64 logical groups. This mode can be useful if sending packets to all of one type of a device simultaneously or the network. (i.e. send a packet to all file servers or all printer servers). The second logical address is a multicast address where all nodes on the network receive the packet. The last receive mode of operation is the so called "promiscuous mode" in which a node will accept all packets on the coax regardless of their destination address.

### COLLISION DETECTION AND IMPLEMENTATION

The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear coax before transmitting, Ethernet handles collisions in a predetermined way. Should two transmitters attempt to seize the coax at the same time, they will collide, and the data on the coax will be garbled. During a transmission, the LANCE monitors the CLSN (collision) pin. This signal is generated by the transceiver when data on the coax gets garbled. A normal collision occurs while the preamble is being transmitted. The LANCE will continue to transmit the preamble then "jams" the network for a predetermined amount of time. This jamming ensures that all nodes have recognized the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm specified in the Ethernet specification in order that the colliding nodes do not repeatedly try to access the network at the same time. Up to 16 attempts to access the network are made by the LANCE before it will report back an error due to excessive collisions.

Extensive error reporting is provided by the LANCE through a microprocessor interrupt and error bits in a status register. The following are the significant error conditions: CRC error on received data; transmitter on longer than was needed to send the data; missed packet error (meaning a packet on the coax was missed because there were no empty buffers in memory), and memory error, in which the memory did not respond (handshake) to a memory cycle request.

### BUFFER MANAGEMENT

A key feature of the LANCE and its on board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings, as shown in Figure 4. There are separate descriptor rings to describe transmit and receive operations. Up to 128 tasks may be queued up on a descriptor ring awaiting execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the length of the data buffer. Data buffers can be chained or cascaded in order to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings in a "look ahead manner" to determine the next empty buffer in order to chain buffers together or to handle back to back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer.

### MICROPROCESSOR INTERFACE

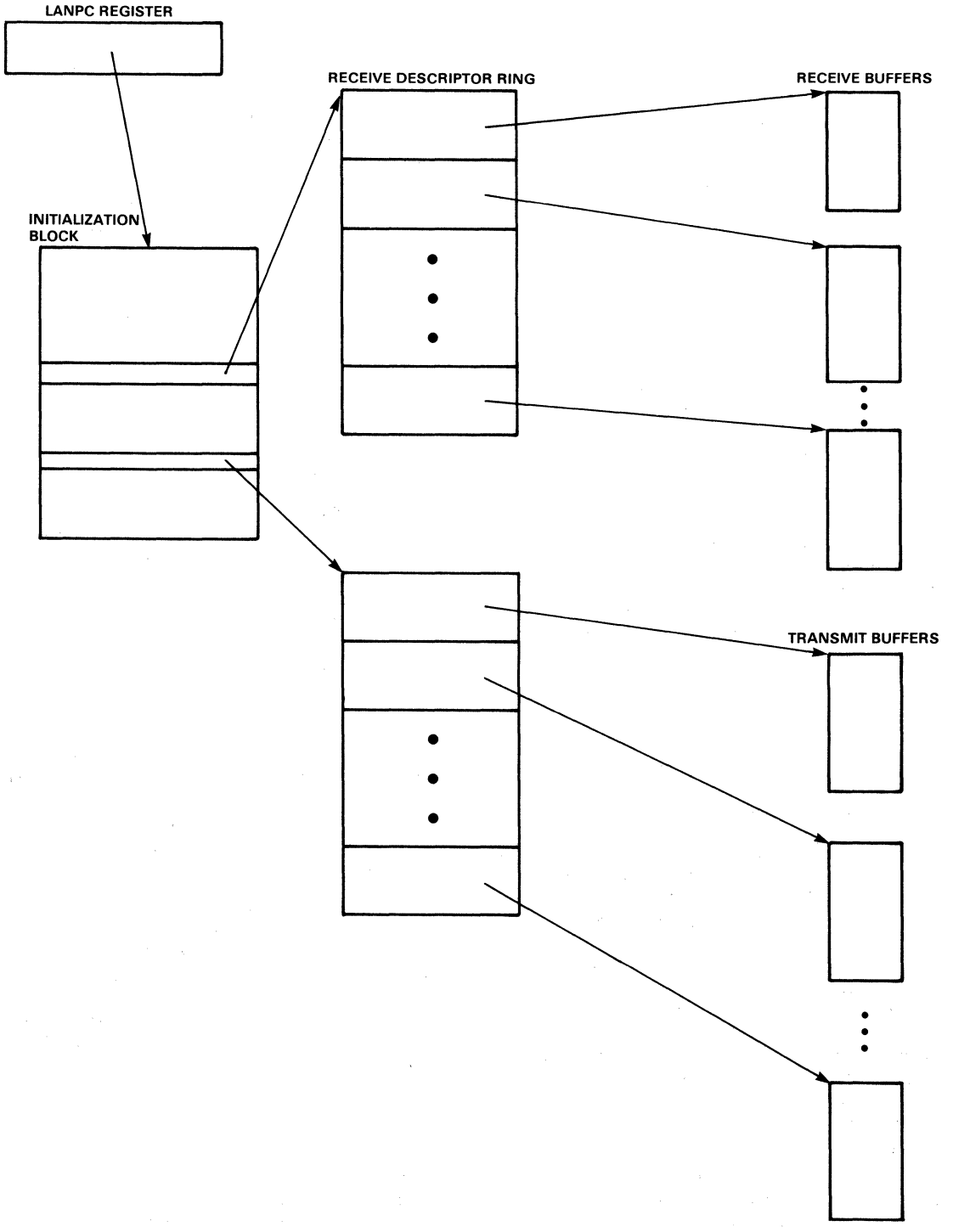
The parallel interface of the LANCE has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the following: 68000, Z8000, 8086, LSI-11, T-11, and MK68200. (The MK68200 is a 16-bit single chip microcomputer under development at Mostek with an architecture modeled after the 68000). The LANCE has a wide 24-bit linear address space when it is in the Bus Master Mode, allowing it to DMA directly into the entire address space of the above microprocessors. No segmentation or paging methods are used within the LANCE, and as such the addressing is closest to that used by the 68000 but is compatible with the others. When the LANCE is a bus master, a programmable mode of operation allows byte addressing either by employing a Byte/Word control signal, much like that used on the 8086 or the Z8000, or by using an Upper Data Strobe/Lower Data Strobe much like that used on the 68000, LSI-11 and MK68200 microprocessors. A programmable polarity on the Address Strobe signal eliminates the need for external logic. The LANCE interfaces with both multiplexed and demultiplexed data busses and features control signals for address/data bus transceivers,

Interrupts to the microprocessor are generated by the LANCE upon completion of its initialization routine, the reception of a packet, the transmission of a packet, transmitter timeout error, a missed packet, and memory error.

The cause of the interrupt is ascertained by reading CSR0. Bit (06) of CSR0, INEA, enables or disables interrupts to the microprocessor. In a polling mode, BIT (07) of CSR0 is sampled to determine when an interrupt causing condition occurred.

## LANCE MEMORY MANAGEMENT

**Figure 4**



## LANCE INTERFACE DESCRIPTION

All data transfers from the LANCE in the Bus Master mode are timed by ALE, $\overline{DAS}$ and $\overline{READY}$. The automatic adjustment of the LANCE cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600 nsec in length and can be increased in 100 nsec increments.

## READ SEQUENCE

At the beginning of a read cycle, valid addresses are placed on DAL00-DAL15 and A16-A21. The BYTE Mask signals ($\overline{BM0}$ and $\overline{BM1}$) become valid at the beginning of this cycle as does READ, indicating the type of cycle. The trailing edge of ALE or $\overline{AS}$ is used to strobe in the addresses A0-A15 into the external latches. Approximately a hundred nanoseconds later, DAL00-DAL15 go into a tristate mode. There is a fifty nanosecond delay to allow for transceiver turnaround, then $\overline{DAS}$ falls low to signal the beginning of the data portion of the cycle. At this point in the cycle, the LANCE stalls waiting for the memory device to assert $\overline{READY}$. Upon assertion of $\overline{READY}$, $\overline{DAS}$ makes a transition from a zero to a one, latching memory data. ($\overline{DAS}$ is low for a minimum of 200 nsec).

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, are used to control the bus transceivers. $\overline{DALI}$ signals to strobe data toward the LANCE and $\overline{DALO}$ signals to strobe data or addresses away from the LANCE. During a read cycle, $\overline{DALO}$ goes inactive before $\overline{DALI}$ goes active to avoid the "spiking" of the bus transceivers.

## WRITE SEQUENCE

The write cycle begins exactly like a read cycle with the READ line remaining inactive. After ALE or $\overline{AS}$ pulse, the DAL00-DAL15 change from addresses to data. $\overline{DAS}$ goes active when the DAL00-DAL15 lines are stable. This data will remain valid on the bus until the memory device asserts $\overline{READY}$. At this point $\overline{DAS}$ goes inactive latching data into the memory device. Data is held for seventy five nanoseconds after the deassertion of $\overline{DAS}$.

## LANCE INTERFACE DESCRIPTION — BUS SLAVE MODE

The LANCE enters the Bus Slave Mode whenever $\overline{CS}$ becomes active. This mode must be entered whenever writing or reading the four status control registers (CSR0, CSR1, CSR2, and CSR3) and the register address pointer (RAP). RAP and CSR0 may be read or written to at any time, but the LANCE must be stopped for CSR1, CSR2, and CSR3 to be written to.

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## BUS MASTER TIMING

**Figure 5**