MK68591/2(P,J,N)

SERIAL INTERFACE ADAPTER (SIA)

COMMUNICATIONS PRODUCTS

FEATURES

- ☐ Compatible with Ethernet and IEEE-802.3 Specifications
- ☐ Crystal-controlled Manchester Encoder/Decoder
- ☐ Manchester Decoder acquires clock and data within six-bit times with an accuracy of ±3 ns.
- ☐ Guaranteed carrier and collision detection squelch threshold limits
  - — Carrier/collision detected for inputs more negative than −275 mV
  - — No carrier/collision for inputs more positive than −175 mV
- ☐ Input signal conditioning rejects transient noise
  - — Transients <10 ns for collision detector inputs
  - — Transients <20 ns for carrier detector inputs
- ☐ Receiver decodes Manchester data with up to ±20 ns clock jitter (at 10 MHz)
- ☐ TTL-compatible host interface
- ☐ Transmit oscillator accuracy ±0.01% (without adjustments)

GENERAL DESCRIPTION

The MK68591/2 Serial Interface Adapter (SIA) is a Manchester Encoder/Decoder compatible with Ethernet and IEEE-802.3 specifications. In an Ethernet/IEEE-802.3 application, the MK68591/2 interfaces the MK68590 Local Area Network Controller for Ethernet (LANCE™) to the Ethernet transceiver cable, acquires clock and data within 6 bit-times and decodes Manchester data up to ± 20 ns phase jitter at 10 MHz. SIA provides both guaranteed signal threshold limits and transient noise suppression circuitry in both data and collision paths to minimize false start conditions.

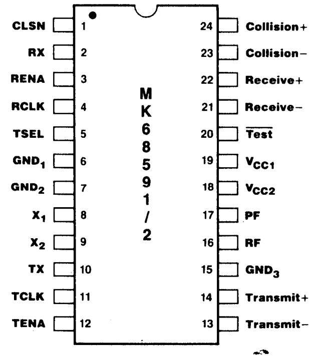


Figure 1. Pin Assignments

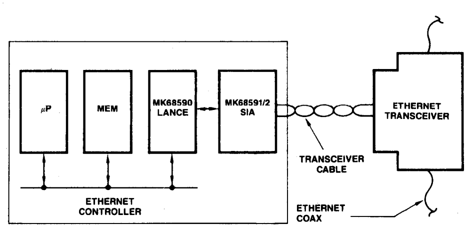


Figure 2. Typical Ethernet Node

LANCE is a trademark of Thomson Components - Mostek Corporation.

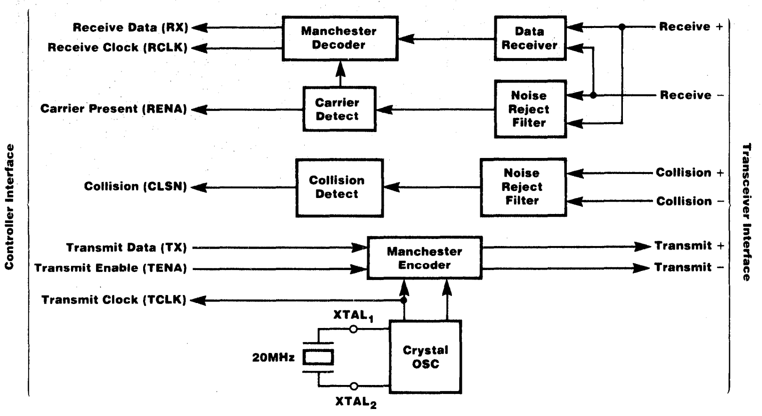


Figure 3. MK68591/2 Block Diagram

PIN DESCRIPTION

CLSN — **Collision (output).** A TTL active high output. Signals at the Collision ± terminals meeting threshold and pulse width requirements will produce a logic high at CLSN output. When no signal is present at Collision ±, CLSN output will be low.

RX — **Receive Data (output).** A MOS/TTL output, recovered data. When there is no signal at Receive ± and $\overline{\text{TEST}}$ is high, RX is high. RX is actuated with RCLK and remains activated until end of message. During reception, RX is synchronous with RCLK and changes after the rising edge of RCLK.

RENA — **Receive Enable (output).** A TTL active high output. When there is no signal at Receive ±, RENA is low. Signals at Receive± meeting threshold and pulse width requirements will produce a logic high at RENA. When Receive ± becomes idle, RENA returns to the low state synchronous with the rising edge of RCLK.

RCLK — **Receive Clock (output).** A MOS/TTL output recovered clock. When there is no signal at Receive ± and $\overline{\text{TEST}}$ is high, RCLK is low. RCLK is activated after the third negative data transition at Receive ±, and remains active until end of message. When $\overline{\text{TEST}}$ is low, RCLK is enabled.

TX — **Transmit (input).** TTL compatible input. When TENA is high, signals at TX meeting setup and hold time to TLCK will be encoded as normal Manchester at Transmit + and Transmit –.

TX High: Transmit + is negative with respect to Transmit – for first half of data bit cell.

TX Low: Transmit + is positive with respect to Transmit – for first half of data bit cell.

TENA — **Transmit Enable (input).** TTL compatible input. Active high data encoder enable. Signals meeting setup and hold time to TCLK allow encoding of Manchester data from TX to Transmit + and Transmit –.

TCLK — **Transmit Clock (output).** MOS/TTL output. TCLK provides symmetrical high and low clock signals at data rate for reference timing of data to be encoded. It also provides clock signals for the controller chip (MK68590 LANCE) and an internal timing reference for receive path voltage controlled oscillators.

Transmit +
Transmit – — **Transmit (outputs).** A differential line output. This line pair is intended to operate into terminated transmission lines. For signals meeting setup and hold time to TCLK at TENA and TX. The Manchester clock and data are outputted at Transmit +/Transmit –. When operating into a 78Ω terminated transmission line, signalling meets the required output

levels and skew for both Ethernet and IEEE-802.3 drop cables.

Receive +
Receive −

Receiver (inputs). A differential input. A pair of internally biased line receivers consisting of a carrier detect receiver with offset threshold and noise filtering to detect the signal, and a data recovery receiver with no offset for Manchester data decoding.

Collision +
Collision −

Collision (inputs). A differential input. An internally biased line receiver input with offset threshold and noise filtering. Signals at Collision ± have no effect on data path functions.

TSEL

Transmit Mode Select. An open collector output and sense amplifier input.

TSEL Low: Idle transmit state Transmit + is positive with respect to Transmit −.

TSEL High: Idle transmit state Transmit + and Transmit − are equal, providing "zero" differential to operate transformer coupled loads.

When connected with an RC network, TSEL is held low during transmission. At the end of transmission, the open collector output is disabled, allowing TSEL to rise and provide a smooth transmission from logic high to "zero" differential idle. Delay and output return to zero are externally controlled by the RC time constant at TSEL. (See Figure 9.)

X_1, X_2

Biased Crystal Oscillator. X_1 is the input and X_2 is the bypass port. When connected for crystal operation, the system clock which appears at TCLK is half the frequency of the crystal oscillator. X_1 may be driven from an external source of two times the data rate. In which case X_2 should be left floating.

RF

Frequency Setting Voltage Controlled Oscillator (V_{CO}) Loop Filter. This loop filter output is a reference voltage for the receive path phase detector. It also is a reference for timing noise immunity circuits in the collision and receive enable path. Nominal reference V_{CO} gain is 1.25 TCLK frequency MHz/V.

PF

Receive Path V_{CO} Phase Lock Loop Filter. This loop filter input is the control for receive path loop damping. Frequency of the receive V_{CO} is internally limited to transmit frequency ± 12%. Nominal receive V_{CO} gain is 0.25 reference V_{CO} gain MHz/V.

$\overline{\text{TEST}}$

Test Control (input). A static input that is connected to V_{CC} for normal MK68591/2 operation and to ground for testing of receive path function. When $\overline{\text{TEST}}$ is grounded, RCLK and RX are enabled so that receive path loop may be functionally tested.

GND_1 — **High Current Ground**

GND_2 — **Logic Ground**

GND_3 — **Voltage Controlled Oscillator Ground**

V_{CC1} — **High Current and Logic Supply**

V_{CC2} — **Voltage Controlled Oscillator Supply**

FUNCTIONAL DESCRIPTION

The MK68591/2 Serial Interface Adapter (SIA) has three basic functions. It is a Manchester Encoder/line driver in the transmit path, a Manchester Decoder with noise filtering and quick lock-on characteristics in the receive path, and a signal detect/converter (10 MHz differential to TTL) in the collision path. In addition, the SIA provides the interface between the TTL logic environment of the LANCE and the differential signaling environment in the transceiver cable.

TRANSMIT PATH

The transmit section encodes separate clock and NRZ* data input signals meeting the set up and hold time to TCLK at TENA and TX, into a standard Manchester II serial bit stream. The transmit outputs (Transmit +/ Transmit −) are designed to operate into terminated transmission lines. When operating into a 78Ω terminated transmission line, signaling meets the required output levels and skew for both Ethernet and IEEE-802.3.

Transmitter Timing and Operation

A 20 MHz fundamental mode crystal oscillator provides the basic timing reference in the SIA. It is divided by two to create the transmit clock reference (TCLK). Both 20 MHz and 10 MHz clocks are fed into the Manchester Encoder to generate the transitions in the encoded data stream. The 10 MHz clock, TCLK, is used by the SIA to internally synchronize transmit data (TX) and transmit

*Non-Return-to-Zero

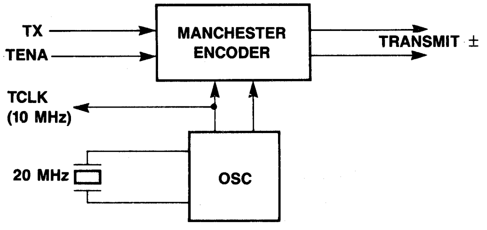


Figure 4. Transmit Section

enable (TENA). TCLK is also used as a stable bit-rate clock by the receive section of the SIA and by other devices in the system (the MK68590 LANCE uses TCLK to drive its internal state machine). The oscillator may use an external 0.005% crystal or an external TTL level input as a reference. Transmit accuracy of 0.01% is achieved (no external adjustments are required).

TENA is activated when the first bit of data is made available on TX. As long as TENA remains high, signals at TX will be encoded as Manchester and will appear at Transmit + and Transmit −. When TENA goes low, the differential transmit outputs go to one of the two idle states defined below:

- TSEL High: The idle state of Transmit +/ Transmit − yields "zero" differential to operate transformer coupled loads (see Figure 14a).
- TSEL Low: In this idle state, Transmit + is positive to Transmit − yielding logical high (see Figure 14b).

RECEIVE PATH

The principle function of the receiver is the separation of the Manchester encoded data stream into clock and NRZ data.

Input Signal Conditioning

Before the data and clock can be separated, it must be determined whether there is "real" data or unwanted noise at the transceiver interface. The MK68591/2 SIA carrier detection receiver provides a static noise margin of −175 to −275 mV for received carrier detection. These DC thresholds assure that no signal more positive than −175 mV is ever decoded and that signals more negative than −275 mV are always decoded. Transient noise of less than 10ns duration in the collision path and 20 ns duration in the data path are also rejected.

This signal conditioning prevents unwanted idle noise on the transceiver cable from causing "false starts" in the receiver. This helps assure a valid response to "real" data.

The receiver section, shown in Figure 6, consists of two data paths. The receive data path is designed to be a zero threshold, high bandwidth receiver. The carrier detection receiver has an additional bias generator. Only data amplitudes larger than the bias level are interpreted as valid data. The noise rejection filter prevents noise transients of less than 20 ns from enabling the data receiver output. The collision detector similarly rejects noise transients of less than 10 ns.

Receiver Section Timing

Receive Enable (RENA) is the "carrier present" indication established when a signal of sufficient amplitude (V_{IDC}) and duration (t_{RPWR}) is present at the receive inputs. Receive Clock (RCLK) and Receive Data (RX) become available after the third negative data transition

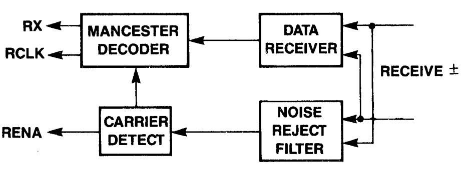


Figure 5. Receiver

at Receive +/ Receive − inputs, and stay active until the end of a packet. During reception, RX is synchronous with RCLK, changing after the rising edge of RCLK.

The receiver detects the end of a packet when the normal transition on the differential inputs cease. After the last low-to-high transition, RENA goes low and RCLK completes one last cycle, storing the last data bit. It then becomes and remains low (see Receive End of Packet Timing diagrams). When $\overline{\text{TEST}}$ is low, RCLK continues to run, tracking data (if available) or synchronizes with TCLK.

Receive Clock Control

To insure quick capture of incoming data, the receiver phase-locked-loop is frequency locked to the transmit oscillator and it phase locks to incoming data edges. Clock and data are available within 6 bit times (accurate to within ±3 ns). The SIA will decode jittered data of up to ±20 ns (see Figure 7).

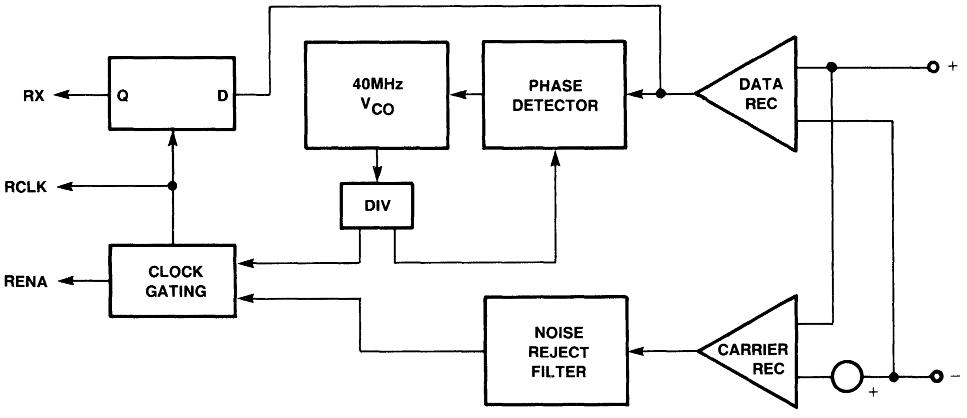


Figure 6. Receiver Section Detail

Differential I/O Terminations

The differential input for the Manchester data (receive ±) is externally terminated by two 40.2 Ω±1% resistors and one optional common mode bypass capacitor. The differential input impedance Z_{IDF} and the common mode input Z_{ICM} are specified so that the Ethernet specification for cable termination impedance is met using standard 1% resistor terminators. The Collision ± differential input is terminated in exactly the same way as the receive input (see Figure 8).

Collision Detection

The Ethernet Transceiver detects collisions on the Ethernet and generates a 10MHz signal on the transceiver cable (Collision +/ Collision −). This collision signal passes through an input stage which assures signal levels and pulse duration. When the signal is detected by the SIA, the SIA sets the CLSN line high. This condition continues for approximately 190ns after the last low-to-high transition on Collision +/ Collision −.

APPLICATION RECOMMENDATIONS

The differential input and output pins should be transformer coupled to meet the IEEE 802.3 16 volt fault tolerance specifications.

This device is not recommended for operation in wire wrapped boards.

This device should be handled with care to avoid electro-static-discharge (ESD) failures. Although this is a bipolar device, serial input and output circuits are designed to meet the IEEE 802.3 specifications and cannot be protected against ESD without affecting the performance of the device.

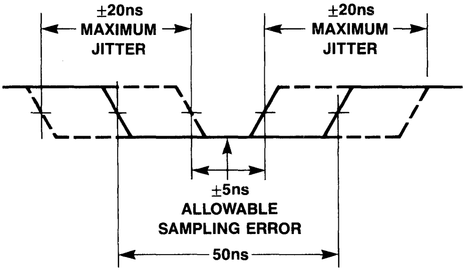
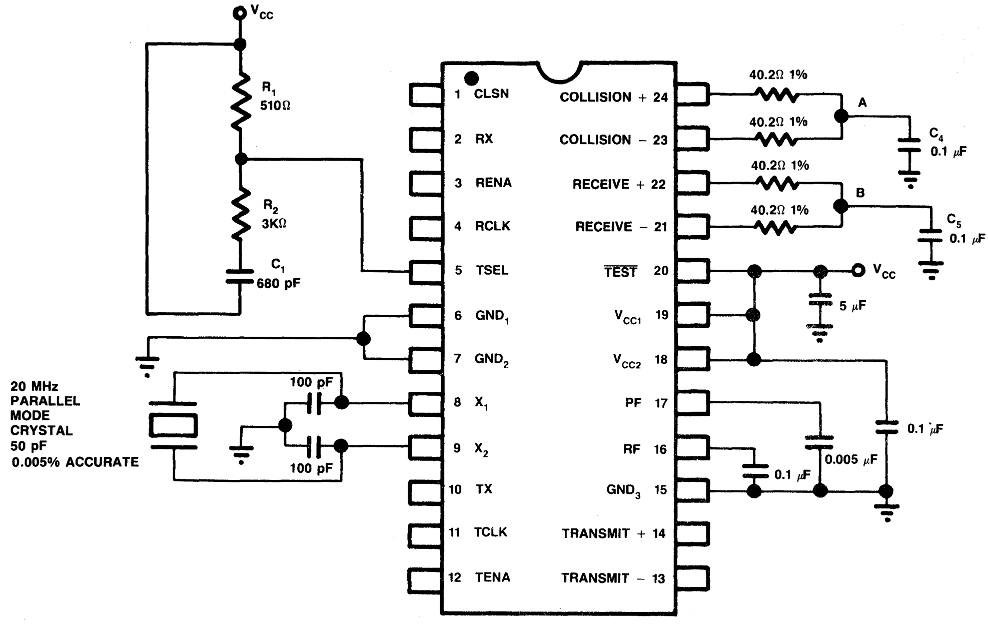


Figure 7. Maximum Jitter Impact On Sampling



NOTES:

1. Connect R_1, R_2, C_1 for 0 differential nontransmit. Connect to ground for logic 1 differential nontransmit. (See Figure 9.)
2. Pin 20 shown for normal device operation.
3. Nodes A and B may be connected directly to ground for proper decoder operations, or to the common mode bypass C_4 and C_5. Some direct coupled transceivers require C_4 and C_5 to ground for proper operation.

Figure 8. MK68591/2 External Component Diagram

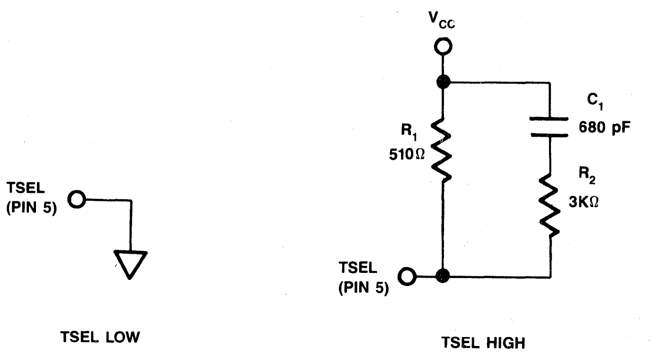


Figure 9. Transmit Mode Select (TSEL) Connection

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature .... −65 to +150°C
Temperature (Ambient) Under Bias .... 0 to 70°C
Supply Voltage to Ground Potential Continuous .... +7.0V
DC Voltage Applied to Outputs for High Output State .... −0.5 to $+V_{CC}$ max
DC Input Voltage (Logic Inputs) .... +5.5V
DC Input Voltage (Receive/Collision) .... −6 to +6 V
Transmit ± Output Current .... −50 to +5 mA
DC Output Current, Into Outputs .... 100 mA
DC Input Current (Logic Inputs) .... ±30 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE The following conditions apply unless otherwise specified:

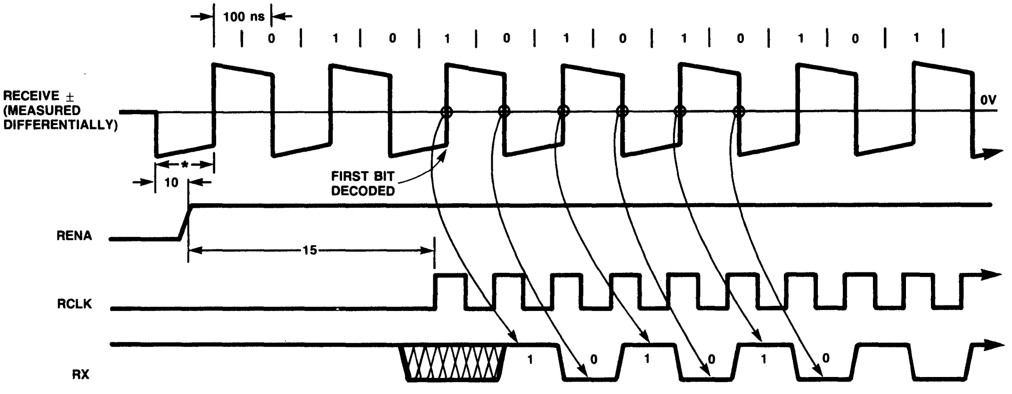
T_A = 0 to 70°C, V_{CC} = 5.0 V±10 percent, MIN = 4.5 V, MAX = 5.5 V, period of crystal oscillator (T_{OSC}) = 50 ns

Parameters	Description		Test Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage RX, RENA, CLSN, TCLK, RCLK		I_{OH} = −1.0 mA	2.4	3.4		V
V_{OL}	Output Low Voltage RCLK, TCLK, RENA, RX, CLSN, TSEL		I_{OL} = 16 mA,		0.36	0.5	V
			I_{OL} = 1 mA		0.25	0.4	
V_{OD}	Differential Output Voltage	V_0	R_L = 78 Ω	550	670	770	mV
	(Transmit +) − (Transmit −)	$\overline{V_0}$	Figure 19	−550	−670	−770	
$V_{OD\ OFF}$	Transmit Differential Output Idle Voltage		R_L =78 Ω Figure 19 TSEL = HIGH	−20	0.5	20	mV
$I_{OD\ OFF}$	Transmit Differential Output Idle Current			−0.5	±0.1	0.5	mA
V_{CMT}	Common Mode Output Transmit Voltage		Figure 19	0	2.5	5	V
V_{ODI}	Differential Output Voltage Imbalance (Transmit ±) $\lvert\,\lvert V_0\rvert - \lvert\overline{V_0}\rvert\,\rvert$		R_L = 78 Ω		5	20	mV
V_{IH}	Input High Voltage TTL			2.0			V
I_{IH}	Input High Current TTL		V_{CC} = Max, V_{IN} = 2.7 V			+50	μA
V_{IL}	Input Low Voltage TTL					0.8	V
I_{IL}	Input Low Current TTL		V_{CC} = Max, V_{IN} = 0.4 V		−270	−400	μA
V_{IRD}	Differential Input Threshold (Rec Data)		Figure 20	−25	0	+25	mV
V_{IDC}	Differential Input Threshold (Carrier/Collision ±)		Figure 20	−175	−225	−275	mV
I_{CC}	Power Supply Current		t_{OSC} = 50 ns		125	180	mA
			t_{OSC} = 50 ns, T_A = Max			160	
V_{IB}	Input Breakdown Voltage V_I = +5.5 (TX, TENA, $\overline{TEST}$)		I_I = 1 mA	5.5			V
V_{IC}	Input Clamp Voltage		I_{IN} = −18 mA			−1.2	V
I_{SCO}	RX, TCLK, CLSN, RENA, RCLK Short Circuit Current			−40	−80	−150	mA
R_{IDF}	Differential Input Resistance		V_{CC} = 0 to Max	6k	8.4k	13k	ohm
R_{ICM}	Common Mode Input Resistance		V_{CC} = 0 to Max	1.5k	2.1k	7.5k	ohm
V_{ICM}	Receive and Collision Input Bias Voltage		I_{IN} = 0	1.5	3.5	4.2	V
I_{ILD}	Receive and Collision Input Low Curent		V_{IN} = −1 V	−0.6	−1.06	−1.64	mA
I_{IHD}	Receive and Collision Input High Current		V_{IN} = 6 V	+0.4	+0.6	+1.10	mA
I_{IHZ}	Receive and Collision Input High Current		V_{CC} = 0, V_{IN} = +6 V	0.4	1.28	1.86	mA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE The following conditions apply unless otherwise specified: $T_A = 0$ to 70°C, $V_{CC} = 5.0$ V±10 percent, MIN = 4.5 V, MAX = 5.5 V, $T_{OSC} = 50$ ns

#	Signal	Parameters	Description	Test Conditions	Min	Typ	Max	Units
RECEIVER SPECIFICATION								
1	RCLK	t_{RCT}	RCLK Cycle Time	$C_L = 50$ pF Figure 17a (See note)	85	100	118	ns
2	RCLK	t_{RCH}	RCLK High Time		38	50		ns
3	RCLK	t_{RCL}	RCLK Low Time		38	50		ns
4	RCLK	t_{RCR}	RCLK Rise Time			2.5	8	ns
5	RCLK	t_{RCF}	RCLK Fall Time			2.5	8	ns
6	RX	t_{RDR}	RX Rise Time			2.5	8	ns
7	RX	t_{RDF}	RX Fall Time			2.5	8	ns
8	RX	t_{RDH}	RX Hold Time (RCLK to RX Change)		5	8		ns
9	RX	t_{RDS}	RX Prop Delay (RCLK to RX Stable)			8	25	ns
10	RENA	t_{DPH}	RENA Turn-On Delay (V_{IDC} Max on Receive ± to $RENA_H$)	Figures 10, 16a, and 20		50	80	ns
11	RENA	t_{DPO}	RENA Turn-Off Delay (V_{IDC} Min on Receive ± to $RENA_L$)	Figures 11 and 20		265	300	ns
12	RENA	t_{DPL}	RENA Low Time	Figure 11	120	200		ns
13	Rec ±	t_{RPWR}	Receive ± Input Pulse Width to Reject (Input$<V_{IDC}$ Min)	Figures 16a and 20		30	20	ns
14	Rec ±	t_{RPWO}	Receive ± Input Pulse Width to Turn-On (Input$>V_{IDC}$ Max)	Figures 16a and 20	45	30		ns
15	RCLK	t_{RLT}	Decoder Acquisition Time	Figure 10		390	450	ns
COLLISION SPECIFICATION								
16	Coll ±0	t_{CPWR}	Collision Input Pulse Width to Reject (Input$<V_{IDC}$ Min)	Figures 16b and 20		18	10	ns
17	Coll ±	t_{CPWO}	Collision Input Pulse Width to Turn-On (Collision ± Exceeds V_{IDC} Max)		26	18		ns
18	Coll ±	t_{CPWE}	Collision Input to Turn-Off CLSN (Input$<V_{IDC}$ Max)		80	117		ns
19	Coll ±	t_{CPWN}	Collision Input to Not Turn-Off CLSN (Input$>V_{IDC}$ Min)			117	160	ns
20	CLSN	t_{CPH}	CLSN Turn-On Delay (V_{IDC} Max on Collision ± to $CLSN_H$)	Figures 15, 16b, and 20		33	50	ns
21	CLSN	t_{CPO}	CLSN Turn-Off Delay (V_{IDC} Min on Collision ± to $CLSN_L$)			133	160	ns
TRANSMITTER SPECIFICATION								
22	TCLK	t_{TCL}	TCLK Low Time	$t_{OSC} = 50$ ns Figures 17b and 18	45	50	55	ns
23	TCLK	t_{TCH}	TCLK High Time		45	50	55	ns
24	TCLK	t_{TCR}	TCLK Rise Time			2.5	8	ns
25	TCLK	t_{TCF}	TCLK Fall Time			2.5	8	ns
26	TX, TENA	t_{TDS}, t_{TES}	TX and TENA Setup Time to TCLK	Figures 13, 14a, 14b, and 17b	5	1.1		ns
27	TX, TENA	t_{TDH}, t_{TEH}	TX and TENA Hold Time to TCLK		5	−1.1		ns
28	TX ±	t_{TOCE}	Transmit ± Output, (Bit Cell Center to Edge)	Figures 14a, 14b, and 19	49.5	50	50.5	ns
29	TCLK	t_{OD}	TCLK High to Transmit ± Output			80	100	ns
30	TX ±	t_{TOR}	Transmit ± Output Rise Time	20 through 80 percent Figure 19		2	4	ns
31	TX ±	t_{TOF}	Transmit ± Output Fall Time			2	4	ns
32	TX ±	V_{OD}	Undershoot Voltage at Zero Differential Point on Transmit Return to Zero (End of Message)	Figure 14a			−100	mV

NOTE:
Assumes equal capacitance loading on RCLK and RX.



* PULSE WIDTH OF ≥ 45 ns IS ALWAYS RECOGNIZED.
HOWEVER, PULSE WIDTH OF ≤ 20 ns IS REJECTED.

Figure 10. Receiver Timing — Start of Packet

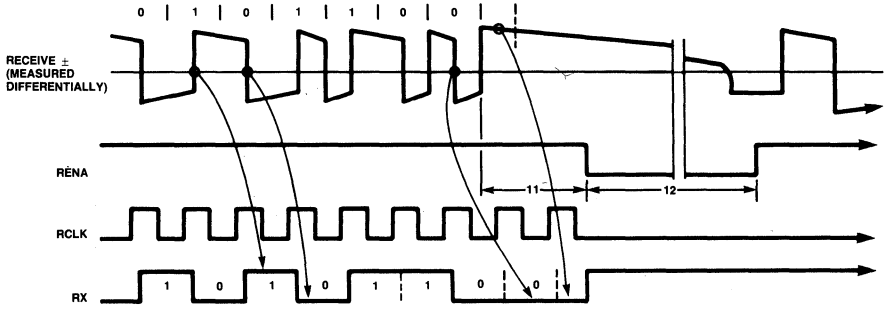


Figure 11. Receiver Timing — End of Packet (Last Bit = 0)

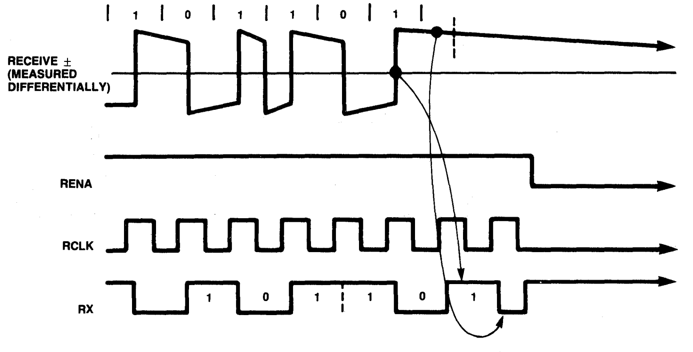


Figure 12. Receiver Timing — End of Packet (Last Bit = 1)

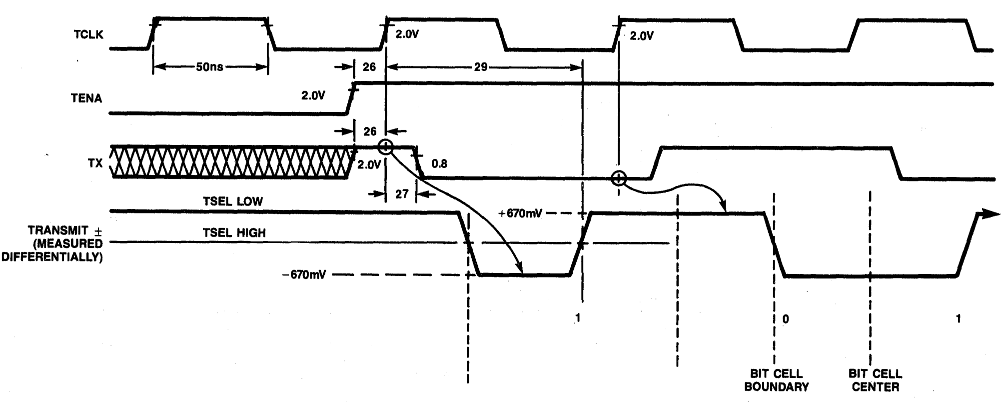


Figure 13. Transmitter Timing — Start of Transmission (TSEL Low, TSEL High)

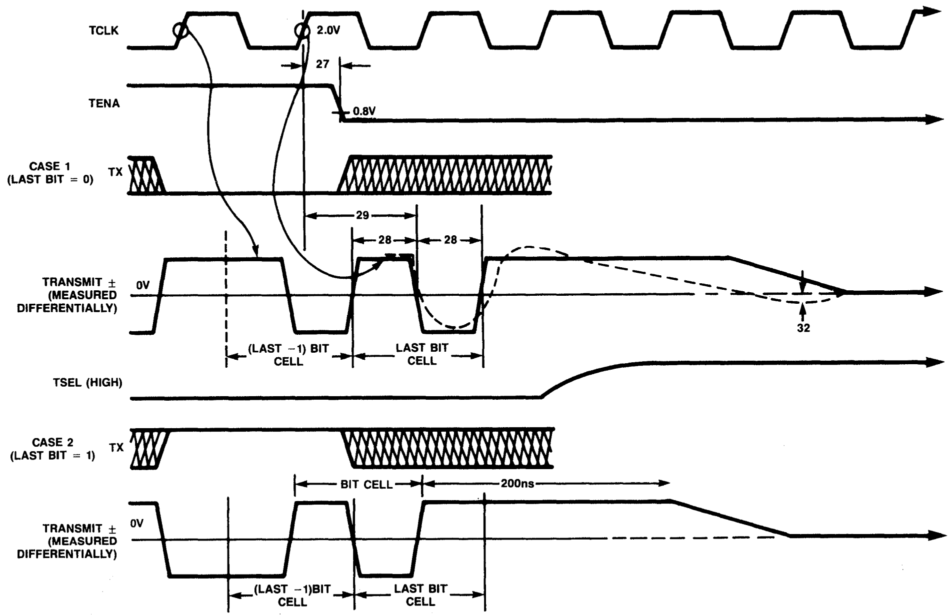


Figure 14a. Transmitter Timing — End of Transmission (TSEL High)

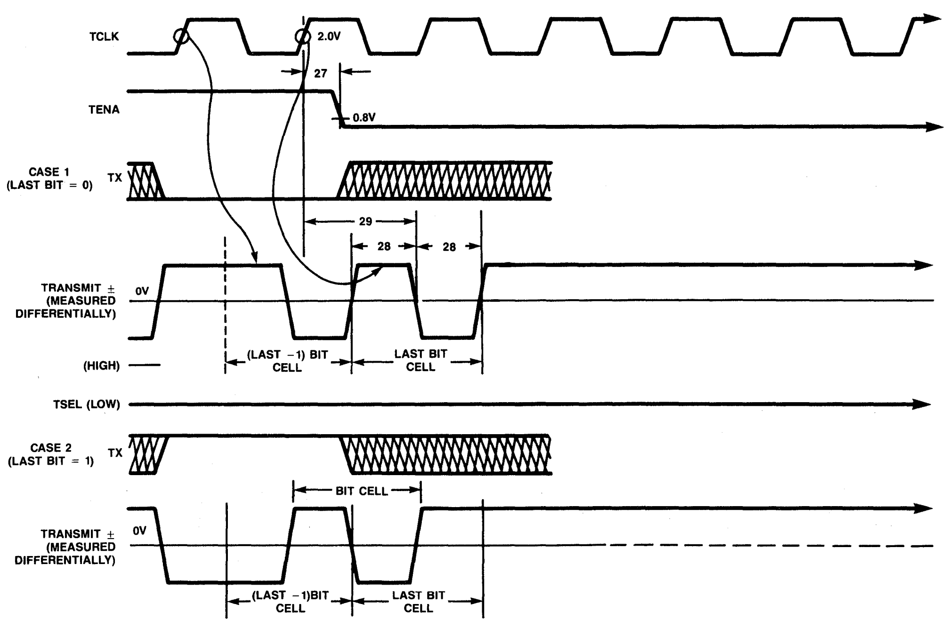
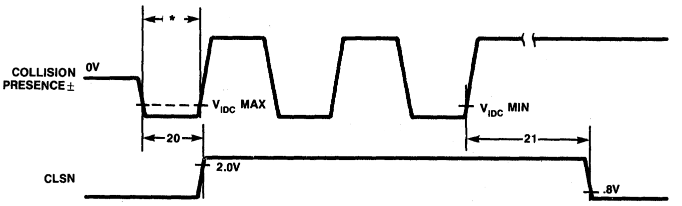


Figure 14b. Transmitter Timing — End of Transmission (TSEL Low)



* PULSE WIDTH OF −26 ns IS GUARANTEED TO BE RECOGNIZED: HOWEVER, PULSE WIDTH OF ≤ 10ns IS REJECTED

Figure 15. Collision Timing

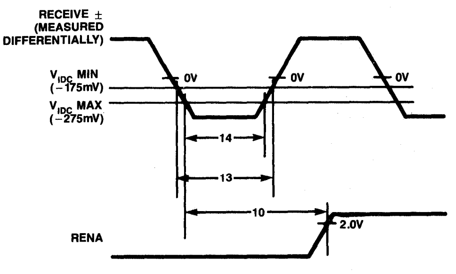


Figure 16a. Receive ± Input Pulse Width Timing

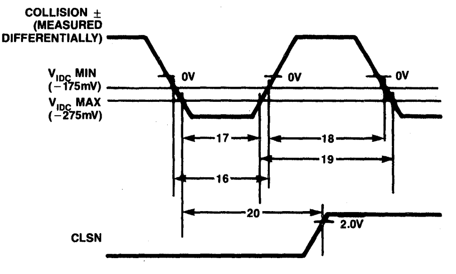


Figure 16b. Collision ± Input Pulse Width Timing

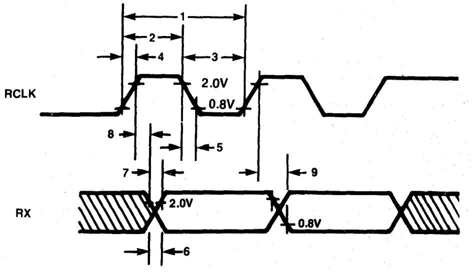


Figure 17a. RCLK and RX Timing

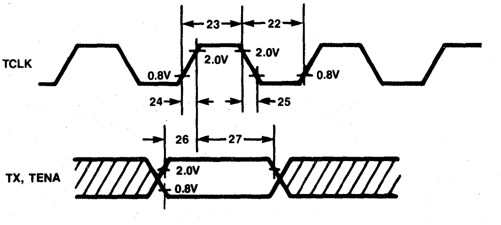


Figure 17b. TCLK and TX Timing

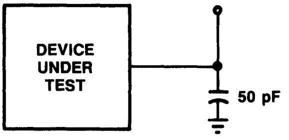


Figure 18. Test Load For RX, RENA, and TCLK

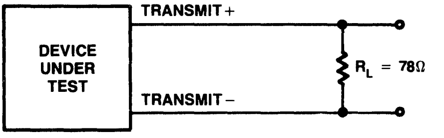


Figure 19. Transmit ± Output Test Circuit

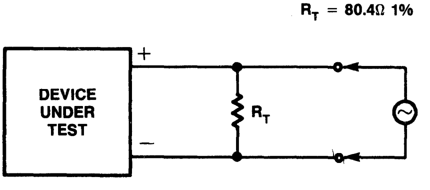
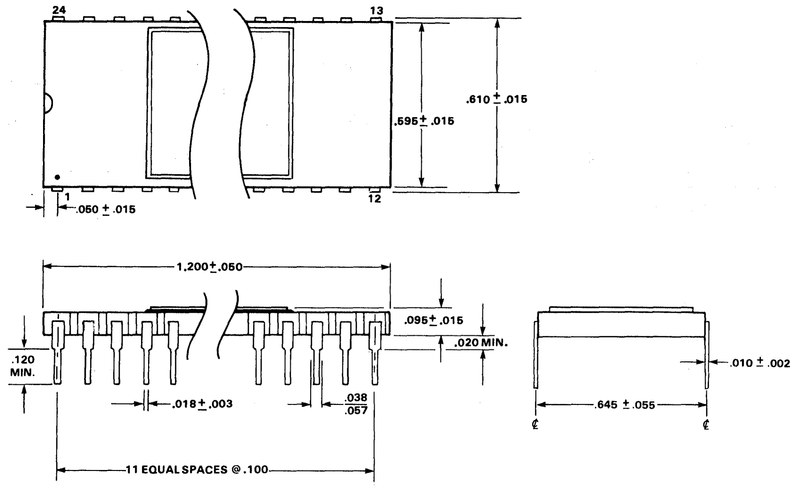


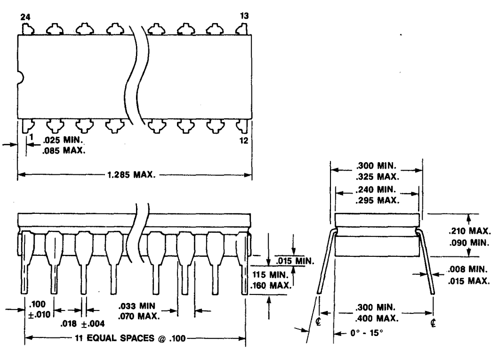
Figure 20. Receive ± and Collision ± Input Test Circuit

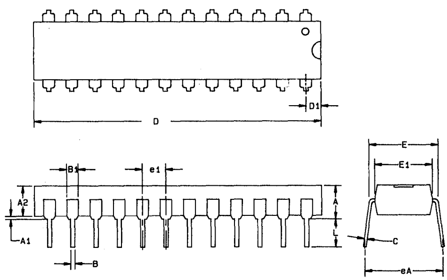
MK68591 (600 mil)



Ceramic Dual-In-Line Package (P)
24 Pin

MK68592 (300 mil)





NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

DIM	INCHES		NOTES
	MIN	MAX	
A	-	.210	2
A1	.015	-	2
A2	.120	.140	
B	.015	.021	3
B1	.050	.070	
C	.008	.012	3
D	1.220	1.250	1
D1	.060	.075	
E	.300	.325	
E1	.240	.270	
e1	.090	.110	
eA	.300	.400	
L	.120	-	

Cerdip Hermetic Package (J)
24 Pin

Plastic Package (N)
24 Pin