PRELIMINARY

LOCAL AREA NETWORK CONTROLLER FOR ETHERNET MK68590

FEATURES

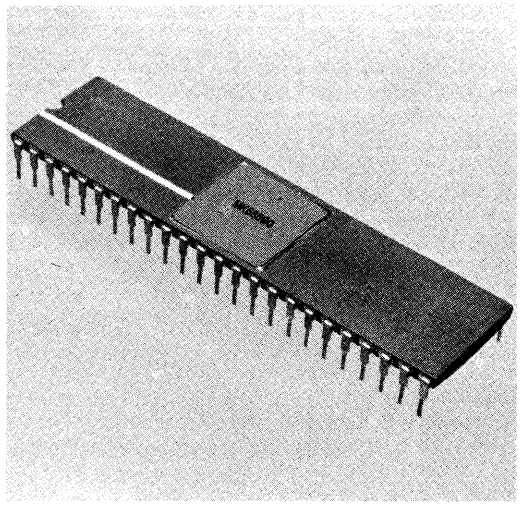
- ☐ 100% compatible Ethernet serial port
- ☐ Data packets moved by block transfers over a processor bus (on-board DMA controller 24-bit linear address space)
- ☐ Buffer management
- ☐ Packet framing
- ☐ Preamble and CRC insertion
- ☐ Preamble stripping and CRC checking
- ☐ General 16-bit microprocessor bus interface compatible with popular processors (68000, 8086, Z800[illegible] LSI-11)
- ☐ Cable fault detection
- ☐ Multicast logical address filtration
- ☐ Collision handling and retry
- ☐ Scaled N-channel MOS VLSI technology
- ☐ 48-pin DIP
- ☐ Single 5-volt power supply
- ☐ Single phase TTL level clock
- ☐ All inputs and outputs TTL compatible
- ☐ Completely compatible with companion Serial Interface Adapter (SIA) chip. (MK68591)

DESCRIPTION

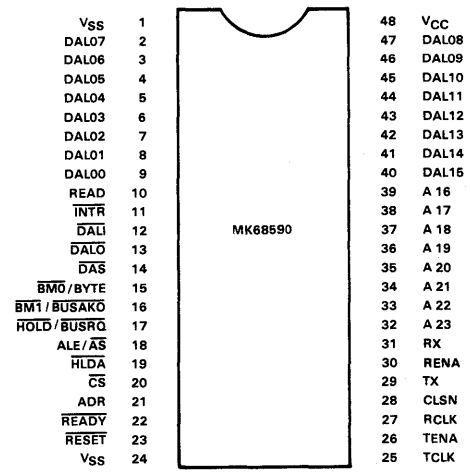
The MK68590-LANCE™ (Local Area Network Controller for Ethernet) is a 48-pin VLSI device designed to simplify greatly the interfacing of a microcomputer or a minicomputer to an Ethernet Local Area Network. This chip operates in a local environment that includes a closely coupled memory and microprocessor. The LANCE uses scaled N-channel MOS technology and is compatible with several microprocessors.

LANCE is a trademark of Mostek Corporation.

MK68590
Figure 1



LANCE PIN ASSIGNMENT
Figure 2



PIN DESCRIPTION

DAL00-DAL15
(Data/Address Bus)
Input/Output Tri-State. The time multiplexed Address/Data bus. These lines will be driven as a Bus Master and as a Bus Slave.

READ
Input/Output Tri-State. Indicates the type of operation to be performed in the current bus cycle. When it is a Bus Master, LANCE drives this signal.

LANCE as Bus Slave:
High - The chip places data on the DAL lines.
Low - The chip takes data off the DAL lines.
LANCE as Bus Master:
High - The chip takes data off the DAL lines.
Low - The chip places data on the DAL lines.

INTR
(Interrupt)
Output Open Drain. When enabled, an attention signal that indicates the occurrence of one or more of the following events: a message reception or transmission has completed or an error has occurred during the transaction; the initialization procedure has completed; or a memory error has been encountered. Programming register (CSR0) enables INTR.

DALI
(Data/Address Line In)
Output Tri-State. An external bus transceiver control line. When LANCE is a Bus Master and reads from the DAL lines, DALI is asserted.

DALO
(Data/Address Line Out)
Output Tri-State. An external bus transceiver control line. When LANCE is a Bus Master and drives the DAL lines, DALO is asserted.

DAS
(Data/Strobe)
Input/Output Tri-State. Defines the data portion of the bus transaction. DAS is driven only as a Bus Master.

BM0, BM1 or BYTE, BUSAKO
(Byte Mask)
Output Tri-State. Pins 15 and 16 are programmable through bit (00) of CSR3 (known as BCON). Asserting RESET clears CSR3.

If BCON = 0
PIN 16 = BM 1 (Output Tri-State)
PIN 15 = BM 0 (Output Tri-State)

BM0, BM1 Byte Mask. Indicates the byte(s) of a bus transaction to read or written. The BM lines are ignored as a Bus Slave and assume word transfers only. The LANCE drives the BM lines only when it is a Bus Master. Byte selection occurs as follows:

BM1	BM0	
LOW	LOW	Whole Word
LOW	HIGH	Byte of DAL 08 - DAL 15
HIGH	LOW	Byte of DAL 04 - DAL 07
HIGH	HIGH	None

If BCON = 1
PIN 16 = BUSAKO (Output)
PIN 15 = BYTE (Output Tri-State)

Byte. An alternate byte selection line. Byte selection occurs when the BYTE and DAL (00) lines are latched during the address portion of the bus transaction. BYTE, BM0 and BM1 are ignored as Bus Slaves. There are two modes of ordering bytes depending on bit (02) of CSR3, (known as BSWP). This programmable ordering of upper and lower bytes when using BYTE and DAL (00) as selection signals is required to make the ordering compatible with various 16-bit microprocessors.

BSWP = 0		BSWP = 1		
BYTE	DAL(00)	BYTE	DAL(00)	
LOW	LOW	LOW	LOW	WHOLE WORD
LOW	HIGH	LOW	HIGH	ILLEGAL CONDITION
HIGH	HIGH	HIGH	LOW	UPPER BYTE
HIGH	LOW	HIGH	HIGH	LOWER BYTE

BUSAKO. The DMA daisy chain output.

HOLD/BUSRQ
(Bus Hold Request)
Input/Output Open Drain. LANCE asserts this signal when it requires access to memory. HOLD is held LOW for the entire bus transaction. This bit is programmable through bit (00) of CSR3 (known as BCON). In the daisy chain DMA mode (BCON = 1) BUSRQ is asserted only if BUSRQ is inactive prior to assertion. Bit (00) of CSR3 is cleared when RESET is asserted.

CSR3(00) BCON = 0
PIN 17 = HOLD (Output Open Drain)
CSR3(00) BCON = 1
PIN 17 = BUSRQ (Output Open Drain)
BUSRQ will be asserted only if PIN 17 is high prior to assertion.

ALE/AS
(Address Latch Enable)
Output Tri-State. Used to demultiplex the DAL lines and define the address portion of the bus cycle. This I/O pin is programmable through bit (01) of CSR3. As ALE, the signal transitions from a HIGH to a LOW at the end of

the address portion of the bus transaction and remains LOW during the entire data portion of the transaction. As $\overline{AS}$, the signal transitions from a LOW to a HIGH at the end of the address portion of the bus transaction and remains HIGH throughout the entire data portion of the transaction. The LANCE drives the ALE/$\overline{AS}$ line only as a Bus Master.

CSR3(01) ACON = 0
PIN 31 = ALE
CSR3(01) ACON = 1
PIN 31 = AS

$\overline{HLDA}$
(Bus Hold Acknowledge)
Input. A response to $\overline{HOLD}$ indicating that the LANCE is the Bus Master. $\overline{HLDA}$ stops its response when $\overline{HOLD}$ ends its assertion.

$\overline{CS}$
(Chip Select)
Input. When asserted, $\overline{CS}$ indicates LANCE is the slave device of the data transfer. $\overline{CS}$ must be valid throughout the data portion of the bus cycle.

ADR
(Register Address Port Select)
Input. When $\overline{CS}$ is asserted, ADR indicates which of the two register ports is selected. ADR must be valid throughout the data portion of the bus cycle.

ADR	PORT
LOW	Register Data Port
HIGH	Register Address Port

$\overline{READY}$
Input/Output Open Drain. When the LANCE is a bus master, $\overline{READY}$ is an asynchronous acknowledgement from external memory that will complete the data transfer. As a bus slave, the chip asserts $\overline{READY}$ when it has put data on the bus, or is about to take data off the bus. $\overline{READY}$ is a response to $\overline{DAS}$. $\overline{READY}$ negates after $\overline{DAS}$ negates. Note: If $\overline{DAS}$ or $\overline{CS}$ deassert prior to the assertion of $\overline{READY}$, $\overline{READY}$ cannot assert.

$\overline{RESET}$
Input. Bus reset signal. Causes LANCE to cease operation, and enter an idle state.

TLCK
(Transmit Clock)
Input. Normally a free-running 10 MHz clock. (Crystal-controlled within .01% accuracy.)

TENA
(Transmit Enable)
Output. Transmit Output Stream Enable. A level asserted with the transmit output bit stream, TX, to enable the external transmit logic.

RCLK
(Receive Clock)
Input. Normally a 10MHz square wave synchronized to the Receive data and only present while receiving an input bit stream.

CLSN
(Collision)
Input. A logical input that indicates that a collision is occurring on the channel.

TX
(Transmit)
Output. Transmit Output Bit Stream.

RENA
(Receive Enable)
Input. A logical input that indicates the presence of data on the channel.

RX
(Receive)
Input. Receive Input Bit Stream.

A16-A23
(High-Order Address Bus)
Output Tri-State. The additional address bits necessary to extend the DAL lines to produce a 24-bit address. These lines will be driven as a Bus Master only.

VCC
Power supply pin. +5 VDC ±5%

VSS
Ground. 0 VDC

FUNCTIONAL CAPABILITIES

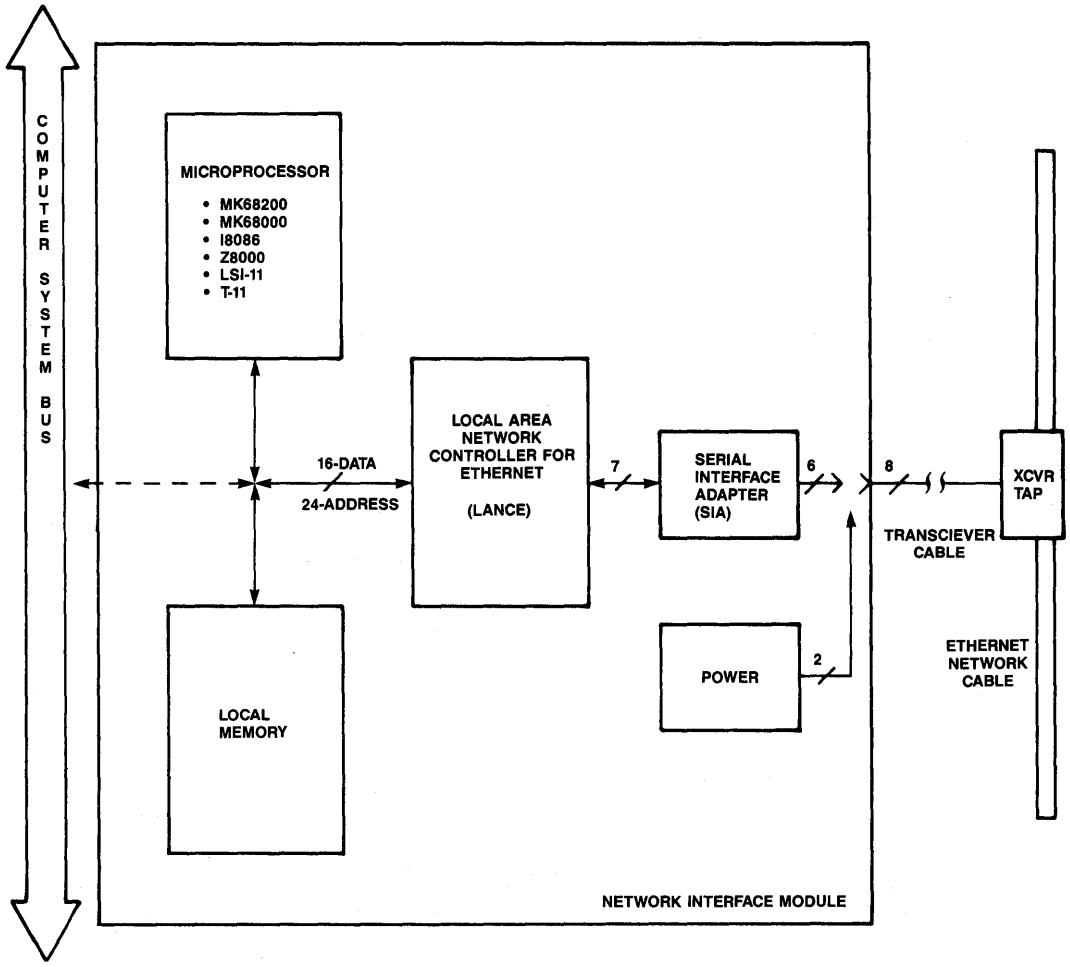
The Local Area Network Controller for Ethernet (LANCE) interfaces to a microprocessor bus characterized by time multiplexed address and data lines. Typically, data transfers are 16 bits wide but byte transfers occur if the buffer memory address boundaries are odd. The address bus is 24 bits wide.

The Ethernet packet format consists of 64-bit preamble, a 48-bit destination address, a 48-bit source address, a 16-bit type field, and from a 46 to 1500 byte data field terminated with a 32-bit CRC. The packets' variable widths accommodate both short status, command and terminal traffic packets, and long data packets to printers and disks (1024 byte disk sectors, for example). Packets are spaced a minimum of 9.6 μsec apart to allow one node enough time to receive back-to-back packets.

The LANCE operates in a minimal configuration that requires close coupling between local memory and a processor. The local memory provides packet buffering for the chip and serves as a communication link between

the chip and the processor. During initialization, the control processor loads the starting address of the initialization block plus the operating mode of the chip via two control registers into LANCE. The host processor talks directly to LANCE only during this initial phase. All further communications are handled via a DMA machine under microword control contained within LANCE. Figure 3 shows a block diagram of the LANCE and SIA device used to create an Ethernet interface for a computer system.

ETHERNET LOCAL AREA NETWORK SYSTEM BLOCK DIAGRAM
Figure 3



FUNCTIONAL DESCRIPTION

SERIAL DATA HANDLING

LANCE provides the Ethernet interface as follows. In the transmit mode (since there is only one transmission path, Ethernet is a half duplex system), the LANCE reads data from a transmit buffer by using Direct Memory Access (DMA) and appends the preamble, sync pattern (two ones after alternating ones and zeros in the preamble), and calculates and appends the complement of the 32-bit CRC. In the receive mode, the destination address, source address, type, data, and CRC fields are transferred to memory via DMA cycles. The CRC is calculated as data and transmitted CRC is received. At the end of the packet, if this calculated CRC does not agree with a constant, an error bit is set and an interrupt is generated to the microprocessor. In the receive mode, LANCE accepts packets under four modes of operation. The first mode is a full comparison of the 48-bit destination address in the packet with the node address that was programmed into the LANCE during an initialization cycle. There are two types of logical addresses. One is a group type mask where the 48-bit address in the packet is put through a hash filter in order to map the 48-bit physical addresses into 1 of 64 logical groups. This mode can be useful if sending packets to all of one type of a device simultaneously on the network. (i.e., send a packet to all file servers or all printer servers). The second logical address is a multicast address where all nodes on the network receive the packet. The last receive mode of operation is the so called "promiscuous mode" in which a node will accept all packets on the coax regardless of their destination address.

COLLISION DETECTION AND IMPLEMENTATION

The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear network cable before transmitting, Ethernet handles collisions in a predetermined way. Should two transmitters attempt to seize the network cable at the same time, they will collide, and the data on the network cable will be garbled. LANCE is constantly monitoring the CLSN (Collision) pin. This signal is generated by the transceiver when the signal level on the network cable indicates the presence of signals from two or more transmitters. If LANCE is transmitting when CLSN is asserted, it will continue to transmit the preamble, (normally collisions will occur while the preamble is being transmitted) then will "jam" the network for 32 bit times (3.2 microseconds). This jamming ensures that all nodes have enough time to detect the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm defined in the Ethernet specification to minimize the probability of the colliding nodes having multiple collisions with each other. After 16 abortive attempts to transmit a packet, LANCE will report a RTRY error due to excessive collisions and step over the transmitter buffer. During reception, the detection of a collision causes that reception to be aborted. Depending on when the collision occurred, LANCE will treat this packet as an error packet if the packet has an address mismatch, as a runt packet (a packet that has less than 64 bytes), or as a legal length packet with a CRC error.

Extensive error reporting is provided by the LANCE through a microprocessor interrupt and error bits in a status register. The following are the significant error conditions: CRC error on received data; transmitter on longer than 1518 bytes; missed packet error (meaning a packet on the network cable was missed because there were no empty buffers in memory), and memory error, in which the memory did not respond (handshake) to a memory cycle request.

BUFFER MANAGEMENT

A key feature of the LANCE and its DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings, as shown in Figure 4. Separate descriptor rings describe either transmit or receive operations. Up to 128 tasks may be queued on a descriptor ring for execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the data buffer length. Data buffers can be chained or cascaded to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings to determine the next empty buffer. This enables it to chain buffers together or to handle back-to-back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer.

MICROPROCESSOR INTERFACE

The parallel interface of the LANCE has been designed to be "friendly" or easy to interface to many popular 16-bit microprocessors. These microprocessors include the following: MK68000, Z8000, 8086, LSI-11, T-11, and MK68200. (The MK68200 is a 16-bit single chip microcomputer being sampled by Mostek with an architecture modeled after the MK68000). The LANCE has a wide 24-bit linear address space when it is in the Bus Master Mode, allowing it to DMA directly into the entire address space of the above microprocessors. The LANCE uses no segmentation or paging methods and as such the addressing is closest to MK68000 addressing. However, it is compatible with the others. When the LANCE is a Bus Master, a programmable mode of operation allows byte addressing either by employing a Byte/Word control signal, much like that used on the 8086 or the Z8000, or by using an Upper Data Strobe/Lower Data Strobe much like that used on the MK68000, LSI-11 and MK68200 microprocessors. A programmable polarity on

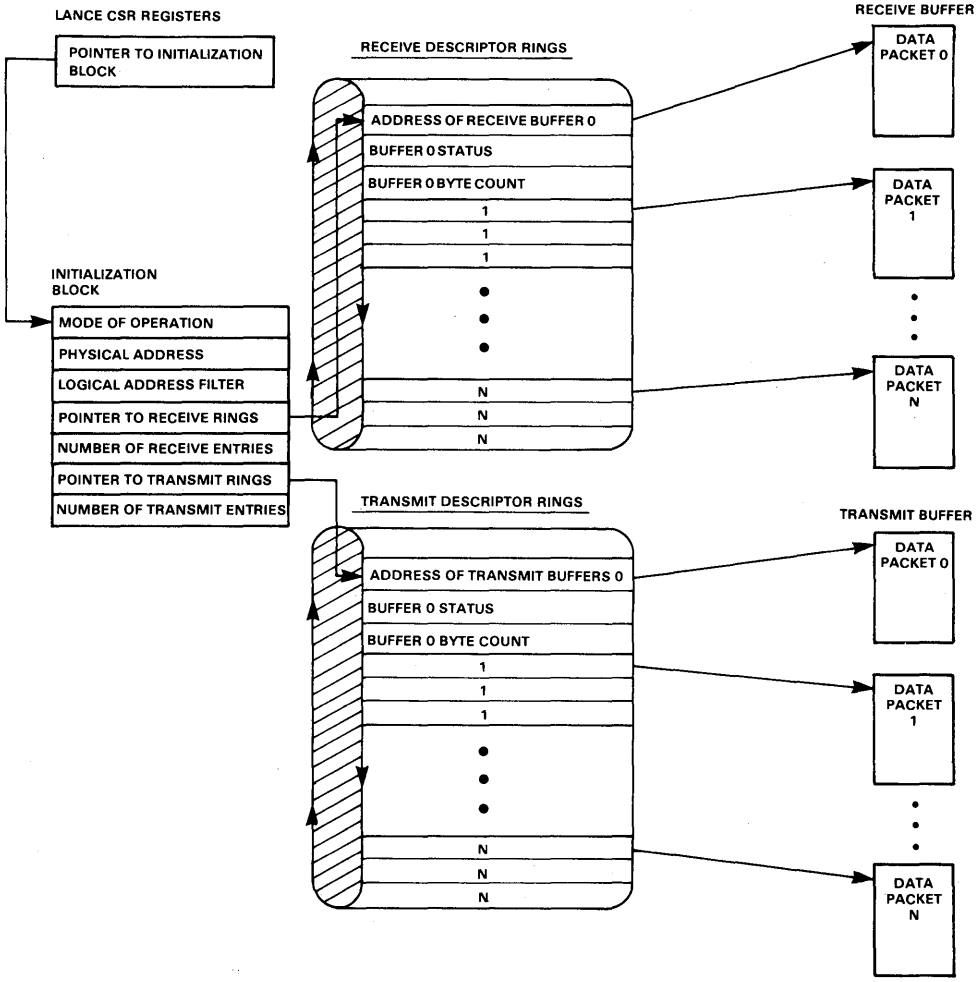
the Address Strobe signal eliminates the need for external logic. LANCE interfaces with multiplexed and demultiplexed data busses and features control signals for address/data bus transceivers.

After the initialization routine, packet reception and transmission, transmitter timeout error, a missed packet, and memory error, LANCE generates interrupts to the microprocessor.

The cause of the interrupt is ascertained by reading CSR0. Bit (06) of CSR0, INEA, enables or disables interrupts to the microprocessor. In a polling mode, BIT (07) of CSR0 is sampled to determine when an interrupt causing condition occurred.

LANCE MEMORY MANAGEMENT

Figure 4



LANCE INTERFACE DESCRIPTION

ALE, $\overline{DAS}$ and $\overline{READY}$ time all data transfers from the LANCE in the Bus Master mode. The automatic adjustment of the LANCE cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600 ns long and can be increased in 100 ns increments.

READ SEQUENCE

At the beginning of a read cycle, valid addresses are placed on DAL00-DAL15 and A16-A21. The BYTE Mask signals ($\overline{BM0}$ and $\overline{BM1}$) become valid at the beginning of this cycle as does READ, indicating the type of cycle. The trailing edge of ALE or $\overline{AS}$ strobes the addresses A0-A15 into the external latches. Approximately 100 ns later, DAL00-DAL15 go into a tri-state mode. There is a 50 ns delay to allow for transceiver turnaround, then $\overline{DAS}$ falls low to signal the beginning of the data portion of the cycle. At this point in the cycle, the LANCE stalls waiting for the memory device to assert $\overline{READY}$. Upon assertion of $\overline{READY}$, $\overline{DAS}$ makes a transition from a zero to a one, latching memory data. ($\overline{DAS}$ is low for a minimum of 200 ns).

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, control the bus transceivers. $\overline{DALI}$ signals to strobe data toward the LANCE and $\overline{DALO}$ signals to strobe data or addresses away from the LANCE. During a read cycle, $\overline{DALO}$ goes inactive before $\overline{DALI}$ goes active to avoid "spiking" of bus transceivers.

WRITE SEQUENCE

The write cycle begins exactly like a read cycle with the READ line remaining inactive. After ALE or $\overline{AS}$ pulse, the DAL00-DAL15 change from addresses to data. $\overline{DAS}$ goes active when the DAL00-DAL15 are stable. This data remains valid on the bus until the memory device asserts $\overline{READY}$. At this point, $\overline{DAS}$ goes inactive, latching data into the memory device. Data is held for 75 ns after the negation of $\overline{DAS}$.

LANCE INTERFACE DESCRIPTION — BUS SLAVE MODE

The LANCE enters the Bus Slave Mode whenever $\overline{CS}$ becomes active. This mode must be entered whenever writing or reading the four status control registers (CSR0, CSR1, CSR2, and CSR3) and the register address pointer (RAP). RAP and CSR0 may be read or written to at any time, but the LANCE must be stopped for CSR1, CSR2, and CSR3 to be written to.

MK68590 ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias . . . . . −25°C to +100°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . −7 V to +7 V
Power Dissipation . . . . . 2.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A=0°C to 70°C, V_{CC} = +5 V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{IL}		−0.5	+0.8	V
V_{IH}		+2.0	V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA		+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA	+2.4		V
I_{IL}	@ V_{in} = 0.4 to V_{CC}		±10	μA

CAPACITANCE

F=1 MHz

SYMBOL	PARAMETER	MIN	MAX	UNITS
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

#	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
1	TCLK	T_{TCT}	TCLK period		99		101
2	TCLK	T_{TCL}	TCLK low time		45		55
3	TCLK	T_{TCH}	TCLK high time		45		55
4	TCLK	T_{TCR}	Rise time of TCLK		0		8
5	TCLK	T_{TCF}	Fall time of TCLK		0		8
6	TENA	T_{TEP}	TENA propagation delay after the rising edge of TCLK	CL = 50 pf			95
7	TENA	T_{TEH}	TENA hold time after the rising edge of TCLK	CL = 50 pf	5		

AC TIMING SPECIFICATIONS (CONTINUED)
T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

#	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
8	TX	T_{TDP}	TX data propagation delay after the rising edge of TCLK	CL=50 pf			95
9	TX	T_{TDH}	TX data hold time after the rising edge of TCLK	CL=50 pf	5		
10	RCLK	T_{RCT}	RCLK period		85		118
11	RCLK	T_{RCH}	RCLK high time		38		
12	RCLK	T_{RCL}	RCLK low time		38		
13	RCLK	T_{RCR}	Rise time of RCLK		0		8
14	RCLK	T_{RCF}	Fall time of RCLK		0		8
15	RX	T_{RDR}	RX data rise time		0		8
16	RX	T_{RDF}	RX data fall time		0		8
17	RX	T_{RDH}	RX data hold time (RCLK to RX data change)		5		
18	RX	T_{RDS}	RX data setup time (RX data stable to the rising edge of RCLK)		60		
19	RENA	T_{DPL}	RENA low time		120		
20	CLSN	T_{CPH}	CLSN high time		80		
21	A/DAL	T_{DOFF}	Bus master driver disable after rising edge of $\overline{HOLD}$		0		50
22	A/DAL	T_{DON}	Bus master driver enable after falling edge of $\overline{HLDA}$		0		150
23	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (Bus master)		0		
24	$\overline{RESET}$	T_{RW}	RESET pulse width low		200		
25	A/DAL	T_{CYCLE}	Read/write, address/data cycle time		600		
26	A	T_{XAS}	Address setup time to the falling edge of ALE		75		
27	A	T_{XAH}	Address hold time after the rising edge of $\overline{DAS}$		35		
28	DAL	T_{AS}	Address setup time to the falling edge of ALE		75		
29	DAL	T_{AH}	Address hold time after the falling edge of ALE		35		
30	DAL	T_{RDAS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master read)		50		

AC TIMING SPECIFICATIONS (CONTINUED)
T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

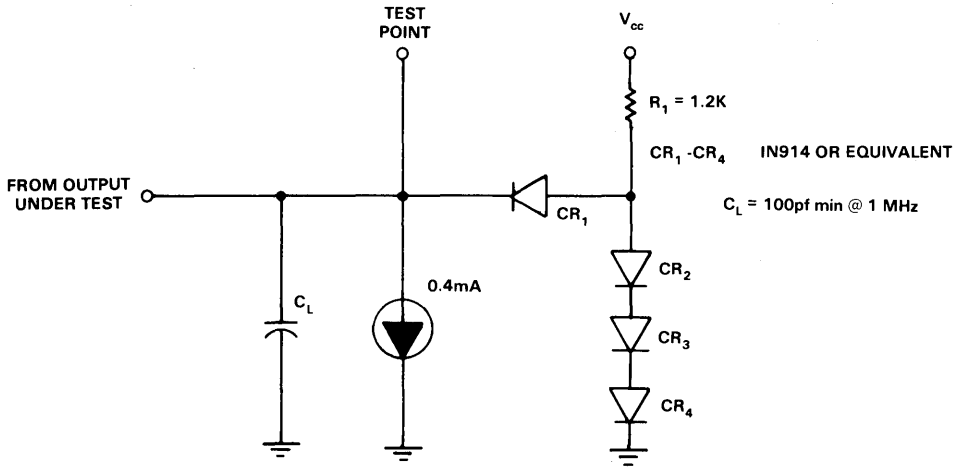
#	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
31	DAL	T_{RDAH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
32	DAL	T_{DDAS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus master write)		0		
33	DAL	T_{WDS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master write)		200		
34	DAL	T_{WDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)		35		
35	DAL	T_{SDO1}	Data driver delay after the falling edge of $\overline{DAS}$ (Bus slave read)	(CSR 0,3, RAP)		400	
36	DAL	T_{SDO2}	Data driver delay after the falling edge of $\overline{DAS}$ (Bus slave read)	(CSR 1,2)		1200	
37	DAL	T_{SRDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)		0		35
38	DAL	T_{SWDH}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
39	DAL	T_{SWDS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
40	ALE	T_{ALEW}	ALE width high		130		
41	ALE	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
42	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width low		200		
43	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		
44	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (BUS master read)		35		
45	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	Taryd= 300 ns	100		250
46	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (Bus master read)		35		
47	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (Bus master read)		135		
48	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
49	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (Bus master read)		55		
50	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of ALE (Bus master read)		110		
51	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (Bus master read)		35		
52	$\overline{DALO}$	T_{WDSI}	Delay from the rising edge of $\overline{DAS}$ to the rising edge of $\overline{DALO}$ (Bus master write)		35		

AC TIMING SPECIFICATIONS (CONTINUED)
T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

#	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
53	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
54	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
55	ADR	T_{SAH}	ADR hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
56	ADR	T_{SAS}	ADR setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
57	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle time (600 ns)				80
58	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (Bus slave read)		75		
59	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus master)		0		
60	$\overline{READY}$	T_{SRO1}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 0, 3, RAP)		600	
61	$\overline{READY}$	T_{SRO2}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 1,2)		1400	
62	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		35
63	READ	T_{SRH}	READ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
64	READ	T_{SRS}	READ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		

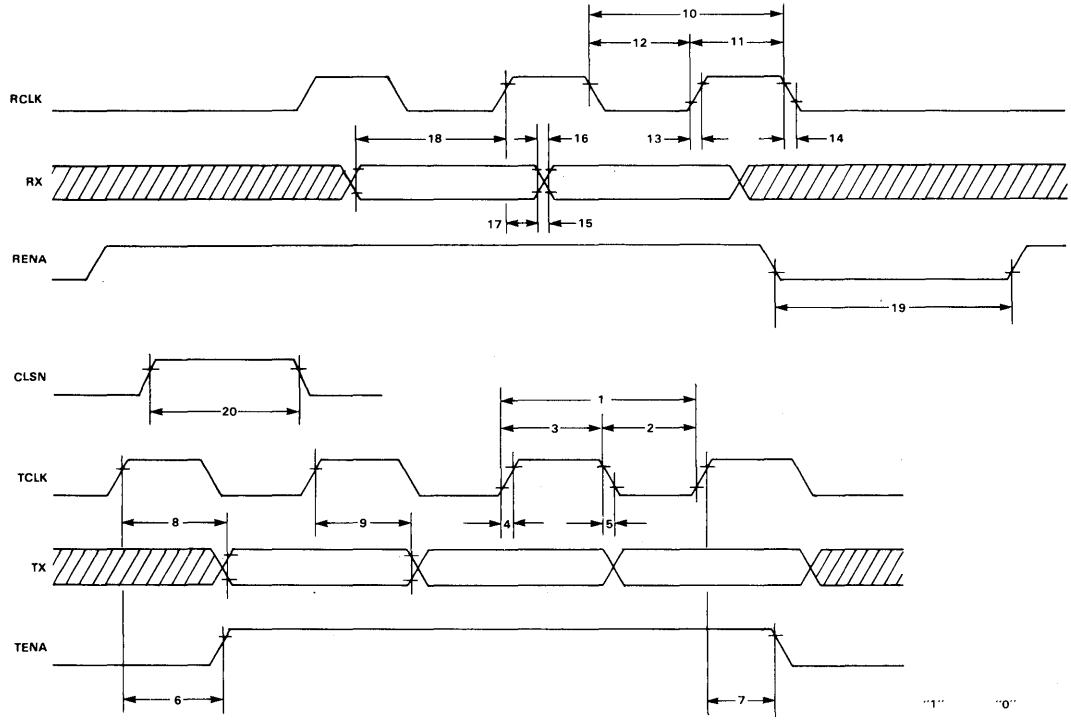
OUTPUT LOAD DIAGRAM

Figure 5



SERIAL LINK TIMING DIAGRAM - SIA INTERFACE SIGNALS

Figure 6

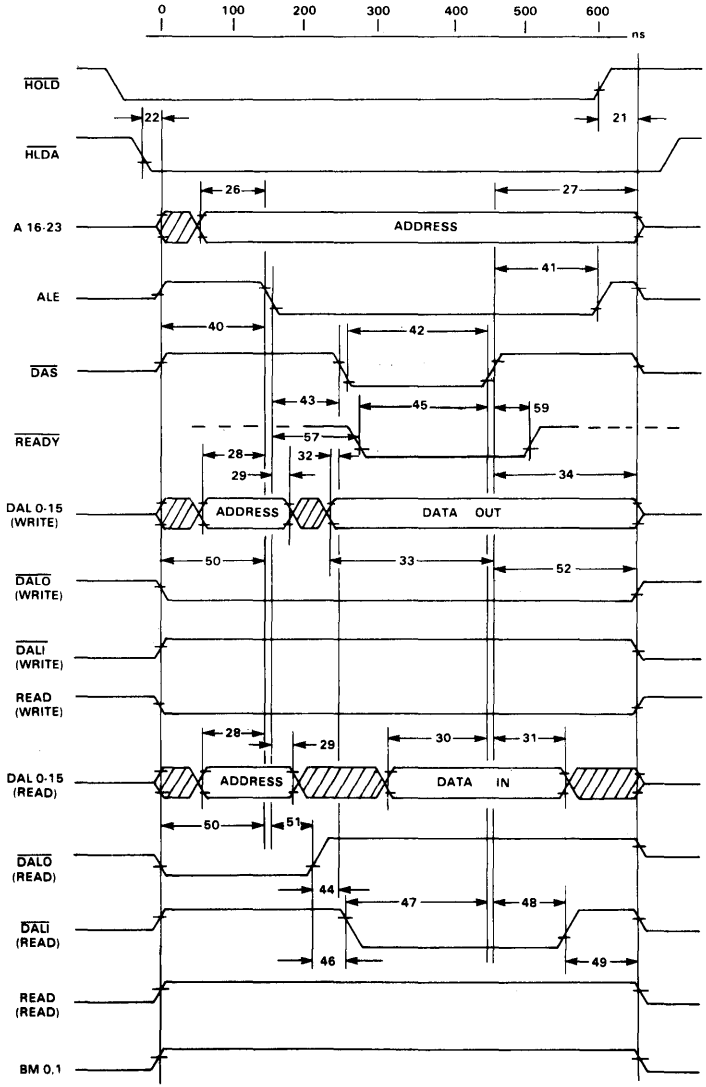


Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8V
FLOAT	V	0.5 V

LANCE BUS MASTER TIMING DIAGRAM

Figure 7



NOTE: The Bus Master cycle time will increase from a minimum of 600 ns in 100 ns steps until the slave device returns $\overline{\text{READY}}$.

LANCE BUS SLAVE TIMING DIAGRAM

Figure 8