Signetics

SCB68171

Very Little Serial Interface Chip (VLSIC)

Objective Specification

Microprocessor Products

DESCRIPTION

The Signetics Very Little Serial Interface Chip (VLSIC) is a bipolar interface device which connects one or more VMSbus controllers to the VMSbus itself. It provides bus driving and receiving in addition to latching data in both the transmit and receive directions.

SERCLK on the VMSbus has a waveform as shown in figure 1, with four edges per cycle which are designated C1, S1, C2, S2. SYSCLK is used to discriminate (differentiate) the phases of SERCLK. The SYSCLK input should have a nominal 50% duty cycle and a cycle time which is 18% (2/11) that of SERCLK, but SYSCLK and SERCLK need not be synchronous or have any fixed phase relationship. The 16MHz SYSCLK on the VMEbus meets these requirements for a 2.9MHz SERCLK.

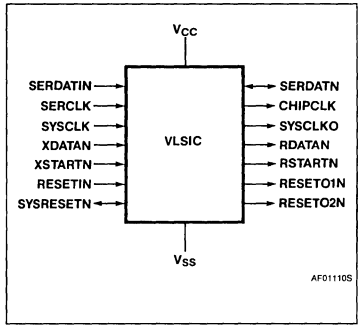
The VLSIC samples both of the XDATAN and XSTARTN inputs on the SERCLK edge designated C1. XDATAN is clocked directly to SERDATN. XSTARTN is clocked into an internal latch. The VLSIC then clocks the low-active OR (positive logic AND) of SERDATN and SERDATIN to RDATAN on the S1 edge. If XDATAN was high and XSTARTN was low at C1, and RSTARTN is high from the previous bit cell, the VLSIC then makes SERDATN low on the C2 edge, thus making a VMSbus start bit. If XDATAN was high at S1, then on the S2 edge it clocks the low active OR of SERDATN and SERDATIN to RSTARTN. If SERDATN was low at S1, it keeps (or makes) RSTARTN high at S2.

CHIPCLK is driven high from the C1 edge of SERCLK, and driven low from the C2 edge. Thus RDATAN and RSTARTN set-up to CHIPCLK edges by approximately the low time of SERCLK. The VMSbus controller(s) must meet the specified set-up and hold times to C1 for data on XDATAN and XSTARTN.

FEATURES

- **70mA open collector drive for SERDATN**
- **Low capacitive loading**
- **Discriminates SERCLK into single-phase chip clock output**
- **Separates data and start bits for both receive and transmit**
- **Provides single bus load for multiple VMSbus controllers**
- **Simplifies controller design and allows use of slower technology**
- **VMEbus receiver for SYSCLK**
- **VMEbus driver/receiver for SYSRESETN**
- **16-pin DIP**

FUNCTIONAL DIAGRAM



JAM FEATURE

A VMSbus controller is required to "jam" the bus by sending a string of "ones" (low) on SERDATN when a start bit is sensed while the controller is sending or tracking a frame. The first one bit should directly follow the misplaced start bit. Since the minimum S2-to-C1 time of SERCLK (25ns) is less than the sum of the maximum S2-to-RSTART-low time plus the minimum set-up of XDATAN to C1, a controller cannot do this using XDATAN in the normal fashion.

The following feature is provided to solve this problem. The condition XDATAN low, XSTARTN low, and CHIPCLK high directly sets the flipflop controlling SERDATN, and makes SERDATN low. (Note that a VMSbus controller would never assert both XDATAN and XSTARTN low in normal operation.) The assertion of both XDATAN and XSTARTN must occur soon enough to satisfy the SERDATN to S1 set-up requirements of all the modules on the VMSbus.

SYSRESET DRIVING/RECEIVING

The VLSIC is primarily intended for use in the P1 region of a VMEbus card. Space and functionality is at a premium in this area. Accordingly, the VLSIC includes an autonomous function of driving and receiving SYSRESETN on the VMEbus. A low on the RESETIN input makes the VLSIC drive the SYSRESETN pin low. SYSRESETN is also received and driven onto two open-collector outputs RESETO1N and RESETO2N. RESETO1N has a high drive capability and is suitable for connection to the RESETN pin of a 680x0 processor, while RESETO2N has lower drive and capacitance and can be connected to the processor's HALTN pin. This function has no connection to the rest of the VLSIC, and could thus be used for some other purpose.

VMSBUS CONTROLLER DESIGN

Controllers using VLSIC should signal as follows on XDATAN and XSTARTN.

1. Controllers should present the next bit on XDATAN and XSTARTN in response to the lowgoing edge of CHIPCLK. For a 2.9MHz SERCLK, they have at least 90nsec to do so, and approximately 120nsec from RDATAN valid.
2. Controllers may release XDATAN, XSTARTN to high in response to the highgoing edge of CHIPCLK. Since these are typically open-collector outputs of the controllers, there may be a timing advantage to do so.
3. A controller should present XDATAN and XSTARTN low in a "jam" situation, in a combinatorial fashion from RSTARTN. Thereafter the controller can release XSTARTN from the lowgoing edge of CHIPCLK, and may either signal 511 or 512 one bits in the usual fashion (1 and 2 above), or may just keep XDATAN low.
4. If two VMSbus controllers connected to the same VLSIC become "locally desynchronized", it is possible that one will present XDATAN low and the other XSTARTN low for the same bit cell. If this occurs, XDATAN predominates and SERDATN is driven low for a "one" bit. Thus the subsequent (transient) combination of XDATAN and XSTARTN low and CHIPCLK high actually has no effect. The controller presenting XSTARTN thereafter receives RDATAN low, and continues to try to send the start bit.

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PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
SERCLK		I	**Direct connect to VMSbus clock:** Clocks SERDATN to RDATAN, RSTARTN. Clocks XDATAN, XSTARTN to SERDATN. Used to generate single-phase CHIPCLK.
SYSCLK		I	**Direct connect to VMEbus clock or other signal meeting the specified frequency relationship to SERCLK:** Used to discriminate the phases of SERCLK.
SYSCLKO		O	**Repeater of SYSCLK for onboard use.**
SERDATN		I/O	**Direct connect to VMSbus data in bipolar open-collector links:** Provides data output function for other types of links (e.g. optical). Requires pull-up resistor in either case.
SERDATIN		I	**Tied to high logic level in bipolar open-collector links:** Provides data input function for other types of links (e.g. optical).
CHIPCLK		O	**Single phase clock for VMSbus controllers.**
RDATAN		O	**Conveys one/zero bits to VMSbus controller(s).**
RSTARTN		O	**Conveys start bits to VMSbus controller(s).**
XDATAN		I	**Input from VMSbus controller(s):** In normal operation, a low on this line indicates a "one" bit should be sent. Simultaneous assertion of XDATAN and XSTARTN low, while CHIPCLK is high, drives SERDATN low directly in a "jam" condition.
XSTARTN		I	**Input from VMSbus controller(s):** In normal operation, a low on this line indicates a "start" bit should be sent. Simultaneous assertion of XDATAN and XSTARTN low, while CHIPCLK is high, drives SERDATN low directly in a "jam" condition.
RESETIN		I	**Input from onboard logic:** Low state forces SYSRESETN low.
SYSRESETN		I/O	**Direct connect to VMEbus system reset:** Open-collector output from RESETIN, received to drive RESETO1N and RESETO2N. Does not affect other VLSIC logic.
RESETO1N		O	**High-drive open-collector output from SYSRESETN.**
RESETO2N		O	**Low-drive open-collector output from SYSRESETN.**
V_{CC}			**+5 Volts**
V_{SS}			**Ground**

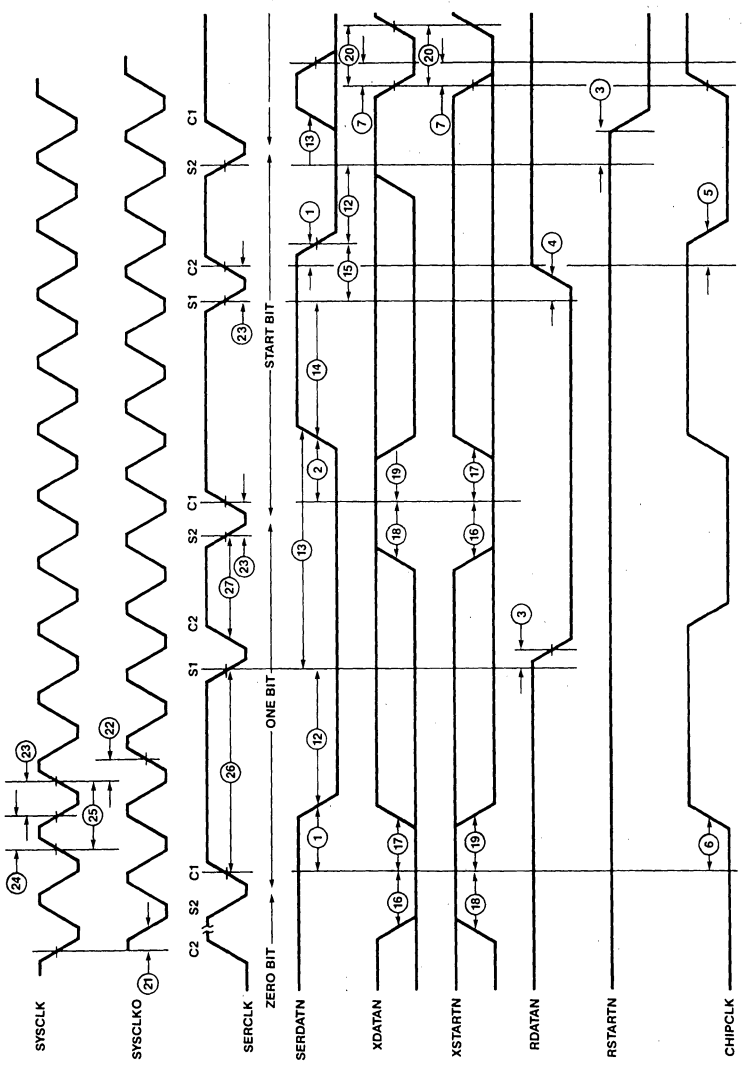

Figure 1. Waveform

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Supply voltage	−0.5 to +7.0	V
Input voltage	−0.5 to +5.5	V
Operating temperature range[2]	0 to +70	°C
Storage temperature	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C, R_L = 90, C_L = 15pF[3,4]

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Max	UNIT
I_{IL}	Low level input current	V_{IN} = 0.4V		−0.4	mA
I_{IH}	High level input current	V_{IN} = 2.7V		20	µA
V_{IL}	Low level input voltage			0.8	V
V_{IH}	High level input voltage				
	SERDATN, SERDATIN, SYSRESETN, RESETIN		1.65		V
	SYSCLK, SERCLK, XDATAN, XSTARTN		2.0		V
$V_{TH+} - V_{TH-}$	Hysteresis				V
	SERDATN, SERDATIN, SYSRESETN, RESETIN		0.15		
V_{OL}	Low level output voltage				
	CHIPCLK, RDATAN, RSTARTN, RESETO2N	I_{OL} = 8mA		0.5	V
	SYSCLKO	I_{OL} = 24mA		0.5	V
	SERDATN, RESETO1N, SYSRESETN	I_{OL} = 70mA		0.5	V
V_{OH}	High level output voltage				
	CHIPCLK, RDATAN, RSTARTN	I_{OH} = −0.4mA	2.7		V
	SYSCLKO	I_{OH} = −1mA	2.7		V
	SYSCLKO	I_{OH} = −2.6mA	2.4		V
I_{OH}	Output leakage current				
	SERDATN, RESETO1N, SYSRESETN	V_{OH} = 2.7V		60	µA
	SERDATN, RESETO1N, SYSRESETN	V_{OH} = 5.5V		250	µA
	RESETO2N	V_{OH} = 5.5V		100	µA
C_I	Input capacitance				
	SERCLK, SYSCLK			8	pF
C_{IO}	I/O capacitance				
	SERDATN			15	pF

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other conditions other than those indicated in the Electrical Characteristics section of this data sheet is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. Parameters are valid over specified temperature range.
4. All voltage measurements are referenced to ground (V_{SS}). All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
5. Output loading 15pF for miminum timing, 300pF for maximum timing.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C, R_L = 90, C_L = 15pF[3,4] (except as noted)

NO.	CHARACTERISTIC	TENTATIVE LIMITS		UNIT
		Min	Max	
1	Prop, C1 or C2 to SERDATN low[5]	9	25	ns
2	Prop, C1 to SERDATN high[5]	10	46	ns
3	Prop, S1 (S2) to RDATAN (RSTARTN) low	7	18	ns
4	Prop, S1 (S2) to RDATAN (RSTARTN) high	6	15	ns
5	Prop, C2 to CHIPCLK low	4	12	ns
6	Prop, C1 to CHIPCLK high	3	9	ns
7	Prop, RDATAN low and RSTARTN low (with CHIPCLK high) to SERDATN low[5]	12	31	ns
8	RDATAN low to CHIPCLK low	t_{CL-6}	t_{CL}	ns
9	RDATAN high to CHIPCLK low	t_{CL-4}	t_{CL}	ns
10	RSTARTN low to CHIPCLK high	t_{CL-9}	t_{CL}	ns
11	RSTARTN high to CHIPCLK high	t_{CL-6}	t_{CL}	ns
12	Set-up, SERDATN and/or SERDATIN low to S1 or S2	8		ns
13	Hold, SERDATN and/or SERDATIN low after S1 or S2	6		ns
14	Set-up, SERDATN and SERDATIN high to S1 or S2	2		ns
15	Hold, SERDATN and SERDATIN high after S1 or S2	8		ns
16	Set-up, XDATAN, XSTARTN low to C1	10		ns
17	Hold, XDATAN, XSTARTN low after C1	0		ns
18	Set-up, XDATAN, XSTARTN high to C1	12		ns
19	Hold, XDATAN, XSTARTN high after C1	0		ns
20	Pulse Width, RDATAN and RSTARTN low with CHIPCLK high	12		ns
21	Prop, SYSCLK low to SYSCLKO low	5	12	ns
22	Prop, SYSCLK high to SYSCLKO high	3	7	ns
23	Pulse width, SYSCLK, SERCLK low (t_{CL})	25		ns
24	Pulse width, SYSCLK high	25		ns
25	Cycle time, SYSCLK (t_{SYCY})	62		ns
26	Pulse width, SERCLK high, C1 to S1			
	(t_{SYCY} = 62.5)	163.5		ns
	(general case)	$3t_{SYCY}-24$		ns
27	Pulse width, SERCLK high, C2 to S2			
	(t_{SYCY} = 62.5)	70	101	ns
	(general case)	70	$2t_{SYCY}-24$	ns