Summary:

A commercial off-the-shelf (COTS) synchronous buck regulator is re-implemented as a Class D audio power amplifier.

# Introduction

Several modular power supply boards came into my possession, destined for the scrap bin. Although the destructive nature of testing that had been applied to these units left most of them irreparable, several boards could be made operational with a reasonable amount of effort. These modular power supplies contain a flyback converter for AC/DC conversion and safety isolation, followed by a synchronous buck converter used to realize the faster transient response characteristic and ride-through time needed by the end system.

While considering whether something creative could be done with the remnants of these boards it occurred to me the buck converter was implemented with a TI TPS40195 voltage mode synchronous buck converter, which has all of the basic functionality needed for implementing a Class D power amplifier. While considering the capability of the flyback converter and the max input voltage of the TPS40195, it became apparent a small 10W amplified speaker box could be made with modest changes to the modular power supply board coupled to a 6-ohm speaker. The ensuing experiment turned out to be a success, so the design process shared for educational and inspirational purposes.

# TPS40195 Re-purposed as an Audio Power Amplifier

The key elements of a typical half-bridge Class D power amplifier all reside within the TPS40195, including the high-side and low-side gate drive logic, error amplifier and PWM modulator. It also operates at supply voltages high enough to generate useful power output into a 4-ohm to 8-ohm speaker – loud enough for reasonable dining room listening levels.

The scheme is illustrated in Fig. 1 below, assuming +VDD is between 15V and 20V. In the specific application the flyback converter output is regulated to 18V.

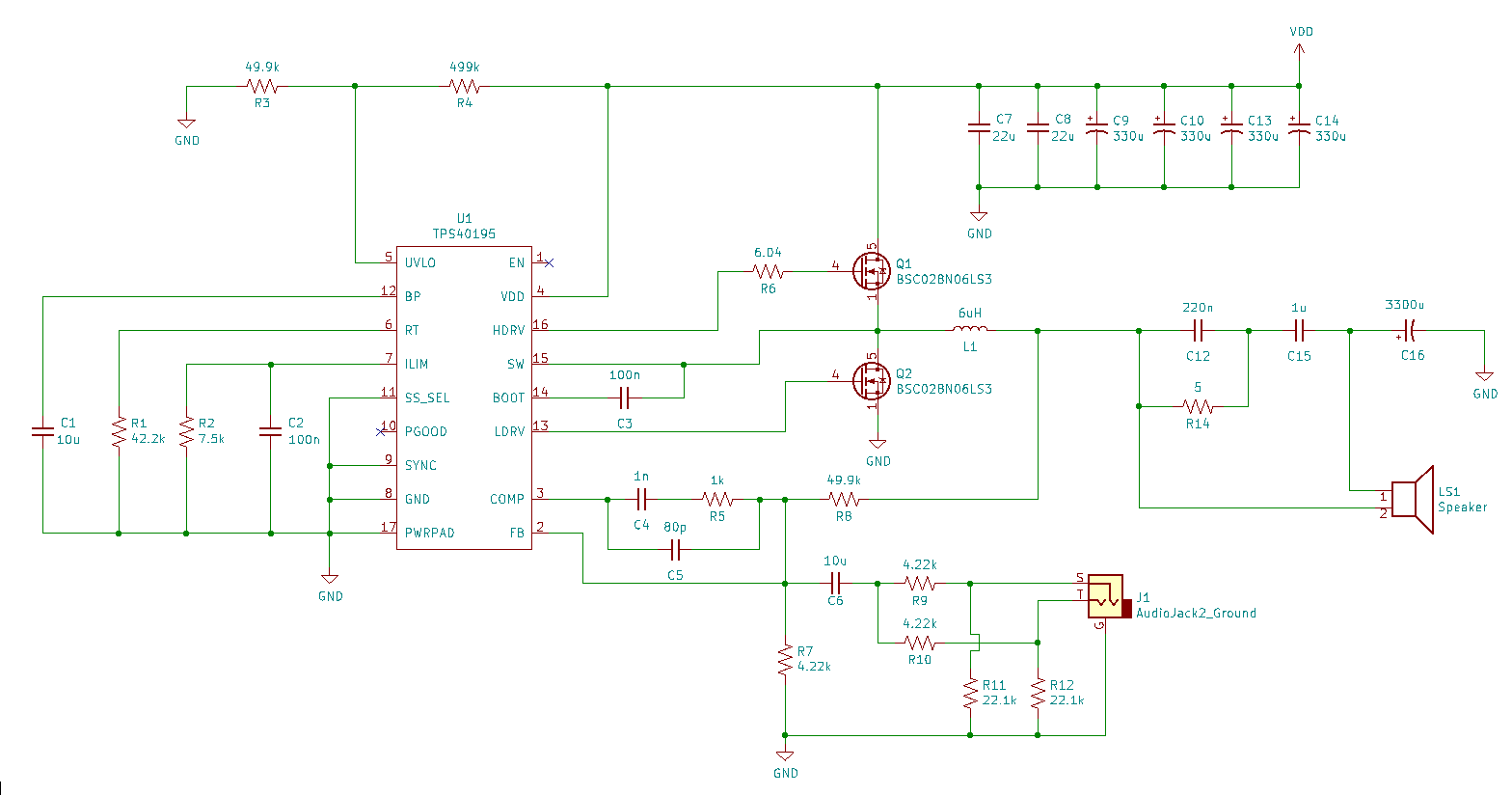


Figure TPS40195 in a Class D power amplifier application

Notable differences between buck converter and audio amplifier applications relate to the approach used for output filtering and feedback loop compensation. The buck converter output filter is typically designed to minimize output voltage ripple to less than 20mVpk-pk while output filter capacitance is often larger than what would be used in an audio amplifier, sized to minimize initial drop during a load step transient while the control loop catches up. By contrast, high frequency voltage ripple in a speaker is of little concern if the associated losses do not substantially heat the voice coil. The audio amplifier step response is only meaningful as a test metric for evaluating the system closed-loop behavior.

Even though a typical buck regulator closed-loop bandwidth may be suitable for serving audio frequency material (as high as 60 kHz), the output filtering capacitance is much higher than what would typically be chosen for an audio amplifier output filter. The reactive currents needed to drive even a modestly-sized capacitive load at audio frequencies will cause significant losses in the system. It is apparent that capacitive loading should be minimal in an audio amplifier, favoring lower reactive currents in trade for a greater amount of switching frequency ripple at the speaker.

Finally, the half-bridge audio amplifier design needs to avoid generating DC current in the speaker. The original buck converter design included a large-valued output capacitor that conveniently forms an 8 Hz high-pass cut-off when used with a 6 ohm speaker, so the low-end response is not substantially attenuated, even into sub-bass frequencies.

Noteworthy in this design implementation the amplifier makes a “pop” in the speaker when the power comes up. The solution to this problem is left to the reader, by any number of viable solutions which may include selection of a purpose-built Class D audio amplifier IC which has been designed to address this problem without external components.

## Main assumptions

An ideal PWM converter is perfectly linear, and feedback would only add unneeded complexity to the design. The dynamic response of the system would be dictated by the response of the low-pass filter formed between the switched inductor, filter capacitor and speaker. Unfortunately, it is not as simple to approach linearity of the ideal PWM and ideal filters as it is to correct for the inherent imperfections by use of feedback.

In practice there are several imperfections in the switching waveforms due to switch timing, on/off transition times, inductor saturation, etc. It was therefore decided to implement feedback, tapped at the low-pass filter output after the inductor.

Maximum open loop gain is desired for reducing distortion as the error term is proportional to the inverse of the loop gain. A high gain control loop will also reduce the amplifier’s output impedance, which is a desirable feature to control the speaker inertia (improved damping factor). The high gain control loop also improves power supply rejection up through most of the audio band.

The first major consideration is deciding whether the feedback control loop should be faster than the output filter (such as a typical approach to controlling a voltage-mode buck converter), or slower. In either case the loop gain crossover frequency should be at least an octave above or below the second-order filter resonance if there is going to be a chance for compensating the loop with substantial phase margin and to obtain a well-behaved closed-loop response.

Conducting a few thought-experiments followed by simulation made it become apparent the having an output filter cut-off lower than the control loop is onerous to compensate and control, especially if one wishes to accommodate a very wide range of speakers. It was particularly difficult to coordinate filter resonance and loop compensation to obtain a maximally flat response void of dips or ripple in the audio band.

On the other hand, by locating the output filter cut-off frequency as high as tolerable it became possible to properly damp it without much hazard of excessive power losses in the damping network by keeping pass-band on the damping resistor mostly above the audio band. Placing the control loop crossover frequency below the output filter resonance proved to be straightforward to compensate using a simple Type II compensator.

## “Back-of-the-envelope” design process

The following steps were used to coordinate output filter and control loop compensation to within the correct octave, while simulation was used to further refine some parameters and verify the selected values work. This design has by no means been optimized, but the steps below are one process that would guide the reader to obtaining decent stability margins and closed-loop frequency response up through 20 kHz. This translates to something that works well enough on the test bench to refine further by test and measurement.

**Step 1: Choose the output filter cut-off frequency**

In this case, it is decided that 20 dB attenuation of the switching frequency fundamental is acceptable. On a 2-pole LRC filter, this requires a cut-off roughly 2 octaves below the switching frequency (12 dB/octave slope). Hence, 550 kHz/4 = 137.5 kHz.

**Step 2: Select output filter inductor value**

The output inductor will play into the amplifier’s bandwidth and slew rate. The bandwidth as set by L/R time constant between the speaker and inductor tends to dominate in the R parallel C realization of an RLC filter when R becomes much smaller than the LC resonator’s characteristic impedance. For example, if we wish to support a speaker cabinet load down to 1 ohm, then the inductor should satisfy,

L = R/[2\*pi\*20kHz] = 7.95μH

A 6μH inductor was used in the buck converter for the output filter, so this value is selected as “close enough”, saving the author time not having to change it.

**Step 3: Choose the output filter capacitor value**

From (1) and (2), we simply need to satisfy,

137.5 kHz = 1/(2\*pi\*sqrt(L\*C)),

Or,

C = 1/(6μH\*(2\*pi\*137.5 kHz)^2) = 223nF, which has a close standard value of 220nF

Note the actual 3 dB cut-off moves around based upon speaker impedance, but the nominal LC resonance computation puts it in the right neighborhood.

Step 4: Select damping resistor

Choosing a damping resistor equal to the LC characteristic impedance will be sufficient when the speaker impedance is large near 130 kHz, or not connected, so

R = sqrt(L/C) = sqrt(6u/220n) = 5.2 ohms (in this case parallel 10 ohm were conveniently at-hand)

**Step 5: Choose DC blocking capacitor for filter damping resistor**

The output filter was designed so that the loop could maintain stability when no speaker is connected, or if high impedance device such as headphone was used. The damping resistor will form a zero with the DC blocking capacitor, which should be about an octave below the crossover frequency.

Fz = 68.75 kHz/2 = 34.38 kHz

Cblock = 1/[2\*pi\*5\*34.38 kHz] = 925.86 uF (nearest value is 1uf)

**Step 6: Choose the control loop crossover frequency**

The two “book ends” of the design are now settled. One would want to keep the crossover frequency an octave below the filter resonance frequency, yet more than an octave above 20 kHz to keep the open loop gain as high as possible.

Min: 2 x 20 kHz = 40 kHz

Max: 137 kHz / 2 = 68.5kHz

Design for the middle of Min and Max, or roughly 54 kHz.

**Step 7: Choose compensation network**

Because the LRC filter resonance was chosen to be an octave above the intended crossover frequency, it is likely only a Type II compensation network will be needed. The series feedback resistor on the board was 50k, and there was no reason to change this, so all other components were selected based upon this. The input supply voltage is 18V and the PWM comparator ramp voltage is 1V peak-peak, so the modulator gain is 18.

g = 18 Modulator gain

Rin = 50k Series resistor feeding error amplifier inverting terminal

fc = 54 kHz Desired control loop crossover frequency

Cf = g/[2\*pi\*Rin\*54kHz] = 1.06 nF Error amplifier feedback capacitor setting dominant pole

Rz = 1/[2\*pi\*Cf\*fc] = 3k, as a starting point, but it was possible to get a flatter closed-loop response by reducing this value.

Cp may be tweaked for additional high frequency filtering if needed

A near available value of 1nF was selected for Cf, and the remainder of the components were tweaked by simulation to obtain acceptable phase margin and closed-loop response behavior.