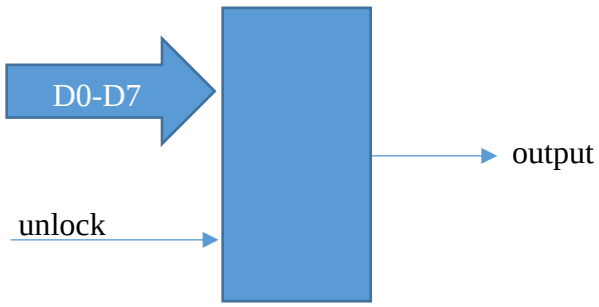
LAB 1: INTRODUCTION TO LOGIC GATES, COMBINATIONAL CIRCUIT DESIGN

1. Introduction to the Logisim-evolution simulation software and installation of Logisim (link: https://github.com/logisim-evolution/logisim-evolution/releases).
2. Read the Logisim user guide in the help section to understand how to use the basic features of Logisim, focusing on the beginner's tutorial and Subcircuits
3. Get familiar with the basic logic gates AND, OR, NOT, XOR, and XNOR. Design the above gates using a 2-input NAND gate.
4. Using Logisim, design the basic logic gates AND, OR, NOT, and XOR with a 2-input NOR gate.
5. Using the TTL 7400 IC, create a 4-input XOR gate.
6. Using 2-input NAND gates, design a logic circuit with 4 input bits X3 (MSB), X2, X1, X0 (LSB) and one output Y. The output Y = 1 if the input value is 0000, 1000, 0101, 1101, 0111, 1111, 0011, or 1011; for all other cases, Y = 0.
7. Use basic logic gates to design a logic circuit that simulates the function of an 8-bit binary lock and an unlock button. The lock will open (output = 1) when the unlock button is pressed and the binary input value matches the last two digits of your student ID.



8. Parity is a method used to detect whether the received data is correct compared to the sent data. There are two types of parity: even parity and odd parity (reference link). Use basic logic gates to design a circuit that allows for the generation and checking of parity for 7 bits of input data, with the parity type based on the last digit of your student ID.