ECE341 - Homework 2

Ton-Minh-Ky Tran

January 31, 2026

1 Investigate different types of flip-flops

2 4-bit asynchronous counter to 15 using D flip-flops

Because this counter's maximum value is 4 bit, we use 4 D flip-flops for each Q. One can observe that if Q_i flips, then Q_{i+1} flips as well as we increment. Since the Q_0 bit always toggles per clock cycle, we hook $\overline{Q_0}$ to D_0. Then for each other flip-flop, we do the same and also hook the previous flip-flop's Q value to the clock input. That way, the flip-flops create a rippling effect and behave similarly to a binary number incrementing. We also connect the Q's to a oscilloscope and see that the period of the waveform of each Q is twice as large as that of the previous Q (highlighting the usage of flip-flops to reduce frequency). An implementation is shown in `24125102_2.circ`.

3 Truncated asynchronous counter to 12 using JK flip-flops

In principle, this is similar to how JK flip-flops counter works shown in the diagram in problem 2. However, we also need to implement the logic such that when the counter hits 13, all flip-flops' clear bit must be enabled, effectively clamping the counter maximum value to 12. Observe that the binary representation of 13 is `1101`, thus we need to check whether Q_0, Q_2, and Q_3 are set (we need not check for Q_1, since the counter will reach `1101` before `1111`). A 3-input AND gate thus suffices. An implementation is shown in `24125102_3.circ`.

4 Synchronous counter using D flip-flops

We first create a transition table to determine the D input for each flip-flop.

Present state			Next state			Input		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	D_2	D_1	D_0
0	0	0	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

Using this transition table, we are able to make Karnaugh maps for each D.

$\mathbf{D_2}$:

$Q_2Q_1 \backslash Q_0$	0	1
00	0	X
01	0	1
11	X	0
10	X	X

$\mathbf{D_1}$:

$Q_2Q_1 \backslash Q_0$	0	1
00	1	X
01	1	1
11	X	0
10	X	X

$\mathbf{D_0}$:

$Q_2Q_1 \backslash Q_0$	0	1
00	0	X
01	1	1
11	X	0
10	X	X

We thus obtain the following:

$$D_2 = \overline{Q_2}Q_0, \quad D_1 = \overline{Q_2}, \quad D_0 = \overline{Q_2}Q_1.$$

Now that we know the required input for each flip-flop, implementing the final circuit is trivial. An implementataion is shown in `24125102_4.circ`.

5 Up down synchronous counter using JK flip-flops

We first consider the case when $C = 1$, making it an up counter. Instead of creating a truth table based on the next value's truth value, we instead create one based on whether the next value is different from the current value; i.e. a toggle. The transition table is thus as follows:

Present state			Next state			Input		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	JK_2	JK_1	JK_0
0	0	0	0	1	0	0	1	0
0	1	0	0	1	1	0	0	1
0	1	1	1	1	1	1	0	0
1	1	1	0	0	0	1	1	1

Using this transition table, we are able to make Karnaugh maps for each JK.

$\mathbf{JK_2}$:

$Q_2Q_1 \backslash Q_0$	0	1
00	0	X
01	0	1
11	X	1
10	X	X

$\mathbf{JK_1}$:

$Q_2Q_1 \backslash Q_0$	0	1
00	1	X
01	0	0
11	X	1
10	X	X

$\mathbf{JK_0}$:

$Q_2Q_1 \backslash Q_0$	0	1
00	0	X
01	1	0
11	X	1
10	X	X

Thus for $C = 1$, we obtain the following:

$$JK_2 = Q_0, \quad JK_1 = Q_2 \odot Q_1, \quad JK_0 = Q_1(Q_2 + \overline{Q_0}).$$

We do the same for $C = 0$. The transition table is thus as follows:

Present state			Next state			Input		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	JK_2	JK_1	JK_0
0	0	0	1	1	1	1	1	1
1	1	1	0	1	1	1	0	0
0	1	1	0	1	0	0	0	1
0	1	0	0	0	0	0	1	0

Using this transition table, we are able to make Karnaugh maps for each JK.

$\mathbf{JK_2}$:

$Q_2Q_1 \backslash Q_0$	0	1
00	1	X
01	0	0
11	X	1
10	X	X

$\mathbf{JK_1}$:

$Q_2Q_1 \backslash Q_0$	0	1
00	1	X
01	1	0
11	X	0
10	X	X

$\mathbf{JK_0}$:

$Q_2Q_1 \backslash Q_0$	0	1
00	1	X
01	0	1
11	X	0
10	X	X

Thus for $C = 0$, we obtain the following:

$$JK_2 = Q_2 \odot Q_1, \quad JK_1 = \overline{Q_0}, \quad JK_0 = \overline{Q_2}(\overline{Q_1} + Q_0).$$

In order to connect the two circuits for each C, we hook each JK and the control bit to an AND gate, totalling to six AND gates. Then we connect the respective Q's for each circuit to an OR gate and connect it to the suitable JK flip-flop. An implementation is shown in `24125102_5.circ`.

6 Digital clock using counter

The implementation includes three counters for the hour, minute, and second counts, with a maximum values set as 23, 59, and 59, respectively. After a brief reading on the counter's input and output description, implementation is trivial. To append the time setting functionality, we utilize the sliders for each value and wire each of them to the counters. An implementation is shown in `24125102_6.circ`.