National Institute for Research Request for Proposal

Advanced study demonstrating application of Field Programmable Gate Array toolchains

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Summary:

Recently, Field Programmable Gate Array (FPGA) development and usage has grown in popularity within aerospace and defense, data center, cybersecurity, automotive, and high-performance computing industries. Some sources project the global FPGA market size will be $11,420 million USD in 2027 with a compound annual growth rate (CAGR) of 10.4%. This increase has been heightened with AMD's recent acquisition of Xilinx, a leading FPGA company, which can result in a tighter integration between FPGAs and CPUs.

The aim of this advanced study is to design and implement a fast Sudoku solver for a FPGA. This would serve as an interesting challenge and valuable proof of concept showing how FPGA tools can be implemented.

Introduction:

FPGAs are integrated circuits having a programmable hardware fabric. Unlike application-specific integrated circuits (ASICs) or graphics processing units (GPUs), the circuitry inside an FPGA chip is not static. The circuitry is dynamically emulated and can be reprogrammed as required. This capability makes FPGAs an alternative to ASICs, which require a long development time as well as a significant investment to design and fabricate.

While FPGAs can be limited in clock speeds compared to General Purpose Processors (GPPs), they offer a much deeper level of parallelism. This means that they can be used to solve problems faster than desktop computers.

This study will hopefully act as a guide for tech companies who will be able to use and improve some of the processes that will be presented and implemented through this study.

I have created multiple sudoku solving systems using other software languages and technologies as side projects in the past. I do it as a good coding challenge to help teach myself a new language. I decided upon this project to push my education, further my skills, and develop my portfolio.

Methodology:

Solving a sudoku puzzle can be treated as a constraint satisfaction problem, an exact-cover problem, graph-coloring problem, or binary-satisfaction problem. Each of these labels have known strategies for finding a solution and can be used in a sudoku solver. Each of these methodologies have different benefits, resource requirements,

complexity, and efficiencies that need to be understood in order to create the fastest algorithm. This will be the focus of my research during the first phase.

To be able to create an advanced algorithm will require an FPGA board with a lot of resources. To ensure this study is completed efficiently and within a 10-week time period, Xilinx cloud solutions will need to be used along with Xilinx Vivado and Vitis IDEs to accelerate the development timeline. Verilog hardware description language will be used to create the system.

Materials:

This study will require the usage of Electrical Engineering labs located in Kate Gleason College of Engineering. In the first phase, I will reach out to RIT professors for their subject matter expertise.

Schedule of Work:

Week 1: Research Phase

> During this week, I will study different Sudoku solving methods including single candidates, missing numbers, naked subsets, hidden subsets, x-wing, forcing chain, swordfish, and 3D Medusa analysis. I will also research known Verilog algorithms.

Week 2-4: Systems Design Phase

> This will include all purchasing and planning. I will start writing code halfway through week 3 and create test plans for when hardware arrives.

Week 5-9: Build, Test, & Debug Phase

> This will take the most amount of time to fully develop the solving algorithms and implement them.

Week 10: Wrap-up & Report Phase

> This will include writing a research monograph and paper to present my work.

Budget:

This is a preliminary budget. Costs may change during the study and an updated bill of materials will be maintained throughout the study.

Item	Qty	Unit Cost	Total Cost	Vendor	Website	Notes
Genesys 2 Kintex-7 FPGA Development Board	1	$999.00	$999.00	Digilent	digilent.com	
Vivado Design Suite for On-Premise Dev for AWS EC2 F1 Instances	1	$3,495.00	$3,495.00	Xilinx	Xilinx.com	
Dell - Precision 7000 17.3" Laptop	1	$3,529.99	$3,529.99	BestBuy	Bestbuy.com	Intel Core i7 - 32 GB Memory - NVIDIA RTX A3000 - 512 GB SSD - Gray

Budget:	$12,000
Item total:	$8,023.99
Research wages:	$3,976.01
Remaining:	$0.00

Biographical Background:

I will be achieving my Bachelor of Science in Electrical Engineering in May 2022. Through my courses and co-op experience, I have been thoroughly trained in FPGA development and computer architecture. Dr. Dorin Patru, a previous professor, has agreed to be my advisor and subject matter expert. He has many publications such as "Reconfigurable Framework for High-Bandwidth Stream-Oriented Data Processing" which is directly applicable to this study. He brings a lot of knowledge and experience and is offering technical guidance.

Conclusion:

To push Moore's Law, we need to keep building upon the latest technologies. However, the latest technologies can be expensive and as a college researcher, I lack the funds to execute my vision. With the money from the National Institute for Research, I will be able to use high-end FPGA tools that are standard in the industry. This will allow me to complete this study in the allotted ten weeks.