OmniVision™

datasheet

PRODUCT SPECIFICATION

1/2.7" color CMOS 1080p (1920x1080) HD image sensor
with OmniPixel3-HS™ technology

OV2735 (rev 1C)

color CMOS 1080p (1920 x1080) HD image sensor with OmniPixel3-HS™ technology

datasheet (CSP)
PRODUCT SPECIFICATION

version 2.01
august 2018

To learn more about OmniVision Technologies, visit www.ovt.com.

applications

- security
- automobile data recorder

ordering information

- **OV02735-H66A-1C** (color, lead-free)
  66-pin CSP
- **OV02735-H66H-1C** (color, lead-free)
  66-pin CSP

features

- programmable controls: gain, exposure, frame rate, image size, horizontal mirror, vertical flip, cropping, and windowing
- automatic image control functions: black level calibration (BLC)
- defective pixel correction (DPC)
- supports binning function
- digital video port (DVP) parallel output interface
- I2C control interface for register programming
- support for two lane MIPI interface (up to 420 Mbps)
- support for image sizes: 1080p @ 30 fps, 720p @ 60 fps, and VGA @ 60 fps
- support for black sun cancellation
- on-chip phase lock loop (PLL)
- support for low power mode

key specifications (typical)

- **active array size:** 1920 x 1080
- **power supply:**
  core: 1.7V~1.9V (1.8V nominal)
  analog: 2.6V~3.0V (2.8V nominal)
  I/O: 1.7V~3.0V (1.8V nominal)
- **power requirements:**
  active: 176 mW
- **temperature range:**
  operating: -30°C to +85°C junction temperature (see **table 6-2**)
  stable image: 0°C to +60°C junction temperature (see **table 6-2**)
- **output interfaces:** two-lane MIPI / DVP parallel
- **output formats:** RAW10
- **lens size:** 1/2.7"
- **lens chief ray angle:** 12° linear (see **figure 8-3**)
- **input clock frequency:** 6 ~ 27 MHz
- **scan mode:** progressive
- **maximum image transfer rate:**
  1080p: 30 fps
  720p: 60 fps
- **sensitivity:** 23 Ke^-/Lux-sec
- **shutter:** rolling
- **max S/N ratio:** 38.6 dB
- **dynamic range:** 72 dB @ 8x gain
- **maximum exposure interval:** 1328 t_{row}
- **pixel size:** 3 µm x 3 µm
- **image area:** 5808 µm x 3288 µm
- **package dimensions:** 6951 µm x 4760 µm

table of contents

list of figures

list of tables

1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV2735 image sensor. The package information is shown in **section 7**.

table 1-1 signal descriptions (sheet 1 of 3)

pin number	signal name	pin type	description
A1	NC	–	no connect
A2	DGND	ground	digital ground
A3	**FSIN**	I/O	frame sync
A4	**VSYNC**	I/O	video output vertical signal
A5	**HSYNC**	I/O	video output horizontal signal
A7	**D2**	output	DVP data output 2
A10	**D5/MDP1**	output	DVP data output 5/MIPI data positive output 1
A11	NC	–	no connect
B1	DOVDD	power	I/O power
B2	DVDD18	power	digital circuit power
B3	**D3**	output	DVP data output 3
B4	DOVDD	power	I/O power
B5	**D0**	output	DVP data output 0
B6	**D1**	output	DVP data output 1
B8	**D6/MDP0**	output	DVP data output 6/MIPI data positive output 0
B9	**D8/MCP**	output	DVP data output 8/MIPI clock positive output
B10	**D4/MDN1**	output	DVP data output 4/MIPI data negative output 1
B11	**MCLK**	input	input clock
C1	AVDD	power	analog power
C2	AVDD	power	analog power
C3	DGND	ground	digital ground
C4	DGND	ground	digital ground
C5	DVDD18	power	digital circuit power
C6	DOVDD	power	I/O power
C7	**PCLK**	I/O	DVP mode pixel clock
C8	**D7/MDN0**	output	DVP data output 7/MIPI data negative output 0

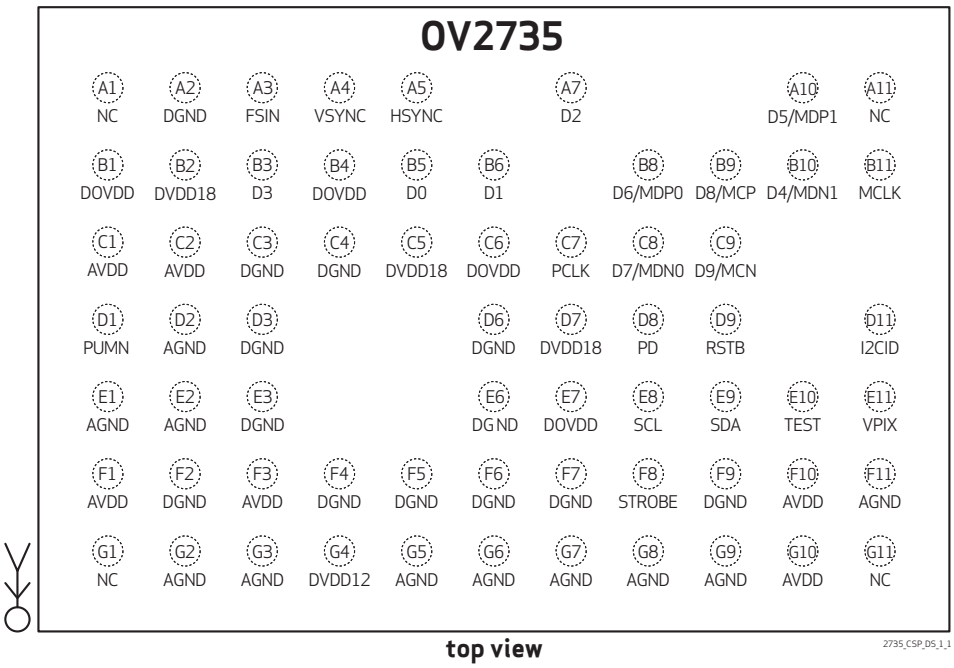
table 1-1 signal descriptions (sheet 2 of 3)

pin number	signal name	pin type	description
C9	D9/MCN	output	DVP data output 9/MIPI clock negative output
D1	PUMN	reference	internal analog reference
D2	AGND	ground	analog ground
D3	DGND	ground	digital ground
D6	DGND	ground	digital ground
D7	DVDD18	power	digital circuit power
D8	PD	input	power down control 0: normal 1: power down
D9	RSTB	input	reset signal (low level reset)
D11	I2CID	input	device address selection 0: I2CID address = 0x78 1: I2CID address = 0x7A
E1	AGND	ground	analog ground
E2	AGND	ground	analog ground
E3	DGND	ground	digital ground
E6	DGND	ground	digital ground
E7	DOVDD	power	I/O power
E8	SCL	input	slave I2C clock bus
E9	SDA	I/O	slave tri-state (I2C data bus)
E10	TEST	reference	test pin
E11	VPIX	reference	internal analog reference
F1	AVDD	power	analog power
F2	DGND	ground	digital ground
F3	AVDD	power	analog power
F4	DGND	ground	digital ground
F5	DGND	ground	digital ground
F6	DGND	ground	digital ground
F7	DGND	ground	digital ground
F8	STROBE	output	strobe control
F9	DGND	ground	digital ground

table 1-1 signal descriptions (sheet 3 of 3)

pin number	signal name	pin type	description
F10	AVDD	power	analog power
F11	AGND	ground	analog ground
G1	NC	–	no connect
G2	AGND	ground	analog ground
G3	AGND	ground	analog ground
G4	DVDD12	power	digital circuit power
G5	AGND	ground	analog ground
G6	AGND	ground	analog ground
G7	AGND	ground	analog ground
G8	AGND	ground	analog ground
G9	AGND	ground	analog ground
G10	AVDD	power	analog power
G11	NC	–	no connect

figure 1-1 pin diagram



top view

table 1-2 pin states under various conditions

pin number	signal name	RSTB = 0	RSTB = 1, PD = 1 hardware power down	RSTB = 1, PD = 0 stream on/active
A3	FSIN	input	input (configurable)	input (configurable)
A4	VSYNC	input	input (configurable)	input (configurable)
A5	HSYNC	output	output (configurable)	output (configurable)
A7	D2	output	output (configurable)	output (configurable)
A10	D5/MDP1	output	output (configurable)	output (configurable)
B3	D3	output	output (configurable)	output (configurable)
B5	D0	output	output (configurable)	output (configurable)
B6	D1	output	output (configurable)	output (configurable)
B8	D6/MDP0	output	output (configurable)	output (configurable)
B9	D8/MCP	output	output (configurable)	output (configurable)
B10	D4/MDN1	output	output (configurable)	output (configurable)
B11	MCLK	input	input	input
C7	PCLK	output	output (configurable)	output (configurable)
C8	D7/MDN0	output	output (configurable)	output (configurable)
C9	D9/MCN	output	output (configurable)	output (configurable)
D8	PD	input	input	input
D9	RSTB	input	input	input
D11	I2CID	input	input	input
E8	SCL	input	input	input
E9	SDA	open-drain	open-drain	open-drain
E10	TEST	input	input	input
F8	STROBE	low	low	low

table 1-3 pad symbol and equivalent circuit (sheet 1 of 2)

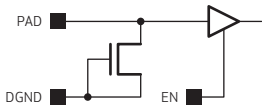
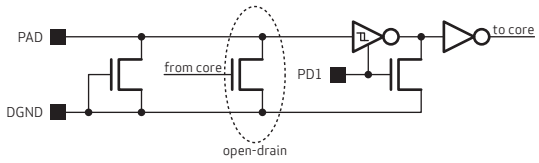
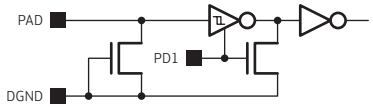
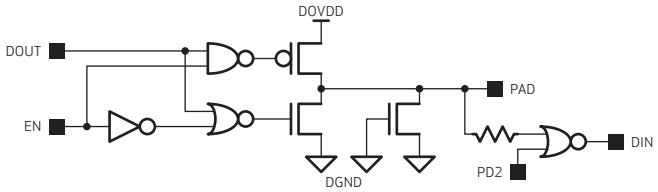
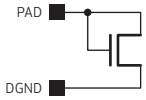
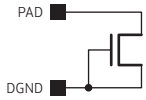
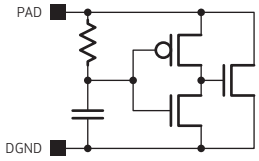
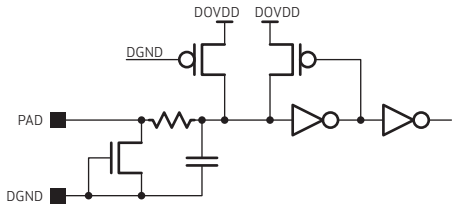
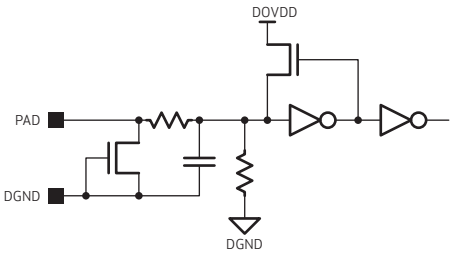
symbol	equivalent circuit
MCLK	
SDA	
SCL	
STROBE, FSIN, D9/MCN, D8/MCP, D7/MDN0, D6/MDP0, D5/MDP1, D4/MDN1, D3, D2, D1, D0	
PUMN	
AGND, DGND, VPIX, TEST	
AVDD, DVDD18, DVDD12, DOVDD	
RSTB	

table 1-3 pad symbol and equivalent circuit (sheet 2 of 2)

symbol	equivalent circuit
I2CID, PD	

2 system level description

2.1 overview

The OV2735 color image sensor is a full function, high definition (HD), 1080p/720p sensor designed to provide support for IP cameras, HD analog type cameras, or 1080p at 30 fps video capture devices. This low voltage CMOS device provides full-framed (at 30 fps), sub-sampled, or windowed images in your choice of format, via either the MIPI or DVP ports, controlled by the standard I2C interface.

With a complete 1080p full size image array capable of 30 frames per second (fps), combined with full user control of the image quality and sync mode for dual camera configuration, the OV2735 is a standard for 16:9 imaging solutions.

All required image processing functions are programmable through the I2C interface. In addition, OmniVision image sensors utilize proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

2.2 architecture

The OV2735 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OV2735 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, pre-charging and sampling the rows of the array sequentially. In the time between pre-charging and sampling a row, the charge in the pixels decreases with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between pre-charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs up to 10-bit data for each pixel in the array.

figure 2-1 OV2735 block diagram

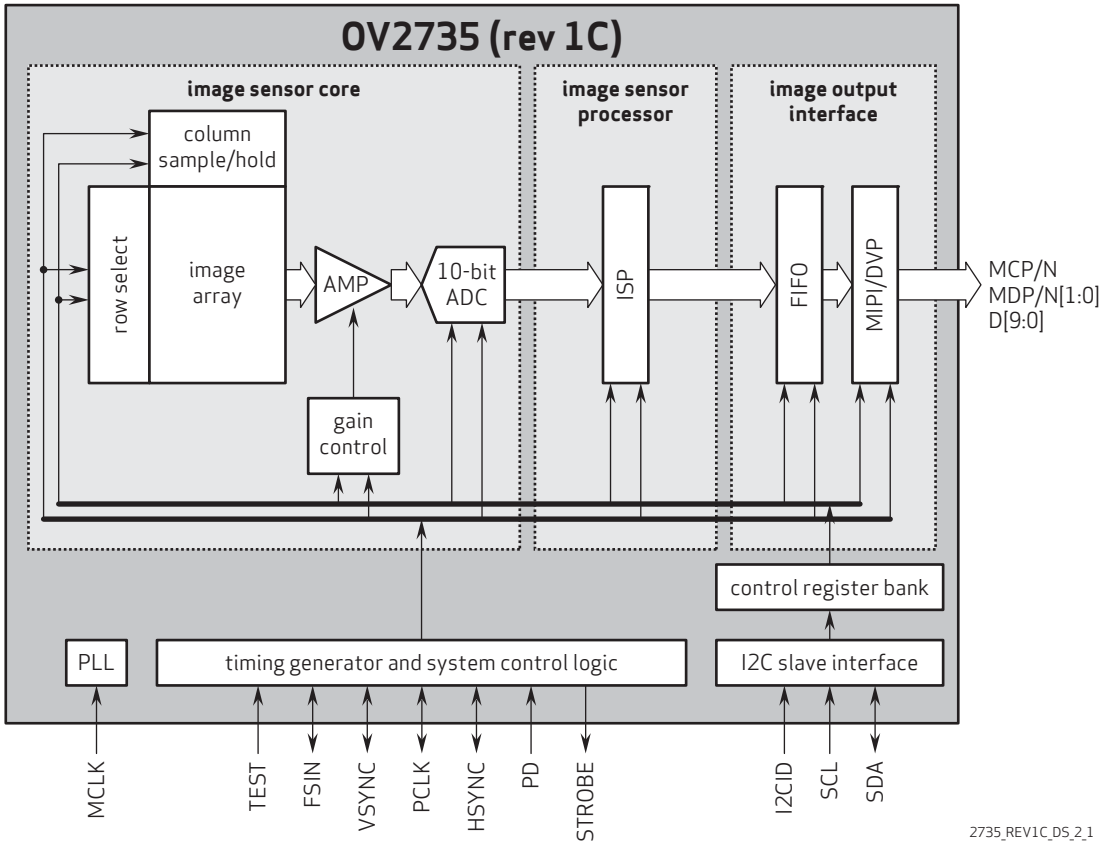
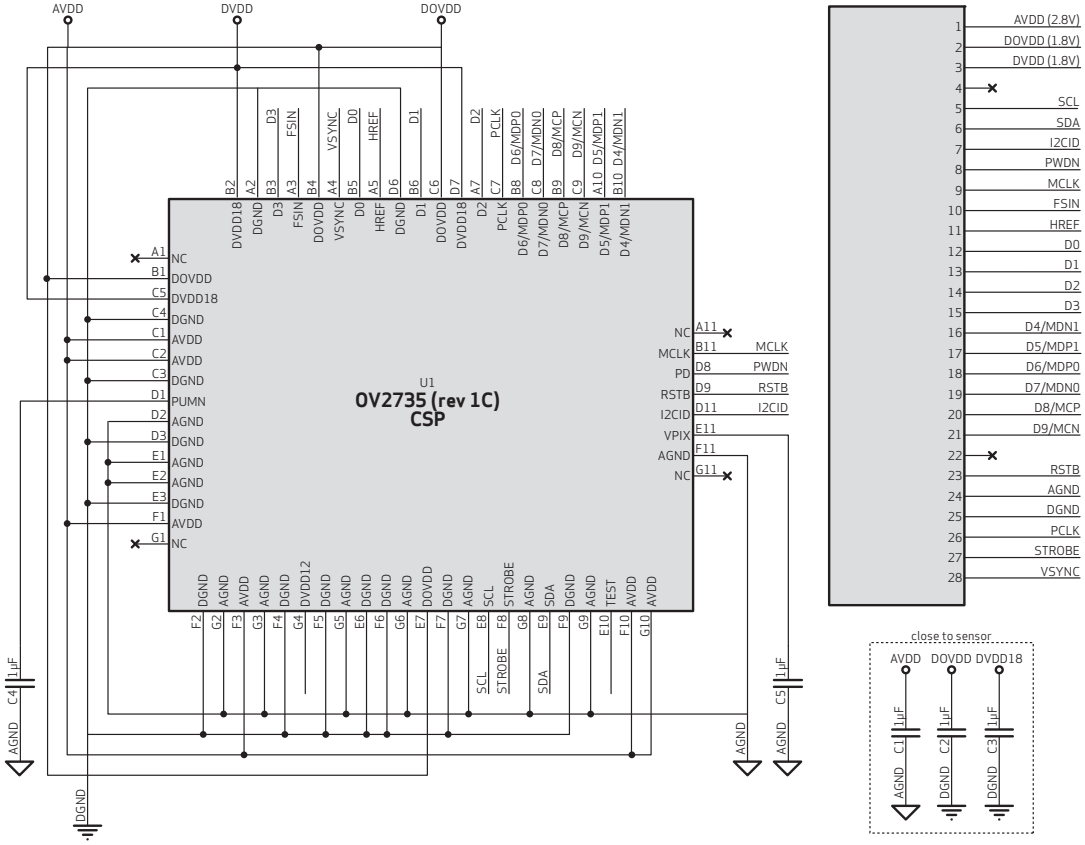


figure 2-2 OV2735 DVP reference schematic



note 1 AVDD is from 2.6V -3.0V, DOVDD range is 1.7V-3.0V, DVDD is 1.8V

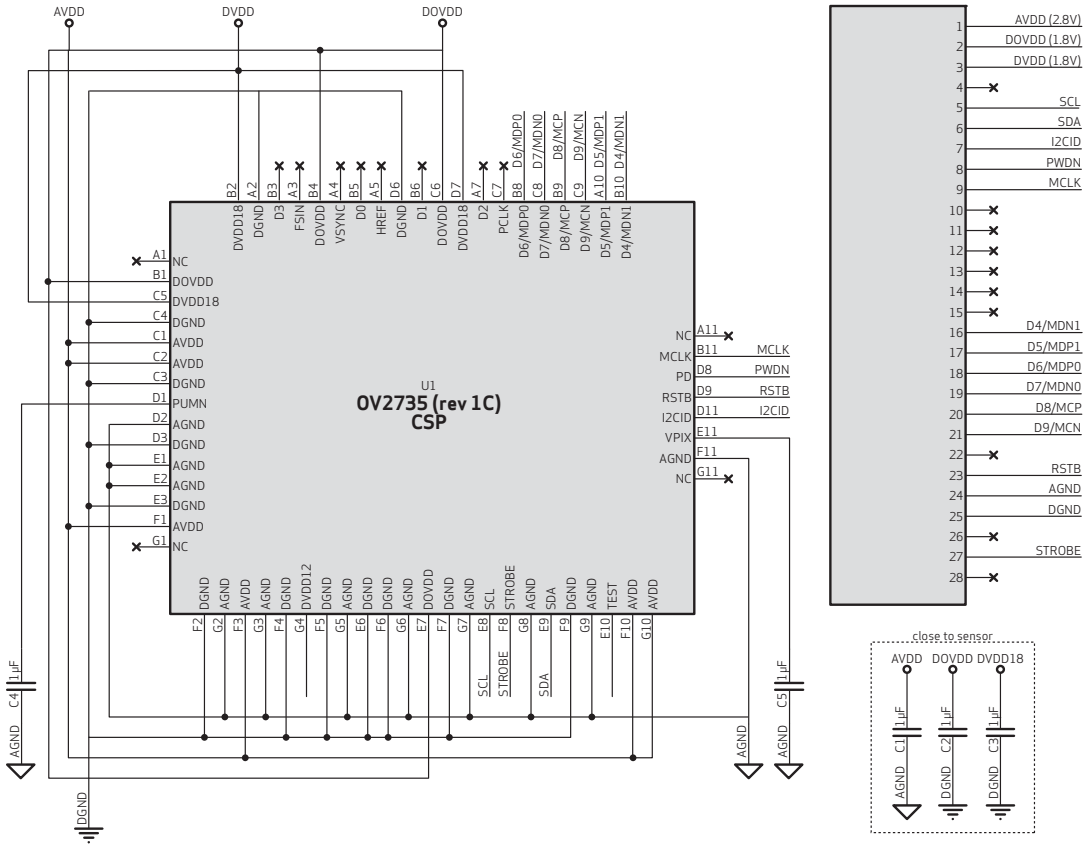
note 2 this design is in 10-bit parallel mode, in which D4/MDN1, D5/MDP1, D6/MDP0, D7/MDN0, D8/MCP, D9/MCN are multiplexed pins in parallel mode respectively for D4, D5, D6 , D7, D8, D9 to use, when in 8-bit mode, D[9:2], D0, D1 can be suspended, I2CID is controlled by I2C address pins, when I2CID is low, address is 0x78, when I2CID is high, address is 0x7A

note 3 chip power supply filter capacitor (minimum must be affixed to 0402 1µF) should be placed near power supply pins (AVDD, DOVDD, DVDD), sensor's AGND and DGND should be inside the module separately and connected to a single point outside the module, AVDD and AGND should not be adjacent to clock, power supply should have no finer than 0.15 mm design, ground floor dragnet

note 4 FPC using anti-jamming design

2735_REV1C_CSP_DS_2_2

figure 2-3 OV2735 MIPI reference schematic



note 1 AVDD is from 2.6V ~3.0V, DOVDD range is 1.7V~3.0V, DVDD is 1.8V

note 2 this design is in 10-bit parallel mode, in which D4/MDN1, D5/MDP1, D6/MDP0, D7/MDN0, D8/MCP, D9/MCN are multiplexed pins in parallel mode respectively for D4, D5, D6 , D7, D8, D9 to use, when in 8-bit mode, D[9:2], D0, D1 can be suspended, I2CID is controlled by I2C address pins, when I2CID is low, address is 0x78, when I2CID is high, address is 0x7A

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note 4 FPC using anti-jamming design

2735_REV1C_CSP_DS_2_3

2.3 format and frame

The OV2735 supports RAW RGB output with one/two MIPI interface.

table 2-1 format and frame rate

format	resolution	frame rate	methodology	10-bit output MIPI data rate	DVP clock frequency
1080p	1920 x 1080	30 fps	full resolution qualified pixel (8+1920+8) x (8+1080+8)	420 Mbps/lane	84 MHz
qHD	960 x 540	60 fps	2x2 binning qualified pixel (4+960+4) x (4+540+4)	200 Mbps/lane	40 MHz
720p	1280 x 720	60 fps	crop from full resolution	375 Mbps/lane	75 MHz
VGA	640 x 480	60 fps	crop and binning	200 Mbps/lane	40 MHz

2.4 output interface

Both MIPI and parallel data output interface are integrated inside OV2735.

2.4.1 parallel interface

The parallel interface defines an interface between a peripheral device and a host processor. The traditional parallel interface is embedded in the OV2735. As a result, the OV2735 can be compatible with most existing mainstream platforms.

2.4.2 MIPI interface

The MIPI interface is a serial interface which can support high-speed, high-precision, and large-array transmission. So, it plays an important role in security surveillance, video conferencing, traffic sign recognition, etc. With it, the OV2735 can provide higher definition images to the applications.

The MIPI inside the OV2735 provides one single uni-directional clock lane and two data lane solutions for communication links between components inside the application device. This MIPI can support some kinds of operating mode, such as burst mode, switch mode, ULPs mode, and line sync mode. Users can select appropriate mode according to their requirements.

2.4.3 D-PHY function

The D-PHY converts parallel data from CSI_TOP to serial data that are compatible with MIPI protocol. Detailed time sequences are shown in **figure 2-4** and **figure 2-5**.

figure 2-4 switching the clock lane between clock transmission and low-power mode

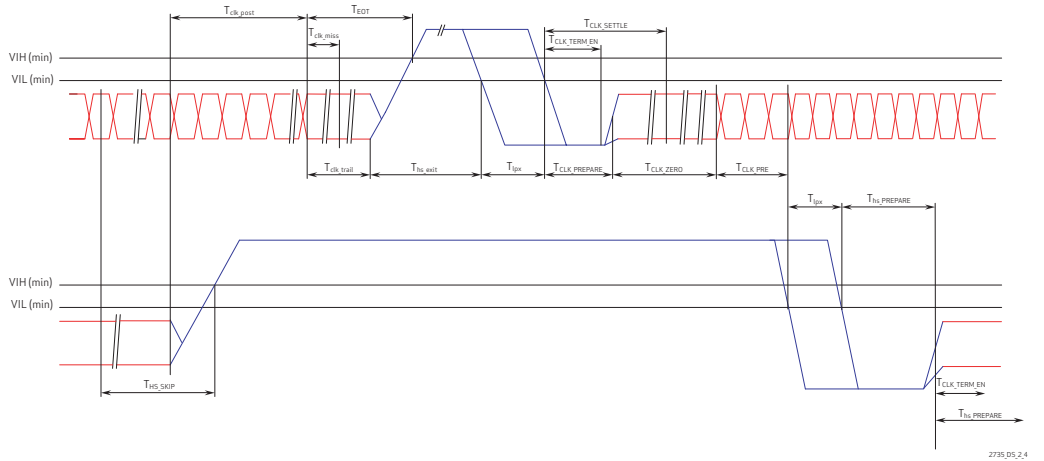
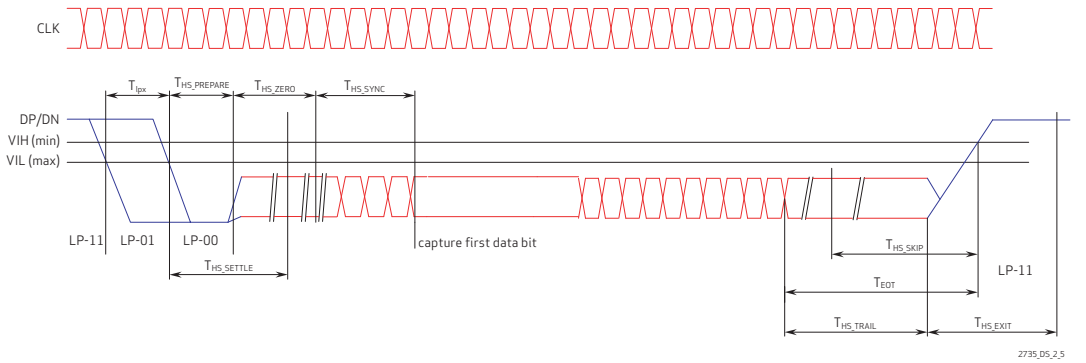


figure 2-5 high-speed data transmission bursts



2.4.4 data lane parameters

table 2-2 data lane parameters

parameter	target	min	max
$T_{HS-PREPARE}$	time that transmitter drives data lane LP-00 line state immediately before HS-0 Line state starts HS transmission	40 ns + 4*UI	85 ns+6*UI
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that transmitter drives HS-0 state prior to transmitting sync sequence	145 ns + 10*UI	
$T_{HS-SETTLE}$	time interval which HS receive shall ignore any data lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$	85 ns + 6*UI	145 ns+10*UI
$T_{HS-SKIP}$	time interval which HS-RX should ignore any transitions on data lane, following a HS burst end point of interval is defined as beginning of LP-11 state following HS burst	40	55 ns+4*UI
$T_{HS-TRAIL}$	time that transmitter drives HS-0 state after last payload clock bit of a HS transmission burst	max (n*8*UI, 60ns + n*4*UI)	
T_{LPX}	transmitted length of any low-power state period	50 ns	
T_{WAKEUP}	time that a transmitter drives a Mark-1 state prior to a stop state in order to initiate an exit from ULPS	1 ms	

2.4.5 clock lane parameters

table 2-3 clock lane parameters

parameter	target	min	max
$T_{CLK-MISS}$	timeout for receive to detect absence of clock transmission and disable clock lane HS-RX	60 ns	
$T_{CLK-POST}$	time that transmitter continues to send HS clock after last associated data lane has transitioned to LP mode interval is define as period from end of $T_{HS-TRAIL}$ to the beginning $T_{CLK-TRAIL}$	60 ns + 52*UI	
$T_{CLK-PRE}$	time that HS clock will be driven by transmitter prior to any associated data lane beginning transition from LP to HS mode	8*UI	
$T_{CLK-PREPARE}$	time that transmitter drives clock lane LP-00 line state immediately before HS-0 line state starts HS transmission	38 ns	95 ns
$T_{CLK-SETTLE}$	time interval which HS receive will ignore any clock lane HS transmissions, starting from beginning of $T_{CLK-PREPARE}$	95 ns	300 ns
$T_{CLK-TRAIL}$	time that the transmitter driver the HS-0 state after the last payload clock bit of a HS transmission burst.	60 ns	
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that transmitter drives HS-0 state prior to starting clock	300 ns	
T_{EOT}	transmitted time interval from start of $T_{CLK-TRAIL}$ or $T_{HS-TRAIL}$, to start of LP-11 state following a HS burst		105 ns + n*12*UI

2.5 power up/off sequence

2.5.1 power up sequence

figure 2-6 power up sequence diagram

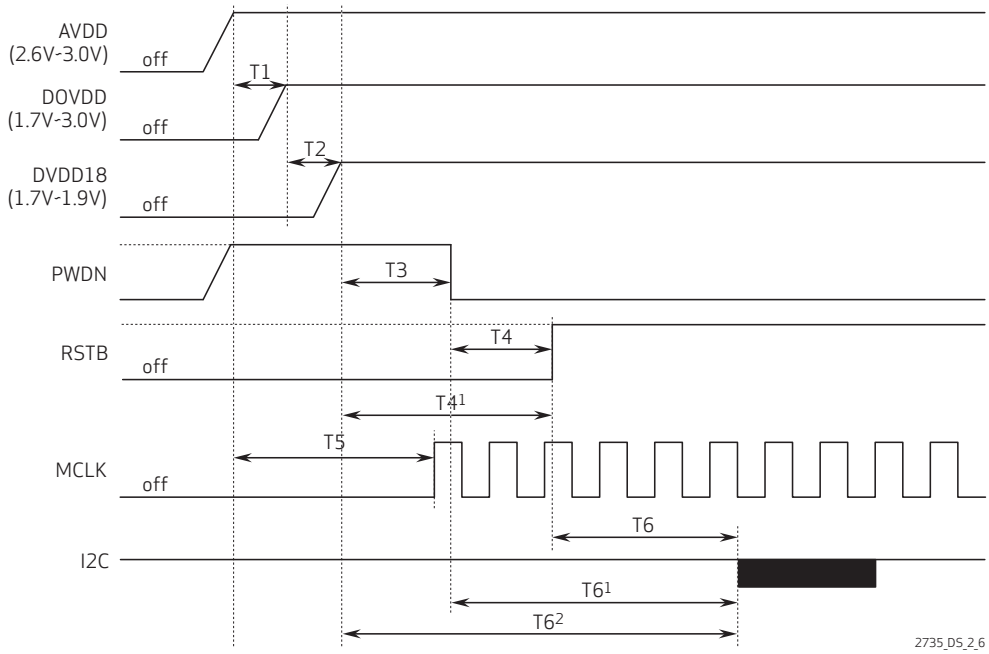


table 2-4 power up sequence parameters

symbol	description	min	unit
T1	delay from AVDD to DOVDD	0	ms
T2	delay from DOVDD to DVDD18	0	ms
T3	delay from DVDD18 stable to sensor power up stable	5	ms
T4	delay from PWDN pulling low to RSTB pulling high	4	ms
T4[1]	delay from DVDD18 power up stable to RSTB pulling high when PWDN signal remains low during power up	9	ms
T5	delay from AVDD stable to MCLK on	0	ms
T6	delay from RSTB pulling high to first I2C command	5	ms
T6[1]	delay from PWDN pulling low to first I2C command when RSTB signal remains high during power up	9	ms
T6[2]	delay from DVDD18 power up stable to first I2C command when PWDN signal remains low and RSTB signal remains high during power up	14	ms

2.5.2 power off sequence

figure 2-7 power off sequence diagram

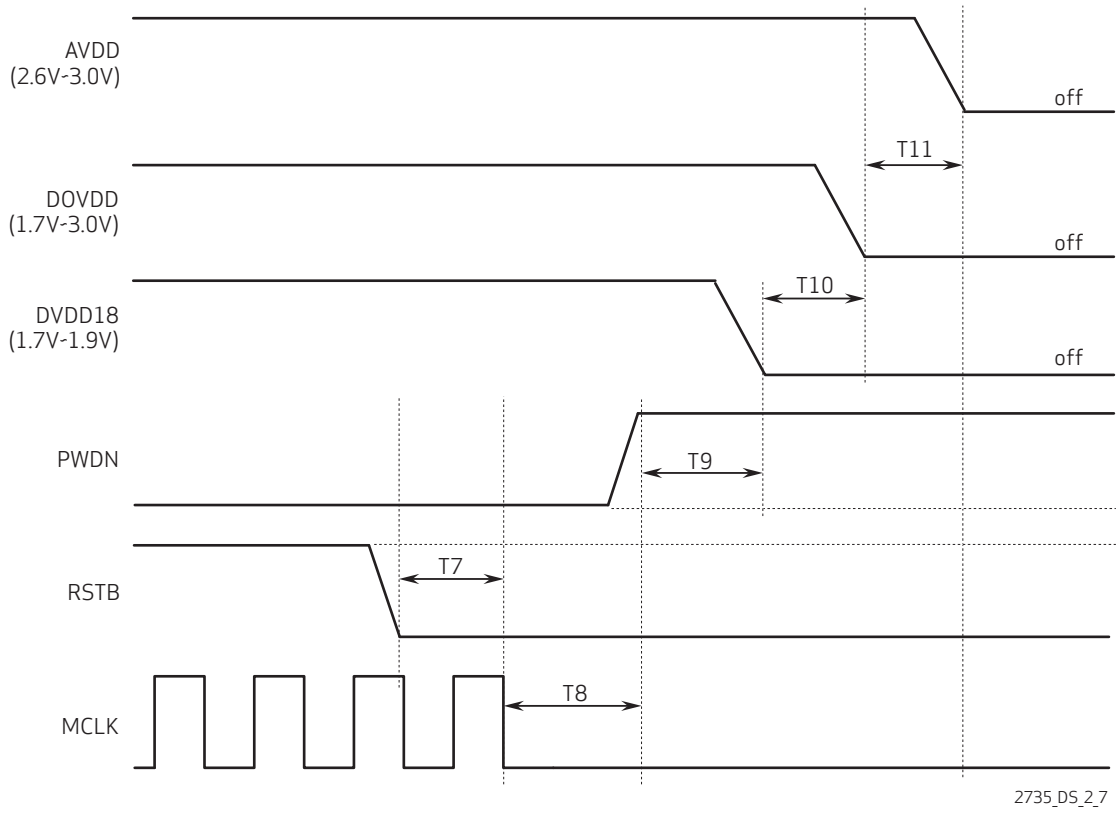


table 2-5 power up sequence parameters

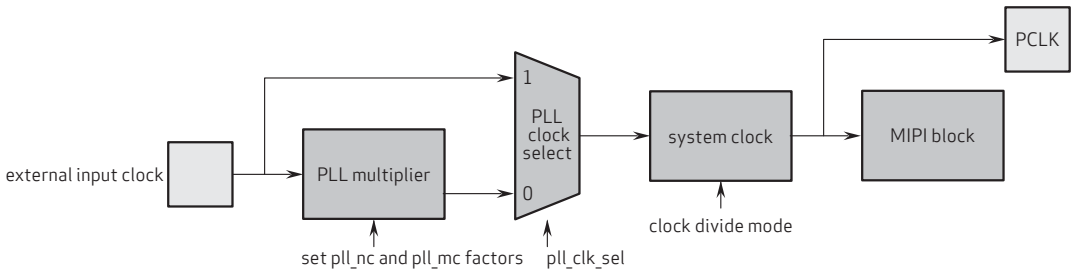
symbol	description	min	unit
T7	delay from RSTB pull low stable to MCLK off	0	ms
T8	delay from MCLK off to sensor power down	0	ms
T9	delay from sensor power down to DVDD18 off	0	ms
T10	delay from DVDD18 off to DOVDD off	0	ms
T11	delay from DOVDD off to AVDD off	0	ms

2.6 PLL and clock generator

The OV2735 contains a phase locked loop (PLL) block, which generates all the necessary internal clocks from the external clock input.

The internal function blocks of the PLL are shown in **figure 2-8**.

figure 2-8 clock scheme



$$F_{out} = F_{in} * \frac{pll\_nc[4:0]+3}{pll\_mc[1:0]+1} \div 2^{pll\_outdiv[1:0]}$$

note $F_{in} * \frac{pll\_nc[4:0]+3}{pll\_mc[1:0]+1}$ is in range of 120 MHz to 300 MHz

2735_DS_2.8

2.7 I2C bus

2.7.1 single read and single write

The OV2735 I2C write address and read address can be chosen by I2CID pin. When the pin is set high, the write address is 0x7A and the read address is 0x7B. When the pin is set low, the write address is 0x78 and the read address is 0x79.

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First, the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

figure 2-9 illustrates the OV2735 single read sequence and single write sequence.

figure 2-9 I2C read and write message description, I2CID pin set high

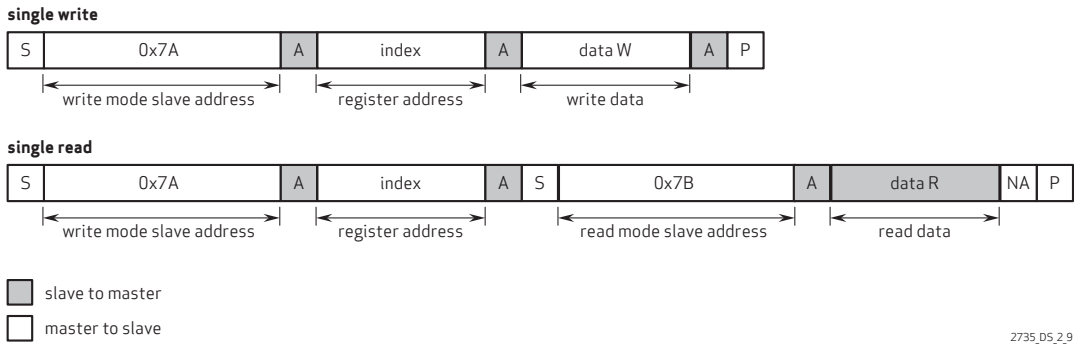
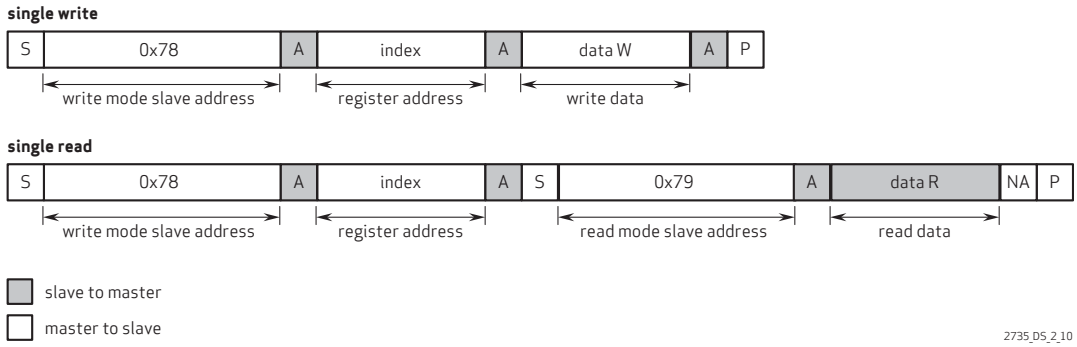


figure 2-10 I2C read and write message description, I2CID pin set low



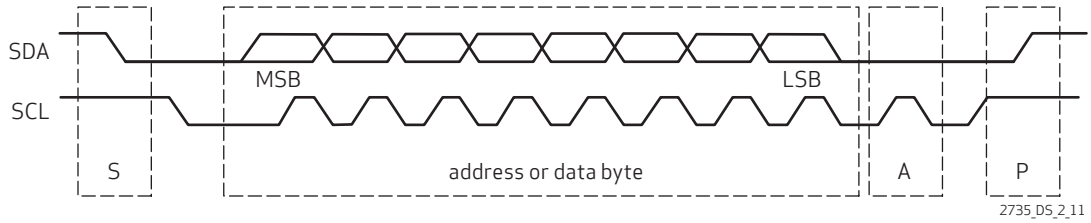
2.7.2 data bit transfer

One data bit is transferred during each clock pulse. The serial clock pulse is provided by the master. The data must be stable during the high period of the serial clock. It can only change when the serial clock is low. Data is transferred 8 bits at a time, followed by an acknowledge bit.

2.7.3 acknowledge bit

The OV2735 will hold the value of the SDA pin to logic '0' during the logic '1' state of the acknowledge clock pulse on SCL.

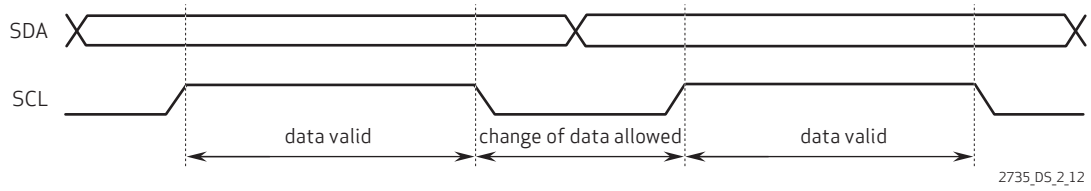
figure 2-11 I2C acknowledge bit diagram



2.7.4 data valid

The master must ensure that data is stable during the logic 1 state of the SCL pin. All transitions on the SDA pin can only occur when the logic level on the SCL pin is '0'.

figure 2-12 I2C data transport diagram



2.7.5 timing parameter

figure 2-13 I2C bus timing parameter diagram

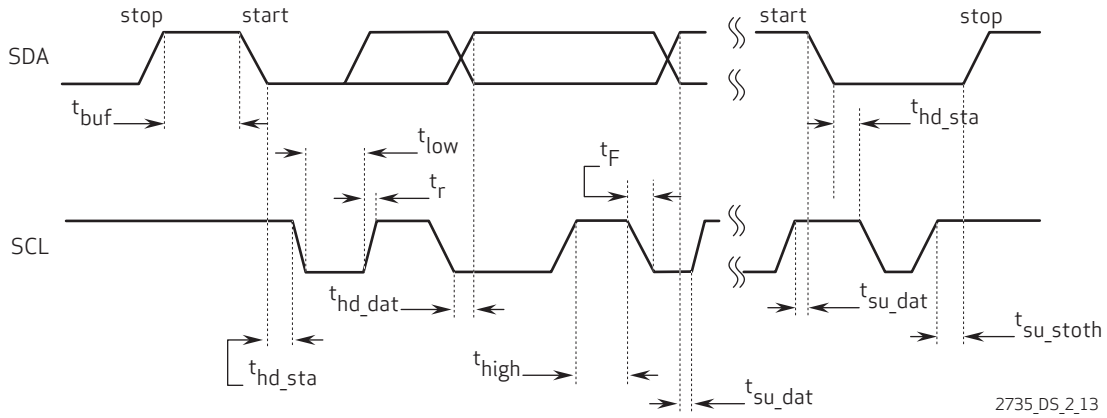


table 2-6 I2C interface timing specifications

symbol	parameter	min	max	unit
f_{scl}	SCL clock frequency	10	400	kHz
t_{buf}	bus free time between a stop and a start	1.3	–	µs
t_{hd_sta}	hold time for a repeated start	0.6	–	µs
t_{low}	LOW period of SCL	1.3	–	µs
t_{high}	HIGH period of SCL	0.6	–	µs
t_{su_sta}	setup time for a repeated start	0.6	–	µs
t_{hd_dat}	data hold time	0	–	µs
t_{su_dat}	data setup time	250	–	ns
t_r	rise time of SCL, SDA	–	300	ns
t_f	fall time of SCL, SDA	–	300	ns
t_{su_sto}	setup time for a stop	0.6	–	µs
C_b	capacitive load of bus line (SCL, SDA)	–	–	pf

3 block level description

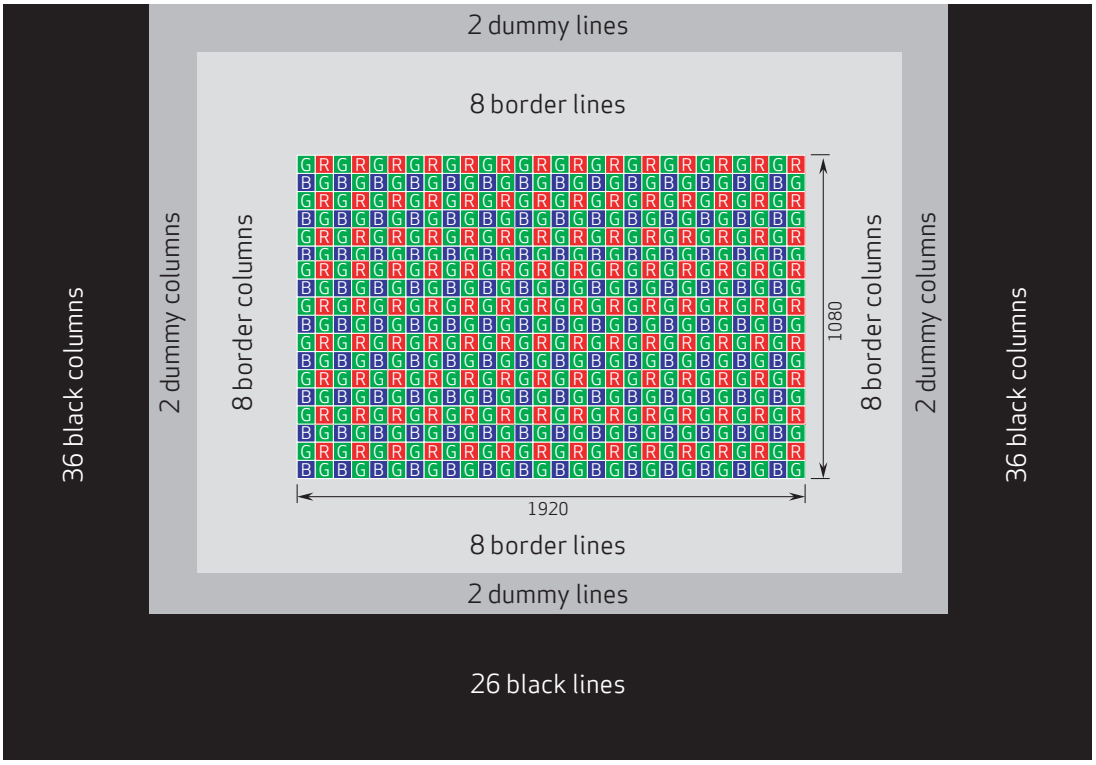
3.1 pixel array structure

The OV2735 sensor has an image array of 2012 columns by 1126 rows (2,265,512 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color GR/BG array is arranged in line-alternating fashion. Of the 2,265,512 pixels, 2,073,600 (1920x1080) are active pixels and can be output.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 3-1 sensor array region color filter layout



note color filter for first pixel at left bottom is blue

2735_DS_3.1

3.2 subsampling

The OV2735 supports a binning mode to provide a lower resolution output while maintaining the field of view. With binning mode ON, the voltage levels of adjacent pixels (of the same color) are averaged before being sent to the ADC. The OV2735 supports 2x2 binning, which is illustrated in **figure 3-2**, where the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged.

figure 3-2 example of 2x2 binning

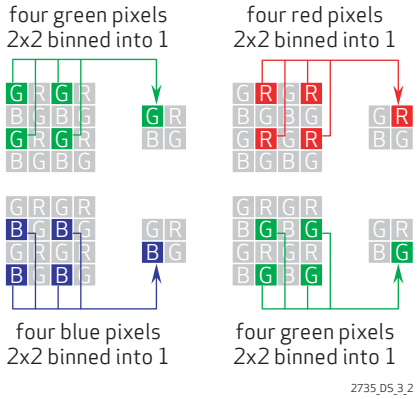


table 3-1 binning-related registers

address	register name	default value	R/W	description
P1:0x31	COMM_CTRL_REG	0x00	RW	Bit[2]: v_binning_en

3.3 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

3.4 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC.

4 image sensor core digital functions

4.1 mirror and flip

The OV2735 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

2735_DS_4_1

table 4-1 mirror and flip registers

address	register name	default value	R/W	description
P1:0x3F	UPDOWN_MIRROR	0x00	RW	Bit[1]: Updown Bit[0]: Mirror

4.2 windowing

The embedded windowing function extracts an image windowing area by defining 4 parameters, including horizontal start, horizontal width, vertical start, and vertical height. By properly setting the parameters, the portions within the sensor array size can be cropped as a visible area. Windowing function will not conflict with the mirror and flip function.

4.3 test pattern

Test pattern and color bar are offered for testing purposes.

4.4 black level calibration

The OV2735 black level calibration function compensates for dark current to ensure constant output black level regardless of change in exposure time, gain, and temperature.

4.5 defect pixel correction

Defect pixels will be detected and be replaced by a value calculated from the neighbor pixel during the defect pixel correction unit.

A defect pixel is a pixel which is black, and is not charged when light hits it, a zero value is read. Such defect pixels will be detected and corrected.

4.6 gain

Digital gain can be controlled by DG_Gr, DG_Gb, DG_R, DG_B. Each digital gain can be configured from a gain of 0 to 2. The format of each digital gain register is "x.yyyyyyy", where "x" refers an integer gain of 0 to 1 and "yyyyyyy" is a fractional gain ranging from 0/128 to 1/128.

Analog gain can be obtained by adjusting the ramp's slope, using pga_gain_ctl register.

5 register tables

The following tables provide descriptions of the device control registers contained in the OV2735. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x7A for write and 0x7B for read (when I2CID=0, 0x78 for write and 0x79 for read).

5.1 clock registers [P0:0x2F - P0:0x30, P0:0x33 - P0:0x35, P0:0x39]

table 5-1 clock registers (sheet 1 of 2)

address	register name	default value	R/W	description
P0:0x2F	PLL_CTRL_BUF	0x10	RW	Bit[7]: pll_clk_sel 0: Disable bypass PLL 1: Enable bypass PLL Bit[6:2]: pll_nc Bit[1:0]: pll_mc PLL output = [PLL input/(pll_mc+1)]*[(pll_nc+3)/(pll_outdiv+1)] Parameters of registers will be enabled in next frame
P0:0x30	CLK_MODE_BUF	0x0F	RW	Bit[7]: pclk_gate_en Bit[6:4]: pclk_ctrl 000: Pclk = pll_clk 001: Pclk = pll_clk/2 010: Pclk = pll_clk/4 011: Pclk = pll_clk/6 100: Pclk = pll_clk/8 101: Pclk = pll_clk/12 Bit[3:2]: clk_pcp_ctrl 00: clk_pcp = pll_clk/2 01: clk_pcp = pll_clk/6 10: clk_pcp = pll_clk/8 11: clk_pcp = eclk Bit[1:0]: clk_ncp_ctrl 00: clk_ncp = pll_clk/2 01: clk_ncp = pll_clk/6 10: clk_ncp = pll_clk/8 11: clk_ncp = eclk Parameters of registers will be enabled in next frame

table 5-1 clock registers (sheet 2 of 2)

address	register name	default value	R/W	description
P0:0x33	CLOCK REGISTER 1	0x01	RW	Bit[7:4]: Not used Bit[3]: dac_clk_gating_en_buf 0: Disable dac_clk gating 1: Enable dac_clk gating Bit[2:1]: dac_clk_mode_buf, 00: dac_clk = pll_clk/2 01: dac_clk = pll_clk/4 10: dac_clk = pll_clk/6 11: dac_clk = pll_clk/8 Bit[0]: cis_clk_mode_buf 0: timer_clk = pclk_pre 1: timer_clk = pclk_pre/2 Parameters of registers will be enabled in next frame.
P0:0x34	BUF_PLL_OUTDIV	0x01	RW	PLL Frequency Divider Control PLL output = [PLL input/(pll_mc+1)] * [(pll_nc+3)/(pll_outdiv+1)] Parameters of registers will be enabled in next frame
P0:0x35	CLOCK REGISTER 2	0x00	RW	Bit[7]: Not used Bit[6:5]: pll_bias_ctl PLL charge pump current control 00: 10 u 01: 20 u (default) 10: 30 u 11: 40 u Bit[4:3]: pll_dctl Choose PLL's PFD delay time to remove dead zone 00: 478p (default) 01: 932p 10: 1.334n 11: 1.736n Bit[2:0]: Not used
P0:0x39	BUF_PCLK_INV	0x01	RW	Pad PCLK Reverse Enable Signal 0: Disable PCLK reverse 1: Enable PCLK reverse Parameters of registers will be enabled in next frame

5.2 soft reset [P0:0x20]

table 5-2 soft reset register

address	register name	default value	R/W	description
P0:0x20	SOFT_RST	0x01	RW	Soft Reset Signal 0: Enable soft reset 1: Disable soft reset Register cannot be self cleared

5.3 power down [P0:0x36 - P0:0x37]

table 5-3 power down registers

address	register name	default value	R/W	description
P0:0x36	PWD_PLL	0x00	RW	Power Down Control of PLL 0: Disable power down of PLL 1: Enable power down of PLL
P0:0x37	PWD_ASP	0x00	RW	Power Down Control of ASP 0: Disable power down of ASP 1: Enable power down of ASP

5.4 parallel port [P0:0x1B, P0:0x1D, P0:0x1F, P0:0x40]

table 5-4 parallel port registers (sheet 1 of 2)

address	register name	default value	R/W	description
P0:0x1B	PARALLEL PORT CTRL 1	0x1F	RW	Bit[7:5]: Not used Bit[4]: evsync_oe_buf Pad evsync output enable signal 0: Enable output 1: Disable output Bit[3]: strobe_oe_buf Pad strobe output enable signal 0: Enable output 1: Disable output Bit[2]: out_end_buf Pad dataout[9:0] output enable signal 0: Enable output 1: Disable output Bit[1]: out_ens_buf Pad VSYNC and HSYNC output enable signal 0: Enable output 1: Disable output Bit[0]: out_enp_buf Pad PCLK output enable signal Parameters of registers will be enabled in next frame 0: Enable output 1: Disable output
P0:0x1D	PARALLEL PORT CTRL 2	0x55	RW	Bit[7:6]: ds_data Driver current select signal of pad dataout[9:0] Bit[5:4]: ds_pclk Driver current select signal of pad PCLK Bit[3:2]: ds_hsync Driver current select signal of pad HSYNC Bit[1:0]: ds_vsync Driver current select signal of pad VSYNC
P0:0x1F	EVSYNC_IE	0x00	RW	Bit[7:1]: Not used Bit[0]: evsync_ie Pad evsync input enable signal 0: Disable input 1: Enable input

table 5-4 parallel port registers (sheet 2 of 2)

address	register name	default value	R/W	description
P0:0x40	PARALLEL PORT CTRL 3	0x00	RW	Bit[7:2]: Not used Bit[1]: ext_sync_mst_en Enable master mode of external sync function 0: OV2735 is slave of external sync 1: OV2735 is master of external sync Bit[0]: ext_sync_en Enable signal of external sync function 0: Disable external sync 1: Enable external sync

5.5 I2C [P0:0x50 - P0:0x51]

table 5-5 I2C registers

address	register name	default value	R/W	description
P0:0x50	I2C_DEV_ADDR_EN	0x00	RW	i2c_dev_addr Enable Signal 0: Disable i2c_dev_addr 1: Enable i2c_dev_addr
P0:0x51	I2C_DEV_ADDR	0x3D	RW	Manual I2C Device Address

5.6 system [P0:0x02 - P0:0x04, P0:0xFD]

table 5-6 system registers

address	register name	default value	R/W	description
P0:0x02	CHIP_ID	0x27	R	chip_id
P0:0x03	CHIP_ID	0x35	R	chip_id
P0:0x04	ECO_VER	0x01	RW	Version of ECO
P0:0xFD	PAGE_FLG	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Page_flg Page number

5.7 resolution, exposure, and analog gain [P1:0x01 - P1:0x38, P1:0x3D, P1:0x3F, P1:0xE8]

For OV2735, the minimum exposure is 4 Tline.

table 5-7 resolution, exposure, and analog gain registers

address	register name	default value	R/W	description
P1:0x01	EXP_RPC_EN	0x00	RW	Enable of Frame Sync Signal 0: Disable 1: Enable
P1:0x03	BUF_EXP_8MSB	0x01	RW	Bit[7:0]: Exposure time in “H” unit[15:8] 1~65535 (0x0001~0xFFFF)
P1:0x04	BUF_EXP_8LSB	0x86	RW	Bit[7:0]: Exposure time in “H” unit[7:0] 1~65535 (0x0001~0xFFFF)
P1:0x23	RPC	–	R	Bit[7:0]: PGA gain control[7:0] (read only) Corresponding to register P1:0x24
P1:0x24	PGA_GAIN_CTL	0x20	RW	Bit[7:0]: PGA gain manual control[7:0]
P1:0x25~ P1:0x30	NOT USED	–	–	Not Used
P1:0x31	RESOLUTION SELECTION	0x00	RW	Resolution Selection 0x00: 1936x1096 0x01: 1288x728 0x02: 648x488 0x04: 968x548 0x08: 968x548 0x10: 2004x1104
P1:0x32~ P1:0x38	NOT USED	–	–	Not Used
P1:0x3D	NOT USED	–	–	Not Used
P1:0x3F	UPDOWN MIRROR	0x00	RW	Bit[7:2]: Not used Bit[1]: Vertical upside down Bit[0]: Horizontal mirror 0x00: Normal (no flip) 0x01: Horizontal flip 0x02: Vertical flip 0x03: Both horizontal and vertical flip
P1:0xE8	RPC_TMP1	–	R	PGA Gain Control Low Byte Takes effect one frame earlier than register of P1:0x23

5.8 digital gain [P1:0x39 - P1:0x43]

table 5-8 digital gain registers[a]

address	register name	default value	R/W	description
P1:0x39	DIG_GAIN_BUF	0x80	RW	Global Digital Gain (1x~2x) 0x80: 1x 0xFF: 2x Accuracy is 1/128
P1:0x40	R_GAIN_BUF	0x80	RW	Digital Gain, Red Channel (1~2x) 0x80: 1x 0xFF: 2x Accuracy is 1/128
P1:0x41	GR_GAIN_BUF	0x80	RW	Digital Gain, Gr Channel (1~2x) 0x80: 1x 0xFF: 2x Accuracy is 1/128
P1:0x42	GB_GAIN_BUF	0x80	RW	Digital Gain, Gb Channel (1~2x) 0x80: 1x 0xFF: 2x Accuracy is 1/128
P1:0x43	B_GAIN_BUF	0x80	RW	Digital Gain, Blue Channel (1~2x) 0x80: 1x 0xFF: 2x Accuracy is 1/128

a. global digital gain and WB gain will also affect sensor black level

5.9 frame length and row length [P1:0x05 - P1:0x0F, P1:0x28 - P1:0x4F, P1:0x8C - P1:0x8D]

table 5-9 frame length and row length registers (sheet 1 of 2)

address	register name	default value	R/W	description
P1:0x05	VBLANK_BUF_8MSB	0x00	RW	Bit[7:0]: Vertical blank in “H” unit[15:8] 0~65535 (0x0000~0xFFFF)
P1:0x06	VBLANK_BUF_8LSB	0x00	RW	Bit[7:0]: Vertical blank in “H” unit[7:0] 0~65535 (0x0000~0xFFFF)
P1:0x08	VPOS_BLANK	0x01	RW	Time Width Between Posedge of VSYNC and Posedge of First HSYNC in “H”unit

table 5-9 frame length and row length registers (sheet 2 of 2)

address	register name	default value	R/W	description
P1:0x09	HBLANK_4MSB	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Horizontal blank in “timer_clk” unit[11:8] 0~4095 (0x000~0xFFF)
P1:0x0A	HBLANK_8LSB	0x00	RW	Bit[7:0]: Horizontal blank in “timer_clk” unit[7:0] 0~4095 (0x000~0xFFF)
P1:0x0D	FRAME_EXP_ SEPERATE_EN	0x00	RW	Bit[7:5]: Not used Bit[4]: Frame_exp_seperate_en When enabled, frame length equal to value of register P1:{0x0E, 0x0F} 0: Disable 1: Enable Bit[3:0]: Not used
P1:0x0E	FRAME_LENGTH_ NUM_8MSB	0x04	RW	Bit[7:0]: Frame length for manual frame length setting[15:8] Used with P1:0x0D[4] enabled
P1:0x0F	FRAME_LENGTH_ NUM_8LSB	0x50	RW	Bit[7:0]: Frame length for manual frame length setting[7:0] Used with P1:0x0D[4] enabled
P1:0x28	ANA_V_DUMMY_ SIZE	0x08	RW	Specify Vertical Row Number Upward and Downward of Active Readout Area, Respectively for 720p and VGA mode
P1:0x29~ P1:0x2F	NOT USED	–	–	Not Used
P1:0x3A	VDELAY_BUF_8MSB	0x00	RW	Bit[7:0]: Vertical blank in “H” unit[15:8]
P1:0x3B	VDELAY_BUF_8LSB	0x00	RW	Bit[7:0]: Vertical blank in “H” unit[7:0]
P1:0x3C~ P1:0x4D	NOT USED	–	–	Not Used
P1:0x4E	FRAME_LENGTH_RE ADONLY_8MSB	–	R	Bit[7:0]: Frame length in “H” unit[15:8]
P1:0x4F	FRAME_LENGTH_RE ADONLY_8LSB	–	R	Bit[7:0]: Frame length in “H” unit[7:0]
P1:0x8C	HS_PERIOD_NUM_ 5MSB	–	R	Bit[7:5]: Not used Bit[4:0]: Row length in “timer_clk” unit[12:8]
P1:0x8D	HS_PERIOD_NUM_ 8LSB	–	R	Bit[7:0]: Row length in “timer_clk” unit[7:0]

5.10 BLC [P1:0x86 - P1:0x89, P1:0xE0 - P1:0xE5, P1:0xF0 - P1:0xFC, P1:0xFE]

table 5-10 BLC registers (sheet 1 of 3)

address	register name	default value	R/W	description
P1:0x86	BLC_GAIN_BLUE	0x80	RW	blc_gain for Blue Channel (0x~2x) Accuracy is 1/128
P1:0x87	BLC_GAIN_RED	0x80	RW	blc_gain for Red Channel (0x~2x) Accuracy is 1/128
P1:0x88	BLC_GAIN_GR	0x80	RW	blc_gain for Gr Channel (0x~2x) Accuracy is 1/128
P1:0x89	BLC_GAIN_GB	0x80	RW	blc_gain for Gb Channel (0x~2x) Accuracy is 1/128
P1:0xE0	BLACK_LEVEL_BR_MSB	–	R	Bit[7]: Not used Bit[6:4]: Black level calibration value, B[10:8] Bit[3]: Not used Bit[2:0]: Black level calibration value, R[10:8]
P1:0xE1	BLACK_LEVEL_GB_8LSB	–	R	Bit[7:0]: Black level calibration value, Gb[7:0]
P1:0xE2	BLACK_LEVEL_B_8LSB	–	R	Bit[7:0]: Black level calibration value, B[7:0]
P1:0xE3	BLACK_LEVEL_R_8LSB	–	R	Bit[7:0]: Black level calibration value, R[7:0]
P1:0xE4	BLACK_LEVEL_GR_8LSB	–	R	Bit[7:0]: Black level calibration value, Gr[7:0]
P1:0xE5	BLACK_LEVEL_G_MSB	–	R	Bit[7]: Not used Bit[6:4]: Black level calibration value, Gb[10:8] Bit[3]: Not used Bit[2:0]: Black level calibration value, Gr[10:8]
P1:0xF0	GB_SUBOFFSET	0x00	RW	Bit[7:0]: Black level offset, Gb channel[7:0] Total register is 9 bits with MSB P1:0xF8[7] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF1	BLUE_SUBOFFSET	0x00	RW	Bit[7:0]: Black level offset, B channel[7:0] Total register is 9 bits with MSB P1:0xF8[6] (-256~255, 0x100~0x0FF) Highest bit is sign bit
P1:0xF2	RED_SUBOFFSET	0x00	RW	Bit[7:0]: Black level offset, R channel[7:0] Total register is 9 bits with MSB P1:0xF8[5] (-256~255,0x100~0x0FF) Highest bit is sign bit

table 5-10 BLC registers (sheet 2 of 3)

address	register name	default value	R/W	description
P1:0xF3	GR_SUBOFFSET	0x00	RW	Bit[7:0]: Black level offset, Gr channel[7:0] Total register is 9 bits with MSB P1:0xF8[4] (-256~255,0x100~0x0FF) Highest bit is sign bit
P1:0xF4	SHIFT_GB	0x00	RW	Black Level Shift, Gb Channel (0~255, 0x00~0xFF)
P1:0xF5	SHIFT_BLUE	0x00	RW	Black Level Shift, B Channel (0~255, 0x00~0xFF)
P1:0xF6	SHIFT_RED	0x00	RW	Black Level Shift, R Channel (0~255, 0x00~0xFF)
P1:0xF7	SHIFT_GR	0x00	RW	Black Level Shift, Gr Channel (0~255, 0x00~0xFF)
P1:0xF8	BLC CTRL 1	0x00	RW	Bit[7]: Black level offset, Gb channel[8] Total register is 9 bits with LSB P1:0xF0 (-256~255,0x100~0x0FF) High 1 bit is sign bit Bit[6]: Black level offset, B channel[8] Total register is 9 bits with LSB P1:0xF1 (-256~255,0x100~0x0FF) High 1 bit is sign bit Bit[5]: Black level offset, R channel[8] Total register is 9 bits with LSB P1:0xF2 (-256~255,0x100~0x0FF) High 1 bit is sign bit Bit[4]: Black level offset, Gr channel[8] Total register is 9 bits with LSB P1:0xF3 (-256~255,0x100~0x0FF) High 1 bit is sign bit Bit[3:2]: bl_position_set2 Black level position control for calibration Bit[1:0]: bl_position_set Black level position control for statistic
P1:0xF9	BLC_BPC_IN_P_8LSB	0x20	RW	Black Level Positive Data for Bad Pixel Replacement, Encoded in Absolute Value
P1:0xFA	BLC_BPC_IN_N_8LSB	0x20	RW	Black Level Negative Data for Bad Pixel Replacement, Encoded in Absolute Value

table 5-10 BLC registers (sheet 3 of 3)

address	register name	default value	R/W	description
P1:0xFB	ABL	0x00	RW	Bit[7]: blc_test_en 0: Low 10 bits output mode 1: High 10 bits output mode Bit[6]: blc_filter_en 0: Dark row median filter disable 1: Dark row median filter enable Bit[5]: blc_gain_en 0: Black level gain expansion disable 1: Black level gain expansion enable Bit[4]: blc_bpc_en 0: Dark row BPC disable 1: Dark row BPC enable Bit[3]: Not used Bit[2:1]: blc_mode 00: 1 frame average mode 01: 4 frames average mode 10: 8 frames average mode 11: 1 frame average mode Bit[0]: blc_en 0: Black level disable 1: Black level enable
P1:0xFC	BLC_BPC_TH_P	0x40	RW	Black Level Positive Threshold for Bad Pixel, Encoded in Absolute Value
P1:0xFE	BLC_BPC_TH_N	0x40	RW	Black Level Negative Threshold for Bad Pixel, Encoded in Absolute Value

5.11 row wise noise [P1:0xC0 - P1:0xC8]

table 5-11 row wise noise registers

address	register name	default value	R/W	description
P1:0xC0	RWN_CTL	0x00	RW	Row-wise Noise (RWN) Reduction Control Bit[7:4]: Not used Bit[3]: rwn_darkrow_en Control RWN function of dark rows to be on/off 0: Off 1: On Bit[2]: rwn_mode 0: Double channel statistics 1: Single channel statistics Bit[1]: rwn_bpc_en Control RWN BPC function to be on/off 0: Off 1: On Bit[0]: rwn_en Control total RWN function to be on/off 0: Off 1: On
P1:0xC1	RWN_BPC_TH_P_1MSB	0x00	RW	Bit[7:1]: Not used Bit[0]: RWN BPC positive threshold, encoded in absolute value[8]
P1:0xC2	RWN_BPC_TH_P_8LSB	0x0C	RW	Bit[7:0]: RWN BPC positive threshold, encoded in absolute value[7:0]
P1:0xC3	RWN_BPC_TH_N_1MSB	0x00	RW	Bit[7:1]: Not used Bit[0]: RWN BPC negative threshold, encoded in absolute value[8]
P1:0xC4	RWN_BPC_TH_N_8LSB	0x0C	RW	Bit[7:0]: RWN BPC negative threshold, encoded in absolute value[7:0]
P1:0xC5	RWN_BPC_IN_P_1MSB	0x00	RW	Bit[7:1]: Not used Bit[0]: RWN BPC positive data for replacement, encoded in absolute value[8]
P1:0xC6	RWN_BPC_IN_P_8LSB	0x08	RW	Bit[7:0]: RWN BPC positive data for replacement, encoded in absolute value[7:0]
P1:0xC7	RWN_BPC_IN_N_1MSB	0x00	RW	Bit[7:1]: Not used Bit[0]: RWN BPC negative data for replacement, encoded in absolute value[8]
P1:0xC8	RWN_BPC_IN_N_8LSB	0x08	RW	Bit[7:0]: RWN BPC negative data for replacement, encoded in absolute value[7:0]

5.12 dual sensor synchronization [P1:0x0B - P1:0x0C, P1:0x17]

table 5-12 dual sensor synchronization registers

address	register name	default value	R/W	description
P1:0x0B	EXTER_SYNC_CTL	0x00	RW	External Frame Synchronize Control Signal Bit[7]: Not used Bit[6]: exter_frame_num_x256_en When enabled, 1 LSB of exter_sync_frame_num (P1:0x17) equals 256 frames 0: Disable 1: Enable Bit[5]: exter_del_en 0: Disable 1: Enable Bit[4]: exter_sync_manual_en Configure a pos in this bit to trigger a sync output in master mode Bit[3]: exter_sync_auto_en Sensor in master mode will send sync signal every exter_sync_frame_num (P1:0x17) frames automatically 0: Disable 1: Enable Bit[2]: Not used Bit[1]: External sync slave mode 0: Disable 1: Enable Bit[0]: External sync master mode 0: Disable 1: Enable
P1:0x0C	EXTER_SYNC_OUT_WIDTH	0x08	RW	Width of Sync Signal Output When Sensor Is Configured as Master in “dac_clk” Unit
P1:0x17	EXTER_SYNC_FRAME_NUM	0x0A	RW	Interval Frame Number of Auto External Frame Synchronize Pulse

5.13 strobe [P1:0x27, P1:0x34 - P1:0x37]

table 5-13 strobe registers

address	register name	default value	R/W	description
P1:0x27	STROBE_LEVEL	0x00	RW	Bit[7:5]: Not used Bit[4]: col_bin_avg_en Control weight coefficient of digital column binning 0: 31 1: 22 Bit[3:1]: Not used Bit[0]: strobe_level Specify fixed level of strobe signal 0: Low level 1: High level
P1:0x34	STROBE_CTRL	0x00	RW	Bit[7]: strobe_req Bit[6]: strobe_inv Bit[5:4]: xeon_width Bit[3]: strobe_level_en Bit[2]: led3_en Bit[1]: led12_en Bit[0]: xeon_en
P1:0x35	STROBE_DEL_NUM	0x00	RW	Frame Number to be Deleted for Strobe Function in “Frame” Unit
P1:0x36	STROBE_ADD_EXP_ 8MSB	0x00	RW	Bit[7:0]: Exposure time added for strobe LED12 Mode in “H” unit[15:8]
P1:0x37	STROBE_ADD_EXP_ 8LSB	0x20	RW	Bit[7:0]: Exposure time added for strobe LED12 Mode In “H” unit[7:0]

5.14 timing control [P1:0x10 - P1:0x6C, P1:0x6E - P1:0x8B, P1:0xB7 - P1:0xEF]

table 5-14 timing control registers (sheet 1 of 9)

address	register name	default value	R/W	description
P1:0x10	RST_NUM_1MSB	0x00	RW	Bit[7:1]: Not used Bit[0]: rst_num period of reset dac_code[8] (dac_clk unit)
P1:0x11	RST_NUM_8LSB	0x20	RW	Bit[7:0]: rst_num period of reset dac_code[7:0] (dac_clk unit)

table 5-14 timing control registers (sheet 2 of 9)

address	register name	default value	R/W	description
P1:0x12	SIG_NUM_3MSB	0x04	RW	Bit[7:3]: Not used Bit[2:0]: sig_num period of signal dac_code[10:8] (dac_clk unit)
P1:0x13	SIG_NUM_8LSB	0x00	RW	Bit[7:0]: sig_num period of signal dac_code[7:0] (dac_clk unit)
P1:0x14	RST1_INIT_3MSB	0x03	RW	Bit[7:3]: Not used Bit[2:0]: rst1_init value of dac_code[10:8]
P1:0x15	RST1_INIT_8LSB	0xFF	RW	Bit[7:0]: rst1_init value of dac_code[7:0]
P1:0x16	TIMING CTRL 1	0x08	RW	Bit[7:4]: Not used Bit[3]: dac_timing_sel Control timing of col_bl_latch 0: Always high 1: Normal timing Bit[2]: FPN_33ms_data_en Control row address in vertical blank region 0: Force invalid address to 2047 1: Force invalid address to 0 Bit[1:0]: FPN_33ms_timing_sel Control timing in vertical blank region
P1:0x17~ P1:0x19	NOT USED	–	–	Not Used

table 5-14 timing control registers (sheet 3 of 9)

address	register name	default value	R/W	description
P1:0x1A	TIMING CTRL 2	0x7B	RW	Bit[7]: image_lag_test 0: Normal timing 1: Image lag test timing Bit[6]: sc0_timing_sel 0: Sc0 is always low 1: Normal timing Bit[5]: ref_timing_sel 0: ref_ctrl is always high 1: Normal timing Bit[4]: ncp_timing_sel 0: ncp_sw_ctrl is always high 1: Normal timing Bit[3]: pcp_timing_sel 0: pcp_sw_ctrl is always high 1: Normal timing Bit[2]: rch_set 0: RCH=0 when reading even rows, RCH=1 when reading odd rows 1: RCH=1 when reading even rows, RCH=0 when reading odd rows Bit[1]: bwi_timing_sel 0: BWI1 and BWI2 test timing 1: BWI1 and BWI2 normal timing Bit[0]: col_en_timing_sel 0: col_en test timing 1: col_en normal timing
P1:0x1B	NOT USED	–	–	Not Used

table 5-14 timing control registers (sheet 4 of 9)

address	register name	default value	R/W	description
P1:0x1C	TIMING CTRL 3	0xE8	RW	Bit[7]: blk_timing_sel 0: Blk is always high 1: Blk normal timing Bit[6]: nb_timing_sel 0: nb_sw is always high 1: nb_sw normal timing Bit[5]: vref2_timing_sel 0: vref2_sw is always high 1: vref2_sw normal timing Bit[4]: tg_blc_timing_sel 0: Dark row triggers normal timing 1: Dark row triggers particular timing Bit[3]: vlow_timing_sel 0: vlow_sw_ctrl is always high 1: vlow_sw_ctrl normal timing Bit[2]: col_test_tx 0: Triggers normal timing 1: Triggers test timing Bit[1]: extra_reset_en 0: Normal timing 1: Double shutter timing Bit[0]: timing_no_wait_en Control timing waits until column counts completely 0: Wait 1: No wait
P1:0x1D~ P1:0x2F	NOT USED	–	–	Not Used
P1:0x30	BINNING DAC_CODE MODE	0x01	RW	Control Binning dac_code Mode Bit[7:3]: Not used Bit[2]: binning31_large Bit[1]: binning31_en Bit[0]: binning22_en
P1:0x32	RST_NUM2_1MSB	0x00	RW	Bit[7:1]: Not used Bit[0]: rst_num2 period of reset dac_code in “dac_clk” unit[8]
P1:0x33	RST_NUM2_8LSB	0x30	RW	Bit[7:0]: rst_num2 period of reset dac_code in “dac_clk” unit[7:0]
P1:0x34~ P1:0x3B	NOT USED	–	–	Not Used
P1:0x3C	DAC_MODE	0x03	RW	dac_code Mode Control 00: Linear, no DDS 01: Speedup, no DDS 10: Linear, DDS 11: Speedup, DDS

table 5-14 timing control registers (sheet 5 of 9)

address	register name	default value	R/W	description
P1:0x3D~ P1:0x4F	NOT USED	–	–	Not Used
P1:0x50	P0	0x12	RW	P0 Cycle for Pixel Timing (dac_clk Unit)
P1:0x51	P1	0x1A	RW	P1 Cycle for Pixel Timing (dac_clk Unit)
P1:0x52	P2	0x20	RW	P2 Cycle for Pixel Timing (dac_clk Unit)
P1:0x53	P3	0x10	RW	P3 Cycle for Pixel Timing (dac_clk Unit)
P1:0x54	NOT USED	–	–	Not Used
P1:0x55	P5	0x13	RW	P5 Cycle for Pixel Timing (dac_clk Unit)
P1:0x56	P6	0x02	RW	P6 Cycle for Pixel Timing (dac_clk Unit)
P1:0x57	P7_1MSB	0x00	RW	P7 Cycle for Pixel Timing (dac_clk Unit)
P1:0x58	P7_8LSB	0x30	RW	P7 Cycle for Pixel Timing (dac_clk Unit)
P1:0x59	P8	0x01	RW	P8 Cycle for Pixel Timing (dac_clk Unit)
P1:0x5A	P9	0x02	RW	P9 Cycle for Pixel Timing (dac_clk Unit)
P1:0x5B	P10	0x08	RW	P10 Cycle for Pixel Timing (dac_clk Unit)
P1:0x5C	NOT USED	–	–	Not Used
P1:0x5D	P12	0x15	RW	P12 Cycle for Pixel Timing (dac_clk Unit)
P1:0x5E	P13	0x00	RW	P13 Cycle for Pixel Timing (dac_clk Unit)
P1:0x5F	P14	0x00	RW	P14 Cycle for Pixel Timing (dac_clk Unit)
P1:0x60	NOT USED	–	–	Not Used
P1:0x61	P15	0x0F	RW	P15 Cycle for Pixel Timing (dac_clk Unit)
P1:0x62	P16	0x00	RW	P16 Cycle for Pixel Timing (dac_clk Unit)
P1:0x63	P17	0x02	RW	P17 Cycle for Pixel Timing (dac_clk Unit)
P1:0x64	P18	0x40	RW	P18 Cycle for Pixel Timing (dac_clk Unit)
P1:0x65	P19	0x00	RW	P19 Cycle for Pixel Timing (dac_clk Unit)
P1:0x66	P20	0x66	RW	P20 Cycle for Pixel Timing (dac_clk Unit)
P1:0x67	P21	0x00	RW	P21 Cycle for Pixel Timing (dac_clk Unit)
P1:0x68	P22	0x68	RW	P22 Cycle for Pixel Timing (dac_clk Unit)
P1:0x69	P23	0x20	RW	P23 Cycle for Pixel Timing (dac_clk Unit)
P1:0x6A	P24	0x34	RW	P24 Cycle for Pixel Timing (dac_clk Unit)
P1:0x6B	P25	0x10	RW	P25 Cycle for Pixel Timing (dac_clk Unit)

table 5-14 timing control registers (sheet 6 of 9)

address	register name	default value	R/W	description
P1:0x6C	P26	0x10	RW	P26 Cycle for Pixel Timing (dac_clk Unit)
P1:0x6E	P27	0x02	RW	P27 Cycle for Pixel Timing (dac_clk Unit)
P1:0x6F	P28	0x20	RW	P28 Cycle for Pixel Timing (dac_clk Unit)
P1:0x70	P29	0x20	RW	P29 Cycle for Pixel Timing (dac_clk Unit)
P1:0x71	P30	0x10	RW	P30 Cycle for Pixel Timing (dac_clk Unit)
P1:0x72	P31	0x70	RW	P31 Cycle for Pixel Timing (dac_clk Unit)
P1:0x73	P32	0x05	RW	P32 Cycle for Pixel Timing (dac_clk Unit)
P1:0x74	P33_1MSB	0x00	RW	P33 Cycle for Pixel Timing (dac_clk Unit)
P1:0x75	P33_8LSB	0x40	RW	P33 Cycle for Pixel Timing (dac_clk Unit)
P1:0x76	P34	0x05	RW	P34 Cycle for Pixel Timing (dac_clk Unit)
P1:0x77	P35 P36	0xA6	RW	Bit[7:4]: P35 cycle for pixel timing (dac_clk unit) Bit[3:0]: P36 cycle for pixel timing (dac_clk unit)
P1:0x78	P37 P38	0xE6	RW	Bit[7:4]: P37 cycle for pixel timing (dac_clk unit) Bit[3:0]: P38 cycle for pixel timing (dac_clk unit)
P1:0x79	P39 P40	0x42	RW	Bit[7:4]: P39 cycle for pixel timing (dac_clk unit) Bit[3:0]: P40 cycle for pixel timing (dac_clk unit)
P1:0x7A	P41	0x02	RW	P41 Cycle for Pixel Timing (dac_clk Unit)
P1:0x7B	P42	0x02	RW	P42 Cycle for Pixel Timing (dac_clk Unit)
P1:0x7C	P43	0x02	RW	P43 cycle for Pixel Timing (dac_clk Unit)
P1:0x7D	P44	0x10	RW	P44 Cycle for Pixel Timing (dac_clk Unit)
P1:0x7E	P45	0x10	RW	P45 Cycle for Pixel Timing (dac_clk Unit)
P1:0x7F	P46	0x00	RW	P46 Cycle for Pixel Timing (dac_clk Unit)
P1:0x80	P47	0x10	RW	P47 Cycle for Pixel Timing (dac_clk Unit)
P1:0x81	P48	0x10	RW	P48 Cycle for Pixel Timing (dac_clk Unit)
P1:0x82	P50 P51	0x2F	RW	Bit[7:4]: P50 cycle for pixel timing (dac_clk unit) Bit[3:0]: P51 cycle for pixel timing (dac_clk unit)
P1:0x83	P52	0x02	RW	P52 Cycle for Pixel Timing (dac_clk Unit)

table 5-14 timing control registers (sheet 7 of 9)

address	register name	default value	R/W	description
P1:0x84	P53	0x50	RW	P53 Cycle for Pixel Timing (dac_clk Unit)
P1:0x85	P60	0x00	RW	P60 Cycle for Pixel Timing (dac_clk Unit)
P1:0x86~ P1:0x89	NOT USED	–	–	Not Used
P1:0x8A	RH RL	0xCC	RW	Bit[7:4]: RH Bit[3:0]: RL Timing parameter of pixel_bias_ctrl
P1:0x8B	SH SL	0xCC	RW	Bit[7:4]: SH Bit[3:0]: SL Timing parameter of pixel_bias_ctrl
P1:0xB7	B2_NUM_A1_3MSB	0x01	RW	Bit[7:3]: Not used Bit[2:0]: b2_num_a1 period for binning dac_code boost2 in “dac_clk” unit[10:8]
P1:0xB8	B2_NUM_A1_8LSB	0x80	RW	Bit[7:0]: b2_num_a1 period for binning dac_code boost2 in “dac_clk” unit[7:0]
P1:0xB9	B4_NUM_A1_3MSB	0x01	RW	Bit[7:3]: Not used Bit[2:0]: b4_num_a1 period for binning dac_code boost4 in “dac_clk” unit[10:8]
P1:0xBA	B4_NUM_A1_8LSB	0xE0	RW	Bit[7:0]: b4_num_a1 period for binning dac_code boost4 in “dac_clk” unit[7:0]
P1:0xBB	B2_NUM_A2_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: b2_num_a2 period for binning dac_code boost2 in “dac_clk” unit[10:8]
P1:0xBC	B2_NUM_A2_8LSB	0x80	RW	Bit[7:0]: b2_num_a2 period for binning dac_code boost2 in “dac_clk” unit[7:0]
P1:0xBD	B4_NUM_A2_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: b4_num_a2 period for binning dac_code boost4[10:8]
P1:0xBE	B4_NUM_A2_8LSB	0xA0	RW	Bit[7:0]: b4_num_a2 period for binning dac_code boost4[7:0]
P1:0xBF~ P1:0xCD	NOT USED	–	–	Not Used
P1:0xCE	RST_NUM2_BIN_ 8LSB	0x80	RW	Bit[7:0]: rst_num2_bin for binning reset dac_code[7:0]

table 5-14 timing control registers (sheet 8 of 9)

address	register name	default value	R/W	description
P1:0xCF	RST_NUM2_BIN_ 2MSB	0x00	RW	Bit[7:2]: Not used Bit[1:0]: rst_num2_bin for binning reset dac_code[9:8]
P1:0xD0	BOOST_EN	0x03	RW	dac_code Boost Enable 00: No boost 01: Boost with only step 2 10: Boost with only step 4 11: Boost with both step 2 and step 4
P1:0xD1	B2_NUM_3MSB	0x02	RW	Bit[7:3]: Not used Bit[2:0]: b2_num period for normal dac_code boost2 in “dac_clk” unit[10:8]
P1:0xD2	B2_NUM_8LSB	0x40	RW	Bit[7:0]: b2_num period for normal dac_code boost2 in “dac_clk” unit[7:0]
P1:0xD3	B4_NUM_3MSB	0x02	RW	Bit[7:3]: Not used Bit[2:0]: b4_num period for normal dac_code boost4 in “dac_clk” unit[10:8]
P1:0xD4	B4_NUM_8LSB	0xC0	RW	Bit[7:0]: b4_num period for normal dac_code boost4 in “dac_clk” unit[7:0]
P1:0xD5	A1 A2	0x31	RW	Bit[7]: Not used Bit[6:4]: A1 Bit[3]: Not used Bit[2:0]: A2 Control binning dac_code steps
P1:0xD6	RST_NUM_BIN_8LSB	0x80	RW	Bit[7:0]: rst_num_bin for binning reset dac_code[7:0]
P1:0xD7	RST_NUM_BIN_ 2MSB	0x00	RW	Bit[7:2]: Not used Bit[1:0]: rst_num_bin for binning reset dac_code[9:8]
P1:0xD8	SIG_NUM_BIN_8LSB	0x00	RW	Bit[7:0]: sig_num_bin for binning signal dac_code[7:0]
P1:0xD9	SIG_NUM_BIN_3MSB	0x04	RW	Bit[7:3]: Not used Bit[2:0]: sig_num_bin for binning signal dac_code[10:8]
P1:0xDA	RCNT_NUM_A1_ 8LSB	0xC0	RW	Bit[7:0]: rcnt_num_a1 for binning reset counter[7:0]
P1:0xDB	RCNT_NUM_A1_ 2MSB	0x00	RW	Bit[7:2]: Not used Bit[1:0]: rcnt_num_a1 for binning reset counter[9:8]
P1:0xDC	SCNT_NUM_A1_ 8LSB	0x40	RW	Bit[7:0]: scnt_num_a1 for binning signal counter[7:0]

table 5-14 timing control registers (sheet 9 of 9)

address	register name	default value	R/W	description
P1:0xDD	SCNT_NUM_A1_ 2MSB	0x02	RW	Bit[7:2]: Not used Bit[1:0]: scnt_num_a1 for binning signal counter[9:8]
P1:0xDE	RCNT_NUM_A2_ 8LSB	0x40	RW	Bit[7:0]: rcnt_num_a2 for binning reset counter[7:0]
P1:0xDF	RCNT_NUM_A2_ 2MSB	0x00	RW	Bit[7:2]: Not used Bit[1:0]: rcnt_num_a2 for binning reset counter[9:8]
P1:0xE0~ P1:0xE8	NOT USED	–	–	Not Used
P1:0xE9	BINNING13_CODE_ EN	0x01	RW	Control Binning dac_code Mode
P1:0xEA	SCNT_NUM_A2_ 8LSB	0xCO	RW	Bit[7:0]: scnt_num_a2 period for binning reset counter in “dac_clk” unit[7:0]
P1:0xEB	SCNT_NUM_A2_ 2MSB	0x00	RW	Bit[7:2]: Not used Bit[1:0]: scnt_num_a2 period for binning reset counter in “dac_clk” unit[9:8]
P1:0xEC	RCNT_NUM_2MSB	–	R	Bit[7:2]: Not used Bit[1:0]: rcnt_num calculated in timing_gen[9:8]
P1:0xED	RCNT_NUM_8LSB	–	R	Bit[7:0]: rcnt_num calculated in timing_gen[7:0]
P1:0xEE	SCNT_NUM_4MSB	–	R	Bit[7:4]: Not used Bit[3:0]: scnt_num calculated in timing_gen[11:8]
P1:0xEF	SCNT_NUM_8LSB	–	R	Bit[7:0]: scnt_num calculated in timing_gen[7:0]

5.15 analog control [P1:0x19, P1:0x1E - P1:0x1F, P1:0x20 - P1:0x2E, P1:0xE7]

table 5-15 analog control registers (sheet 1 of 3)

address	register name	default value	R/W	description
P1:0x19	ICOMP	0xC1	RW	Bit[7:4]: Icomp1 Control first stage comparator bias current Bit[3:0]: Icomp2 Control second stage comparator bias current
P1:0x1E	ANALOG CTRL 1	0x02	RW	Bit[7:2]: Not used Bit[1]: en_dac Enable current DAC Bit[0]: vref2_ds_sel Reference voltage driver of second stage comparator
P1:0x1F	ANALOG CTRL 2	0x31	RW	Bit[7:6]: Not used Bit[5]: cp1_en Clock driver of positive charge pump Bit[4]: cp2_en Clock driver of positive charge pump Bit[3:2]: blcmp_bias Column blackout bias control Bit[1:0]: pll_icp_sel PLL charge pump current control
P1:0x20	VNCP	0x7B	RW	Bit[7]: Not used Bit[6:4]: vncp_en Select driver ability of NCP Bit[3:0]: vncp_sel Select output voltage of NCP for tx
P1:0x21	PCP_RST_SEL	0x40	RW	Bit[7]: Not used Bit[6:4]: pcp_rst_sel Select output voltage of charge pump for restg Bit[3:0]: Not used
P1:0x22~ P1:0x24	NOT USED	–	–	Not Used
P1:0x25	ANALOG CTRL 3	0x20	RW	Bit[7]: bl_en Black out control signal of column Bit[6:3]: Vblsel Sunspot detection voltage Bit[2:0]: Tcon1 Test control

table 5-15 analog control registers (sheet 2 of 3)

address	register name	default value	R/W	description
P1:0x26	ANALOG CTRL 4	0x5A	RW	Bit[7:6]: vref2_com_sel Reference voltage of second stage comparator control Bit[5:2]: vlow_com_sel Reference voltage of FD low voltage Bit[1:0]: vlow_ds_sel Reference voltage driver of FD low voltage
P1:0x27~ P1:0x28	NOT USED	–	–	Not Used
P1:0x29	ANALOG CTRL 5	0x03	RW	Bit[7:2]: Not used Bit[1]: sc1_sel Select PMOS switch Bit[0]: sa_mode Sense amp mode select
P1:0x2A	ANALOG CTRL 6	0xAA	RW	Bit[7:5]: ADC range control Bit[4:2]: rgcnt_ctl Select output voltage of counter regulator Bit[1:0]: rgcol_ctl Regulator of column decoder control
P1:0x2B	ANALOG CTRL 7	0x02	RW	Bit[7:5]: Not used Bit[4:2]: sa_irst_ctl Latch pulse width control of SA Bit[1:0]: sa_pw1_ctl Reset pulse width control of SA
P1:0x2C	ANALOG CTRL 8	0x60	RW	Bit[7]: Not used Bit[6]: adc_high_8bit When set to high, dataout = datain When set to low, dataout = {datain[7:0], 2'h0} Bit[5:4]: pvdd_sel Select pixel LDO output voltage Bit[3:0]: cntclk_delay Delay counter clock
P1:0x2D	ANALOG CTRL 9	0x00	RW	Bit[7:4]: colclk_delay Delay column decoder clock Bit[3:0]: dacclk_delay Delay DAC clock
P1:0x2E	ANALOG CTRL 10	0x00	RW	Bit[7:4]: dclk_delay Delay dclk clock Bit[3:0]: saclk_delay Delay sense amplifier clock

table 5-15 analog control registers (sheet 3 of 3)

address	register name	default value	R/W	description
P1:0xE7	REG_UPDATE	0x00	RW	Bit[7:2]: Not used Bit[1]: reg_update_mode Bit[0]: reg_update_cmd Control register to take effect immediately

5.16 MIPI [P1:0x8E - P1:0x98, P1:0x9C - P1:0x9D, P1:0xA0 - P1:0xAF, P1:0xB1 - P1:0xB5]

table 5-16 MIPI registers (sheet 1 of 4)

address	register name	default value	R/W	description
P1:0x8E	H_SIZE_MIPI_4MSB	0x07	RW	MIPI Column Number
P1:0x8F	H_SIZE_MIPI_8LSB	0x90	RW	MIPI Column Number
P1:0x90	V_SIZE_MIPI_3MSB	0x04	RW	MIPI Line Number
P1:0x91	V_SIZE_MIPI_8LSB	0x48	RW	MIPI Line Number
P1:0x92	MIPI CTRL 1	0x02	RW	Bit[7]: Not used Bit[6]: MIPI data driver control Bit[5]: MIPI clock driver control Bit[4]: MIPI data driver selected Bit[4:3]: MIPI clock driver selected Bit[2]: LP driver ability Bit[1:0]: LP voltage level
P1:0x93	R_CLK_POST	0x0A	RW	Clock Lane Post Time Control
P1:0x94	MIPI CTRL 2	0x33	RW	Bit[7:4]: Clock lane LPX time control Bit[3:0]: Data lane LPX time control
P1:0x95	PREPARE	0x22	RW	Bit[7:4]: Clock lane prepare time control Bit[3:0]: Data lane prepare time control
P1:0x96	R_HS_ZERO	0x06	RW	Data Lane Zero Time Control
P1:0x97	DATA ID	0x2B	RW	Bit[7:6]: Virtual lane select Bit[5:0]: Data type select 0x2A: Raw8 0x2B: Raw10
P1:0x98	TRAIL	0x23	RW	Bit[7:4]: Clock lane trail time control Bit[3:0]: Data lane trail time control
P1:0x9C	R_CLK_ZERO	0x09	RW	Clock Lane Zero Time Control

table 5-16 MIPI registers (sheet 2 of 4)

address	register name	default value	R/W	description
P1:0x9D	HS	0x15	RW	Bit[7]: MIPI clock mode control 0: mipi_clk continuous (default) 1: Switch Bit[6]: HS voltage control: 0 Bit[5:4]: Data1, hs_level: 01 Bit[3:2]: Ata0, hs_level: 01 Bit[1:0]: Clock, hs_level: 01
P1:0xA0	MIPI_EN_BUF	0x00	RW	mipi_en_buf
P1:0xA1	MIPI CTRL 3	0x02	RW	Bit[7:5]: Not used Bit[4:3]: MIPI FS packet to LS packet time control Bit[2:0]: MIPI transmission speed select
P1:0xA2	R_INIT_M	0x0B	RW	MIPI Initial Time Control Bit
P1:0xA3	R_INIT_L	0x40	RW	MIPI Initial Time Control Bit
P1:0xA4	MIPI CTRL 4	0x40	RW	Bit[7:6]: Not used Bit[5:2]: r_exit Data lane exit time control Bit[1:0]: MIPI wakeup time control[17:16]
P1:0xA5	R_WAKEUP_M	0x86	RW	Bit[7:0]: MIPI wakeup time control[15:8]
P1:0xA6	R_WAKEUP_L	0x88	RW	Bit[7:0]: MIPI wakeup time control[7:0]
P1:0xA7	DC_TEST_LP_LK	0x3F	RW	MIPI Output Control When MIPI in MIPI DC Test Mode Bit[7]: MIPI clock output control 0: MIPI clock pad output in LP state 1: MIPI clock pad output in HS state Bit[6]: MIPI data output control 0: MIPI clock pad output in LP state 1: MIPI clock pad output in HS state Bit[5:4]: MIPI CKP/CKN voltage control Bit[3:2]: MIPI D0P/D0N voltage control Bit[1:0]: MIPI D1P/D1N voltage control
P1:0xA8	DC_TEST_DATA_HS	0xFF	RW	MIPI Output Control When MIPI in MIPI DC Test Mode
P1:0xA9~ P1:0xAD	NOT USED	–	–	Not Used
P1:0xAE	FRAME_END_DLY LSB	0x65	RW	Time Control Between Long Packet and FE Packet

table 5-16 MIPI registers (sheet 3 of 4)

address	register name	default value	R/W	description
P1:0xAF	FRAME_END_DLY MSB	0x00	RW	Time Control Between Long Packet and FE Packet
P1:0xB1	HS	0x82	RW	Bit[7]: MIPI clock switch control 0: MIPI clock enter LP state when vblank time and hblank time 1: MIPI clock enter LP state when vblank time Bit[6]: Not used Bit[5:3]: ph_delay Bit[2:1]: Control phase between MIPI clock and data 00: 1/4 UI 01: 1/2 UI 10: 3/4 UI 11: Not used Bit[0]: MIPI PHY shutdown control 0: MIPI DPHY shutdown 1: Enable DPHY
P1:0xB2	MIPI CTRL 4	0x40	RW	Bit[7]: MIPI clock lane start mode 0: MIPI clock enters LP mode when MIPI work 1: MIPI clock lane enters HS mode when MIPI work Bit[6]: Double lane control 0: MIPI works in single lane mode 1: MIPI works in double lane mode Bit[5]: MIPI DC test mode enable 0: MIPI works in normal mode 1: MIPI works in DC test mode Bit[4]: MIPI output pad control 0: MIPI output pad tri-stated when MIPI is not working 1: MIPI output pad driving ground when MIPI is not working Bit[3]: MIPI initial mode enable 0: MIPI works in normal mode 1: MIPI works in initial mode Bit[2]: MIPI ULP mode enable 0: MIPI works in normal mode 1: MIPI works in ULP mode Bit[1]: MIPI line sync mode enable Bit[0]: Test mode MIPI test color bar 0: MIPI outputs ISP image 1: MIPI outputs test pattern
P1:0xB3	MIPI CTRL 5	0x09	RW	Bit[7]: Not used Bit[6:2]: MIPI PLL NC control Bit[1:0]: MIPI PLL MC control

table 5-16 MIPI registers (sheet 4 of 4)

address	register name	default value	R/W	description
P1:0xB4	MIPI CTRL 6	0x11	RW	Bit[7:6]: Not used Bit[5:4]: MIPI PLL current control Bit[3]: MIPI PLL bypass enable Bit[2]: MIPI PLL enable 0: MIPI PLL power down 1: MIPI PLL work normally Bit[1:0]: MIPI PLL output clock frequency
P1:0xB5	MIPI CTRL 7	0x00	RW	Bit[7:4]: MIPI PLL current control Bit[3:0]: PFD delay control

5.17 state [P2:0x05, P2:0x10 - P2:0x19]

table 5-17 state registers (sheet 1 of 2)

address	register name	default value	R/W	description
P2:0x05	FIX_STATE	0x00	RW	Bit[7:5]: Not used Bit[4]: fix_state_en Fix state enable 0: Disable fix state 1: Enable fix state Bit[3]: Not used Bit[2:0]: fix_state_mode Fix which mode of state
P2:0x10	EXP_NR_OUTD_8HSB	0x00	RW	Exposure Threshold High Byte from Normal to Outdoor
P2:0x11	EXP_NR_OUTD_8LSB	0x8B	RW	Exposure Threshold Low Byte from Normal to Outdoor
P2:0x12	EXP_OUTD_NR_8HSB	0x00	RW	Exposure Threshold High Byte from Outdoor to Normal
P2:0x13	EXP_OUTD_NR_8LSB	0x8D	RW	Exposure Threshold Low Byte from Outdoor to Normal
P2:0x14	EXP_HEQ_DUMMY_8HSM	0x04	RW	Exposure Threshold High Byte Between Normal and Dummy
P2:0x15	EXP_HEQ_DUMMY_8LSM	0x60	RW	Exposure Threshold Low Byte Between Normal and Dummy
P2:0x16	EXP_HEQ_LOW_8HSM	0x04	RW	Exposure Threshold High Byte Between Normal and Low Light

table 5-17 state registers (sheet 2 of 2)

address	register name	default value	R/W	description
P2:0x17	EXP_HEQ_LOW_ 8LSM	0x60	RW	Exposure Threshold Low Byte Between Normal and Low Light
P2:0x18	RPC_HEQ_LOW	0xC0	RW	RPC Threshold Between Normal and Low Light
P2:0x19	RPC_HEQ_DUMMY	0x80	RW	RPC Threshold Between Normal and Dummy

5.18 package [P2:0x35]

table 5-18 package registers

address	register name	default value	R/W	description
P2:0x35	OUTMODE1	0x00	RW	Bit[7:2]: Not used Bit[1]: unpro_raw_out_en Unprocessed raw output enable 0: Disable unprocessed raw 1: Enable unprocessed raw Bit[0]: Not used

5.19 memory [P2:0x5E - P2:0x5F]

table 5-19 memory registers

address	register name	default value	R/W	description
P2:0x5E	MEMORY CTRL 1	0x07	RW	Bit[7:4]: Not used Bit[3]: line_buf_standby Memory CEN 0: Enable memory work 1: Disable memory work Bit[2]: mem_down_en Memory shut down enable when hblank 0: Disable memory shut down 1: Enable memory shut down Bit[1]: auto_first_en Auto br_frst enable up/down or mirror 0: Disable auto BR first 1: Enable auto BR first Bit[0]: br_first Output B/R first or G first 0: Gb/Gr first output 1: B/R first output
P2:0x5F	MEMORY CTRL 2	0x00	RW	Bit[7:5]: Not used Bit[4]: Error_flag_mem 0: There is no error 1: There is error Bit[3:2]: Not used Bit[1]: test_done_mem 0: Test is not done 1: Test is done Bit[0]: Memory BIST test enable 0: Disable memory BIST test 1: Enable memory BIST test

5.20 BPC [P2:0x34, P2:0x5D, P2:0x60 - P2:0x92, P3:0xC0, P4:0x12 - P4:0x3F]

table 5-20 BPC registers (sheet 1 of 5)

address	register name	default value	R/W	description
P2:0x34	ISP_MODE	0xFF	RW	Bit[7]: bpc_dpix_en Double bad pixel enable 0: Disable double bad pixel 1: Enable double bad pixel Bit[6]: bpc_flt_en Filter BPC field enable 0: Disable BPC field 1: Enable BPC field Bit[5]: Not used Bit[4]: awbgain_position_set AWB gain position reverse 0: Disable awbgain_position revise 1: Enable awbgain_position revise Bit[3]: demo_en demo_gf bypass enable 0: Disable demo_gf work 1: Enable demo_gf work Bit[2:0]: Not used
P2:0x5D	BPC CTRL 1	0x01	RW	Bit[7:2]: Not used Bit[1:0]: bayer_order Bayer raw order 00: GBGB 01: BGBG 10: GRGR 11: RGRG
P2:0x60	LSC_BPC_EN	0xFF	RW	Bit[7:4]: Not used Bit[3]: BPC enable in dummy 0: Disable 1: Enable Bit[2]: BPC enable in outdoor 0: Disable 1: Enable Bit[1]: BPC enable in normal 0: Disable 1: Enable Bit[0]: BPC enable in lowlight 0: Disable 1: Enable
P2:0x61	VSYNC_DELAY_NUM	0x00	RW	Line Number of VSYNC Delay
P2:0x62	ROW_START LSB	0x01	RW	Low Byte of Starting Point of Row Counting

table 5-20 BPC registers (sheet 2 of 5)

address	register name	default value	R/W	description
P2:0x63	ROW_START MSB	0x00	RW	High Byte of Starting Point of Row Counting
P2:0x64~ P2:0x8F	NOT USED	–	–	Not Used
P2:0x90	DP_DIF_TH_B_ NORMAL	0x1E	RW	Double Bad Pixel Black Threshold in Normal
P2:0x91	DP_DIF_TH_B_ DUMMY	0x1E	RW	Double Bad Pixel Black Threshold in Dummy
P2:0x92	DP_DIF_TH_B_LOW	0x1E	RW	Double Bad Pixel Black Threshold in Low Light
P3:0xC0	DP_POS_EN	0x00	RW	OTP Sends DPIX Coordinate Enable 0: Disable OTP send DPIX coordinate 1: Enable OTP send DPIX coordinate
P4:0x12	ISP_REGF_12	0x00	RW	bpc_vt_eff BPC Offset Ratio Value
P4:0x13	ISP_REGF_13	0x00	RW	bpc_wt_eff BPC White Minimum Threshold
P4:0x14	ISP_REGF_14	0x14	RW	bpc_dt_eff BPC Black Maximum Threshold
P4:0x15	ISP_REGF_15	0x80	RW	bpc_range_thr_outdoor DBPC Range Threshold in Outdoor
P4:0x16	ISP_REGF_16	0x80	RW	bpc_range_thr_nr DBPC Range Threshold in Normal
P4:0x17	ISP_REGF_17	0x80	RW	bpc_range_thr_dummy DBPC Range Threshold in Dummy
P4:0x18	ISP_REGF_18	0x80	RW	Bpc_range_thr_low DBPC Range Threshold In Low Light
P4:0x19	ISP_REGF_19	0x10	RW	bpc_dif_thr_outdoor BPC Grad Difference Threshold in Outdoor
P4:0x1A	ISP_REGF_1A	0x10	RW	bpc_dif_thr_nr BPC Grad Difference Threshold in Normal
P4:0x1B	ISP_REGF_1B	0x10	RW	bpc_dif_thr_dummy BPC Grad Difference Threshold in Dummy
P4:0x1C	ISP_REGF_1C	0x10	RW	bpc_dif_thr_low BPC Grad Difference Threshold in Low Light
P4:0x1D	ISP_REGF_1D	0x10	RW	bpc_grad_thr_outdoor BPC Edge Grad Threshold in Outdoor
P4:0x1E	ISP_REGF_1E	0x10	RW	bpc_grad_thr_nr BPC Edge Grad Threshold in Normal

table 5-20 BPC registers (sheet 3 of 5)

address	register name	default value	R/W	description
P4:0x1F	ISP_REGF_1F	0x10	RW	bpc_grad_thr_dummy BPC Edge Grad Threshold in Dummy
P4:0x20	ISP_REGF_20	0x10	RW	bpc_grad_thr_low BPC Edge Grad Threshold in Low Light
P4:0x21	ISP_REGF_21	0x46	RW	white_range_thr_outdoor Below this interval pixel value judgment point is without relative difference, but absolute difference in outdoor
P4:0x22	ISP_REGF_22	0x46	RW	white_range_thr_nr Below this interval pixel value judgment point is without relative difference, but absolute difference in normal
P4:0x23	ISP_REGF_23	0x46	RW	white_range_thr_dummy Below this interval pixel value judgment point is without relative difference, but absolute difference in dummy
P4:0x24	ISP_REGF_24	0x46	RW	white_range_thr_low Below this interval pixel value judgment point is without relative difference, but absolute difference in low light
P4:0x25	ISP_REGF_25	0x0A	RW	white_delta_thr_outdoor Determines absolute difference of use of bright pixels in outdoor
P4:0x26	ISP_REGF_26	0x0A	RW	white_delta_thr_normal Determines absolute difference of use of bright pixels in normal
P4:0x27	ISP_REGF_27	0x0A	RW	white_delta_thr_dummy Determines absolute difference of use of bright pixels in dummy
P4:0x28	ISP_REGF_28	0x0A	RW	white_delta_thr_low Determines absolute difference of use of bright pixels in lowlight
P4:0x29	ISP_REGF_29	0x0A	RW	black_delta_thr_outdoor Determines absolute difference of use of dark pixels in outdoor
P4:0x2A	ISP_REGF_2A	0x0A	RW	black_delta_thr_normal Determines absolute difference of use of dark pixels in normal
P4:0x2B	ISP_REGF_2B	0x0A	RW	black_delta_thr_dummy Determines absolute difference of use of dark pixels in dummy

table 5-20 BPC registers (sheet 4 of 5)

address	register name	default value	R/W	description
P4:0x2C	ISP_REGF_2C	0x0A	RW	black_delta_thr_low Determines absolute difference of use of dark pixels in lowlight
P4:0x2D	ISP_REGF_2D	0x0A	RW	bpc_flag_thr_outdoor Third row of central point and first line of three number of comparison, threshold control in outdoor
P4:0x2E	ISP_REGF_2E	0x0A	RW	bpc_flag_thr_normal Third row of central point and first line of three number of comparison, threshold control in normal
P4:0x2F	ISP_REGF_2F	0x0A	RW	bpc_flag_thr_dummy Third row of central point and first line of three number of comparison, threshold control in dummy
P4:0x30	ISP_REGF_30	0x0A	RW	bpc_flag_thr_low Third row of central point and first line of three number of comparison, threshold control in lowlight
P4:0x31	ISP_REGF_31	0x32	RW	dpix_wht_ofst_outdoor DPIX White Minimum Offset Value in Outdoor
P4:0x32	ISP_REGF_32	0x32	RW	dpix_wht_ofst_normal DPIX White Minimum Offset Value in Normal
P4:0x33	ISP_REGF_33	0x32	RW	dpix_wht_ofst_dummy DPIX White Minimum Offset Value in Dummy
P4:0x34	ISP_REGF_34	0x32	RW	dpix_wht_ofst_low DPIX White Minimum Offset Value in Low Light
P4:0x35	ISP_REGF_35	0x20	RW	dpix_blk_ofst_outdoor DPIX Black Minimum Offset Value in Outdoor
P4:0x36	ISP_REGF_36	0x20	RW	dpix_blk_ofst_normal DPIX Black Minimum Offset Value in Normal
P4:0x37	ISP_REGF_37	0x20	RW	dpix_blk_ofst_dummy DPIX Black Minimum Offset Value in Dummy
P4:0x38	ISP_REGF_38	0x20	RW	dpix_blk_ofst_low DPIX Black Minimum Offset Value in Low Light

table 5-20 BPC registers (sheet 5 of 5)

address	register name	default value	R/W	description
P4:0x39	ISP_REGF_39	0x00	RW	Bit[7:6]: dpix_wht_ratio_outdoor Double bad pixel white ratio in outdoor Bit[5:4]: dpix_wht_ratio_normal Double bad pixel white ratio in normal Bit[3:2]: dpix_wht_ratio_dummy Double bad pixel white ratio in dummy Bit[1:0]: dpix_wht_ratio_low Double bad pixel white ratio in lowlight
P4:0x3A	ISP_REGF_3A	0xFF	RW	Bit[7:6]: dpix_blk_ratio_outdoor Double bad pixel black ratio in outdoor Bit[5:4]: dpix_blk_ratio_normal Double bad pixel black ratio in normal Bit[3:2]: dpix_blk_ratio_dummy Double bad pixel black ratio in dummy Bit[1:0]: dpix_blk_ratio_low Double bad pixel black ratio in lowlight
P4:0x3B	ISP_REGF_3B	0x1E	RW	dp_dif_th_w_outdoor Double Bad Pixel White Threshold in Outdoor
P4:0x3C	ISP_REGF_3C	0x1E	RW	dp_dif_th_w_normal Double Bad Pixel White Threshold in Normal
P4:0x3D	ISP_REGF_3D	0x1E	RW	dp_dif_th_w_dummy Double Bad Pixel White Threshold in Dummy
P4:0x3E	ISP_REGF_3E	0x1E	RW	dp_dif_th_w_low Double Bad Pixel White Threshold in Low Light
P4:0x3F	ISP_REGF_3F	0x1E	RW	dp_dif_th_b_outdoor Double Bad Pixel Black Threshold in Outdoor

5.21 demo SIF [P2:0xA0 - P2:0xA7, P2:0xC0 - P2:0xD3]

table 5-21 demo SIF registers (sheet 1 of 2)

address	register name	default value	R/W	description
P2:0xA0	DEM_V_START_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Image vertical start[10:8]
P2:0xA1	DEM_V_START_8LSB	0x00	RW	Bit[7:0]: Image vertical start[7:0]
P2:0xA2	DEM_V_SIZE_3MSB	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Image vertical size[10:8]
P2:0xA3	DEM_V_SIZE_8LSB	0x48	RW	Bit[7:0]: Image vertical size[7:0]
P2:0xA4	DEM_H_START_3MSB	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Image horizontal start[10:8]
P2:0xA5	DEM_H_START_8LSB	0x00	RW	Bit[7:0]: Image horizontal start[7:0]
P2:0xA6	DEM_H_SIZE_3MSB	0x03	RW	Bit[7:3]: Not used Bit[2:0]: Image half horizontal size[10:8]
P2:0xA7	DEM_H_SIZE_8LSB	0xC8	RW	Bit[7:0]: Image half horizontal size[7:0]
P2:0xC0	RAW_R_OFFSET_8LSB_ OUTDOOR	0x00	RW	Bit[7:0]: Offset add on R channel in outdoor[7:0]
P2:0xC1	RAW_R_OFFSET_8LSB_ NORMAL	0x00	RW	Bit[7:0]: Offset Add on R channel in normal[7:0]
P2:0xC2	RAW_R_OFFSET_8LSB_ DUMMY	0x00	RW	Bit[7:0]: Offset add on R channel in dummy[7:0]
P2:0xC3	RAW_R_OFFSET_8LSB_ LOW	0x00	RW	Bit[7:0]: Offset add on R channel in low light[7:0]
P2:0xC4	RAW_R_OFFSET	0x00	RW	Bit[7:6]: Offset add on R channel in outdoor[9:8] Bit[5:4]: Offset add on R channel in normal[9:8] Bit[3:2]: Offset add on R channel in dummy[9:8] Bit[1:0]: Offset add on R channel in lowlight[9:8]
P2:0xC5	RAW_B_OFFSET_8LSB_ OUTDOOR	0x00	RW	Bit[7:0]: Offset add on B channel in outdoor[7:0]
P2:0xC6	RAW_B_OFFSET_8LSB_ NORMAL	0x00	RW	Bit[7:0]: Offset Add on B channel in normal[7:0]
P2:0xC7	RAW_B_OFFSET_8LSB_ DUMMY	0x00	RW	Bit[7:0]: Offset add on B channel in dummy[7:0]

table 5-21 demo SIF registers (sheet 2 of 2)

address	register name	default value	R/W	description
P2:0xC8	RAW_B_OFFSET_8LSB_LOW	0x00	RW	Bit[7:0]: Offset add on B channel in low light[7:0]
P2:0xC9	RAW_B_OFFSET	0x00	RW	Bit[7:6]: Offset add on B channel in outdoor[9:8] Bit[5:4]: Offset add on B channel in normal[9:8] Bit[3:2]: Offset add on B channel in dummy[9:8] Bit[1:0]: Offset add on B channel in lowlight[9:8]
P2:0xCA	RAW_GR_OFFSET_8LSB_OUTDOOR	0x00	RW	Bit[7:0]: Offset add on Gr channel in outdoor[7:0]
P2:0xCB	RAW_GR_OFFSET_8LSB_NORMAL	0x00	RW	Bit[7:0]: Offset add on Gr channel in normal[7:0]
P2:0xCC	RAW_GR_OFFSET_8LSB_DUMMY	0x00	RW	Bit[7:0]: Offset add on Gr channel in dummy[7:0]
P2:0xCD	RAW_GR_OFFSET_8LSB_LOW	0x00	RW	Bit[7:0]: Offset add on Gr channel in low light[7:0]
P2:0xCE	RAW_GR_OFFSET	0x00	RW	Bit[7:6]: Offset add on Gr channel in outdoor[9:8] Bit[5:4]: Offset add on Gr channel in normal[9:8] Bit[3:2]: Offset add on Gr channel in dummy[9:8] Bit[1:0]: Offset add on Gr channel in lowlight[9:8]
P2:0xCF	RAW_GB_OFFSET_8LSB_OUTDOOR	0x00	RW	Bit[7:0]: Offset add on Gb channel in outdoor[7:0]
P2:0xD0	RAW_GB_OFFSET_8LSB_NORMAL	0x00	RW	Bit[7:0]: Offset Add on Gb channel in normal[7:0]
P2:0xD1	RAW_GB_OFFSET_8LSB_DUMMY	0x00	RW	Bit[7:0]: Offset add on Gb channel in dummy[7:0]
P2:0xD2	RAW_GB_OFFSET_8LSB_LOW	0x00	RW	Bit[7:0]: Offset add on Gb channel in low light[7:0]
P2:0xD3	RAW_GB_OFFSET	0x00	RW	Bit[7:6]: Offset add on Gb channel in outdoor[9:8] Bit[5:4]: Offset add on Gb channel in normal[9:8] Bit[3:2]: Offset add on Gb channel in dummy[9:8] Bit[1:0]: Offset add on Gb channel in lowlight[9:8]

5.22 OTP status [P3:0xE7, P3:0xEC]

table 5-22 OTP status registers

address	register name	default value	R/W	description
P3:0xE7	PGM_PERMIT	0x00	RW	OTP Programming Permit Flag 0: Forbid PGM process 1: PGM process permit
P3:0xEC	OTP STATUS CTRL 1	0x00	RW	Bit[7:4]: Not used Bit[3]: otp_pgm_flag OTP program flag Bit[2]: read_flag Byte read flag Bit[1]: bat_rd_flag OTP batch read flag Bit[0]: otp_busy OTP busy flag All flags read only

5.23 OTP mode control [P3:0xC0, P3:0xEA - P3:0xEB, P3:0xE8, P3:0xD0]

table 5-23 OTP mode control registers (sheet 1 of 2)

address	register name	default value	R/W	description
P3:0xC0	DP_POS_EN	0x00	RW	Enable Signal Transferring Position of Dead Pixel from OTP to ISP 0: Disable transferring 1: Enable transferring
P3:0xEA	DATA_BYT_WR	0x00	RW	Data Required to Program to OTP in Byte Program Mode
P3:0xEB	ADDR_BYT_WR	0x00	RW	OTP Cell Address in Byte Program Mode
P3:0xE8	OTP_PGM_EN	0x00	RW	Start Program OTP Note: Before using this command, user should make sure that OTP is not busy and has written exact address with a suitable value when program operation permits

table 5-23 OTP mode control registers (sheet 2 of 2)

address	register name	default value	R/W	description
P3:0xD0	OTP MODE CTRL 1	0x00	RW	Bit[7:3]: Not used Bit[2:1]: page_half_flag Select signal of OTP batch program address 00: Select OTP 0x00~0x3F to program 01: Select OTP 0x40~0x7F to program 10: Select OTP 0x80~0xBF to program 11: Select OTP 0xC0~0xFF to program Bit[0]: otp_batch_en 0: Disable batch program 1: Start batch program

5.24 OTP batch buffer [P4:0x00 - P4:0x3F]

table 5-24 OTP batch buffer registers (sheet 1 of 3)

address	register name	default value	R/W	description
P4:0x00	FLAG_LOAD0	0x00	RW	Bit[7:5]: Not used Bit[4]: flag_load0 Block 4 programmed flag 0: Block 4 is empty 1: Block 4 is programmed Bit[3]: flag_load0 Block 3 programmed flag 0: Block 3 is empty 1: Block 3 is programmed Bit[2]: flag_load0 Block 2 programmed flag 0: Block 2 is empty 1: Block 2 is programmed Bit[1]: flag_load0 Block 1 programmed flag 0: Block 1 is empty 1: Block 1 is programmed Bit[0]: flag_load0 Block 0 programmed flag 0: Block 0 is empty 1: Block 0 is programmed
P4:0x01	FLAG_LOAD1	0x00	RW	Reserved Flag Register
P4:0x02	LINE_CODE	0x00	RW	Production Identification

table 5-24 OTP batch buffer registers (sheet 2 of 3)

address	register name	default value	R/W	description
P4:0x03	LOT_YEAR LOT_MONTH	0x00	RW	Production Identification
P4:0x04	LOT_DAY	0x00	RW	Production Identification
P4:0x05	LOT_SNUM	0x00	RW	Production Identification
P4:0x06	WAFER_ID	0x00	RW	Production Identification
P4:0x07	WAFER_X	0x00	RW	Production Identification
P4:0x08	WAFER_Y	0x00	RW	Production Identification
P4:0x09~ P4:0x11	RSVD	–	–	Reserved
P4:0x12	ISP_REGF_12	0x00	RW	Data Byte 12 in Batch Operation Mode
P4:0x13	ISP_REGF_13	0x00	RW	Data Byte 13 in Batch Operation Mode
P4:0x14	ISP_REGF_14	0x14	RW	Data Byte 14 in Batch Operation Mode
P4:0x15	ISP_REGF_15	0x80	RW	Data Byte 15 in Batch Operation Mode
P4:0x16	ISP_REGF_16	0x80	RW	Data Byte 16 in Batch Operation Mode
P4:0x17	ISP_REGF_17	0x80	RW	Data Byte 17 in Batch Operation Mode
P4:0x18	ISP_REGF_18	0x80	RW	Data Byte 18 in Batch Operation Mode
P4:0x19	ISP_REGF_19	0x10	RW	Data Byte 19 in Batch Operation Mode
P4:0x1A	ISP_REGF_1A	0x10	RW	Data Byte 1A in Batch Operation Mode
P4:0x1B	ISP_REGF_1B	0x10	RW	Data Byte 1B in Batch Operation Mode
P4:0x1C	ISP_REGF_1C	0x10	RW	Data Byte 1C in Batch Operation Mode
P4:0x1D	ISP_REGF_1D	0x10	RW	Data Byte 1D in Batch Operation Mode
P4:0x1E	ISP_REGF_1E	0x10	RW	Data Byte 1E in Batch Operation Mode
P4:0x1F	ISP_REGF_1F	0x10	RW	Data Byte 1F in Batch Operation Mode
P4:0x20	ISP_REGF_20	0x10	RW	Data Byte 20 in Batch Operation Mode
P4:0x21	ISP_REGF_21	0x46	RW	Data Byte 21 in Batch Operation Mode
P4:0x22	ISP_REGF_22	0x46	RW	Data Byte 22 in Batch Operation Mode
P4:0x23	ISP_REGF_23	0x46	RW	Data Byte 23 in Batch Operation Mode
P4:0x24	ISP_REGF_24	0x46	RW	Data Byte 24 in Batch Operation Mode

table 5-24 OTP batch buffer registers (sheet 3 of 3)

address	register name	default value	R/W	description
P4:0x25	ISP_REGF_25	0x0A	RW	Data Byte 25 in Batch Operation Mode
P4:0x26	ISP_REGF_26	0x0A	RW	Data Byte 26 in Batch Operation Mode
P4:0x27	ISP_REGF_27	0x0A	RW	Data Byte 27 in Batch Operation Mode
P4:0x28	ISP_REGF_28	0x0A	RW	Data Byte 28 in Batch Operation Mode
P4:0x29	ISP_REGF_29	0x0A	RW	Data Byte 29 in Batch Operation Mode
P4:0x2A	ISP_REGF_2A	0x0A	RW	Data Byte 2A in Batch Operation Mode
P4:0x2B	ISP_REGF_2B	0x0A	RW	Data Byte 2B in Batch Operation Mode
P4:0x2C	ISP_REGF_2C	0x0A	RW	Data Byte 2C in Batch Operation Mode
P4:0x2D	ISP_REGF_2D	0x0A	RW	Data Byte 2D in Batch Operation Mode
P4:0x2E	ISP_REGF_2E	0x0A	RW	Data Byte 2E in Batch Operation Mode
P4:0x2F	ISP_REGF_2F	0x0A	RW	Data Byte 2F In Batch Operation Mode
P4:0x30	ISP_REGF_30	0x0A	RW	Data Byte 30 in Batch Operation Mode
P4:0x31	ISP_REGF_31	0x32	RW	Data Byte 31 in Batch Operation Mode
P4:0x32	ISP_REGF_32	0x32	RW	Data Byte 32 in Batch Operation Mode
P4:0x33	ISP_REGF_33	0x32	RW	Data Byte 33 in Batch Operation Mode
P4:0x34	ISP_REGF_34	0x32	RW	Data Byte 34 in Batch Operation Mode
P4:0x35	ISP_REGF_35	0x20	RW	Data Byte 35 in Batch Operation Mode
P4:0x36	ISP_REGF_36	0x20	RW	Data Byte 36 in Batch Operation Mode
P4:0x37	ISP_REGF_37	0x20	RW	Data Byte 37 in Batch Operation Mode
P4:0x38	ISP_REGF_38	0x20	RW	Data Byte 38 in Batch Operation Mode
P4:0x39	ISP_REGF_39	0x00	RW	Data Byte 39 in Batch Operation Mode
P4:0x3A	ISP_REGF_3A	0xFF	RW	Data Byte 3A in Batch Operation Mode
P4:0x3B	ISP_REGF_3B	0x1E	RW	Data Byte 3B in Batch Operation Mode
P4:0x3C	ISP_REGF_3C	0x1E	RW	Data Byte 3C in Batch Operation Mode
P4:0x3D	ISP_REGF_3D	0x1E	RW	Data Byte 3D in Batch Operation Mode
P4:0x3E	ISP_REGF_3E	0x1E	RW	Data Byte 3E in Batch Operation Mode
P4:0x3F	ISP_REGF_3F	0x1E	RW	Data Byte 3F in Batch Operation Mode

5.25 mapped registers of OTP cell [P5:0x00 - 0x3F]

table 5-25 mapped registers of OTP cell

address	register name	default value	R/W	description
P5:0x00~ P5:0x3F	DATA_BYT_WR	0x00	RW	Mapped to P5:0x00 Register ~ Mapped to P5:0x3F Register

5.26 page selection [0xFD]

table 5-26 page selection register

address	register name	default value	R/W	description
0xFD	PAGE_FLG_D2	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Page select 000: Page0 001: Page1 010: Page2 100: OTP

6 operating specifications

6.1 absolute maximum ratings

table 6-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6.2 functional temperature

table 6-2 functional temperature

parameter	range
operating temperature (for applications up to 90 fps)[a]	-30°C to +85°C junction temperature
stable image temperature[b]	0°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

6.3 DC characteristics

table 6-3 DC characteristics (-30°C < T_J < 85°C)[a]

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}	supply voltage (digital core)	1.62	1.8	1.98	V
V_{DD-IO}	supply voltage (digital I/O)	1.7 (3.15)	1.8 (3.3)	3.0 (3.45)	V
I_{DD-A}			36.5	45	mA
I_{DD-IO}	active (operating) current[b]		0.13	1	mA
I_{DD-D}			40.8	55	mA
digital inputs (typical conditions: DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[c]	SCL and SDA			0.54	V
V_{IH}[c]	SCL and SDA	1.26			V

a. external clock is stopped during measurement

b. I_{DD} is tested under 30° Celsius in full dark environment with AGC x1 gain

c. based on DOVDD = 1.8V

6.4 timing characteristics

table 6-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (MCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5	ns
	clock input duty cycle	45	50	55	%

7 mechanical specifications

7.1 physical specifications

figure 7-1 package specifications

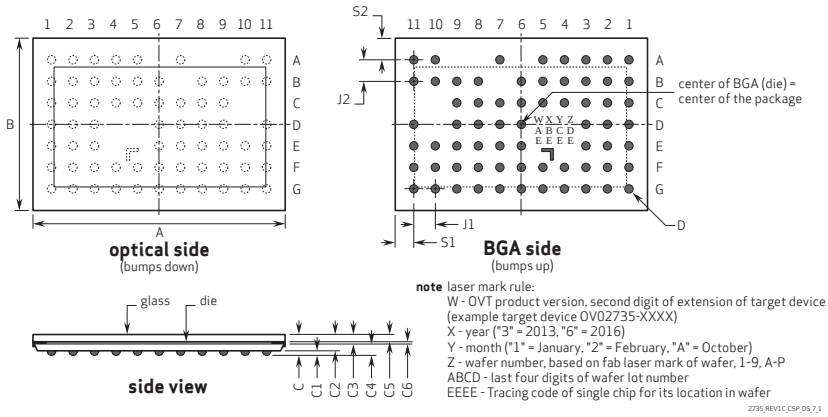


table 7-1 package dimensions

parameter	symbol	min	typ	max	unit
package body dimension x	A	6926	6951	6976	µm
package body dimension y	B	4735	4760	4785	µm
package height	C	671	731	791	µm
ball height	C1	90	120	150	µm
package body thickness	C2	576	611	646	µm
thickness from top glass surface to die	C3	425	445	465	µm
image plane height	C4	241	286	331	µm
glass thickness	C5	385	400	415	µm
air gap between sensor and glass	C6	41	45	49	µm
ball diameter	D	200	230	260	µm
total pin count	N		66 (4 NC)		
pins pitch x-axis	J1		590		µm
pins pitch y-axis	J2		590		µm
edge-to-pin center distance along x	S1	495.5	525.5	555.5	µm
edge-to-pin center distance along y	S2	580	610	640	µm

7.2 IR reflow specifications

note The OV2735 uses a lead-free package.

note To reduce image artifacts from infrared light and to provide the best image quality. OmniVision recommends an IR cut filter.

figure 7-2 IR reflow ramp rate requirements

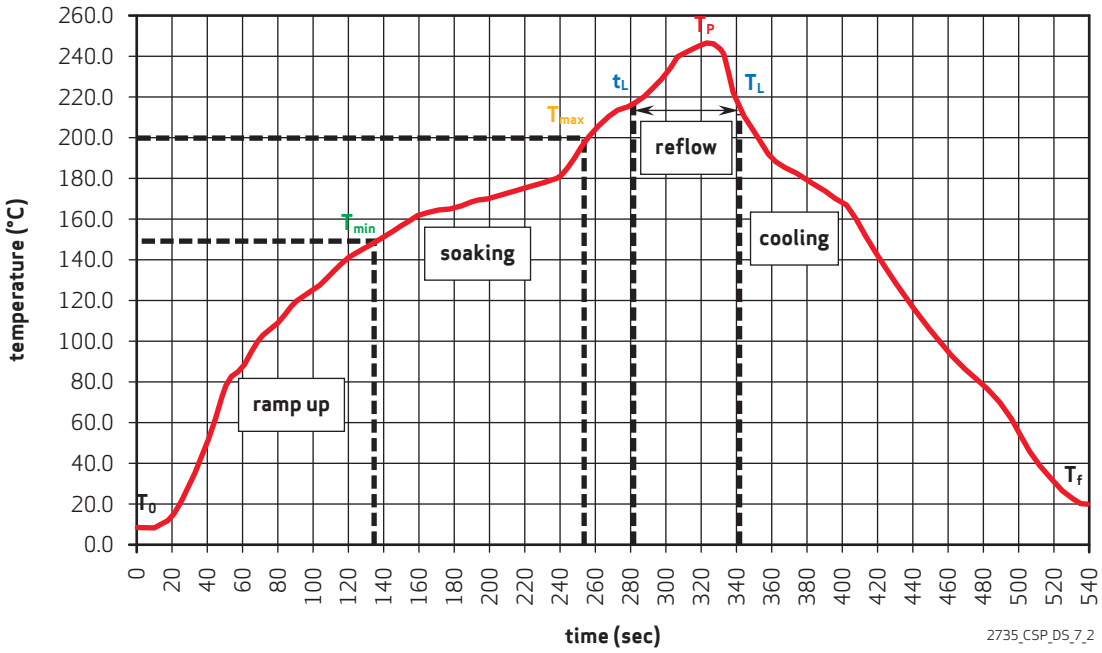


table 7-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_P)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5° (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_P to T_L)	cooling down from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling down from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

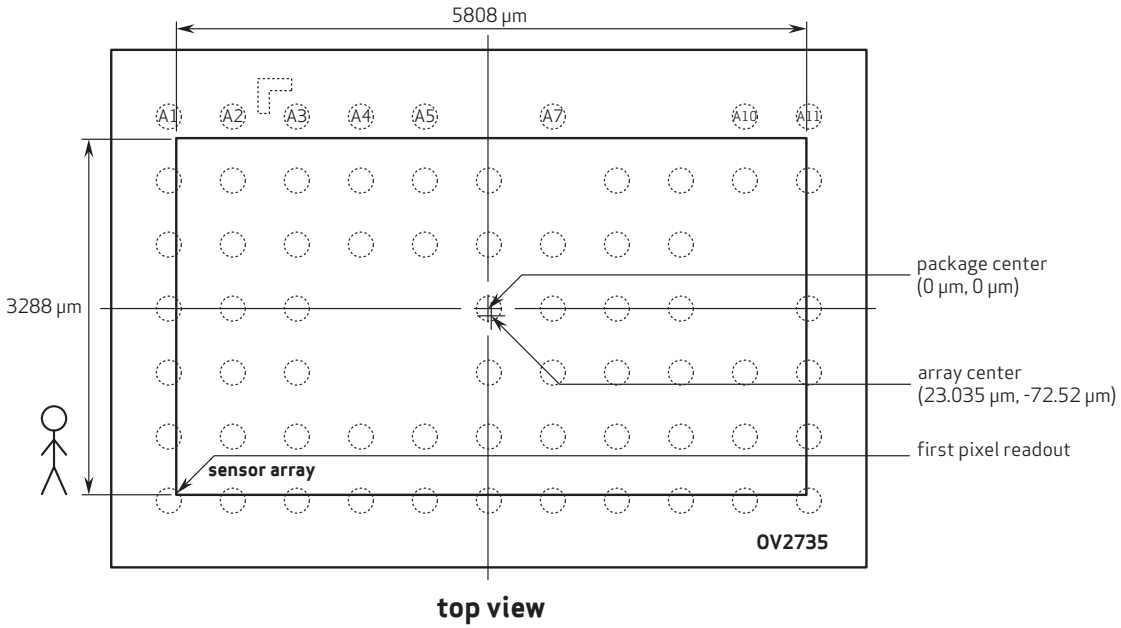
a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM <500 as recommendation

8 optical specifications

8.1 sensor array center

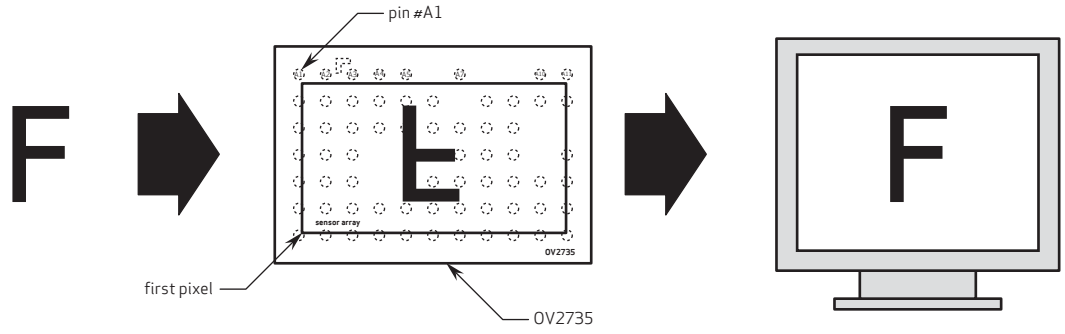
figure 8-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

2735_CSP_DS_8_1

figure 8-2 final image output



0V2735_CSP_DS_8_2

8.2 lens chief ray angle (CRA)

figure 8-3 chief ray angle (CRA)

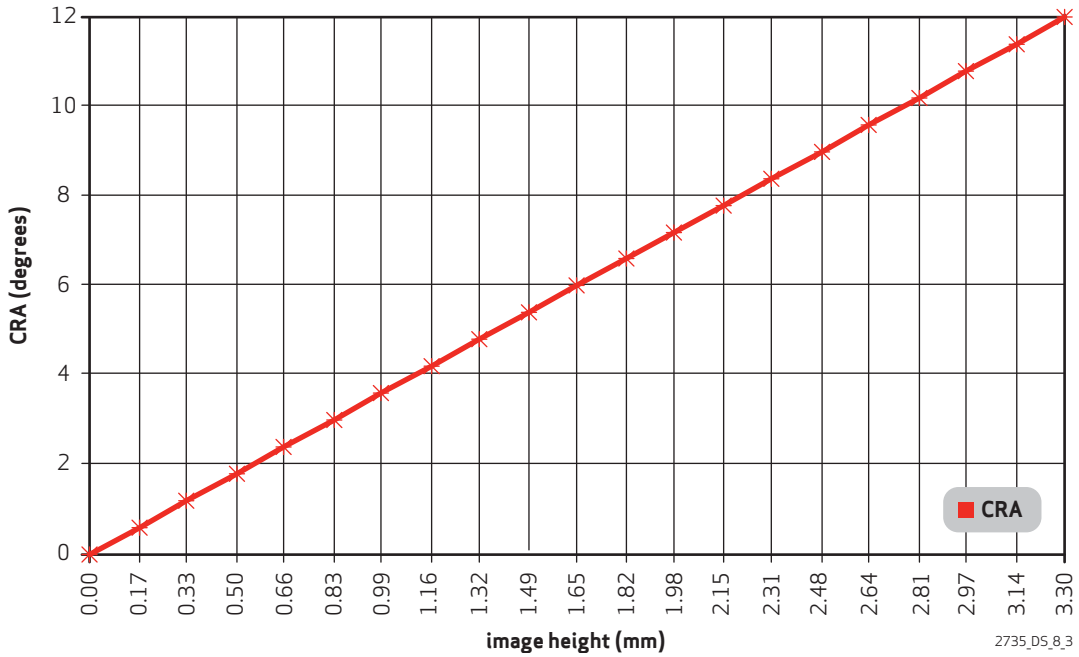


table 8-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0.0	0.00	0.0
0.05	0.17	0.6
0.10	0.33	1.2
0.15	0.50	1.8
0.20	0.66	2.4
0.25	0.83	3.0
0.30	0.99	3.6
0.35	1.16	4.2
0.40	1.32	4.8
0.45	1.49	5.4
0.50	1.65	6.0

table 8-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.55	1.82	6.6
0.60	1.98	7.2
0.65	2.15	7.8
0.70	2.31	8.4
0.75	2.48	9.0
0.80	2.64	9.6
0.85	2.81	10.2
0.90	2.97	10.8
0.95	3.14	11.4
1.00	3.30	12.0

revision history

version 2.0 05.14.2018

- initial release

version 2.01 08.23.2018

- in section 7.1, updated figure 7-1
- in section 8.1, updated figure 8-1 and added new figure 8-2

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