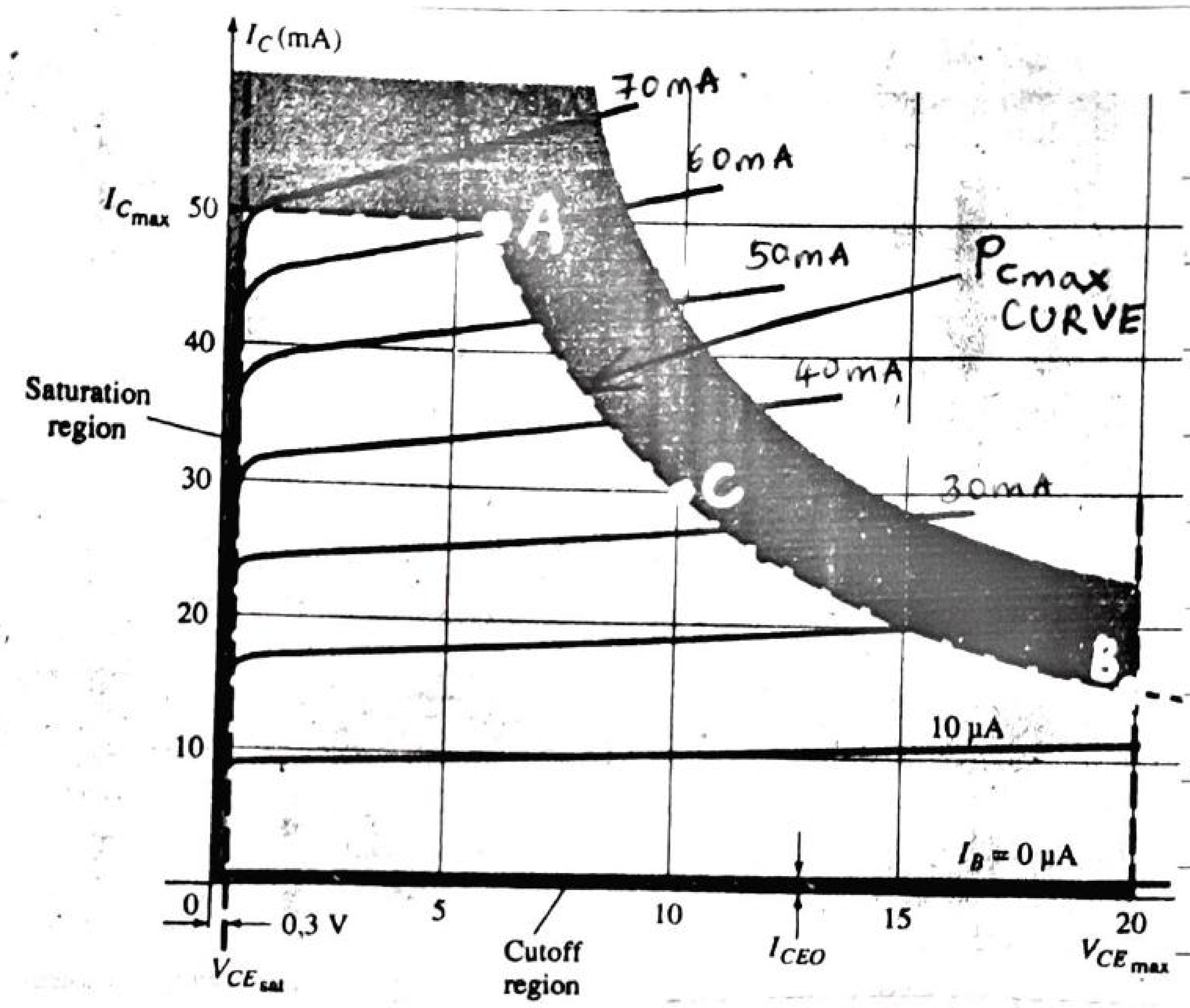
why limits are needed?

LIMITS OF OPERATION

For each transistor, there is a region of operation on the characteristics. Operation in this region will ensure that max. ratings are not being exceeded & the output signal exhibits minimum distortion.



The limits of operation are:

(1) Maximum collector current (I_{Cmax})

(2) Maximum Collector-to-Emitter voltage (V_{CEmax})

(3) V_{CEsat} : It is the minimum V_{CE} that can be applied without the transistor going into the non-linear region (saturation region). It is defined by a vertical line on the characteristics (usually 0.3V).

(4) Cut-off Region: It is defined as the region below $I_C = I_{CEO}$. This region must be avoided if o/p signal is to have minimum distortion.

(5) P_{Cmax} : This is the max power dissipation level given by

$$\boxed{P_{Cmax} = V_{CE} I_C}$$

Note: For CB Configuration $\boxed{P_{Cmax} = V_{CB} I_C}$

Operating in the resulting region of the figure will ensure:

i) Minimum distortion of o/p signal.

ii) Current & voltage levels that will not damage device.

If the characteristic curves are unavailable or are not specified, be sure that I_C, V_{CE} & $(V_{CE} \cdot I_C)$ fall into the following range:

$$\boxed{\begin{array}{c} I_{CEO} \leq I_C \leq I_{Cmax} \\ V_{CEsat} \leq V_{CE} \leq V_{CEmax} \\ V_{CE} I_C \leq P_{Cmax} \end{array}}$$

★★ NOTE → The Power dissipation curve is plotted as follows:-

Suppose $P_{Cmax} = 300mW$.

At any point on the characteristics, the product of V_{CE} and I_C should not exceed 300mW.

If we choose $I_C = 50mA$

$$V_{CE} I_C = 300mW$$

$$\therefore V_{CE} = \frac{300mW}{50mA} = 6V \quad \text{(This is point A)}$$

(See fig.)

If we choose $V_{CE} = 20V$

$$V_{CE} I_C = 300mW$$

$$\therefore I_C = \frac{300mW}{20V} = 15mA \quad \text{(This is point B)}$$

Now say $I_C = 25mA$

$$V_{CE} = \frac{300mW}{25mA} = 12V \quad \text{(This is point C)}$$

$\therefore$ A Rough estimate of the Power dissipation curve can be drawn as shown in the fig.

Problems.

1) For a certain transistor, $I_C = 6.25\ mA$, $I_B = 100\ \mu A$. & collector to base leakage current is $5\ \mu A$. Determine emitter current & α_{dc}.

Soln: $I_C = 6.25\ mA$, $I_B = 100\ \mu A$, $I_{CBO} = 5\ \mu A$.

$$I_E = I_B + I_C = 100\ \mu A + 6.25\ mA = 6.35\ mA.$$

$$I_C = \alpha_{dc} I_E + I_{CBO}.$$

$$\therefore \alpha_{dc} = \frac{I_C - I_{CBO}}{I_E} = 0.9835.$$

2) When emitter current of a transistor is changed by 1 mA, its collector current changes by 0.995 mA. Calculate: (i) its CB short ckt current gain α
(ii) its CE short ckt current gain β.

Soln: $$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E} = \frac{0.995 \times 10^{-3}}{1 \times 10^{-3}} = 0.995$$

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \quad \underline{\underline{OR}} \quad \beta = \frac{\alpha}{1-\alpha} = \frac{0.995}{1-0.995} = 199.$$

3) Determine Emitter Current I_E for a transistor if $I_B = 40\ \mu A$ & $\alpha_{dc} = 0.98$.

Soln: $$I_E = \frac{1}{(1-\alpha_{dc})} I_B.$$ (CC Configuration)

$$= \frac{1}{(1-0.98)} \times 40\ \mu A$$

$$= 2\ mA.$$