SAIL-RISCV Memory Model Refactor

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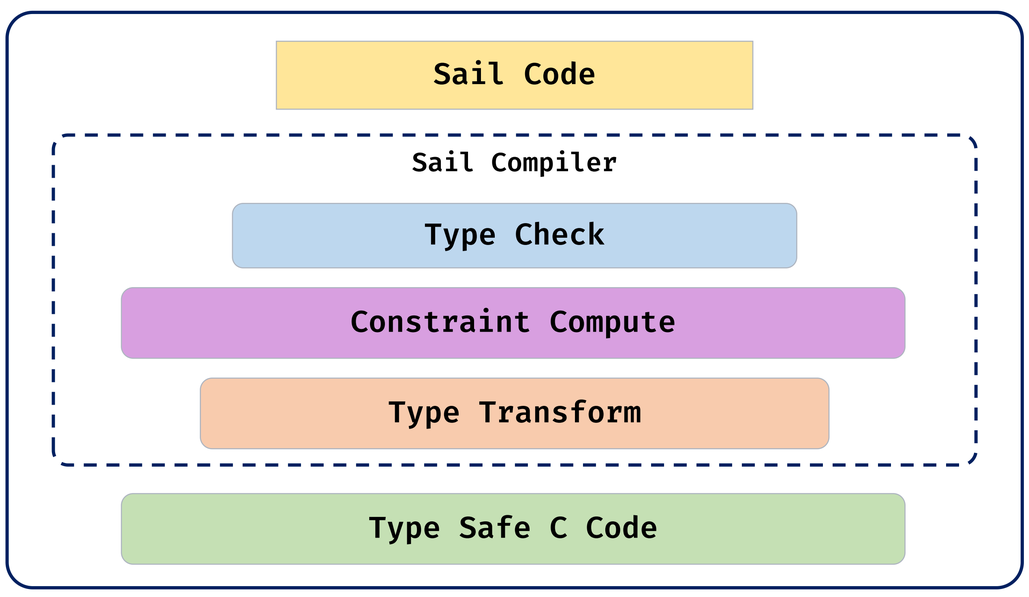
Motivation

- SAIL-RISCV is the golden model for the RISC-V ISA, 34 bit physical address is not supported in RV32 target.
- Sail has a very flexible type system, and dynamic conditional constraint support, but it also bring the ambiguity between physical and virtual memory.
- RISC-V has several virtual memory modes, different modes have different vector fields and different virtual address translation methods, bring implementation inconsistencies



Guarantee Type Safety

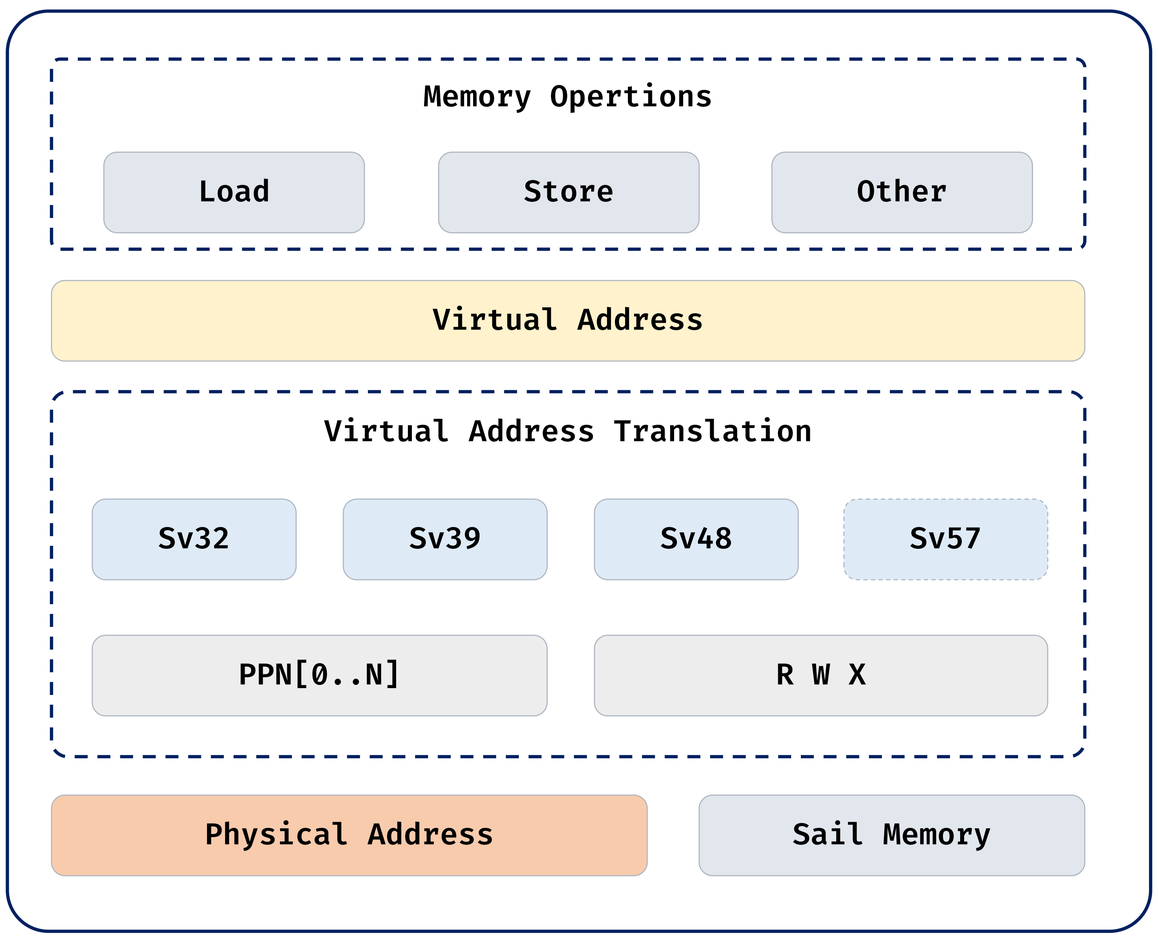
- Using newtype to distinguish physical and virtual memory.
- Refined the communication mechanism with Sail's simulated memory to accommodate arbitrary-width physical addresses, which are then mapped to corresponding Sail memory model addresses.

type safety with newtype

```
<type_def> ::=
  type <id> <typaram> = <typ>
  | type <id> = <typ>
  | type <id> <typaram> -> <kind> = <typ>
  | type <id> : <kind> = <typ>
  | type <id> : <kind>

newtype physaddr = physaddr : xlenbits

enum kind_zphysaddr { Kind_zphysaddr };

struct zphysaddr {
  enum kind_zphysaddr kind;
  union {struct { uint64_t zphysaddr; };};
};
```

Extend Physical Address

- RISC-V has many Virtual Memory Model, and different xlen like RV32, RV64 has different Virtual Memory Model can be used. These Mode
- Different Vitual Memory Model has different satp register defination, and has different addresst translation method, we use sail' flexable type system to unify these operations.
- Enable 34-bit physical address support by allowing arbitrary-width address mappings to Sail supported address types.



Test & Consolution

- Compared to alternative methods, our implementation offers greater flexibility, reducing the coupling risk between physical and virtual memory and providing a more precise memory abstraction for the Sail-RISCV model.
- utilizing newtype constructs ensures compile-time memory type safety.
- Experimental results confirmed our success in resolving type-safety concerns and extending Sail-RISCV's support for 34-bit physical addresses.
- This enhancement, we believe, bolsters the accuracy of Sail-RISCV as a golden model for RISC-V. Future efforts will focus on further enhancing the performance and reliability of Sail-RISCV.