

1. Description

1.1. Project

Project Name	477final
Board Name	NUCLEO-F413ZH
Generated with:	STM32CubeMX 6.0.1
Date	11/23/2020

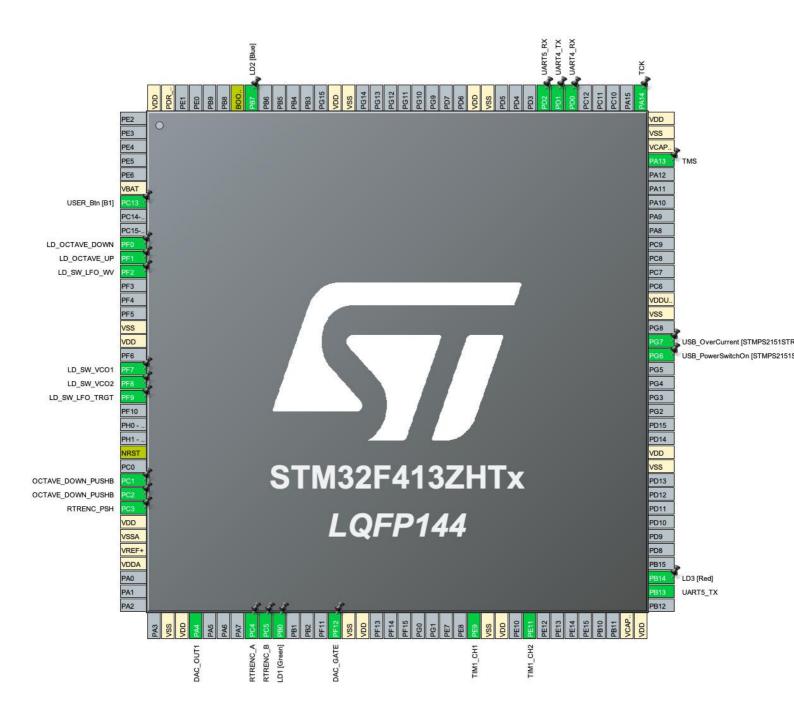
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F413/423
MCU name	STM32F413ZHTx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



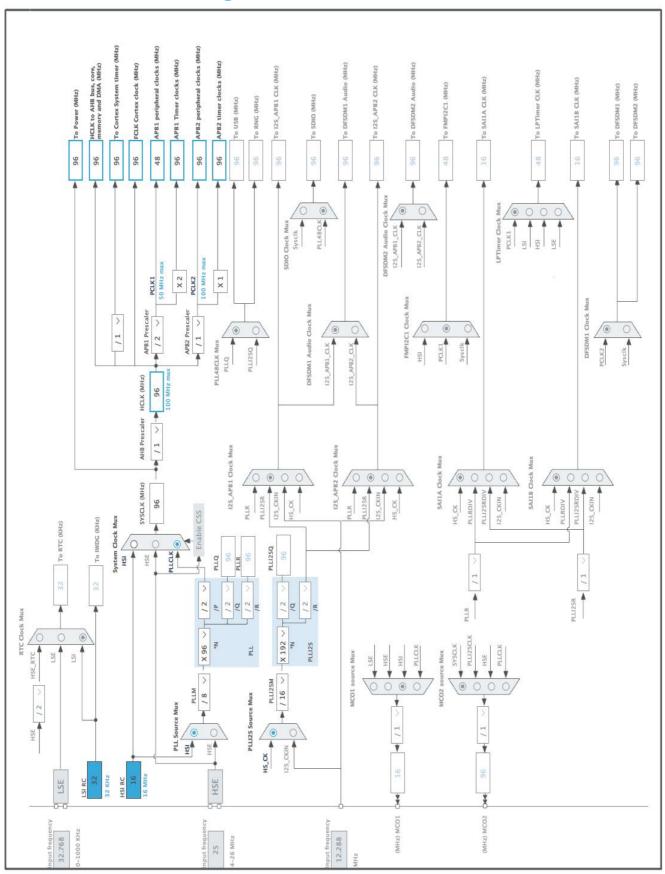
3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
10	PF0 *	I/O	GPIO_Output	LD_OCTAVE_DOWN
11	PF1 *	I/O	GPIO_Output	LD_OCTAVE_UP
12	PF2 *	I/O	GPIO_Output	LD_SW_LFO_WV
16	VSS	Power		
17	VDD	Power		
19	PF7 *	I/O	GPIO_Output	LD_SW_VCO1
20	PF8 *	I/O	GPIO_Output	LD_SW_VCO2
21	PF9 *	I/O	GPIO_Output	LD_SW_LFO_TRGT
25	NRST	Reset		
27	PC1	I/O	GPIO_EXTI1	OCTAVE_DOWN_PUSHB
28	PC2	I/O	GPIO_EXTI2	OCTAVE_DOWN_PUSHB
29	PC3	I/O	GPIO_EXTI3	RTRENC_PSH
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC_OUT1	
44	PC4	I/O	GPIO_EXTI4	RTRENC_A
45	PC5	I/O	GPIO_EXTI5	RTRENC_B
46	PB0 *	I/O	GPIO_Output	LD1 [Green]
50	PF12 *	I/O	GPIO_Output	DAC_GATE
51	VSS	Power		
52	VDD	Power		
60	PE9	I/O	TIM1_CH1	
61	VSS	Power		
62	VDD	Power		
64	PE11	I/O	TIM1_CH2	
71	VCAP_1	Power		
72	VDD	Power		
74	PB13	I/O	UART5_TX	
75	PB14 *	I/O	GPIO_Output	LD3 [Red]
83	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
84	VDD	Power		
91	PG6 *	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7 *	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
94	VSS	Power		
95	VDDUSB	Power		
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
114	PD0	I/O	UART4_RX	
115	PD1	I/O	UART4_TX	
116	PD2	I/O	UART5_RX	
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDD	Power		
137	PB7 *	I/O	GPIO_Output	LD2 [Blue]
138	BOOT0	Boot		
143	PDR_ON	Power		
144	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



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5. Software Project

5.1. Project Settings

Name	Value
Project Name	477final
Project Folder	/Users/rchoyhughes/STM32CubeIDE/workspace_1.4.0/477final
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_UART4_Init	UART4
4	MX_DAC_Init	DAC
5	MX_TIM1_Init	TIM1
6	MX_UART5_Init	UART5

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F413/423
MCU	STM32F413ZHTx
Datasheet	DS11581_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	1.7

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

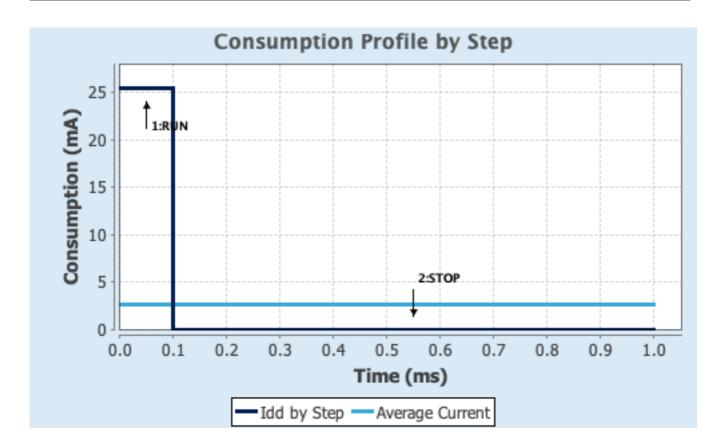
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH/ART/PREFETCH	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash- PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	25.4 mA	15.3 µA
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	103.49	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.55 mA
Battery Life	1 month, 24 days,	Average DMIPS	125.0 DMIPS
	23 hours		

6.6. Chart



7. IPs and Middleware Configuration

7.1. DAC

mode: OUT1 Configuration7.1.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer Enable
Trigger None

7.2. **GPIO**

7.3. RCC

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value 16

TIM Prescaler Selection Disabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.5. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1 Channel2: PWM Generation CH2

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 16 bits value) 65535
Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0
auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)

Disable (Trigger input effect not delayed)

Trigger Event Selection

Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable
BRK Polarity High

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0
Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

7.6. UART4

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate **9600** *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

7.7. UART5

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate 31250 *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive Only *

Over Sampling 16 Samples

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	тск
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PD0	UART4_RX	Alternate Function Push Pull	Pull-up	High *	
	PD1	UART4_TX	Alternate Function Push Pull	Pull-up	High *	
UART5	PB13	UART5_TX	Alternate Function Push Pull	Pull-up	High *	
	PD2	UART5_RX	Alternate Function Push Pull	Pull-up	High *	
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_Btn [B1]
	PF0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD_OCTAVE_DOWN
	PF1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD_OCTAVE_UP
	PF2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD_SW_LFO_WV
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD_SW_VCO1
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD_SW_VCO2
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD_SW_LFO_TRGT
	PC1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	OCTAVE_DOWN_PUSHB
	PC2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	OCTAVE_DOWN_PUSHB
	PC3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	RTRENC_PSH
	PC4	GPIO_EXTI4	External Interrupt Mode with Falling edge trigger detection	Pull-up *	n/a	RTRENC_A
	PC5	GPIO_EXTI5	External Interrupt Mode with Falling edge trigger detection	Pull-up *	n/a	RTRENC_B
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green]
	PF12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Fast *	DAC_GATE
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
	PG7	GPIO_Input	Input mode	Mo pull-up and no pull-down	Speed n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Droopmation Driority	CubDriority	
Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
EXTI line1 interrupt	true	0	0	
EXTI line2 interrupt	true	0	0	
EXTI line3 interrupt	true	0	0	
EXTI line4 interrupt	true	0	0	
EXTI line[9:5] interrupts	true	0	0	
UART5 global interrupt	true	0	0	
PVD interrupt through EXTI line 16	unused			
Flash global interrupt	unused			
RCC global interrupt	unused			
TIM1 break interrupt and TIM9 global interrupt	unused			
TIM1 update interrupt and TIM10 global interrupt	unused			
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused			
TIM1 capture compare interrupt	unused			
EXTI line[15:10] interrupts	unused			
UART4 global interrupt	unused			
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused			
FPU global interrupt		unused		

8.3.2. NVIC Code generation

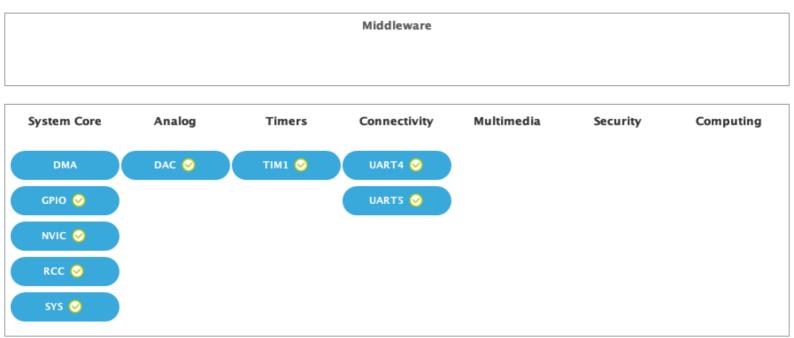
Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Pre-fetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
System service call via SWI instruction	true	true	false
Debug monitor	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true
EXTI line1 interrupt	true	true	true
EXTI line2 interrupt	true	true	true
EXTI line3 interrupt	true	true	true
EXTI line4 interrupt	true	true	true
EXTI line[9:5] interrupts	true	true	true
UART5 global interrupt	true	true	true

^{*} User modified value

9. System Views

- 9.1. Category view
- 9.1.1. Current



10. Docs & Resources

Type Link

Datasheet http://www.st.com/resource/en/datasheet/DM00282249.pdf

Reference http://www.st.com/resource/en/reference_manual/DM00305666.pdf

manual

Programming http://www.st.com/resource/en/programming_manual/DM00046982.pdf

manual

Errata sheet http://www.st.com/resource/en/errata_sheet/DM00318678.pdf

Application note http://www.st.com/resource/en/application_note/CD00167594.pdf

Application note http://www.st.com/resource/en/application_note/CD00211314.pdf

Application note http://www.st.com/resource/en/application_note/CD00249778.pdf

Application note http://www.st.com/resource/en/application_note/CD00259245.pdf

Application note http://www.st.com/resource/en/application_note/CD00264321.pdf

Application note http://www.st.com/resource/en/application_note/CD00264342.pdf

Application note http://www.st.com/resource/en/application_note/CD00264379.pdf

Application note http://www.st.com/resource/en/application_note/DM00024853.pdf

Application note http://www.st.com/resource/en/application_note/DM00040802.pdf

Application note http://www.st.com/resource/en/application_note/DM00040808.pdf

Application note http://www.st.com/resource/en/application_note/DM00042534.pdf

Application note http://www.st.com/resource/en/application_note/DM00046011.pdf

Application note http://www.st.com/resource/en/application_note/DM00072315.pdf

Application note http://www.st.com/resource/en/application_note/DM00073742.pdf

Application note http://www.st.com/resource/en/application_note/DM00073853.pdf

Application note http://www.st.com/resource/en/application_note/DM00080497.pdf

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Application note http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note http://www.st.com/resource/en/application_note/DM00213525.pdf

Application note http://www.st.com/resource/en/application_note/DM00220769.pdf http://www.st.com/resource/en/application_note/DM00227538.pdf Application note Application note http://www.st.com/resource/en/application_note/DM00257177.pdf Application note http://www.st.com/resource/en/application_note/DM00272912.pdf http://www.st.com/resource/en/application_note/DM00226326.pdf Application note http://www.st.com/resource/en/application_note/DM00236305.pdf Application note http://www.st.com/resource/en/application note/DM00281138.pdf Application note Application note http://www.st.com/resource/en/application note/DM00296349.pdf Application note http://www.st.com/resource/en/application note/DM00325582.pdf Application note http://www.st.com/resource/en/application note/DM00327191.pdf Application note http://www.st.com/resource/en/application_note/DM00343623.pdf Application note http://www.st.com/resource/en/application_note/DM00377852.pdf Application note http://www.st.com/resource/en/application_note/DM00354244.pdf Application note http://www.st.com/resource/en/application_note/DM00315319.pdf http://www.st.com/resource/en/application_note/DM00380469.pdf Application note Application note http://www.st.com/resource/en/application_note/DM00354333.pdf Application note http://www.st.com/resource/en/application_note/DM00395696.pdf Application note http://www.st.com/resource/en/application_note/DM00431633.pdf Application note http://www.st.com/resource/en/application_note/DM00493651.pdf Application note http://www.st.com/resource/en/application_note/DM00536349.pdf