ATMX150RHA ASIC Design Manual

Introduction

This design manual presents all the required information and flows to design an ASIC for aerospace applications. It gives you an overview of Microchip-specific and standard commercial tool kits along with design-methodologies for successful space-compliant implementations.

ATMX150RHA is manufactured on a 150 nm, five-metal-layers SOI CMOS with Thick Metal technology option.

Microchip proprietary process, AT77KRHA, is intended for use with a supply voltage of 1.8V for core and 2.5V/3.3V for periphery.

The digital ATMX150RHA QML domain (QML-V, QML-Q, and ESCC QML) includes:

- Up to 22 million of gates, equivalent NAND2
- 3.3V and 2.5V I/Os
- Memory cells compiled (ROM, SRAM, DPRAM, and Register file memory)
- High speed LVDS buffers 655 Mbps
- A PLL (PLL400MRHA)

In addition, out of the QML domain, ATMX150RHA offers additional I/Os and some analog blocks, giving the capability of designing mixed-signal ASICs. The analog blocks have been internally-qualified individually in specific conditions, detailed in the qualification package QP-IP block for ATMX150RHA.

Reference Documents

- RAD ATMX150RHA: *Microchip ATMX150RHA Rad-Hard CMOS 150 nm cell-based ASIC family Radiation Characterization Test Report Total Dose (TID) and Single Event Effects (SEE)*
- QP-ATMX150RHA: *Qualification Package ATMX150RHA*
- QP-IP Blocks for ATMX150RHA: *Qualification Package Specific IP Blocks for ATMX150RHA Mixed-Signal Offer*
- 41059: *Datasheet Rad-Hard 150 nm SOI CMOS Cell-Based ASIC for Space Use*
- 2012_EC_051_ELE: *3V3 I/O Library Databook*
- 2012_EC_052_ELE: *2V5 I/O Library Databook*
- 2012_EC_055: *ELE Supply, ESD and Analog I/O Library Databook*
- 2014_EC_143_ELE: *5V I/O Library Databook*

Advice

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Table of Contents

1. Overview

This section provides details on ATMX150RHA periphery, array, and layout specifities details.

1.1 Periphery

1.1.1 Buffer Description

The peripheral buffer (also called pad) is the electrical interface between the external signals (voltage range from 0V to 2.5V, 0V to 3.3V, or 0V to 5.0V) and the internal core signals (from 0V to 1.8V). Several power supply rails are used inside the chip.

Supply rails naming conventions are as follows:

- VCCB and VSSB are used for buffer external power supply and ground.
- VCC and VSS are used for buffer internal power supply and ground.
- vdd! and gnd! are used for core power supply and ground.

VCCB (VSSB) and VCC (VSS) are isolated from each other while VCC (VSS) is connected to vdd! (gnd!). ATMX150RHA buffer family is also called IO33 family, IO25 family or IO50 family.

The VCCB voltage range differs based on the buffer family as listed in the following:

- IO33: VCCB = 3.3V (3V to 3.6V)
- IO25: VCCB = 2.5V (2.3V to 2.7V)
- IO50: VCCB = 5V (4.5V to 5.5V)

IO25, IO33, and IO50 families contain:

- Bi-directional pads
- Tri-state output pads
- Output only pads
- Input only pads (Inverting, Non-Inverting, and Schmitt Trigger)

Furthermore, the bi-directional, tri-state outputs, and input only pads are available with or without pull-up or pull-down structures.

- Specific pads have been developed for 3.3V and 2.5V:
  - LVDS transmitter and receiver differential pads
  - LVPECL receiver differential pads
- In 3.3V only:
  - 3.3V PCI bi-directional, tri-state output, and output only pads
- Standard pads input level compatibility:
  - IO33: CMOS and LVTTL compatible
  - IO25: CMOS and LVTTL compatible
  - IO50: CMOS and/or TTL compatible

For specific pads (PCI, LVDS, and LVPECL), see the corresponding data sheets.

1.1.2 Tolerance and Cold Sparing Features

I/O buffers are tolerant, which means, that an external voltage higher than VCCB can be applied to the pad when it is in input-mode or high impedance (bi-directional buffers, tri-state buffers in Hi-Z, and LVDS when disable).

I/O buffers are cold sparing, which means, that an external signal can be applied to the pad when VCCB is 0V.

In both the cases, tolerant or cold sparing, there is no impact on core supply, buffer supply, and reliability, if the applied signal respects the recommended operating conditions. In that case, the leakage current is less than 1 µA.

1.1.3 Clusters

The periphery of the chip (pad ring) can be split into several I/O segments (I/O clusters), which can be supplied at different voltages (that is, “n” clusters at 2.5V, “m” clusters at 3.3V, and “p” clusters at 5V). Some clusters can be unpowered while others are active.

A specific power control line (referenced as “porin”-signal) is distributed inside the cluster to be able to force all I/Os of the cluster in tri-state mode whatever their initial state is (that is, an output only buffer is also turned to Hi-Z mode).

This porin-signal can be driven in two ways:

- Cold Sparing mode: Porin is active when VCCB = 0V (case of VCCB power supply pad including a power control feature).
- Hot Swap mode: A specific pad in the cluster is dedicated to power control (pv25p25z, pv33p33z or pv50p50z). When this pad is left open (driven to “0” by an internal pull-down), Porin is activated and thus the I/Os of the device are set into Cold Sparing mode, even if VCCB is supplied.

See

- Buffers Supply Rules
- Power ON/OFF Sequencing

1.1.4 ESD Protection

The introduction of a multiple supply architecture increases the sensitivity to electro-static discharges. In ATMX150RHA periphery, the VCCB and VSSB supplies are isolated from VCC and VSS supplies. Furthermore, when making clusters, the VCCB supply rail is split into several segments.

A solution to improve ESD immunity consists of adding discharge conduction paths between supply rails. To implement this solution, some specific cells must be inserted in the pad ring.

Two kinds of cells are used:

- Back-to-back diodes between VSSB and VSS
- Grounded N-Gates between two VCCB segments

Some ESD cells are “pad count” transparent implemented in the die corners, but other ESD cells must be taken into account in the pad ring definition where each ESD cell has the size of a standard pad.

See

- Power Pads and ESD Cells
- ESD Protection Rules

1.1.5 Pad Site and Pad Pitch

In ATMX150RHA family, the standard pad width and the minimum pad pitch are 95 µm.

For differential pads, the width and the minimum pad pitch are as follows:

- LVDS transmitter: Width = 3 x 95 µm and pitch = 190 µm
- LVDS receiver and LVPECL receiver: Width = 2 x 95 µm and pitch = 95 µm

1.1.6 Pads Naming Conventions

This section details the naming conventions for the pad library elements.

I/O Pads Naming Conventions
I/O pads name segments: 12345678

- 1 = P = Pad
- 2 = Level used for characterization
  - C = CMOS
  - T = TTL
  - E = PECL
  - L = LVDS
  - P = PCI

- 3 = Output signal level
  - 25 = 2.5V
  - 33 = 3.3V
  - 50 = 5.0V
- 4 = Pad function
  - B = Bi-Directional
  - T = Tri-State
  - O = Output
  - D = Input
- 5 = Pad-function-related options
  - 00 = Non-Inverting
  - 10 = Inverting
  - 20 = Schmitt Non-Inverting
  - 30 = Schmitt Inverting
- 6 = Drive-capability
  - 01 = 2 mA
  - 02 = 4 mA
  - 04 = 8 mA
  - 06 = 12 mA
  - 08 = 16 mA
- 7 = Special Type
  - U = Pull-up
  - D = Pull-down
- 8 = Z = Cold sparing

Power Pads Naming Conventions

Power pads name segments: 123456

- 1 and 2 = PV (P is for Pad, V is for Power)
- 3 = External supply level
  - 33 = 3.3V
  - 25 = 2.5V
  - 50 = 5.0V
- 4 = Supply type
  - I = Internal power (supply to core and to pads inner stage)
  - ID = Internal power for double pad ring configuration
  - E = External power (supply to pads outer stage)
  - P = Power control
  - EP = External power + power control
  - F = Feed-through (direct supply or signal to blocks inside core)
- 5 = Applied supply voltage
  - 00 = 0V
  - 18 = 1.8V
  - 33 = 3.3V
  - 25 = 2.5V
- 6 = Z = Cold sparing

1.1.7 Power Pads and ESD Cells

The following table lists the power pads and rails details.

Table 1-1. Power Pads and Supply Rails

Lib Name	Cell Name	Ring Net Continuity							Pad Connection		Type
		iref	vref	porin	VCC	VSS	VCCB	VSSB	Core	Ring	
IO18RHA	btbdcrndez	•	•	•	•	•	•	•	—	—	Corner
	btbdcrndiz	•	•	•	•	•	•	•	—	—	Corner
	btbdcrnz	•	•	•	•	•	•	•	—	—	Corner
	btbdn18ez	•	•		•	•		•	—	—	Cluster delimiter
	btbdz	•	•	•	•	•	•	•	—	—	Filler
	pv18ft	•	•	•	•	•	•	•	cinout	—	Isolated cell supply
	pv18id00z	—	—	—	—	—	—	—	gnd!	—	Inner ring core supply
	pv18id18z								vdd!	—	Inner ring core supply
IO33RHA IO25RHA same as IO33RHA	btbdn33ez				•	•		•	—	—	Cluster delimiter
	pv33e00z	•	•	•	•	•	•	•	—	VSSB	Supply
	pv33e33z	•	•	•	•	•	•	•	—	VCCB	Supply
	pv33ebtbcrndez	•	•	•	•	•	•	•	—	VCCB/ VSSB	Corner/Supply
	pv33ebtbcrnz	•	•	•	•	•	•	•	—	VCCB/ VSSB	Corner/Supply
	pv33ep33z	•	•	•	•	•	•	•	—	VCCB	Supply with power control for Cold-sparing mode
	pv33f00z	•	•	•	•	•	•	•	VSSBC3V3	VSSB	Supply
	pv33f33z	•	•	•	•	•	•	•	VCCBC3V3	VCCB	Supply
	pv33ft	•	•	•	•	•	•	•	cinout	—	Isolated cell supply
	pv33i00z	•	•	•	•	•	•	•	gnd!	VSS	Supply
	pv33i18z	•	•	•	•	•	•	•	vdd!	VCC	Supply
	pv33id00z	•	•	•	•	•	•	•	gnd!	VSS	Supply
	pv33id18z	•	•	•	•	•	•	•	vdd!	VCC	Supply
	pv33p33z	•	•	•	•	•	•	•	—	—	Cluster power control for hot-swap mode

.....continued

Lib Name	Cell Name	Ring Net Continuity							Pad Connection		Type
		iref	vref	porin	VCC	VSS	VCCB	VSSB	Core	Ring	
IO50RHA	pv50e00z	•	•	•	•	•	•	•	gnd!	VSSB/VSS	Supply
	pv50ep50z	•	•	•	•	•	•	•	—	VCCB	Supply with power control for Cold-sparing mode
	pv50f00z	•	•	•	•	•	•	•	VSSBC5V	VSSB	Supply
	pv50f50z	•	•	•	•	•	•	•	VCCBC5V	VCCB	Supply
	pv50fp50z	•	•	•	•	•	•	•	VCCBC5V	VCCB	Supply with power control for Cold-sparing mode
	pv50ft	•	•	•	•	•	•	•	cinout5v	—	Isolated cell supply
	pv50i00z	•	•	•	•	•	•	•	gnd!	VSS	Supply
	pv50i18z	•	•	•	•	•	•	•	vdd!	VCC	Supply

Notes:

- All cells can be found in 2012_EC_055_ELE: ATMX150RHA SUPPLY ESD AND ANALOG I/O DATABOOK.
- pv33i00z and pv33i18z are used to supply core inside IO33 buffer clusters.
- pv33e00z and pv33e33z are used to supply buffer IO33.
- pv33p33z are used to control buffer tolerance independently of VCCB (see Clusters: Hot Swap Mode).
- pv33ep33z combines VCCB and power control (see Clusters: Cold Sparing Mode).
- pv33ebtbcrnz (see Corner Pads).
- pv33f00z, pv50f00z, pv33f33z, and pv50f50z (with ESD protection as described in chapter ESD Protection), are used to supply digital or analog blocks inside the core.
- pvxxft (xx = 18, 33, or 50 for 1.8V, 3.3V, or 5.0V) are dedicated pads (with ESD protection as described in chapter ESD Protection) to supply IP-blocks (For example, BG).

Double Pad Ring

In the double pad ring configuration, all core power supply pads must be placed exclusively in the inner ring. Only supply-buffers of type PV18IDxxZ are allowed.

The number of pads on the inner ring is tailored to the actual need of each design. These core supplies are automatically routed to the inner ring. As long as the inner ring is exclusively used for core supply pads, the designs achieve space quality levels. However, the resulting total number of pads on the inner ring must not go above the maximum number given in the table 1.10 for double pad ring in paragraph 1.4.

ESD Cells

Each I/O or Power pad includes its own ESD protection structure (usually snapback based, versus VCCB and VSSB) but other structures are added to improve overall ESD protection:

- BTBDZ: Back to back diodes between VSSB and VSS.
- BTBDN33Z: Back to back diodes between VSSB and VSS + Grounded N-gates between two adjacent VCCB rails. BTBDN33EZ must be used, if at least one adjacent segment is IO33.

Corner Pads

To take advantage of the room available in die corners, the following pads are added:

- BTBDCRNZ: Same ESD cells as BTBDZ but placed in corner
- PV33EBTBCRNZ: PV33E33Z + PV33E00Z + BTBDZ

The bonding feasibility of an extra VCCB and VSSB supply pair must be checked on a case by case basis.

Feedthrough Pad
ATMX150RHA offers the possibility to isolate by deep trench some part of the circuit. To supply these functions, the PVxxFT pad must be used.

Ensure that in this case, PVxxFT used for supplies must be placed in a cluster supplied by other pads to enable the ESD protections implemented in the PVxxFT pads.

ESD Protection Rules
With a continuous VSSB rail, at least one back to back diode structure must be used per die side (If used, the corner structure is enough). Contact the technical center that supports your area to check on the ESD Protection Rules.

Each time the VCCB rail is cut a grounded N-gate must be inserted between the two VCCB segments.

PVxxFT does not cut the peripheral power rails, so no additional ESD structure is needed.

1.1.8 Standard Pads

The following table lists the standard pad names and its related details.

Table 1-2. Standard ATMX150RHA Pad Names (xx Among 01, 02, 04, 06, and 08)

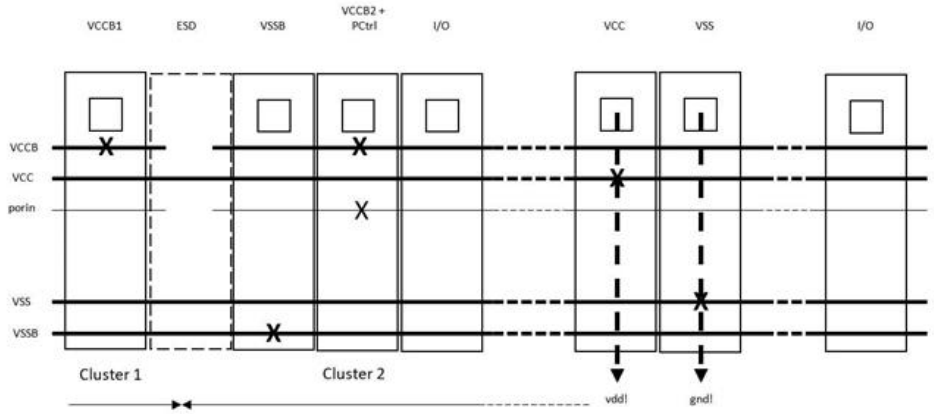
Buffer Type		IO25	IO33	IO50
Bidirectional	I/O	pt25bxxz	pt33bxxz	—
	I/O with Pull-Down	pt25bxxdz	pt33bxxdz	pt50b02dz
	I/O with Pull-Up	pt25bxxuz	pt33bxxuz	pt50b02uz
Tri-state Output	3-state O	pt25txxz	pt33txxz	pc50t04z
	3-state O with Pull-Down	pt25txxdz	pt33txxdz	—
	3-state O with Pull-Up	pt25txxuz	pt33txxuz	—
Output Only	—	pt25oxxz	pt33oxxz	pc50o04z
Non Inverting Input	—	pc25d00z	pc33d00z	pc50d00dz
	I with Pull-Down	pc25d00dz	pc33d00dz	pc50d00uz
	I with Pull-Up	pc25d00uz	pc33d00uz	—
Inverting Input	—	pc25d10z	pc33d10z	pc50d10z
	I with Pull-Down	pc25d10dz	pc33d10dz	—
	I with Pull-Up	pc25d10uz	pc33d10uz	—
Schmitt Non Inverting Input	—	pc25d20z	pc33d20z	—
	I with Pull-Down	pc25d20dz	pc33d20dz	pc50d20dz
	I with Pull-Up	pc25d20uz	pc33d20uz	pc50d20uz
Schmitt Inverting Input	—	pc25d30z	pc33d30z	pc50d30z
	I with Pull-Down	pc25d30dz	pc33d30dz	—
	I with Pull-Up	pc25d30uz	pc33d30uz	—

Note: No mixed power supply for 2.5V, 3.3V is authorized within one cluster.

Clusters

The following figure shows a cluster configuration example.

Figure 1-1. A Standard I/O-Cluster Configuration Example



- VCCB1: PV33E33Z
- ESD: BTBDN33EZ
- VSSB: PV33E00Z
- VCCB2 + Pctrl: PV33EP33Z (Cold Sparing mode)
- I/O: PT33... or PC33...
- VCC: PV33I18Z (Core 1.8V supply inside IO33 cluster)
- VSS: PV33I00Z (Core 0V ground inside IO33 cluster)

Remarks:

- VCC, VSS, and VSSB are continuous rail along with the I/O ring.
- VCCB rail and porin (Power Control line) are cut at each cluster end (One cluster can be active while another one can be powered OFF).
- VCC and VSS pads are used for both the core supplies (vdd! and gnd!) and I/O buffers core side (VCC and VSS).
- The power-on-reset-line in the buffer area is driven by VCCB-buffers with power control. To avoid noise on the power-on-reset line, these must not be placed at long distance from each other (For example, alternate 3 PVxxExxZ, 1 PVxxEPxxZ, 3 PVxxExxZ, and so on). In that case, all the power control sources belonging to one cluster are connected in parallel to a single porin line. If PVxxPxxZ are used instead of PVxxEPxxZ (Hot Swap mode), all the PVxxPxxZ must be connected together externally. Each power control source draws ~ 7.5 µA from VCCB. The correct implementation is checked by the Microchip design center.
- The pad's position inside the cluster is not predefined. It is a good practice to group supplies in pairs. The number of VCCB and VSSB pairs inside a cluster depends on I/O drive strength, frequency, and load. The number of VCC and VSS pairs is defined by Core Power consumption, and a good practice is to have uniform VCC and VSS pair distribution all around the die.

See

- Buffer Supply Rules

1.1.9 PCI Buffers

The PCI buffers are based on the 3.3V PCI standards where inputs are required to be clamped to both ground and VCCB (3.3V) rails. To be also Cold Sparing, these buffers are:

- Cold sparing when VCCB = 0V (clamped to VSSB only)
- Clamped to VCCB and VSSB when VCCB = 3.3V

The PCI family includes three buffer types:

- PP33B01Z: Bi-directional
- PP33T01Z: 3-State output

- PP33O01Z: Output only

The PCI drive strength is almost equivalent to the standard IO33 drive 08. The main differences are:

- Non-tolerance
- Input trigger levels, which are slightly lower (V_{IH} min = 0.5 VCCB)

1.1.10 LVDS Buffers

The LVDS family is based on the ANSI/TIA/EIA-644 standards. It is composed of:

- A voltage/current reference (PL33REFZ/PL25REFZ).
- A transmitter buffer (PL33TXZ/PL25TXZ) with Outp and Outn differential outputs.
- A receiver buffer (PL33RXZ/PL25RXZ) with Inp and Inn differential inputs.
- A receiver buffer including 100Ω termination (PL33RXRZ/PL25RXRZ) with Inp and Inn differential inputs.

When the pads of the above mentioned types are not used and not power supplied (VCCB = 0V), they are Cold Sparing. When the pads of type PL33RXZ, PL25RXZ, PL33RXRZ, PL25RXRZ, PL33TXZ, and PL25TXZ are not used and disabled (ien = 1 or eon = 1), they are tolerant (voltage up to supply-voltage-level can be applied on the pads without damage).

To use the PL33RXZ, PL25RXZ, PL33RXRZ, PL25RXRZ, PL33TXZ, and PL25TXZ pads, do enable them with ien = 0 or eon = 0.

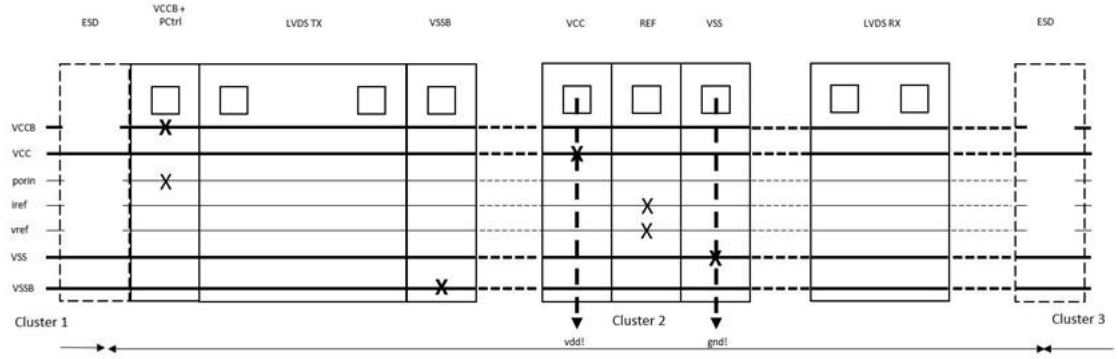
The LVDS standard transmission levels are ±350 mV differential around 1.25V common mode. As these levels are tight to achieve in military temperature range, the PL33REFZ/PL25REFZ pads provide two references to the other LVDS pads of the same cluster:

- The external ref voltage, which is used by transmitter only to force the common mode voltage (Vref)
- A current reference, which is used by both transmitter and receiver (Iref)

LVDS Cluster

The following figure shows an LVDS buffer example.

Figure 1-2. An LVDS Cluster Example



LVDS Cluster is at 3.3V or 2.5V:

- ESD: BTBDN33EZ
- VCCB + Pctrl: PV33EP33Z (Cold Sparing mode)
- LVDS TX: PL33TXZ/PL25TXZ
- VSSB: PV33E00Z
- VCC: PV33I18Z (Core 1.8V supply inside IO33 cluster)
- LVDS REF: PL33REFZ/PL25REFZ
- VSS: PV33I00Z (Core 0V ground inside IO33 cluster)
- LVDS Rx: PL33RXZ/PL25RXZ

Notes:

- Same VCCB + Pctrl, VSSB, VCC, and VSS pad types as for standard IO33-pads are used.
- The two additional signals (iref and vref) are generated by the REF-buffer.

Important: It is not allowed to use more than 1 REF per cluster.

- A single REF can be used for several LVDS TX and RX. To limit the distance from REF to the far end of the cluster, the maximum cluster width is 16 LVDS differential elements (TX or RX) and the best place for the REF pad is at the center of the cluster.
- It is better to distribute all the necessary VCCB, VSSB, VCC, and VSS pins to make shields around the different LVDS differential pairs and around the REF pad.
- The LVDS TX takes the place of three standard I/O pads and the LVDS RX takes the room of two.
- To avoid noise issues, it is not allowed to mix LVDS and Standard-IO buffers.

See

- Buffer Supply Rules

1.1.11 LVPECL Buffer

The PE33RXZ/PE25RXZ PECL buffer is a simplified version of the PL33RXZ/PL25RXZ LVDS buffer. It is a differential input with the LVPECL levels, and it does not need ref. Therefore, it can be implemented inside a standard IO33 cluster.

The PECL RX occupies two standard I/O places.

1.1.12 Power ON/OFF Sequence

In a multiple power supply application, the discrepancy between the various supply rise/fall times may induce high currents through the ESD protection clamping diodes during Power ON/OFF sequences. This applies to the different core- and IO-voltage as well as separate supply-voltage for analog IPs or dedicated parts of the digital logic.

To avoid damage or problems because of high currents, an Application-note “Power-supply sequencing for Aerospace ASIC” describes the correct order of switching on and off the different power-supplies.

1.2 Analog Blocks

The analog IPs are internally qualified and are delivered with a datasheet and qualpack.

The following checks are done to get the analog IPs internally qualified:

- Electrical characterization
- TID and SEE characterization
- HTOL proven

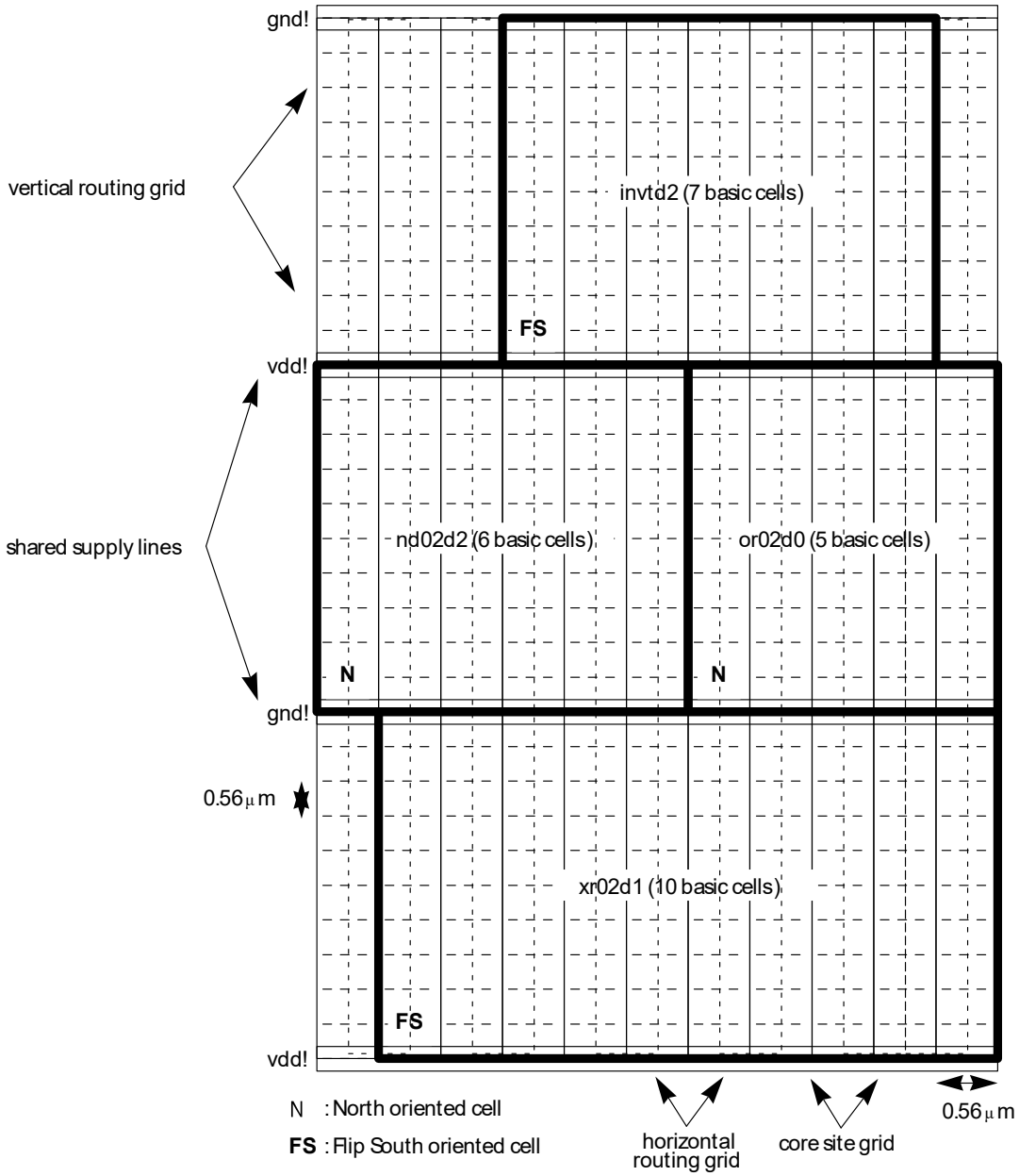
The analog IPs consist of voltage regulators, a voltage reference and monitoring device, clock synthetiser, and signal conditioning IPs. For more details and a complete list of available analog blocks, contact the technical center that provides support in your area.

1.3 Core

1.3.1 Core Array and Cells

The following figure shows the core array and cell layout core supply rails.

Figure 1-3. Core Array and Cell Layout Core Supply Rails



All cells of the ATMX150RHA library are a multiple of a basic core cell, covering 1 vertical track (metal 2/4) and 10 horizontal tracks (metal 1/3). There are two metal1 supply lines (gnd! and vdd!) per cell, which are alternately shared by rows of cells as shown in the preceding figure.

Two core rings surround the core. There are no strict rules, but they may be routed in the following layers:

- gnd! ring in metal5
- vdd! ring in CIND

Both the rings are superposed.

1.3.2 Supply Lines Over the Core

Besides internal metal1 lines (as shown in Figure 1-3), gnd! and vdd! stripe lines are regularly routed all over the core to ensure a good distribution of consumption current and to avoid noise (due to IR drop) and electro-migration problems:

- gnd! stripe lines are often routed horizontally in metal5 and vertically in CIND.
- vdd! stripe lines are often routed horizontally in metal5 and vertically in CIND.

1.3.3 Memory Hard Blocks

The ATMX150RHA memory libraries are developed from the Virage memory compilers. All these memories are synchronous. This section provides the description of the single-port synchronous SRAM, the dual-port (2RW) synchronous SRAM, and the two-port (1W, 1R) synchronous register-file.

The memory cells are designed to work in the following voltage range:

- VDD = 1.8V ±0.15V

The ATMX150RHA memory library has been characterized and validated in the following temperature range:

- T = -55 ℃ to 145 ℃

Multiple-Bit Upset (MBU) and Multiple-Cell Upset (MCU)

Multiple upsets occur when several bit-flips are triggered by a single particle. Several upsets in a memory word are called MBUs, whereas several upsets in different memory words are referenced as MCUs.

Integrated circuits tend to be increasingly sensitive to multiple upset events as gaps between transistors are becoming smaller. This allows charges deposited by ions and protons to be collected by several sensitive nodes of the circuit and thus results in SEUs in different memory cells.

Error-Correcting Codes (ECCs), such as Hamming codes, are well adapted to mitigate SEUs as they can detect and correct errors in a word. However, MBUs are a real challenge for advanced technologies as they require elaborated and complex ECCs.

The following figures show the MBU and MCU details.

Figure 1-4. Two Upsets in the Same Word Provoked by a Single Particle (MBU)

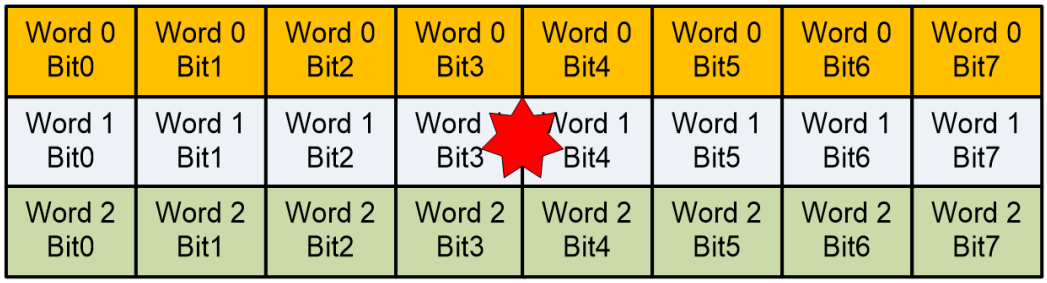
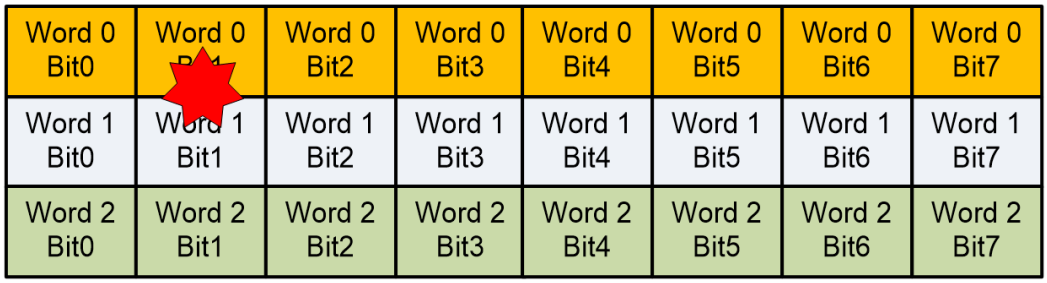


Figure 1-5. Two Upsets in Different Words Provoked by a Single Particle (MCU)



Memories' layout and bitmap depend upon three main parameters:

- The number of address bits (giving the number of words)
- The word size (number of bits per word)
- The column multiplexer option (called CM in the document)

All of these parameters have a direct effect on the shape of the generated memory and are correlated (non-independent). This interdependence is summarized in the dedicated block diagram (see Figure 1-8 , Figure 1-12, and Figure 1-16).

Bitmap

The memories generated by the ATMX150RHA compiler have an internal organization (physical topology) that is different from the logical word/addressing scheme visible by the higher-level specification.

As the approach used for SEU testing of those resources is an algorithm that could retrieve several errors (related or not) in the same test cycle, it is crucial to differentiate true MBUs (that is, induced by a single particle) from several SEUs induced by many particles.

Therefore, for the accurate analysis of MBUs, it is mandatory to perform a logic to physical mapping (descrambling or bit-mapping) of the address/bit position data. This mapping is the same for all the memories generated by the ATMX150RHA compiler.

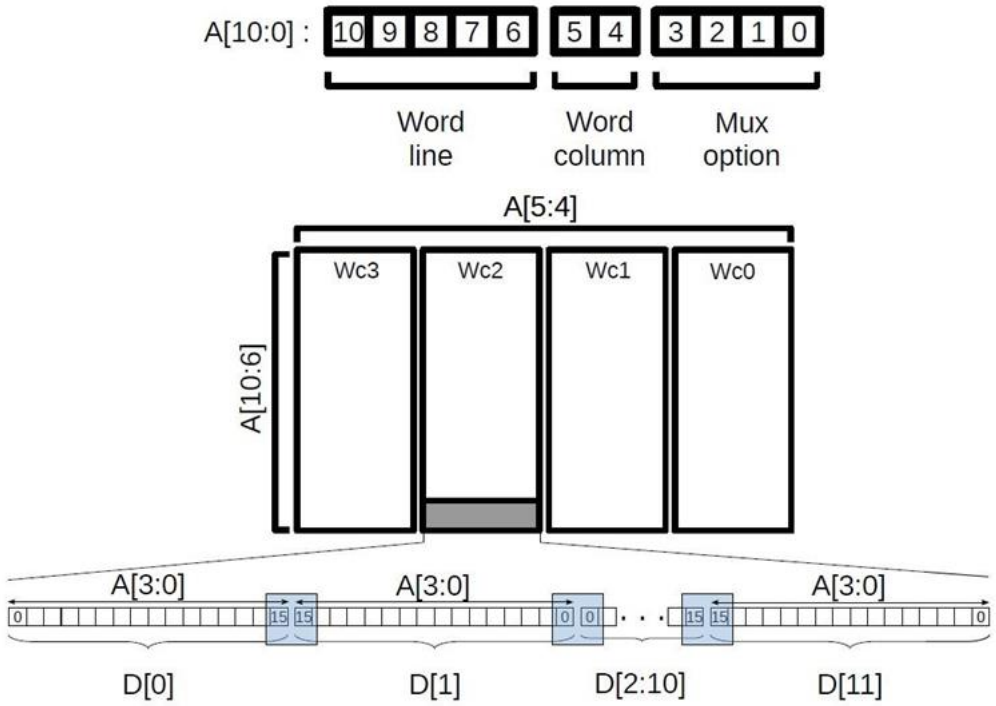
As bitmap example, a single port SRAM (hdss1_2048x12cm16sw0ab) organized into 2048 words of 12 bits (that is, 2Kx12) with a column multiplexer option of 16.

The address (11 bits in our example) is made of three fields:

- The word line bits (MSB): Bits 10 to 4 in our example.
- The word column bits (always equal to 2 whatever the column multiplexing option is): Bits 5 and 4 in our example.
- The column multiplexing option bits (LSB): Bits 3 to 0 in our example.

The following figure shows the memory layout and address bits splitting.

Figure 1-6. Memory Layout/Address-Bits Splitting



It can be seen that when A[3:0] = 0, bits D[1]/D[2], D[3]/D[4], D[5]/D[6], D[7]/D[8], and D[9]/D[10] are physically adjacent and are sensitive to MBU. The same configuration applies when A[3:0] = 15 for bits D[0]/D[1], D[2]/D[3], D[4]/D[5], D[6]/D[7], D[8]/D[9], and D[10]/D[11].

For other values of A[3:0], bits within a same word are not physically adjacent and consequently can be considered as not sensitive to MBU.

For any type of memory, the ratio of adjacent bits (relative to total number of bits in memory) is equal to (n = number of bits per word, cm = column multiplexing option):

$$R = \frac{2(n-1)}{n \square m}$$

In this example, R = 11.46%.

Conclusion

Some memories generated by the ATMX150RHA memory compiler (DPRAM or SPRAM) exhibit physically adjacent bits within some words. These bits may be sensitive to MBU.

The ratio of these bits (relative to the total number of bits) is provided in the paragraph above and is mainly dependent upon the column multiplexing factor.

To minimize the global MBU sensitivity of a memory, you must generate it with the highest possible column multiplexing factor.

1.3.3.1 Single-Port Synchronous SRAM

Separated output and input pins allow a write through cycle. An asynchronous write through mode (AWT) allows testing of interface shadow logic through scan. You can choose the output as a 3-state or always active. In case, the 3-state option is selected (application with several memories driving the same bus), you must ensure to avoid contention-problems as well as floating states. The BIST interface is optional but strongly recommended. The special test modes allow externally bypassing read and write self-timed. You have the flexibility in specifying the logical size of the SRAM, including both the word size and the number of address locations, the column mux, and the output enable option. This memory includes an optional sub-word feature providing write to each group of 2, 4 or 8 bit sub-words. A maskable write enable signal (WEM) serves each sub-word.

The following figures show the SRAM block diagram and address-, word-, and bit-size ranges.

Figure 1-7. SRAM Block Diagram

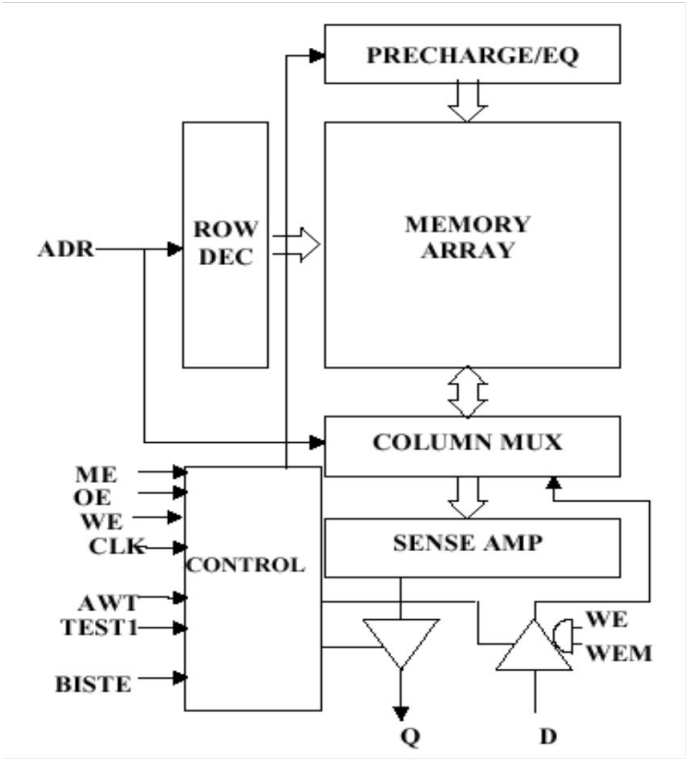
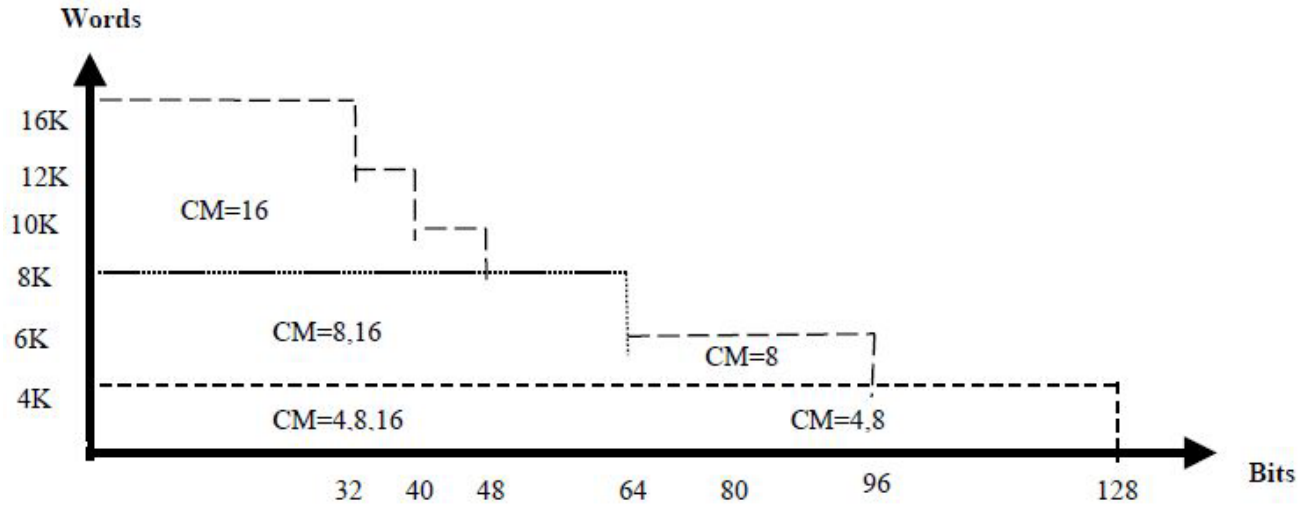


Figure 1-8. SRAM Address-, Word-, and Bit-Size Ranges



Microchip recommendations:

- To minimize multiple upsets per word, it is recommended to use the largest possible column mux (CM = 16).
- To bypass the memories during scan, it is recommended to use AWT.

Note: Even if AWT and BIST are not requested during memory generation, the mux logic is inserted by the compiler; the AWT and the BIST signals are tied to 0 in that case.

Table 1-3. SRAM Size Limits

	Minimum	Maximum	Increment
Address inputs	4	14	1
Address (words)	16	16384	1 x CM [1]
Word size (number of I/O bits)	2	128	1
Total bits in a core	32	512K	—

1. CM = 4, 8, and 16

The following figures show the read- and write-cycle timing of SRAM.

Figure 1-9. SRAM Read-Cycle Timing

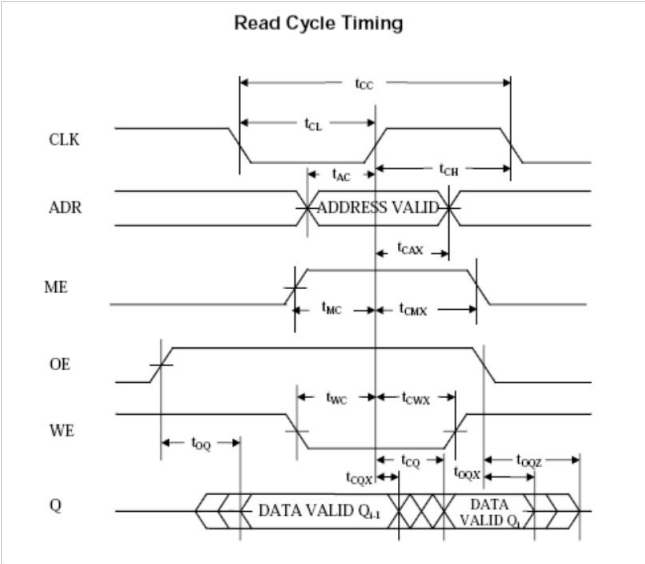
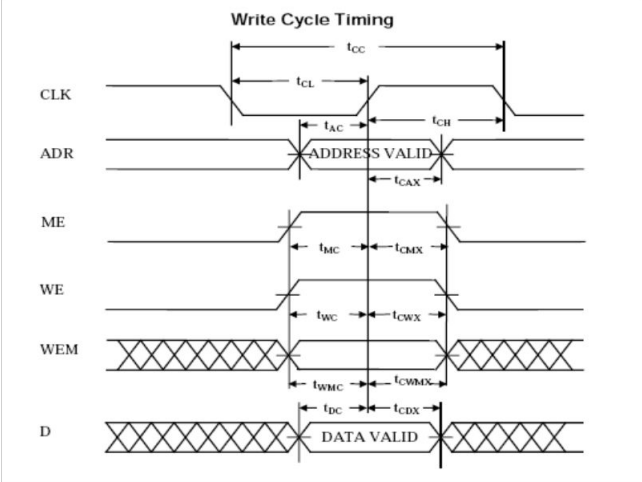


Figure 1-10. SRAM Write-Cycle Timing



The following table lists the SRAM 16kx8 timing specification.

Table 1-4. SRAM 16kx8 Timing Specification

Symbol	Parameter	Slow 145 1.60V	Fast -55 2.0V
TCC	Clock cycle time	9.2	—
TCL	Clock low cycle width	1.0	—
TCH	Clock high cycle width	1.0	—
TCQ	Clock to data out delay	9.1	—
TOQ	Output enable time	0.80	—
TAC	Address set up time before clock	0.60	—
TCAX	Address hold time before clock	—	0

.....continued			
Symbol	**Parameter**	**Slow 145 1.60V**	**Fast -55 2.0V**
TDC	Data set up time before clock	0.40	—
TCDX	Data hold time after clock	—	0
TMC	Memory enable set up time before clock	0.50	—
TCMX	Memory enable hold time after clock	—	0
TWC	Write enable set up time before clock	0.40	—
TCWX	Write enable hold time after clock	—	0
TDQ	Data in to data out delay when AWT = 1	1.40	—
TAWQ	AWT to data out delay	1.50	—

1.3.3.2 Dual-Port Synchronous SRAM

Separated output and input pins allow a write through a cycle. An asynchronous write through mode (AWT) allows testing of interface shadow logic through scan. You can choose the output as a 3-state or always active. In case, the 3-state option is selected (application with several memories driving the same bus), you must ensure to avoid contention-problems as well as floating states. The BIST interface is optional but strongly recommended. The special test modes allow externally bypassing read and write self-timed. You have the flexibility in specifying the logical size of the DPRAM, including both the word size and the number of address locations, the column mux, and the output enable option. This memory includes an optional sub-word feature providing write to each group of 2, 4 or 8 bit sub-words. A maskable write enable signal (WEMA/WEMB) serves each sub-word.

The following figures show dual-port SRAM block diagram and address-, word-, and bit-size ranges.

Figure 1-11. Dual-Port SRAM Block Diagram

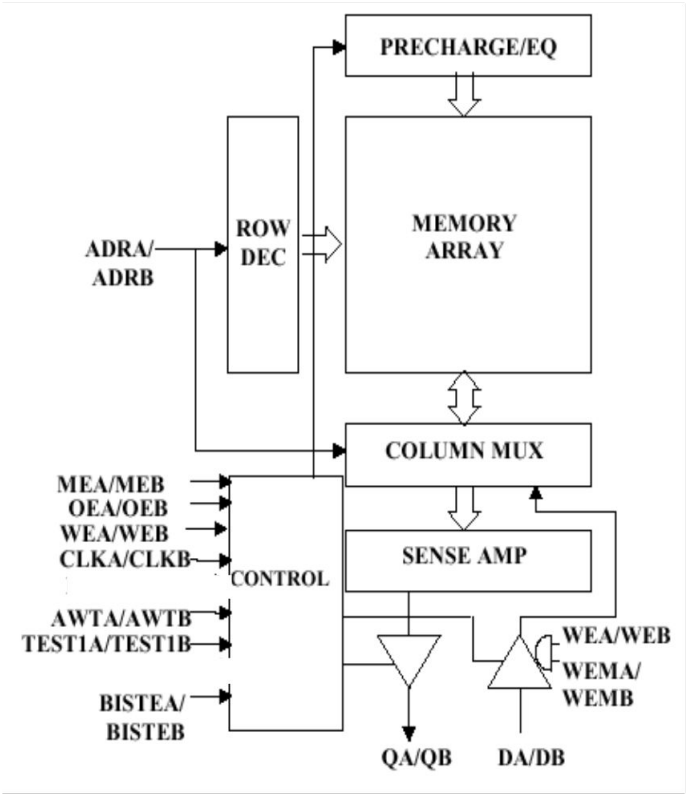
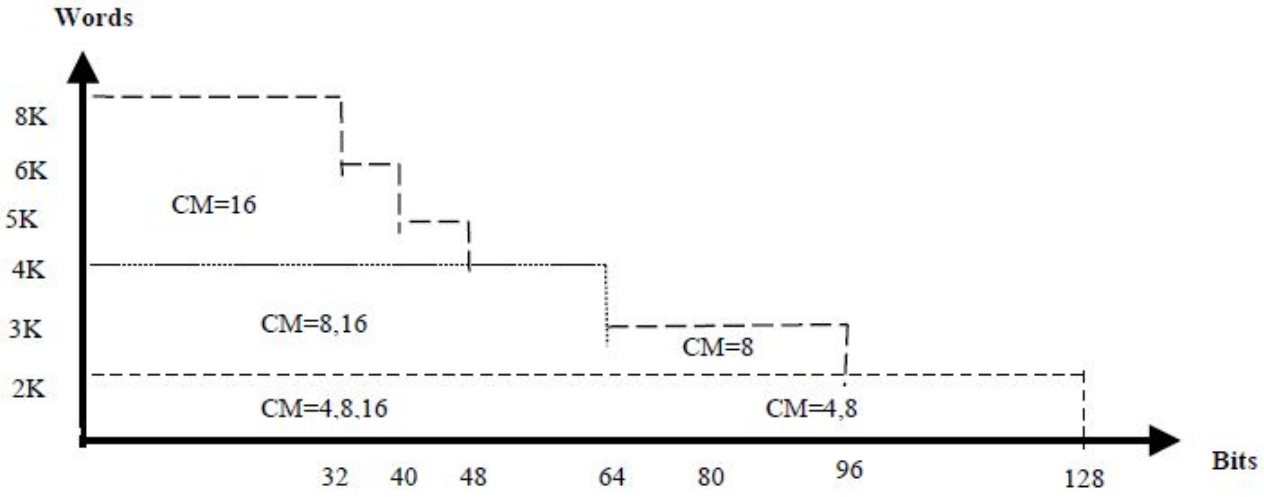


Figure 1-12. Dual-Port SRAM Address-, Word-, and Bit-Size Ranges



Microchip recommendations:

- To minimize multiple upsets errors per word, use the largest possible column mux (CM = 16).
- To bypass the memories during scan, it is recommended to use AWT.

Note: Even if AWT and BIST are not requested during memory generation, the mux logic is inserted by the compiler; the AWT and the BIST signals are tied to 0 in that case.

The following table lists the dual-port SRAM size limits.

Table 1-5. Dual-Port SRAM Size Limits

	Minimum	Maximum	Increment
Address inputs	4	13	1
Address (words)	16	8192	1 x CM [1]
Word size (number of IO bits)	2	128	1
Total bits in a core	32	256K	—

1. CM = 4, 8, and 16

The following figures show the dual-port SRAM read- and write-cycle timings.

Figure 1-13. Dual-Port SRAM Read-Cycle Timing

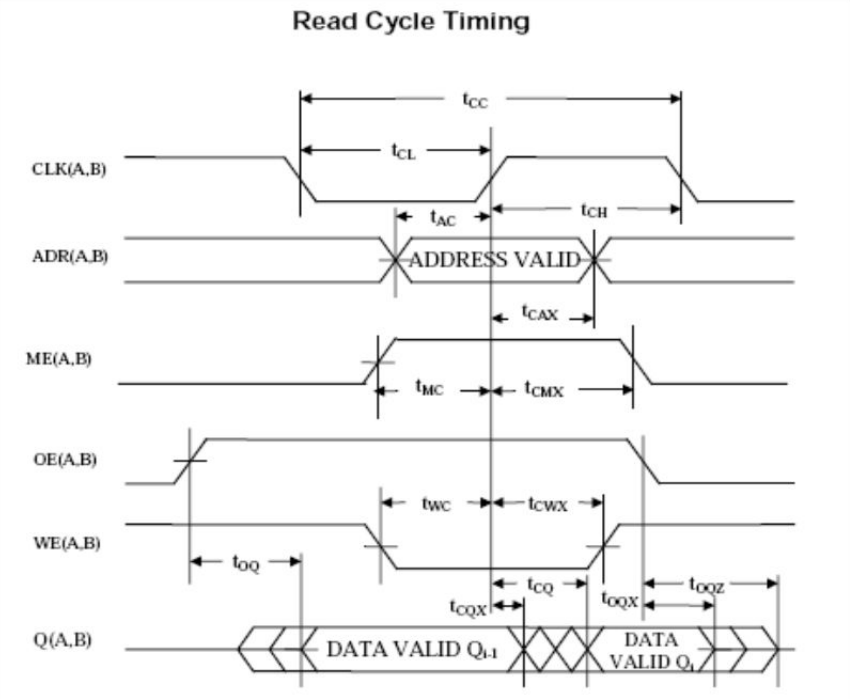
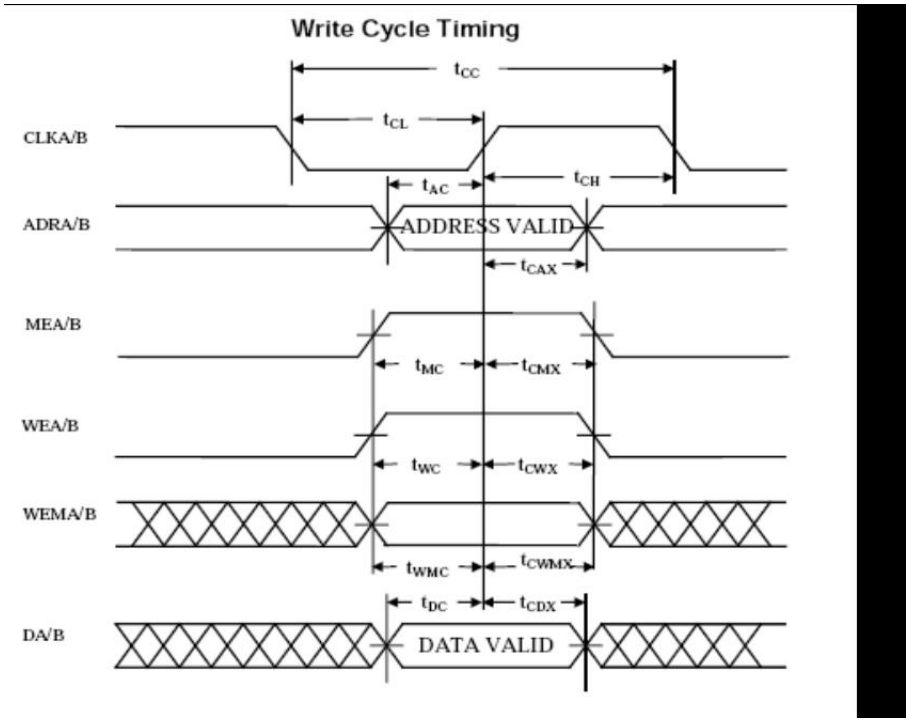


Figure 1-14. Dual-Port SRAM Write-Cycle Timing



The following table lists the dual-port SRAM 8kx8 timing specification.

Table 1-6. Dual-Port SRAM 8kx8 Timing Specification

Symbol	Parameter	Slow 145 1.60V	Fast -55 2.0V
TCC	Clock cycle time	6.0	—
TCL	Clock low cycle width	1.2	—
TCH	Clock high cycle width	1.1	—
TCQ	Clock to data out delay	6.0	—
TOQ	Output enable time	0.8	—
TAC	Address set up time before clock	0.7	0.4
TCAX	Address hold time before clock	0.7	—
TDC	Data set up time before clock	0.4	—
TCDX	Data hold time after clock	—	0
TMC	Memory enable set up time before clock	0.5	—
TCMX	Memory enable hold time after clock	—	0
TWC	Write enable set up time before clock	0.4	—
TCWX	Write enable hold time after clock	—	0
TDQ	Data in to data out delay when AWT = 1	1.4	—
TAWQ	AWT to data out delay	1.6	—

The following figures show the dual-port contention issues of case A and B.

Dual-Port Contention Issues

Case A

A. Dual port Contention Issue (Port A address equal to Port B address)

Port A	Port B	DA	DB	QA	QB	Memory State
Read	Read	DA	DB	Mem[a]	Mem[a]	No Change
Write	Read	DA	DB	DA	Unknown	Mem[a] <= DA
Read	Write	DA	DB	Unknown	DB	Mem[a] <= DB
Write	Write	DA	DB	DA	DB	Mem[a] <= Unknown

Case B

B. Dual port Contention Issue (Port A address not equal to Port B address)

Port A	Port B	DA	DB	DOA	DOB	Memory State
Read	Read	DA	DB	Mem[a]	Mem[b]	No Change
Write	Read	DA	DB	DA	Mem[b]	Mem[a] <= DA
Read	Write	DA	DB	Mem[a]	DB	Mem[b] <= DB
Write	Write	DA	DB	DA	DB	Mem[a] <=DA Mem[b] <= DB

Same Address Access Limitations

- If port A cycle is separated from port B cycles by less than Tcc and addresses are the same, consider this is the same address (case A).
- If port A cycle is separated from port B cycles by more than Tcc, consider this as different addresses regardless of address on port A and port B (case B).

1.3.3.3 Two-Port Synchronous Register-File

Separated output and input pins allow a write through cycle. An asynchronous write through mode (AWT) allows testing of interface shadow logic through scan. Separated clocks (clka and clkb), output (dob), and input (dia) pins allow independent read and write cycles. You can choose the output as a 3-state or always active. In case, the 3-state option is selected (application with several memories driving the same bus), you must ensure to avoid contention-problems as well as floating states. The BIST interface is optional but strongly recommended. The special test modes allow externally bypassing read and write self-timed. You have the flexibility in specifying the logical size of the register file including both the word size and the number of address locations, the column mux, and the output enable option. This memory includes an optional sub-word feature providing write to each group of 2, 4 or 8 bit sub-words. A maskable write enable signal (WEMA) serves each sub-word.

The following figures show two-port register file block diagram and address, word- and bit-size ranges.

Figure 1-15. Two-Port Register File Block Diagram

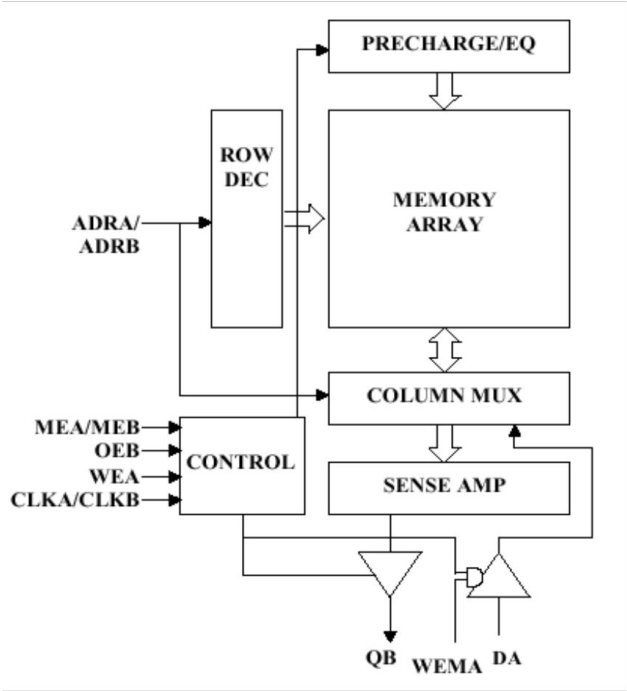
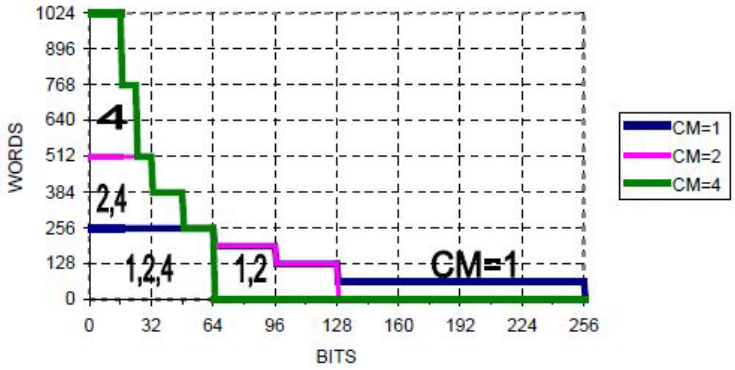


Figure 1-16. Two-Ports Register File: Address, Word- and Bit-Size Ranges



Microchip recommendations:

- To minimize multiple upsets errors per word, use the largest possible column mux (CM = 4).
- To bypass the memories during scan, it is recommended to use AWT.

Note: Even if AWT and BIST are not requested during memory generation, the mux logic is inserted by the compiler; the AWT and BIST signals are tied to 0 in that case.

The following table lists the register-file size limits.

Table 1-7. Register-File Size Limits

	Minimum	Maximum	Increment
Address inputs	3	10	1
Address (words)	8	1024	1 x CM [1]
Word size (number of IO bits)	2	256	1
Total bits in a core	16	16K	—

1. CM = 1, 2, and 4.

The following figures show the two-port SRAM read- and write-cycle timings.

Figure 1-17. Two-Port SRAM Read-Cycle Timing

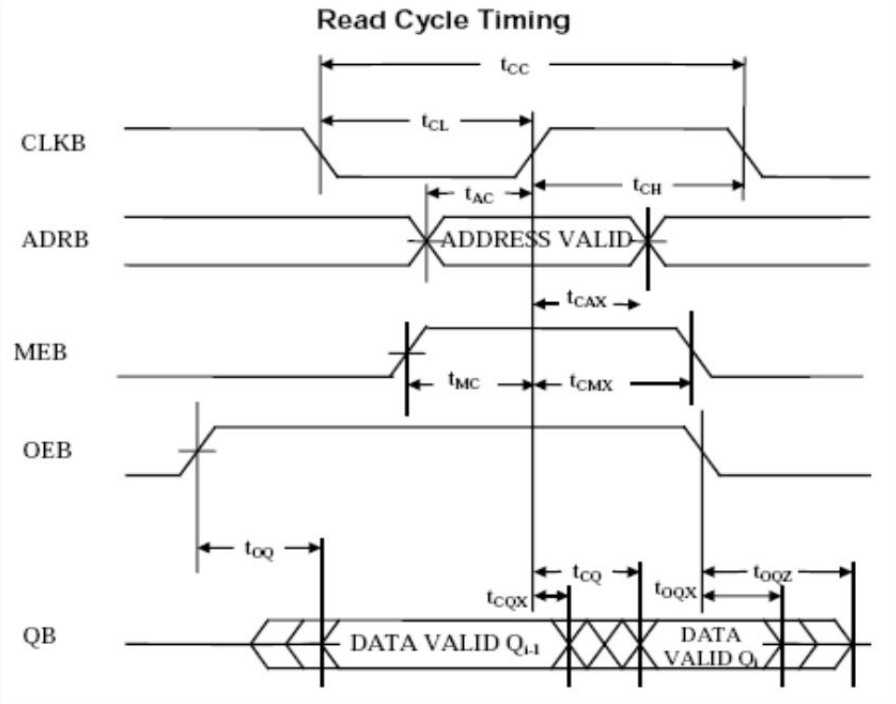
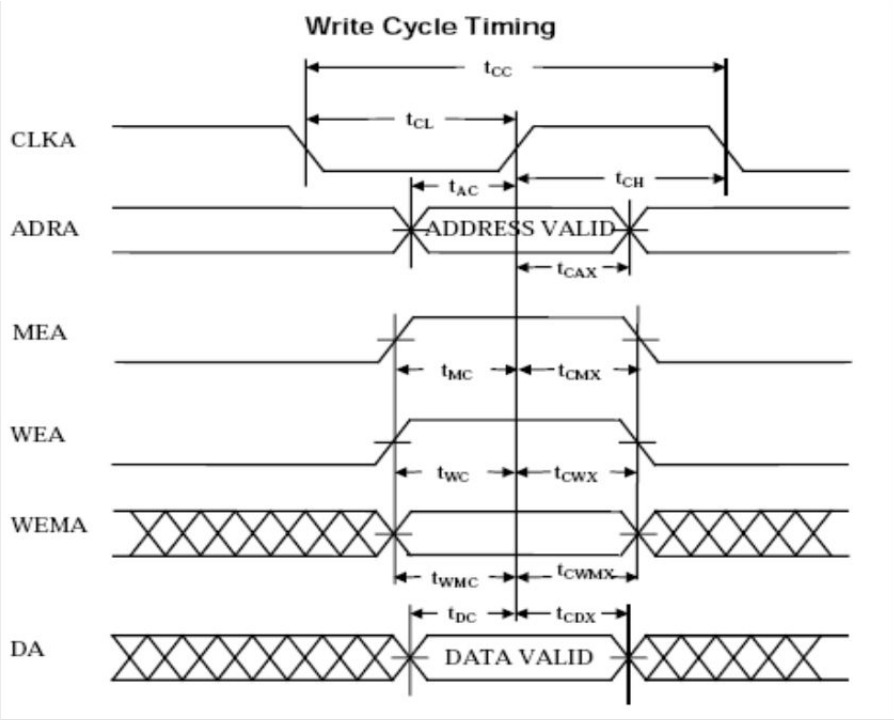


Figure 1-18. Two-Port SRAM Write-Cycle Timing



The following table lists the two-port register-file 2kx8 timing specification.

Table 1-8. Two-Port Register-File 2kx8 Timing Specification

Symbol	Parameter	Slow 145 1.60V	Fast -55 2.0V
TCC	Clock cycle time	6.1	—
TCL	Clock low cycle width	2.7	—
TCH	Clock high cycle width	3.2	—
TCQ	Clock to data out delay	5.2	—
TOQ	Output enable time	0.8	—
TAC	Address set up time before clock	0.5	—
TCAX	Address hold time before clock	—	0
TDC	Data set up time before clock	0.8	—
TCDX	Data hold time after clock	—	0
TMC	Memory enable set up time before clock	0.4	—
TCMX	Memory enable hold time after clock	—	0
TWC	Write enable set up time before clock	0.4	—
TCWX	Write enable hold time after clock	—	0
TDQ	Data in to data out delay when AWT = 1	0.80	—
TAWQ	AWT to data out delay	1.50	—

Dual-Port Contention Issues

Case A: Port A address equal to port B address. The following table shows the dual-port contention issue when the address of port A is same as the address of port B, clka is within Tcc (clkb) and clka = clkb.

Port A	Port B	dia	dob	Memory State
Write	Read	dia	Unknown	Mem[a] <= dia

Case B: Port A address is not equal to port B address. The following table shows the dual-port contention issue when the address of port A is not equal to the address of port B, clka is not within Tcc (clkb) and clka = clkb.

Port A	Port B	dia	dob	Memory State
Write	Read	dia	Mem[b]	Mem[a] <= dia

1.4 Array Organization

Though, ATMX150RHA is a standard cell library, pre-defined matrix sizes and pad frames have been set to ease the assembly of every individual ASIC design by sticking to presently available package cavity sizes and layouts. These are close in size to the ATC18RHA95 matrix sizes. Nevertheless, the development of a dedicated matrix as well as a dedicated package is possible.

The following tables list, for each matrix, for a single or a double pad ring configuration, the maximum number of pads on the outer ring, the maximum number of pads implementable on the inner ring, and the resulting typical gate count capability of each matrix based on NAND2-equivalent at 50% density without memories. The matrix-name

ATMX150RHA_<xxx><Y> indicates the number of IO-slots on the outer IO-ring (xxx), if it is a single or double-ring (Y) matrix.

The following tables list the standard array dimensions and standard arrays outer and inner rings configuration.

Table 1-9. Standard Arrays Dimensions

Name	Size (mm)	Area (mm^2)	Gates (typ)
ATMX150RHA_216 (D)	6.19 x 6.19	38	1 (0.8)M
ATMX150RHA_324 (D)	8.76 x 8.76	77	2.2 (1.7)M
ATMX150RHA_404 (D)	10.66 x 10.66	114	3.5 (2.8)M
ATMX150RHA_504 (D)	13.03 x 13.03	170	5.5 (4.4)M
ATMX150RHA_544 (D)	14.1 x 14.1	199	6,5 (5.4)M
ATMX150RHA_604 (D)	15.4 x 15.4	237	7.6 (6.7)M
ATMX150RHA_644 (D)	16.34 x 16.34	267	8.7 (7.7)M
ATMX150RHA_704 (D)	17.78 x 17.78	316	10.4 (9.4)M

Table 1-10. Standard Arrays Outer and Inner Rings Configuration

Name	Outer Ring Programmable Pads	Inner Ring Max. Number of Pads	Possible Power Supply Buffer in Corners
ATMX150RHA_216D	216	88	8
ATMX150RHA_324D	324	140	8
ATMX150RHA_404D	404	180	8
ATMX150RHA_504D	504	232	8
ATMX150RHA_544D	544	252	8
ATMX150RHA_604 (D)	604	284	8
ATMX150RH5_644 (D)	644	304	8
ATMX150RHA_704 (D)	704	332	8

1.5 Cell, Gate, and Site

In ATMX150RHA, the relation among cell, gate, and site is defined as follows:

Table 1-11. Relation Among Cell, Gate, and Site

	Cell	Gate	Site
Definition	**Element of the Cell Library**	**Lowest Drive NAND2 Used as Logic Design Unit**	**Placement Grid Unit Used as Physical Layout Unit**
Value	inv0d0, nd02d0, dfbrb1, and aoi211d1	4 sites = 12, 54 μm^2	0.56 x 5.6 = 3.136 μm^2

1.6 ATMX150RHA Layout Specificities

1.6.1 Power Grid Verification

Power grid verification is performed with dedicated tools, applying different state-of-the-art techniques. Static power-grid analysis as well as vectorless and vcd-driven analysis are performed to calculate the potential voltage-drop in the core. On top, electromigration-rules are checked to guarantee full functionality over the lifetime.

1.6.2 Crosstalk Analysis

Crosstalk has a non-negligible influence on the timing of a chip. Parasitic extraction tools allow to calculate coupling capacitances between signals. Based on this information, tools such as Primetime calculate the impact on the timing and propose layout modifications to solve the timing problems. Microchip needs detailed timing information from the customer (described in a constraint file in sdc format) to properly analyse the layout and repair potential issues. The more detailed the timing description, the better is the quality of the layout generated.

1.6.3 Antenna Processing

During manufacturing, when metal layers are processed on top of transistor gates, electrical charges are created upon the surface of the metal layer. If the charges are big enough, they can destroy the transistor input gate (oxide). Therefore, the transistor is no longer functional. This phenomenon is called the Process Antenna Effect (PAE). The PAE is checked and fixed by the router by computing the following ratio:

- Antenna ratio = SUM (metal area for one layer) / (input gate area)

The sum of metal area is the sum of all the wires touching the transistor gate. The maximum antenna ratio is given for each layer in the technology file. During the routing, the ratio is computed, and when it is bigger than the limit, the router is able to change some wires.

The antenna effects are checked during three steps of the physical design:

- The automatic routing (anticipation)
- The verification after routing
- The final chip DRC (with all blocks)

1.6.4 Spare Cells

As there are no fix under-layers for cell-based products, all the levels must be processed for each new application. If no care is taken, a simple debug, requiring few extra gates and links, may have the same mask cost as the original run.

This is the reason why cell-based designers are used to add extra cells distributed on the chip core. These spare cells are not used for the first run but may be easily taken for a small fix, with only few metalization layers to be redone. The spare cells usually represent 3% to 5% of the total amount of cells. The used models distribution can be as follows:

- 50% flip-flops/latches (prefer the larger possibilities with set, reset, inverted Q, and so on)
- 30% simple combinatory cells (inv, nand, nor, and mux)
- 20% complex gates (large aoi and oai)

For each cell type, prefer medium drive capabilities to be able to route long wires to reach the bug locations. Although, the spare cells are randomly distributed by the placement tool to cover the whole core. All spare cell inputs must be tied to supply.

2. Deliveries and Mixed-Signal Design Methodologies

The challenge of mixed-signal designs is the combination of two different design-approaches. Even if today's technologies require libraries for the digital cells with more than just a triplet with in-to-out timing, they are easier to handle than the complex analog blocks. Especially, the interface between the analog design and digital design must be handled carefully to give a maximum of design-safety and at the same time simplicity to allow reasonable design-times.

2.1 Deliveries

2.1.1 Analog Design

Analog design is mostly done at a transistor-level, as it requires precise simulations of the analog behavior. Entry-point is a schematic, which details all the active as well as passive elements.

2.1.1.1 Physical Design Kit (PDK)

- Elementary devices including rad-hard Pcell (For example, ELT transistors) for Cadence Design environment
- Electrical models (Spectre/HSpice/Eldo) over an extended temperature range Tj (-55 °C, 145 °C)
- Design rules DRC/ARC/LVS checker (Assura/Calibre)
- Documentation: Design Rules, Electrical Rules, and Recommended Radiation Design Rules

2.1.1.2 Open Access Library (OALib, Under DELA Addendum)

- Libraries of standard cells and I/O pads including (schematic, layout, symbol, and extracted) for Cadence
- Black box libraries of analog IPs including encrypted transistor level netlist (Spectre, HSpice, and Eldo)
- Documentation: Datasheets and Application Notes

2.1.2 Digital Design

Contrary to the design of analog circuitry, digital design is done at a higher level of abstraction. Starting from a textual behavioral circuit description and using automated flows to generate the gate-level equivalent and the related layout, it allows short cycle-times for the high complexity-designs:

- Design environment setup
- Libraries of standard cells, I/O pads, and analog IPs (timing, physical, and behavioral models)
- Documentation: Design Manual, Databooks, and Application Notes

For more details, contact the technical center that provides support in your area.

2.2 Mixed Signal Design Methodologies

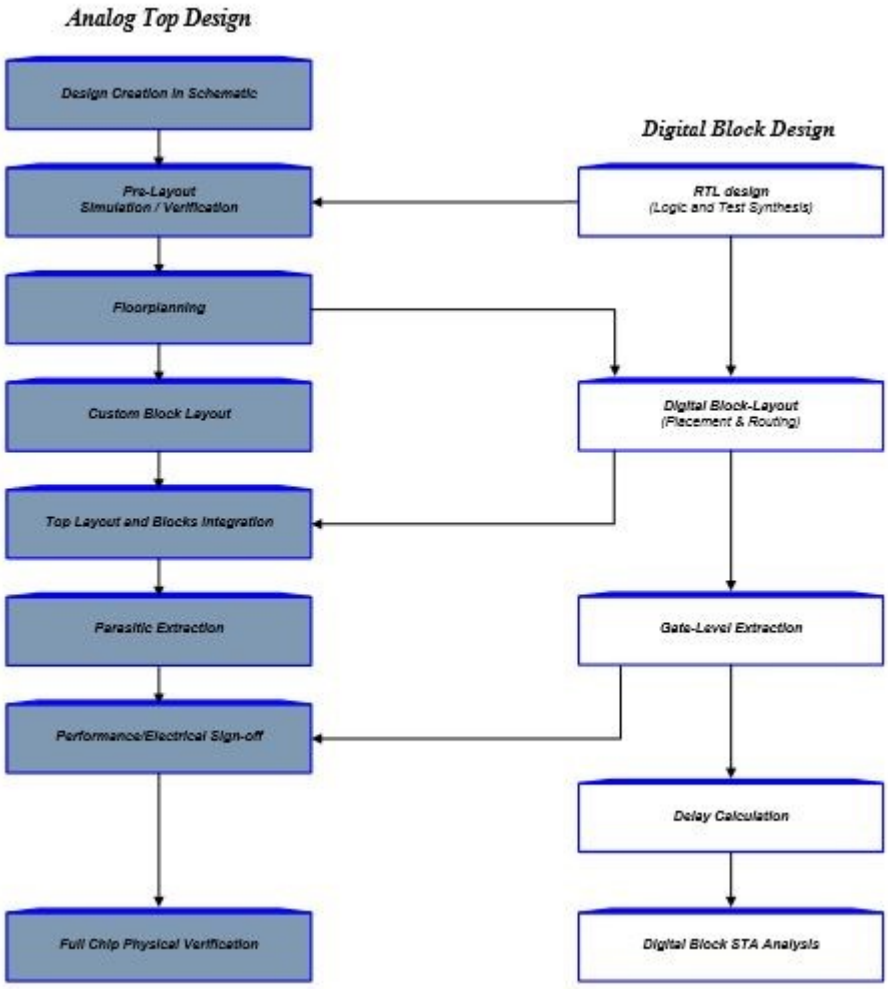
Globally, two approaches exist as of today:

- Analog-on-top: Where the design is performed in the analog world, embedding the digital part just as a black box.
- Digital-on-top: Where the abstract of an analog IP is embedded in a digital design-flow.

Analog-on-top is generally applied, when the analog part is dominant, determining the floor plan and cannot easily be divided in autonomous sub-blocks. The digital part is then generated with the standard tools and an abstract is placed in the analog design.

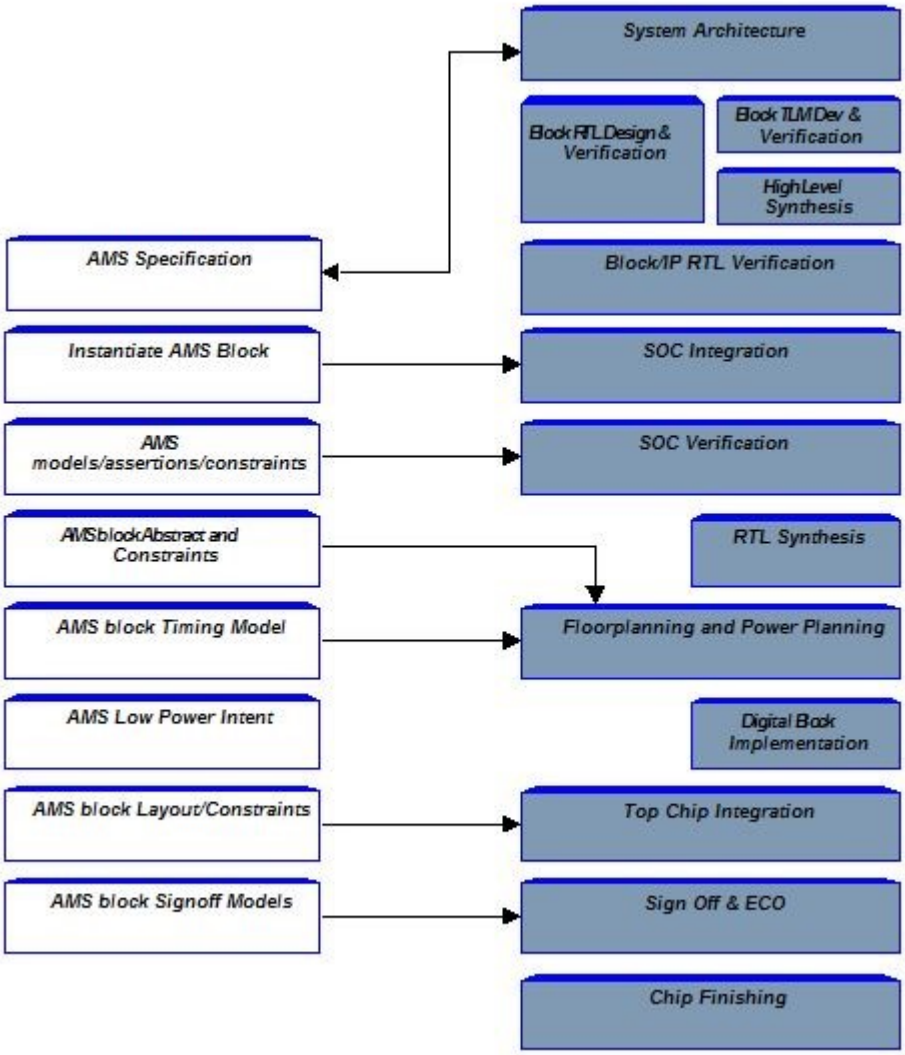
The following figures show analog-on-top flow and digital-on-top flow.

Figure 2-1. Analog-on-Top Flow



Digital-on-Top can be used, when the digital part is dominant and the analog IPs can be implemented “as-such”, and do not require fine-tuning within the design.

Figure 2-2. Digital-on-Top Flow



3. Design Management

To be compliant with the Microchip rules, the different project phases are related to different milestones. These must be followed-up in dedicated reviews.

3.1 Milestones

The following table lists the different project phases and its milestones.

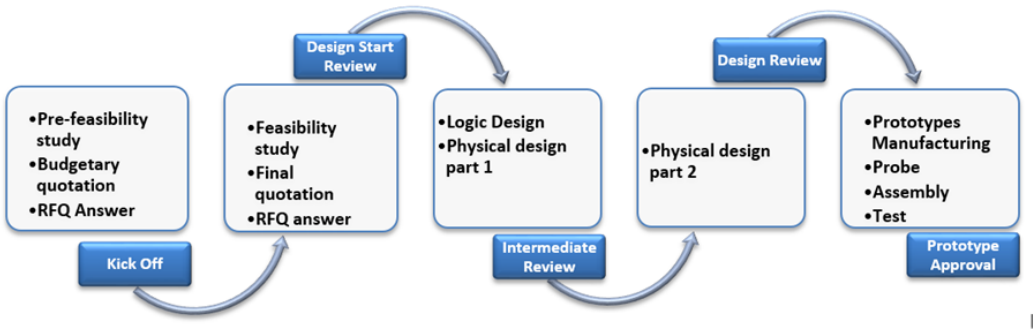
Table 3-1. Project Phases and Milestones

Project Phases	Milestones
Kick-Off Meeting	
ASIC Feasibility	Feasibility Review/Design Start Review
ASIC Development Phase 1	Intermediate Review
ASIC Development Phase 2	Design Review
Prototype Manufacturing	Validation/Industrialization Prototype Delivery
Product Verification	Prototype Approval
Product Launch	
Production	Release to Manufacturing
Manufacturing	

3.2 Design Phases

According to the flow chosen, the development of an ASIC chip can be split into five main phases. A meeting is set between each phase. The following figure shows the different phases of the design management.

Figure 3-1. Design Management Phases



- Phase 1: ASIC Pre-feasibility
  - Meeting: Kick-Off Meeting **(Optional)**
- Phase 2: ASIC Feasibility
  - Meeting: Design Start Review **(DSR)**
- Phase 3: ASIC Development Phase 1
  - Meeting: Intermediate Review **(IR)**
- Phase 4: ASIC Development Phase 2
  - Meeting: Design Review **(DR)**

- Phase 5: Prototypes Manufacturing
  - Prototype Approval **(AGR)**

During the review meetings, the conformity of the design to Microchip rules is checked and acknowledged in formal documents, and the data is transferred to the next phase. All fundamental changes, resulting in area increase, frequency/activity increase, power consumption increase, and package change can lead to cancel the current step and to go back to the previous one. This is monitored in a dedicated Design-Transfer Tracking document.

ASIC Pre-Feasibility Phase
During the pre-feasibility phase, several meetings and reviews can be setup to clarify customer requirements and project constraints. The results of the pre-feasibility study are provided to Marketing to build the Budgetary proposal to be sent to the customer. Once the order covering the feasibility is placed, a Kickoff review (also called, Preliminary Design Start Review) is organized.

Kick-Off Meeting (KOM)
The purpose of this meeting is to review at least the design perimeter supporting the budgetary proposal, defined design tasks, roles and responsibilities, project schedule, and risk assessment.

The KOM can be either a conference call or a face-to-face meeting.

ASIC-Feasibility Phase
During this phase, a preliminary database is used and the design tasks required to assess the feasibility are performed.

The results of the feasibility study are gathered in a report provided to the customer and reviewed during the feasibility review. Based on the feasibility report, the marketing builds a quote allowing sales to make a final commercial proposal.

DSR Meeting
As soon as the development order is placed, a Design Start Review (DSR) is organized. The DSR is a meeting to start the ASIC development between the customer and Microchip (under the responsibility of the Marketing and involving the Technical Center, the Product Engineering, Sales, and any other necessary resource).

The DSR is the ASIC development formal start meeting between the customer and Microchip. The feasibility study conclusions are discussed, including restrictions and critical points if any. At this step, all design constraints (specific skews, maximum frequency, blocks, and so on) are identified. This meeting also includes a review of the risk assessment table.

ASIC Development Phase 1
This section presents the physical design part 1 phase, which consists of the different tasks starting from a chip netlist to a fully placed, routed, and verified layout. Physical design part 1 can be divided into two main steps:

- Circuit layout, that is, placement, routing, and extraction
- Post-layout verifications, including simulations and static timing analysis

Once the netlist is ready, the circuit layout may be created using EDI or INNOVUS. This is first started by generating the matrix and pre-placing blocks using a symbolic layout editor. Peripheral cells can be pre-placed automatically from the bonding file (internal .P format). In the next step, the supply nets are routed within EDI or INNOVUS (core and block rings, periphery rings, and core cells supplies). The other components are then automatically placed, clock trees are synthesized with CTS (EDI) or CCOPT (INNOVUS), and the automatic routing of all the wires is finally performed.

EDI or INNOVUS takes into account timing constraints. Groups, regions, cannot occupy areas can be defined to ease and/or optimize the routing. These constraints may come from the floor-plan tool or from the symbolic layout editor. Timing constraints used during synthesis must be given too. Microchip uses pt_check to verify the quality of the timing constraints. The layout editor can also be used for critical path pre-routing and after the routing for correction of violations or routing optimization.

After routing or manual layout editing, the P&R-tool checks all the interconnection logic and design rules. The extraction of the parasitic elements introduced by routing is then performed with Synopsys StarRCXT or Cadence

QRC. At the end, some automatic bufferization may have to be done using the P&R-tool, when overloaded drivers are found. After any bufferization, a new verify and parasitic extraction will be carried out.

IR Meeting
The Intermediate Review meeting is held:

- When the place-and-route of the design is done based on the final customer netlist.
- When Static Timing Analysis (STA) matches with the customer requirements.

The objective of this meeting is to freeze the final layout: bonding diagram, netlist, critical paths, and also to discuss about the industrialization of the product.

At this step, the risk assessment table shall be updated if necessary.

After completing the Design Entry and Physical Design Part 1, timing objectives are reached and an equivalence checking between the output netlist and the entry netlist of this phase has been demonstrated, a formal meeting is set up involving the customer and Microchip, for the official freezing of the data and the start of the Physical Design Part 2 and Validation.

ASIC Development Phase 2
Physical Design Part 2 is dedicated to the layout-checks before fab operations (ARC, DRC, and LVS). Potential layout modifications have minor timing impact, but it is mandatory to re-run final STA again taking into account Cross Talk. IRdrop verifications are also run before Design Review.

DR Meeting
The objective of the Design Review meeting is to review the entire circuit database and to validate the physical design.

At this step, the risk assessment table shall be updated if necessary.

After completing the design layout, the entire circuit database is reviewed by the customer and Microchip in order to validate the Physical Design Part 2.

The main criteria to be checked are:

- Simulation results and STA with post-layout back-annotation timings
- Pad-placement with bonding diagrams and package features
- Test program in compliance with Microchip tester rules

The final agreement for processing the parts is mentioned in a formal document, which is signed by both sides, and includes all the reference file names and technical comments with a check list.

Prototype Manufacturing
Once the Design Review meeting has been held, the project database is transferred to the data mask preparation team for dataprep before to be sent to the maskshop. This database is then followed step by step by the Product Engineering (PE) group. The masks and test devices are created and used to process and test the samples before and after the assembly steps.

The test program generated during the development phase is applied either onto the wafer or after the dice are packaged. The test equipment is used for this operation. The samples are then shipped to the customer for functional acceptance.

The following lists the deliverables at the end of each design phase.

Table 3-2. Deliverables at the End of Each Design Phase

Design Phases	Deliverables	Who
Feasibility Study	ASIC feasibility study report ([TC]-FSR-F[xxxx]-[Design_Name].doc) Design start review document ([TC]-DSR-[Code]-[Design_Name].doc)	Microchip Customer/ Microchip

.....continued

Design Phases	Deliverables	Who
Logic Design and Physical Design Part 1	ASIC intermediate review document ([TC]-IR-[Code]-[Design_Name].doc) + Files as required in the document Updated risk analysis from the previous step	Customer/ Microchip Microchip
Physical Design Part 2	ASIC design review document with procurement specification (AID or ASIC Sheet) ([TC]-DR-[Code]-[Design_Name].doc) + Files as required in the document Updated risk analysis from the previous step	Customer/ Microchip Microchip
Prototypes Manufacturing and Test	Packaged parts and associated datalogs	Microchip

4. Design Flows

In the ATMX150RHA offer as discussed previously, four different ways to work are proposed by Microchip and each way involves different tools and different points of meeting between the customer and Microchip.

The two main contributors to choose the right flow are:

- Composition and size of the design
- Nature of the top-level design

Prior to all design-activities is a feasibility, which allows to decide for the right flow and gives an idea of the size and the complexity of the design.

Pre-layout digital gatelevel-simulation with estimated parasitics is not possible; only unit-delay can be applied.

4.1 Full-Custom Flow

The first one is the full-custom flow for a pure analog design. Microchip is less involved as the customer can work more alone except for packaging and final check on GDSII. To schedule the tape out and the packaging, a meeting point is still needed between Design Start Review (DSR) and Tape-out (DR) to define and support early enough the work on PE side.

The libraries for the digital IO-cells and the OALib may be delivered on demand.

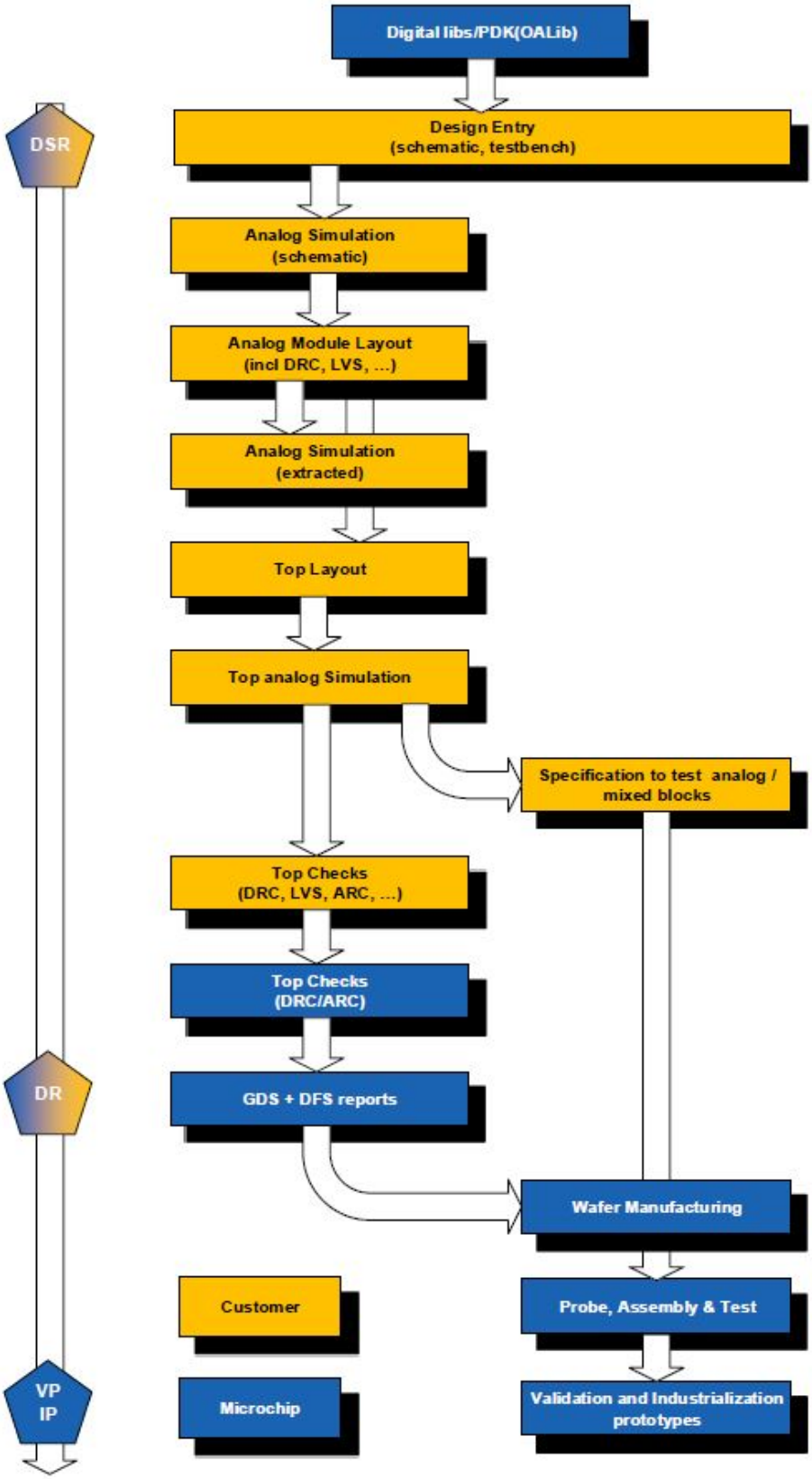
The following table lists the tools involved in full-custom flow.

Table 4-1. Tools Involved in Full-Custom Flow

Task Description	CAD Provider	Tool
Analog Schematic Entry	Cadence	Virtuoso Schematic Editor
Analog Simulation	Cadence	Spectre
	Synopsys	FineSim, FineSim-Pro, and hspice
	Mentor Graphics	Eldo
Analog Module Layout	Cadence	Virtuoso Layout Editor
Extraction	Cadence	QRC
Top Layout	Cadence	Virtuoso Layout Editor
Top Checks	Cadence	Assura

The following diagram shows the full-custom flow diagram.

Figure 4-1. Full-Custom Flow



4.2 Analog-On-Top

If Spice simulation is required to analyze the design at the top and full chip level, an analog-on-top methodology is required. The libraries for the digital IO-cells and the OALib may be delivered on demand.

The following sections show the tools involved and tools supported by Microchip.

Analog Part

Table 4-2. Tools Involved in Analog-On-Top Flow - Analog Part

Task Description	CAD Provider	Tool
Analog Schematic Entry	Cadence	Virtuoso Schematic Editor
Analog Simulation	Cadence	Spectre
	Synopsys	FineSim, FineSim-Pro, and hspice,
	Mentor Graphics	Eldo
Analog Module Layout	Cadence	Virtuoso Layout Editor
Extraction	Cadence	QRC
Top Layout	Cadence	Virtuoso Layout Editor
Top Checks	Cadence	Assura

Digital Part

Table 4-3. Tools Involved in Analog-On-Top Flow - Digital Part

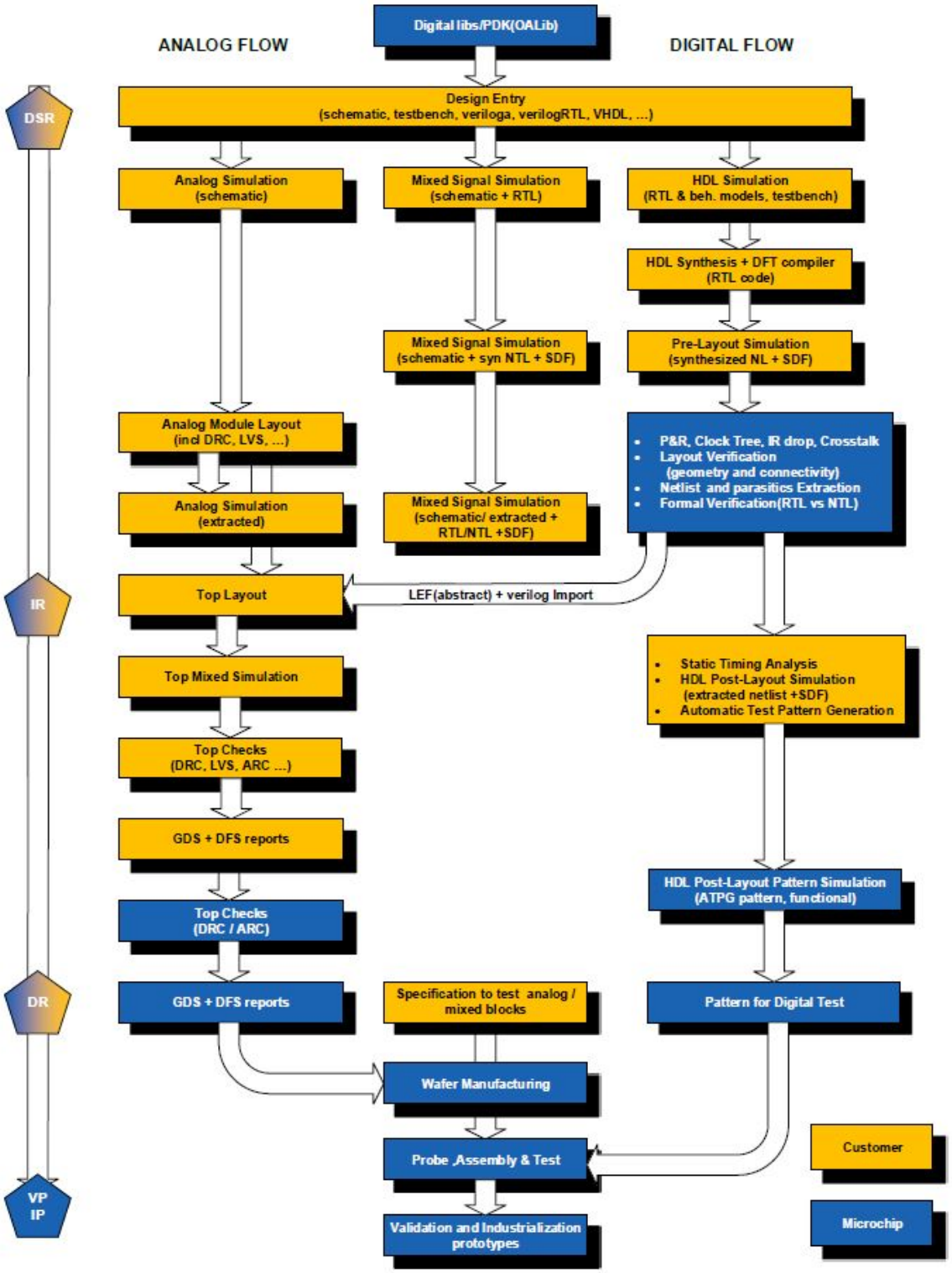
Task Description	CAD Provider	Tool
Design Entry/HLS	Mentor	Catapult [1]
HDL Simulation	Mentor Cadence	Questasim, Modelsim Incisive, Xcelium
HDL Synthesis	Synopsys	Design Compiler (Topo/Graphical)
DFT Insertion	Synopsys	DFT Compiler and DFT Max
Memory Bist Insertion	Mentor	MBIST-Architect
P&R, Clock Tree, Crosstalk	Cadence	Encounter Digital Implementation and Innovus
IR Drop	Ansys	RedHawk
	Cadence	Voltus
Formal Verification	Synopsys Cadence	Formality Conformal
Parasitic Extraction	Synopsys Cadence	STARRCXT QRC
Static Timing Analysis	Synopsys	Primetime Suite
ATPG	Synopsys	Tetramax

.....continued		
Task Description	**CAD Provider**	**Tool**
Post Layout Simulation	Mentor Cadence	Questasim AMS Designer, Incisive, Xcelium
Top Checks	Cadence	Assura

Note:

1. If C++ or SystemC is used.

Figure 4-2. Analog-on-Top



4.3 Digital-On-Top

Designs, which require a timing-driven methodology throughout floor-planning and can be signed off using STA, are more suitable for a digital-on-top methodology. The libraries for the digital IO-cells and the OALib may be delivered on demand.

Analog Part

Table 4-4. Tools Involved in Digital-On-Top Flow - Analog Part

Task Description	CAD Provider	Tool
Analog Schematic Entry	Cadence	Virtuoso Schematic Editor
Analog Simulation	Cadence	Spectre
	Synopsys	FineSim, FineSim-Pro, hspice
	Mentor Graphics	Eldo
Analog Module Layout	Cadence	Virtuoso Layout Editor
Extraction	Cadence	QRC
Top Layout	Cadence	Virtuoso Layout Editor
Top Checks	Cadence	Assura

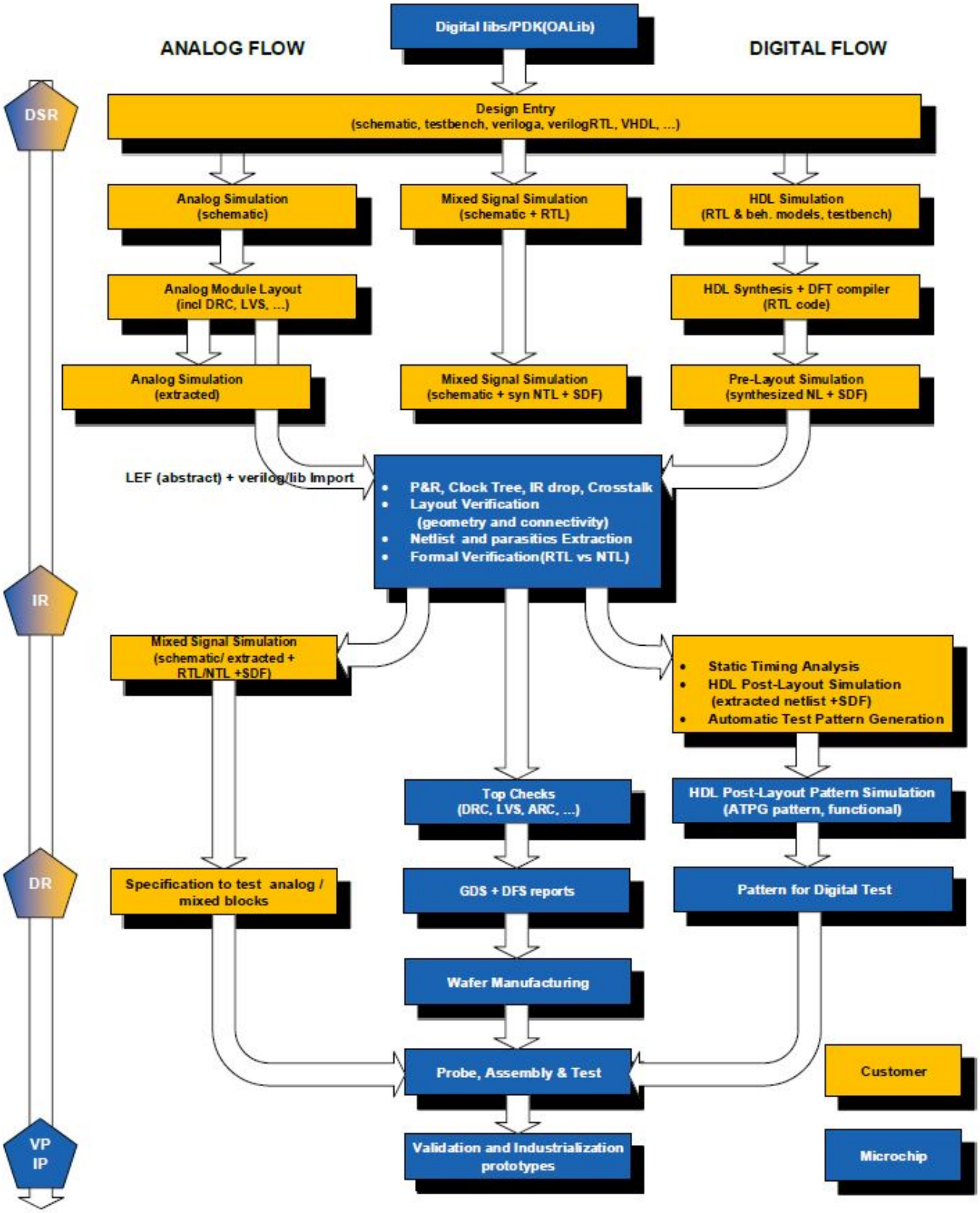
Digital Part

Table 4-5. Tools Involved in Digital-On-Top Flow - Digital Part

Task Description	CAD Provider	Tool
HDL Simulation	Mentor Cadence	Questasim and Modelsim Incisive and Xcelium
HDL Synthesis	Synopsys	Design Compiler (Topo/Graphical)
DFT Insertion	Synopsys	DFT Compiler and DFT Max
Memory Bist Insertion	Mentor	MBIST-Architect
P&R, Clock Tree, Crosstalk	Cadence	Encounter Digital Implementation and Innovus
IR Drop	Ansys	RedHawk
	Cadence	Voltus
Extraction	Synopsys Cadence	Star RCXT QRC
Formal Verification	Synopsys Cadence	Formality Conformal
Static Timing Analysis	Synopsys	Primetime Suite
ATPG	Synopsys	Tetramax
Post Layout Simulation	Mentor	Questasim, Incisive, and Xcelium

.....continued		
Task Description	**CAD Provider**	**Tool**
Top Checks	Cadence	Assura

Figure 4-3. Digital-on-Top



4.4 Full Digital Flow (Qualified QML-V, QML-Q, and ESCC QML)

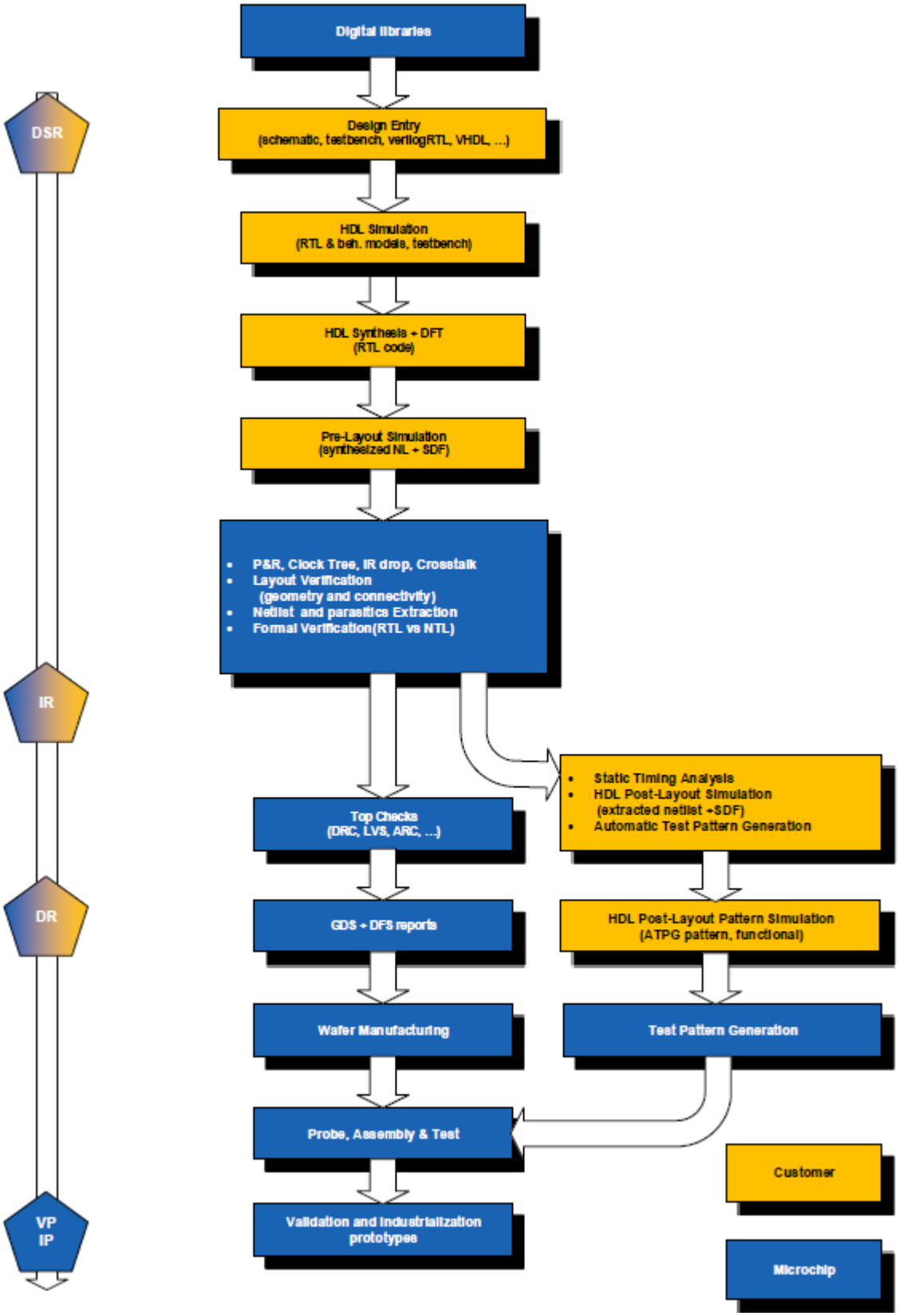
This flow is the classical digital flow.

Digital Part

Table 4-6. Tools Involved in Full Digital Flow

Task Description	CAD Provider	Tool
Design Entry	—	High Level Synthesis Tool
HDL Simulation	Mentor Cadence	Questasim and Modelsim Incisive and Xcelium
HDL Synthesis	Synopsys	Design Compiler (Topo/Graphical)
DFT Insertion	Synopsys	DFT Compiler and DFT Max
Memory Bist Insertion	Mentor	MBIST-Architect
P&R, Clock Tree, Crosstalk	Cadence	Encounter Digital Implementation, Innovus
IR Drop	Ansys	RedHawk
	Cadence	Voltus
Extraction	Synopsys Cadence	Star RCXT QRC
Formal Verification	Synopsys Cadence	Formality Conformal
Static Timing Analysis	Synopsys	Primetime Suite
ATPG	Synopsys	Tetramax
Post Layout Simulation	Mentor	Questasim and Modelsim
Post Layout Simulation	Cadence	Incisive and Xcelium
Top Checks	Cadence	Assura

Figure 4-4. Full Digital Flow (Qualified QML-V, QML-Q, and ESCC QML)



5. Design Tasks and Deliverables

5.1 Design Tasks

The following table lists the responsibility matrix generally used for the different flows. It may be adjusted to the requirements of the project.

Table 5-1. Design Tasks, Deliverables, and Responsibilities

Task Description	Flow Analog Responsible	Flow A_on_Top Responsible	Flow D_on_Top Responsible	Digital Responsible	Comments
Design Start Review (DSR)	Customer Microchip	Customer Microchip	Customer Microchip	Customer Microchip	—
SDC Timing Constraints Gate Level Netlist Pinout Tentative floorplan	—	Customer	Customer	Customer	List of Constraints (timing, package, IP, power, buffers, and so on)
Digital Block Level Place Clock Tree Synthesis Trial Route Extraction	—	Microchip	Microchip	Microchip	—
Analog Block Level Place Route Extraction	—	Customer (*)	Customer (*)	Microchip	(*) Could be Microchip in case of Microchip Analog IPs
Top Level Place Clock Tree Synthesis Trial Route Extraction	—	Customer	Microchip	Microchip	—
Customer Verification: simulation Static Timing Analysis	—	Customer	Customer	Customer	If not OK, constraints are relaxed or architecture tuned to pass this milestone. Three trials maximum. Beyond, cancellation charges or new Request For Quotation.

.....continued

Task Description	Flow Analog Responsible	Flow A_on_Top Responsible	Flow D_on_Top Responsible	Digital Responsible	Comments
Equivalence Checking	—	Customer	Microchip	Microchip	—
Final Route Metal Filling Signal Integrity Full Extraction Equivalence Checking	—	Customer	Microchip	Microchip	—
Final Customer Verification: simulation Static Timing Analysis	—	Customer	Customer	Customer	—
Intermediate Review (IR)	NA	Customer Microchip	Customer Microchip	Customer Microchip	Customer Agreement > IR signed
Test vector generation Burn in board definition and program Marking Diagram	—	Customer	Customer	Customer	—
Design Finishing	Microchip (*)	Microchip	Microchip	Microchip	ARC/DRC/LVS, (* DRC only for full analog), seal ring, mask patterns and dummies
Design Review (DR)	Customer Microchip	Customer Microchip	Customer Microchip	Customer Microchip	Customer Agreement > DR signed Procurement specification and test oriented simulations available. Flight Models Purchase Order received.

5.2 Deliverables

The following table lists the ownership matrix of the deliverables for the different flows. The list of deliverables and ownership may be adjusted to the requirements of the project.

Table 5-2. Deliverables at Each Design Step

Deliverable	Analog	A_on_Top	D_on_Top	Digital
ASIC Preliminary Specification (optional)	Microchip	Microchip	Microchip	Microchip
Project identification (name and type)	Customer	Customer	Customer	Customer
Package description	Customer	Customer	Customer	Customer
Rough description (nb FF, nb, type, and size of hard block, nb Cells, frequency)	Customer	Customer	Customer	Customer
Development schedule	Customer	Customer	Customer	Customer
Kick-Off Meeting				
Overall description of the ASIC	Customer	Customer	Customer	Customer
Estimated number of cells	—	Customer	Customer	Customer
Estimated number type and size of hard blocks (PLL, memories, analog, and so on)	—	Customer	Customer	Customer
Number of I/Os without supply	—	Customer	Customer	Customer
Expected AC and DC characteristics	—	Customer	Customer	Customer
Expected static and dynamic consumption	—	Customer	Customer	Customer
Main frequency and activity per block	—	Customer	Customer	Customer
Timing Constraints file including clock tree	—	Customer	Customer	Customer
Analog block description (abstract, model behavioral, timing, power, and connectivity)	—	—	Customer	—
Die size	Customer	Customer	Customer	Microchip
Package type	Customer	Customer	Customer	Customer
Preliminary pinout and floorplan	—	Customer	Customer	Customer
Preliminary netlist	—	Customer	Customer	Customer
Digital block (abstract, model behavioral, timing, and power)	—	—	Microchip	—
Detailed feasibility study report ([TC]-FSR-F[xxxx]-[Design_name]) including Risk analysis and Development schedule update	A ↔ C	A ↔ C	A ↔ C	A ↔ C
DSR Meeting				
Final pinout	—	Customer	Customer	Customer
Pinout verification (EMI, SSO rules, and bonding rules)	Microchip	Microchip	Microchip	Microchip
Final SDC constraints file	—	Customer	Customer	Customer
Final Netlist	—	Customer	Customer	Customer

.....continued

Deliverable	Analog	A_on_Top	D_on_Top	Digital
Final Analog blocks with I/O fixed, DRC-LVS free of error	—	Customer	Customer	Customer
Final floorplan	—	Customer	Customer	Customer
Final representative power consumption VCD file	—	Customer	Customer	Customer
Clock tree description, paths and FF numbers, clock groups, and clock domains	—	Customer	Customer	Customer
Equivalence checking report	—	Microchip	Microchip	Microchip
Netlist post layout	—	Microchip	Microchip	Microchip
SPEF with back annotated parasitics	—	Microchip	Microchip	Microchip
Equivalence checking report	—	Microchip	Microchip	Microchip
Post layout timing file(s)	—	Microchip	Microchip	Microchip
Activity, sdc and Vcd for IR drop-analysis in functional- and test-mode (if needed) based on post-layout netlist	—	Customer	Customer	Customer
STA with coupling capacitances	—	Customer	Customer	Customer
First IR drop results	—	Microchip	Microchip	Microchip
Intermediate review ([TC]-IR-[Code]-[Design_name]) including risk analysis and development schedule update	A ↔ C	A ↔ C	A ↔ C	A ↔ C
IR Meeting				
Test-oriented simulations and test-vectors in TECT-Database	—	Customer	Customer	Customer
Two marking files (1 for prototypes and 1 for production parts)	—	Customer	Customer	Customer
GDSII	Customer	Customer	—	—
DFS report (ARC/DRC/LVS)	Customer	Customer	—	—
Procurement specification (AID draft version or ASIC sheet)	Microchip	Microchip	Microchip	Microchip
Design review ([TC]-DR-[Code]-[Design_name]) including risk analysis and development schedule update	A ↔ C	A ↔ C	A ↔ C	A ↔ C
DR Meeting				

6. Design Libraries for Digital Design

Microchip provides a set of libraries, which are necessary for the safe design of complex microcircuits. These libraries are delivered along with installation notes to help the customer set up the design environment properly.

These library files describe the functionality, including or not timings and other attributes, with respect to each targeted tool's model features and methods.

The delivery contains relevant descriptions of standard cells, peripheral cells, and depending on the customer's needs, also analog or digital IPs. These are reflecting different pre-defined ranges of temperature, voltage, and process.

Table 6-1. ATMX150RHA Design Libraries Supported CAD Tools

Tool	Supplier	Purpose
Set of tools	Microchip	Microchip design support tools
QUESTASIM MODELSIM	Mentor	VHDL RTL + gate level simulation
DESIGNCOMPILER	Synopsys	HDL synthesis
DC TOPO, ICC	Synopsys	Physical synthesis see appendix_ATMX150RHA_synthesis_recommandation
PRIMETIMEPX	Synopsys	Power analysis see appendix_ppx
QUESTASIM, INCISIVE, XCELIUM	Mentor Cadence	Post-layout simulation
DFTC, TETRAMAX	Synopsys	Scan insertion (DFTC), JTAG (BSDC), Scan vectors generation see appendix_ATMX150RHA_dftc and appendix_ATMX150RHA_tmax
EDI/INNOVUS	Cadence	Floor-planning and layout prototyping
PRIMETIME	Synopsys	Static timing analysis and SDF generation
Redhawk	Ansys	IR-Drop analysis
VOLTUS	Cadence	IR-Drop analysis
CONFORMAL	Cadence	Equivalence checking and formal proof
FORMALITY	Synopsys	Equivalence checking and formal proof

The different types of information that can be found in the ATMX150RHA libraries are:

- **Functionality**
  The cell functionality is coded for most of the supported tools (synthesis, simulation, and so on). For gate-level simulation, VERILOG-models are provided.
- **Timings**
  Cell timings are present in some of the design-libraries (synthesis and timing-analysis). The values are resulting from characterizations done at the electrical level.

  The timings are characterized in the Space range, (that is, min/typ/max):
  - Temperature: -55/25/145 °C
  - Voltage: 1.95/1.8/1.65 Volts for Core; 2.75/2.5/2.25V and 3.6/3.3/3V for the peripheral cells

- Process: Best/Typical/Worst

The different timing elements found in the design libraries are the following:

- Input to output delay for each valid path
- Output slopes for each valid path from inputs
- Timing checks: setup, hold, min-pulse width, recovery, removal

The values of internal cell delays and output slopes are stored in Look Up Tables (”LUT”). These tables give input to output delays or output slopes depending on input slope and output capacitance:

- Delays: 7x7 LUT
- Slopes: 7x7 LUT

The timing checks are also modeled in LUT with different values of input slope on input pins and references.

The models are compatible with SDF V3.0 back-annotation.

- **Other Parameters**
For synthesis tools, some other parameters are necessary:
  - Wire-Load Models (WLM): To estimate delays before layout.
  - Element Size: The size of each cell expressed in μm^2 used for area estimation.
  - Power Values: Characterized values required by the power optimizer and the static power analysis tool.
  - Fanins/Max-fanouts: Input gate capacitance and output max load expressed in pF.

The physical views (for floor-planning for instance) contain width, height, I/O locations and layers and blockages.

Logic Synthesis
Logic Synthesis translates the RTL customer code to a structural netlist using Microchip ATMX150RHA libraries. This structural netlist is provided to Microchip in a verilog format for feasibility study or design layout development.

Test Synthesis
Test Synthesis inserts test structures such as scan and bist. It ensures a high fault coverage on the circuit for detecting fab defaults during probe and test operations.

Note: Stuck-at faults detection and Transition Delay Faults are mandatory to ensure a high level of confidence in the production parts. For that purpose, Memory-Bist shall also be executed at application-frequency.

Logic Simulation
The logic simulator runs a set of defined patterns (stimuli) on the circuit netlist. Delays, either estimated or from a physical view, are usually defined in a file in SDF format. The simulation is run in three corners (min, typ, and max), and the results must be compatible with respect to the clock period.

Static Timing Analysis
The static timing analyzer highlights all critical paths and checks timing violations (setup, hold, and so on).

Static timing analysis has to be run several times during ATMX150RHA flow. Prior to the Intermediate Review, a post layout STA is run taking into account all parasitic-effects. The Intermediate Review is done only when STA matches with customer requirements.

Between IR and DR, a new STA might be required, if DRC/ARC or LVS leads to layout-modifications. To take into account the effects of cross coupling capacitances, the SPEF file with coupling capacitances, generated by STARRCXT/QRC in signal integrity mode is loaded in Primetime SI tool for analysis.

Important: For STA before Cross Talk analysis, hold margin min required is 0.1 ns.

Voltage Drop Effect on Timing Analysis
The standard approach is to get IRdrop (vdd + gnd) below 10% in dynamic mode with the package-extraction included and below 5% for static-analysis.

To do this with the best accuracy, as this IRdrop can have an effect on the power scheme of the die (stripes and follow pin distribution, number of supply buffers). Microchip asks the customer to produce a vcd file with all

internal nets on a few cycles representing the worst case activity. This file must be available at the IR meeting at the latest. If not possible, Microchip runs vectorless dynamic analysis with a toggle activity specified on inputs, outputs, and all internal nets provided by the customer.

ATPG, Stuck-at, and TDF Vectors
When scan structures have been inserted in the netlist (during logic synthesis or after with a scan insertion tool), an automatic test pattern generation (ATPG) can be performed.

Microchip requires to use both vectors Stuck-At fault model and Transition Delay Fault model (TDF).

Objectives are to reach at least a test coverage of 80% for TDF and 98% for stuck-at Fault.

Concerning ATPG patterns, Microchip requires:

- A complete STIL99 format file
- min/typ/max simulations from a serial test bench on the first five patterns
- The transcript/log files (min/typ/max) from simulation of the parallel test bench must be provided to Microchip

No mismatch between testvectors derived from MIN- and MAX-simulations is recommended, in case of mismatch, only one case will be tested.

⚠ CAUTION As the STIL file is coming from an ATPG tool with no timing model in the library, special care must be taken during STA for the timing of global nets such as Scan_mode, Scan_enable, and Reset. Their timing might have an impact on the frequency of the ATPG-patterns.

See the ASIC Test Manual (ATD-DE-GR-R0324) for more information.

Post Layout Verification
Once the Place-and-Route phase is achieved, the 3D parasitic values due to the routing are extracted. This file is used in conjunction with the final routed netlist.

To ensure that the circuit has the same response as before the layout step, the layout parameters of the circuit components (cells and buffers) are back annotated into the simulation. The parasitic file (SPEF) generated by StarRCXT from Synopsys or QRC from Cadence is read by a timing calculator integrated in PRIMETIME. These values are used for STA and to generate the Standard Delay File (SDF) timing file for simulation. The simulator replaces the default or estimated values describing the effect of the layout, with the real timings from the SDF.

This has to be done for functional simulations running in min, typ, and max.

Equivalence Checking
As the netlist may be changed during these optimization steps, it may be useful to verify the last version is still equivalent to the original synthesis result. This is the goal of the equivalence checking. In the past, only time-consuming simulation could eventually show existing mismatches.

An equivalence checker is an application that uses formal techniques to prove or disprove the functional equivalence of two designs. For example, you can use an equivalence checker to compare a gate-level netlist to its Register Transfer Level (RTL) source or to a modified version of that gate-level netlist. After the comparison, the equivalence checker reports whether the two designs are functionally equivalent or not. An equivalence checker can significantly reduce the design cycle by providing a faster alternative to simulation for regression testing.

The techniques that an equivalence checker uses are static and thus do not require simulation vectors. Consequently, you only need to provide a functionally correct or golden design (called the reference design) and a modified version of the design (called the implementation). By comparing the implementation against the reference design, you can determine whether the implementation is functionally equivalent to the reference design.

Formal-proof is generally applied whenever a significant netlist-change occurs, like scan-insertion, scan-chain reordering or if any manual impact because of minor logic-modification was performed.

6.1 Design-Support Tools

The Microchip design-support tools help to secure the data-transfer from the customer to Microchip. There are two groups of tools; design-oriented checks and test-oriented tools.

The design-oriented checks are performed by RUN_PT_DRC, which is based on Primetime from Synopsys and checks the consistency of constraints and several rules imposed by the use for space.

The test-tools check the availability and correctness of all what is needed to produce the device. It consists of TVT_NG2, a tool which converts simulation-results to test vectors and TECT, which creates a database with the necessary information for the assembly, probe and final test of the device.

PT_DRC: Design-rules and Timing constraints check

- Section run_pt_drc

TVT_NG: Simulation Results Formatting for Testers

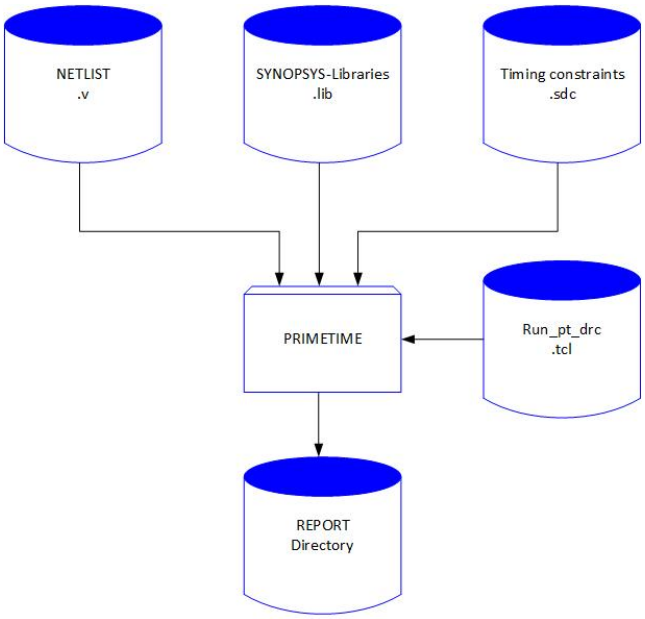
- Section TECT and TVT_NG

TECT: Database-handling for Testprograms and Burn-In-Board

Section TECT and TVT_NG

6.1.1 run_pt_drc

Figure 6-1. Design-Rules and Timing-Constraints Check



run_pt_drc is a tool dedicated to design checks based on Primetime.

6.1.1.1 Pre-Defined DRC Configurations

run_pt_drc offers the user, through -check option, the use of several DRC configurations according to the status of the design to check (out of synthesis or post layout). These predefined DRC configurations are listed as follows:

- full: All possible DRC tests are run. This is by default.
- checkin: The minimum check list for pre-layout (out of synthesis) netlists. This is the sign-off DRC configuration for this kind of netlists and all tests must pass or be formally waived for acceptance (to start the place-and-route phase).
- checkout: The minimum check list for post layout netlists. This is the sign-off DRC configuration for this kind of netlists and all tests must pass or be formally waived for acceptance (for transfer to sign-off STA simulations).

- full_checkin: A complete check list for prelayout (out of synthesis) netlists. Includes checks done by checkin configuration plus some extra design analysis. See the DRC Test Procedures section for the differences between checkin and full_checkin configurations.
- full_checkout: A complete check list for post-layout netlists. Includes checks done by checkout configuration plus some extra design analysis. See the DRC Test Procedures section for the differences between checkout and full_checkout configurations.

6.1.1.2 DRC Test Procedures

DRC tests are tcl procedures applied on the design to test. They are called in the file '<*config*>_drc_config.tcl', where <*config*> is the name of a predefined DRC configuration or 'custom'.

The following table lists the tcl procedures (in alphabetical order) and if they are called (or not) in the predefined DRC configurations.

Function Configuration	Full	Checkin	Checkout	full_checkin	full_checkout
drc_analog	×	×	×	×	×
drc_clock_as_data	×	—	—	×	×
drc_clock_tree	×	—	—	—	×
drc_combinational_drivers	×	—	—	×	×
drc_delay_chains	×	—	—	—	×
drc_fanout	×	—	×	—	×
drc_floating_inputs	×	×	×	×	×
drc_floating_outputs	×	×	×	×	×
drc_floating_outputs2	—	—	—	—	—
drc_forbidden_lib_cells	×	×	×	×	×
drc_lib_cells_without_set_reset	×	—	—	×	×
drc_loops	×	×	×	×	×
drc_max_voltage	×	×	×	×	×
drc_min_transition	×	—	×	—	×
drc_multiple_drivers	×	×	×	×	×
drc_no_clock	×	—	—	×	×
drc_pll	×	×	×	×	×
drc_ports	×	×	×	×	×
drc_reset_tree	×	×	×	×	×
drc_statistics	×	×	×	×	×
report_clock_steering	×	—	—	×	×

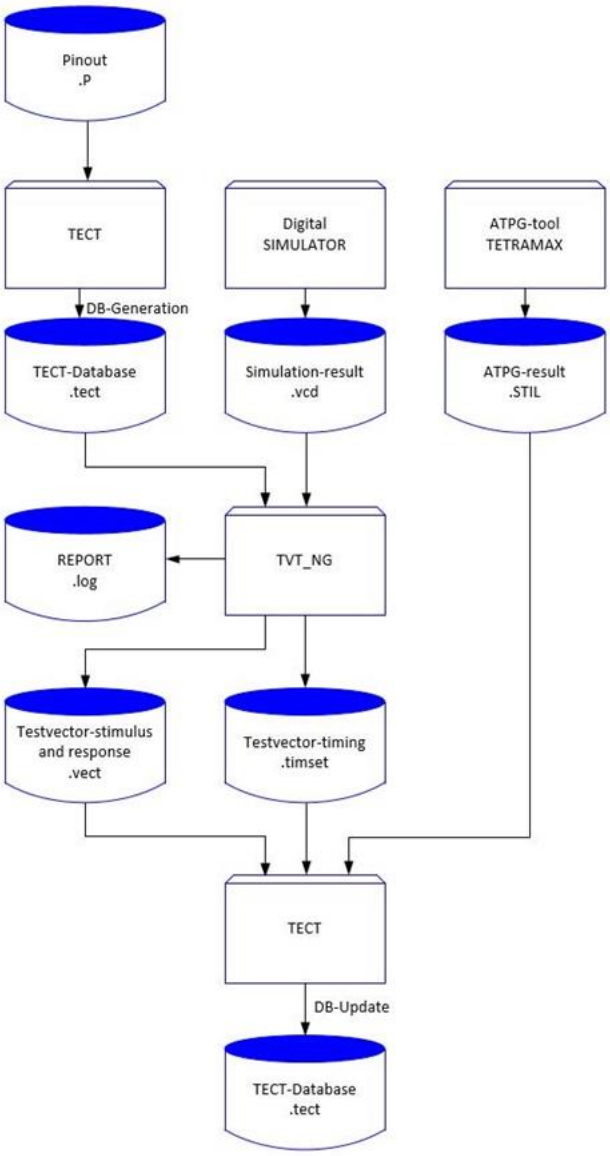
The list of checks is not exhaustive and may be subject to changes.

The complete list and details of how to use `run_pt_drc` are described in the `run_pt_drc` user's guide, which can be found in the document, *aero_util_ug.pdf*.

If you have not received this file, contact your local design center.

6.1.2 TECT and TVT_NG

Figure 6-2. Test Generation Flow



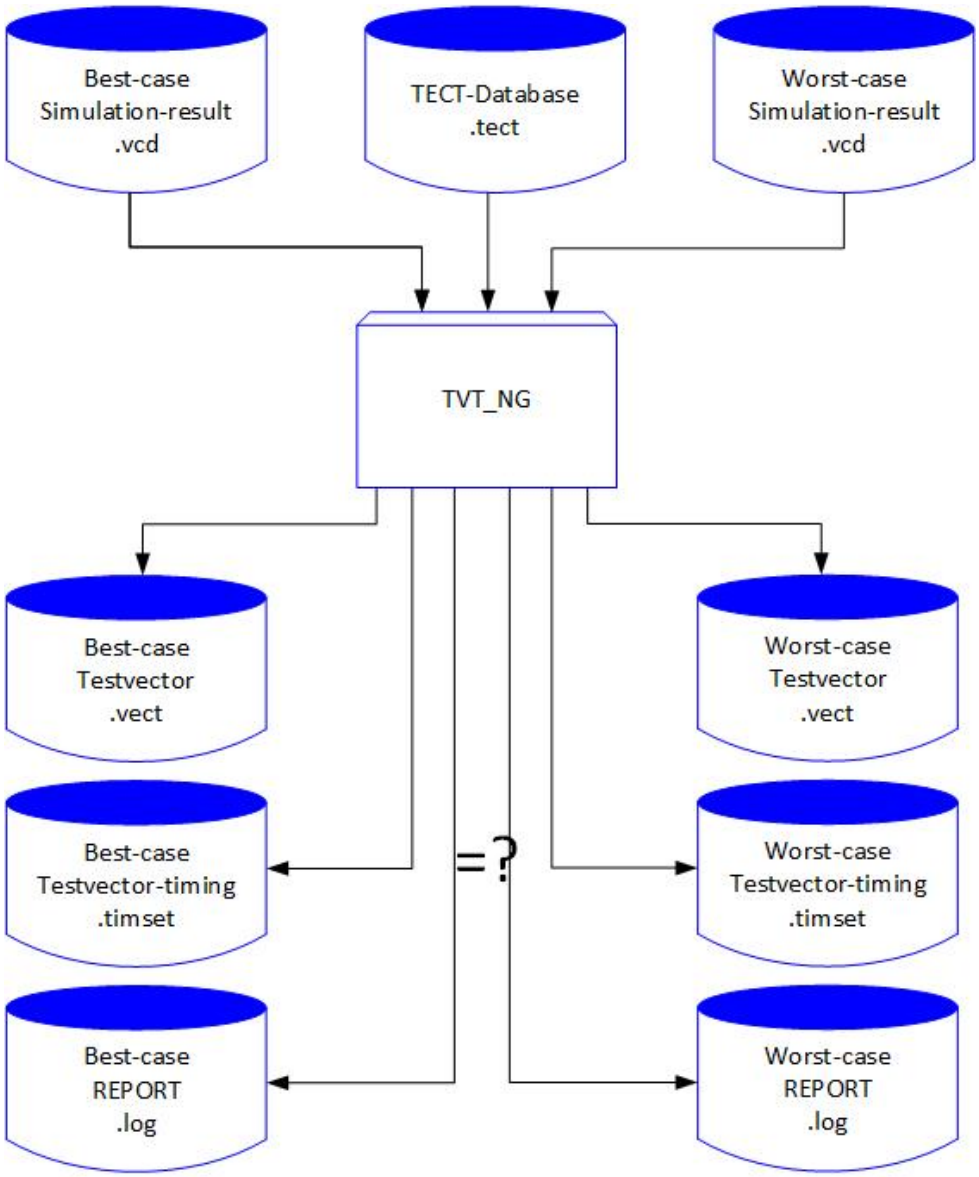
TECT is a database-tool, which combines Pinout-, Burn-In-Board, and Test-information. The database is used to transfer test-related data to the product-engineering group. TVT_NG is a tool developed to verify Test Rules, generate Test vectors and guarantee the correctness of these before the transfer to Microchip.

TECT reads the Pinout-description .P-file and generates the TECT-database. This database is used along with the simulation-/ATPG-result files, where inputs, outputs and bi-directional (plus their control signals) are treated by TVT_NG to check, that it is compliant to the Microchip Test-Oriented Simulation (TOS) rules (see the ASIC Test Manual ATD-DE-GR-R0324 document).

The output of TVT_NG is a vector file (.vect), which will then be used by the tester to check that the real circuit response is consistent with the expected one.

TVT_NG also allows the comparison between best-case and worst-case simulations, which must give identical strobe results and thus identical vector-files. Since the result of TVT_NG is a file containing the input stimuli and the corresponding output response at the strobe instant (that is, at the instant when the tester will strobe the outputs), a simple diff-command on worst .vect and best .vect files is enough to check that the circuit has the same behavior throughout the operating range.

Figure 6-3. Best- and Worst-Case Simulation Comparison



7. Design Rules

7.1 Power Supply Rules

The preliminary methodology described in the following paragraphs is mainly based on electro-migration considerations. The global power pairs count is one point, but the supply pads distribution around the die and the package impedance characteristics are also key features to insure the best timing performances.

Important:
It is explicitly required to validate the computed number of supply pairs (for both core and buffers) and the placement of I/O buffers in the periphery by Microchip's proprietary tool COP. On top, only this tool is able to handle properly the electro-migration rules.

A further verification with package characteristics (for example, reflection, termination, and so on.) must be done with a Microchip expert.

7.1.1 General Rules

The die switching power can be divided into array (cells) power and I/O (buffers) power. The associated supply pads are (see Power Pads and ESD cells):

- Buffer outer stage supplies (VCCB, VSSB): also called VDB and VSB
- Core (vdd!, gnd!) + Buffer inner stage (VCC, VSS): also called VDA and VSA

The maximum allowed current per supply pad is: Ic = 60 mA.

Average power is given in uW/MHz. For data (N), Mbit/s is equivalent to (N/2) MHz.

7.1.2 Array Supply Rules

The number of supply pairs (VDA and VSA) is determined from the worst case current between:

- Itot: Total circuit current in worst case operating conditions
- Ipeak: Peak current related to simultaneous switching of gates

Important:
Microchip recommends to limit the number of simultaneously switching flip-flops (that is, Flip-Flops switching with the same clock-edge) to 50000.

There are two ways to get a first idea of the power-consumption. The calculation of average consumption as shown here below will only serve for a first dimensioning of the supply-scheme. There is also an Excel-sheet "ATMX150RHA_Current Consumption_Evaluation_Form_v01.xlsx" available allowing to calculate in more detail the consumption to be expected. RedHawk from ANSYS, Primetime_PX from Synopsys and Voltus from Cadence can be used to analyze the consumption based on the final layout and a representative simulation-result (vcd-file) from the customer.

Average Power and Current
The parameter definitions are as follows:

- Ka: Global activity factor of the circuit (0< Ka < 1)
- Ngates: Number of logic gates in the circuit
- F: Maximum frequency in the circuit (in MHz)
- Pavg: Average power per logic gate and MHz in µW. This value is based upon circuit statistics (cell usability and average parasitics) and is representative of a typical circuit architecture. It is given for worst case operating conditions (process, VDD, temperature)

- Ptot: Total circuit power in worst case operating conditions (process, VDD, temperature), dependent upon number of logic gates and global circuit activity
- Itot: Total circuit current in worst case operating conditions (process, VDD, temperature)

Pavg = 0.057 µA*1.95V/MHz/gate

Ptot (µW) = Ka x Ngates x Pavg x F

Itot (mA) = Ptot / (1000 x VDA)

Peak Current
The parameter definitions are as follows:

- Nssf: Max number of simultaneously switching flip-flops
- Ipeak: Core peak current in mA

Ipeak = Nssf x 0.250

Number of Core Supply Pairs
Np vda/vsa = max (Itot, Ipeak/3) / Ic

Where Itot and Ipeak are expressed in mA and Ic is the maximum allowed current per supply pad. The ultimate number of supply-pairs is confirmed during the feasibility-study.

Recommendations

- In case of several clock trees switching at different times, apply the formula to each of them, and take the worst case
- In case of asynchronous clocks, take the worst case which is the simultaneous switching case

It is better to:

- Group VDA/VSA per pair (side by side supply pads without any buffer sites between them)
- Distribute the pairs as evenly as possible around the die (each supply pad should not exceed the Ic limit)
- see also VDA and VSA Pairs for Buffers

Double bonding does not decrease VDA/VSA supply pairs count.

7.1.3 Buffer Supply Rules

The number of supply pairs (VDB and VSB) is determined from the worst case current between:

- Itot: Total circuit current in worst case operating conditions
- Ipeak: Peak current related to Simultaneous Switching Outputs (SSO)

Note: The values given in the tables in this section are only estimations. To obtain the final values run COP, Microchip's proprietary tool.

Average Power and Current
The parameter definitions are as follows:

- <N_i> is type i buffer count in the cluster
- <Cout_i> is type i buffer capacitive load (in pF)
- <Fout_i> is type i buffer frequency (in MHz)
- <P_i> is type i buffer intrinsic power consumption (in µW/MHz) (see the following table)
- <Vout_i> is type i buffer maximum voltage swing
  - 2.75V or 3.6V for IO25 or IO33
  - 0.5V for LVDS and LVPECL
- <Pstatic_i> is type i buffer static power (Istatic x VDB_i expressed in µW)

Pout (µW) = SUMi (N_i x((Cout_i x(Vout_i)2 + P_i) x Fout_i + Pstatic_i))

Itot (mA) = Pout / (1000 x VDB), where VDB is the cluster buffer voltage.

Table 7-1. Buffer Intrinsic Power (µW/MHz) Per Type

Buffer Type	P_i	Pstatic_i
IO25 (Type = 01, 02, 04, 06, 08) used at 2.5V	90, 95, 100, 105, 125	0
IO33 (Type = 01, 02, 04, 06 ,08) used at 3.3V	150, 155, 155, 190, 240	0
IO50 (Type = 01, 02, 04, 08) used at 5.0V	310, 340, 400, 790	0
PCI (PP33B01Z, -T01Z, -O01Z)	250	0
LVDS transmitter (pl33txz)	155	20000
LVDS receiver (pl33rxz, pl33rxrz)	7.5	10000
PECL receiver (pe33rxz)	7.5	4000
LVDS transmitter (pl25tx)	180	16000
LVDS receiver (pl25rx, pl25rxrz)	4.5	5500
PECL receiver (pe25rxz)	4.5	3000

Peak Current (SSO)

The parameter definitions are as follows:

- <N_i> is type i buffer count in the cluster
- <Drive_i> is type i buffer drive strength
- <Istatic_i> is type i static current (see the following table)
- <alpha> is a coefficient to take into account the dynamic peak current associated with the drive capability (see the following table)

IPeakTotal (mA) = SUMi (N_i x (Ipeak+ Istatic_i))

Table 7-2. Peak Current Parameters Per Type

Buffer Type	Ipeak outputs(mA)	Istatic (mA)	Ipeak inputs (mA)
IO25 outputs (Drive = 2.2, 4.5, 9.1, 13.6, 18.1) Type 01, 02, 04, 06, 08	3 x Drive	0	N/A
IO33 outputs (Drive = 2.7, 5.4, 10.8, 16.2, 21.6) Type 01, 02, 04, 06, 08	3 x Drive	0	N/A
IO50 outputs (Drive = 4.8, 4.9, 9.7, 19.3) Type 01, 02, 04, 08	3 x Drive	0	N/A
IO33 or IO25 inputs at 3.3V or 2.5V	N/A	—	2.5
IO50 inputs at 5V	N/A	—	2.68
PCI (pp33b01z, t01z, o01z)	56	0	N/A
LVDS reference (pl33refz)	0	0.4	0
LVDS transmitter (pl33txz)	5	6.0	N/A
LVDS receiver (plrxz, pl33rxrz)	0	3.0	5
PECL receiver (pe33rxz)	0	2.0	3.5

.....continued			
Buffer Type	**Ipeak outputs(mA)**	**Istatic (mA)**	**Ipeak inputs (mA)**
LVDS reference (pl25refz)	0	0.3	0
LVDS transmitter (pl25txz)	5	5.0	N/A
LVDS receiver (pl25rxz, pl25rxrz)	0	2.0	5
PECL receiver (pe25rxz)	0	1.5	3.5

Number of Buffer Supply Pairs
Np vdb/vsb = 1.4*max (Itot , IPeakTotal/3) / Ic

Where Itot and Ipeak are expressed in mA and Ic is the maximum allowed current per supply pad. The factor of 1.4 is a tentative to take into account potential non-linear repartition of currents in the periphery. The ultimate number of supply-pairs will be confirmed during the feasibility-study.

VDA and VSA Pairs for Buffers
The VDA and VSA supplies are also used in peripheral buffers to supply the VDA-to-VDB/VDB-to-VDA level shifters and core-oriented input triggers.

Buffer Type	VDA/VSA
IO33, PCI	1 pair for 16 buffers
LVDS/PECL buffers	1 pair for 8 buffers

The pad-oriented input-triggers are supplied with VCCB!

If the above-mentioned requirements are already fulfilled by respecting the “Array supply rules” no additional VDA/VSA pairs are needed. For double pad ring, see Buffers Description and Power Pads and ESD Cells.

Recommendations
To help ease the supply bounce problems related to simultaneous switching outputs:

- Use minimum drive output buffers necessary to achieve required speed
- Group input buffers together and output buffers together with supply pins between them. As input triggers ground is connected to VSS the crosstalk between input and output buffers is more through VCCB
- Add extra VDB/VSB pads pairs especially around critical clock signals
- See specific recommendations for LVDS buffers (“LVDS Cluster”) for which supplies may be used as shields between differential pairs
- Distribute the pairs as evenly as possible across the cluster:
  - Each supply pad current should not exceed the IC limit whether this pad is located inside or at an extremity of the cluster
  - This help to minimize the equivalent rail resistance from any buffer to the nearest VDB/VSB pair

Double bonding do not decrease VDB/VSB supply pairs count. VDB supply with or without power control has the same IC limit. For each type repartition, see Cluster.

7.2 SEE Mitigation

A general handbook/cookbook about “Techniques for Radiation Effects Mitigation in ASICs and FPGAs” can be found at https://escies.org/download/webDocumentFile?id=64426.

7.2.1 Hardened Flip-Flops

It is recommended to use hardened flip-flops rather than standard FF when possible for the first level of SEE protection. To the minimum pulse width on the clock input, a hardened flip-flop gives the first level of SEE protection.

7.2.2 Triple Modular Redundancy

Triple Modular Redundancy is a very efficient solution to cope with both SEU and SET errors. For SEU, TMR using standard FF is even more efficient than an SEU hardened flip-flop.

Using TMR with a triplicated clock tree dramatically decreases the occurrence of an SET event.

To be fully efficient, it is recommended to triplicate the reset tree as well, as it can be even more critical than the clock tree, as the minimum pulse width is rather small on the set and clear inputs of flips-flops.

7.2.3 Clock and Reset Trees (Microchip Responsibility)

As far as possible, the clock and reset trees must be built with cells having a significant drive. If a particular block of flip-flops must be protected, the clock tree must be built as much as possible of high-drive cells to minimize the number of combinatorial cells that could propagate SET pulses.

If possible, for gated clocks, use NOR cell rather NAND cell; OR cell rather than AND cell; low drive rather than strong.

XOR: Use xn02d4 rather than xn02d2

8. Revision History

Revision	Date	Description
A	03/2021	This document is updated for Rev A changes. Following is a list of changes made in this release: • Global improvement and adaptation of design-tools.
1.7	10/2019	Replace Atmel by Microchip, update flows, responsibilities, DK maturity-evolution
1.6 beta	06/2016	No more celtic (Foundation Flows for P&R) EDI replaces FE No more incremental SDF
1.5 beta	03/2015	Add acronym F in the pad naming convention Table 1 modified
1.4 beta	09/2014	Introduce IO50 buffers
1.3 beta	04/2014	Framemaker to word conversion Radiation evaluation on IO5V
1.2 beta	10/2013	Introduce NPI process Introduce Power Grid Verification
1.1 beta	06/2013	Update Chapter xx
1.0 beta	11/2012	Creation

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