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A Manual on ASIC Front to Back End Design Flow

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***Abstract*— This paper presents a manual that covers the necessary design steps for a basic ASIC design flow. It is shown how the manual writing process is organized such that each chapter covers a certain step in the design flow. The manual has been written especially with practicality in mind and has been successfully applied to under- and postgraduate teaching.**

I. Introduction

Teaching microelectronics at under- or postgraduate level puts high demands on students and teachers. Most electrical engineering students already know a traditional software programming language such as Java, C or C^{++}. However, the use of a hardware description language, in this case VHDL, requires a much broader background on, e.g. system architecture, hardware design, and implementation limitations. Moreover, tools such as a HDL simulator, a design compiler and a place and route (P&R) tool are required to complete the design chain. These tools are powerful in performance, and require some extensive user experience to achieve good results. A large amount of literature, databases, and manuals are available [1]–[5]. However, a beginner may have some difficulties in finding the appropriate media, whereas this broad variety is helpful for advanced and experienced designers. At the same time, the teacher has to keep an overview of the recent progress in technology, tools and supportive media. In order for the graduated students to be attractive to industry, the course material has to be updated according to the technology and EDA-tool progress pace, which is an administrative problem.

The Department of Electroscience at Lund Institute of Technology offers a *Digital IC Project & Verification* course that recently became part of the curriculum in the Swedish SoCware Master program [6]. Contrary to earlier years, the majority of course participants now has an international background and thus the previous knowledge in digital design is heterogeneous. Therefore, it is not longer sufficient to provide only the media that have been previously used when having students with a more predictable experience. Thus, the course organizers decided to provide a manual that is tailored to the needs and experiences of different course participants.

II. Manual Development

The authors of the manual are PhD students in the digital design group. The idea was to bring the knowledge among the PhD students to paper in a way such that it can be used for under- and postgraduate teaching. Existing knowledge gaps had to be filled as the chapters of the manual are intended to cover a technology independent ASIC design flow. Moreover, each chapter can be used independently from the preceding chapters. This allows the experienced reader to skip the parts they are already familiar with.

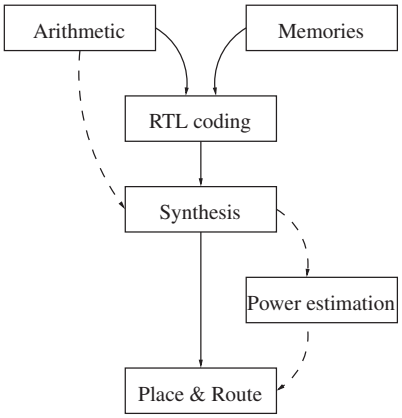

Fig. 1. Manual structure that follows a traditional ASIC design flow. The dashed lines show optional ways of using the manual.

The manual content was discussed in several meetings before assigning the different topics to a specific chapter. Each chapter was assigned to two authors in order to gain a better foundation of the material. After the first draft, the authors briefly presented the content of their chapter. On these occasions, the authors obtained valuable feedback that was taken into consideration in the continued writing process. Finally, each chapter was presented to the members of the digital design group as a lecture that also includes "hands-on" parts of the chapters where applicable, i.e., design examples were shown to the audience. This resulted in additional feedback, which was considered in the conclusive writing. Thereafter, the chapters were distributed among the authors for proofreading. The result is a manual of 150 pages that consists of 7 chapters.

III. Manual Content

Traditionally, the focus of books on digital hardware design is often limited to one area, e.g., signal processing, system level design, HDL, or arithmetic. The developed manual combines a range of topics that follow a common ASIC design flow, from code development to chip layout, see Fig. 1. The chapters cover issues that have to be taken into account before coding, e.g., arithmetic and memory concepts, as well as a

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hardware design methodology and pure technology-dependent steps, i.e., synthesis and P&R. How to carry out power estimation through simulation is taken up as an add-on in the last chapter. As indicated by the dashed lines in the figure, there are several ways of using the manual based on the experience and the demands of the reader. In the following paragraphs, intentions and contents of the chapters are presented.

A. Design methodology

For novices an introduction to VHDL is presented as well as basic concepts of describing and simulating digital hardware in a structured way. Moreover, it is shown how to develop platform independent code that supports several technologies such as reconfigurable logic and various cell libraries. However, this chapter is not a complete reference to the language itself, but more an overview and a selection of the most important parts of the language. References guide the interested reader to more advanced and thorough descriptions of the topic.

B. Arithmetic

Digital designs are often comprised of datapaths of various kinds and arithmetic is therefore an important topic. It is shown how to infer a component for an arithmetic operation in a digital design. The most commonly used arithmetic operations are presented and the connection between the VHDL description and the final hardware structure realized during synthesis is illustrated to increase understanding. This chapter gives the reader an overview on how to implement a highly effective hardware structure by coding and controlling the synthesis tool, in this case *Synopsys* Design Compiler.

C. Memories

Another important topic in digital ASIC design today is memories, i.e., not only the amount of memory but also the memory hierarchy, including caches and off-chip memories. Each memory hierarchy should be optimized for high speed, low power, small area, or a combination of these, dependent on the application. Since this is a too large topic to cover in a single chapter, three different design examples are chosen to illustrate possible optimizations to various memory structures.

D. Synthesis

Synthesis results highly depend on the coding style. Many designs with poor performance stem from a bad coding style. Thus, synthesis has to be understood so the designer is aware of her actions. This chapter gives an overview of the whole synthesis process and covers the basic synthesis concepts and guidelines for design optimization. It starts with the basic concept of what synthesis does, followed by example environment setups for synthesis, and wireload model basics. By describing the synthesis process, a better understanding of setting constraints is promoted.

E. Place & Route

P&R is the final step before sending the design for fabrication. Due to the non-trivial handling of the tool, in this case *Cadence* Silicon Ensemble, this chapter is described in a cookbook manner, i.e., the steps to be taken from a netlist to the final layout are listed step by step. For problems deviating from the described flow, one has to consult standard manuals. However, this design flow is approved by several successful designs.

F. Power estimation

Battery-driven devices and very high performance computers both rely on power-optimized hardware. Hence, it becomes increasingly important to estimate and eventually optimize power consumption in early stages of the design flow. This chapter gives an introduction to power estimation and optimization techniques in an ASIC design flow with *Synopsys* Power Compiler. Tool-independent optimization techniques are presented for different abstraction levels. It is also shown how the design tool interacts with information from the cell library and external simulation tools to estimate and optimize power at gate level.

IV. Laboratory Support

Various chapters include design examples which are provided as complete packages for verification purpose. This gives the user both an introduction to the topic wherefrom she can pursue and modify the examples for her own needs.

V. Experiences and Future Development

The manual is successfully tested as course literature in the *Digital IC Project & Verification* course [7]. Moreover, the chapter on P&R has been used for an external short-course organized by *Europractice* at *IMEC*, with participants from universities and companies throughout Europe having an experienced level in front-end digital design.

The content of each chapter will be updated continuously by experiences gained in the digital ASIC group. Currently, the transition from *Silicon Ensemble* to *SoCEncounter* in the P&R chapter is under progress. This update will also include an extraction for post-layout timing analysis.

Acknowledgment

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