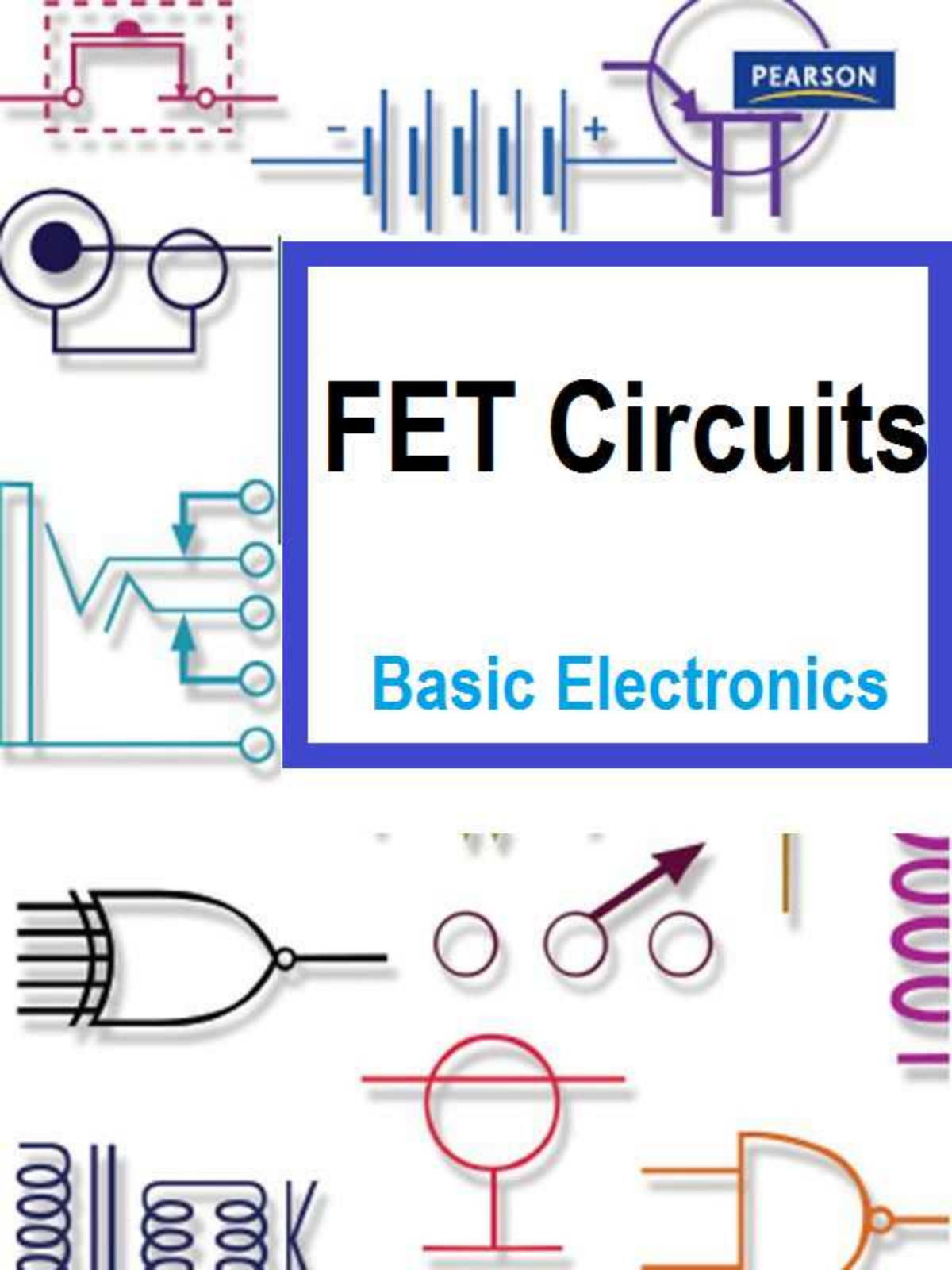

PEARSON
FET Circuits
Basic Electronics

7

FET Circuits

Outline

Objectives

This chapter begins with a discussion on the FET biasing technique and proceeds to formulate the working of the FET as an amplifier. AC equivalent circuit is provided for Small-signal analysis, and all possible kinds of problems are solved. After this, the high-frequency MOSFET model has been explained, followed by a discussion on a number of additional FET circuits supplemented with detailed theoretical investigations. Lastly, a comparison between the FET and the BJT is provided with a mapping of their respective advantages and disadvantages.

7-1 INTRODUCTION

The first modern day field-effect device was proposed and analysed by W. Shockley in 1952. The operational JFET was subsequently designed by Ross and Dancy in 1953. In the previous chapter we studied the basics of the FET as a three-terminal unipolar voltage-controlled device. Now let us move forward toward and understand the FET as an active circuit element. The various configurations of the FET, their corresponding features, and related operations will be examined.

Before we begin, a glance into the relative comparison between the BJT and the FET is required. One of the most important characteristics of the FET is its high input impedance. Contrary to this, the BJT has a much higher sensitivity to changes in the applied signal. In other words, the variation in the

output current is typically a great deal more for the BJT than for the FET for the same change in the input voltage. Generally, the FET is more thermally stable than the BJT, and is often of a smaller size than the BJT. Thus, the FET, especially the GaAs FET is used in core devices meant for very high-scale monolithic integrated circuits, such as the microwave.

7-2 FET BIASING

In the FET, the relationship between the input and output quantities is governed by the non-linear Shockley's equation. The current–voltage relationship can be written as:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (7\text{-}1)$$

In the case of the JFET and MOSFET, and also for the enhancement-type MOSFET, Eq. (7-1) gets modified as:

$$I_D = k(V_{GS} - V_T)^2 \qquad (7\text{-}2)$$

It is essential to note that these equations do not change with each network configuration as long as the device is being operated in the active region. The biasing assembly simply defines the level of current and voltage associated with the operating point through its own set of equations.

7-2-1 Fixed-Bias Arrangement

The FET fixed-bias arrangement is the simplest of all the biasing arrangements. The fixed-bias arrangement and its corresponding network for dc analysis are shown in Fig 7-1.

In Fig. 7-1(a), v_i and v_o are the input and output ac voltages, and C_1 and C_2 are the coupling capacitors. The coupling capacitors become open-circuited for the dc analysis, and have low impedance for the ac analysis. The resistor R_G ensures that for the ac analysis, the voltage V_i appears across the input source of the circuit.

For dc analysis, $I_g = 0$ A and $V_{RG} = I_g R_G = 0$ V. This zero voltage drop across the resistor enables us to replace the resistor R_G by a short, and hence, Fig. 7-1(b) is obtained. Thus, applying Kirchoff's law across the input loop, $V_{GS} = V_{GG}$. As the fixed supply is the dc voltage, and the voltage does not get divided anywhere, a fixed-bias configuration is obtained. Consequently, the drain current is given by:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (7\text{-}3)$$

which is the same as Eq. (7-1).

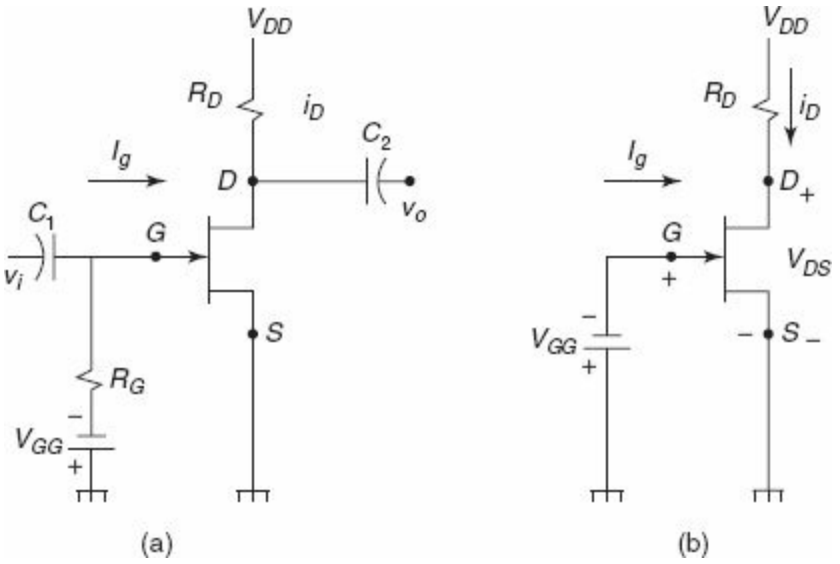


Figure 7-1 (a) Fixed-bias circuit (b) Corresponding network for dc analysis

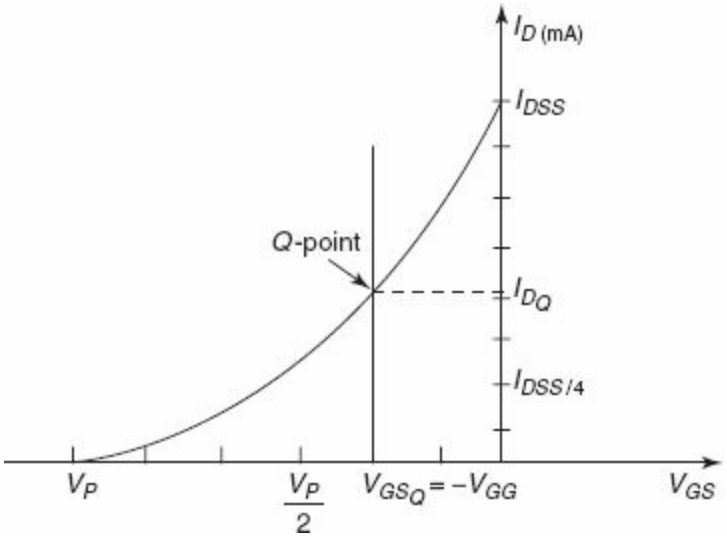


Figure 7-2 Shockley's equation and calculation of the operating point

Since the gate-to-source voltage in this case is a fixed quantity, the corresponding sign can be replaced in the above Shockley's equation, and the value of I_D can be calculated. If the drain current I_D [from Eq. (7-3)] is plotted against V_{GS}, we obtain the following curve as shown in Fig. 7-2.

Figure 7-2 shows that the operating Q-point can also obtained by simply superimposing the vertical line at $V_{GS} = -V_{GG}$. This intersection also gives the drain current I_{DQ} in the given situation.

7-2-2 Self-Bias Arrangement

The self-bias arrangement is a better biasing arrangement as it eliminates the need for two dc supplies. The controlling gate-to-source voltage is being determined by the voltage across the resistor R_s introduced in the series with the source of Fig. 7-3.

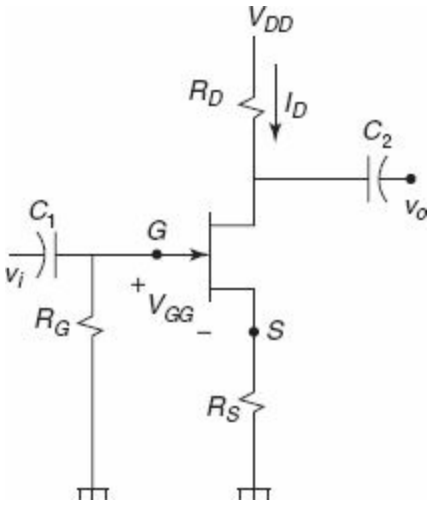


Figure 7-3 Self-bias arrangement

In case of dc analysis, the capacitors are replaced by open circuits and the circuit is modified, as shown in Fig. 7-4.

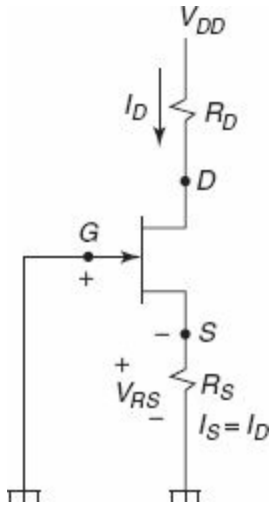


Figure 7-4 Simplified circuit for dc analysis

In Fig. 7-4, the current through the resistor at the source leg, R_S, is the drain current, for which the voltage drop across R_S is:

$$V_{R_s} = I_S R_S = I_D R_S \qquad (7\text{-}4)$$

Again, considering the loop including the gate and the drain in Fig. 7-4, we can write:

$$V_{GS} = -I_D R_S \qquad (7\text{-}5)$$

It is essential to note that the gate-to-source voltage V_{GS} is a function of the output current, and this is remarkably different in comparison to the fixed bias arrangement.

Applying Eq. (7-5) in Eq. (7-1), we obtain:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2 \qquad (7\text{-}6)$$

The solution of Eq. (7-6) leads to a quadratic equation which can be obtained for a solution of I_D. The operating point can be obtained by superimposing the characteristic curve and the expression for the gate-to-source voltage as obtained from Eq. (7-5). Thus, we obtain the curve as shown in Fig. 7-5. The Q-point is shown at the intersection point on the characteristic curve.

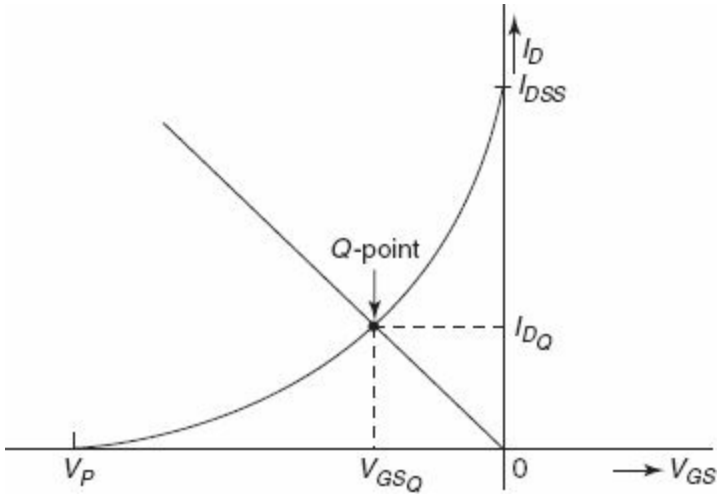


Figure 7-5 Sketch of the self-bias circuit along with the Q-point.

7-2-3 Voltage Divider Biasing Arrangement

The basic configuration in this case is the same as that applied for the BJT, although the dc analysis is quite different. The gate current for the FET is zero, but the magnitude of I_B for the common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. The circuit is as shown in Fig. 7-6.

For the dc analysis, the bypass capacitors included in the circuit should be replaced by an open circuit. The circuit is simplified for easy analysis. This enables us to find the Thevenin voltage V_G as:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \qquad (7\text{-}7)$$

Applying Kirchhoff's voltage law in the clockwise direction to the gate-source circuit, we obtain:

$$V_G - V_{GS} - V_{R_s} = 0 \qquad (7\text{-}8)$$

We can also write:

$$V_{GS} = V_G - V_{R_s} \qquad (7\text{-}9)$$

where, the value of V_{R_S} is expressed as:

$$V_{R_S} = I_S R_S = I_D R_S \qquad (7\text{-}10)$$

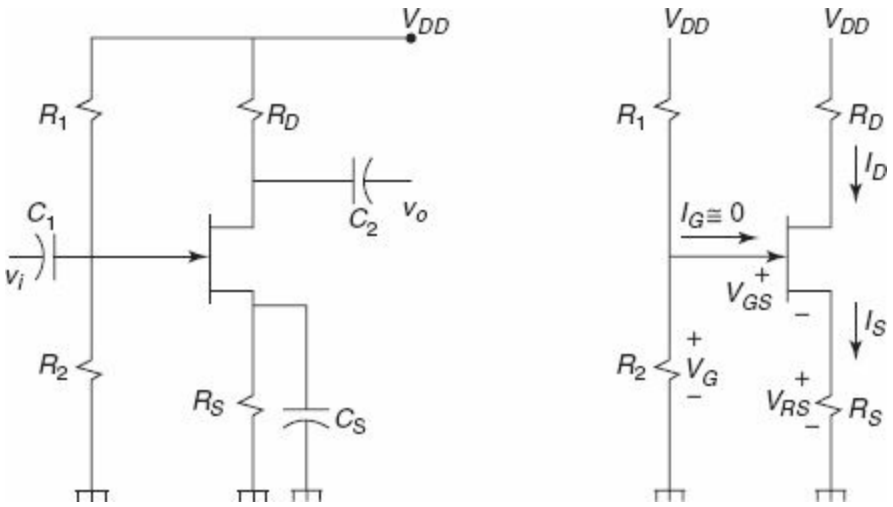


Figure 7-6 (a) Voltage divider bias circuits (b) Circuit for dc analysis

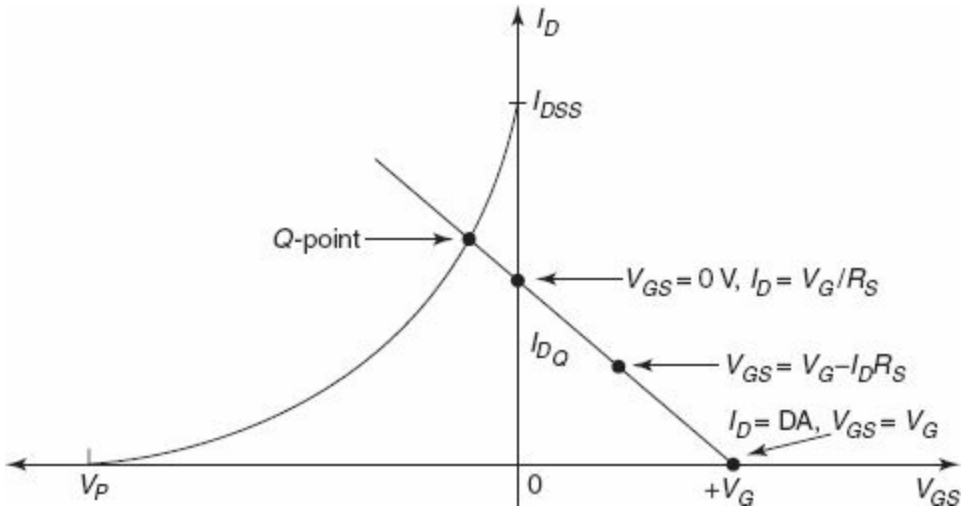


Figure 7-7 Determination of the Q-point for the voltage divider bias configurations

Therefore, by substituting the value of V_{R_S} from Eq. (7-10) in Eq. (7-9) we can write:

$$V_{GS} = V_G - I_D R_S \qquad (7\text{-}11)$$

An analysis of Eq. (7-11) reveals the fact that the equation includes the same variables that appear in the Shockley's equation. This also includes V_G and R_S which are determined by the network in consideration. Equation (7-11) is a relation of a straight line, and their points of intersection with the axis are found as follows:

For $I_D = 0$,

$$V_{GS} = V_G - 0 = V_G \qquad (7\text{-}12a)$$

and for, $V_{GS} = 0$,

$$I_D = \frac{V_G}{R_S} \qquad (7\text{-}12b)$$

Figure 7-7 shows the points of intersection and the subsequent determination of the Q-point from the graphical analysis for the voltage divider bias configurations.

7-3 FET AS AN AMPLIFIER

In this section, we shall study the operation of the FET as a common-source amplifier. This observation is made by considering an enhancement-type MOSFET biased by a dc voltage V_{GS}, with the time-varying input signal v_{gs} superimposed on it. The investigation begins with the calculation of the dc bias point.

7-3-1 DC Bias Point

To operate the MOSFET as an amplifier, it must be biased in the saturation region where we obtain a linear variation between the input voltage and the output voltage. The circuit for the study of MOSFET as an amplifier is shown in Fig. 7-8.

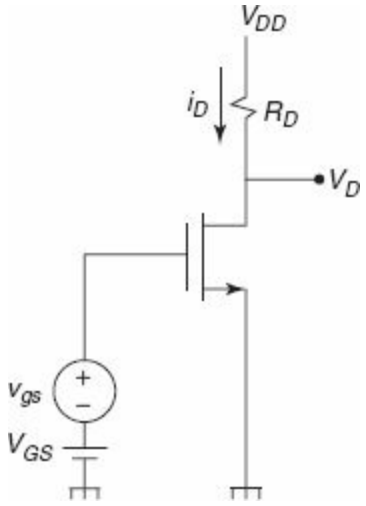


Figure 7-8 Circuit for the study of the MOSFET as an amplifier

With the input signal set to zero, the drain current can be expressed as:

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_T)^2 \qquad (7\text{-}13)$$

(neglecting the channel-width modulation).

Also from Fig. 7-8, we obtain the KVL for the output part of the circuit as:

$$V_D = V_{DD} - R_D I_D \qquad (7\text{-}14)$$

The condition that has to be maintained in order to keep the device operating in the saturation region is:

$$V_D > V_{GS} - V_T \qquad (7\text{-}15)$$

After considering the calculation of the dc bias point, the instantaneous drain current is given by:

$$\begin{aligned} i_D &= \frac{1}{2} k_n' \frac{W}{L} (V_{GS} + v_{gs} - V_t)^2 \\ &= \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 - k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} + \frac{1}{2} k_n' \frac{W}{L} v_{gs}^2 \end{aligned} \qquad (7\text{-}16)$$

In Eq. (7-16), we observe that the first term on the right hand side results in the dc bias current I_D. Now, comparing the second and the last terms, it is seen that the last term introduces an unwanted distortion, and thus, Eq. (7-16) can be equivalently written as:

$$i_D = I_D + i_d \qquad (7\text{-}17)$$

where, $i_d = k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$.

This is obtained only on the condition that:

$$\frac{1}{2} k_n' \frac{W}{L} v_{gs}^2 \ll k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

This results in:

$$v_{gs} \ll 2(V_{GS} - V_t) \qquad (7\text{-}18)$$

Thus, from the definition of transconductance, we obtain:

$$g_m \equiv \frac{i_d}{v_{gs}} = k_n' \frac{W}{L} (V_{GS} - V_t) \qquad (7\text{-}19)$$

7-3-2 Voltage Gain of the FET

Voltage gain of the FET is defined as the ratio of drain voltage (v_d) and gate-to-source voltage (v_{gs}), and is given by:

$$A_v = \frac{V_D}{V_{gs}} \qquad (7\text{-}20a)$$

The expression for the total instantaneous output voltage, obtained by considering the circuit as shown in Fig. 7-8, is given by:

$$v_D = V_{DD} - i_D R_D \qquad (7\text{-}20b)$$

Under the condition of small-signal analysis, substituting the value of i_d from Eq. (7-17), we get:

$$v_D = V_{DD} - (I_D + i_d)R_D \qquad (7\text{-}20c)$$

Equation (7-20c) can be approximated as:

$$v_D = V_D - R_D i_d \qquad (7\text{-}21)$$

Thus, the signal component of the drain voltage is:

$$v_d = -i_d R_D = -g_m R_D v_{gs} \qquad (7\text{-}22)$$

The negative sign indicates that the output drain voltage is exactly 180° out of phase with respect to the input signal. Thus, the voltage gain is given by:

$$A_v = \frac{V_D}{V_{gs}} = -g_m R_D$$

or,

$$A_v = -g_m R_D \qquad (7\text{-}23)$$

7-4 ELECTRICAL PARAMETERS OF THE FET

In the FET, the drain current is a function of the drain-to-source voltage and gate-to-source voltage. For small-signal analysis, the ac component of the drain current is expressed as a combination of the ac component drain-to-source voltage v_{ds}, and gate-to-source voltage v_{gs}, in the following way:

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_d} \qquad (7\text{-}24)$$

In Eq. (7-24), g_m represents the mutual conductance or transconductance, and the unit of g_m is mho or siemens or A/V. The g_m is expressed as a ratio of drain current to the corresponding gate-to-source voltage for constant drain-to-source voltage.

$$g_m = \frac{i_d}{v_{gs}}, \quad \text{for } v_{ds} = 0 \qquad (7\text{-}25)$$

In Eq. (7-24), r_d represents the ac resistance or channel resistance, and the unit is in ohms. It is the ratio of the drain-to-source voltage to the drain current for a constant gate-to-source voltage, and can be written as:

$$r_d = \frac{v_{ds}}{i_d}, \quad \text{for } v_{gs} = 0 \qquad (7\text{-}26)$$

The amplification factor is expressed as the ratio of v_{ds} to v_{gs} for a constant drain current, and is given by:

$$\mu = -\frac{v_{ds}}{v_{gs}}, \quad \text{for } i_d = 0 \tag{7-27}$$

μ is a positive quantity. Substituting $i_d = 0$ in Eq. (7-24), we can write:

$$-\frac{v_{ds}}{v_{gs}} = r_d g_m \tag{7-28a}$$

$$\mu = r_d g_m \tag{7-28b}$$

Therefore, the amplification factor of the FET is the product of channel resistance and transconductance.

7-5 AC EQUIVALENT CIRCUIT FOR SMALL-SIGNAL ANALYSIS

From the previous analysis it is observed that that the signal quantities are superimposed on the dc quantities. For instance, the total drain current i_D is given by the superimposition of two currents—the dc drain current I_D, and the small-signal current i_d. Similar is the case for the drain voltage v_D.

Upon examination, it is observed that the analysis becomes exceptionally simplified if the ac analysis is segregated from the dc analysis. In order to obtain some stable circuit configurations for their lucid analysis, the following circuit forms are studied.

7-5-1 Small-Signal Model for the MOSFET

If the circuit of an FET is considered from the signal point of view, it is found that the FET is basically a voltage-controlled current source. It provides a current of $g_m v_{gs}$ upon accepting a voltage of v_{gs} applied between the gate and the source terminal. The input impedance of this controlled source is very high. Also, the output resistance is high, and is ideally assumed to be infinite. Using all these factors together Fig. 7-9 is obtained.

In the analysis of the FET amplifier circuits, the FET is replaced by the ac equivalent circuit. The rest of the circuit, i.e., the circuit configuration is left unaltered, and the dc voltage sources are replaced with a short circuit. The reason behind this replacement is that the voltage across an ideal dc voltage source does not change, and thus, there will always be a zero voltage change at the output. Similar statements should be used for the dc current sources, but with the only difference that their equivalent replacement is an open circuit.

The severe deficiency of the above depicted small-signal representation is that it has been assumed that the drain current in saturation is independent of the drain voltage. Also, from previous study, it should be noted that the drain current depends on v_{DS} in a linear manner. Such dependence is easily depicted using the resistance r_o, whose value is given approximately by:

$$r_o \cong \frac{|V_A|}{I_D} \tag{7-29}$$

where, V_A is the applied voltage.

Besides, the small-signal model parameters g_m and r_o depend on the dc bias point. As done previously, we can write:

$$\frac{v_d}{v_{gs}} = -g_m(R_D \| r_o) \qquad (7\text{-}30)$$

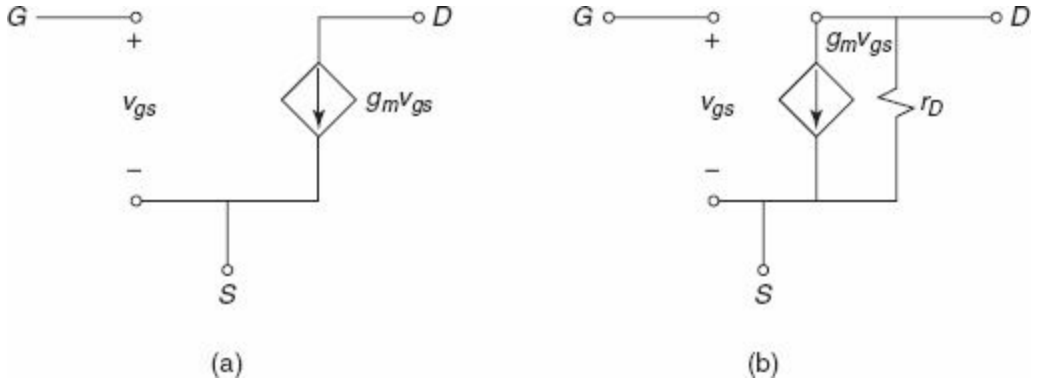


Figure 7-9 Small-signal models of MOSFET: (a) Neglecting channel length modulation (b) Including channel length modulation

FOR ADVANCED READERS

T Equivalent-Circuit Model

A simple circuit transformation of the equivalent-circuit model for the MOSFET is called the T model. The circuit is depicted in Fig 7-10.

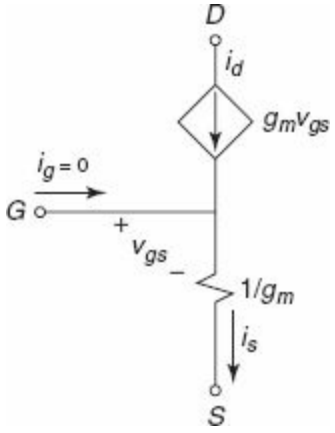


Figure 7-10 T equivalent-circuit model

At this stage it is advisable to look at the transformation of the circuit into an equivalent T circuit. This is explained in the following steps:

i. A second current source is added, i.e., $g_m v_{gs}$, in addition to the current source in series with the previous one. In doing so, we also make sure that the terminal currents are not changed, which ensures that we get an allowable transformation.
ii. The newly created circuit node is attached to the gate terminal as shown Fig. 7-10.
iii. It is notable that a controlled current source $g_m v_{gs}$ is connected across its control voltage v_{gs}.

iv. The controlled source is replaced by a resistance as long as an equal current flows through this resistance. Therefore, the value of the resistance is:

$$\frac{V_{gs}}{g_m V_{gs}} = \frac{1}{g_m}$$

The circuit with this replaced resistance is given in Fig. 7-11.

It is to be noted that in the development of the T model, we did not consider the inclusion of the resistance r_o in the circuit. If such a model is required, then the resistance r_o can be inserted between the drain and the source. Such a circuit is depicted in Fig. 7-12.

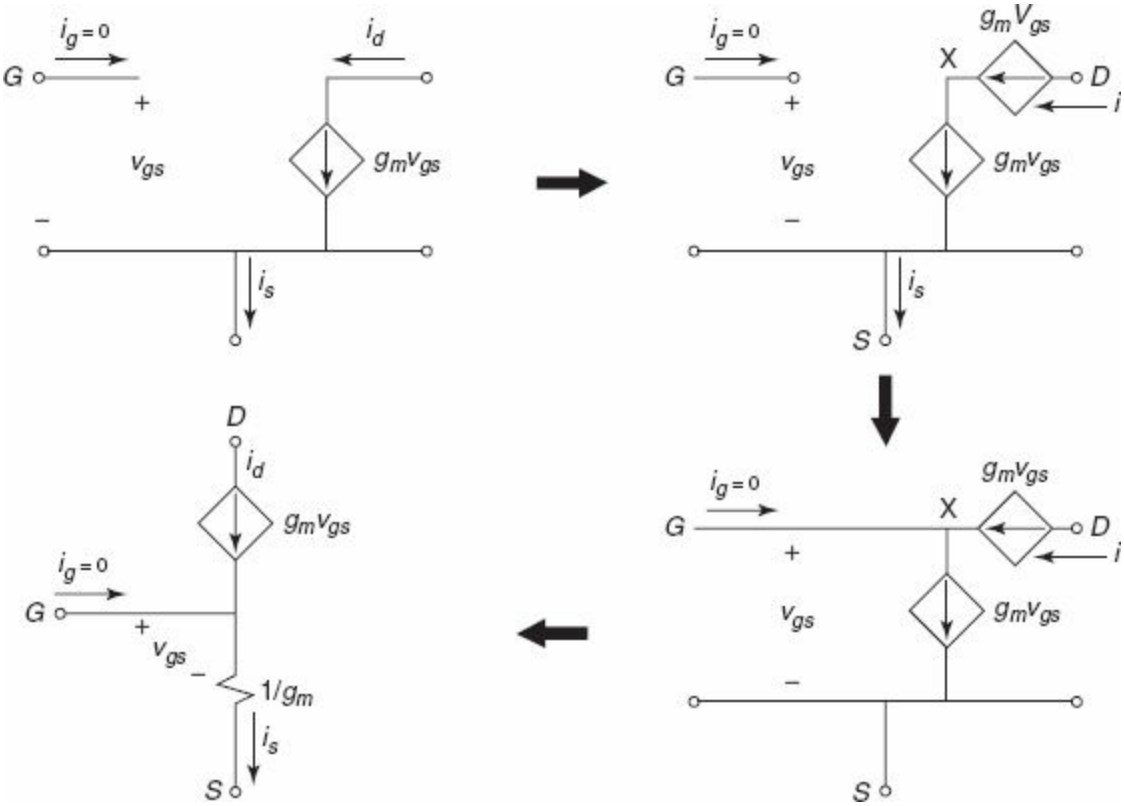


Figure 7-11 Conversion of small-signal model into T equivalent-circuit model

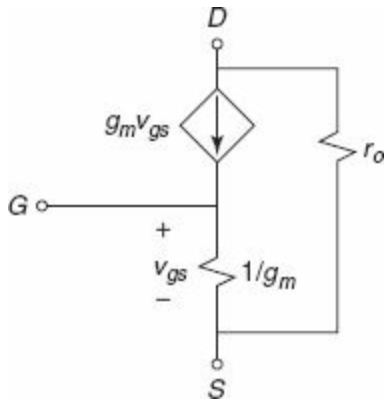
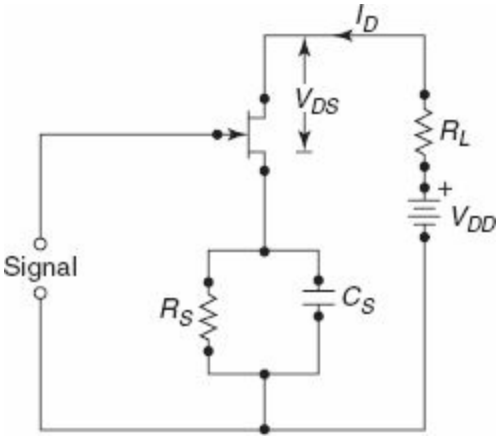


Figure 7-12 T model circuit along with the drain-to-source resistance r_o

Solved Examples

Example 7-1 Derive an expression for voltage gain for the FET amplifier, as shown in the diagram.



Solution:

The value of R_s can be determined from the following relation:

$$R_S = \frac{V_{GS}}{I_D}$$

where, V_{GS} = voltage drop across R_s

I_D = current through R_s

Voltage gain of the FET amplifier is:

$$A_V = \frac{\mu R_L}{r_D + R_L}$$

As,

$$\mu = r_d \times g_m$$

Substituting the value of μ, we get:

$$A_V = \frac{r_d g_m R_L}{r_d + R_L} = \frac{g_m R_L}{1 + \frac{R_L}{r_d}}$$

If $r_d >> R_L$

$$\frac{r_d}{R_L} >> 1 \quad \text{and} \quad \frac{R_L}{r_d} \to 0$$

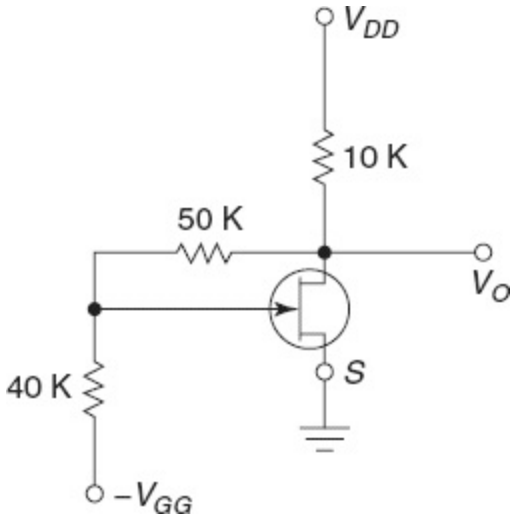
$\therefore$

$$A_V = \frac{g_m R_L}{1 + 0} = g_m R_L$$

or, $A = g_{fs} \times R_L$, i.e., the gain of the FET.

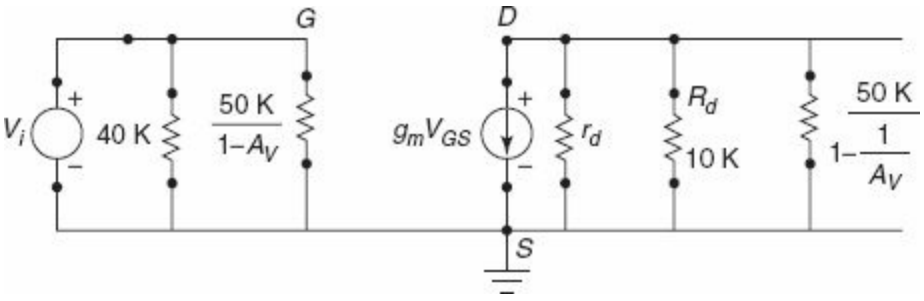
Example 7-2 If an input signal V_i is impressed between the gate and the ground, find the amplification

$A_v = V_0/V_i$. Apply Miller's theorem to the 50 K resistor. The FET parameters are $\mu = 30$ and $r_d = 5$ K. Neglect capacitances.



Solution:

Applying Miller's theorem to the 50 kΩ resistor, we obtain the following equivalent circuit.



The voltage gain of the amplifier, as calculated in Example 7-1, is given by:

$$A_V = \frac{-g_m}{\frac{1}{r_d} + \frac{1}{R_d} + \frac{1 - \frac{1}{A_V}}{R}} = -g_m$$

or,

$$A_V \left(\frac{1}{r_d} + \frac{1}{R_d} + \frac{1}{R} - \frac{1}{RA_V}\right) = -g_m$$

or,

$$A_V \left(\frac{1}{r_d} + \frac{1}{R_d} + \frac{1}{R}\right) = -g_m + \frac{1}{R}$$

or,

$$A_V\left(\frac{1}{5}+\frac{1}{10}+\frac{1}{50}\right)=-\frac{30}{5}+\frac{1}{50}=-\frac{299}{50}$$

$$A_V\left(\frac{16}{50}\right)=-\frac{299}{50} \quad \therefore \quad A_V=-\frac{299}{16}=-18.7$$

Example 7-3 If in Example 7-2, the signal V_i is impressed in series with the 40 kΩ resistor (instead of from gate to ground), find $A_V = V_o/V_i$.

Solution:
From Example 7-2, $A_V = -18.7$.
If the signal is impressed in series with the 40 kΩ resistor:

$$A_{VS}=\frac{A_V R_1}{R_1+40\text{ K}}$$

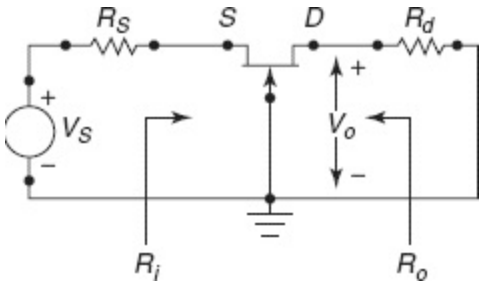
where,

$$R_1=\frac{50\text{ K}}{1+18.7}=2.54\text{ K}$$

Hence,

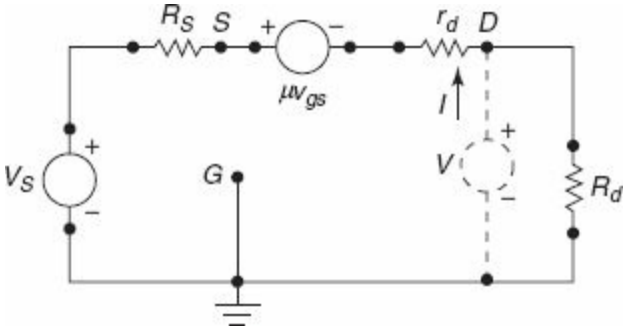
$$A_{Vs}=(-18.7)\frac{2.54}{1.54+40}=-1.11$$

Example 7-4 The circuit, as shown in the diagram, is called the common-gate amplifier. For this circuit, find (a) the voltage gain (b) the input impedance and (c) the output impedance. Power supplies are omitted for simplicity. Neglect capacitances.



Solution:

a. The small-signal equivalent circuit is shown in the following diagram.



Then,

$$V_{gs} = -V_s + IR_s \qquad (1)$$

Applying KVL around the loop we have:

$$V_S - \mu V_{gs} = I(R_S + r_d + R_d)$$

Now, substituting V_{gs} from Eq. (1), we have:

$$V_S(\mu + 1) = I[r_d + R_d + (\mu + 1)R_S]$$

or,

$$\frac{I}{V_s} = \frac{(\mu + 1)}{[r_d + R_d + (\mu + 1)R_s]} \qquad (2)$$

but,

$$V_o = IR_d$$

hence,

$$A_V = \frac{V_o}{V_s} = \frac{(\mu + 1)R_d}{[r_d + R_d + (\mu + 1)R_s]}$$

b. $R_i = \dfrac{V_s}{I} = R_s + \dfrac{R_d + r_d}{(\mu + 1)}$, where Eq. (2) has been used.

c. To find R_O we set $V_S = 0$, disconnect R_d and apply a voltage V between D and the ground. Then there exists a current I through the circuit, given by:

$$V + \mu V_{gs} = (r_d + R_S)I$$

but,

$$V_{gs} = -IR_S$$

$\therefore$

$$V - \mu R_S I = (r_d + R_S)I$$

or,

$$V = \mu R_S I + r_d I + R_S I$$

or,

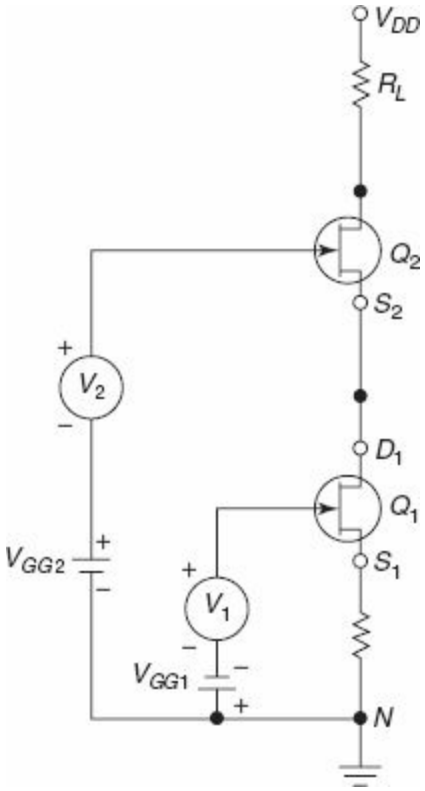
$$V = I[R_S\,(\mu + 1) + r_d]$$

or,

$$R_o = \frac{V}{I} = r_d + (\mu + 1) R_s$$

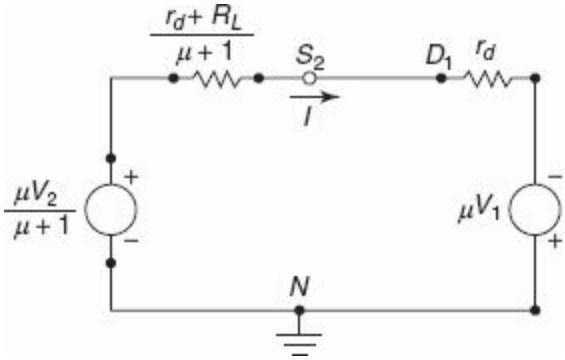
Example 7-5 Find an expression for the signal voltage across R_L. The two FETs are identical, with parameters μ, r_d and g_m.

Hint: Use the equivalent circuits for the generalized amplifier of a common drain arrangement at S_2 and D_1.



Solution:

Using small-signal equivalent circuit for FET Q_2 and for Q_1, we have the following figure.



Applying KVL around the loop, we obtain:

$$\frac{\mu V_2}{\mu + 1} + \mu V_1 = I\left[r_d + \frac{r_d + R_L}{\mu + 1}\right]$$

Solving for I, we obtain:

$$I = \frac{\mu}{(\mu + 2)r_d + R_L} V_2 + \frac{\mu(\mu + 1)}{(\mu + 2)r_d + R_L} V_1$$

but

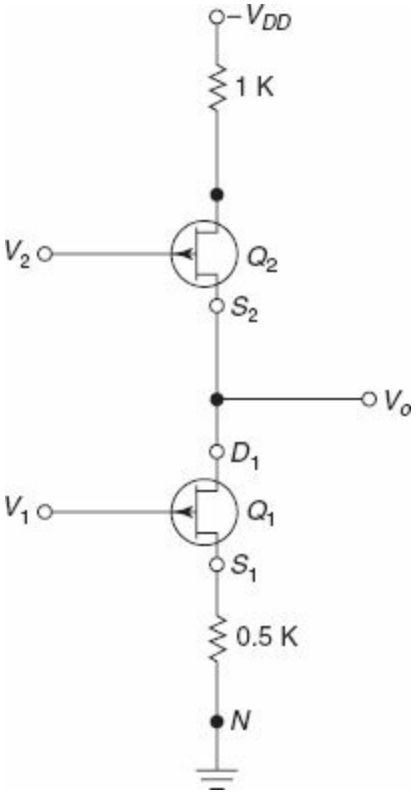
$$V_L = -IR_L$$

$\therefore$

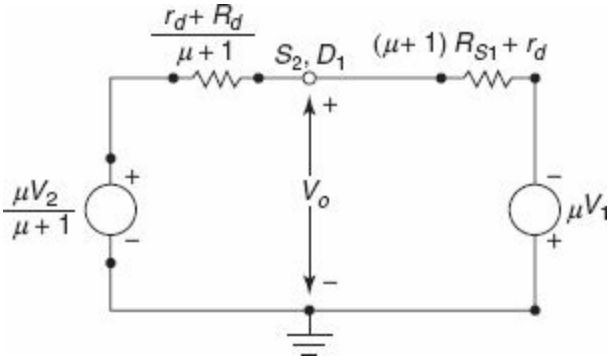
$$V_L = -\frac{\mu R_L}{(\mu + 2)r_d + R_L} [V_2 + (\mu + 1)V_1]$$

Example 7-6 Each FET, as shown in the diagram has parameters r_d = 15 K and g_m = 2mA/V. Using the equivalent circuits at S_2 and D_1, find the gain v_o/v_i under the conditions:

a. If $v_2 = 0$
b. If $v_1 = 0$



Solution:
Using super position we obtain:



$$v_o = \frac{\frac{R_d + r_d}{(\mu + 1)}(-\mu v_1) + [(\mu + 1)R_{s1} + r_d]\frac{\mu}{\mu + 1}v_2}{\frac{R_d + r_d}{\mu + 1} + (\mu + 1)R_{s1} + r_d}$$

a. If $v_2 = 0$:

$$\frac{v_o}{v_1} = \frac{-\mu(R_d + r_d)}{R_d + (\mu + 1)^2 R_{s1} + (\mu + 2)r_d}$$

$$= \frac{-30(16\ \text{K})}{(1 + 31^2 \times 0.5 + 32 \times 15)\text{K}}$$

$$= -\frac{480}{961.5} = -0.499$$

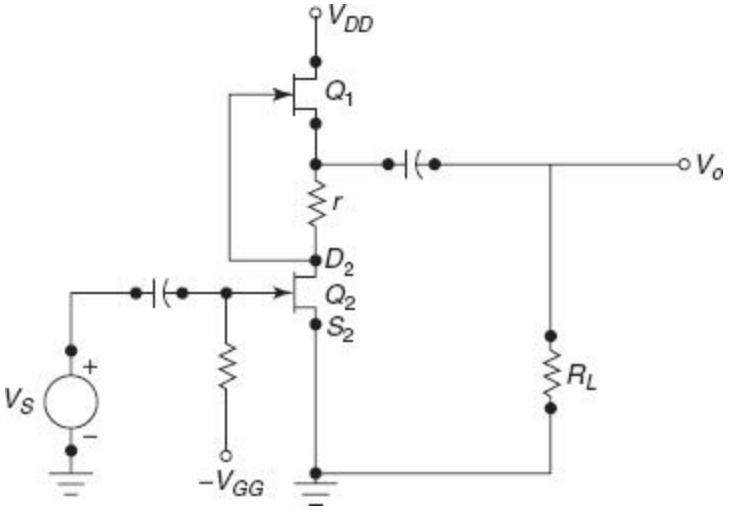
b. If $v_1 = 0$:

$$\frac{v_o}{v_2} = \frac{\frac{\mu}{\mu + 1}[(\mu + 1)R_{s1} + r_d]}{\frac{R_d + r_d}{\mu + 1} + (\mu + 1)R_{s1} + r_d}$$

$$= \frac{30 \times 0.5 + \frac{30 \times 15}{31}}{\frac{16}{31} + 31(0.5) + 15} = \frac{29.52}{31.02} = 0.952$$

Example 7-7 (a) Prove that, $r = 1/g_m + 2R_L/\mu$, provided that the magnitude of the signal current is the same in both the FETs. Neglect the reactance of the capacitors. (b) If r is chosen, as in part (a), prove that the voltage gain is given by:

$$A = \frac{-\mu^2}{\mu + 1}\frac{R_L}{R_L + \frac{r_d}{2}}$$



Solution:

a. If the equivalent circuit is under the condition that the signal current is the same in both FETs as indicated, KVL in loop 1 gives:

$$2IR_L + \mu V_{gs1} + Ir_d = 0$$

where,

$$V_{gs1} = -I_r$$

Thus,

$$I(2R_L + r_d) = I\mu r$$

or,

$$r = \frac{2R_L}{\mu} + \frac{1}{g_m}$$

b. KVL in loop 2 gives $(2R_L + r + r_d)I = \mu V_S$

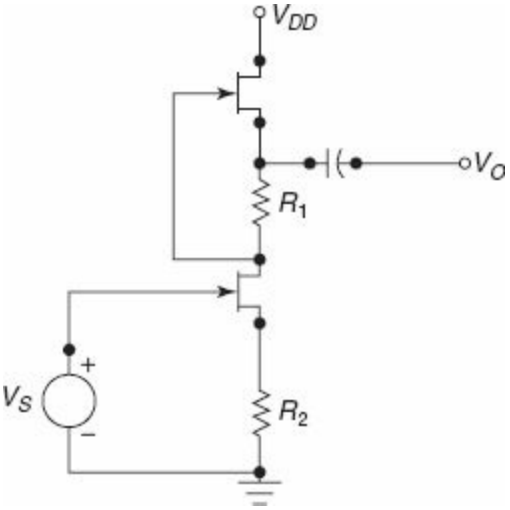
Hence,

$$A = \frac{V_o}{V_s} = \frac{2IR_L}{V_s} = -2R_L \frac{\mu}{2R_L + r + r_d}$$

Using the result of part (a), we obtain:

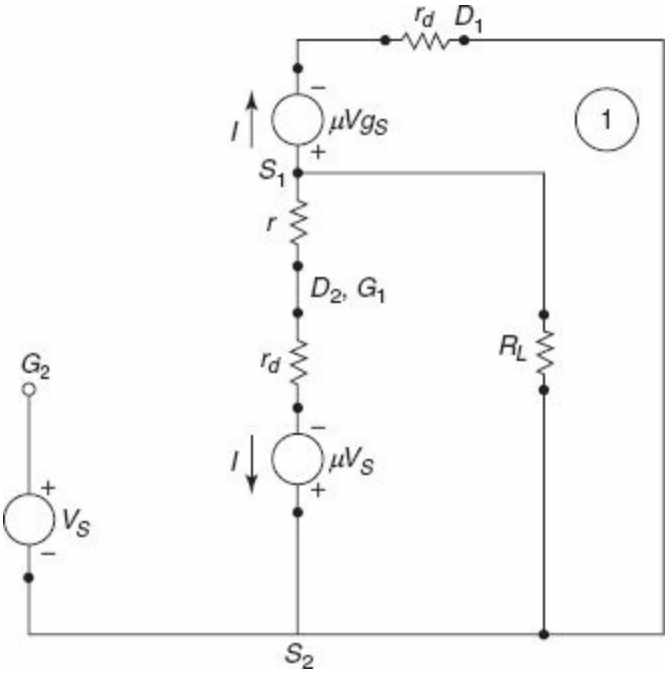
$$A = \frac{-2R_L\mu^2}{(\mu + 1)(2R_L + r_d)} = \frac{-\mu^2}{\mu + 1} \times \frac{R_L}{R_L + \frac{r_d}{2}}$$

Example 7-8 (a) If $R_1 = R_2 = R$ and the FETs have identical parameters, verify that the voltage amplification is $V_o/V_s = -\mu/2$, and the output impedance is $1/2\ [r_d + (\mu + 1)R]$. (b) Given $r_d = 62$ K, $\mu = 10$, $R_1 = 2$ K and $R_2 = 1$ K. Find the voltage gain and the output impedance.



Solution:

a. The small-signal equivalent circuit is shown in the following diagram.



KVL in the loop gives:

$$\mu V_{gs1} + \mu V_s = [2r_d + (\mu + 2)R]I$$

But,

$$V_{gs1} = -IR$$

Hence,

$$-\mu RI + \mu V_s = [2r_d + (\mu + 2)R]I$$

or,

$$I = \frac{\mu}{2[r_d + (\mu + 1)R]} V_s$$

We notice that, $V_o = -I(r_d + R) + \mu V_{gs1} = -I[r_d + (\mu + 1)R]$

Hence,

$$\frac{V_o}{V_s} = -\frac{\mu}{2}$$

To find the output impedance we ground D_1 and we have:

$$I_s = \frac{\mu V_s}{r_d + (\mu + 1)R}$$

For D_2 open circuit, we have exactly the V_o that we had found previously:

$\therefore$

$$V_o = -\frac{\mu}{2} V_s$$

Hence,

$$R_o = \frac{V_o}{I_s} = \frac{1}{2}[r_d + (\mu + 1)R]$$

b. In this case KVL around the loop gives:

$$\mu V_{gs1} + \mu V_S = I[2r_d + (\mu + 1)R_2 + R_1]$$

or,

$$-\mu R_1 I + \mu V_S = I[2r_d + (\mu + 1)R_2 + R_1]$$

or,

$$I = \frac{+\mu}{[2r_d + (\mu + 1)(R_2 + R_1)]} V_s$$

and,

$$V_o = -I(r_d + R_1) + \mu V_{gs1}$$

or,

$$V_o = -I[r_d + (\mu + 1)R_1]$$

Hence,

$$A = \frac{V_o}{V_s} = \frac{-\mu[r_d + (\mu + 1)R_1]}{[2r_d + (\mu + 1)(R_2 + R_1)]}$$

$$= \frac{-10(62 + 22)}{124 + 33} = \frac{-84}{157} \times 10 = -5.35$$

In this case:

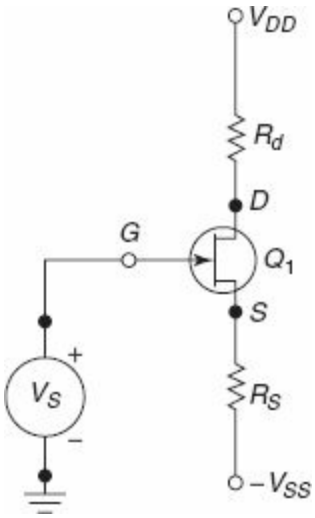
$$I_s = \frac{-\mu V_s}{r_d + (\mu + 1)R_2}$$

or,

$$R_o = \frac{V_o}{I_s} = \frac{V_o}{V_s} \times \frac{V_s}{I_s} = A \times \left[\frac{r_d + (\mu + 1)R_2}{-\mu}\right]$$

$$= 5.3 \times 7.3 \text{ K} = 39 \text{ K}$$

Example 7-9 (a) If in the amplifier stage, as shown in the diagram, the positive supply voltage V_{DD} changes by $\Delta V_{DD} = v_a$, how much does the drain-to-ground voltage change? (b) How much does the source-to-ground voltage change under the conditions as given in (a)?
(c) Repeat (a) and (b) if V_{DD} is constant, but V_{ss} changes by $\Delta V_{ss} = v_s$.



Solution:

a. The equivalent circuit of this amplifier is shown in the following diagram:

A voltage source is in series with R_d and $V_1 = 0$ (see diagram). KVL around the loop gives:

$$I = \frac{V_a}{R_d + r_d + (\mu + 1)R_s}$$

Notice,

$$V_{dn} = I[r_d + (\mu + 1)R_S]$$

or,

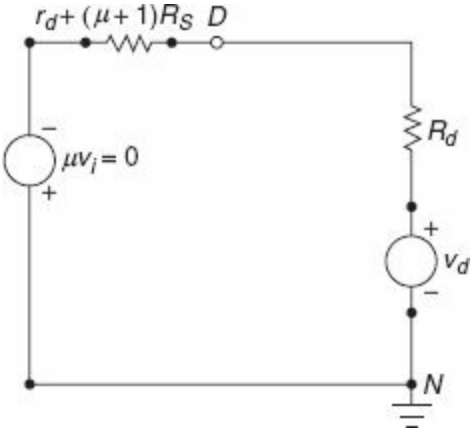
$$V_{dn} = \frac{r_d + (\mu + 1)R_s}{R_d + r_d + (\mu + 1)R_s} \times V_a$$

b. Also,

$$V_{sn} = I(\mu + 1)R_S$$

Hence,

$$V_{sn} = \frac{(\mu + 1)R_s}{R_d + r_d + (\mu + 1)R_s} \times V_a$$



c. The equivalent circuit is given in with a source in series with R_S and $v_1 = 0$:

Hence,

$$I = \frac{(\mu + 1)V_s}{R_d + r_d + (\mu + 1)R_s}$$

Now,

$$V_{dn} = R_d \times I$$

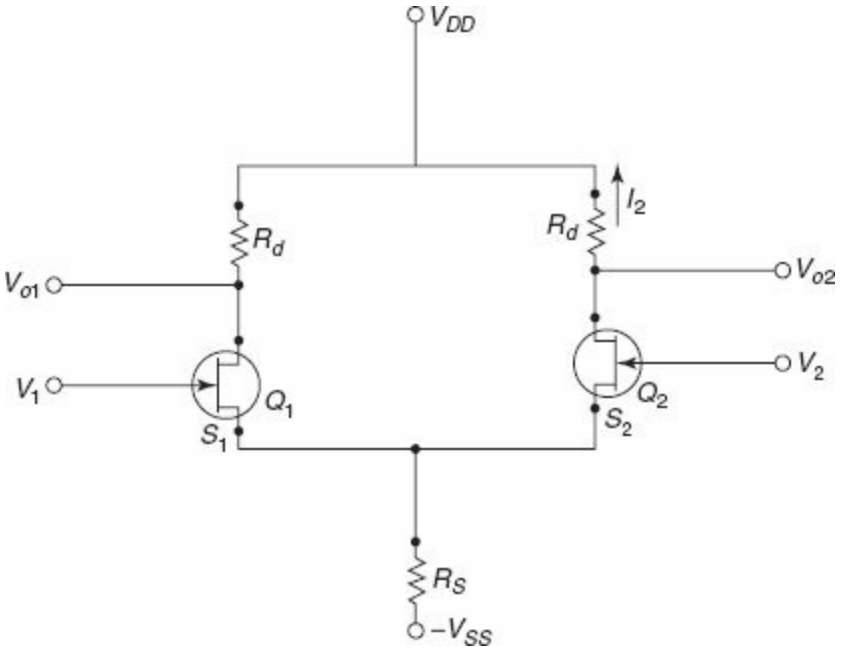
or,

$$V_{dn} = \frac{(\mu + 1)R_d}{R_d + r_d + (\mu + 1)R_s}V_s$$

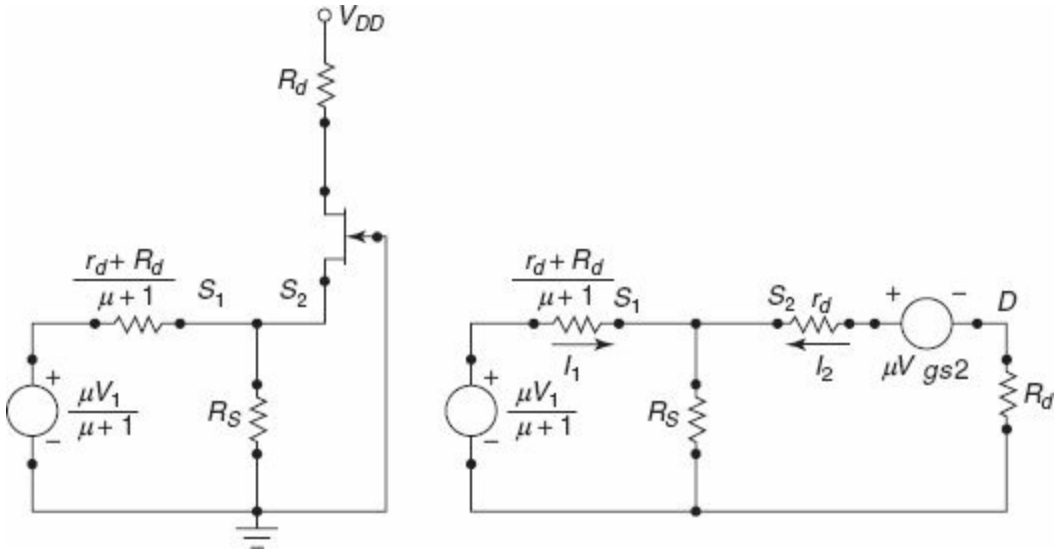
Similarly,

$$V_{sn} = (r_d + R_d)I = \frac{(\mu + 1)(r_d + R_d)}{R_d + r_d + (\mu + 1)R_s}V_s$$

Example 7-10 If in the circuit, as shown in the diagram, $V_2 = 0$, then this circuit becomes a source-coupled phase inverter, since $V_{o1} = -V_{o2}$. Solve for the current I_2 by drawing the equivalent circuit, looking into the source of Q_1 hen replace Q_2 by the equivalent circuit, looking into its drain. The source resistance R_s may be taken to be arbitrarily large.



Solution:



We note that:

$$V_{gs2} = -\frac{\mu}{\mu + 1}V_1 + \frac{r_d + R_d}{\mu + 1}I_1$$

Also, since R_s is arbitrarily large, $I_1 = -I_2$.
Applying KVL around the loop we have:

$$I_1\left(\frac{r_d + R_d}{\mu + 1} + r_d + R_d\right) = \frac{\mu}{\mu + 1}V_1 + \frac{\mu^2}{\mu + 1}V_1 - \frac{\mu}{\mu + 1}(r_d + R_d)I_1$$

or,

$$I_1 \times 2(r_d + R_d) = \mu V_1$$

Hence,

$$I_1 = \frac{\mu V_1}{2(r_d + R_d)} = -I_2$$

but,

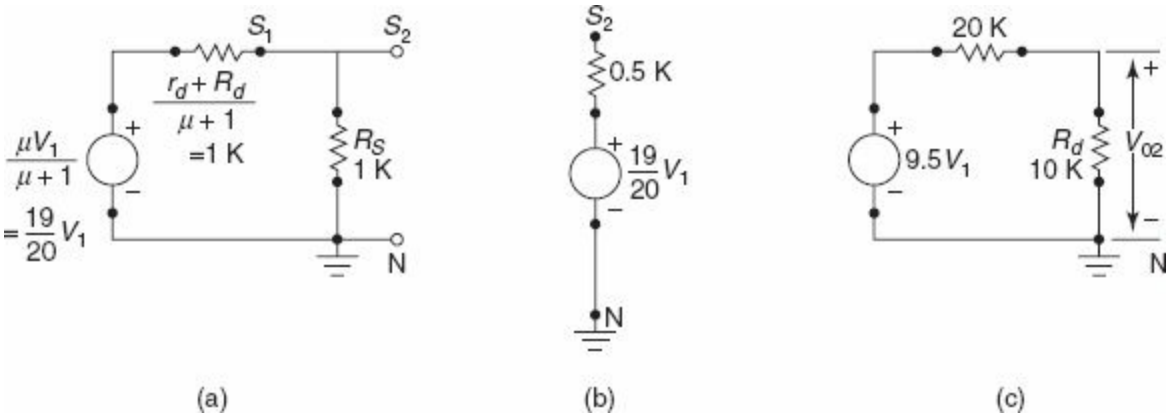
$$V_{o1} = -I_1 \times R_d = \frac{-\mu R_d}{2(r_d + R_d)} V_1$$

and,

$$V_{o2} = -I_2 R_d = \frac{\mu R_d}{2(r_d + R_d)} V_1$$

Example 7-11 In the circuit of Example 7-10, assume that $V_2 = 0$, $R_d = r_d = 10$ K, $R_s = 1$ K and $\mu = 19$. If the output is taken from the drain of Q_2, find (a) the voltage gain, (b) the output impedance.

Solution:



a. Looking into the source S_1 we see the equivalent circuit, as shown in Fig. (a). The Thevenin equivalent of S_2 is indicated in Fig. (b). Looking into D_2 we see the circuit in Fig. (c), from which:

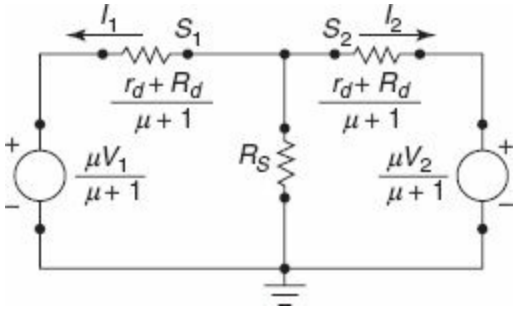
$$A = \frac{V_{o2}}{V_1} = \frac{9.5 \times 10}{10 + 20} = 3.17$$

b. From Fig. (c), $R_o' = 10 \text{ K} \parallel 20 \text{ K} = \dfrac{20 \times 10}{30} = 6.67 \text{ K}$

Example 7-12 In the circuit of Example 10, $V_2 \neq V_1$, $R_d = 30$ K, $R_s = 2$ K, $\mu = 19$, and $r_d = 10$ K. (a) Find the voltage gain A_1 and A_2 defined by $V_{o2} = A_1 V_1 + A_2 V_2$. (b) If R_s is arbitrarily large, show that $A_2 = -A_1$. Note that the circuit now behaves as a different amplifier.

Solution:

a. The equivalent circuit as seen upon looking into the sources of the FETs is as shown in the following diagram.



KVL in loop 1 and 2 respectively, gives:

$$-\frac{\mu}{\mu+1}V_1 = \left(\frac{r_d + R_d}{\mu+1} + R_s\right) I_1 + R_s I_2$$

$$-\frac{\mu}{\mu+1}V_2 = I_1 R_s + \left(\frac{r_d + R_d}{\mu+1} + R_s\right) I_2$$

Solving for I_2 we obtain:

$$I_2 = \frac{\frac{-\mu}{\mu+1}\left(\frac{r_d + R_d}{\mu+1} + R_s\right)}{\left(\frac{r_d + R_d}{\mu+1}\right)\left(\frac{r_d + R_d}{\mu+1} + 2R_s\right)} V_1 + \frac{R_s \frac{\mu}{\mu+1}}{\left(\frac{r_d + R_d}{\mu+1}\right)\left(\frac{r_d + R_d}{\mu+1} + 2R_s\right)} V_2$$

But, $V_{o2} = R_d I_2$

Hence,

$$A_1 = \frac{-\mu[r_d + R_d + (\mu+1)R_s]R_d}{(r_d + R_d)[r_d + R_d + 2(\mu+1)R_s]}$$

Hence,

$$A_2 = \frac{\mu(\mu+1)R_s R_d}{(R_d + r_d)[R_d + r_d + 2(\mu+1)R_s]}$$

For the given values of R_d, R_S, r_d and μ we have:

$$A_1 = \frac{-19 \times 80 \times 30}{40 \times 120} = -9.5$$

and,

$$A_2 = \frac{19 \times 20 \times 30 \times 2}{40 \times 120} = 4.75$$

b. If $R_S \to \infty$, then

$$A_1 = \frac{-\mu(\mu+1)R_d}{2(\mu+1)(r_d + R_d)}$$

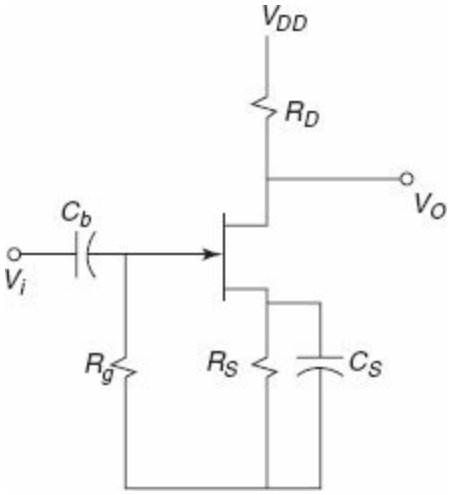
$$= \frac{-\mu R_d}{2(r_d + R_d)} = -A_2$$

or,

$$A_1 = -A_2 = -7.14$$

Example 7-13 The common source mode amplifier stage shown in the diagram has the following

parameters: $R_d = 12$ K, $R_g = 1$ M, $R_s = 470\Omega$, $V_{DD} = 30$ V, C_S, is arbitrarily large, $I_{DDS} = 3$ mA, $V_p = -2.4$ V and $r_d >> R_d$. Determine (a) the gate-to-source bias voltage V_{GS}, (b) the drain current I_D, (c) the quiescent voltage V_{DS} and (d) the small-signal voltage gain A_V.



Solution:

a. From the basic equation of the JFET:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

where, from the given diagram:

$$V_{GS} = -I_D R_S$$

or,

$$V_{GS} = -I_{DSS} R_s \left(1 - \frac{V_{GS}}{V_P}\right)^2 = -3 \times 0.47 \left(1 + \frac{V_{GS}}{2.4}\right)^2$$
$$= -1.41\left(1 + \frac{2V_{GS}}{2.4} + \frac{V_{GS}^2}{2.4^2}\right)$$

Upon solving, we get $V_{GS} = -0.7$ V

b. $I_D = 3\left(1 - \frac{0.7}{2.4}\right)^2 = 3\left(\frac{1.7}{2.4}\right)^2 = 1.5\,\text{mA}$

c. $V_{DS} = V_{DD} - I_D(R_d + R_s) = 30 - 1.5 \times 12.47 = 11.25$ V

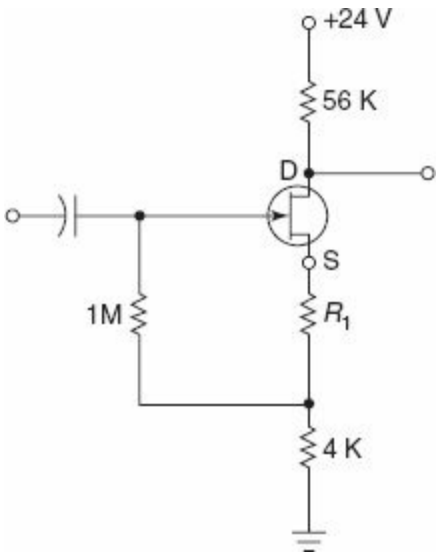
d. Since $r_d >> R_d$, $A_V = -g_m R_d$ where, we have:

$$g_m = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)$$
$$= \frac{2 \times 3 \times 10^{-3}}{2.4}\left(1 - \frac{0.7}{2.4}\right)$$
$$= 1770\,\mu\text{mho} = 1.77\,\text{mA/V}$$

Hence,

$$AV = -1.77 \times 12 = 21.2$$

Example 7-14 The amplifier stage, as shown in the diagram, uses an *n*-channel FET having $I_{DSS} = 2$ mA and $V_P = -1$ V. If the quiescent drain-to-ground voltage is 10 V, find R_1.



Solution:
From the circuit given in the diagram:

$$I_D = \frac{V_{DD} - V_{DN}}{R_d} = \frac{24 - 10}{56} = 0.25\,\text{mA}$$

$$= I_{DDS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2(1 + V_{GS})^2$$

or,

$$1 + V_{GS} = \left(\frac{1}{8}\right)^{\frac{1}{2}} = 0.35$$

$\therefore$

$$V_{GS} = -0.65\text{ V}$$

but,

$$V_{GS} = -I_D R_1$$

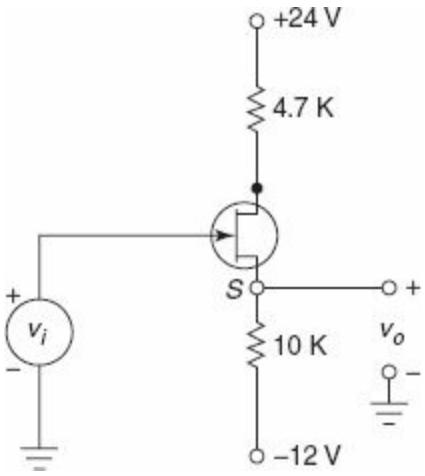
or,

$$R_1 = -\frac{V_{GS}}{I_D} = \frac{0.65}{0.25 \times 10^{-3}} = 2.6\text{ K}$$

Example 7-15 The FET, as shown in the diagram, has the following parameters: $I_{DSS} = 5.6$ mA and $V_P = -4$ V.

a. Find v_o, if $v_i = 0$
b. Find v_o, if $v_i = 10$ V
c. Find v_i, if $v_o = 0$

NOTE: v_i and v_o are constant voltages (and not small-signal voltages)



Solution:

KVL in the G–S loop gives:

$$v_i = V_{GS} + 10i_d - 12$$

or,

$$i_d = \frac{v_i + 12 - V_{GS}}{10}$$

a. If $v_i = 0$:

$$i_d = \frac{12 - V_G}{10} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 5.6\left(1 + \frac{V_{GS}}{4}\right)^2 = 5.6\left(1 + \frac{V_{GS}}{2} + \frac{V_{GS}^2}{16}\right)$$

Solving, we obtain $V_{GS} = -2$ V and $i_d = 1.4$ mA.

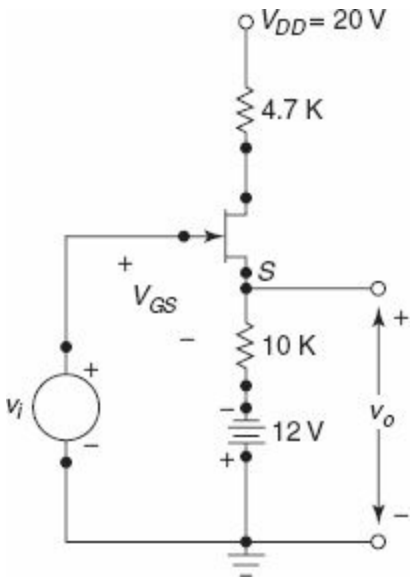
$\therefore v_o = 10i_d - 12 = 14 - 12 = 4$ V

b. If $v_i = 10$ V:

$$i_d = \frac{v_i + 12 - V_{GS}}{10} = 2.2 - \frac{V_{GS}}{10}$$

$$= 5.6\left(1 + \frac{V_{GS}}{2} + \frac{V_{GS}^2}{16}\right)$$

or, $V_{GS} \approx -1.4$ v, $i_d = 2.43$ mA



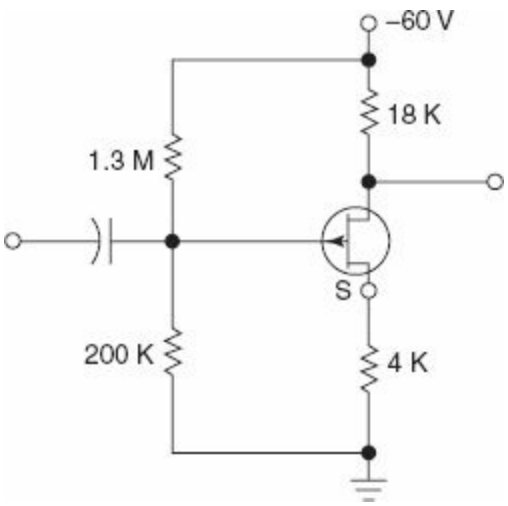
c. If $v_0 = 0$, $i_d = \dfrac{12\text{ V}}{10\text{ K}} = 1.2\text{ mA} = 5.6\left(1 + \dfrac{V_{GS}}{4}\right)^2$

or,

$$\left(1 + \frac{V_{GS}}{4}\right)^2 = \frac{1.2}{5.6} = 0.214,\ V_{GS} = -2.15\text{ V}$$

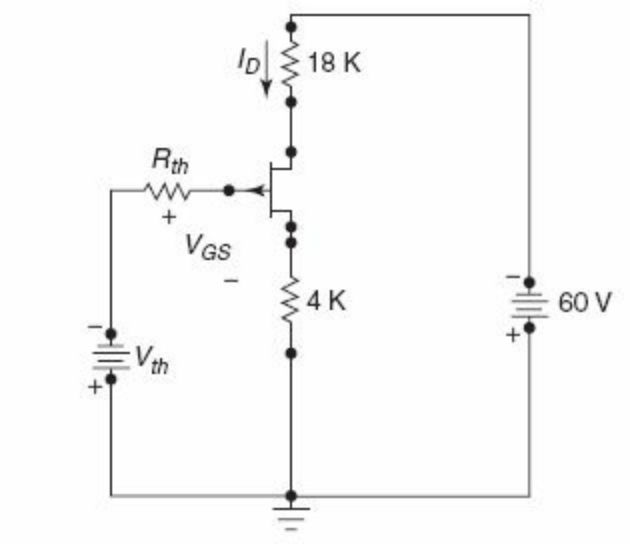
Then, $v_i = V_{GS} = -2.15$ V

Example 7-16 If $|I_{DSS}| = 4$ mA, $V_P = 4$ V, calculate the quiescent values of I_D, V_{GS} and V_{DS}.



Solution:

If we find Thevenin's equivalent to the left of the gate of the given circuit, we obtain the circuit as shown in the following diagram:



where, R_{TH} = 200K‖ 1.3 M = 173.5 K

and,

$$-V_{Th} = \frac{200\,\text{K}}{1500\,\text{K}}(-60) = -8\,\text{V}$$

KVL in the G–S loop gives:

$$V_{GS} = -4\text{I}_\text{D} - 8 \text{ or } I_D = -\frac{8 + V_{GS}}{4} = -2 - \frac{V_{GS}}{4}$$

$$= I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = -4\left(1 - \frac{V_{GS}}{4}\right)^2$$

Solving, we get:

$$V_{GS} = 1\text{V and } I_D = -2.25\text{ mA}$$

Hence,

$$V_{DS} = -60 + (18 + 4)\,(2.25)$$

$$= -60 + 49.5$$

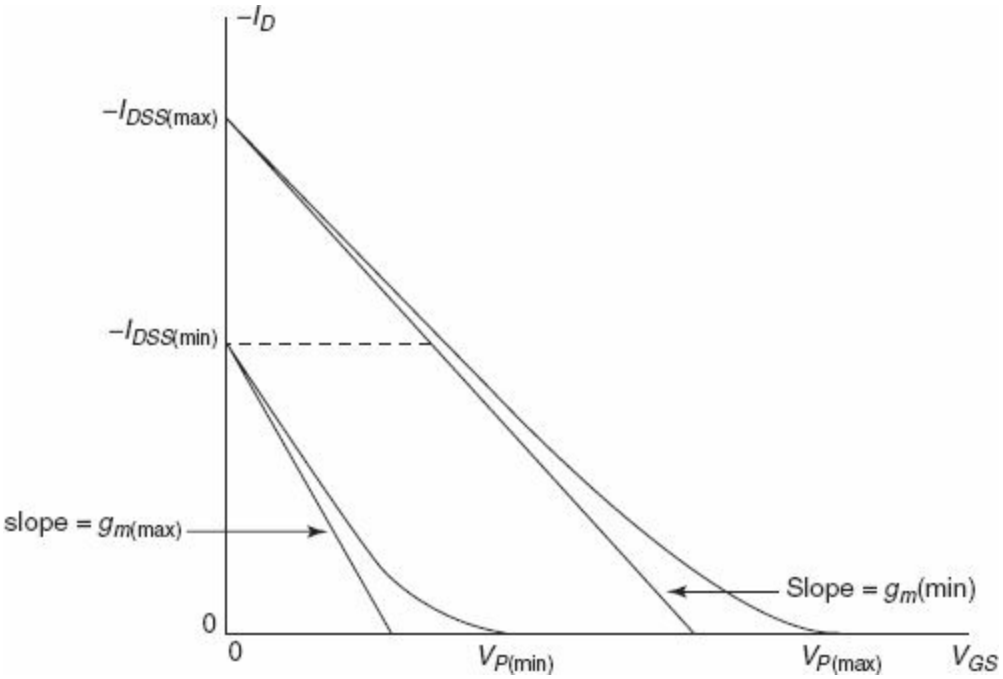
$$= -10.5\text{ V}$$

Example 7-17 In the given diagram, two extreme transfer characteristics are indicated. The values of $V_{P(\text{max})}$ and $V_{P(\text{min})}$ are difficult to determine accurately. Hence, these values are calculated from the experimental values of $I_{DSS(\text{max})}$, $I_{DSS(\text{min})}$, $g_{m(\text{max})}$, and $g_{m(\text{min})}$ measured at a drain current corresponding to $I_{DSS(\text{min})}$. Verify that:

a. $V_{P(\text{max})} = -\frac{2}{g_{m(\text{min})}}(I_{DSS(\text{max})} I_{DSS(\text{min})})^{\frac{1}{2}}$

b. $V_{P(\min)} = -\dfrac{2I_{DSS,(\min)}}{g_{m(\max)}}$

c. If for a given FET, $I_{DSS}(\min) = 1.5$ mA, $I_{DSS}(\max) = 8$mA, $g_m(\min) = 1.4$ mA/V and $g_m(\max) = 3.5$ mA/V, evaluate $V_P(\max)$ and $V_P(\min)$.



Solution:

a. The basic equation of transconductance is given by:

$$\left[g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = -\frac{2}{V_P}(I_{DSS} I_{DS})^{1/2}\right]$$

Applying this to the upper curve we have:

$$g_{m(\min)} = -\frac{2I_{DSS(\max)}}{V_{P(\max)}}\left(1 - \frac{V_{GS}}{V_{P(\max)}}\right)$$

where, V_{GS} corresponds to $I_D = I_{DSS(min)}$ or $I_D = I_{DSS(min)} = I_{DSS(max)}$

From,

$$\left(1 - \frac{V_{GS}}{V_{P(\max)}}\right): \qquad V_{GS} = V_{P(\max)}\left(1 - \sqrt{\frac{I_{DSS(\min)}}{I_{DSS(\max)}}}\right)$$

Substituting, we have:

$$g_{m(\min)} = \frac{-2I_{DSS(\max)}}{V_{P(\max)}}\left(1 - 1 + \sqrt{\frac{I_{DSS(\min)}}{I_{DSS(\max)}}}\right)$$

or,

$$V_{P(\max)} = \frac{-2I_{DSS(\max)}}{g_{m(\min)}}\left(\sqrt{\frac{I_{DSS(\min)}}{I_{DSS(\max)}}}\right)$$
$$= \frac{-2}{g_{m(\min)}}\left(I_{DSS(\max)} \times I_{DSS(\min)}\right)^{\frac{1}{2}}$$

b. For the lower curve $g_{m0} = \frac{-2I_{DSS}}{V_P}$ becomes:

$$g_{m(\max)} = \frac{-2I_{DSS(\min)}}{V_{P(\min)}}$$

or,

$$V_{P(\min)} = \frac{-2I_{DSS(\min)}}{g_{m(\max)}}$$

c.

$$V_{P(\max)} = \frac{-2}{1.4}(8 \times 1.5)^{\frac{1}{2}} = -4.95\,\text{V}$$
$$V_{P(\min)} = \frac{-2 \times 1.5}{3.5} = -0.86\,\text{V}$$

Example 7-18 In the circuit, as shown in the diagram, the FET is used as an adjustable impedance element by varying the dc bias, and thereby the g_m of the FET.

a. Assume that there is a generator V between the terminals A and B. Draw the equivalent circuit. Neglect inter-electrode capacitances.
b. Show that the input admittance between A and B is:

$$Y_i = Y_d + (1 + g_m R)Y_{CR}$$

where, Y_d is the admittance corresponding to r_d, and Y_{CR} is the admittance corresponding to R and C in series.
c. If $g_m R >> 1$, show that the effective input capacitance is:

$$C_i = \frac{g_m \alpha}{\omega(1 + \alpha^2)}$$

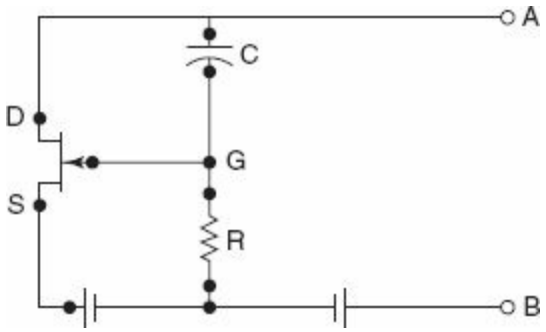
and the effective input resistance is:

$$R_i = \frac{(1 + \alpha^2)r_d}{1 + \alpha^2(1 + \mu)}$$

where, $\alpha \equiv \omega CR$.
d. At a given frequency, show that the maximum value of C_i (with either C or R is varied) is obtained when $\alpha = 1$ and $(C_i)_{\max} = g_m/2\omega$. Also show that the value of R_i corresponding to this C_i is:

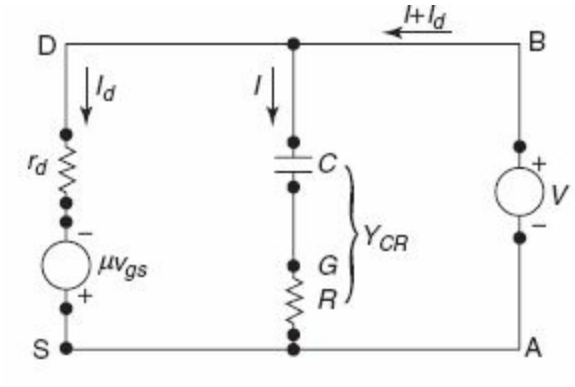
$$(R_i)_{\max} = \frac{2r_d}{2 + \mu}$$

which, for $\mu >> 2$, is reduced to $(R_i)_{\max} = 2/g_m$



Solution:

a. Using the small-signal equivalent circuit we have:



b. $I_d = \dfrac{V + \mu V_{gs}}{r_d}$, but $V_{gs} = I_R$ and $I = V \times Y_{CR}$

Hence, $V_{gs} = VY_{CR} \times R$

$$I_d = \left(\frac{1}{r_d} + g_m R Y_{CR}\right) V$$

but,

$$Y_1 V = I + I_d = \left(Y_{CR} + \frac{1}{r_d} + g_m R Y_{CR}\right)$$

or,

$$Y_1 = Y_d + (1 + g_m R) Y_{CR}$$

c. Since $g_m R >> 1$, we have:

$$Y_1 = Y_d + g_m R \frac{1}{R - j\left(\frac{1}{\omega C}\right)}$$

$$= \frac{1}{rd} + \frac{g_m R^2}{R^2 + \left(\frac{1}{\omega^2 C^2}\right)} + j \frac{g_m \left(\frac{R}{\omega C}\right)}{R^2 + \left(\frac{1}{\omega^2 C^2}\right)} = G_1 + j\omega C_1$$

Hence,

$$\omega C_1 = \frac{g_m RC\omega}{1 + (\omega RC)^2} = \frac{g_m \alpha}{1 + \alpha^2} \text{ or } C_1 = \frac{g_m a^2}{(1 + \alpha^2)\omega}$$

also,

$$G_1 = \frac{1}{r_d} + \frac{g_m\omega^2C^2R^2}{\omega^2C^2R^2 + 1} = \frac{1}{r_d} + \frac{a^2}{1 + a^2} = \frac{1 + (1 + r_dg_m)a^2}{r_d(1 + a^2)}$$

Hence,

$$R_1 = \frac{1}{G_1} = \frac{(1 + a^2)r_d}{1 + a^2(1 + \mu)}$$

d. For ω = constant, C_1 is a function of α, hence:

$$\frac{dC_1}{d\alpha} = \frac{g_m\omega(\alpha^2 + 1) - 2\alpha^2g_m\omega}{\omega^2(1 + \alpha^2)^2} = 0$$

or, $\alpha^2 = 1$ or $\alpha = 1$, since α is always greater than zero.,

also,

$$\frac{d^2C_1}{d\alpha^2} = \frac{-2g_m\omega^2\alpha(\alpha^2 + 1)^2 - g_m\omega^2(1 - a^2)2(1 + \alpha^2) \times 2\alpha}{\omega^2(1 + \alpha^2)^2} \quad (< 0 \text{ for } \alpha < \sqrt{3})$$

Hence, for $\alpha = 1$:

$$(C_1)_{\max} = \frac{g_m}{2\omega}$$

and, follows that:

$$(R_1)_{\max} = \frac{2r_d}{2 + \mu}$$

Example 7-19 Solve Example 7-18 if the capacitance C is replaced by an inductance L.

Solution:

If we replace C with L in Example 7-18 (a), we obtain:

$$Y_1 = Y_d + (1 + g_mR)Y_{LR}$$

where,

$$Y_{LR} = \frac{1}{R + j\omega L}$$

Hence,

$$Y_1 = G_1 + j\omega C_1 = \frac{1}{r_d} + \frac{g_mR^2}{R^2 + \omega^2L^2} - j\frac{g_mRL}{R^2 + \omega^2L^2}$$

which gives,

$$j\omega C_1 = -j\frac{\omega g_mRL}{R^2 + \omega^2L^2}$$

But then Y_1 is a parallel combination of a conductance G_1 and inductance L_1 and:

$$Y_1 = G_1 - j\,\frac{1}{\omega L_1}$$

or,

$$\frac{1}{\omega L_1} = \frac{\omega g_m RL}{R^2 + \omega^2 L^2}$$

or,

$$L_1 = \frac{R^2 + \omega^2 L^2}{\omega^2 g_m RL} = \frac{1 + \omega^2 \frac{L^2}{R^2}}{\omega g_m \left(\frac{\omega L}{R}\right)}$$

If we say:

$$\frac{\omega L}{R} = \alpha$$

$$L_1 = \frac{1 + \alpha^2}{\omega g_m \alpha}$$

then,

$$G_1 = \frac{r_d g_m R^2 + R^2 + \omega^2 L^2}{(R^2 + \omega^2 L^2) r_d} = \frac{\mu + 1 + \alpha^2}{(1 + \alpha^2) r_d}$$

$$R_1 = \frac{(1 + \alpha^2) r_d}{\mu + 1 + \alpha^2}.$$

For ω constant, L_1 is a function of α hence [for $(L_1)_{\max}$] we find:

$$\frac{dL_1}{d\alpha} = \frac{2\omega g_m \alpha^2 - \omega g_m (1 + \alpha^2)}{\omega^2 g_m \alpha^2} = 0$$

or,

$$\alpha = 1 \text{ and } (L_1)_{\max} = \frac{2}{\omega g_m}$$

For $\alpha = 1{:}1$

$$(R_1)_{\max} = \frac{2 r_d}{\mu + 2}$$

Example 7-20 For a constant drain-to-source voltage, if the gate-to-source voltage is changed from 0 to −2 V, the corresponding change in the drain current becomes 2 mA. Calculate the transconductance of the FET if the ac drain resistance is 200 K. Also calculate the amplification factor of the FET.

Solution:
Transconductance is given by:

$$g_m = \left.\frac{i_d}{v_{gs}}\right|_{v_{ds}=0}$$

hence, $g_m = \frac{2}{2} = 1$ mA/V

again, $\mu = g_m r_d = 1 \times 10^{-3} \times 200 \times 10^3 = 200$, which is the amplification factor.

Example 7-21 Calculate the dynamic resistance of a JFET having an amplification factor of 80 and transconductance 400 μmho.

Solution:
Using the formula $\mu = g_m r_d$, we have:

$$80 = 400 \times 10^{-6} \times r_d \Rightarrow r_d = 0.2 \times 10^6 \text{ ohm}$$

Example 7-22 The following data were obtained in an experiment with an FET:

V_{GS}(Volt)	0	0	0.3
V_{DS}(VoIt)	6	16	16
I_D(mA)	12	12.3	12

Calculate: (a) ac drain resistance, (b) transconductance and (c) amplification factor.

Solution:

a. AC drain resistance:

$$r_d = \left.\frac{v_{ds}}{i_d}\right|_{v_{ds}=0}$$

$\therefore$

$$r_d = \left.\frac{16-6}{12.3-12}\right|_{v_{gs}=0} = \frac{10}{0.3} = 3.33 \text{ k}\Omega$$

b. Transconductance is given by:

$$g_m = \left.\frac{i_d}{v_{gs}}\right|_{r_{ds}=0}$$

$$g_m = \left.\frac{i_d}{v_{gs}}\right|_{r_{ds}=0} = \frac{12.3-12}{0-0.3} = \frac{0.3}{-0.3} = 1 \text{ (neglecting the sign)}$$

c. Amplification factor is given by:

$$\mu = g_m r_d$$

$$\mu = 3.33 \times 1 = 3.33$$

Example 7-23 The Q-point of a JFET in a source self-bias arrangement is chosen at $V_{GS} = -1.5$ V and $I_{Dsat} = 2$ mA. Find the value of the resistance R_S.

Solution:
We have:

$$R_S = \frac{|V_{GS}|}{|I_{Dsat}|} = \frac{1.5}{2 \times 10^{-3}} \text{Ohm} = 750 \text{ Ohm}$$

Example 7-24 An FET amplifier in the common-source configuration uses a load resistance of 250 kΩ and the transconductance is 0.5 mA/V. What is the voltage gain of the amplifier? Given $r_d = 200$ kΩ.

Solution:

The voltage gain is:

$$A_V = -\frac{\mu R_L}{r_d + R_L}$$

Here, $r_d = 200$ kΩ, $g_m = 0.5$ mA/V and $R_L = 250$ kΩ.
We have:

$$\mu = r_d g_m = 200 \times 0.5 = 100$$

Hence,

$$A_V = -\frac{100 \times 250}{100 + 250} = -71.42$$

Example 7-25 An n-channel JFET has $I_{DSS} = 10$ mA and pinch-off voltage $V_p = -4$ V. Find the drain current for $V_{GS} = -2$ V. If the transconductance g_m of the JFET with the same I_{DSS} at $V_{GS} = 0$ is 4 millimho, find the pinch-off voltage.

Solution:
We know that:

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The transconductance is:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}\bigg|_{V_{DS}=\text{const.}} = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$$

Clearly, $g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$ is the value of g_m when $V_{GS} = 0$

Here $I_{DSS} = 10$ mA, $V_P = -4$ V, $V_{GS} = -2$ V, and $g_{mo} = 4$ mS.
Substituting these values, we obtain:

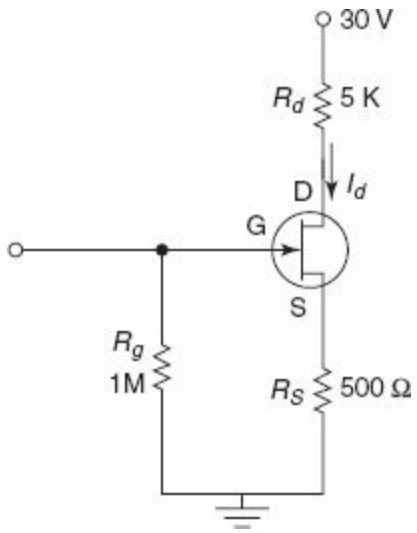
$$I_{DS} = 10\left(1 - \frac{2}{4}\right)^2 = 2.5 \text{ mA}$$

$$V_P = -\frac{2I_{DS}}{g_{mo}} = -\frac{2 \times 10}{4} = -5 \text{ V}$$

Example 7-26 The drain current of a JFET, as shown in the diagram, is given by:

$$I_D = 20\left(1 + \frac{V_{GS}}{4}\right)^2 \text{ mA}$$

Calculate the quiescent values of I_D, V_{DS} and V_{GS}.



Solution:
We know that:

$$I_D = I_{DS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Therefore, by comparison, we get $I_{DS} = 20$ mA and $V_p = -4$ V.
The gate-source voltage V_{GS} is equal to voltage drop across R_S:

$$V_{GS} = -I_D \times 500\ \Omega = -I_D \times 0.5 \text{ K}$$

Substituting the values of I_{DS}, V_p and V_{GS} we get:

$$I_D = 20\left(1 + \frac{-0.5\,\text{K}\,I_D}{4}\right)^2$$

$$= 20\,(1 - 0.125\,I_D)^2$$

$$= 20\,[(1) - (2 \times 1 \times 0.125)\,I_D + (0.125)^2\,I_D^2]$$

or,

$$I_D = 20 - 5\,I_D + 0.3125\,I_D^2$$

or,

$$0.3125\,I_D^2 - 6\,I_D + 20 = 0$$

$\therefore$

$$I_D = \frac{-(-6) \pm \sqrt{(-6)^2 - 4 \times 0.3125 \times 20}}{2 \times 0.3125}$$

$$= \frac{6 \pm \sqrt{36 - 25}}{0.625} = \frac{6 \pm 3.31}{0.625}$$

$\therefore$

$$I_D \text{ is either, } \frac{6 + 3.31}{0.625} = 14.9 \text{ mA}$$

or,

$$\frac{6 - 3.31}{0.625} = 4.3 \text{ mA}$$

Out of these two values, I_D = 14.9 mA is physically absurd because I_D ($R_d + R_s$), i.e., 14.9 mA (5 K + 0.5 K) = 81.95 volts.
This is more than the supply voltage. We shall only consider I_D = 4.3 mA.

$\therefore$

$$V_{GS} = -I_D \times 0.5\text{ K} = -4.3 \times 0.5 = -2.15\text{ V}$$

and

$$V_{DS} = V_{DD} - I_D\,(R_d + R_s)$$

$$= 30 - 4.3\text{ mA}\,(5\text{ K} + 0.5\text{ K})$$

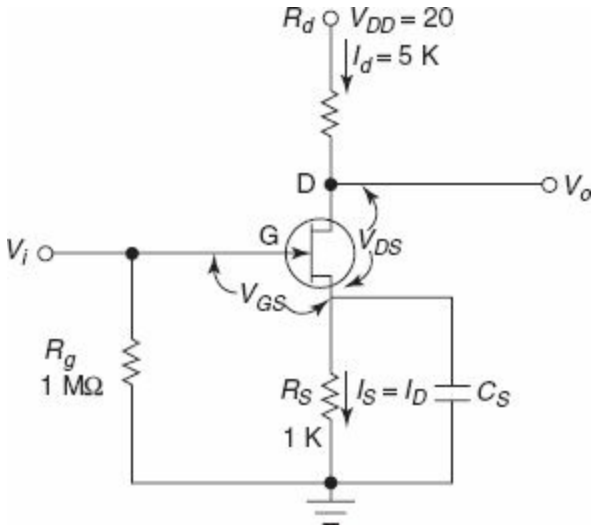
$$= 30 - 23.65\text{ V}$$

$$= 6.35\text{ V}$$

Example 7-27 The diagram shows an FET amplifier circuit. If the FET has I_{DSS} = 3 mA, V_p = −2.4 V

and $r_d >> R_d$, calculate:

a. Quiescent values of I_D, V_{DS} and V_{GS}
b. Voltage gain A_v



Solution:

$$0.52\, I_D^2 - 3.5\, I_D + 3 = 0$$

or,

$$I_D^2 - 6.73\, I_D + 5.76 = 0$$

$\therefore$

$$I_D = \frac{6.73 \pm \sqrt{(6.73)^2 - 4 \times 1 \times 5.77}}{2}$$

$$= 5.72 \text{ mA or } 1.01 \text{ mA}$$

We have,

$$V_{GS} = -I_D \times R_S$$

$$= -I_D \times 1 \text{ K}$$

We know that the drain current:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Substituting the given values of I_{DSS} and V_p, we get:

$$I_D = 3 \times \left[1 - \frac{V_{GS}}{(-2.4)}\right]^2 \text{ mA}$$

$$= 3 \times \left(1 + \frac{V_{GS}}{2.4}\right)^2$$

Substituting the equation of I_D we get:

$$I_D = 3 \times \left(1 - \frac{I_D \times 1\text{K}}{2.4}\right)^2$$

$$= 3 \times \left[1 - \frac{2}{2.4} I_D + \left(\frac{1}{2.4}\right)^2 I_D^2\right]$$

$$= 3 - 2.5\, I_D + 0.52\, I_D^2$$

a. The possible value is $I_D = 1.01$ mA

$\therefore$

$$V_{GS} = -I_D R_S = -1.01 \times 1\text{ K} = -1.01\text{ V}$$

and,

$$V_{DS} = V_{DD} - I_D R_S - I_D R_d$$

$$= 20 - I_D (R_S + R_d)$$

$$= 20 - 1.01 \times (1\text{ K} + 10\text{ K}) = 8.89\text{ V}.$$

b. The voltage gain $A_v = -g_m (Rd \parallel rd)$
Since it is given that $r_d >> R_d$, therefore, r_d can be ignored for $(R_d \parallel r_d)$ value. Taking magnitude only $|A_V| = |g_m . R_d|$ the value of g_m is:

$$g_m = \frac{2}{V_p}\sqrt{I_D I_{DSS}}$$

$$= \frac{-2}{-2.4}\sqrt{1.01\text{ mA} \times 3\text{ mA}}$$

$$= \frac{2}{2.4}\sqrt{3.03}\text{ mA/V}$$

$$= 1.45\text{ mA/V} = 1.45\text{ mA/V}$$

$\therefore$

Voltage gain $|A_v| = 1.45 \times 10 = 14.5$

Example 7-28 A common source FET amplifier with unbypassed R_s has the following circuit parameters: $R_d = 15$ K, $R_g = 1$ M, $r_d = 5$ k, $g_m = 5$m and $V_{DD} = 20$ V. Calculate A_v, Z_o and Z_i.

Solution:
Using the given values we can find:

$$\mu = r_d g_m = 5\text{ K} \times 5\text{ mho} = 25$$

The expression for A_v and R_o:

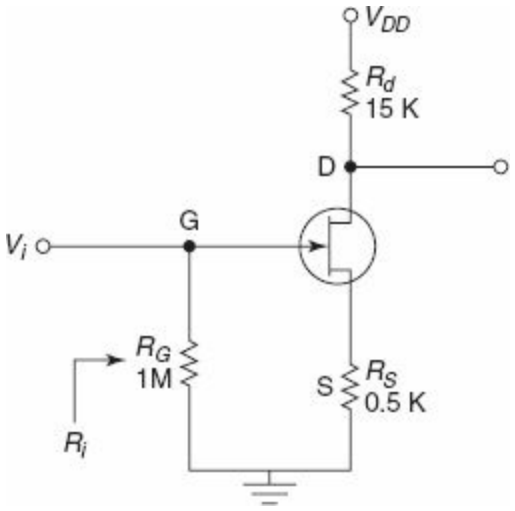
$$A_v = \frac{-\mu R_d}{r_d + R_d}$$

$$= \frac{-25 \times 15\,\text{K}}{5\,\text{K} + 15\,\text{K}}$$

$$= \frac{-375}{20} = 18.75$$

$$Z_o = r_d$$

$$= 5\,\text{K}$$



Z_i = Input resistance of the FET amplifier

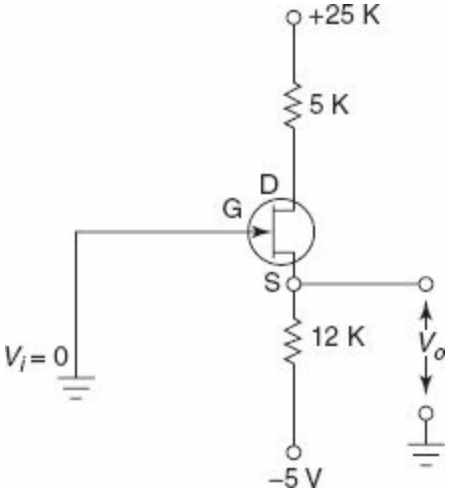
$\cong R_g$ (resistance of gate-to-source − infinite) = 1 MΩ

Example 7-29 The circuit, as shown in the diagram, uses a JFET with $I_{DSS} = 5$ mA and $V_p = -4.5$ V. If V_i and V_o represent voltages and not the small-signal values, calculate the following:

a. V_o for $V_i = 0$
b. V_i for $V_o = 0$

Solution:
We know that:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$



Substituting the given value of I_{DSS} and V_p we get:

$$I_D = 5\left(1 + \frac{V_{GS}}{4.5}\right)^2 \text{ mA} \qquad (1)$$

a. When $V_i = 0$

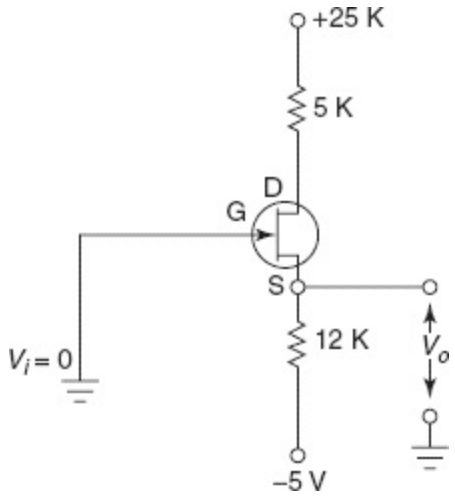
For this condition, we first redraw the circuit.
Taking KVL around the input loop, we get:

$$V_{GS} = I_D R_S - 5 \text{ V}$$

$$= I_D \times 12 - 5 \text{ V } (I_D \text{ in mA})$$

or,

$$I_D = \frac{V_{GS} + 5}{12} \qquad (2)$$



Substituting Eq. (2) in Eq. (1) we get:

$$\frac{V_{GS} + 5}{12} = 5\left(1 + \frac{V_{GS}}{4.5}\right)^2$$

or,

$$V_{GS} + 5 = 60\left(1 + \frac{2V_{GS}}{4.5} + \frac{V_{GS}^2}{4.5^2}\right)$$
$$= 60 + 26.67\ V_{GS} + 2.963 V_{GS}^2$$

or,

$$2.963\ V_{GS}\,2 + 25.67\ V_{GS} + 55 = 0$$

$\therefore$

$$V = \frac{-25.67 \pm \sqrt{(25.67)^2 - 4 \times 2.963 \times 55}}{2 \times 2.963}$$
$$= -4.78\ \text{V} \quad \text{or} \quad -3.88\ \text{V}$$

The output voltage V_o is voltage of the source w.r.t the ground. Since the gate is connected to the ground, $V_o = V_{SG} = -V_{GS}$

$\therefore$

$$V_o = +4.78\ \text{V or } +3.88\ \text{V}$$

b. When $V_o = 0$

The output point (the source S) is grounded, as shown in the diagram.

$\therefore$

$$I_D R_S = 5\ \text{V}$$

or,

$$I_D = \frac{5\ \text{V}}{12\ \text{K}} = 0.415\ \text{mA}$$

Substituting this value of I_D in Eq. 1:

$$0.415 = 5\left(1 + \frac{V_{GS}}{4.5}\right)^2$$

or,

$$\left(1 + \frac{V_{GS}}{4.5}\right)^2 = \frac{0.415}{5} = 0.083$$

or,

$$1 + \frac{V_{GS}}{4.5} = \sqrt{0.083} = 0.288$$

or,

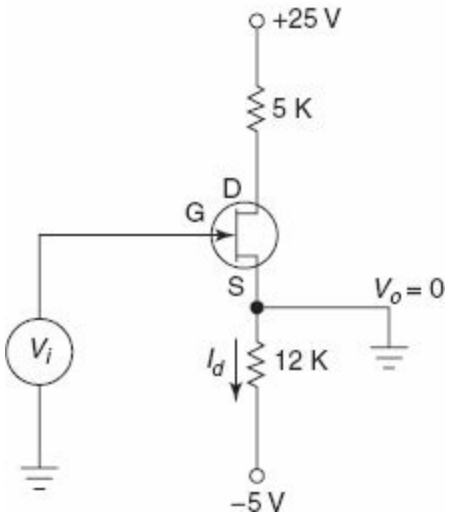
$$V_{GS} = 4.5(0.288 - 1) = -3.2\ \text{V}$$

Taking KVL around the input loop:

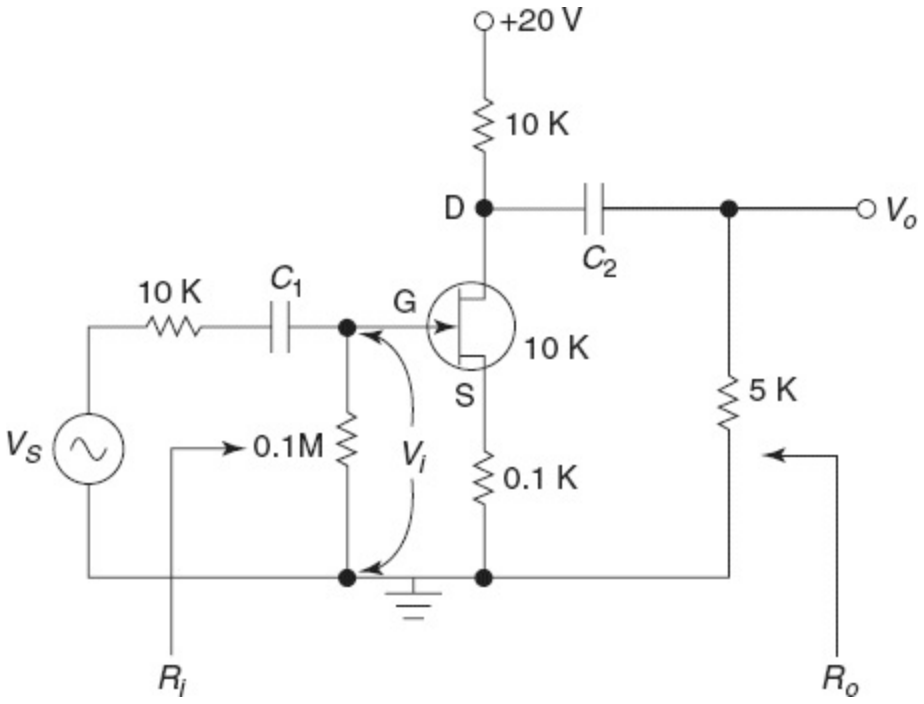
$$V_i = V_{GS}$$

$\therefore$

$$V_i = -3.2\ \text{V}$$



Example 7-30 For the circuit, as shown in the following diagram, calculate $A_v = V_o/V_s$ and Z_o if g_m = 5 mA / V and r_d = 10 KΩ.



Solution:

$$\mu = g_m r_d = 5 \text{ mA/v} \times 10 \text{ k}\Omega = 50$$

At signal frequency, both C_1 and C_2 are assumed to be short-circuited. Therefore, the 10 K load resistance effectively comes in parallel with R_d (10 K).

Therefore, effective R_d = 10 K || 10 K = 5 kΩ.

The voltage gain (V_o / V_i) is:

$$A_v = \frac{-\mu R_d}{r_d + R_d + (\mu + 1)R_s}$$

$$= \frac{-50 \times 5\ \text{K}}{10\ \text{K} + 5\ \text{K} + (50 + 1) \times 0.1\ \text{K}}$$

$$= -12.44$$

The right voltage V_i appearing across the 0.1 M resistance is:

$$V_i = \frac{0.1\ \text{M}}{0.1\ \text{M} + 10\ \text{K}} \times V_s$$

$\therefore$

$$\frac{V_i}{V_s} = \frac{100\ \text{K}}{110\ \text{K}} = 0.909$$

The overall voltage gain:

$$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s}$$

$$= A_v \frac{V_i}{V_s}$$

$$= -12.44 \times 0.909 = -11.3$$

The output impedance:

$$Z_o = r_d + (\mu + 1)\ R_S$$

$$= 10\ \text{K} + (50 + 1)\ 0.1\ \text{K}$$

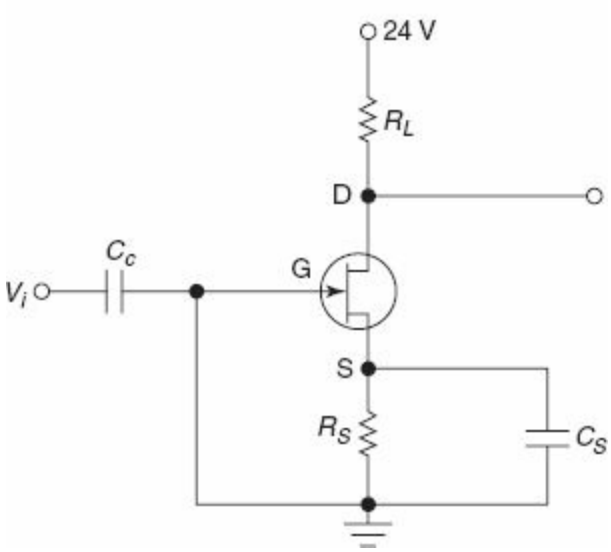
$$= 15.1\ \text{K}$$

The effective output impedance:

$$Z_o' = Z_o\ //\ 10\ \text{K}\ //\ 10\ \text{K}$$

$$= 15.1\ \text{K}\ //\ 5\ \text{K} = 3.75\ \text{k}\Omega$$

Example 7-31 The *n*-channel JEFT, as shown in the following diagram, has $V_p = -4$ V and I_{DSS} = 1.65 mA. The operating point desired is I_{DQ} = 0.8 mA. Assume $r_d >> R_L$. Calculate (a) *VGSQ*, (b) g_m, (c) *R*s, (d) V_{DSQ} and (e) *RL*, such that a voltage gain of 20 dB is obtained. R_s is passed by the large capacitor C_s and reactance of C_c is negligible at signal frequency.



Solution:

a. We know that

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting I_{DSS} = 1.65 mA, V_p = −4 V and I_{DQ} = 0.8 mA:

$$0.8 = 1.65\left(1 + \frac{V_{GS}}{4}\right)^2$$

or,

$$1\left(1 + \frac{V_{GS}}{4}\right)^2 = \frac{0.8}{1.65} = 0.485$$

$$1 + \frac{V_{GS}}{4} = \sqrt{0.485} = 0.696$$

$$V_{GS} = 4 \times (0.696 - 1)$$

$$= -1.214 \text{ V}$$

∴

$$V_{GSQ} = -1.214 \text{ V}$$

b.

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_p}\right)$$

where,

$$g_{mo} = \frac{-2\, I_{DSS}}{V_p}$$

∴

$$g_{mo} = \frac{-2 \times 1.65}{-4} = 0.825 \text{ mA/V}$$

$\therefore$

$$g_m = 0.825\left(1 - \frac{(-1.214)}{(-4)}\right)$$

$$= 0.825 \times 0.6965 = 0.575 \text{ mA/V}$$

c. Looking into the input loop:

$$V_{GS} = I_{DQ} R_S$$

$\therefore$

$$-1.214 \text{ V} = -0.8 \text{ mA} \times R_s$$

$\therefore$

$$R_s = \frac{1.214}{0.8} = 1.518 \text{ k}\Omega$$

d. It is given that the voltage gain has to be 20 dB. Now voltage gain in dB = 20 log (voltage gain)

$\therefore$

$$20 \text{ dB} = 20 \log_{10} A_v$$

$\therefore$

$$A_v = 10$$

Since it is given that $r_d >> R_L$, the voltage gain of the CS amplifier:

$$A_v = -g_m R_L$$

$$|A_v| = g_m R_L$$

$\therefore$

$$10 = 0.575 \text{ mA/V} \times R_L$$

$\therefore$

$$R_L = \frac{10}{0.575 \text{ mA/V}} = 17.4 \text{ k}\Omega$$

e. Taking the KVL for the output loop:

$$24 \text{ V} = I_D R_L + V_{DS} + I_D R_s$$

or,

$$V_{DS} = 24 \text{ V} - I_D R_L - I_D R_s$$

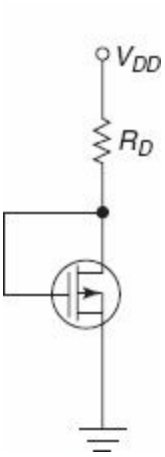
$$= 24 \text{ V} - 0.8 \text{ mA} \times 17.4 \text{ K} - 0.8 \text{ mA} \times 1.518 \text{ k}\Omega$$

$$= 8.86 \text{ V}$$

$\therefore$

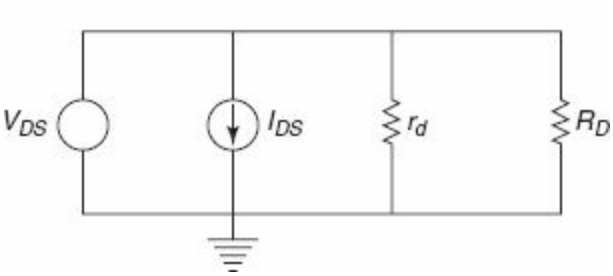
$$V_{DSQ} = 16.48 \text{ V}$$

Example 7-32 (a) Draw the low-frequency small-signal model of the circuit shown in the diagram (b) Determine Z_o. (c) Evaluate Z_o for $r_d = 50$ kΩ and $R_D = 20$ kΩ.



Solution:

a. The equivalent circuit at low-frequency small-signal model is:



b. Output resistance:

$$Z_o = r_d \| R_D$$

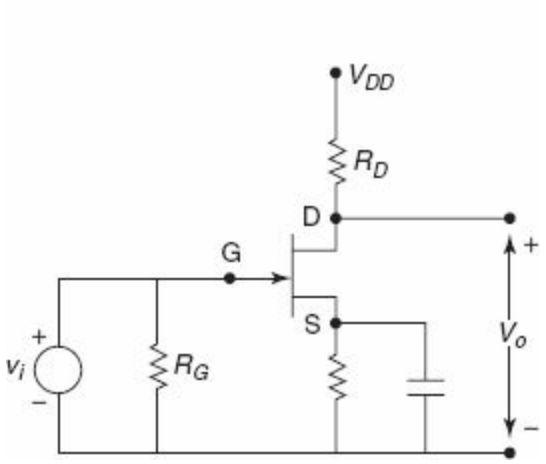
c. Hence, for $R_D = 20$ kΩ and $r_d = 50$ kΩ

$$Z_o = \frac{r_d R_D}{r_d + R_D} = \frac{20 \times 10^3 \times 50 \times 10^3}{20 \times 10^3 + 50 \times 10^3}$$

$$= \frac{1000}{70} \times 10^3$$

$$= 14.28 \text{ k}\Omega$$

Example 7-33 In the CS amplifier, as shown in the diagram, let $R_D = 5$ kΩ, $R_G = 500$ kΩ, $\mu = 60$, and $r_{ds} = 30$ kΩ. Find the value of the voltage-gain ratio $A_v = v_o/v_i$ and current gain ratio $A_i = i_d/i_i$.

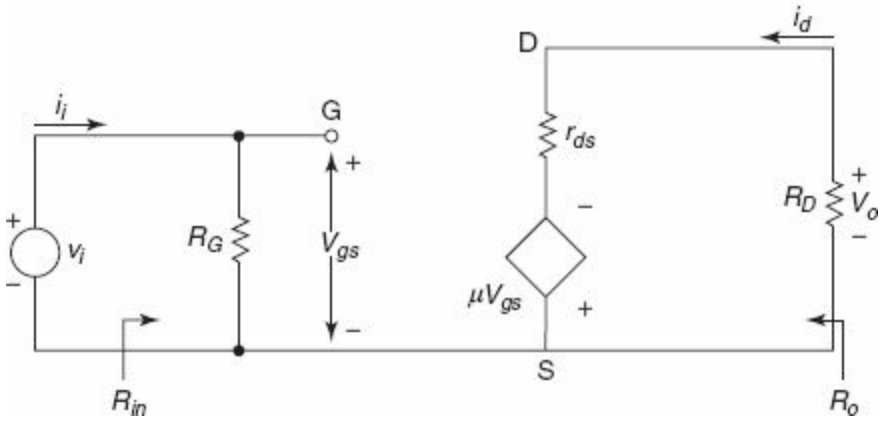


Solution:

Voltage-gain ratio:

By voltage division at the output network of the applicable equivalent circuit, as shown in the following diagram, we have:

$$v_o = \frac{R_D}{R_D + r_{ds}} \mu v_{gs}$$



Substitution of $v_{gs} = v_i$ and rearrangement gives:

$$A_v = \frac{v_o}{v_i} = \frac{\mu R_D}{R_D + r_{ds}} = \frac{60 \times 5}{5 + 30} = 8.57$$

Current-gain ratio:

KVL around the output network leads to:

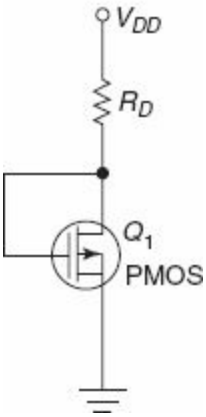
$$i_d = \frac{\mu v_{gs}}{r_{ds} + R_D}$$

But, Ohm's law requires that $\upsilon_{gs} = i_i R_G$ which, when substituted gives:

$$A_i = \frac{i_d}{i_i} = \frac{\mu R_G}{r_{ds} + R_D} = \frac{60 \times 500}{30 + 5} = 857.14$$

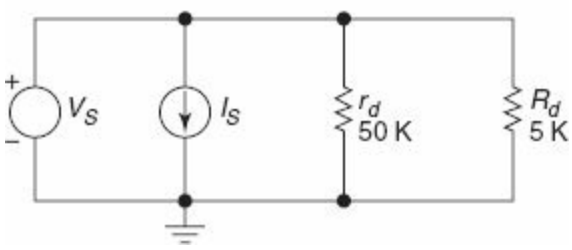
Example 7-34

a. Draw the low frequency small signal model of the circuit as shown in the diagram.
b. Determine Z_O.
c. Evaluate Z_O for g_m = 1.0 m-mho, r_d = 50 kΩ, R_D = 5 kΩ.



Solution:

a. The equivalent circuit at low-frequency small-signal model is:



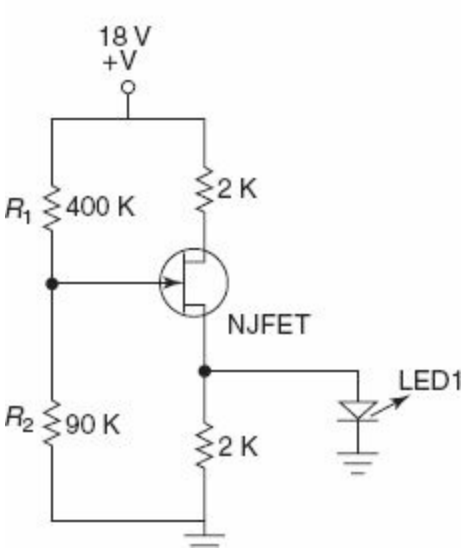
b. Output resistance, $Z_O = R_{DS} \parallel R_D$

c. Hence, for R_D = 5 kΩ and R_{DS} = 50 kΩ:

$$Z_o = \frac{50 \times 5}{50 + 5}$$

$$= 4.54 \text{ k}\Omega$$

Example 7-35 An *n*-channel JFET has $V_P = -5$ V, and I_{DSS} = 12mA and is used in the circuit shown. The parameter values are V_{DD} = 18 V, R_S = 2 kΩ, R_D = 2 kΩ, R_1 = 400 kΩ and R_2 = 90 kΩ.



a. If the resistance R_2 is changed, what must be the new value of R_2 if I_D = 8 mA?
b. Using the values as given, but changing V_{DD}, find the new values of V_{DD} for which I_D = 8 mA.
c. For the condition in (b), what is the new value of V_{DS}?

Solution:

Let us consider the voltage across the R_2 to be V_2.

Now, applying the KVL in the lower loop of the circuit:

$$V_2 = I_D R_S + V_{GS}$$

where, I_D is the drain current and V_{gs} is the gate-to-source voltage.

$\therefore$ Voltage drop across R_2 is, $V_2 = \dfrac{R_2}{R_1 + R_2} V_{DD}$

Putting the value of V_2, we get:

$$\frac{R_2}{R_1 + R_2} V_{DD} = I_D R_S + V_{GS}$$

or,

$$\frac{90}{90 + 400} 18 = 2 I_D + V_{GS}$$

or,

$$2I_D + V_{GS} = 3.3$$

In case of the JFET, the drain current is:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 12\left(1 + \frac{V_{GS}}{5}\right)^2$$

or,

$$1.65 - \frac{V_{GS}}{2} = 12 + \frac{24}{5} V_{GS} + 0.48 V_{GS}^2$$

or,

$$0.48 V_{GS}^2 + 5.3 V_{GS} + 10.35 = 0$$

or,

$$V_{GS} = -8.5 \text{ V or } -2.53 \text{ V}$$

$\therefore$

$$V_{GS} = -2.53 \text{ V}$$

From equation for I_D:

$$I_D = (3.306 - \text{VGS})/2 = 2.92 \text{ mA}$$

Applying KVL in the outer loop of the circuit:

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

or,

$$18 = 2.92 \times 2 + V_{DS} + 2.92 \times 2$$

or,

$$V_{DS} = 6.32 \text{ V}$$

a. Again we have:

$$\frac{R_2}{R_1 + R_2} V_{DD} = I_D R_S + V_{GS}$$

or,

$$\frac{R_2}{400 + R_2} 18 = 8 \times 2 - 2.53$$

or,

$$R_2 = 1189.4 \text{ k}\Omega$$

The new value of R_2 is 1189.4 K, if $I_D = 8$ mA

b. We have:

$$\frac{R_2}{R_1 + R_2} V_{DD} = I_D R_S + V_{GS}$$

or,

$$V_{DD} \frac{90}{400 + 90} = 8 \times 2 - 2.53$$

or,

$$V_{DD} = 73.34 \text{ V}$$

The new value of V_{DD} is 73.34 V when $I_D = 8$ mA.

c. We know that:

$$V_{DD} = I_D \times R_D + V_{DS} + I_D \times R_S$$

or,

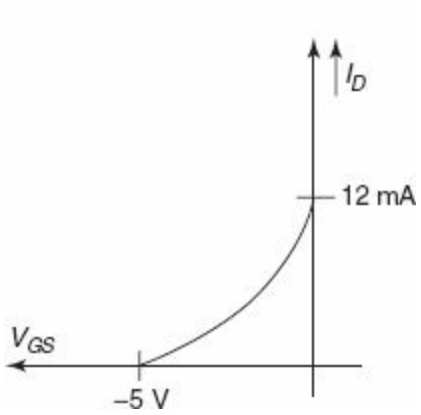
$$73.34 = 8 \times 2 + V_{DS} + 8 \times 2$$

$\therefore$

$$V_{DS} = 41.34 \text{ V}$$

The new value of V_{DS} is 41.34 V.

Example 7-36 The given diagram shows the transfer characteristics of an FET. Write an equation for drain current.



Solution:

From the figure:

$$I_{DSS} = 12 \text{ mA}$$

$$V_{GS(\text{off})} = -5 \text{ V}$$

We know that:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2 = 12\left(1 - \frac{V_{GS}}{-5}\right)$$

$\therefore$

$$I_D = 12\left(1 + \frac{V_{GS}}{5}\right)^2 \text{mA}$$

Example 7-37 An FET has a drain current of 5 mA. If $I_{DSS} = 12$mA and $V_{GS(\text{off})} = -6$ V, find the value of (a) V_{GS} and (b) V_p.

Solution:

a. ∵

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(\text{off})}}\right)^2$$

⇒

$$5 = 12\left(1 + \frac{V_{GS}}{6}\right)^2$$

$$\frac{5}{12} = \left(1 + \frac{V_{GS}}{6}\right)^2$$

$$\sqrt{\frac{5}{12}} = 1 + \frac{V_{GS}}{6}$$

$$-0.355 = \frac{V_{GS}}{6}$$

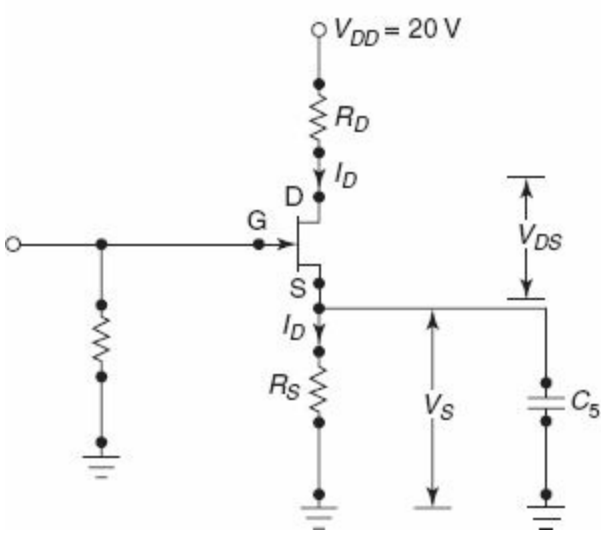
∴

$$V_{GS} = -2.13 \text{ V}$$

b.

$$V_{GS}(\text{off}) = V_P = 6 \text{ V}$$

Example 7-38 In a self-bias *n*-channel FET, the operating point is to be set at $I_D = 1.5$ mA and $V_{DS} = 10$ V. The FET parameters are $I_{DSS} = 5$ mA and $V_P = -2$ V. Find the values of R_S and R_D. Given that $V_{DD} = 20$ V.



Solution:

∵

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$\therefore$

$$1.5 = 5\left(1 + \frac{V_{GS}}{2}\right)^2$$

$$V_{GS} = -0.9 \text{ V}$$

Now,

$$V_{GS} = V_G - V_S$$

$\therefore$

$$V_S = V_G - V_{GS} = 0 - (-0.9)$$

$\therefore$

$$V_S = 0.9 \text{ V}$$

$$R_S = \frac{V_S}{I_D} = \frac{0.9}{1.5} \text{ mA} = 0.6 \text{ k}\Omega$$

Now, apply KVL to the outer loop:

$\therefore$

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$\therefore$

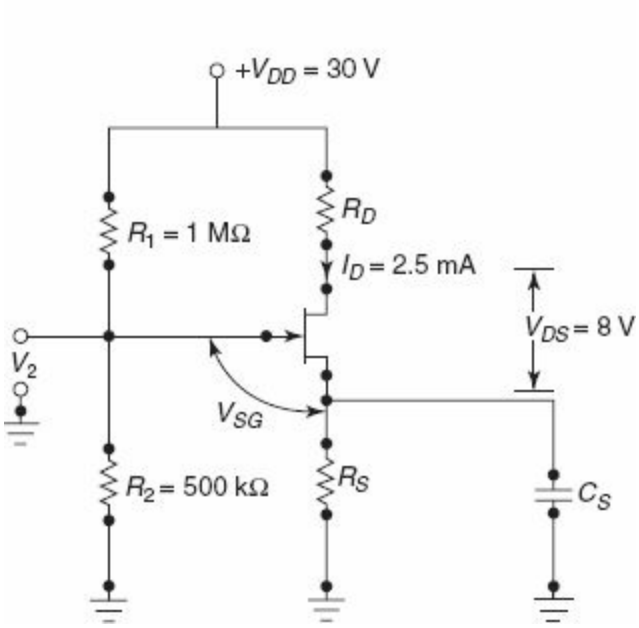
$$20 = 1.5 \text{ mA} \times R_D + 10 + 0.9 \ (\because I_D R_S = V_S)$$

$\therefore$

$$R_D = \frac{20 - 10.9}{1.5 \times 10^{-3}}$$

$$R_D = 6.06 \text{ k}\Omega$$

Example 7-39 In an *n*-channel FET biased by potential divider method, it is desired to set the operating point at $I_D = 2.5$ mA and $V_{DS} = 8$ V. If $V_{DD} = 30$ V, $R_1 = 1$ MΩ and $R_2 = 500$ kΩ, find the value of R_S. The parameters of the FET are $I_{DSS} = 15$ mA and $V_P = -5$ V.



Solution:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or,

$$2.5 = 15\left(1 + \frac{V_{GS}}{5}\right)^2$$

or,

$$\frac{5}{2 \times 15} = \left(1 + \frac{V_{GS}}{5}\right)^2$$

or,

$$V_{GS} = -2.96 \text{ V}$$

Now,

$$V_2 = \frac{V_{DD} R_2}{R_1 + R_2} = \frac{30 \times 500}{1000 + 500}$$

$$V_2 = 10 \text{ V}$$

or,

$$V_2 = V_{GS} + I_D R_S$$

or,

$$10 = -2.96 + 2.5 \times 10{-}3R_S$$

or,

$$R_s = \frac{12.5}{2.5} \times 10^3$$

or,

$$R_S = 5.18\ \text{k}\Omega$$

Applying KVL to outer loop:

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

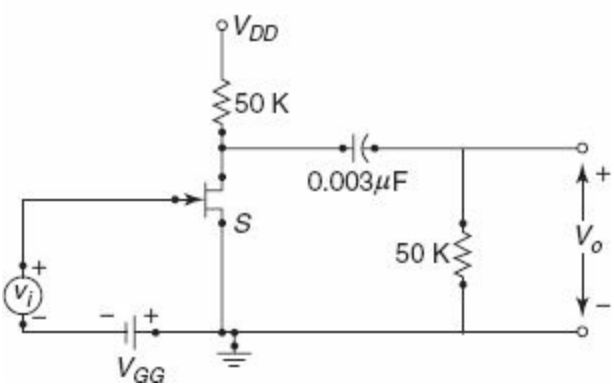
or,

$$30 = 2.5 \times 10^{-3} R_D + 8 + 2.5 \times 10^{-3} \times 5.18 \times 10^3$$

or,

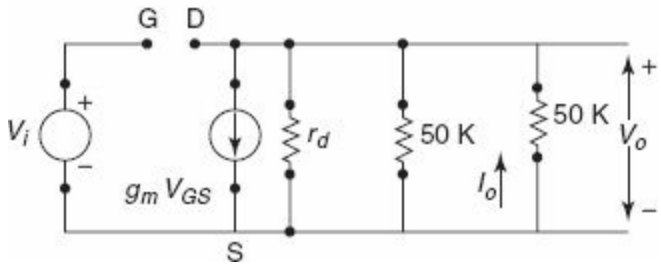
$$R_D = 3.62\ \text{k}\Omega$$

Example 7-40 (a) Calculate the voltage gain $A_V = V_o/V_i$ at 1 KHz for the circuit, as shown in the diagram. The FET parameters are $g_m = 2\text{mA/V}$ and $r_d = 10\ \text{k}\Omega$. Neglect capacitance. (b) Repeat part (a) if the capacitance 0.005 μF is taken underconsideration.



Solution:

a. The equivalent small-signal circuit is shown as follows.



We neglect the 0.005μF capacitance and we have $V_{GS} = V_i$

$R = r_d \parallel 50\ \text{K} \parallel 50\ \text{K} = r_d \parallel 25\ \text{K} = 7.14\ \text{K}$

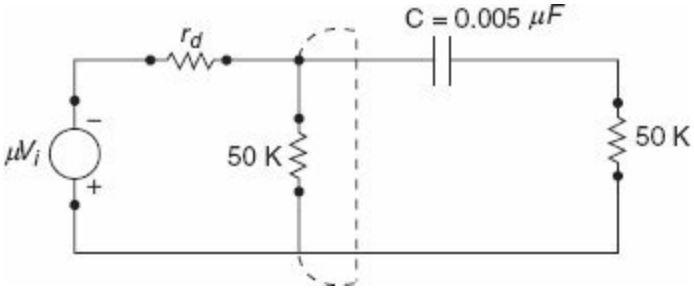
The voltage gain of the amplifier, as calculated in Example 7-1, is:

$$A_V = -g_m R$$

Hence,

$$A_V = -2 \times 7.14 = -14.28$$

b. The small-signal equivalent circuit seen at the drain is as shown in the following diagram.



Then the Thevenin's equivalent consists of:

$$R_{Th} = r_d \parallel 50\text{ K} = 10\text{ K} \parallel 50\text{ K} = 8.33\text{ K}$$

and,

$$V_{Th} = \mu V_i \frac{50\text{ K}}{50\text{ K} + 10\text{ K}} = \frac{20 \times 50}{60} V_i$$

$$= 16.67\, V_i \text{ at } 1\text{ KHz}, Z_C = -j\,31.83\text{ K}$$

Then,

$$\frac{V_o}{V_i} = \frac{-50\text{ K}(16.67)}{50\text{ K} + 8.33\text{ K} - j31.83\text{ K}} = \frac{-833}{58.33 - j31.83}$$

$$= \frac{-833}{66.45} \angle\ 28.62° = -12.54 < 28.62°$$

Example 7-41 The transconductance of an FET used in a voltage-amplifier circuit is 2 mS, and the load resistance is 10 kΩ. Calculate the voltage amplification of the circuit. Assume that $r_d >> R_L$.

Solution:
Given,

$$g_{fs} = 2\text{ mS}$$

$$R_L = 10\text{ k}\Omega$$

As,

$$r_d >> R_L$$

The voltage gain is given by:

$$A_V = g_{fs} R_L = 2\text{ mS} \times 10\text{ k}\Omega = 20$$

Example 7-42 Show that, if two identified FETs are connected in parallel, then g_m is double and r_d is half of that of the individual. If two FET's are not identical, show that:

$$\frac{1}{r_d} = \frac{1}{r_{d1}} + \frac{1}{r_{d2}} \qquad \text{and} \qquad \mu = \frac{\mu_1 r_{d2} + \mu_2 r_{d1}}{r_{d1} + r_{d2}}$$

Solution:

The relationship among the FET parameters can be written as:

$$\mu = \frac{\partial V_{DS}}{\partial V_{GS}}$$

This can be further modified and written as:

$$\mu = \frac{\partial V_{DS}}{\partial I_D} \times \frac{\partial I_D}{\partial V_{GS}}$$

$\therefore$

$$\mu = \frac{\partial V_{DS}}{\partial I_D} \times \frac{\partial I_D}{\partial V_{GS}} \qquad (1)$$

where,

$$r_d = \frac{\partial V_{DS}}{\partial I_D} \qquad \text{and} \qquad g_{fs} = \frac{\partial I_D}{\partial V_{GS}}$$

μ is the amplification factor.

If two FETs are in parallel then the current change is the double of that of a single FET for a given change in gate voltage.

Now,

$$g_m = \frac{I_{dSI}(\text{total})}{V_{gS}}$$

$\therefore$

$$g_m = g_{m1} + g_{m2} \qquad (2)$$

Also,

$$g_d = g_{d1} + g_{d2} \qquad (3)$$

$\because$

$$g_d = \frac{1}{r_d} \quad \text{when} \quad \mu = 1$$

$\therefore$

$$\frac{1}{r_d} = \frac{1}{r_{d1}} + \frac{1}{r_{d2}}$$

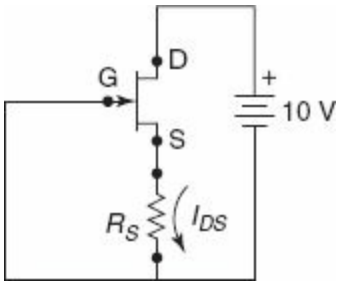
Also,

$$\begin{aligned}\mu &= g_m r_d \\ &= (g_{m1} + g_{m2}) \frac{r_{d1} r_{d2}}{r_{d1} + r_{d2}} \\ &= \left(\frac{\mu_1}{r_{d1}} + \frac{\mu_2}{r_{d2}}\right) \frac{r_{d1} \times r_{d2}}{r_{d1} + r_{d2}} \\ &= \frac{\mu_1 r_{d2} + \mu_2 r_{d1}}{r_{d1} + r_{d2}} \times \frac{r_{d1} r_{d2}}{r_{d1} + r_{d2}}\end{aligned}$$

$\therefore$

$$\mu = \frac{\mu_1 r_{d2} + \mu_2 r_{d1}}{r_{d1} + r_{d2}}$$

Example 7-43 The JFET, as shown in the diagram, has an $I_{dss} = 10$ mA, and $V_p = -5$ V. Find the value of resistance R_S for a drain current $I_{DS} = 6.4$ mA.



Solution:
Given,

$$I_{DSS} = 10 \text{ mA}, V_p = -5 \text{ V}$$

$$I_{DS} = 6.4 \text{ mA}, R_S = ?$$

$$6.4 = 10\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$0.8 = \left(1 - \frac{V_{GS}}{V_p}\right)$$

$V_{GS} = 0.2\ V_p = 0.2 \times (-5) = -1$ V

$\Rightarrow$

$$I_{DS}\, R_S = 1$$

Therefore,

$$R_s = \frac{1}{I_{DS}} = \frac{1}{6.4 \times 10^{-3}} 156\ \Omega$$

Example 7-44 If $|I_{DSS}| = 4$ mA, $V_p = 4$ V, calculate the quiescent value of I_D, V_{GS} and V_{DS}

Solution:

$$R_{TH} = 200\ \text{K} \parallel 1.3\ \text{M}$$
$$= 173.5\ \text{K}$$
$$-V_{TH} = \frac{200\ \text{K}}{1500\ \text{K}}(1 - 60) = -8\ \text{V}$$

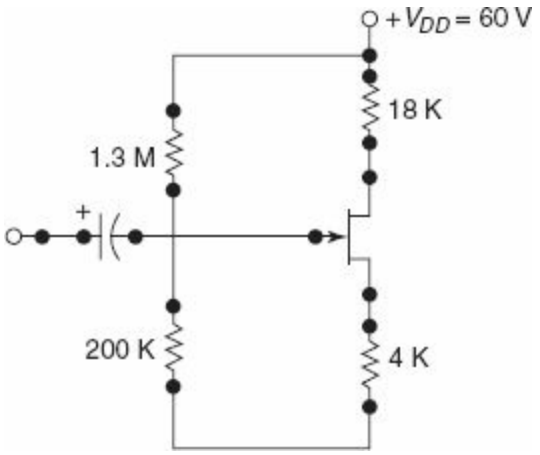
or,

$$V_{GS} = -4I_D - 8$$
$$I_D = -\frac{8 + V_{GS}}{4}; \quad I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

⇒

$$\left(\frac{-8 - V_{GS}}{4}\right) = 4\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$V_{GS} = I_V \Rightarrow I_D = \left(\frac{-8 - V_{GS}}{4}\right) = -2.25\ \text{mA}$$



Solving, we get:

$$V_{GS} = I_V$$

$$I_D = -2.25\ \text{mA}$$

Hence,

$$V_{DS} = -60 - (18 + 4)\ (2.25)$$

$$= -60 + 49.5 = -10.5\ \text{V}$$

7-6 HIGH-FREQUENCY MOSFET MODEL

The high-frequency MOSFET model takes into account many capacitances of the device, such as inter-electrode capacitance, wiring capacitance, etc. It is advisable to peep into the details of these capacitances which arise due to many parameters related to the fabrication of the device. Among the many internal capacitances of the device, the gate-to-channel capacitance is the most common one.

There are basically two types of capacitances in the high-frequency MOSFET model.

i. The gate capacitance effect: A parallel plate capacitor is formed due to the channel and the gate electrode where the silicon dioxide layer forms the dielectric substance.
ii. The source−body and drain−body capacitive effect: These are capacitances which arise due to the reverse-biased $p-n$ junctions formed by the $n+$ source region and p-type substrate, and by the $n+$ type drain region and substrate.

Effectively, there are five capacitances C_{gs}, C_{gd}, C_{gb}, C_{sb} and C_{db}, where the subscripts locate the position of the terminals between which the capacitances are located.

7-6-1 Effective Capacitance of the Gate

With the gate capacitances, as listed in the previous section, it is advisable to revisit their expressions prior to investigating the operation of the device in the high-frequency region.

i. When the MOSFET operates in the triode region at a relatively small voltage v_{DS}, the depth of the channel in the bulk is uniform. The equivalent gate-channel capacitance can be considered to be divided equally between the source and the gate ends. Thus, $C_{gs} = C_{gd} = WLC_{ox}/2$ where, the letters carry their usual meaning.
ii. As the MOSFET operates in the saturation region, the channel is tapered into shape, and is gradually pinched-off at the drain end. Under such circumstances, the capacitances are given by:

$$C_{gs} = \frac{2WLC_{ox}}{3} \quad \text{and} \quad C_{gd} = 0$$

iii. When the MOSFET is in the cut-off region, the channel disappears, and the capacitances take the values as given by:

$$C_{gs} = C_{gd} = 0 \text{ and } C_{gb} = WLC_{ox}$$

7-6-2 The Junction Capacitance

The depletion-layer capacitance resulting from the two reverse-biased regions between the gate and the bulk, and the drain and the bulk respectively, is quantitatively given by:

$$C_{sb} = \frac{C_{sbo}}{\sqrt{1 + \frac{V_{sb}}{V_o}}} \qquad (7\text{-}31)$$

where, C_{sbo} is the value of the desired capacitance at zero body-source bias, V_o is the junction built in voltage 0.7 V and V_{sb} is the applied reverse-biased voltage.

7-6-3 The High-Frequency Models of the MOSFET

Figure 7-13 shows the high-frequency model of the MOSFET. This model is too complex to be analysed manually, but with the SPICE software, meant for circuit analysis, the procedure becomes exceedingly simple. This model is primarily used to predict the high-frequency response of the MOSFET.

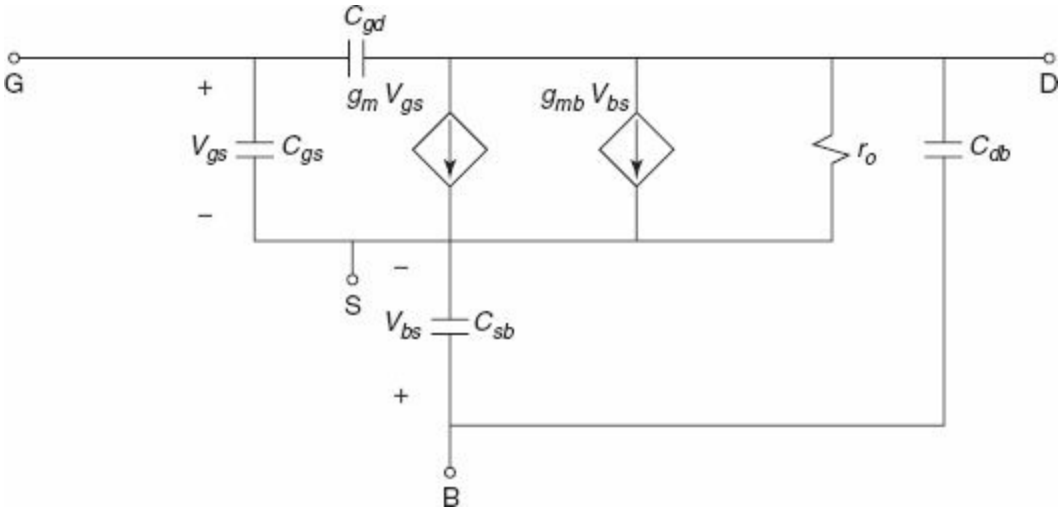


Figure 7-13 High-frequency equivalent model of MOSFET

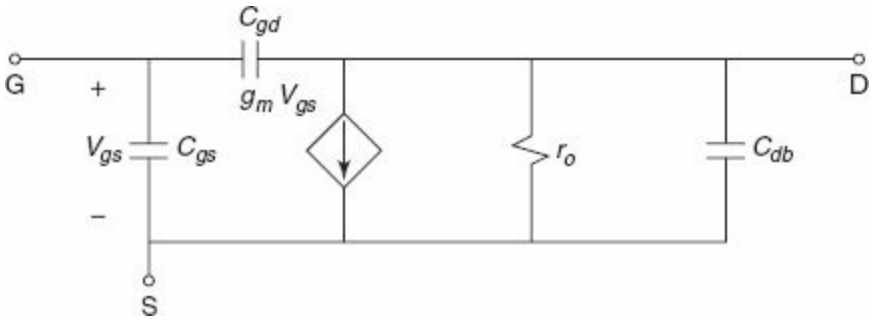


Figure 7-14 High-frequency MOSFET model when the source is connected to the base

When the condition so arises that the source is connected to the body, then the model, as shown in Fig. 7-13, gets simplified (see Fig 7-14). Again, in the model, as shown in Fig. 7-14, when C_{db} is neglected, the resulting circuit is as given by Fig. 7-15.

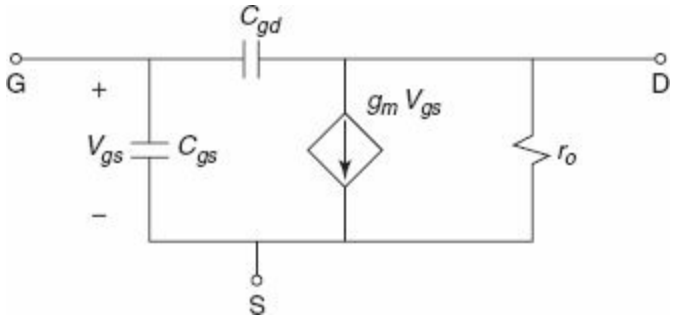


Figure 7-15 Circuit obtained upon neglecting C_{db}

A parameter used to judge the operation of a high-frequency MOSFET as an amplifier, is the unity-gain bandwidth. The frequency at which short-circuit current gain of the common-source arrangement

becomes unity, is known as the unity-gain frequency. This analysis is done using a hybrid π model with a common-source configuration.

It can be noticed easily that the current in the short circuit is given by:

$$I_0 = g_m V_{gs} - sC_{gd}V_{gs} \tag{7-32}$$

where, s is a complex variable.

Since C_{gd} is very small, Eq. (7-32) can be written as $I_0 \approx g_m V_{gs}$.

And from Fig. 7-16, we get:

$$V_{gs} = \frac{I_i}{s(C_{gs} + C_{gd})} \tag{7-33}$$

Substituting, $I_0 = g_m V_{gs}$ we obtain:

$$\frac{I_0}{g_m} = \frac{I_i}{s(C_{gs} + C_{gd})}$$

$$\frac{I_0}{I_i} = \frac{g_m}{s(C_{gs} + C_{gd})} \tag{7-34}$$

Taking $s = j\omega$ (where, ω is the frequency of the applied voltage), and since the magnitude of current gain becomes unity at this frequency, we can write:

$$\omega_T = \frac{g_m}{(C_{gs} + C_{gd})} \tag{7-35}$$

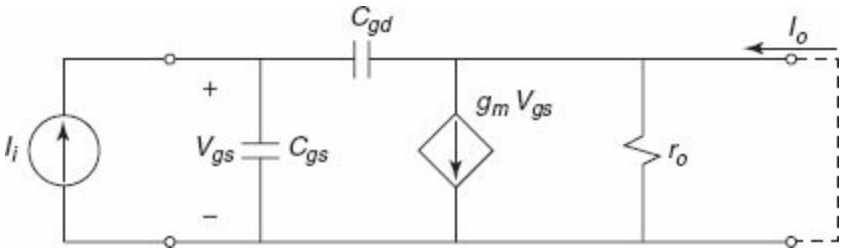


Figure 7-16 Circuit representation for obtaining short-circuit current gain

Solved Examples

Example 7-45 Calculate the input admittance of an FET at 10^3 and 10^6 Hz when the total drain circuit impedance is (a) a resistance of 50 K and (b) a capacitive reactance of 50 K at each frequency. (Take the inter-electrode capacitances into consideration.) The FET parameters are $\mu = 20$, $r_d = 10$ K, $g_m = 2.0$ mA/ V, $C_{gs} = 3.0$ pF, $C_{ds} = 1.0$ pF and C$gd = 2.0$ pF. Express the results in terms of the input resistance and capacitance.

Solution:

We have two equations:

$$A_V = \frac{-g_m + Y_{gd}}{g_d + Y_d + Y_{ds} + Y_{gs}}$$

$$Y_1 = Y_{gs} + (1 - A_V)Y_{gd}$$

a. $R_d = 50$ K

For, $f = 10^3$Hz.

$Y_{gs} = j\omega C_{gs} = j2\pi \times 10^3 \times 3.0 \times 10^{-12} = j1.88 \times 10^{-6}$

$Y_{ds} = j\omega C_{ds} = j2\pi \times 10^3 \times 1.0 \times 10^{-12} = j0.628 \times 10^{-6}$

$Y_{gd} = j\omega C_{gd} = j2\pi \times 10^3 \times 2.0 \times 10^{-12} = j1.26 \times 10^{-6}$

$Y_d = 2 \times 10^{-6}\, g_d = 10^{-4}$

Hence,

$$A_V = \frac{-2 \times 10^{-3} + j1.26 \times 10^{-6}}{12 \times 10^{-6} + j1.88 \times 10^{-6}} \approx \frac{-2}{12} \times 10^2 = -16.7$$

and, $C_1 = 3.0 + 17.7 \times 2 = 38.4$ pF

For, $f = 106$ Hz:

$Y_{gs} = j1.88 \times 10^{-6}$

$Y_{ds} = j0.628 \times 10^{-6}$

$Y_{gd} = j1.26 \times 10^{-6}$

Hence,

$$A_V = \frac{-2 \times 10^{-3} + j\,1.26 \times 10^{-6}}{1.2 \times 1^{-5} + j\,1.88 \times 10^{-6}} = \frac{-200 + j1.26}{12 + j1.68} = -16.3 + j\,1.97$$

$$Y_1 = \frac{1}{R_1} + j\omega C_1; \quad C_1 = 37.6 \text{ pF}; \quad \frac{1}{R_1} = 1.26 \times 10^{-6} \times 1.97 = 2.48 \times 10^{-6}$$

$$R_1 = \frac{10^5}{2.48} = 40.4 \text{ K}$$

b. $Z_L = j5 \times 10^4$; $Y_L = j2 \times 10^{-6}$

For, $f = 10^3$Hz:

$$A_V = \frac{-g_m}{g_d + Y_L} = \frac{-2 \times 10^{-3}}{10^{-4} + j\,2 \times 10^{-5}}$$

$$= \frac{-200}{10 + j2} = -19.2 + j3.84$$

$$Y_1 = \frac{1}{R_1} + j\omega C_1 = + j\omega C_{gs} + (20.2 - j3.84)j\omega C_{gd}$$

or,

$$C_1 = 30 + 20.2 \times 2.0 = 43.4 \text{ pF}$$

and,

$$\frac{1}{R_1} = 4.84 \times 10^{-6}$$

or,

$$R_1 = +20.8 \text{ M}$$

For, $f = 10^6$ Hz:

$$A = \frac{-2 \times 10^{-3} + j1.26 \times 10^{-6}}{10^{-4} + j3.88 \times 10^{-6}}$$

$$= \frac{-200 + j1.26}{10 + j3.88}$$

$$= -17.4 + j6.85$$

$$C_1 = 3.0 + 18.4 \times 2.0 = 39.8 \text{ pF}$$

and,

$$\frac{1}{R_1} = \frac{10^5}{8.64} = 11.6 \text{ K}$$

Example 7-46 Starting with the low-frequency small-signal circuit model of the FET, show that, for the CG amplifier stage with $R_s = 0$ and $C_{ds} = 0$:

a. $A_v = \dfrac{(g_m + g_d)R_d}{1 + R_d(g_d + j\omega C_{gd})}$

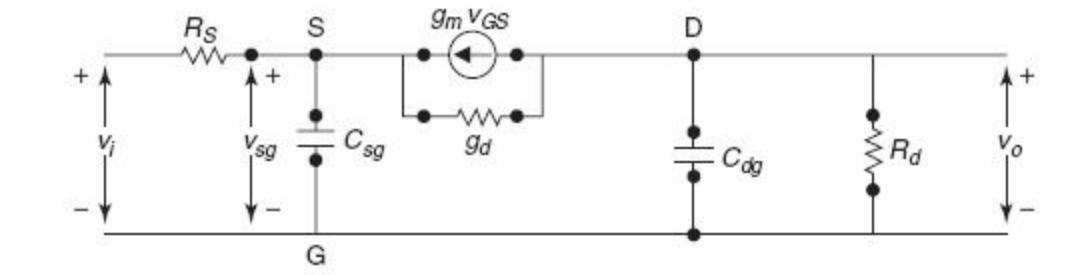
b. $Y_i = g_m + g_d(1 - A_v) + j\omega C_{sg}$

c. Repeat part (a), taking the source resistance R_S into account.

d. Repeat part (b), taking the source resistance R_S into account.

Solution:

The small-signal equivalent of a CG ampliifer can be drawn as shown in the following diagram:



a. $R_S = 0$, then $V_1 = V_{sg} = -V_{gs}$ $A_V = \dfrac{v_o}{v_i} = \dfrac{v_o}{v_{sg}}$

where,

$$v_o = I_{sc} Z \tag{1}$$

and,

$$i_{sc} = -g_m v_{gs} + g_d v_{sg} = (g_m + g_d) v_{sg}$$

Z = output impedance with $v_{sg} = 0$

Now,

$$Y = \frac{1}{Z} = \frac{1}{R_d} + g_d + j\omega C_{dg}$$

Substituting the values of I_{sc} and Z in Eq. (1):

$$v_o = \frac{g_m + g_d}{\frac{1}{R_d} + g_d + j\omega C_{dg}} \times v_i$$

Hence,

$$A_V = \frac{g_m + g_d}{\frac{1}{R_d} + g_d + j\omega C_{dg}} = \frac{(g_m + g_d) R_d}{1 + R_d (g_d + j\omega C_{dg})}$$

b. KCL at node S gives:

$$i_S = v_{sg} (j\omega C_{sg}) - g_m v_{gs} + g_d (v_{sg} - v_O)$$

$\therefore$

$$Y_1 = \frac{i_s}{v_{sg}} = j\omega C_{sg} + g_m + g_d (1 - A_V)$$

c. With

$$R_S \neq 0, v_{sg} = v_i - i_S R_S$$

where,

$$i_S = (g_m + g_d + j\omega C_{sg}) v_{sg} + R_S g_d v_O$$

we get,

$$v_{sg} = v_i - R_S (g_m + g_d + j\omega C_{sg}) v_{sg} + R_S g_d v_O$$

or,

$$v_{sg} = \frac{v_i + R_s g_d v_o}{1 + (g_m + g_d + j\omega C_{sg}) R_s}$$

Now, KCL at node D gives:

$$g_m v_{gs} + v_o \left(\frac{1}{R_d} + g_d + j\omega C_{dg} \right) = g_d v_{sg}$$

but, $v_{gs} = -v_{sg}$

so,

$$v_o\left(\frac{1}{R_d} + g_d + j\omega C_{dg}\right) = (g_m + g_d)v_{sg}$$

or,

$$v_o\left(\frac{1}{R_d} + g_d + j\omega C_{dg}\right) = \frac{(g_m + g_d)(v_i + R_s g_d v_o)}{1 + (g_m + g_d + j\omega C_{sg})R_s}$$

or,

$$v_o\left[\frac{1}{R_d} + g_d + j\omega C_{dg} - \frac{(g_m + g_d)R_s g_d}{1 + (g_m + g_d + j\omega C_{sg})R_s}\right] = \frac{(g_m + g_d)v_i}{1 + (g_m + g_d + j\omega C_{sg})R_s}$$

Hence,

$$A_V' = \frac{v_o}{v_i}$$

$$= \frac{(g_m + g_d)}{\left(\frac{1}{R_d} + g_d + j\omega C_{dg}\right)\,[1 + (g_m + g_d + j\omega C_{sg})R_s] - (g_m + g_d)R_s g_d}$$

d. With $R_S \neq 0$:

$$Y_1' = \frac{1}{R_s + \frac{1}{Y_1}} = \frac{Y_1}{1 + R_s Y_1}$$

$$= \frac{j\omega C_{sg} + g_m + g_d(1 - A_V)}{1 + R_s[j\omega C_{sg} + g_m + g_d(1 - A_V)]}$$

Example 7-47 (a) For the source follower with $g_m = 2$ mA/V, $R_s = 100$ K and $r_d = 50$ K, and with each inter-node capacitance 3pF, find the frequency at which the reactive component of the output admittance equals the resistive component. (b) At the frequency found in part (a), calculate the gain and compare it with the low-frequency value.

Solution:

a. From the equation of input admittance, we have $Y_0 = g_m + g_d + j\omega C_T$

but,

$$C_T = C_{gs} + C_{ds} + C_{sn} = 9\,pF$$

Hence,

$$\omega C_T = g_m + g_d$$

or,

$$\omega = \frac{2 \times 10^{-3} + 2 \times 10^{-5}}{9 \times 10^{-12}}$$

$$= \frac{2.02 \times 10^{-3}}{9 \times 10^{-12}} = 0.224 \times 10^{9}$$

or,

$$f = 0.356 \times 10^{6} = 35.6 \text{ MHz}$$

b. At low frequencies the gain is given by:

$$A_V = \frac{g_m R_s}{1 + (g_m + g_d)R_s}$$

$$= \frac{200}{1 + 202} = \frac{200}{203} = 0.985$$

For, $f = 35.6$ MHz, $\omega = 0.224 \times 10^{9}$.

$\therefore j\omega C_{gs} = j\ 0.224 \times 10^{9} \times 3 \times 10^{-12} = j\ 0.672 \times 10^{-3}$

$j\omega C_T = j\ 0.224 \times 10^{9} \times 9 \times 10^{-12} = j\ 2.02 \times 10^{-3}$

We have:

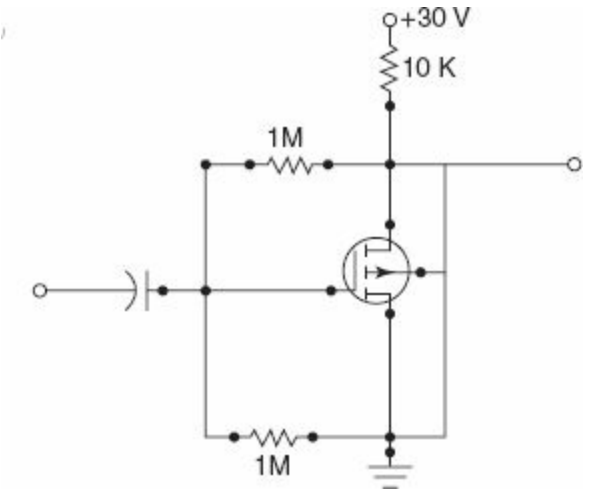
$$A_V = \frac{(1 + j\,0.672) \times 10^{-3} \times 10^{5}}{1 + 2.02(1 + j) \times 10^{-3} \times 10^{5}} = \frac{200 + j67.2}{202(1 + j)}$$

Hence,

$$|A_V| = \frac{10^2 \sqrt{4 + 0.45}}{202\sqrt{2}}$$

= 0.738 as compared to 0.985 at low frequencies.

Example 7-48 The drain current (in milliamperes) of the enhancement-type MOSFET, as shown in the diagram, is given by $I_D = 0.2(V_{Gs} - 3)^2$ in the region $V_{Ds} \geq V_{Gs} - V_P$. If $V_P = +3$ V, calculate the quiescent values I_D, V_{GS} and V_{DS}.



Solution:

Given, $I_D = 0.2(V_{GS} - 3)^2$

where, from the circuit we have:

$$V_{GS} = \frac{1}{2}(30 - 10I_D)$$

Substituting and solving we obtain:

$$I_D = 0.2(15 - 5I_D - 3)2 = 0.2(144 - 120I_D + 25I_D{}^2)$$

or,

$$5I_D - 25I_D + 28.8 = 0$$

Then, $I_D = \frac{25 \pm \sqrt{625 - 576}}{10} = \frac{25 \pm \sqrt{49}}{10}$ and I_D = 1.8 mA or 3.2 mA.

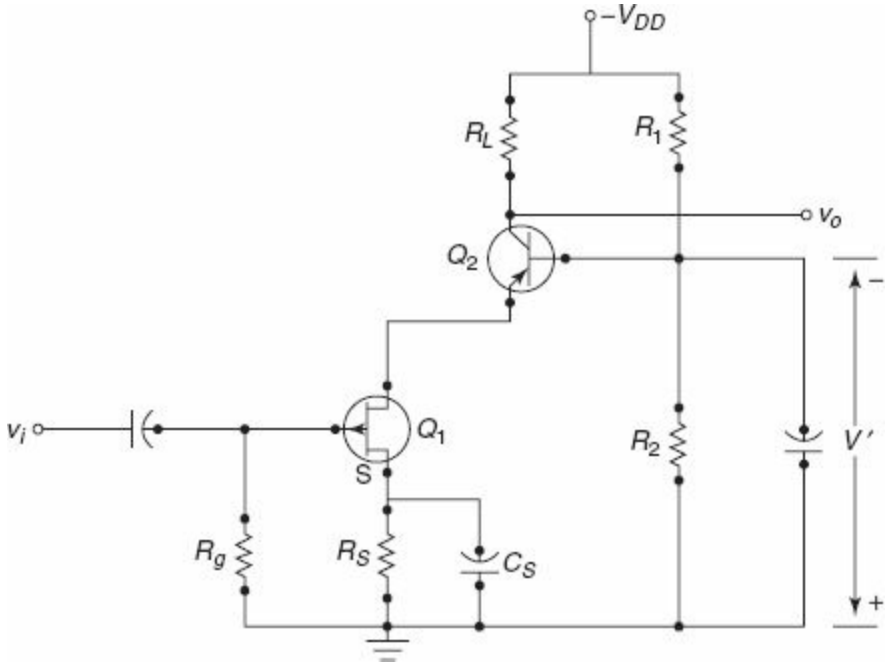
The second value of I_D is rejected since $V_{GS} = 3(30 - 32) = -1$V and the FET will be cut off. Therefore, I_D = 1.8 mA. Then:

$$V_{GS} = \frac{1}{2}(30 - 18) = +6 \text{ V}$$

and,

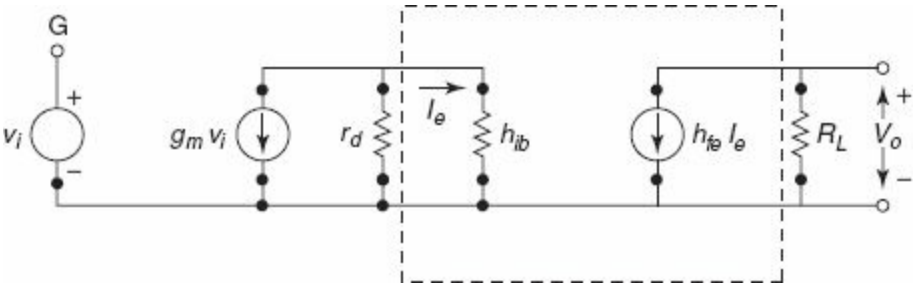
$$V_{DS} = 30 - 1.8 \times 10 = -12 \text{ V}$$

Example 7-49 For the given FET circuit show that if load resistance $R_L << 1/h_{ob2}$, the voltage gain of the hybrid cascade amplifier stage is given to a very good approximation by $A_V = g_m h_{fb} R_L$ where, g_m is the FET transconductance.



Solution:

From the equivalent circuit, as shown in the following diagram, we have:



$$v_o = -h_{fb} i_e R_L$$

where,

$$i_e = -g_m v_1 \frac{r_d}{r_d + h_{ib}} = -g_m v_1$$

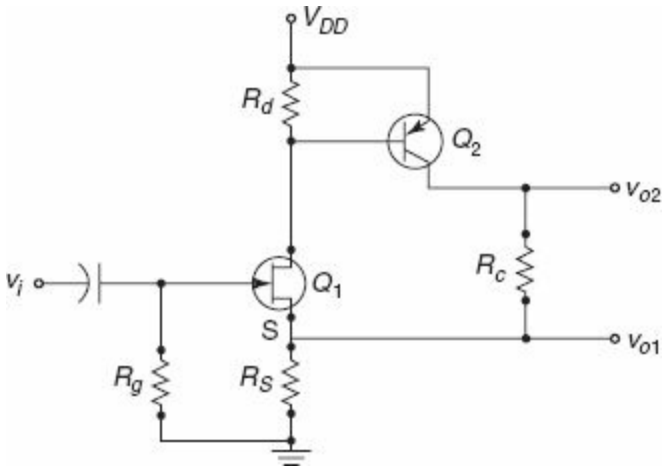
since,

$$r_d >> h_{ib}$$

Substitutin, we obtain:

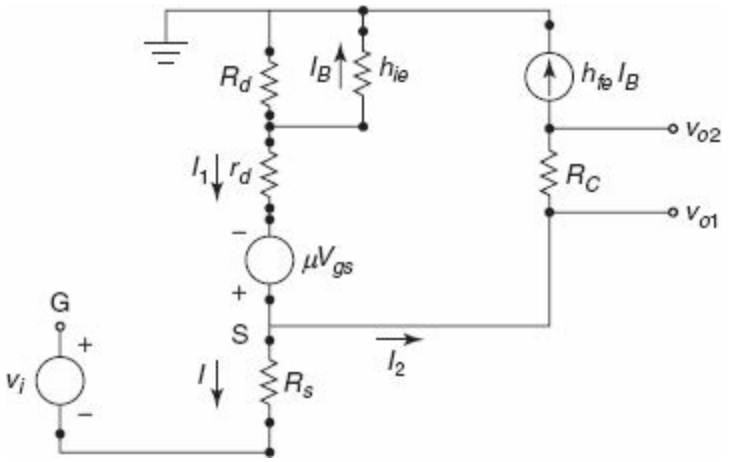
$$A_V = \frac{v_o}{v_1} = -h_{fb} R_L (-g_m) = h_{fb} R_L g_m$$

Example 7-50 For the circuit, as shown in the diagram, if $h_{ie} << R_d$, $h_{ie} << r_d$, $h_{fe} >> 1$, and $\mu >> 1$, show that (a) $A_{v1} = v_{o1}/v_i \approx g_m h_{fe} R_s / 1 + g_m h_{fe} R_s$ and (b) $A_{v2} = v_{o2}/v_i \approx g_m h_{fe} (R_s + R_c)/1 + g_m h_{fe} R_s$ where, g_m is the FET transconductance.



Solution:

The small-signal equivalent circuit is as shown in the following diagram.



The approximate equivalent circuit is used for Q_2.

From the circuit, $v_{gs} = v_1 - IR_s$, where, $I = I_1 - I_2 = I_1 - h_{fe}I_B$.

Since $h_{ie} << R_D$, then:

$$I_B \approx -I_i, I = (1 + h_{fe})I_i$$

KVL in the FET loop gives:

$$[h_{ie} + i_d + R_s(1 + h_{fe})]\, I_1 = \mu v_{gs} = \mu v_1 = \mu(1 + h_{fe})\, R_s\, I_1$$

or,

$$I_1 = \frac{\mu v_1}{h_{fe} + r_d + (\mu + 1)(1 + h_{fe})R_s} \approx \frac{g_m v_1}{1 + g_m h_{fe} R_s}$$

sinnce

$$r_d >> h_{ie}, h_{fe} >> 1 \text{ and } \mu >> 1$$

then,

$$v_{o1} = IR_s = (1 + h_{fe})R_s I_1 \approx h_{fe} R_s I_1$$

$\therefore$

$$A_{V1} = \frac{v_{o1}}{v_1} \approx \frac{g_m h_{fe} R_s}{1 + g_m h_{fe} R_s}$$

and

$$v_{o2} = v_{o1} - h_{fe} I_B R_C \approx (h_{fe} R_s + h_{fe} R_C) I_1 = h_{fe}(R_s + R_C) I_1$$

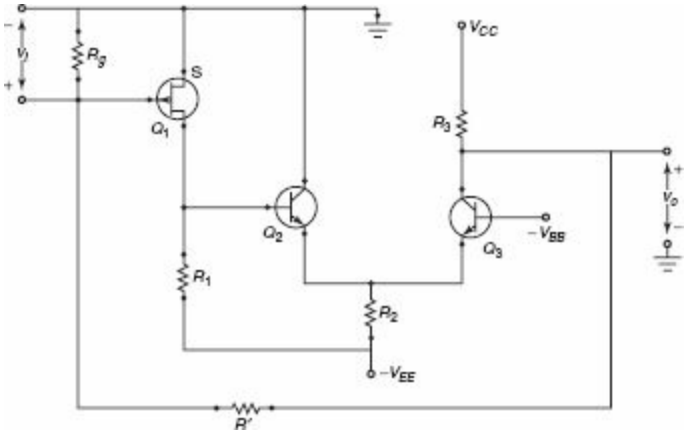
hence,

$$A_{V2} = \frac{v_{o2}}{v_1} \approx \frac{g_m h_{fe}(R_s + R_C)}{1 + g_m h_{fe} R_s}$$

Example 7-51 If $r_d >> R_1\, R_2 >> h_{ib3}$, $1/h_{oe2} >> h_{ib3}$, $R' >> R_3$ and $1/h_{ob3} >> R_3$, show that the

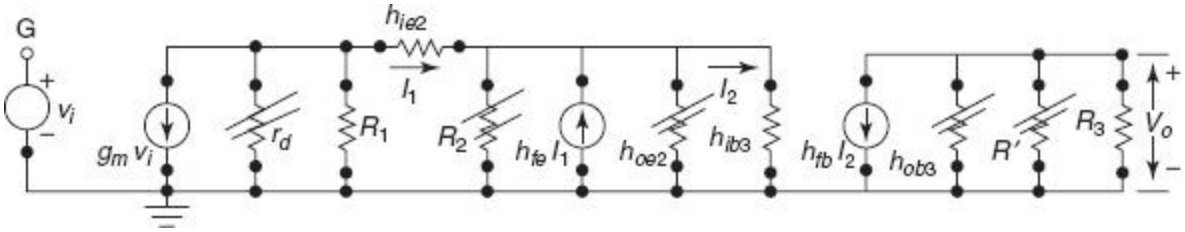
voltage gain at low frequencies is given by:

$$A_O = \frac{v_o}{v_i} = g_m(1 + h_{fe2})h_{fb3}\frac{R_1R_3}{R_1 + h_{ie2} + h_{ib3}(1 + h_{fe2})}$$



Solution:

A small-signal equivalent circuit of the amplifier is as shown in the following diagram.



It is assumed that h_r is negligible for Q_2 and Q_3.

Moreover, if $r_d >> R_1$, $R_2 >> h_{1bs}$, $\frac{1}{h_{oe2}} >> h_{1bs}$, $\frac{1}{h_{ob3}} >> R_s$ and $R' >> R_s$, we can cross out these elements as shown in the diagram.

Then,

$$v_o = -h_{fbs}I_2R_s \text{ where } I_s = (1 + h_{fe2})I_1$$

and,

$$I_1 = \frac{-g_m v_1 R_1 - (1 + h_{fe2})h_{ibs}I_1}{h_{ie2} + R_1}$$

or,

$$I_1 = \frac{-g_m v_1 R}{R_1 + h_{ie2} + (1 + h_{fe2})h_{ibs}}$$

$\therefore$

$$v_o = \frac{g_m(1 + h_{fe2})R_2R_sh_{fb2}v_1}{R_1 + h_{ie2} + (1 + h_{fe2})h_{ibs}}$$

Hence,

$$A_o = \frac{v_o}{v_1} = g_m(1 + h_{fe2})h_{fbs}\frac{R_1R_s}{R_1 + h_{ie2} + h_{ibs}(1 + h_{fe2})}$$

Note that A_o is negative, since h_{fbs} is a negative number. Thus, the feedback provided by R' is degenerative and stabilizing the amplifier at the same time.

Example 7-52 (a) A MOSFET connected in the CS configuration works into a 100 K resistive load. Calculate the complex voltage gain and the input admittance of the system for frequencies of 100 and 100,000 Hz. Take the inter-electrode capacitances into consideration. The MOSFET parameters are $\mu = 100$, $r_d = 40$ K, $g_m = 2.5$ mA/V, $C_{gs} = 4.0$ pF, $C_{ds} = 0.6$ pF and $C_{gd} = 2.4$ pF. Compare these results with those obtained when the inter-electrode capacitances are neglected. (b) Calculate the input resistance and the capacitance.

Solution:

$Y_{gs} = j\omega C_{gs} = j\ 2\pi \times 10^2 \times 4.0 \times 10^{-12} = j\ 2.51 \times 10^{-9}$ mho

$Y_{ds} = j\omega C_{ds} = j\ 2\pi \times 10^2 \times 0.6 \times 10^{-12} = j\ 3.77 \times 10^{-10}$ mho

$Y_{gd} = j\omega C_{gd} = j\ 2\pi \times 10^2 \times 2.4 \times 10^{-12} = j\ 1.51 \times 10^{-9}$ mho

$$g_d = \frac{1}{r_d} = 2.5 \times 10^{-5} \text{ mho}$$

$$Y_d = \frac{1}{R_d} = 10^{-5} \text{ mho}$$

$$g_m = 2.5 \times 10^{-3} \text{ mho}$$

The gain of a one-stage amplifier is given by:

$$A_V = \frac{-g_m + Y_{gd}}{g_d + Y_d + Y_{ds} + Y_{gs}} = \frac{-2.5 \times 10^{-3} + j1.51 \times 10^{-9}}{2.5 \times 10^{-5} + 10^{-5} + j1.88 \times 10^{-9}}$$

It is seen that the j terms are negligible in comparison with the real term. In that case:

$$A_V = -\frac{2.5}{3.5} \times 10^2 = -71.4$$

Since the gain is a real number, the input impedance consists of a capacitor whose value is given by:

$$\frac{Y_i}{j\omega} = C_i = C_{gs} + (1 + g_mR_d')C_{gd}$$

$$C_i = C_{gs} + (1 - A_V)C_{gd} = 4.0 + 72.4 \times 2.4 = 177.5 \text{ pF}$$

We repeat these calculations for $f = 10^6$ Hz.

Then,

$$Y_{gs} = j2.51 \times 10^{-6} \text{ mho}$$

$$Y_{ds} = j0.377 \times 10^{6} \text{ mho}$$

$$Y_{gd} = j1.51 \times 10^{-6} \text{ mho}$$

Hence,

$$A_V = \frac{-2.5 \times 10^{-3} + j1.51 \times 10^{-9}}{3.5 \times 10^{-5} + j0.188 \times 10^{-8}} = \frac{-2.5 \times 10^{-3}}{3.5 + j0.188} \times 10^{6}$$

$$= \frac{-2.5 \times 3.5 \times 10^{2}}{12.30} + j\,\frac{2.5 \times 0.188 \times 10^{2}}{12.30}$$

$$= -71.2 + j3.82$$

From the equation, $Y_i = Y_{gs} + (1 - A_V)Y_{gd}$ we have:

$$G_1 + j\omega C_1 = j\omega C_{gs} + 72\, j\omega C_{gd} + 3.82\, \omega C_{gd}$$

or,

$$C_1 = C_{gs} + 72\, C_{gd} = 177 \text{ pF}$$

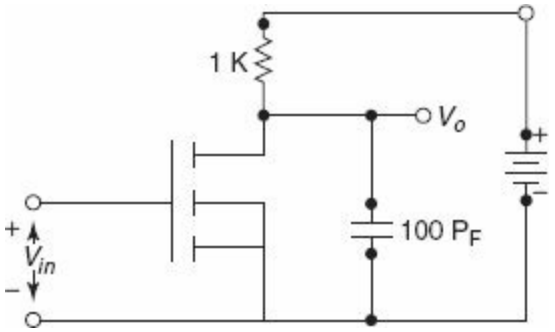
or,

$$G_1 = 2\pi \times 10^{6} \times 2.4 \times 10^{-12} \times 3.82 = 0.580 \times 10^{-6} \text{ mho}$$

$$R_1 = 1.735 \times 10^{6}\Omega = 173.5 \text{ k}\Omega$$

Example 7-53 An *n*-channel MOSFET having a V_T of 2 V (threshold voltage) is used in the circuit, as shown in the following diagram. Initially T is OFF and in a steady state. At time $t = 0$, a step voltage of magnitude 4 V is applied to the input so that the MOSFET turns on instantaneously. Draw the equivalent circuit and calculate the time taken for the output V_o to fall to 5 V. The device constant of the MOSFET is given by:

$$\frac{1}{2} k_n' \frac{W}{L} = K = 5 \text{ mA/V}^2,\ R_{DS} = \infty, C_{DS} = 0;\ C_{DG} = 0.$$



Solution:

Given *n*-channel MOSFET:

$$V_T = 2$$

T is in the OFF and steady state, therefore, MOS turns on:

$$K = 5\ \text{mA}/V^2,\ R_{DS} = \infty,\ C_{DS} = 0,\ C_{DG} = 0$$

Assuming that initally the capacitor is charged to 10 V, as the MOSFET is OFF:

$$V_{Gs} = 4\ \text{V}$$

$$I_D = K(V_{GS} - V_T)2$$

$$= 5(4 - 2)2 = 20\ \text{mA}$$

In the saturation region:

$$V_{GS} > V_T \quad \text{(satisfied)}$$

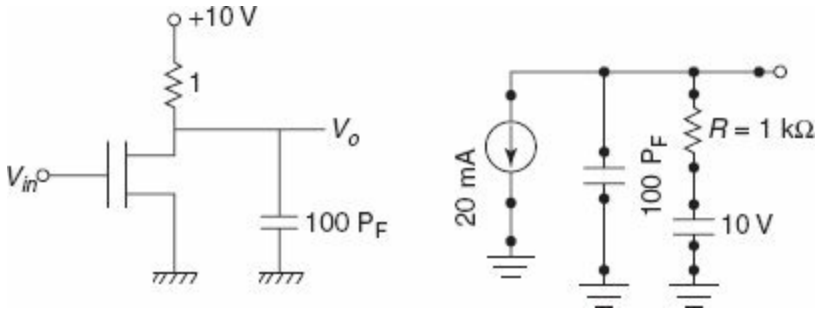
$$V_{GD} > V_T$$

$$\alpha_1 - V_o\ 2 \Rightarrow -V_o - 2$$

$\therefore$

$$V_o\ 2\ \text{V}$$

Since V_o falls only to 5 V, the MOSFET is in the pinch-off region.



Application of KCL to the model gives:

$$2 \times 10^3 = -\frac{Cdv_o}{dt} + \frac{10 - V_o}{R}$$

Taking Laplace transform:

$$\frac{20 \times 10^{-3}}{5} = 10 \times 10^{12}[SV_o(s) - V_o(0)] + \frac{10 \times 10^{-3} V_o(S) \times 10^{-3}}{5} + \frac{10 \times 10^{-3}}{5}$$

$$= -V_o(S)[10 \times 10^{12} S - 10^3] + 100 \times 10^{12}$$

$$(S + 10^7)V_o(s) = -\frac{10^8}{5} - 10$$

$$V_o(S) = \frac{10^8}{S(S + 10^7)} = \frac{10}{S(S + 10^7)}$$

$$V_o(S) = \frac{10}{5} - \frac{10}{S + 10^7} - \frac{10}{S(S + 10^7)}$$

Inverse Laplace gives:

$$V_o(t) = 10^2 e^{-t}(10^7)$$

$$V_o = 5 \text{ V}$$

⇒

$$5 = 20(1^{-t} \times 10^7)$$

⇒

$$t = 10^{-7} \log_e^4 = 13.8 \times 10^{-8} = 138 \text{ ns}$$

Example 7-54 An *n*-channel has $I_{DSS} = 1$ mA and $V_p = -5$ V. Find the maximum transconductance.

Solution:

Given,

$$I_{DSS} = 1 \text{ mA and } V_p = -5 \text{ V}$$

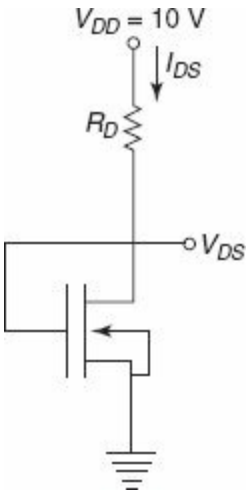
It can be shown that the transconductance of the FET is:

$$g_m = \frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) = \frac{2I_{DSS}}{|V_P|} = \frac{2 \times 1 \times 10^{-3}}{5} \text{ millimho} = 0.4 \text{ millimho}$$

Example 7-55 An NMOS circuit is shown in the given diagram. The specifications of the circuit are as follows:

$$V_{DD} = 10\text{ V}; \beta = k\left(=\frac{1}{2}k_n'\frac{W}{L}\right) = \mu n\, C_{ox}(W/L) = 10^{-4}\text{A/V}_2$$

$V_T = 1$ V and $I_{DS} = 0.5$ mA. Evaluate V_{DS} and R_D for the circuit. Neglect body-effect for V_T.



Solution:
Given an NMOS circuit, for which:

$$\beta = 10^{-4}\text{ A/}V^2,\ V_{DD} = 10\ V,\ V_T = 1\ V,\ I_{DS} = 0.5\text{ mA}.$$

We know, in saturation:

$$I_D = K(V_{GS} - V_T)^2$$

$$5 \times 10^{-4} = 10^{-4} \times (V_{GS} - 1)^2$$

and,

$$V_{DS} = V_{GS} = 3.24\text{ V}$$

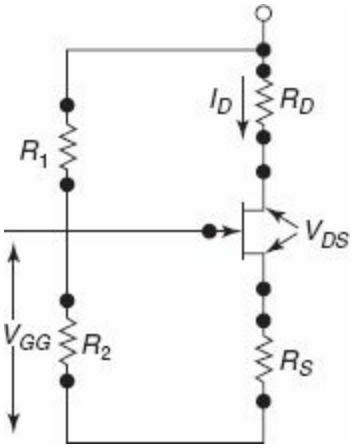
Hence,

$$R_D = \frac{V_{DD} - V_{DS}}{I_{DS}} = \frac{10 - 3.24}{0.5} = 13.5\text{ K}$$

Example 7-56 A JFET amplifier with a voltage divider biasing circuit, as shown in the following diagram, has the following parameters: $V_p = -2$ V, $I_{DSS} = 4$ mA $R_D = 910\ \Omega$, $R_S = 3\ \text{k}\Omega$, $R_1 = 12\ \text{M}\Omega$, $R_2 = 8.57\ \text{M}\Omega$ and $V_{DD} = 24$ V. Find the value of the drain current I_D at the operating point. Verify whether the FET will operate in the pinch-off region.

Solution:

$$V_{GG} = V_D \frac{R_2}{R_1 + R_2} = 24 \times \frac{8.57 \times 10^6}{(12 + 8.57)10^6} = 10 \text{ V}$$



From the gate-source loop:

$$V_{GS} = V_{GG} - I_D R_S \qquad (1)$$

Using Eq. (1) we have:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 4\left(1 - \frac{10 - I_D \times 3}{2}\right)^3$$

$$9I_D^2 - 73I_D + 144 = 0$$

$$I_D = 3.39 \text{ mA or } 4.72 \text{ mA}$$

$$I_D = 4.72 \text{ mA} > 4 \text{ mA} = I_{DSS}$$

This value is inappropriate so, $I_{DQ} = 3.39$ mA is selected.

$$V_{GSQ} = V_{GG} - I_{DQ}R_S$$

$$= 10 - (3.39 \times 10^{-3} \times 10^3) = -0.17 \text{ V}$$

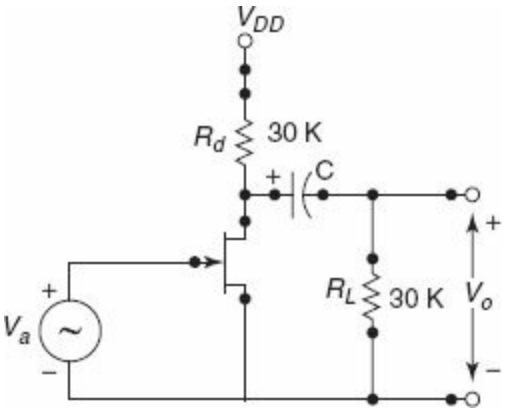
$$V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)$$

$$= 24 - 3.39 \times 10^{-3}\,(0.91 + 3) \times 10^3 = 10.74$$

$$V_{DGQ} = V_{DSQ} - V_{GSQ} = 10745 + 0.17 = 10.915 \text{ V}$$

which is greater than $|V_D| = 2$ V
Hence the FET is in the pinch-off region.

Example 7-57 (a) Calculate the voltage gain $A_V = V_o / V_i$, at 5 KHz for the circuit, as shown in the diagram. The FET parameters are $g_m = 2$ mA/V and $r_d = 10$ K. Neglect capacitances.(b) Repeat part (a) if the capacitance 0.025 μF is taken under consideration.



Solution:

$$g_m = \frac{2\text{mA}}{V}; r_d = 10\text{ K}$$

a.

$$R_L' = 30\text{ K} \parallel 30\text{ K} = \frac{30 \times 30}{30 + 30} = 15\text{ k}\Omega$$

$$A_V = \frac{V_o}{V_i} = \frac{-\mu R_L'}{R_L' + r_d + R_s(1 + \mu)} = -\frac{g_m r_d R_L'}{R_L' + r_d}$$

$$= \frac{-(2 \times 10^{-3})(10 \times 10^3)(15 \times 10^3)}{(15 \times 10^{-3}) + (10 \times 10^3)}$$

$$A_V = -29.99 \approx -30$$

b.

$$C = 0.025\ \mu\text{F}$$

$$f_1 = \frac{1}{2\pi(r_d \| R_d + R_L)C_C}$$

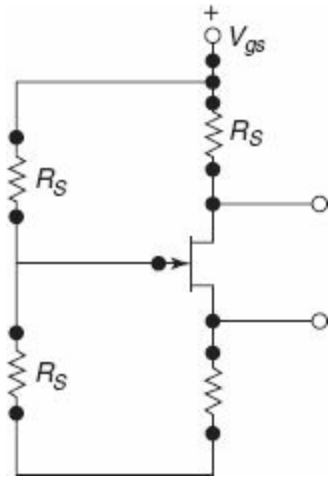
$$f_1 = \frac{1}{2\pi(10\text{ K} \| 30\text{ K}) + 30\text{ K})0.025 \times 10^{-6}} = 169.7\text{ Hz}$$

$\therefore$

$$A_{VL} = \frac{A_v}{\sqrt{1 + \left(\frac{f_1}{f}\right)^2}} = \frac{-30}{1 + \left(\frac{169.7}{5k}\right)^2}$$

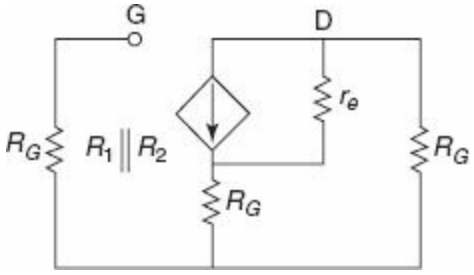
Example 7-58 Consider the JFET circuit as given in the diagram.

a. Determine the resistance seen from terminal 2 and the ground at low frequencies.
b. Valuate the resistance in part (a) for $R_D = 4\text{ k}\Omega$, $R_S = 2.5\text{ k}\Omega$, $R_1 = 20\text{ k}\Omega$, $R_2 = 100\text{ k}\Omega$, $g_m = 2.5$ ms and $r_d = 60\text{ k}\Omega$.
c. Repeat part (b) if $R_D = 0$.

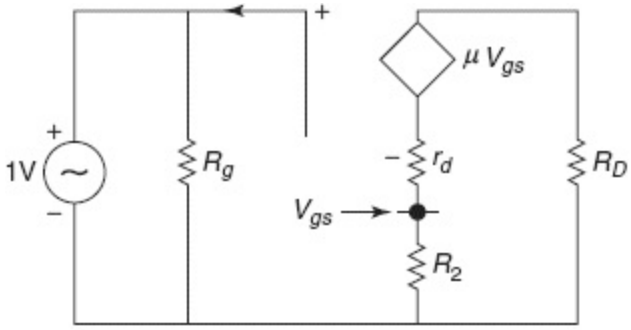


Solution:

The small-signal model of the circuit is as shown in the given diagram. Use of Thevenin's equivalent converts the circuit, as shown in the following diagram.



If an input signal of 1 V is applied:



$$V_{gs} = 1 - R_S \left(\frac{\mu V_{gs}}{r_d + R_S + R_D} \right)$$

$$V_{gs} = \left(\frac{r_d + R_S + R_D}{r_d(1 + \mu)R_S + R_D} \right) \quad (\because \quad V_i = 1 \text{ V})$$

Open circuit voltage V_{2G} (O.C.) at terminal 2:

$$= \left(\frac{\mu V_{gs}}{r_d + R_S + R_D} \right) \times R_S = \left(\frac{\mu R_S}{r_d + (1 + \mu)R_S + R_D} \right)$$

Short circuit current (terminal 2 shorted to G):

$$V_{gs} = V_1 = 1 \text{ V (as } R_S \text{ is shorted)}$$

$$I_{2G}(\text{S.C.}) = \frac{\mu V_{gs}}{r_d + R_D} = \frac{\mu V_{gs}}{r_d + R_D}$$

a. Resistance as seen from terminal 2 and G:

$$R_o = \frac{V_{2G}(\text{O.C})}{I_{2G}(\text{S.C.})}$$

$$= \frac{\mu R_s}{r_d + (1 + \mu R_S) + R_D} \times \frac{(r_d + R_d)}{\mu} = \frac{1}{1 + \dfrac{(1 + \mu)R_S}{r_d + R_D}}$$

b.

$$R_o = \frac{2.5}{1 + \dfrac{(1 + 2.5 + 60)2.5}{60 + 4}} = 362\ \Omega$$

c.

$$R_D = 0$$

$$R_o = \frac{2.5}{1 + \dfrac{(1 + 2.5 + 60)2.5}{60 + 4}} = 343\ \Omega$$

Example 7-59 Design a source follower circuit at *Q*-point having $V_{DS} = 14$ V, $I_{DQ} = 3$ mA, $V_{DD} = 20$ V, $g_m = 2$ ms, $r_d = 50$ k, $V_{\text{Gs}} = -1.5$ V.

Solution:

The circuit of the bootstrapped source follower may be considered for this.

Therefore,

$$20 \text{ V} = 14 \text{ V} + 3 \text{ mA } (R_1 + R_2)$$

$$R_1 + R_2 = 2 \text{ K}$$

$$-1.5/-3 \text{ mA } R_1 \Rightarrow R_1 = 0.5 \text{ K}$$

$$R_2 = 2 - 0.5 = 1.5 \text{ K}$$

Output resistance:

$$R_o = \frac{1}{g_m} = \frac{1}{2\text{ ms}} = 0.5\text{ k}\Omega$$

$$V_s = A_v^1 V_g \frac{(R_1 + R_2)}{R_1 + R_2 - \frac{1}{g_m}} = A_v^1 V_g \frac{2\text{ k}}{2\text{ k} + 0.5\text{ k}}$$

$$A_V = \frac{V_s}{V_g} = 0.8 A_v^1$$

The effective input resistance is expressed as:

$$R_1 = \frac{R_3}{1 + \frac{V_s}{V_g}\left(\frac{R_2}{R_1 + R_2}\right)}$$

$$= \frac{R_3}{1 - 0.8A_V \times \frac{0.5\text{ K}}{2\text{ K}}}$$

$$= \frac{R_3}{1 - 0.8 \times 0.25} = \frac{R_3}{0.8} = 1.25\, R_3$$

7-7 ADDITIONAL FET CIRCUITS

FET circuits are used extensively in the modern semiconductor industry. The Fin FET, for example, is very popular among microprocessor manufacturers. In the Fin FET, the source/drain region forms "fins" on the silicon surface; thus, the name. The FREDFET (fast-reverse epitaxial diode field-effect transistor) and the EOSFET (electrolyte-oxide-semiconductor field-effect transistor) are FET circuits that are used in motors and neurochips respectively. The OFET (organic field-effect transistor) uses an organic semiconductor compound and it can be used as a light-emitting device. Apart from these there are numerous modern FET circuits available in the market today. Some of these are discussed in the following sections.

7-7-1 MOS Differential Amplifiers

MOS differential amplifiers are one of the most important building blocks in MOS analog circuits. Figure 7-17 depicts the MOS differential pair.

Figure 7-17 shows two matched MOSFETs Q_1 and Q_2, biased with a constant current source. Here, the loads of the differential amplifiers are not shown. A relation needs to be found between the drain current and the input voltage. Also, it is assumed that the two MOSFETs operate in the saturation region.

The drain currents of the two transistors are given by:

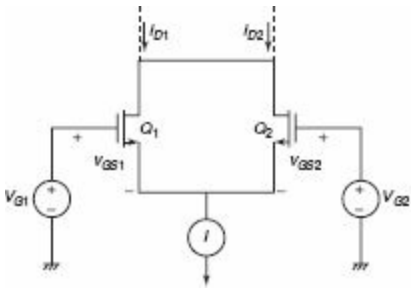


Figure 7-17 Circuit representation of a differential amplifier

$$i_{D1} = \frac{1}{2} k_n' \frac{W}{L} (V_{gs1} - V_T)^2 \qquad (7\text{-}36a)$$

and,

$$i_{D2} = \frac{1}{2} k_n' \frac{W}{L} (V_{gs2} - V_T)^2 \qquad (7\text{-}36b)$$

Subtracting Eq. (7-36b) from Eq. (7-36a), and replacing $v_{gs1} - v_{gs2} = v_{id}$, we obtain:

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2} k_n' \frac{W}{L}} v_{id} \qquad (7\text{-}37)$$

The constraint imposed by the current source is given by:

$$i_{D1} + i_{D2} = I \qquad (7\text{-}38)$$

Solving Eq. (7-37) and Eq. (7-38) we obtain:

$$i_{D1} = \frac{I}{2} + \sqrt{k_n' \frac{W}{L} I} \frac{v_{id}}{2} \sqrt{1 - \frac{(v_{id}/2)^2}{I/k_n' \frac{W}{L}}}$$

$$i_{D2} = \frac{I}{2} - \sqrt{k_n' \frac{W}{L} I} \frac{v_{id}}{2} \sqrt{1 - \frac{(v_{id}/2)^2}{I/k_n' \frac{W}{L}}}$$

Also, when the circuit is at the quiescent point, we have:

$$i_{D1} = i_{D2} = \frac{I}{2} \quad \text{and} \quad v_{GS1} = v_{GS2} = V_{GS}$$

where,

$$\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_T)^2$$

We know that:

$$g_m = \frac{2I_D}{(V_{GS} - V_T)}$$

In this case, we have:

$$g_m = \frac{2I_D}{(V_{GS} - V_T)}, \text{ (since we already have } i_{D1} = i_{D2} = i/2)$$

7-7-2 Current Source Circuits

The concept of a power supply should be clear before we proceed to study the current source circuits. A practical current source is a voltage source where the resistance, in series with the voltage source, is zero. It is a current supply with a resistance in parallel. An ideal current source provides a constant current regardless of the load connected to it. Constant current sources are built using FET devices, as shown in Fig. 7-18.

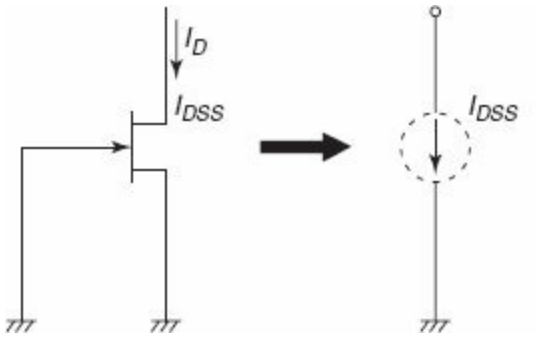


Figure 7-18 MOSFET current source

If the voltage V_{GS} is set to zero, the drain current is fixed at a constant current. Thus, we find that the essential condition for a MOSFET to operate as a current source is to operate the device in the saturation region. This can be easily found by a detailed look at the transfer characteristics.

7-8 COMPARISON BETWEEN THE FET AND THE BJT

Now that we have studied the field-effect transistor and the bipolar-junction transistor in detail, let us map their respective characteristics and draw a comparison between the two.

1. In the BJT, the carriers are transported by the process of diffusion but in the FET, it is the drift mechanism that helps the movement of carriers.
2. In the FET, carriers of only one type—either electron or hole (majority carrier)—are responsible for the conduction, but for the BJT both types of carriers—electrons and holes (majority and minority)—are involved in current conduction.
3. The FET is thermally more stable than the BJT, which is the primary reason behind the extensive usage of the FET.
4. The FET is a voltage-controlled device or voltage amplifier, whereas the BJT is a current-controlled device or current amplifier.
5. The input impedance offered by the FET is much higher than that offered by the BJT.
6. The FET is easy to fabricate, and hence all the ICs use the FET as their basic technology.
7. Fabrication of the FET requires less space compared to the BJT; therefore, the FET is usually preferred for the VLSI design.
8. The FET is less noisy compared to the BJT, which facilitates their extensive usage in communication devices.
9. The FET offers high power gain compared to the BJT.

POINTS TO REMEMBER

1. The FET is a voltage-controlled unipolar device with high input impedance.

2. As long as the device is in the active region, the FET characteristic equations do not change with each network connection.
3. The network or the biasing assembly simply defines the level of current and voltage associated with the operating point through its own set of equations.
4. The self-bias arrangement eliminates the need for two voltage supplies.
5. To operate the MOSFET as an amplifier, it must be biased in the linear region where we obtain a linear variation between the input voltage and the output voltage.
6. Under proper operation of the device as an amplifier, the signal quantities are superimposed on dc quantities. Thus, the total drain current under any such arrangements of the MOSFET in a circuit, is the superimposition of the dc current and the small-signal current. Similar is the case for output voltage.
7. A simple circuit transformation causes the small-signal ac model of a MOSFET to lead to the formation of the T equivalent circuit.
8. The high-frequency model of the MOSFET takes into account the various capacitances of the device.
9. The parameter to judge the high-frequency operation of the MOSFET as an amplifier is given by the unity-gain frequency. It is defined as the frequency at which the short-circuit gain of the common-source arrangement becomes unity.

IMPORTANT FORMULAE

1. For the depletion-type MOSFET and for the JFET, the basic relation guiding the input and output quantities is given by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

2. For the enhancement-type MOSFET, Shockley's equation gets modified and is given by:

$$I_D = k\,(V_{GS} - V_T)^2$$

3. The basic equations for the JFET/depletion-type MOSFETs.
   a. Fixed bias configuration:

$$V_{GS} = -V_{GG} = V_G$$

   b. Self bias configuration:

$$V_{GS} = -I_D R_S$$

   c. Voltage divider biasing configuration:

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$
$$V_{GS} = V_G - I_D R_s$$

4. The dc bias point required to operate the MOSFET device as an amplifier is obtained by solving the basic equation as given by:

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_T)^2$$

(neglecting channel width modulation). And the drain voltage of the circuit is:

$$V_D = V_{DD} - I_D R_D$$

5. The instantaneous drain current is obtained after the bias point is introduced and is given by:

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} + v_{gs} - V_t)^2$$
$$= \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 - k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$
$$+ \frac{1}{2} k_n' \frac{W}{L} + v_{gs}^2$$

6. For small-signal analysis, we have the instantaneous drain current as:

$$i_D = I_D + i_d$$

and,

$$i_d = k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

This is obtained only on the condition that:

$$\frac{1}{2} k_n' \frac{W}{L} v_{gs}^2 \ll k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

which results in $v_{gS} << 2(V_{GS} - V_t)$

7. Equivalent transconductance is given by:

$$g_m = \frac{i_d}{v_{gs}} = k_n' \frac{W}{L} (V_{GS} - V_T)$$

8. Small-signal component of drain voltage is:

$$v_d = -i_d R_D = -g_m R_D v_{gs} \Rightarrow \frac{v_d}{v_{gs}} = -g_m R_D$$

9. Voltage gain for a MOSFET amplifier is given by:

$$\frac{v_d}{v_{gs}} = -g_m (R_D \| r_o)$$

where, $r_o = \frac{|V_A|}{I_D}$

10. Current gain in the high-frequency model of the MOSFET is given by:

$$\frac{I_o}{I_i} = \frac{g_m}{s(C_{gs} + C_{gd})}$$

11. Unity-gain frequency (bandwidth) is given by:

$$\omega_T = \frac{g_m}{(C_{gs} + C_{gd})}$$

12. The currents at the drain terminals of the differential amplifier are given by:

$$i_{D1} = \frac{I}{2} + \sqrt{k_n' \frac{W}{L}}\, I \frac{v_{id}}{2} \sqrt{1 - \frac{\left(\frac{v_{id}}{2}\right)^2}{\frac{I}{k_n' \frac{W}{L}}}}$$

$$i_{D2} = \frac{I}{2} - \sqrt{k_n' \frac{W}{L} I}\,\frac{v_{id}}{2}\sqrt{1 - \frac{\left(\frac{v_{id}}{2}\right)^2}{\frac{I}{k_n' \frac{W}{L}}}}$$

And the transconductance in this case is given by:

$$g_m = \frac{I_D}{(V_{GS} - V_T)}$$

OBJECTIVE QUESTIONS

1. For an *n*-channel JFET, with a constant drain-source voltage, if the gate-source voltage is increased (more negative) pinch-off would occur for:
    a. High values of drain current
    b. Saturation value of drain current
    c. Zero drain current
    d. Gate current equal to drain current
2. For a junction FET in the pinch-off region, as the drain voltage is increased the drain current:
    a. Becomes zero
    b. Abruptly decreases
    c. Abruptly increases
    d. Remains constant
3. In modern the MOSFET, the material used for the gate is:
    a. High-purity silicon
    b. High-purity silica
    c. Heavily doped polycrystalline silicon
    d. Epitaxially grown silicon
4. The threshold voltage of an *n*-channel MOSFET can be increased by:
    a. Increasing the channel dopant concentration
    b. Reducing the channel dopant concentration
    c. Reducing the gate oxide thickness
    d. Reducing the channel length
5. An *n*-channel JFET has a pinch-off voltage of $V_P = -5$ V, $V_{DS(max)} = 20$ V and $g_m = 2$ mA/V. The minimum 'ON' resistance is achieved in *n*th JFET for:
    a. $V_{GS} = -7$ V and $V_{DS} = 0$ V
    b. $V_{GS} = 0$ V and $V_{DS} = 0$ V
    c. $V_{GS} = 0$ V and $V_{DS} = 20$ V
    d. $V_{FGS} = -7$ V and $V_{DS} = 20$ V
6. A JFET has $I_{DSS} = 10$ mA and $V_P = 5$ V. The value of the resistance R_S for a drain current $I_D = 6.4$ mA is:
    a. 150 Ω
    b. 470 Ω
    c. 560 Ω
    d. 1 kΩ
7. FET is:
    a. Bipolar
    b. Unipolar
    c. Tripolar
    d. None of the above
8. In an FET, the transconductance g_m is proportional to:

a. I_{DS}
b. I^2_{DS}
c. $\sqrt{I_{DC}}$
d. $1/I_{DSS}$

9. In an FET, g_{mo} is pel to:
   a. I_{DSS}
   b. $\sqrt{I_{DSS}}$
   c. I^2_{DSS}
   d. $1/I_{DSS}$
10. In a JFET, transconductance g_m is of the order of:
   a. 1 mS
   b. 100 mS
   c. 1 S
   d. 100 S
11. In an FET, dynamic drain resistance r_d is of the order of:
   a. 1 kΩ
   b. 10 kΩ
   c. 100 Ω
   d. 100 kΩ
12. In a MOSFET, dynamic drain resistance *rd* is of the order of:
   a. 10 kΩ
   b. 1 kΩ
   c. 10 Ω
   d. 100 kΩ
13. The input resistance r_{gs} in the small-signal model of the MOSFET is of the order of:
   a. 100 kΩ
   b. 1 MΩ
   c. 100 MΩ
   d. 10^4 MΩ
14. The feedback resistance r_{gd} in the small-signal model of the MOSFET is of the order of:
   a. 1 MΩ
   b. 100 MΩ
   c. 10^4 MΩ
   d. 10^6 MΩ
15. The feedback capacitance C_{gd} in the small-signal model of the JFET is of the order of:
   a. 5 pF
   b. 15 pF
   c. 500 pF
   d. 1 pF
16. The drain-to-source resistance C_{ds} in the high-frequency model of the JFET is of the order of:
   a. 1 pF
   b. 10 pF
   c. 100 pF
   d. 1000 pF
17. The gate-to-source resistance C_{gs} in the high-frequency model of the JFET is of the order of:
   a. 5 pF
   b. 50 pF
   c. 500 pF
   d. 5000 pF
18. The gain bandwidth of an FET amplifier w.r.t. a BJT amplifier is:

a. Low
b. High
c. Equal
d. Zero

19. Voltage gain of a common-gate amplifier with $\mu = 15$, $r_d = 20$ K, and $R_L = 2$ K, internal resistance of the voltage source is:
    a. 0.64
    b. 6.4
    c. 0.89
    d. 0.9
20. The input resistance of a BJT amplifier w.r.t. its FET counterpart is:
    a. More
    b. Less
    c. Equal
    d. None of the above
21. Total input capacitance across the input terminals of a CS amplifier at high frequency with $r_d = 20$ K, $R_D = 5$ K, $g_m = 5$ ms, C_{gs}, = 8 pF, $C_{gd} = 4$ pF and C_{ds}, = 2 pF is:
    a. 44 pF
    b. 76 pF
    c. 26 pF
    d. 22 pF
22. CMOS is equal to:
    a. NMOS + PMOS
    b. PMOS + PMOS
    c. VMOS + NMOS
    d. None of the above
23. CMOS is formed by the:
    a. Twin tub method
    b. CZ method
    c. LPE method
    d. None of the above

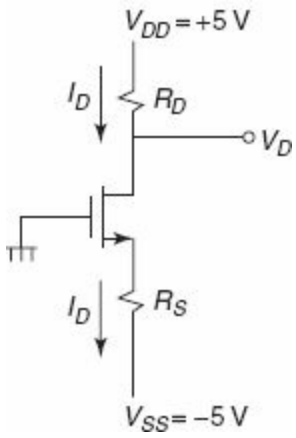
REVIEW QUESTIONS

1. Define the following:
    a. Transconductance
    b. Drain resistance
    c. Amplification factor of an FET
2. Show the small-signal model of the FET at (a) low frequencies and (b) high frequencies. Account for the drastic changes in this model.
3. Point out and discuss the capacitances of the general device that have been included in the high-frequency model.
4. Draw the MOSFET NOR circuit and discuss its operation.
5. Draw a MOSFET NAND circuit.
6. Explain how a MOSFET acts as a load.
7. Draw the CMOS NAND circuit and discuss its operation.
8. Draw the three biasing circuits of the MOSFET and discuss their respective operations. Calculate the location of the *Q*-point under these biasing arrangements.
9. In which portion of the drain characteristics is the *Q*-point of an FET amplifier usually selected?
10. Draw the drain-to-gate bias circuit diagram of an enhancement-type MOSFET and show how the gate-source junction is forward-biased.
11. Deduce the relationship: μ = gain= $r_d g_m$
12. Why does the FET give better low-frequency amplification than the BJT?
13. Discuss the small-signal operation of a common-source *n*-channel JFET.

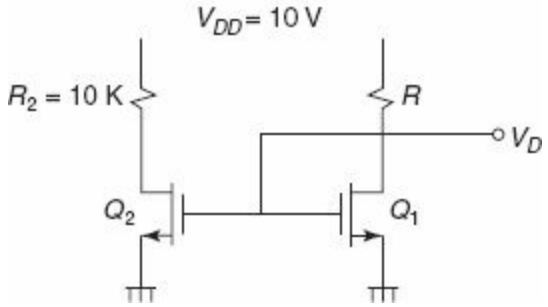
14. Derive an expression for the small-signal voltage gain of a common-source FET amplifier.
15. Define the importance of unity-gain frequency and also derive its expression.
16. Draw a comparison between the BJT and the FET with respect to their operations.
17. Compare the gate terminal and the bulk region as control electrodes.
18. How can the bulk region act as a gate?
19. Does it make sense to talk about the current-gain of a MOSFET? Why?
20. What is f_T for a small-signal MOSFET amplifier?
21. What are the dominant parasitic elements in determining f_T?

PRACTICE PROBLEMS

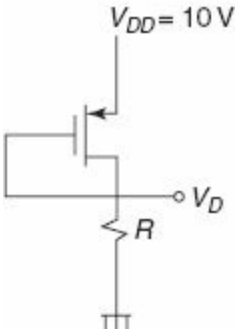
1. For the circuit, as shown in the diagram, find the values of R_D and R_S for establishing a drain current of 1mA and drain voltage. Given that:
   $V_T = 2$ V, $\mu_n C_{OX} = 20\ \mu$A/V^2, $L = 10\ \mu$m and $W = 400\ \mu$m.



2. A small-signal CS FET amplifier has a load resistance R_L. For what value of load resistance is the ac power dissipation maximum? (HINTS: r_d)
3. Consider the circuit given in the diagram. Given that:
   $V_T = 2$ V, $\mu_n\ C_{ox} = 20\ \mu$A/V^2,
   $L_1 = L_2 = 10\ \mu$m $W_1 = 100\ \mu$m and $\lambda = 0$.

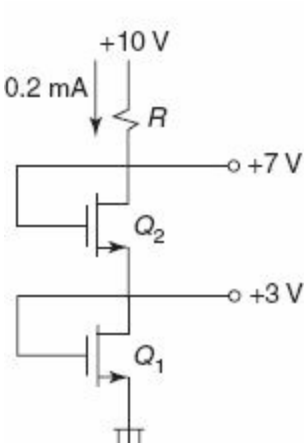


   With this data find the value of R required to establish a current of 0.1 mA in Q_1. Also find W_2 for Q_2 operating in the saturation region with a current of 0.5 mA.
4. The PMOS circuit, as shown in the diagram, has:
   $V_t = -2$ V, $\mu_p C_{0X} = 8\ \mu$A/V^2, $L = 10\ \mu$m
   and $\lambda = 0$.
   Find the values required for W and R to establish a drain current of 0.1 mA and voltage V_D of 7 V.

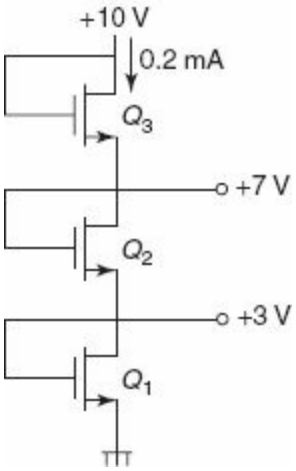


5. The NMOS circuit, as shown in the diagram, has the following specifications:

   $V_t = 2$ V, $\mu_n C_{ox} = 20\ \mu$A/V^2, $L_1 = L_2 = 10\ \mu$m
   and $\lambda = 0$.
   Find the values of the gate width for transistors, Q_1 and Q_2. Also find the value of R required to obtain the voltage and current values as indicated.

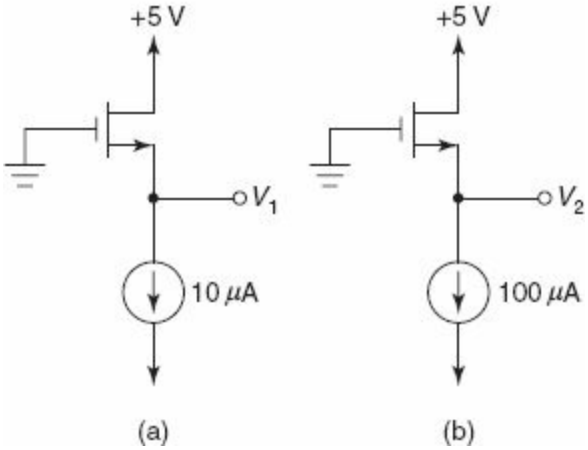


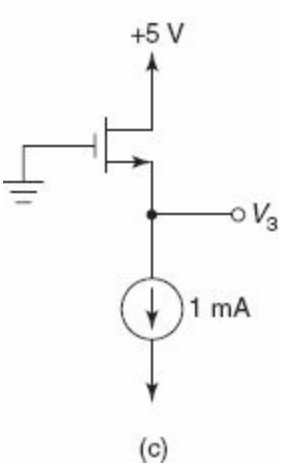
6. The NMOS transistors, as shown in the diagram, have the following specifications:
   $V_t = 2$ V, $\mu_n C_{0X} = 20\ \mu$A/V^2 and
   $L_1 = L_2 = L_3 = 10\ \mu$m.
   Find the required values of gate width for the three transistors required to obtain the voltages and current as indicated.



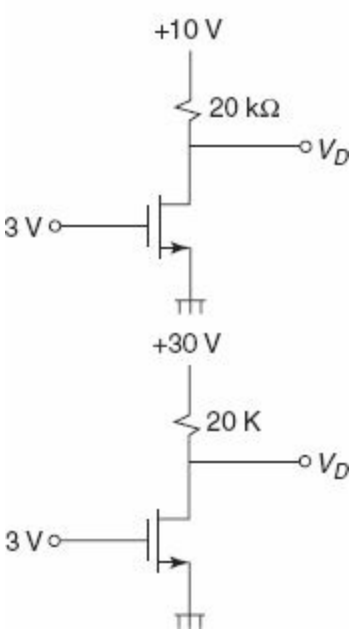
7. For the circuits, as labeled in the diagram, find the node voltages. For all the transistors:

$k_n' \frac{W}{L} = 0.5$ mA/V^2, and $V_T = 2$ V.

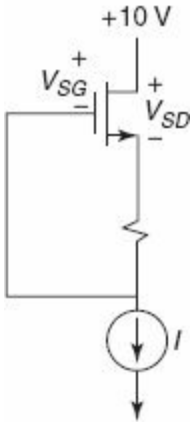




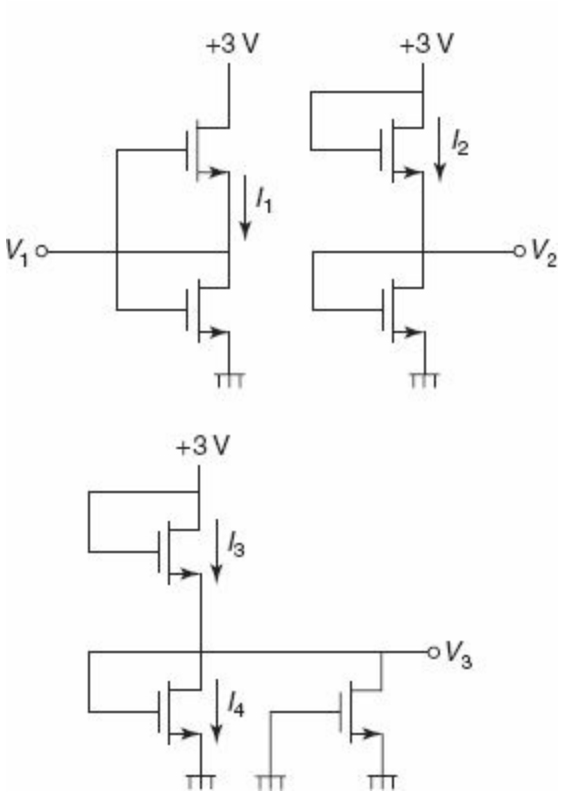
8. For the circuits shown, as in the diagram, find the drain voltages assuming that k_n' (W/L) = 200 μA/V^2. V_t = 2 V and V_A = 20 V.



9. For the PMOS transistor, as shown in the circuit, k_p' = 8 μA/V^2, W/L = 25 and $|V_{tp}|$ = 1 V. With I = 100μA, find the voltages V_{SD} and V_{SG} for R = 0,10 kΩ, 30 kΩ and 100 kΩ. And, for what value of R is $V_{SD} = V_{SG}$?



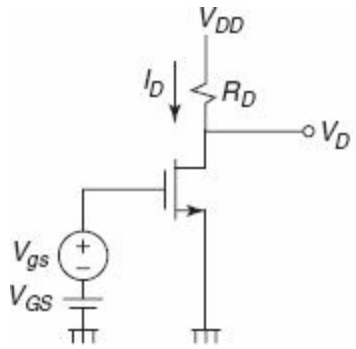
10. For the circuits, as shown in the diagram, $\mu_n C_{ox} = 2.5\ \mu\text{p}C_{ox} = 20\ \mu\text{A/V}^2$, $|V_t| = 1$ V, $\lambda = 0$, $\gamma = 0$, $L = 10\ \mu$m and $W = 30\ \mu$m. Find the labeled values of currents and voltages.



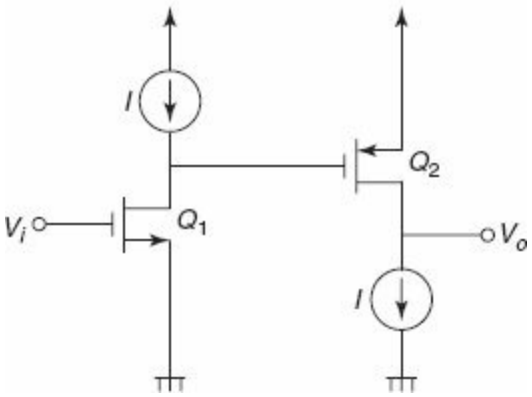
11. An NMOS amplifier is to be designed so as to provide a 0.50 V peak output signal across a 50 kΩ resistor that can be used as a drain resistor. For a gain of at least 5, what value of g_m is required?
12. In Problem 11, using the transistor with a dc supply of 3 V and $V_t = 0.9$ V, what values of I_D and V_{GS} would you choose? What value of W/L is required for $\mu_n C_{ox} = 100\ \mu\text{A/V}^2$?
13. Consider an NMOS transistor having $V_t = 2$ V, $k_n'(W/L) = 1$ mA/V^2. Let the transistor be biased with voltage $V_{GS} = 4$ V. What is the dc bias current for operation in saturation?
14. If a +0.1 V signal is superimposed on V_{GS}, find the corresponding increment in collector current by evaluating the total collector current i_D and subtracting the dc bias I_D.
15. Consider the given diagram under the following conditions:

    $V_t = 2$ V, k_p' $(W/L) = 1$ mA/V^2, $V_{GS} = 4$ V,

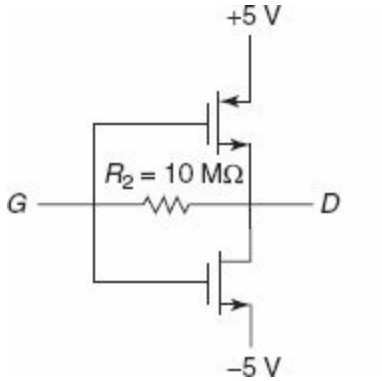
    $V_{DD} = 10$ V and $R_D = 3.6$ kΩ.
    Find the dc quantities, I_D and V_D.



16. From Problem 15 find the transconductance at the dc bias point. If the MOSFET has $\lambda = 0.01\text{V}^{-1}$, find r_o at the bias point and then calculate the gain.
17. Consider two identical transistors in current mirror circuits with the following specifications: $k_p' W/L = 40\ \mu\text{A/V}^2$, $V_t = 0.8$ V and $V_A = 20$ V. Let $I_{REF} = 10\ \mu$A. What is the output voltage at which I_o is exactly equal to I_{REF}? What will be the change in output current corresponding to a + 2 V increase in the output current?
18. The given diagram shows a circuit formed by cascading two common source stages. Assuming that the biasing current sources have very high output resistance, find the overall gain of $Q1$ and Q_2 in terms of g_m and r_o.



19. The MOSFETs, as shown in the diagram, are matched with the following data: $k_p'\ (W/L)_1 = k_p'(W/L)_2 = 50\ \mu\text{A/V}^2$ and $|V_t| = 2$ V. The resistance of R_2 is 10 MΩ. For G and D open, what are the drain currents of the two transistors?

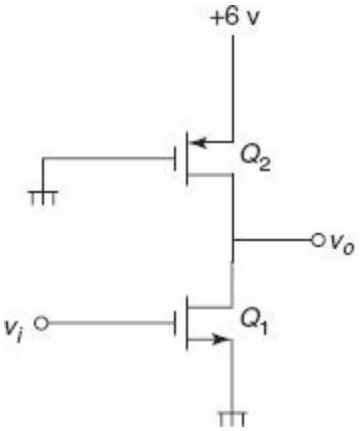


20. From Problem 19, for $r_o = \infty$, find the voltage gain of the amplifier from G to D? For finite r_o ($r_0 = |V_A|/I_D$, $|V_A| = 180$), what is the voltage gain from G to D and the input resistance at G?
21. For the circuit in the given figure, let $|V_t| = 2$ V. For each of the following cases:

    a. $k_p'(W/L)_2 = k_p'(W/L)_1$

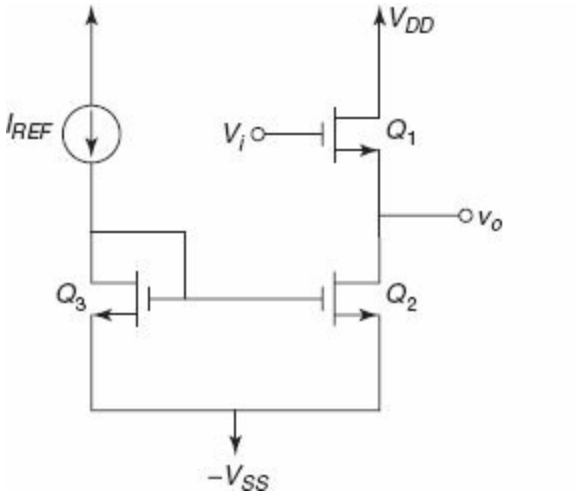
b. $k_p'(W/L)_2 = 0.1k_p'(W/L)_1$

find v_0 for different value of v_i 0 V, 3 V and 9 V.



22. A JFET with $V_P = -1$V and $I_{DSS} = 1$ mA shows an output resistance of 100 kΩ when operated in pinch-off with $v_{gs} = 0$ V. What is the value of output resistance when the device is operated in pinch-off with $v_{gs} = -0.5$ V?

23. Consider the source follower circuit, as shown in the diagram, when fabricated in the technology with $k_p' = 20\ \mu$A/V^2, $V_t = 1$ V and $V_A = 100$ V. Let $W/L = 10$ for all transistors, $I_{REF} = 300\ \mu$A and $\chi = 0.1$. Find g_{m1}, r_{01}, r_{02} and A_v.



24. Calculate the ac transconductance and drain resistance of an FET from the following data.

V_{GS}	V_{DS}	I_D
0 V	5.9 V	11 mA
0 V	13.9 V	10 mA
0.3 V	14 V	9.9 mA

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