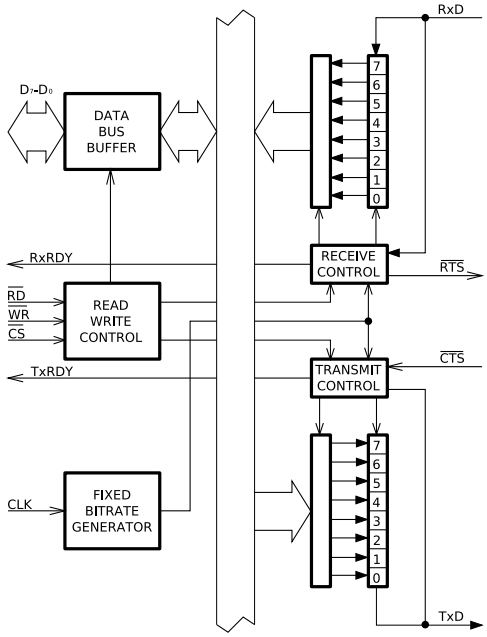
FBART - Fixed Bitrate Asynchronous Receiver Transmitter

Features

- Asynchronous operation
- Fixed bitrate, derived from system clock
- Fixed protocol, 8 bits, no parity, 1 stop bit
- Full duplex, 1 byte buffer for transmitter and receiver respectively



Functional description

General

The FBART is a fixed bitrate asynchronous receiver transmitter. System clock must be 16 times that of desired bitrate. The transmitter and receiver parts are independent making a full duplex operation possible. Both transmitter and receiver have a one byte buffer each reducing the need for flow control, making it possible to read/write previous/next data during reception/transmission of ongoing data.

Data bus buffer

The 3-state, bidirectional, 8-bit buffer is used to interface the FBART to a system bus. Direction of the data bus is determined by the assertion of either the rd or wr signal combined with an active setting of the cs signal.

Reset(reset)

A low on this input holds the FBART in an idle mode and resets internal states and buffers. The reset input is asynchronous.

CLK(clock)

The CLK input is used to generate internal device timing and determines the bitrate of both transmission and reception. The clock must be 16 times that of desired bitrate.

WR(write)

A low on this input will open the data bus for writing a data byte to the internal transmit data register. Data is written on the low to high transition of the WR signal. Prior to asserting the WR signal care should be taken to observe the state of the TxRDY signal, indicating whether the transmitter is ready for writing more data or not. If new data is written to the transmitter when TxRDY indicates a not ready state, previously written data may be lost.

RD(read)

A low on this input will open the databus for reading a data byte from the internal receiver data register. Prior to reading, it is useful to check status

of the RxRDY signal indicating whether new data is available.

CS(chip select)

A low on this input will select the device. In practice this means that the WR and RD signals will operate normally. A high on this input will deselect the device and the WR and RD signals will have no effect. All other signals and internal operations are unaffected from the CS signal.

Flow control

RTS(request to send)

The RTS output signal is an active low request to the sender that the FBART device is ready to recieve more data by the RxD input. It is not neccessary to use this signal if operation of the FBART device ensures that prior data in the receive data register is read before new data arrives.

CTS(clear to send)

The CTS input signal is an active low signal from the receiver indicating that it is "clear to send" and that the receiver is ready to receive more data by the TxD output. If it can be determined that the receiver always will be ready to receive data, the CTS input can be grounded, hence always signalling a clear to send.

Handshaking

TxRDY(transmitter ready)

This output will indicate with an active "high" signal that the transmitter part of the FBART device is ready to have more data written to its transmit data register.

RxRDY(receiver ready)

This output will indicate with an active "high" signal that the receiver part of the FBART device has new data in its receive data register ready to be read. If this data is not read and both the receiver data register and the receiver shift register are full, the receiver part will hold its operation, signalling via RTS that it is not ready for more data, until the receiver data register is read.

Data transfer

Data write sequence

A typical write sequence can be seen in figure 1. At some point TxRDY will go high indicating the transmitter is ready to accept more data. During assertion of WR, CS must be low. Data is written on the low to high transition of WR so at this point data must be stable and simulaneously TxRDY will go low indicating that the transmit data register is full. Once data has been moved internally to the transmit shift register this is indicated by TxRDY going high and the transmitter is ready to accept more data. If TxRDY remains low, the previous data byte in the transmit shift register has not yet been completely transmitted.

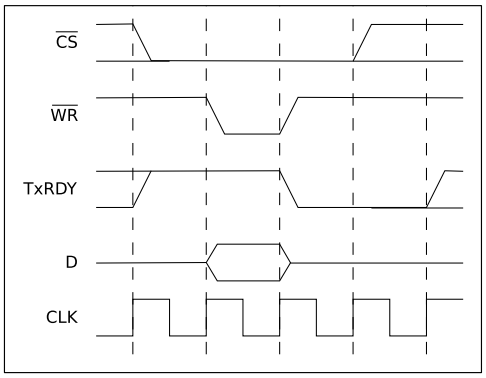


Figure 1: Write sequence

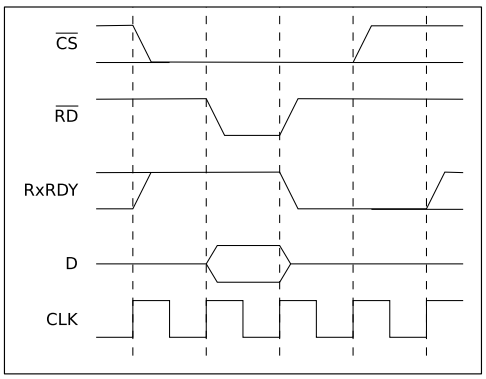


Figure 2: Read sequence

Data read sequence

A typical read sequence can be seen in figure 2. At some point RxRDY will go high indicating new data is available for reading. During assertion of RD, CS must be low. Typically data is read on the low to high transition of RD, which also 3-states the data bus. As a response of the low to high transition of RD, RxRDY will go low indicating that data has been read.

TxD(transmit data)

This output will send transmit data from the transmit shift register and internally generate start bit, data bits and stop bit in that order.

RxD(receive data)

This input will receive data to the receive shift register and internally recognize start bit, data bits and stop bit in that order.