CS440

ARM11

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Contents

0.1 In the beginning there was Acorn

In 1985 the first ARM processor, the Acorn RISC Machine was introduced to the world (Levy and Promotions, 2005). Later in 1990 the Advanced RISC Machines Ltd.(ARM) would be launched. Unlike other RISC processor vendors of their time ARM began creating small scale processors. A whitepaper (Kamath and Kaundin, 2001) from 2001 Strategy made this statement:

> At Wipro, significant focus has been on the ARM processor technology, since we believe that will drive the evolving market for embedded applications, mobile devices and next generation information appliances.

Although this insight was probably not difficult to gauge by 2001, the scale at which embedded mobile devices has exploded onto the market has been impressive. Larger corporations, which have not been know for ingenuity, such as Microsoft, have been dealt a massive blow by new mobile devices such as Apples IOS based iPhone and iPad, or the fleets of Android based devices. The need for a smaller architecture has never been greater and ARM is sitting center stage.

0.1.1 The need for a smaller silicon area

The ARM architecture a **Reduced Instruction Set Computer** or RISC based architecture is now considered a dominant choice for developers and manufacturers. The ARM architecture incorporates standard RISC fea-

tures (*ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition* 2011, A1-2):

- a large uniform register file.
- a load/store architecture, where data-processing operations only operate on register contents, not directly on memory contents.
- simple addressing modes, with all load/store addresses being determined from register contents and instruction fields only.

The ARM architecture has proven to be a better choice for smaller devices due to the low power consumption along with good performance. The **RM Architecture Reference Manual** listed the following additional reasons ARM is designed for smaller devices (*ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition* 2011, A1-2):

- instructions that combine a shift with an arithmetic or logical operation.
- auto-increment and auto-decrement addressing modes to optimize program loops.
- Load and Store Multiple instructions to maximize data throughput.
- conditional execution of almost all instructions to maximize execution throughput.

0.2 The Instruction Set Architecture

Currently ARMv6 has ISA support for the following (*Specifications* 2013):

- ARM
- Thumb®

- Jazelle DBX®
- DSP extension
- Floating Point Unit

0.2.1 state switching

The ARM processor allows switching of states using the BX and BLX instructions. The ARM state is 32-bit word-aligned, the Thumb a 16-bit halfword-aligned, and the Jazelle state is variable length, byte aligned for instructions (*ddi0301h* 2009, pp. 2-12).

0.2.2 A32

ARM is also known as A32 (*A32(ARM)* 2013). ARMv6 architecture is amongst a few others which use A32 such as ARMv5TEJ and ARMv4T.

Instruction length and format

ARM instructions are 32-bits wide and have a 4-byte boundary (*A32(ARM)* 2013). The subdivisions of the ARM instruction set can be seen in the below figure 1 (*ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition* 2011, A5-2). As you can see each ARM instruction is composed of a 32-bit word. The 32-bit word's subdivisions are determined by bits [31:25,4]. Additionally, the conditional subdivision can be see between bits [31:28]. The conditional field allows for more optimizations.

31 30 29 28	27 26 25	24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5	4	3 2 1 0
cond	op1		op	

Figure 1: ARM subdivisions

General Instruction Categories

The following figure 2, shown below, illustrates the encoding which defines the various classes of instructions used with ARMv6 (*ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition* 2011, A5-2):

cond	op1	op	Instruction classes
not 1111	00x	-	Data-processing and misc instructions
not 1111	010	-	Load/Store word and unsigned byte
not 1111	011	0	Load/Store word and unsigned byte
not 1111	011	1	Media instructions
not 1111	10x	-	Branch, branch with link, and block data transfer
not 1111	11x	-	Supervisor Call and coprocessor instructions
1111	-	-	Unconditionally executed

Figure 2: ARM Instruction encoding

The Branch Instruction

As can be seen in figure 2 op1 determines the instruction class. For example when op1 = 10x one of the various branching or block data transfer instructions is being used. If branch is the instruction specifically being used then 10xxxx will be found between [25:20] as shown in figure 3 be-

low (*ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition* 2011, A5-27):

31 30 29 28	27 26	25 24 23 22 21 20	19 18 17 16	15	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
cond	1 0	op			
not 1111	1 0	10xxxx			

Figure 3: Branch equals 10xxxx

Going a step further, the following figure 4 shows the branch instructions details in Encoding A1 (*ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition* 2011, A8-44).

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
cond	1 0 1 0	imm24

Figure 4: imm32 = SignExtend(imm24:'00', 32);

Encoding A1 indicates multiples of 4 in the range −33554432 to 33554428. Other encodings such as T1, T2, T3, and T4 have smaller ranges with T1 being the smallest of the permitted offsets. The T1 range is −256 to 254. All other offset ranges besides Encoding A1 are in even numbers, while Encoding A1, shown in figure 4, is in Multiples of 4. ARM encodings are labeled as A1, A2, A3 and so forth, while Thumb encodings are listed as T1, T2, T3 and so forth. Additionally, there are also encodings for ThumbEE

which are listed as E1, E2, E3 and so forth (*ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition* 2011, A8-282).

The MOV Instruction

Looking back at figure 2 to op1 = 00x you can see the 27th and 26th bit is determined to be both 0 for all instructions defined as data processing and misc.

31 30 29 28	27 26	25	24 23 22 21 20	19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
cond	0 0	op	op1		op2	

Figure 5: Data-processing and misc

One instruction which falls under the category of data processing is the MOV instruction. The following figure demonstrates the use of the MOV instruction in encoding A1 (*ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition* 2011, A8-194).

31 30 29 28	27 26	25	24 23 22 21	20	19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
cond	0 0	1	1 1 0 1	S	(0)(0)(0)(0)	Rd	imm12

Figure 6: MOV instruction

0.2.3 Syntax for using the branch and mov instructions

The aforementioned instructions mov and branch are used in the following manor:

```
/*an assembly code example using instruction mov*/
.global main
.func main

main:
     mov r0, #11 /* Put the number eleven in register r0*/
     bx lr
```

The below code clip shows a unconditional branch being used:

```
/*an assembly code example using the unconditional branch
    instruction*/
.text
.global main
main:
      mov r0, #11
      b finish/*branch to finish*/
      mov r0, #22
finish:
      bx lr
```

When the above code is run the second mov instruction will be skipped due to the branch instruction pointing to *finish*.

0.3 The main components of the ARM1176JZF-S

The following components are considered the main components for the ARM1176JZF-S processor (*ddi0301h* 2009, pp. 1-8):

0.3.1 List of components

Integer Core The ARM1176JZF-S processor is built around the ARM11 integer core. Therefore, it is a implementation of the ARMv6 architecture. This architecture handles the following critical items (*ddi0301h* 2009, pp. 1-9):

- Instruction sets
- Conditional execution
- Registers
- Modes and exceptions
- Thumb instruction set
- DSP instructions
- Media extensions
- Datapath
- Branch prediction
- Return Stack

Load Store Unit (LSU) The load-store pipeline decouples loads and stores from the MAC and ALU (*ddi0301h* 2009, pp. 1-11).

Prefetch unit Fetches instructions from the instruction cache, external memory and instruction TCM to predict branch outcomes (*ddi0301h* 2009, pp. 1-11).

Memory system The memory system provides the core with features such as virtual indexing, export of memory, memory access control and many other capabilities (*ddi0301h* 2009, pp. 1-12).

AMBA AXI interface This bus interface allows high bandwidth connectivity between the processor, second level caches, on-chip RAM, peripherals, and interfaces to external memory (*ddi0301h* 2009, pp. 1-16).

Coprocessor interface This is a external coprocessor which interfaces with the ARM1176JZF-S to handle ARM coprocessor instructions (*ddi0301h* 2009, pp. 1-17).

Debug Using the ARMv6 debug architecture the following levels of debugging are allowed (*ddi0301h* 2009, pp. 1-18):

- debug everywhere
- debug in non-secure privileged user, and secure user.
- debug in non-secure.

Instruction cycle summary and interlocks Allows handling of cycle timing behavior.

Vector Floating-Point (VFP) Handles floating point arithmetic operations (*ddi0301h* 2009, pp. 1-19).

System control Controls the memory system and other functionality (*ddi0301h* 2009, pp. 1-21).

Interrupt handling The interrupt handling deal with the following areas (*ddi0301h* 2009, pp. 1-21):

- Vectors Interrupt Controller port
- Low interrupt latency configuration
- Configuration
- Exception processing enhancements

0.4 ARM1176JZF-S pipeline stages

The ARM1176JZF-S processor overlaps operations to improve clock rate speed for each instruction. For the following figures 7-12 note that the first 4 stages Fe1, Fe2, De, Iss are considered the **common decode pipeline**. From the common decode pipeline the direction taken will determine if the instruction will seek a ALU pipeline, Multiply pipeline, or a Load/Store pipeline.

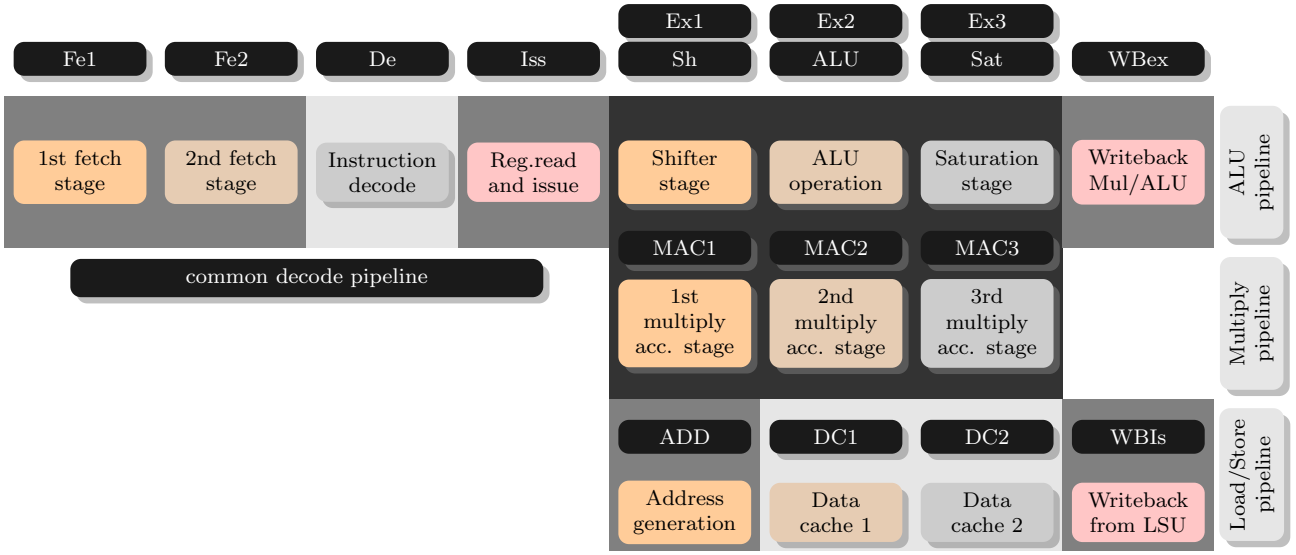

Figure 7: ARM1176JZF-S pipeline stages

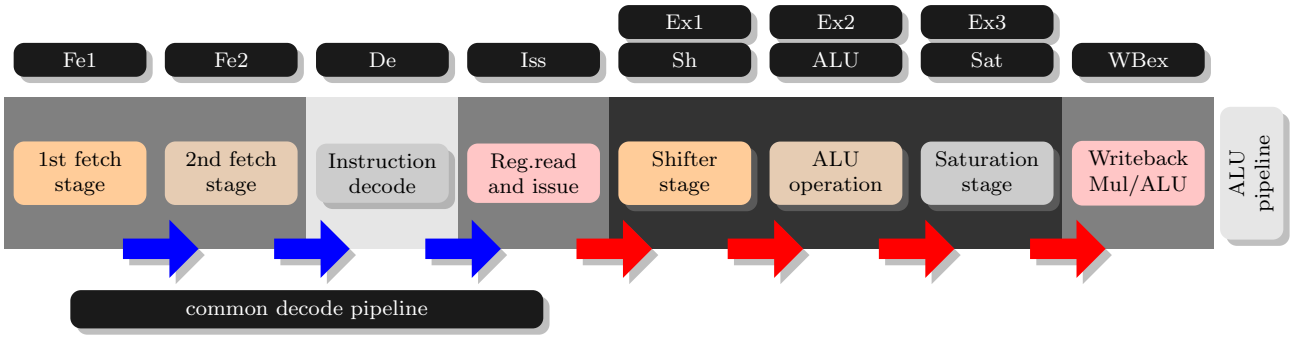

Figure 8: ARM1176JZF-S ALU Operation

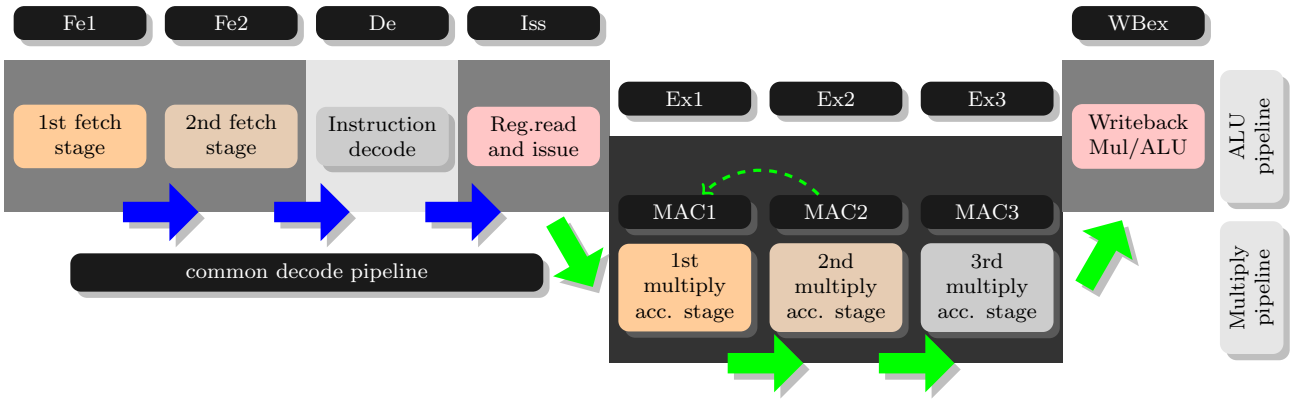

Figure 9: ARM1176JZF-S Multiply Operation

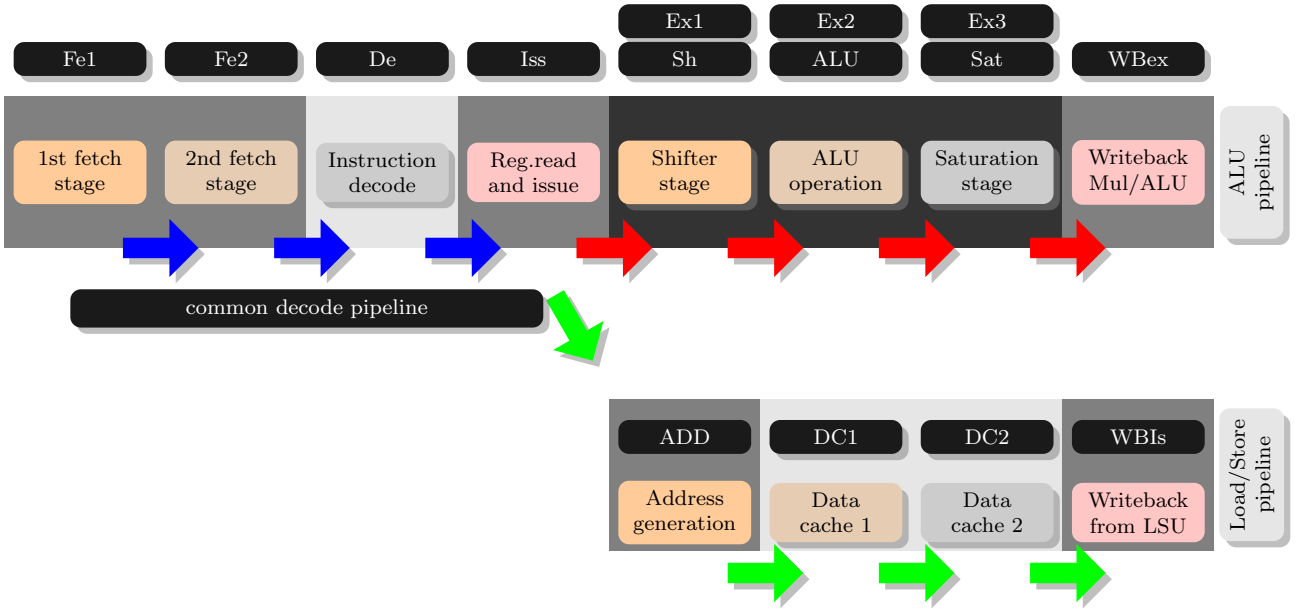

Figure 10: ARM1176JZF-S LDR/STR operation

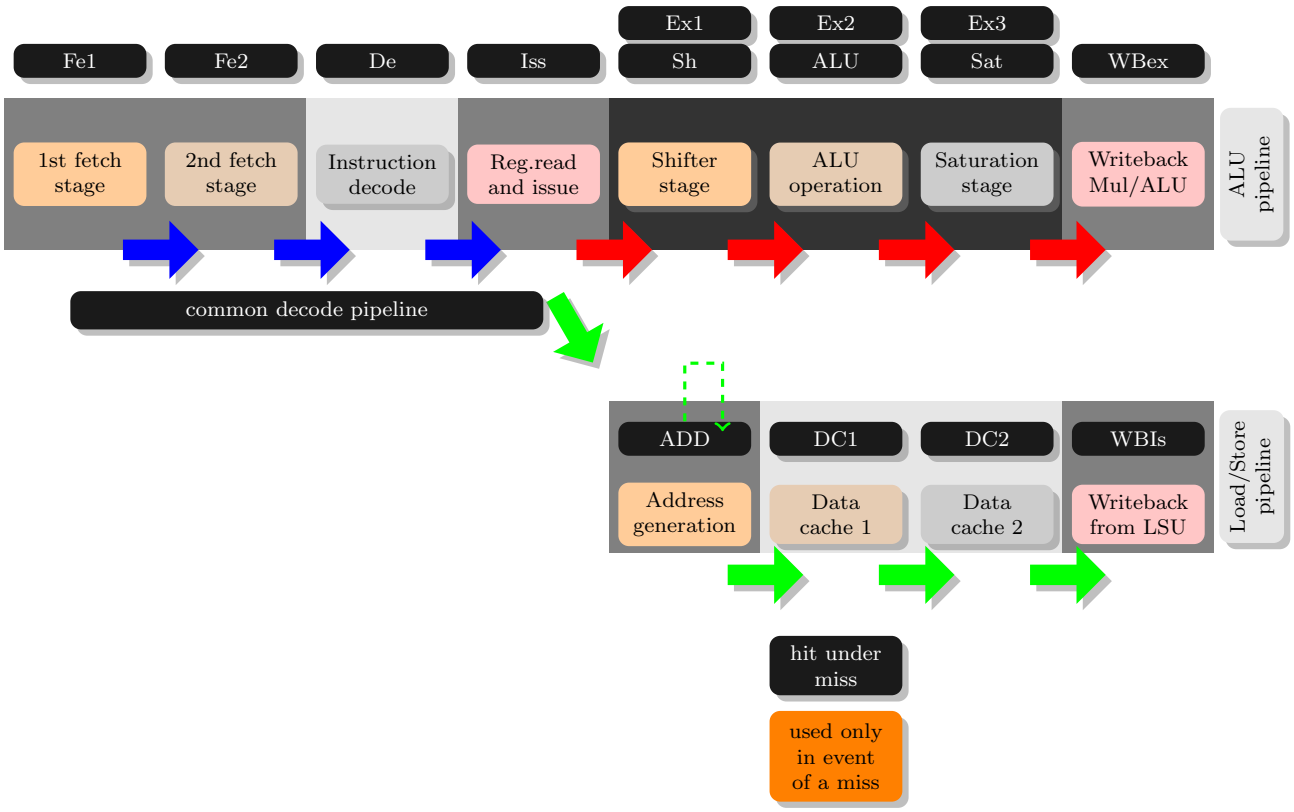

Figure 11: ARM1176JZF-S LDM/STM operation

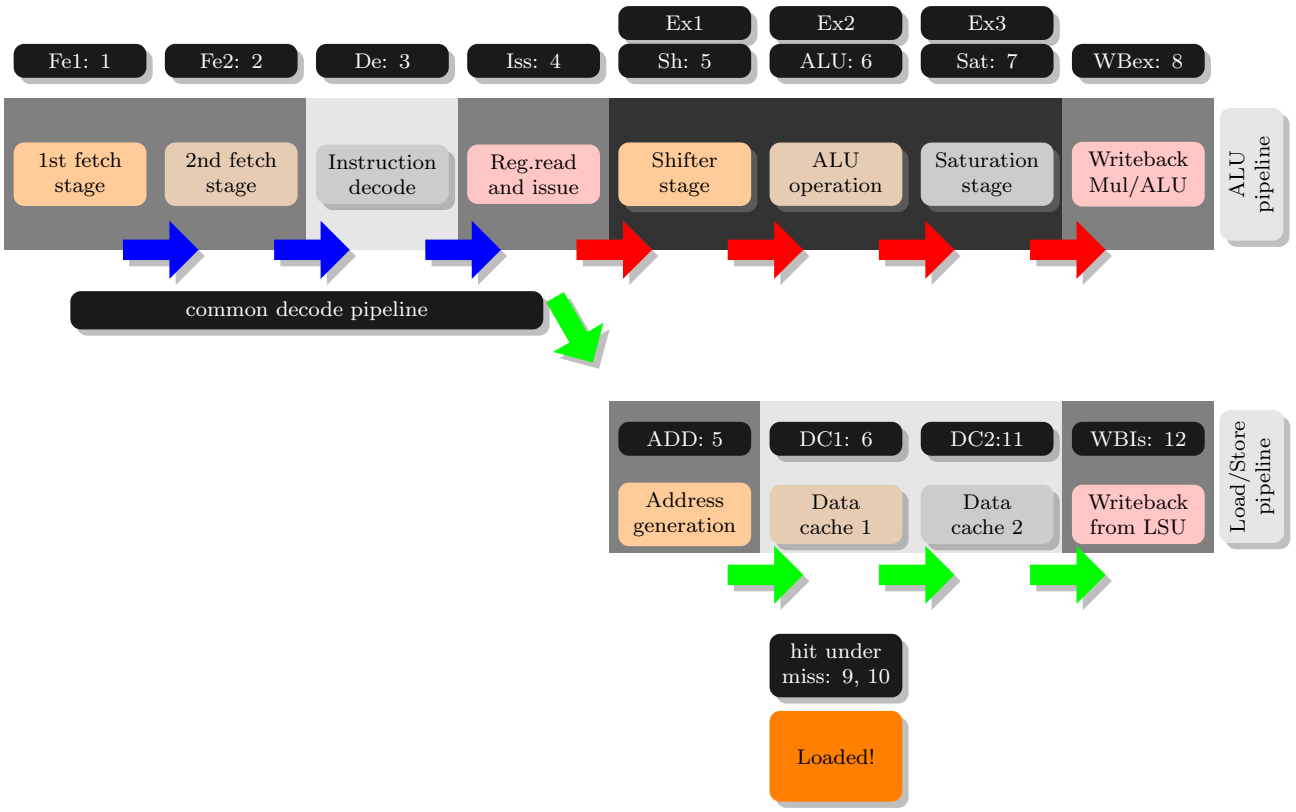

Figure 12: ARM1176JZF-S Example LDR miss

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