Single Cycle Datapath

Datapath Elements

Program counter (PC) an incrementing counter that keeps track of the memory address of the instruction that is to be executed next.

Memory address register (MAR) holds the address of a memory block to be read from or written to.

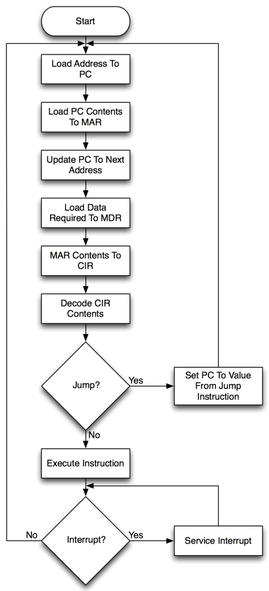
Memory data register (MDR) a two-way register that holds data fetched from memory (and ready for the CPU to process) or data waiting to be stored in memory

Instruction register (IR) a temporary holding ground for the instruction that has just been fetched from memory

Control unit (CU) decodes the program instruction in the IR, selecting machine resources such as a data source register and a particular arithmetic operation, and coordinates activation of those resources

Arithmetic logic unit (ALU) performs mathematical and logical operations

Fetch Execute Cycle



R-Type Instruction Classes

Field	0	rs	rt	rd	ShiftAmt	funct
Bit Positions	31:26	25:21	20:16	15:11	10:6	5:0

Some R-Type Math Instructions

instruction	opcode	function	func base 2
add	0	32	100000
sub	0	34	100010
and	0	36	100100
or	0	37	100101
slt	0	42	101010

R-Type Example

Opcode	rs	rt	rd	ShiftAmt	funct
add	$17	$18	$9	N/A	32
000000	10001	10010	01001	00000	100000
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

R-Type in datapath

I-Type instruction classes

opcode	rs	rt	memory address offset
lw	$17	$8	8
100011	10001	01000	0000 0000 0000 1000
sw	$20	$16	44
101011	10100	10000	0000 0000 0010 1100

ALU control lines

ALU control lines	Function
0000	AND
0001	OR
0010	add
0110	subtract
0111	set on less than
1100	NOR