CHAPTER 4

SPACE VECTOR PULSE WIDTH MODULATION

4.1 INTRODUCTION

Multilevel inverters generate sinusoidal voltages from discrete voltage levels, and pulse width modulation (PWM) strategies accomplish this task of generating sinusoids of variable voltage and frequency. Modulation methods for Hybrid Multilevel Inverter can be classified according to the switching frequency methods. Many different PWM methods have been developed to achieve the following: Wide linear modulation range, less switching loss, reduced Total Harmonic Distortion (THD) in the spectrum of switching waveform: and easy implementation and less computation time. The most widely used techniques for implementing the pulse with modulation (PWM) strategy for multilevel inverters are Sinusoidal PWM (SPWM) and space vector PWM (SPWM). The SVPWM is considered as a better technique of PWM implementation as it has advantages over SPWM in terms of good utilization of dc bus voltage, reduced switching frequency and low current ripple is presented in Beig et al (2007), Gupta and Khambadkone (2007), and Franquelo et al (2006).

SVPWM is considered a better technique of PWM implementation, as it provides the following advantages,

(i) Better fundamental output voltage.

(ii) Useful in improving harmonic performance and reducing THD.

(iii) Extreme simplicity and its easy and direct hardware implementation in a Digital Signal Processor (DSP).

(iv) SVPWM can be efficiently executed in a few microseconds, achieving similar results compared with other PWM methods.

In this chapter, a space vector is defined in a two-dimensional (2-D) plane and a SVM is performed in the 2-D plane. Furthermore, a three-dimensional (3-D) space vector has been defined in this chapter for cascaded H-bridge multilevel inverter. All the existing space vector modulation schemes are implemented in a two-dimensional, and are therefore unable to deal with the zero-sequence component caused by unbalanced load. Complexity and computational cost of traditional SVPWM technique increase with the number of levels of the inverter as most of the space vector modulation algorithms proposed in the literature involve trigonometric function calculations or look-up tables. Previous works on three-dimensional space vector modulation algorithms have been presented in Prats et al (2003) and Oscar Lopez et al (2008) for diode-clamped inverter. However, unequal dc sources cannot be applied to diode-clamped inverter. Meanwhile, the first 3-D space vector modulation for cascaded H-bridge inverter is presented in Karthikeyan and Chenthur Pandian (2011), which is capable of dealing with zero-sequence component caused by unbalanced load.

The three-dimensional space vector modulation schemes are supersets of, and thus are compatible with, conventional two-dimensional space vector modulation schemes. A new optimized 3-D SVPWM (3-D OSVPWM) technique was proposed by Karthikeyan and Chenthur Pandian (2011), which is similar to already existing 3-D SVPWM presented in, following a similar notation. The proposed SVPWM technique calculate the nearest switching vectors sequence to the reference vector and the on-state durations of the respective switching state vectors by means of simple

addition and comparison operation, without using trigonometric function calculations, look-up tables or coordinate system transformations. Such very low complexity and computational cost make them very suitable for implementation in low cost devices. It is important to notice that these 3-D OSVPWM techniques can be applied with balanced and unbalanced systems. Implementation of the 2-D SVPWM and 3-D OSVPWM techniques is carried out. Both SVPWM algorithms are implemented into a Field Programmable Gate Arrays (FPGA) from Xilinx Foundation. Matlab Simulink is used to develop all simulation works. Finally, both algorithmic implementations have been tested with a cascaded H-bridge multilevel inverter.

4.2 SVPWM FOR THREE-LEG VOLTAGE SOURCE INVERTER

The topology of a three-leg voltage source inverter is shown in Figure 4.1. Eight possible switching combinations are generated by the switching network shown in Figure 4.1 Six out of these eight topologies producing a nonzero output voltage are known as the non-zero switching states and the remaining two topologies producing zero output voltage are known as zero switching states.

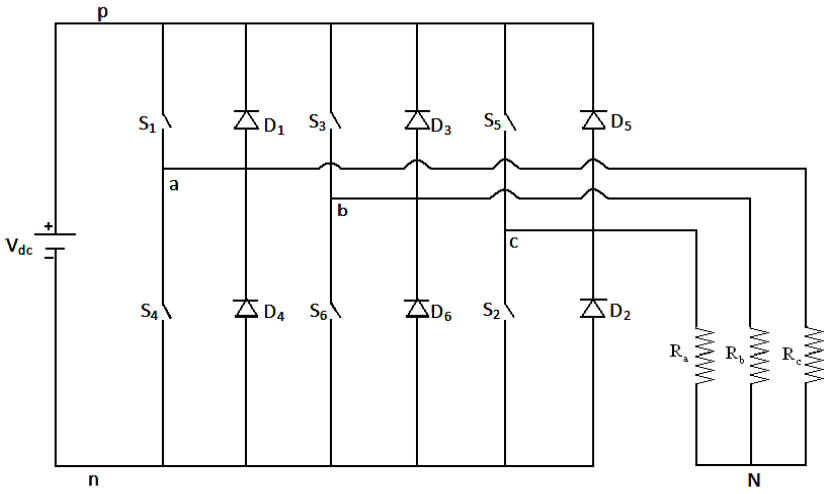

Figure 4.1 Three-Phase Voltage Source Inverter

4.2.1 Voltage Space Vectors

Space Vector Modulation (SVM) for three-leg VSI is based on the representation of the three phase quantities as vectors in a two-dimensional (α,β) plane. Considering topology 1 of Figure 4.2, which is repeated in Figure 4.3 a. The line voltages V_{ab}, V_{bc} and V_{ca} are given by

$$\begin{aligned} V_{ab} &= +V_{dc} \\ V_{bc} &= 0 \\ V_{ca} &= -V_{dc} \end{aligned} \tag{4.1}$$

This can be represented in the (α,β) plane as shown in Figure 4.3(b), where voltages V_{ab}, V_{bc} and V_{ca} are three line voltage vectors displaced 120^0 in space. The effective voltage vector generated by this topology is represented as V_1 (pnn) in Figure 4.3.b. The switching network shown in Figure 4.1 has a total of eight possible switching combinations.

Each switching combination is shown in Figure 4.2, and is represented according to the phase leg connection, where '*p*' denotes that phase leg is connected to the positive rail of the DC link, and '*n*' denotes that phase leg is connected to the negative rail of the DC link. For example, switching combination '*pnn*' represents the condition where the phase A output terminal V_a is connected to the positive DC rail, and phase B and C output terminals V_b and V_c are connected to the negative DC rail.

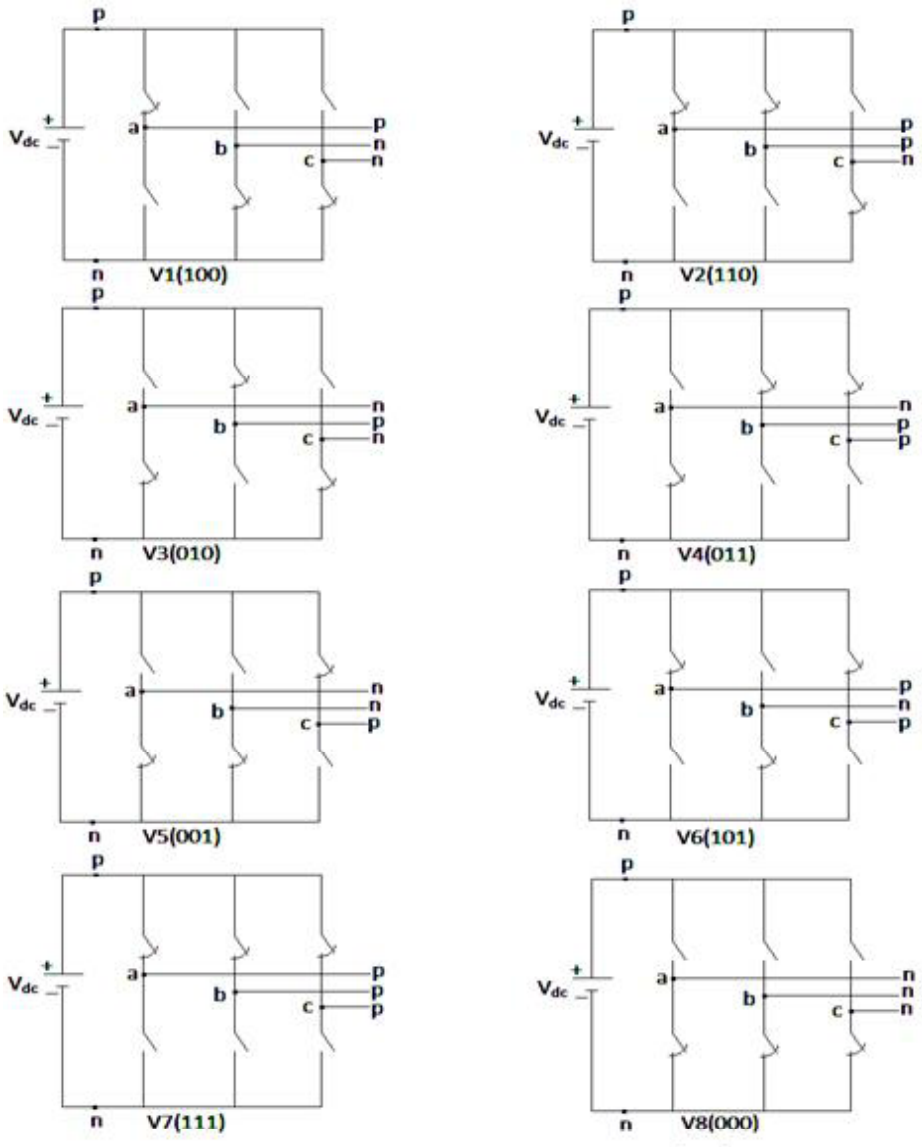

Figure 4.2 Eight Switching State Topologies of Three-Phase Inverter

Each switching combination results in a set of three phase voltages at the AC terminal of the switching network. A reference vector V_1 can be obtained by transforming the reference three-phase voltage into the $\alpha - \beta$ plane, as shown in Figure 4.3.b. A balanced three-phase sinusoidal waveform is obtained when the reference vector is rotating in the $\alpha - \beta$ plane.

Proceeding on similar lines the six non-zero voltage vectors $(V_1 - V_6)$ can be shown to assume the positions shown in Figure 4.4. The tips of these vectors form a regular hexagon (dotted line shown in Figure 4.4). The area enclosed by two adjacent vectors, within the hexagon, is chosen as a sector. Thus there are six sectors numbered 1 to 6 in Figure 4.4.

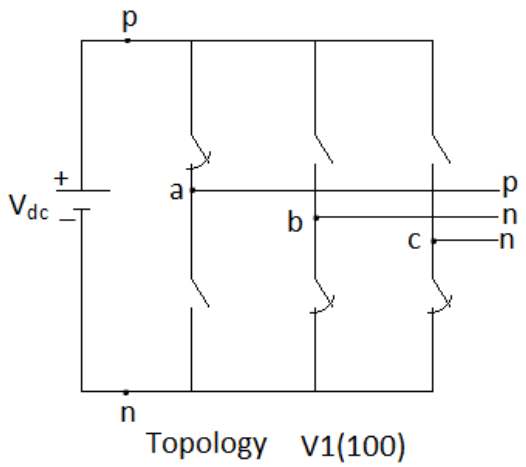

Figure 4.3.a. Topology V_1 (100) Voltage Source Inverter

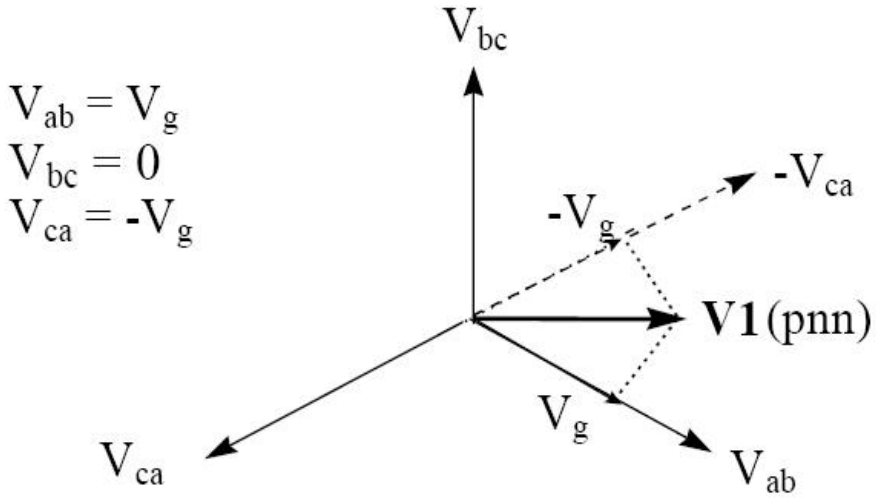

Figure 4.3.b. Topology Representation of α, β plane

The output line voltages generated by this topology in Figure 4.5.a are given by

$$\begin{aligned} V_{ab} &= 0 \\ V_{cb} &= 0 \\ V_{ca} &= 0 \end{aligned} \tag{4.2}$$

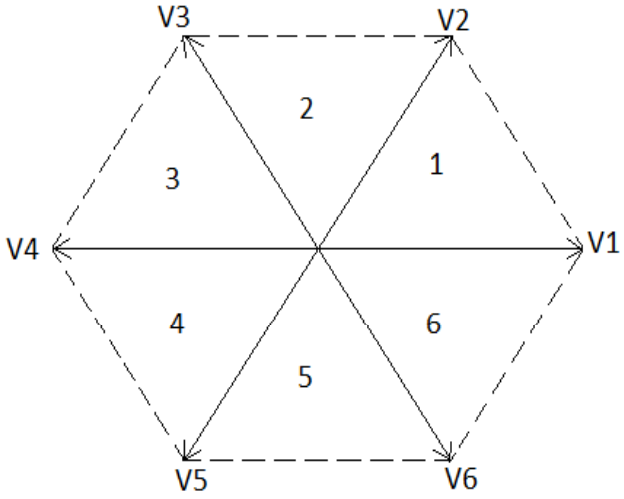

Figure 4.4 Non-Zero Voltage Vectors in the α, β Plane.

The output voltages are represented as vectors which have zero magnitude and hence are referred to as zero-switching state vectors or zero voltage vectors. The position at origin in the (α, β) plane is as shown in Figure 4.5.b. A total of eight vectors are obtained by transforming the three-phase voltages into the $a-b$ coordinate and the same are called switching state vectors.

4.2.2 Space Vector Modulation

The desired three phase voltages at the output of the inverter could be represented by an equivalent vector V rotating in the counter clock wise direction as shown in Figure 4.6.a. The magnitude of this vector is related to

the magnitude of the output voltage as shown in Figure 4.6.b and the time this vector takes to complete one revolution is the same as the fundamental time period of the output voltage.

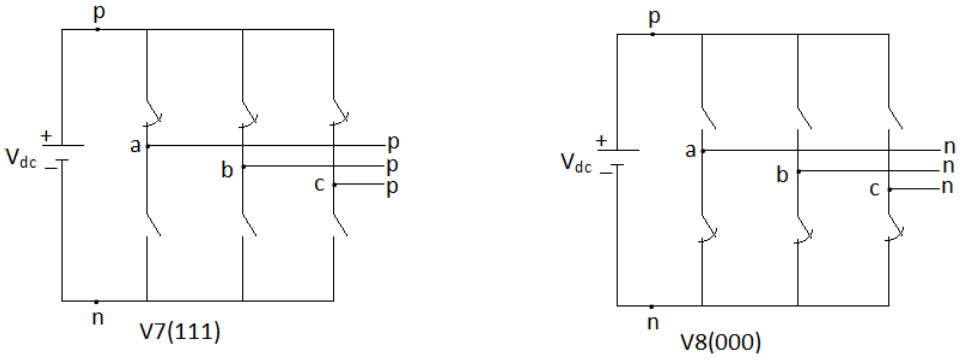

Figure 4.5.a. Zero Output Voltage Topologies

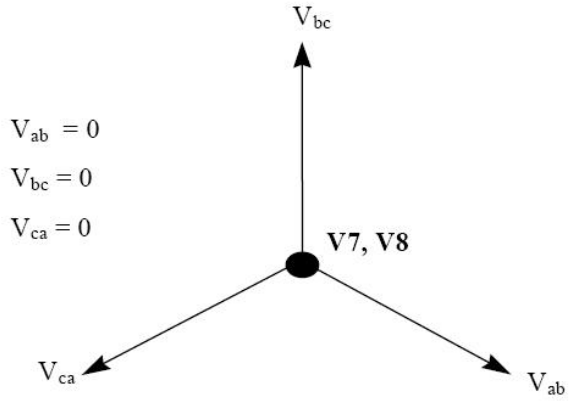

Figure 4.5.b Representation of the zero voltage vectors in the α, β plane

When the desired line-to-line output voltage vector V is in sector 1 as shown in Figure 4.7., vector V could be synthesized by the pulse-width modulation (PWM) of the two adjacent switching state vectors V_1(pnn) and V_2(ppn), the duty cycle of each being d_1 and d_2, respectively, and the zero vector (V_7 (nnn) / V_8 (ppp)) of duty cycle d_0:

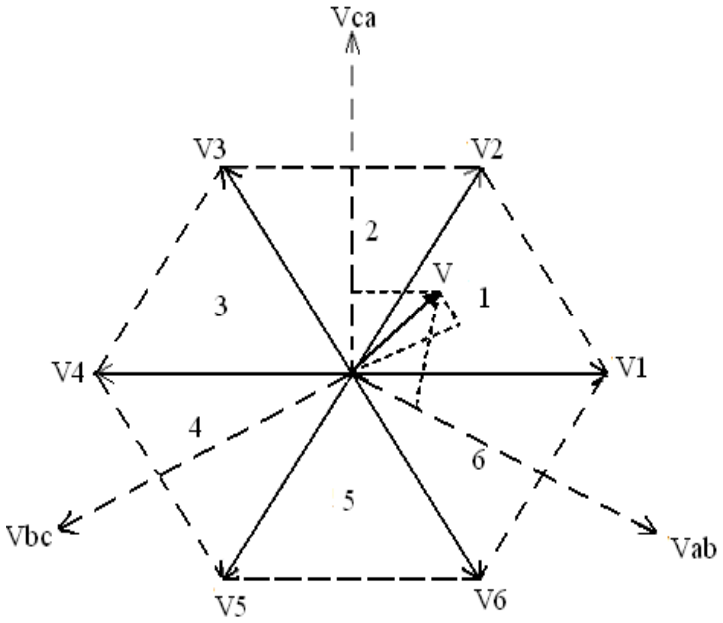

Figure 4.6.a Output voltage vector in the α, β plane

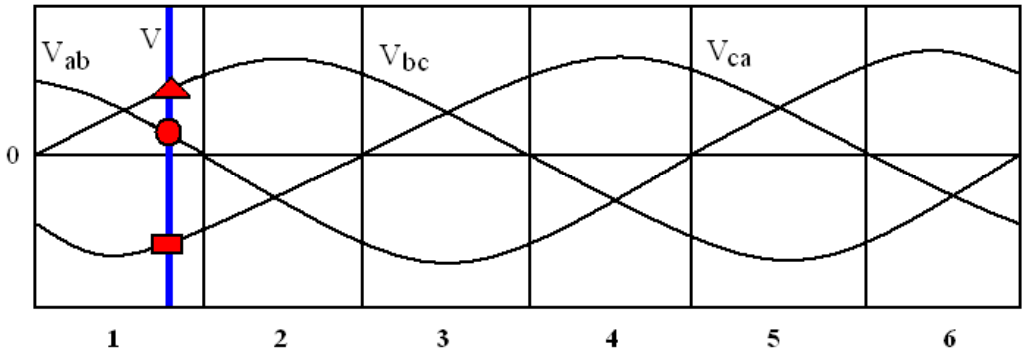

Figure 4.6.b Output Line Voltage

$$d_1\vec{V}_1 + d_2\vec{V}_2 = \vec{V} = mV_g e^{je} \tag{4.3}$$

$$d_1 + d_2 + d_0 = 1 \tag{4.4}$$

where, $0 \le m \le 0.850$ is the modulation index. This would correspond to a maximum line-to-line voltage of $1.0V_g$, which is 15% more than conventional sinusoidal PWM is presented in Van Der Broeck et al (1988).

All SVPWM schemes and most of the other PWM algorithms, use the Equations 4.3 and 4.4 for the output voltage synthesis. The modulation algorithms that use non-adjacent switching state vectors have been shown to produce higher THD and/or switching losses. But some of them, for e.g. hysteresis modulation, can be very simple to implement and can provide faster transient response. The duty cycles d_1, d_2 and d_0, are uniquely determined from Figure 4.7, and the equations of 4.3 and 4.4, the only difference between PWM schemes that use adjacent vectors is the choice of the zero vector(s) and the sequence in which the vectors are applied within the switching cycle.

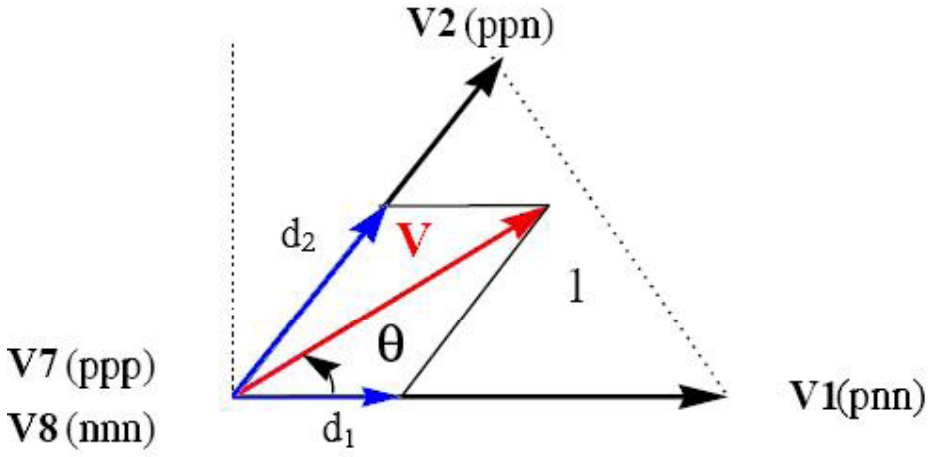

Figure 4.7 Synthesis of the Required Output Voltage Vector in Sector 1

4.3 SPACE VECTOR MODULATION ALGORITHMS

4.3.1 Two-Dimensional Space Vector

For any balanced three-phase variable, $V_a + V_b + V_c$, where $\vec{V}$ be the voltage vector, there is a relationship

$$V_a + V_b + V_c = 0 \tag{4.5}$$

The above equation suggests that the three variables could be mapped into a vector $\vec{V}$ on the orthogonal $\alpha - \beta$ plane, where

$$\vec{V} = \vec{V}_\alpha + j\vec{V}_\beta \tag{4.6}$$

The transformation for this orthogonal co-ordinate mapping, sometime called 3/2 transformation, is expressed as

$$\left[V_\alpha, V_\beta\right]^T = T_2\left[V_a \quad V_b \quad V_c\right]^T \tag{4.7}$$

where T is the transformation matrix and is expressed as

$$T = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{4.8}$$

4.3.2 Three-Dimensional Space Vector

For any balanced three-phase inverter, an assumption is always made that, $V_a + V_b + V_c = 0$, where $\vec{V}$ be the voltage vector. The three variables in *a-b-c* coordinate V_{abc} can be mapped into a vector $\vec{V}$ on the orthogonal $\alpha - \beta$ plane. Since each variable maintains the equal phase difference for each phase, zero–sequence current is automatically nullified as the reference vectors will be on a plane. When the system becomes unbalanced, there is no zero–sequence component or triple harmonics because the reference vectors are on a plane. So the three-dimensional space vector representation and mapping will be similar to that of 2-D one.

4.3.3 Two-Dimensional SVPWM for Calculating Switching Angles

A two-dimensional scheme for an *n*-level $(n \geq 3)$ cascaded multilevel inverter is proposed. In the proposed method, a simple algorithm of forming switching sequence is applied that leads to minimum change in voltage. An effective hybrid multilevel inverter must ensure that the Total Harmonic Distortion (THD) in the voltage output waveform is small enough. An algorithm is proposed for the cascaded multilevel inverter with equal voltage steps under the space vector modulation. The algorithm results in the minimal THD of output voltage of the cascaded multilevel inverter with equal voltage steps.

A new expression of THD is presented to simplify the derivation. The output voltage of the hybrid multilevel inverter is $(2S+1)$ with the SVPWM modulation. $E_{p1}, E_{P2}, E_{p3}...E_{pn}$ indicates the voltage steps in positive side and $E_{n1}, E_{n2}, E_{n3}...E_{nn}$ indicates the voltage steps in negative steps. $\theta_1, \theta_2, \theta_3...\theta_n$ are the switching angles that indicates the on and off instance of switches inside the inverter are presented in Liang and Nwankpa (1999), Sirisukprasert et al (2002) and Zhou and Wang (2002).

4.3.3.1 Mathematical formulation

The algorithm can be expressed from the basis waveform by applying Fourier series analysis, the amplitude of any odd n^{th} harmonic can be expressed as,

$$V_n = \frac{4}{n\pi} \sum_{k=1}^{n} \left[E_k \cos\left(n\theta_k\right) \right] \tag{4.9}$$

where n is an odd harmonic and θ_k is the k^{th} switching angle. The amplitude of all even harmonics is zero. The modulation index m is defined as,

$$m = \frac{\pi}{4} \frac{V_1}{\sum_{i=1}^{n} E_i} \tag{4.10}$$

V_n is the total harmonic component and V_1 is the fundamental harmonic component.

The voltage THD is defined as

$$THD = \sum_{n=3,5,7,\ldots}^{\infty} \sqrt{\frac{V_n^2}{V_1^2}} \tag{4.11}$$

Now, to find the problem and to implement an algorithm for the following variable inputs of the inverter $V_1, V_2, V_3 \ldots V_n$ Modulation index term m. Output of the algorithm $\theta_1, \theta_2, \theta_3 \ldots \theta_n$ such that THD is minimum. The input voltages $V_1, V_2, V_3 \ldots V_n$ are from dc sources.

The input m is determined by a controller in multilevel inverter. The pulse angles $\theta_1, \theta_2, \theta_3 \ldots \theta_n$ are used by the inverter to control the switches. It is important to note that minimizing voltage THD is desirable in some applications. In some high power applications one desires to limit each order harmonic to certain maximum allowed values. For the three phase system, the triple order harmonic can be cancelled without help of modulation techniques, yet it is desired to minimize THD for certain applications is presented in Beig et al (2004), Naik and Udaya (2005) and Khajehoddin et al (2007).

From modulation index m, determine the value of ρ by evaluating

$$m = \sum_{k=1}^{n} e_k \sqrt{1 - (\mu_k \rho)^2} \tag{4.12}$$

where,

$$e_k = \frac{E_k}{\sum_{i=1}^{n} E_l} \tag{4.13}$$

$$\mu_k = \frac{\sum_{i=1}^{nk} E_i - E_k / 2}{\sum_{i=1}^{n} E_i - E_n / 2} \tag{4.14}$$

The switching angles are determined by,

$$\theta_k = \sin\left(\mu_k \rho\right) \tag{4.15}$$

The output voltages of the inverter is,

$$V = \sum_{k=1}^{\infty} E_k \left(V_{\theta k} - V_{\pi-\theta k} + V_{\pi+\theta k} + V_{2\pi+\theta k}\right) \tag{4.16}$$

where V is unit function. By Fourier series expansion,

$$V = \sum_{n=1,3,5,\ldots} V_n \sin\left(n\theta\right)$$

where,

$$V_n = \frac{4}{n\pi} \sum_{n=1,3,5,..}^{\infty} E_1 \cos\left(n\theta_1\right) \tag{4.17}$$

Modulation index m for the basic output voltage

$$m = \frac{\pi}{4} V_1 = \frac{\pi}{4} \sum_{n=1}^{\infty} E_1 \cos\left(n\theta_1\right) \tag{4.18}$$

The THD is expressed as

$$\text{THD} = \sum_{n=3,5,7,\ldots}^{\infty} \sqrt{\frac{V_n^2}{V_1^2}} \tag{4.19}$$

4.3.3.2 General structure of the algorithm

The control processing unit calculates the basic parameters to apply a switching state. The input data to the control processing unit is the reference space vector. During various iterations, the unit determines the sector number, triangle number of the subhexagon. The sector number and triangle number identify the correct switching sequence. The flowchart is given for an *n*-level inverter and can be used for any *n*-levels without change.

The input supply is the amplitude of the voltage steps and modulation index *m*, the initial value of ρ_o. The flow diagram of the proposed algorithm to find minimum THD is shown in Figure 4.8. The modulation index m_c is calculated for various iterations. The difference between two modulation index terms is calculated.

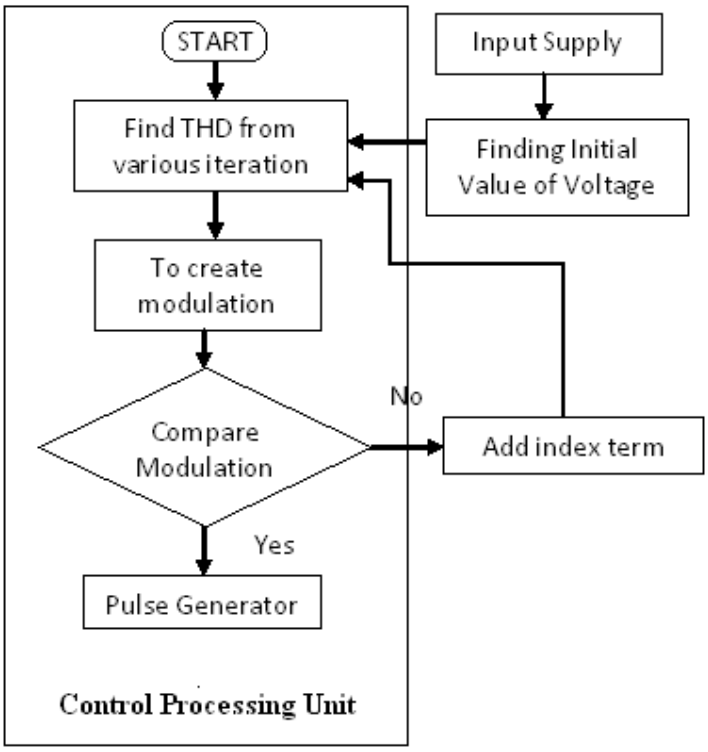

Figure 4.8 Flowchart of the Algorithm

$$\left|m - m_c\right| < \delta \tag{4.20}$$

where,

δ – Reference value increases (or) decreases the pulse generation in the pulse generator.

If the difference between the two modulation index terms is less than reference value δ, the proposed algorithm outputs the optimal switching angles. The iteration method is used to solve and find minimization of the voltage THD.

4.3.3.3 Principles of the 2-D SVPWM technique

The SVPWM technique can be easily extended to all multilevel inverters by Rodriguez et al (2002). This section explains the 2-D technique for the generation of SVPWM for a five-level inverter. By using the space-vector diagram, the basic principles of the SVPWM method can be easily explained. Figure 4.9 shows the space vector diagram of a five level inverter. The SVPWM implementation involves two phases: i) Selecting the switching vector, and ii) Determining the center of the subhexagon.

A. Selection of the Switching Vector

In the 2-D method, the small triangles formed by the adjacent voltage space vectors are called sectors. Such six sectors around a space vector forms a hexagon called subhexagon. The space vector modulation diagram of a multilevel inverter can be viewed composed of a number of subhexagons. Sector identification is done by determining the triangle that encloses the tip of the reference space vector.

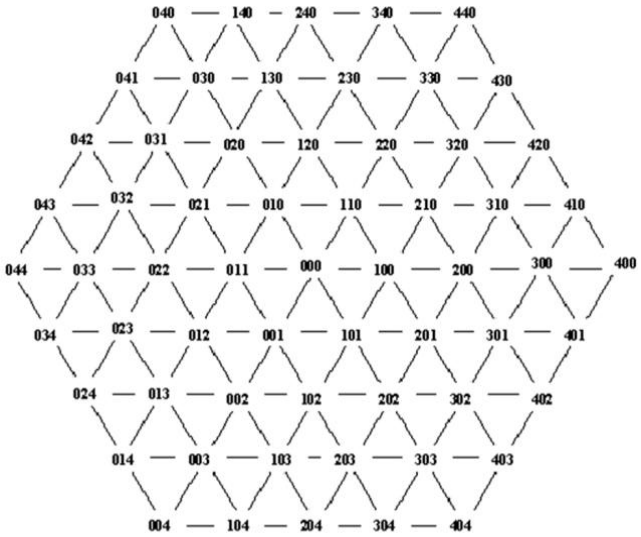

Figure 4.9 Space Vector Diagram for a Five Level Inverter

Numerous publications on two-dimensional space vector modulation strategies are developed and applied to multilevel inverters with equal dc sources. Previous works from authors on 2-D SVPWM algorithms presented in Aneesh Mohamed et al (2009) and McGrath et al (2003) shows that the reference voltage vector is identified from a single sub hexagon. In the proposed 2-D SVPWM technique, the 2-D algorithm chooses two subhexagons randomly. From the two chosen subhexagons, the 2-D algorithm compares and selects the subhexagon that contains the nearest reference vector.

The selected subhexagon that contains the tip of the reference space vector is mapped to the inner subhexagon by subtracting the vector located at the center of the subhexagon, from which switching sequence generations are carried out. This comparison process helps in determining the appropriate subhexagon having the nearest reference vector as well as the sector to which the reference vector is pointing to is determined for calculating the switching states and the switching times.

After identification of the sector in which the tip of the reference vector is located, four adjacent triangles having four nearest state vectors (two redundant vectors) to the reference vector are identified. The adjacent switching vectors and its corresponding switching sequence for the multilevel inverter are determined. Then the algorithm determines the time duration of each switching sequence. Once the duration of the switching sequence is calculated, then its corresponding switching angles are determined. The 2-D algorithm proposed reduces the total harmonic distortion of output voltage of the inverter as the exact voltage vector is chosen for switching sequence generation. The proposed modulation is computational very efficient and cost effective which can be applied to multilevel inverters with any number of levels.

The shaded region in Figure 4.10 shows two subhexagons. They are represented as “subhexagon I” having vector 000 as the centre and “subhexagon II” having the vector 032 as the centre. Another “subhexagon III” is also considered, having a vector 330 as the centre. The inner subhexagon can be viewed as a space vector diagram of a two-level inverter whose inverter voltage vectors switch between the lower most levels. Subhexagon II can be also viewed as a space vector diagram of a two level inverter whose voltage vectors involve higher levels.

The shifting of subhexagon in the space vector diagram of a multilevel inverter to the zero vector 000 simplifies the switching time calculations associated with multilevel inverters. The shifting of subhexagon II in the space vector diagram of a multilevel inverter toward the zero vector 000 involves the mapping of the sectors of subhexagon II to the sectors of the inner subhexagon. This is done by subtracting the vector at the centre of the subhexagon II from its other vector.

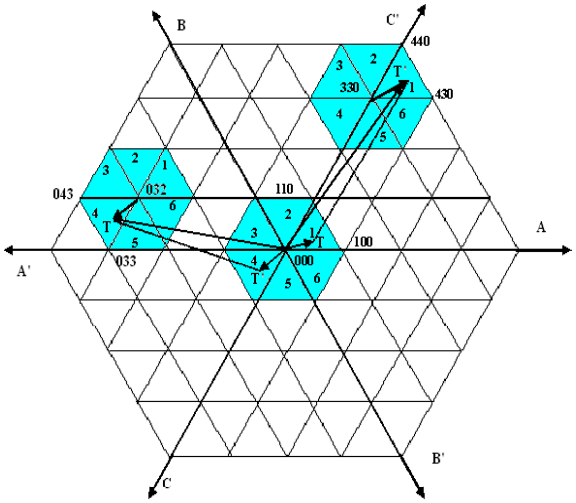

Figure 4.10 Mapping of Reference Space Vector for Switching Vector Generation

In a reverse approach of mapping, the inner subhexagon can be mapped to subhexagon II by adding the voltage space vector at the centre of subhexagon II to the vector of the inner subhexagon. Consider the voltage vectors 000, 001, 101 and 111 associated with sector 5 of the inner subhexagon and the voltage space vector 032 which is the vector at the centre of subhexagon II. Adding the voltage space vector 032 to the voltage space vector associated with sector 5 of the inner subhexagon gives the vectors 032 (001+033), 022(101+022) and 421(100+021), which are the vectors associated with sector 5 of subhexagon.

Also, the voltage space vector associated with any subhexagon can be generated by adding the vector at the centre of the particular subhexagon to the voltage space vector of the corresponding sectors in the inner subhexagon. The mapping of the inner subhexagon to any other outer subhexagon called as reverse mapping is used to generate the vectors associated with any sector in the space vector diagram of the multilevel inverter is presented in Aneesh Mohamed et al (2009).

B. Determining the Centre of the subhexagon

The space vector diagram of a five-level inverter, shown in Figure 4.11 can be viewed as the form of five levels with four layers. These levels are represented as Level 1 to 5. The instantaneous reference space vector lying in layer4 (P=4) and within the S_1 region forms a triangular shape.

Depending upon the layer of operation of the instantaneous reference space vector, all vectors for the center of the subhexagon are generated, and the vector which is closest to the reference space vector is taken as the center of the subhexagon. Figure 4.11 also shows the six 60^o regions S_1, S_2, S_3, S_4, S_5 and S_6.

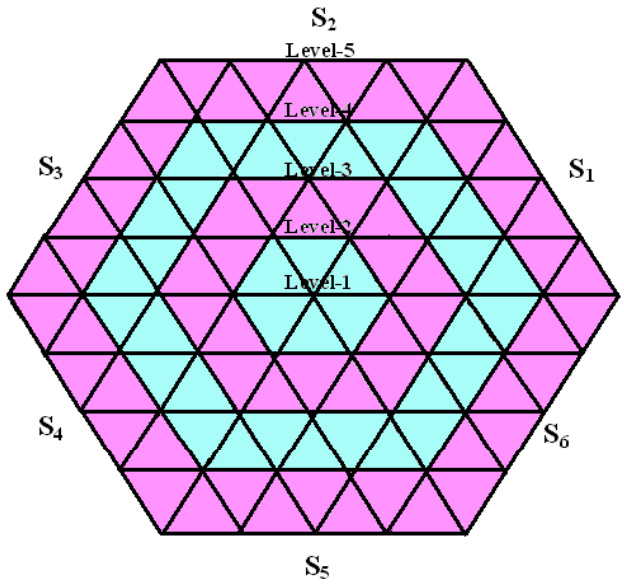

Figure 4.11 Levels in the Space Vector Diagram of a Five-Level Inverter

The subhexagon associated with the instantaneous reference space vector can be considered as centered on the inner side of layer 4. The instantaneous reference space vector can be resolved in to the axes V_x, V_y and V_z using the following where V_a, V_b and V_c are the instantaneous amplitude of the three reference phase voltages

$$V_x = \sqrt{3/2}\left(V_a - V_c\right)$$
$$V_y = \sqrt{3/2}\left(V_b - V_a\right) \quad (4.21)$$
$$V_z = \sqrt{3/2}\left(V_c - V_b\right)$$

The axis lying in the 60◦ region which contains the instantaneous reference space vector will have maximum magnitude among the values.

4.3.4 3-D Space Vector Pulse Width Modulation

A simple three-dimensional (3-D) space vector algorithm of multilevel inverters for mitigating harmonic content in three phase systems was proposed by Prats et al (2003), and Franquelo et al (2006). The three-dimensional SVPWM (3-D SVPWM) scheme computes the switching state vectors and the nearest switching sequence. The 3-D modulation technique allows directly compensating harmonics in three phase systems and optimizing the switching sequence minimizing the number of switchings.

Most of the SVM algorithms found in the literature for multilevel inverters use a representation of voltage vectors in $\alpha\beta\gamma$ coordinates, instead of using *abc* coordinates The $\alpha\beta\gamma$ representation offers an interesting information about the zero-sequence component of both currents and voltages (proportional to the *gamma* coordinate), however the change of reference frame have to be carried out, implies complex calculations. In addition, the three-dimensional (3-D) representation of the switching vectors, in $\alpha\beta\gamma$ is difficult to understand. Most methods based on $\alpha\beta\gamma$ representation need to determine the “sextant” in which the desired voltage vector is included, which leads to many complicated operations, including rotations, complex comparisons etc.

Using $\alpha\beta\gamma$ coordinates, the possible tetrahedrons that compose the state vectors space have different shapes and volumes. It is not easy to develop computationally efficient modulation algorithms to find out the tetrahedron where the reference vector is pointing to. However, Zhang et al (2002) has developed 3-D SVPWM algorithms using $\alpha\beta\gamma$ coordinates for three-leg four-wire (3L4W) topologies. But these algorithms are complex and their computational cost is very high.

This is the fundamental drawback of this type of 3-D SVPWM algorithms. Therefore, it is necessary to change the way of representation for the multilevel state vectors space. This is the reason because *abc* coordinates are used by other authors doing modulation algorithms very simple and more easily implemented. In order to reduce the 3-D SVPWM computational cost, multilevel inverters state vectors space can be represented using *abc* coordinates instead of $\alpha\beta\gamma$ coordinates.

The 3-D SVPWM techniques carry out a search of the four nearest state vectors to determine the switching sequence. Using *abc* coordinates, the 3-D SVPWM algorithm control complexity and the computational load is lower than using $\alpha\beta\gamma$ coordinates. Using *abc* coordinates, the control region is a cube or a prism for three-legged inverter. The 3-D SVPWM technique presented in need to synthesis 3-D vector space and identifies the subcube where the reference vector is located. Once this subcube is determined, it is divided into six tetrahedrons, and the 3-D SVPWM has to calculate the tetrahedron where the reference vector is pointing to.

Finally, the switching sequence and the corresponding duty cycles are determined. This technique can be used as the modulation algorithm in all applications needing a 3-D vector control such as an active filter, where the conventional 2-D SVM cannot be used. The 3-D space vector modulation

schemes are supersets of, and as a result 3-D SVPWM is compatible with conventional two dimensional space vector modulation schemes.

4.3.4.1 Synthesis of Reference Vector

The 3-D space vector modulation is to synthesize the reference vector V_{ref} using the switching vectors in the abc coordinate. It is similar to that of 2-D space vector modulation (describe in section 4.2). Synthesis of the reference vector in abc coordinates needs to take the following steps: (1) selection of switching vectors and (2) sequencing the switching vectors.

4.3.4.1.1. Selection of Switching Vectors

For the 2-D space vector modulation it is easy to identify the adjacent switching vectors. For 3-D space vector, it takes the following steps to identify the adjacent vectors.

1. The 3-D SVPWM techniques carry out a search of the four nearest state vectors to determine the switching sequence. Using abc coordinates, the control region is a cube or a prism for a three-legged inverter. Then the control region is divided into several sub-cubes. The four vectors nearest to the reference vector must be identified. The 3-D SVPWM algorithm easily calculates the four state vectors which generate the reference vector. The multilevel control region is a cube, which is divided into several sub-cubes and the first step of the modulation algorithm is to find the sub-cube where the reference vector is pointing to. The cubes in three-dimensional space are formed by a certain number of sub-cubes depending on the number of the levels of the inverter. Only one subcube for two-level inverters, eight sub-cubes for

three-level inverters, twenty-seven sub-cubes for four-level inverters. In general, $(n-1)^3$ sub-cubes into each cube, where n is the number of levels of the multilevel inverter.

2. Once this subcube is determined, it is divided into six tetrahedrons. Thus, the reference vector will be pointing to a volume which is a tetrahedron. Within each sub-cube, six tetrahedrons can be identified. The adjacent switching vectors are defined by the tetrahedrons. Therefore, it is necessary to define the tetrahedron where the reference vector is pointing to. This tetrahedron is easily found using comparisons with three 45^0 planes into the 3-D space, which define the six tetrahedrons inside the subcube. The three planes define the six tetrahedrons. Notice that only a maximum of three comparisons are needed regardless the inverter number of levels.

3. Once *abc* coordinates are known, the algorithm calculates the four state vectors corresponding to the four vertices of the tetrahedron into the selected sub-cube, which form the switching sequence. These vectors will generate the reference vector. Configurations of the 3-D space with different numbers of tetrahedrons in the cube have been studied. However, the minimum number of comparisons is obtained using the six tetrahedrons.

4.3.4.1.2. Sequencing of the Switching Vectors

The SVPWM algorithm calculates the four state vectors into the 3-D space and the corresponding duty-cycles and a maximum of three comparisons for calculating the suitable tetrahedron. The computational load is always the same and it is independent of the number of levels. In addition,

the algorithm provides the switching sequence that minimizes the total harmonic distortion.

4.3.4.2 Calculation of the duty cycles

Once the state vectors which generate each reference vector are known, the corresponding duty-cycles are calculated. The numeric evaluation of the duty cycles or on-state durations of the switching states are reduced to a simple addition. The algorithm generates a matrix S with four state vectors and the corresponding switching times t_i. Where S_a^i, S_b^i, S_c^i with $i = 1,..,4$ are the coordinates of each state vector and d_i is the corresponding duty cycle

$$S = \begin{bmatrix} S_a^1 & S_b^1 & S_c^1 \\ S_a^2 & S_b^2 & S_c^2 \\ S_a^3 & S_b^3 & S_c^3 \\ S_a^4 & S_b^4 & S_c^4 \end{bmatrix} \begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ d_4 \end{bmatrix} \qquad t_i = d_i T_m \qquad i = 1,..,4 \tag{4.22}$$

Where, T_m is the sample time.

The coordinates abc represent the different voltage levels between each phase and the neutral. They take values between zero and $2(n-1)$, where n is the number of levels of the multilevel inverter. The duty cycles are only functions of the reference vector components and the integer part of reference vector coordinates. In addition, the optimized switching sequence is selected in order to minimize the number of switching.

4.3.5 Optimized Three-Dimensional SVPWM for Balanced and Unbalanced Systems

A simple and generalized 3-D OSVPWM (optimized 3-D space vector modulation) is presented for multilevel inverters, which can be used for

any number of levels of multilevel inverter. The 3-D OSVPWM scheme proposed is similar to the existing 3-D SVPWM presented in Prats et al (2003), and Leon et al (2009)**,** following the similar notation. Since the proposed scheme is similar to the already existing 3-D SVPWM scheme, once the duty cycle, which is the function of reference vector components is calculated. Then it translates the generating vectors into switching pulses. In general, the SVPWM techniques are used to generate an average voltage vector equal to the reference voltage vector.

In two-dimensional SVPWM (2-D SVPWM), the space vectors are contained in a plane when the system is balanced without triple harmonics. A perfect balance of the dc voltages of a multilevel inverter cannot be achieved in all loading conditions. Load imbalances or transient loads have a significant impact on the multilevel inverter dc voltage ripple. In this case, 2-D SVPWM modulation techniques are not prepared for this unbalance because they do not take it into account to carry out the modulation process. As a result, errors appear in the output modulated voltages because they do not match to the desired output voltages when they are brought to average over a period of switching.

This fact leads to an increase of the harmonic distortion of the output voltages and currents of the multilevel inverters. This problem has been previously addressed by Blaabjerg et al (1999) and Enjeti and Shireen (1992), avoiding the influence of the dc-link voltage ripple on the output signals for two-level inverters. Previous works from Parts et al (2003) and Leon et al (2009) focused on 3-D SVPWM algorithm shows the reference vectors are not on a plane, if the system is unbalanced for multilevel inverter. A new three-dimensional space vector modulation scheme named as 3-D OSVPWM is presented. The simple and generalized 3-D OSVPWM scheme proposed for multilevel inverter is an improved version of the previous 3-D

SVPWM technique because the proposed technique can be used for any number of levels of the multilevel inverter. The 3-D OSVPWM technique presented, takes into account the actual unbalance of the multilevel inverter to carry out the necessary calculations, avoiding errors in the modulation process. The proposed 3-D OSVPWM algorithm maintains 120^0 phase for each phase to compute switching state vectors and the nearest switching sequence. The reference vectors are on a plane with 120^0 phase shift for each phase.

Each switching state of the inverter is represented by a switching voltage vector. The method is to choose the vectors that, applied during a certain time over the switching period, produce a voltage vector equal to the reference or desired voltage vector. The proposed 3-D OSVPWM algorithm permits the on-line selection of the nearest space vectors sequence for generating the reference voltage vector. The 3-D OSVPWM algorithm readily computes the nearest switching vectors sequence to the reference vector and calculates the on-state durations of the respective switching state vectors. Since each vector maintains an equal phase difference for each phase, the flow of zero–sequence current is automatically nullified as there will be no γ component in the voltage vector and the reference vectors will be contained on a plane.

When the system becomes unbalanced, there is no zero–sequence component of both current and voltage (proportional to the γ coordinate) or triple harmonics because the reference vectors are on an equal 120^0 phase shift plane. So the 3-D space vector representation and mapping will be similar to that of 2-D one. This technique can be used as modulation algorithm in all applications needing a 3-D control vector such as active filters, where the conventional two dimensional space vector modulations cannot be used. The unequal dc voltage does not affect the THD of the output waveform, leading

to an economical cost and reduction of the harmonic content. The 3-D OSVPWM can be applied to multilevel inverters with any number of levels. Using the proposed 3-D OSVPWM, balanced and unbalanced systems can be modulated with balanced or unbalanced dc voltages.

4.3.5.1 Determination of 3-D Control Region

In the 3-D SVPWM technique explained in Section 4.3.4., the dc voltages of a multilevel inverter are not balanced. Therefore, the existing 3-D SVPWM technique cannot be used because the 3-D control region changes and it is not formed by regular cubes. The 3-D control region of a multilevel inverter changes because the distinct locations of the switching state vectors move due unbalance in the voltage. Three different dc voltages V_{dc1}, V_{dc2} and V_{dc3} have to be considered for a three-bridge fourteen-level cascaded multilevel inverter. The various possible $V_{phase\text{-}0}$ voltages of the multilevel inverter are $0, V_{dc1}, V_{dc1}+V_{dc2}$ and $V_{dc1}+V_{dc2}+V_{dc3}$. The phase states can be represented using generalized dc voltages V_{dc1}, V_{dc2} and V_{dc3}.

In general, the 3-D control region formed will be cube with size $V_{dc1}+V_{dc2}+V_{dc3}$, which forms several rectangular sub cubes with different sizes, depending on the voltages of different dc sources. The 3-D control region of a fourteen-level power inverter having $V_{dc1} < V_{dc2} < V_{dc3}$ is represented in Figure 4.12. The λ_i values are the size of the sub cubes that form the 3-D control region, are as follows:

$$V_{dctotal} = V_{dc1} + V_{dc2} + \ldots\ldots + V_{dcn} \tag{4.23}$$

$$\lambda_i = \frac{V_{di}}{V_{dctotal}} \tag{4.24}$$

The actual output voltages of the multilevel inverter are determined from the vector V_o. The elements of the vector V_o are in increasing order from zero to the positive value. In the N-level inverter, the vector is represented as

$$V_o = \{0, V_{dc1}, V_{dc1}+V_{dc2}, ..., V_{dc1}+...+V_{dcn-1}\} \quad (4.25)$$

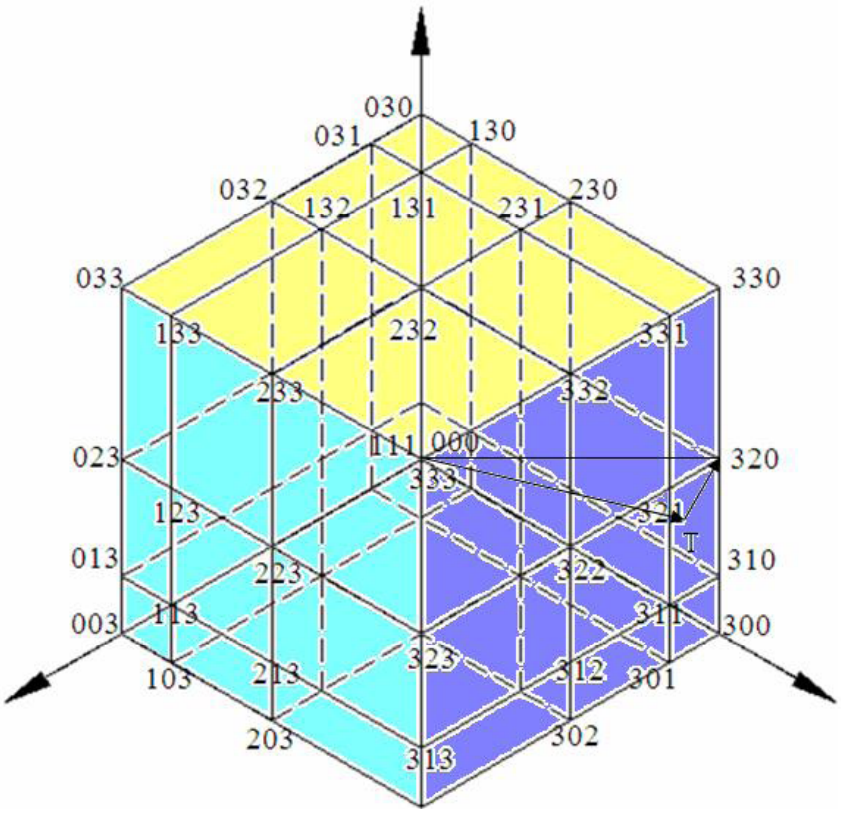

Figure 4.12 Three-Dimensional Control Region of a Five –Level Inverter with Voltage Unbalance in the DC Link $Vdc_1<Vdc_2<Vdc_3$

Normalizing the vector V_o with respect to the total dc voltage generating vector V_{on}

$$V_{on} = \frac{V_o}{V_{dctotal}} \tag{4.26}$$

$$V_{on} = \left\{ 0, \frac{V_{dc1}}{V_{dctotal}}, \frac{V_{dc1}+V_{dc2}}{V_{dctotal}}, ..., \frac{V_{dc1}+...+V_{dcn-1}}{V_{dctotal}} \right\} \tag{4.27}$$

$$= \left\{ 0, \lambda_1, \lambda_1 + \lambda_2, ..., \lambda_1 + ... + \lambda_{N-1} \right\} \tag{4.28}$$

$$= \left\{ 0, \lambda_1, \lambda_1 + \lambda_2, ..., 1 \right\} \tag{4.29}$$

4.3.5.2 Reference vector normalization

The reference vector calculated is defined as $V_{refn} = \{V_a, V_b, V_c\}$ where V_j is the voltage of phase *j* with respect to point zero. The reference vector V_{ref} is normalized using the total dc voltage of the multilevel inverter. The normalized reference voltages V_a, V_b and V_c take values between zero and one.

The reference vector in the n^{th} component is represented as

$$V_{refn} = \{ v_a, v_b, v_c \} = \left\{ \frac{V_a}{V_{dctotal}}, \frac{V_b}{V_{dctotal}}, \frac{V_c}{V_{dctotal}} \right\} \tag{4.30}$$

4.3.5.3 Algorithm for generating switching angles

1) Read the instantaneous magnitudes of phase voltages.
2) Determine the coordinates of the instantaneous space vector.
3) The coordinates of the reference space vector is normalized through division by the normalization constant $V_{DC} / n - 1$.
4) Determine the tetrahedron region enclosing the normalized cube for an *n*-level inverter.

5) Calculate the modulation index *m*, which is determined by a number of iterations repeatedly applied to various tetrahedrons.

6) Identify the tetrahedron region having *m*, calculated in step (5)

7) Determine the centroid of each of the four triangles. Also determine the tetrahedron with centroid closest to the 16 triangles.

8) Each triangle gives three vectors and switching states.

9) Determine the nearest switching angle and the resultant *m* from step (5), go to next step, else go to step (7).

10) The tetrahedron finally determined represents the tetrahedron enclosing the space vector.

11) Continue the process of identifying the voltage space vector in different tetrahedron of the cube.

12) Select the zero vector from the vectors located at the vertices of the identified subcube.

4.3.5.4 Determination of the tetrahedron

Several iterations are carried out over each component to find out the nearest centroid of the tetrahedral region enclosing the normalized subcube. Several iterations are carried out in phase a, to find where v_a is located inside V_{on} vector, comparing with each element. Finally, the lower and upper closer elements in vector V_{on} of the range where v_a is located can be determined. For example, for the four level stages, it is as follows

$$V_{on}=\left\{0,\ \frac{V_{dc1}}{V_{dc1}+V_{dc2}+V_{dc3}},\ \frac{V_{dc1}+V_{dc2}}{V_{dc1}+V_{dc2}+V_{dc3}},\ \frac{V_{dc1}+V_{dc2}+V_{dc3}}{V_{dc1}+V_{dc2}+V_{dc3}}\right\} \tag{4.31}$$

$$= \{0,\ \lambda_1,\ \lambda_1+\lambda_2,\ \lambda_1+\lambda_2+\lambda_3\} \tag{4.32}$$

$$= \left\{0,\ \frac{1}{3},\ \frac{2}{3},\ 1\right\} \tag{4.33}$$

If $\lambda_1 < v_a < 1$, the factor v_a is λ_1 and the factor Vs_a is one. For each phase of the reference vector this process is repeated to calculate the vector $V_{abc} = \{V_a, V_b, V_c\}$ which is the nearest centroid of the triangular region where the reference vector $\{V_a, V_b, V_c\}$ is located. Also, the vector $Vs_{abc} = \{Vs_a, Vs_b, Vs_c\}$ is determined. Vectors $\Delta = \{\lambda_a, \lambda_b, \lambda_c\}$ and $\Delta V = \{\rho_a, \rho_b, \rho_c\}$ can be calculated.

$$\Delta = \{\lambda_a, \lambda_b, \lambda_c\} = \{Vs_a - V_a, Vs_b - V_b, Vs_c - V_c\} \tag{4.34}$$

$$\Delta V = \{\rho_a, \rho_b, \rho_c\} = \{v_a - V_a, v_b - V_b, v_c - V_c\} \tag{4.35}$$

The switching sequences and the duty cycles calculations are summarized in Table 4.1 and the parameters μ_a, μ_b and μ_c in the table are defined as

$$\mu_a = \frac{\rho_a}{\lambda_a},\ \mu_b = \frac{\rho_b}{\lambda_b},\ \mu_a = \frac{\rho_c}{\lambda_c} \tag{4.36}$$

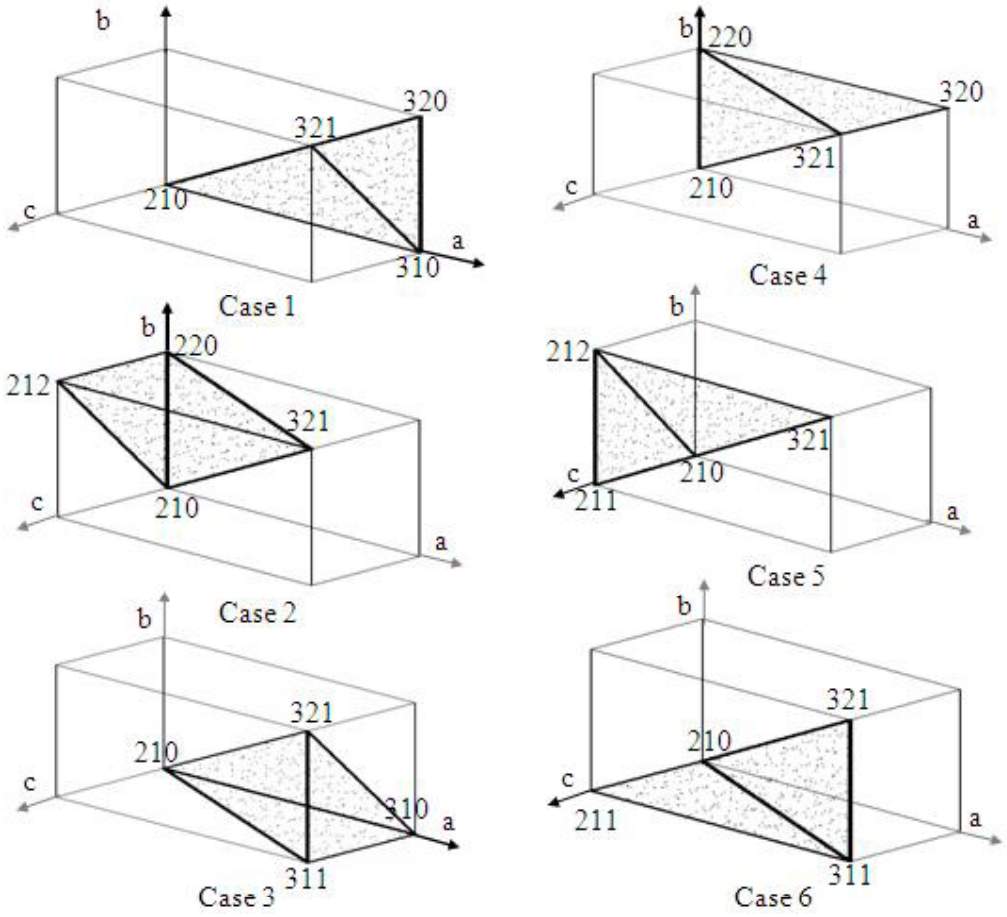

Figure 4.13 Division of Each Rectangular Subcube of the 3-D SVPWM Control Region of a Multilevel Inverter with Unbalanced DC Voltages

The proposed modulation technique finds out the four nearest state vectors to form the switching sequences to generate the reference voltage. The switching sequence consisting of four nearest state vectors have four tetrahedron in each sub cube and six different cases is shown in Figure 4.13. Determine the centroid of each of the four triangles; each triangle gives three vectors and a switching state.

Table 4.1 Switching sequence and Duty Cycles Determined by the 3-D SVPWM Technique

S. No	Cube Cases	State Vector Sequences	Duty Cycles
1	Case 1	210, 310, 321 210, 310, 320 210, 321, 320 321, 310, 320	$D = 1-\mu_a$ $D = \mu_a - \mu_c$ $D = \mu_c - \mu_b$ $D = \mu_b$
2	Case 2	210, 212, 220 210, 212, 321 210, 220, 321 212, 321, 220	$D = 1-\mu_c$ $D = \mu_c - \mu_a$ $D = \mu_a - \mu_b$ $D = \mu_b$
3	Case 3	210, 311, 310 210, 311, 321 210, 310, 321 310, 311, 321	$D = 1-\mu_c$ $D = \mu_c - \mu_b$ $D = \mu_b - \mu_a$ $D = \mu_a$
4	Case 4	210, 321, 220 210, 320, 220 210, 321, 320 220, 320, 321	$D = 1-\mu_b$ $D = \mu_b - \mu_a$ $D = \mu_c - \mu_a$ $D = \mu_a$
5	Case 5	210, 211, 212 210, 321, 212 210, 321, 211 212, 321, 211	$D = 1-\mu_b$ $D = \mu_b - \mu_a$ $D = \mu_a - \mu_c$ $D = \mu_c$
6	Case 6	210, 311, 321 210, 311, 211 210, 211, 321 211, 311, 321	$D = 1-\mu_a$ $D = \mu_a - \mu_c$ $D = \mu_b - \mu_c$ $D = \mu_c$

4.4 2-D SVPWM ALGORITHM COMPONENTS

Figure 4.14 shows the block diagram designed for the 2-D algorithm, which included the following components: frequency, $dq2\alpha\beta$, 2-DSVM, $\alpha\beta 2abc$, PWM3 and dead time.

4.4.1 Component Frequency-

The user can select one of four modulator switching frequencies available by means of the input signal f_s. The selected frequency defines the needed values for the switching period T and the dead time T_d. A dead time of 5% of the switching period was used.

4.4.2 Component dq to αβ

This element carries out the following dq to $\alpha\beta$ transformation of the reference vector $\left[v_r{}^d, v_r{}^q\right]$ from the rotational frame to the stationary frame.

$$\begin{bmatrix} v_r{}^\alpha \\ v_r{}^\beta \end{bmatrix} = \begin{bmatrix} \sqrt{3} & -1 \\ 0 & 2 \end{bmatrix} \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_r{}^d \\ v_r{}^q \end{bmatrix} \tag{4.37}$$

4.4.2.1 Component 2-DSVM

This component is the core of the system. It determines the nearest three vector $\left[v_{s1}{}^\alpha, v_{s1}{}^\beta\right]^T$, $\left[v_{s2}{}^\alpha, v_{s2}{}^\beta\right]^T$ and $\left[v_{s3}{}^\alpha, v_{s3}{}^\beta\right]^T$ to the reference vector in the $\left[v_r{}^\alpha, v_r{}^\beta\right]^T$ in the $\alpha\beta$ frame and calculates their corresponding switching times which is presented in Celanovic and Boroyevic (2001).

4.4.2.2 Component αβ to abc

This component transforms back three nearest vectors from $\alpha\beta$ to the abc frame. This is achieved by evaluating the Equation 4.37. This expression has multiple solutions. Therefore, the following algorithm was developed to obtain a vector sequence that minimizes the number of switchings. The twenty four triangular regions have been joined in the six highlighted groups shown in Figure 4.15. The vector sequence starts with the boxed vector of the group, and it is tailored with adjacent vectors. The $\left[v_{s1}{}^{a}, v_{s1}{}^{b}, v_{s1}{}^{c} \right]^{T}$ is the boxed vector and vector $\left[v_{s2}{}^{a}, v_{s2}{}^{b}, v_{s2}{}^{c} \right]^{T}$ and $\left[v_{s3}{}^{a}, v_{s3}{}^{b}, v_{s3}{}^{c} \right]^{T}$ are taken accordance with the arrow inside the region.

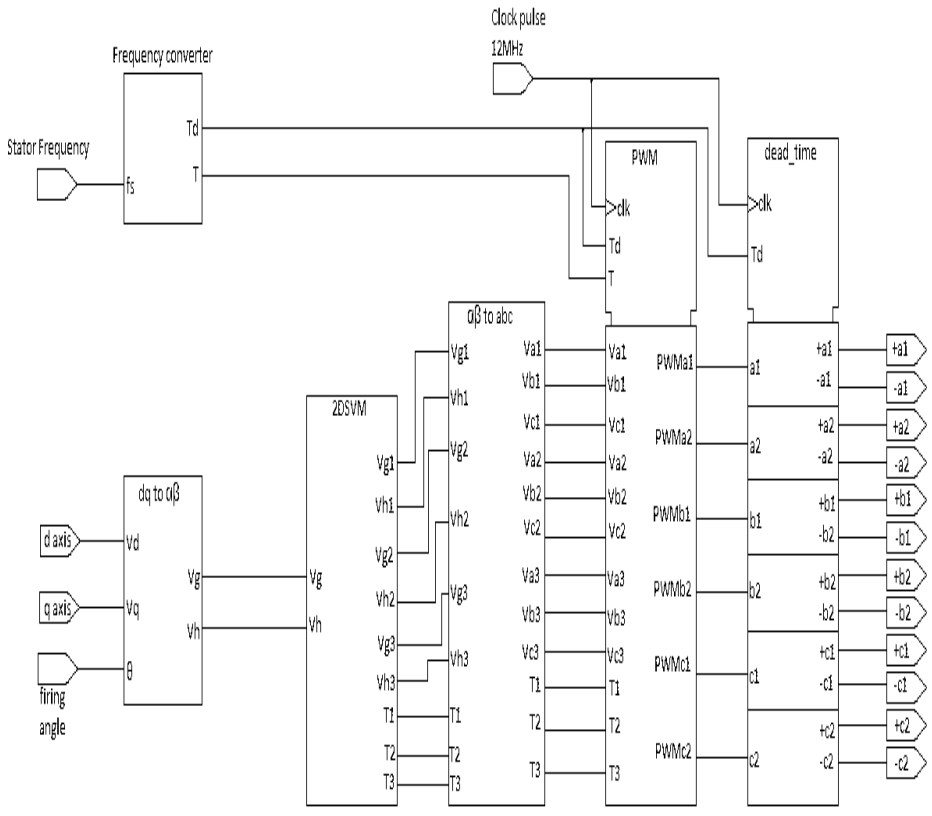

Figure 4.14 2-DSVPWM Algorithm

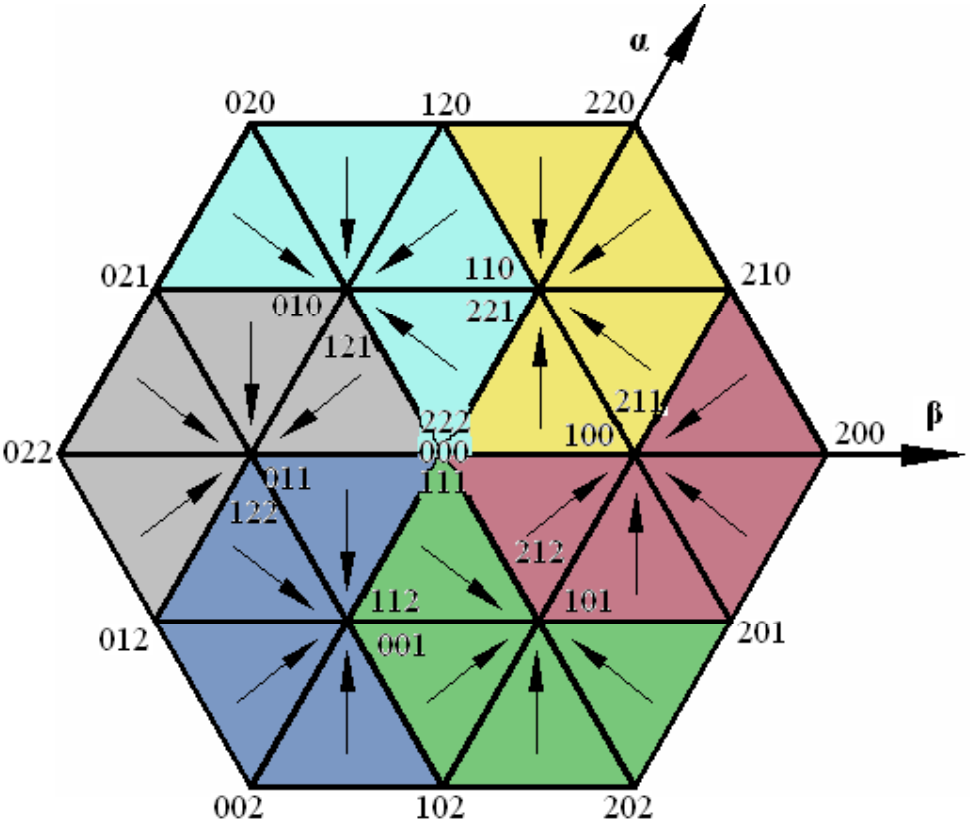

Figure 4.15 Switching Vector Sequence Selection

The following components PWM3 generates a symmetrical sequence that starts and ends with the same vector, therefore, there are no additional switchings when the reference vector changes between triangular regions that belong to the same group, but it only adds two extra switchings when the reference changes to the next group. Hence, this vector selection method minimize the number of switchings when the reference vector stays inside a region as well as when it changes region.

4.4.2.3 Components PWM3

It arranges the three vectors of the sequence in the symmetrical way into the switching period. The sequence generated is the following.

$$
\begin{aligned}
&\left[v_{s1}{}^{a}, v_{s1}{}^{b}, v_{s1}{}^{c} \right]^{T} && \text{------} \frac{T_1}{4} \\
&\left[v_{s2}{}^{a}, v_{s2}{}^{b}, v_{s2}{}^{c} \right]^{T} && \text{------} \frac{T_2}{2} \\
&\left[V_{s3}{}^{a}, V_{s3}{}^{b}, V_{s3}{}^{c} \right]^{T} && \text{------} \frac{T_3}{2} \\
&\left[v_{s1}{}^{a+1}, v_{s1}{}^{b+1}, v_{s1}{}^{c+1} \right]^{T} && \text{------} \frac{T_1}{2} \\
&\left[V_{s3}{}^{a}, V_{s3}{}^{b}, V_{s3}{}^{c} \right]^{T} && \text{------} \frac{T_3}{2} \\
&\left[v_{s2}{}^{a}, v_{s2}{}^{b}, v_{s2}{}^{c} \right]^{T} && \text{------} \frac{T_2}{2} \\
&\left[v_{s1}{}^{a}, v_{s1}{}^{b}, v_{s1}{}^{c} \right]^{T} && \text{------} \frac{T_1}{4}
\end{aligned}
\qquad (4.38)
$$

After that, it generates the six PWM signals corresponding to each complementary pair of switches.

4.4.2.4 Components dead-time

Finally, this circuit generates the trigger signal for each power switch, introducing the proper dead time to give each Metal Oxide Semiconductor Field Effect Transistor (MOSFET) enough time to switch off, before its complementary one is switched on. This is done, as shown in Figure 4.17 by delaying the rising edges of the trigger signals by the time T_d.

4.4.3 3D SVPWM Components

Figure 4.16 shows the block diagram designed for the 3-D algorithm, which includes the following components: frequency, $dq2abc$, 3D SVPWM, PWM4 and dead time.

4.4.4 Component Frequency

This block is similar to the one used in the 2D SVPWM algorithm for calculating the switching period T and the dead time T_d.

4.4.5 Component *dq* to *abc*

This component implements the following $dq2abc$ co-ordinate transformation

$$\begin{bmatrix} v_r^{\,a} \\ v_r^{\,b} \\ V_r^{\,c} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 0 \end{bmatrix} \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} v_r^{\,d} \\ v_r^{\,q} \end{bmatrix} \tag{4.39}$$

4.4.5.1 Component 3DPWM

This component finds the four nearest switching vectors $\left[v_{s1}^{\,a}, v_{s1}^{\,b}, v_{s1}^{\,c}\right]^T$, $\left[v_{s2}^{\,a}, v_{s2}^{\,b}, v_{s2}^{\,c}\right]^T$, $\left[v_{s3}^{\,a}, v_{s3}^{\,b}, v_{s3}^{\,c}\right]^T$, and $\left[v_{s4}^{\,a}, v_{s4}^{\,b}, v_{s4}^{\,c}\right]^T$ to the reference vector and calculates their corresponding switching times, and the resulting sequences minimizes of switches.

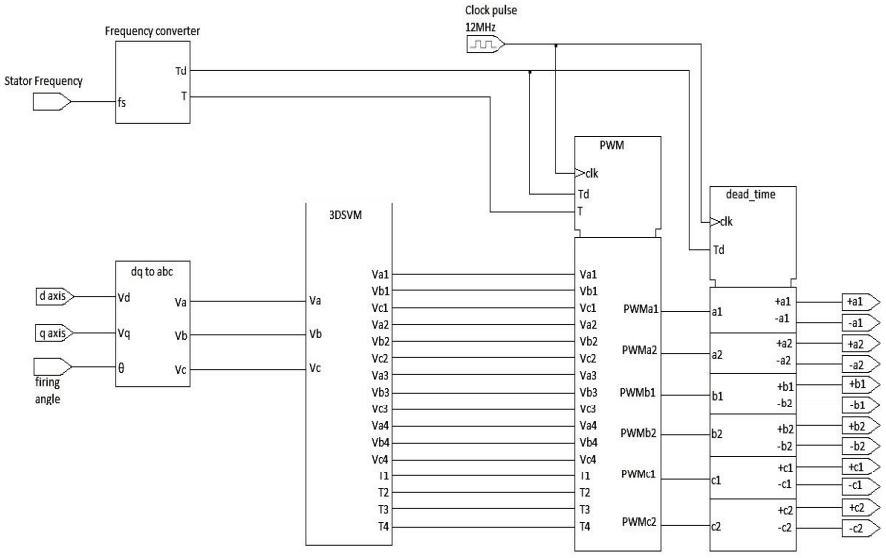

Figure 4.16 3D SVPWM Algorithm

4.4.5.2 Components of PWM

This block is very similar to the PWM3 but working with four input vectors instead of three. It arranges the vectors in a symmetrical way into the switching time and generates the Six PWM signals corresponding to each complementary pair of MOSFETs. The sequence generated is the following.

$$
\begin{aligned}
&\left[v_{s1}{}^{a}, v_{s1}{}^{b}, v_{s1}{}^{c} \right]^{T} \quad \text{------} \frac{T_1}{2} \\
&\left[v_{s2}{}^{a}, v_{s2}{}^{b}, v_{s2}{}^{c} \right]^{T} \quad \text{------} \frac{T_2}{2} \\
&\left[v_{s3}{}^{a}, v_{s3}{}^{b}, v_{s3}{}^{c} \right]^{T} \quad \text{------} \frac{T_3}{2} \\
&\left[v_{s4}{}^{a}, v_{s4}{}^{b}, v_{s4}{}^{c} \right]^{T} \quad \text{-------} T_4 \\
&\left[v_{s3}{}^{a}, v_{s3}{}^{b}, v_{s3}{}^{c} \right]^{T} \quad \text{------} \frac{T_3}{2} \\
&\left[v_{s2}{}^{a}, v_{s2}{}^{b}, v_{s2}{}^{c} \right]^{T} \quad \text{------} \frac{T_2}{2} \\
&\left[v_{s1}{}^{a}, v_{s1}{}^{b}, v_{s1}{}^{c} \right]^{T} \quad \text{------} \frac{T_1}{2}
\end{aligned}
\tag{4.40}
$$

4.4.5.3 Component dead time

This circuit generates the trigger signal for each power switch, introducing the proper dead time to give each MOSFET enough time to switch off, before its complementary one is switched on.

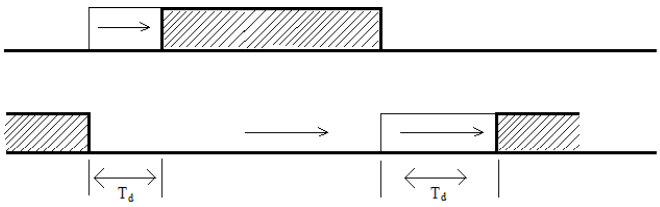

Figure 4.17 Dead Time Implementation

This is done, as shown in Figure 4.17 and to generate the twelve trigger signals inserting the corresponding dead times.

4.5 COMPONENT IMPLEMENTATION

The hardware description of the components of the algorithms shown in Figure 4.9 and 4.11 has been hand-coded in VHDL. An exception was made with the components dq to $\alpha\beta$ and dq to abc. These components have been developed in the Simulink with the System Generator libraries provided by Xilinx. The VHDL code that describes these components has been automatically generated using the System Generator tool, in order to produce a correct system implementation in a short design time.

4.5.1 Component Frequency

One of the four frequencies and dead time pairs can be selected by means of the two-bit signal f_s. Signals T and T_d are integer numbers that express the switching period and dead time in microseconds. Signal T is twelve bits wide, which allows periods of upto $1023\mu s$ i.e., $977.5Hz$. T_d is a

six bit signal, which allows defining a dead time upto $63\mu s$. The modulator switching period T and the corresponding dead time T_d are selected by means of a four-channel multiplexer, as shown in the Figure 4.18.

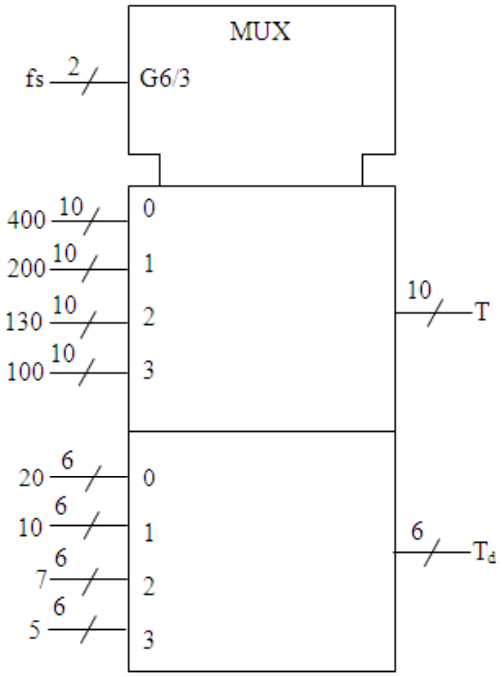

Figure 4.18 Component Frequency

4.5.2 Components *dq* to *αβ*

The implementation of transformation from the rotating to the stationary frames is given in Equation 4.37. Figure 4.19 shows the Simulink models used to describe the components and to generate the corresponding VHDL description files. Internal arithmetic operations are done with adequate precision using fixed-point number representation and two's complement format. The fractional part of the final result was rounded to 8-bits in order to calculate the switching times with adequate accuracy in the component 2-D SVPWM. For an n-level inverter in the 2-D SVPWM algorithm, the integer part of the result takes values from $-(n-1)\ to\ (n-1)$. Therefore 3 bit are

necessary to represent the integer part. The output signals in the 2-D case are 11-bit wide.

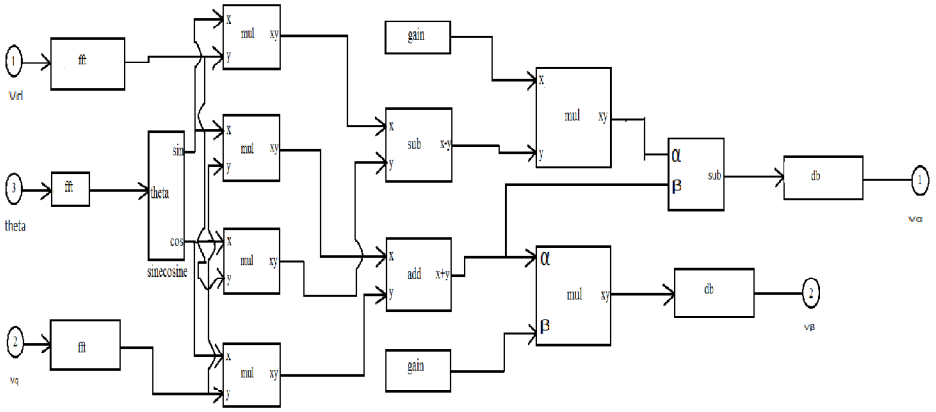

Figure 4.19 Component of dq to $\alpha\beta$

4.5.3 Components dq to abc

The component implements transformation Equation 4.39 from the rotating to the stationary frames. Figure 4.20 shows the Simulink models used to describe the components and to generate the corresponding VHDL description files. Internal arithmetic operations are done with adequate precision using fixed-point number representation and two's complement format. The fractional part of the final result was rounded to 8-bits in order to calculate the switching times with adequate accuracy in the component 3-D SVPWM. For an n-level inverter, in the 3-D SVPWM algorithm the integer parts of the results take values in the range $0\ to\ (n-1)$. Therefore, 2 bits are necessary to represent the integer part. Consequently, the output signals in the 3-D case are 10 bit wide. The 3-D SVPWM can be used without any modification for a CHB inverter of upto 5 levels. If the number of level increases then more bits would be needed to represent these signals properly. The sine and cosine operations have been implemented by means of a table

stored in a memory. 256 points of the sinusoidal waveform have been stored with 8-bits of resolution. In order to store the data a 256*8 memory is needed. Therefore an external RAM was used to take advantage of the FPGA hardware resources.

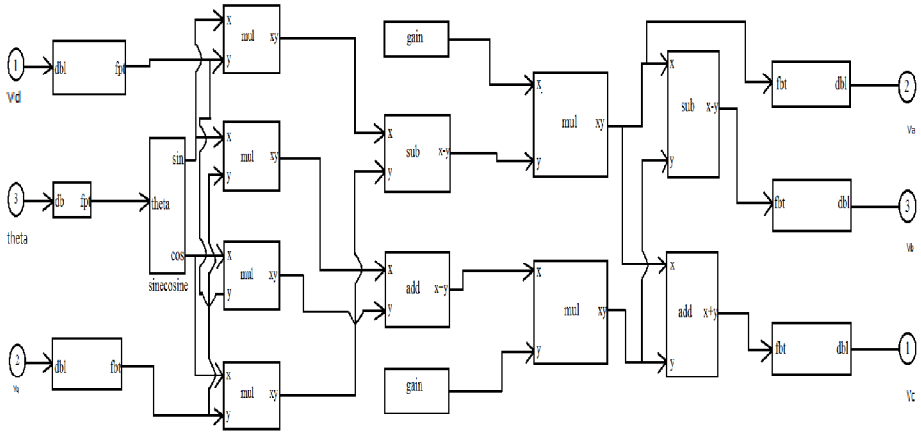

Figure 4.20 Component *dq* to *abc*

4.5.4 Component 2-D SVM

The 2-D SVPWM has been implemented strictly following the algorithm descriptions given in Celanovic and Boroyevic (2001) by means of simple arithmetic and comparison operations.

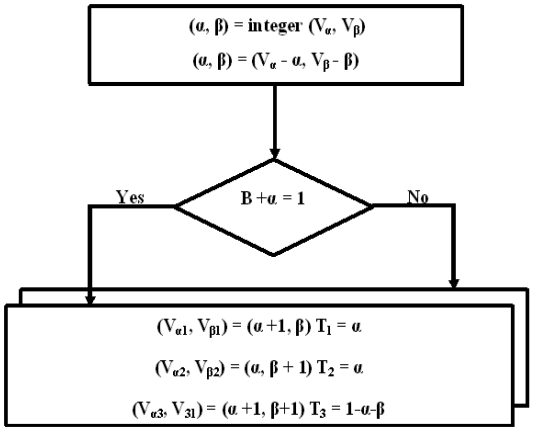

Figure 4.21 Flow Diagram of VHDL Description of the 2-D SVPWM Component

The nearest vector and switching times are calculated from the integer and fractional part of the reference. The signals corresponding to the vector component has been 3-bit in the 2-D algorithm and the unit switching times are 8-bit wide.

The integer and fractional part of the references can be done by the proper bit extraction from the fixed point number. Corrections have been done in the case of negative numbers in the 2-D algorithm. Figure 4.21 show the flow diagram of the VHDL description and the bit extraction operation.

4.5.5 Component 3D SVPWM

The 3-D SVPWM has been implemented strictly following the algorithm descriptions given in Prats et al (2003) by means of simple arithmetic and comparison operations.

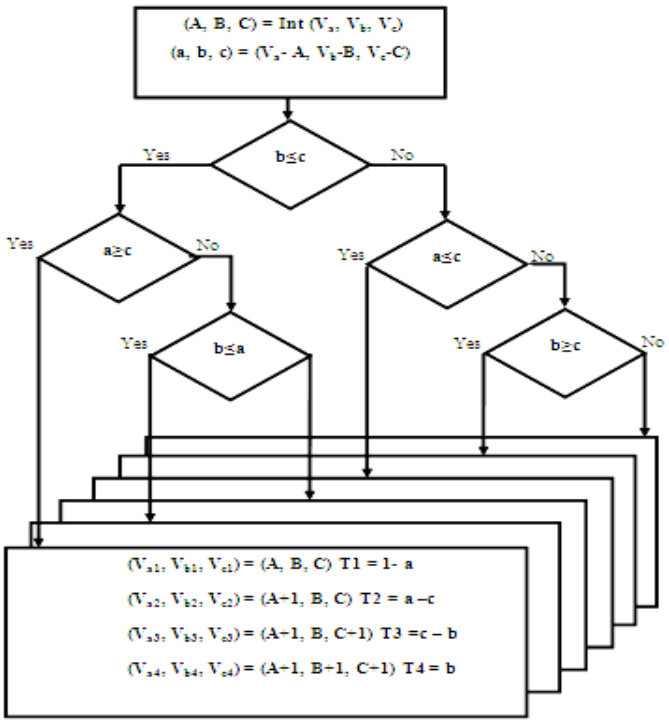

Figure 4.22 Flow Diagram of VHDL Description of the 3D SVPWM Component

The nearest vector and switching times are calculated from the integer and fractional part of the reference. The signals corresponding to the vector component has 2-bit in the 3-D algorithm and the unit switching times are 8-bit wide. Figure 4.22 shows the flow diagram of the VHDL description and the bit extraction operation.

4.5.6 Component $\alpha\beta$ to abc

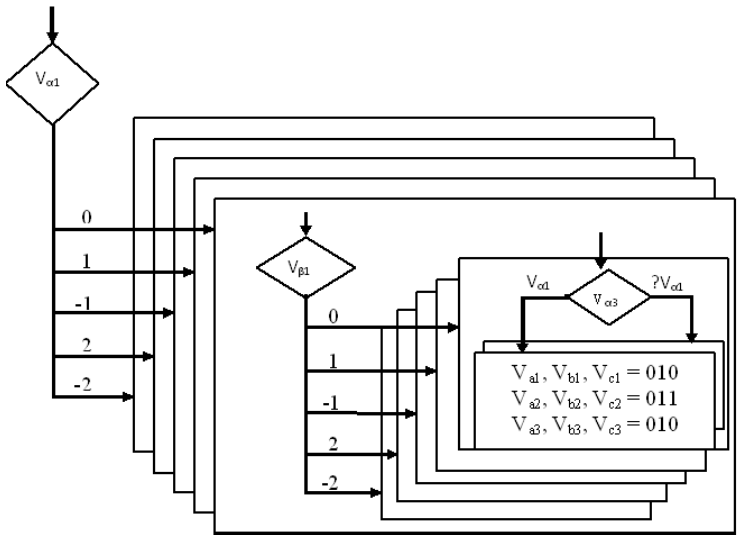

Figure 4.23 Flow Diagram of VHDL Description of the $\alpha\beta$ to abc component

Figure 4.23 shows the flow diagram utilized for the VHDL description of this block in accordance with Figure 4.15. As shown previously, the output signals of the component have 2-bits which are enough to represent the three levels of inverter.

4.5.7 Components PWM3 and PWM4

Figure 4.19 shows the PWM4 implementation. The implementation of component PWM3 is very similar. But, in this case unit time T_4 is not needed and the four vector is internally generated as

$$\left[v_{s4}{}^{a},\ v_{s4}{}^{b}, v_{s4}{}^{c} \right]^{T} = \left[v_{s1}{}^{a} + 1, v_{s1}{}^{b} + 1, v_{s1}{}^{c} + 1 \right]^{T} \tag{4.41}$$

The block sequence compares the switching time corresponding to each vector with the value of a counter to generate the vector index corresponding to each time interval. The 50 *MHz* master clock of the S_3 was divided using the digital clock manager of the FPGA in order to obtain a 10 *KHz* clock. That clock allows generating the PWM signals with a time precision of 0.1 µs. Due to the fact that vector times are 8-bit wide, then the maximum switching frequency available in the system is *100MHz* without the frequency division of the master clock, the maximum. Switching frequency could be increased 5 times, upto *125 KHz*. The output of the multiplexer is the space vector that must be generated by the inverter at a particular time.

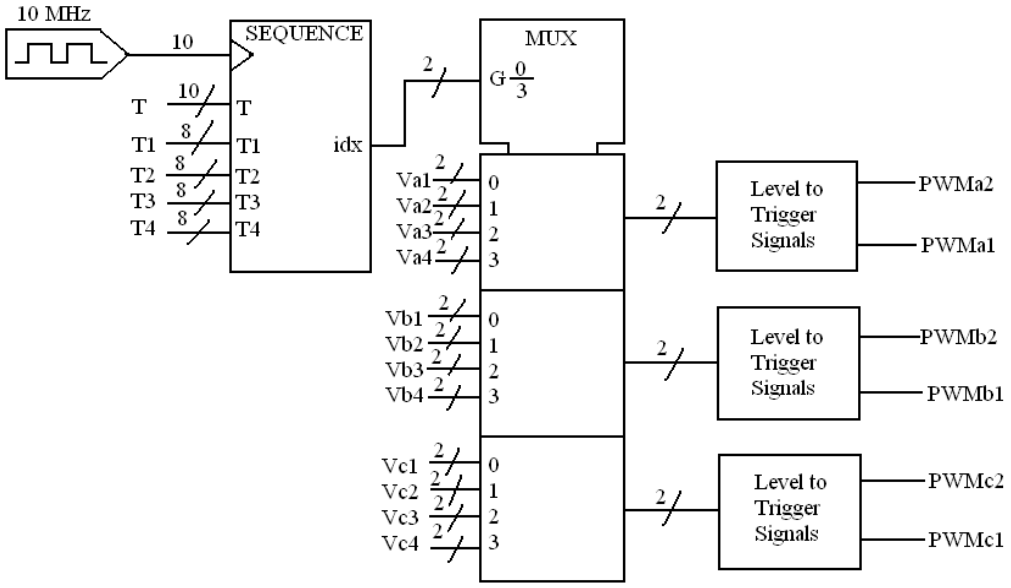

Figure 4.24 Component Diagram of the PWM4

The level of each phase in the corresponding trigger signals is translated by the component Level to trigger signal. This translation depends on the inverter topology, therefore this block must be redesigned if an inverter

different from the CHB is used. It is not necessary to modify the rest of components because both modulation algorithms do not depend on the topology.

4.5.8 Component Dead-Time

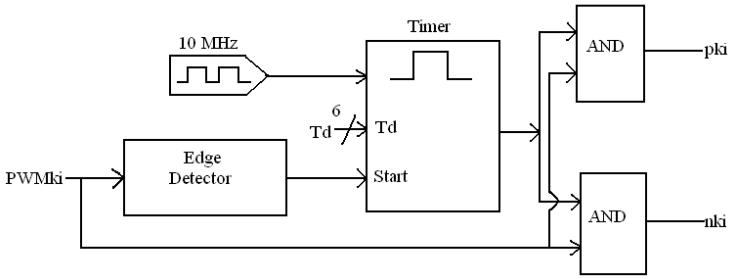

Figure 4.25 Component of Dead Time Description

This block generates the inverse of trigger signals adding the corresponding dead time. It was implemented using an edge detector together with a counter working as a timer in order to delay rising edges of the trigger signal as show in Figure 4.25.

4.6 RESOURCES

All circuits were combined in a top file according to Figure 4.14. and 4.16. Finally, the whole system is synthesized and implemented in the XS200E FPGA through the use of the Xilinx foundation ISE tools, which are specific for these tasks. Both algorithm implementations use only one ERAM, to generate the sine and cosine functions, but the 2-D algorithm uses half flip-flops and two hardware multipliers less than 3-D algorithm. This is because the first algorithm works with only three 2-D vectors, instead of four 3-D vectors of the second algorithm. Although the 2-D algorithm works with fewer vectors represented with fewer bits, both implementations use similar number of logic blocks and look-up tables (LUTs). This is due to the need for

an extra task to select the generating vectors in the 2-D algorithm. Consequently, the 3-D algorithm is easier to implement but uses more logical resources of the FPGA.

In order to extend the proposed implementation to a higher level inverter, many considerations have to be taken into account. The implementation of the component frequency is independent of the inverter topology; therefore it can be used without any modification. Components $dq\,to\,\alpha\beta$, $dq\,to\,abc$, 2-D SVPWM and 3-D SVPWM only need slight modifications in order to adapt the bit number of signals to the number of level of the inverter. Resources used by those components increases with the increase in the number of levels. In fact, they could be directly used for a five level topology. Components PWM3, PWM4 and dead-time have to be extended in order to generate additional PWM signals for extra MOSFET's of the inverter. Therefore, resources used by the additional components increases almost linearly with number of levels of the CHB inverter. The component $\alpha\beta\,to\,abc$ was designed for a five-level inverter.

4.7 COMPARISON OF SVPWM AND PWM

The SVPWM is considered a better technique of PWM implementation as it has some advantages over SPWM in terms of good utilization of dc-bus voltage, reduced switching frequency and low current ripple. SVPWM provides the following advantages: i) better fundamental output voltage; ii) useful in improving harmonic performance and reducing THD; and iii) easier hardware implementation in digital signal processor. SVPWM can be efficiently executed in a few micro seconds, achieving similar results compared with other PWM methods.

The carrier-based PWM methods were developed first and were widely used in most applications. One of the earliest modulation signals for carrier-based PWM is sinusoidal PWM (SPWM). The SPWM technique is based on the comparison of a carrier signal and a pure sinusoidal modulation signal. The SVPWM technique calculates and computes the duty cycles but SPWM technique derives through comparison. The utilization rate of the DC voltage for traditional sinusoidal PWM is only 78.5% of the DC bus voltage, which is far less than that of the six-step wave (100%). This technique can be used in single-phase and three-phase inverters. The SVPWM technique can increase the fundamental component by up to 27.39% that of SPWM. The fundamental voltage can be increased up to a square wave mode where a modulation index of unity is reached. The SVPWM is significantly better than SPWM by approximately 15.5%.

4.8 SUMMARY

In this chapter, two very efficient SVPWM techniques were discussed. The basic idea about SVPWM for three-legged voltage source inverter was discussed in detail. It is illustrated how the voltage space vectors are defined in a two-dimensional (2-D) plane and three-dimensional (3-D) plane for a cascaded H-bridge multilevel inverter. Furthermore, two-dimensional (2-D) and three-dimensional (3-D) space vector modulation algorithms are explained. Mathematical formulation for calculating switching angles and switching sequence was determined and the Fourier series theory was used to derive the harmonic equations corresponding to the multilevel switching scheme.

The basic idea about the existing three-dimensional space vector modulation schemes was discussed. Furthermore, the optimized three-dimensional (3-D) space vector modulation for balanced and unbalanced system was explained. A new 3-D OSVPWM technique is proposed to carry

out the necessary calculations taking the actual values of the dc voltages in the modulation process and therefore undesirable harmonic distortions in output waveform is avoided in unbalanced condition. The optimized 3-D space vector modulation algorithm for cascaded H-bridge inverter was proposed to handle the zero-sequence component caused by unbalanced load. Using the proposed 3-D OSVPWM, balanced and unbalanced systems can be modulated with balanced or unbalanced dc voltages. The computational cost of the proposed modulation technique is very low and the technique can be applied to multilevel inverter with any number of levels.