A CD40194 CMOS Bidirectional Shift Register is wired as shown. Its operation is described by the provided table. Complete the timing diagram. For this problem the clock frequency is so low, and hence the clock period is so long, that the delay between the active clock edge and the new output is negligible on the time-scale of this diagram.

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Mode (Control							1
S_0	S_1	Q_0^+	$\boldsymbol{Q_1^+}$	$oldsymbol{Q}_2^+$	Q_3^+			
0	0	Q_0	Q_1	Q_2	Q_3			SI_R O_2 O_3 O_2 O_3
0	1	Q_1	Q_2	Q_3	SI_L			$ \longrightarrow $
1	0	SI_R	Q_0	Q_1	Q_2			S_1 CD40194 Clr 0-1
1	1	D_0	D_1	D_2	D_3			$S_0 \longrightarrow D_0 D_1 D_2 D_3 \longrightarrow Ck$
								$\begin{bmatrix} 1 \\ 1 \end{bmatrix} \begin{bmatrix} 1 \\ 0 \end{bmatrix} \begin{bmatrix} 1 \\ 1 \end{bmatrix}$
a, 1		ЩЦ		ЦШ				
$Ck 0_{-}$		╎ ┞╇╇	-		╇╇┩┤┼		┍╇╇┩┼┼┞╇╇╃╏┤┥	> t
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$S_0 \stackrel{1}{0}_{-}$	- + + - -	╎ ┞╟┩	╁┟┟┤┤	╌┼├├┤┤	├ ├ ┤ ┼	- + - + + + + + + + +		
c 1		<mark>╻</mark> ╏╏╏	 	$\downarrow\downarrow\downarrow\downarrow\downarrow\downarrow$	\downarrow \downarrow \downarrow \downarrow \downarrow			
$S_1 \stackrel{1}{0}_{-}$	- + + - -					╃╃╃╃╇╇╇╇╇ ╃	╶├├┤┥┼┼├┤┥┼├┤┥	++ - +++ - ++++++++++++++++++++++++++
$\rho_{\rm s}^{1}$	╌┼├├╁┿	\Box		++++	┝ ┾┼╅┤├	4+4+4+	╌┝┝┤┥╁┾┝┤┥╁╏┼┼	┥ ┡ ┩┩╇┡ ┩╃╄┾╃╇╄╌╌╴
$Q_0 Q_{-}$	+++	╅┾┝┨┪	╅┾┝┤┪┪	·╁┞┨┪┪	┞ ┝├ ┞ ┿┿	╶ ╀╄ ┡ ╃╃╇╄╄╃╇	┾┝ ┼╃╇╄ ╏ ╒╏┥	++ - +++ - +++ - +++-> t
q_{10}^{1}	- + + - -	╁╁┝╏┥	╁┾┾┽┥	┿┼┼┼	╒╞ ╬┽┼	┷╅┝╟┥┥╁┝╟┥╁	·┡┠╣ ┇╃╃╇╇╇╇	╶ ┼┼╁┤┼┞ ┤┼┞ ┤┼┞ ┤┼┞╴╴╴
¢10	┿┾┼	╿	╃┾┝┤┥┥	·┾┝┤┥┽	 	┤ <mark>╇╞╞╡╡╇┾┾┼┽</mark>	┿┿╇╫┼┼┼┼	
$Q_{2}^{1}_{0}$	- + + - -	╁╁┝╏┪	╅┾┝┤┥┪	·├ <mark>┝</mark> ┽╪┿╴	┝┝ ┼┽┼	╃╅╂╃╃ ╋	╼┾┼┽╪┼┼┽┼╁┞╎┤	╎╃╫┡╎┩╃╫┡ ╎┩╃╫┝┝
020	┿┼┼	┞ ╞┼┼┼	 	┿╇┤┥┤	 	+++	┾┝ ┤┥┼┝┤┥┼┡┿┽	
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