A CD40194 CMOS Bidirectional Shift Register is wired as shown. Its operation is described by the provided table. Complete the timing diagram.

For this problem the clock frequency is so low, and hence the clock period is so long, that the delay between the active clock edge and the new output is negligible on the time-scale of this diagram.

Mode Control S_0	S_1	Q_0^+	Q_1^+	Q_2^+	Q_3^+
0	0	Q_0	Q_1	Q_2	Q_3
0	1	Q_1	Q_2	Q_3	SI_L
1	0	SI_R	Q_0	Q_1	Q_2
1	1	D_0	D_1	D_2	D_3