ECE 5560 Spring 2025

HW 1

Reading:

Section 1.1-1.2.3, 1.2.9, 1.4-1.4.3, Section 2.1-2.3, 2.4.1

Problems:

1) Assume we have a FIR filter described by

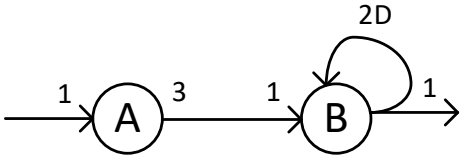
$$y(n) = ax(n) + bx(n-2) + cx(n-3)$$

   a) Draw a block diagram of the data-broadcast-format implementation of this filter. What is the critical path of this implementation architecture?

   b) Draw the corresponding signal flow graph (SFG).

   c) Apply the transposition technique on the SFG, and draw the block diagram corresponding to the transposed SFG. What is the critical path of resulted architecture?

2) Draw the single-rate DFG corresponding to the following multi-rate DFG.



3) Compute the iteration bound of the DFG in Fig. 2.12 in the text book (page 58).

4) Compute the iteration bound of the DFG in Fig. 2.14 in the text book (page 59) assuming a multiplication takes 2 u.t. to compute and an addition takes 1 u.t. to compute.

5) Consider the following compound loop. Assume that the computation time of loop l1 and l2 are P1 and P2, respectively. The numbers of delay elements in these loops are D1 and D2. Prove that the loop bound of the compound loop l1+l2 does not exceed $T_\infty = \max\{\frac{P1}{D1}, \frac{P2}{D2}\}$.