



THE OHIO STATE UNIVERSITY

COLLEGE OF ENGINEERING

ECE 3561

Advanced Digital Design

Class 11: Counters 2 – Other Sequences Counter Design

Drew Phillips

Spring 2024



Counter Design Procedure Summary

- 1) Determine counting sequence.
- 2) Determine number (and type) of FFs.
- 3) Construct truth table with state and next state combinations.
- 4) Determine FF input excitations for each state to next state transition and add to truth table.
- 5) Determine FF input excitation equations using K-map.
- 6) Draw the counter circuit logic diagram using the FFs and the combinational logic from the excitation equations.



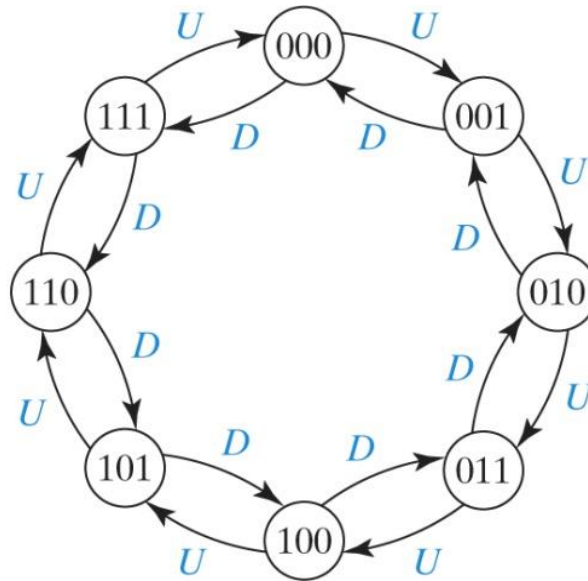
Ex 3: Up-Down Modulo-8 Counter

FIGURE 12-18

Transition Graph
and Table for
Up-Down
Counter

© Cengage Learning 2014

U: counting up
D: counting down



CBA	$C^+B^+A^+$	
	U	D
000	001	111
001	010	000
010	011	001
011	100	010
100	101	011
101	110	100
110	111	101
111	000	110

$$D_A = A^+ = A \oplus 1 = A'$$

(A changes state every clock cycle)

$$D_B = B^+ = B \oplus A'$$

(B changes state when A = 0)

$$D_C = C^+ = C \oplus B'A'$$

(C changes state when B = A = 0)

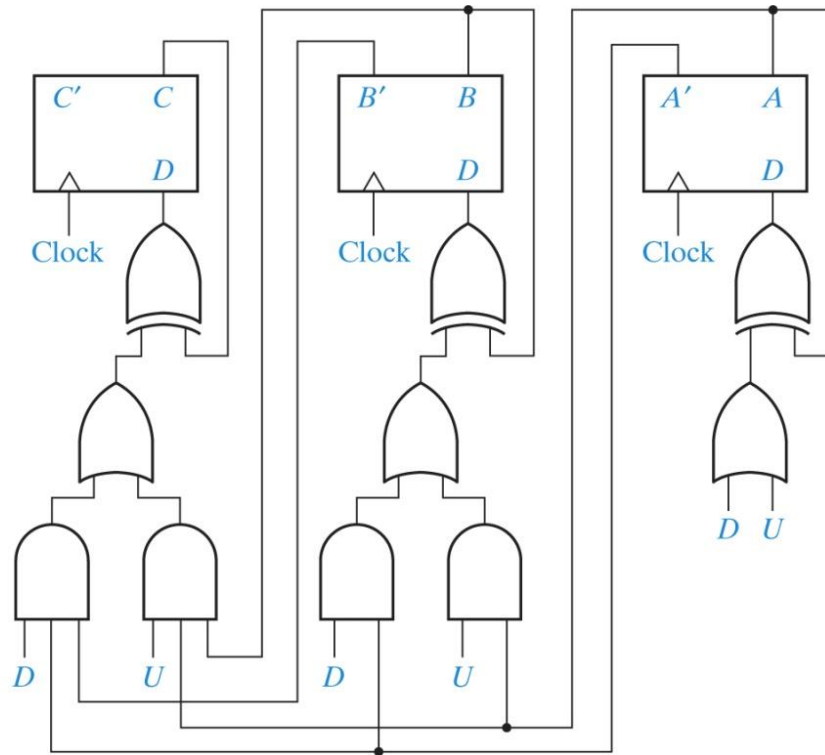
Observe when counting down:

Ex 3: Up-Down Modulo-8 Counter

FIGURE 12-19

Binary Up-Down Counter

© Cengage Learning 2014



Note that now we only transition states when U or D is set.

$$\begin{aligned} D_A &= A^+ = A \oplus (U + D) \\ D_B &= B^+ = B \oplus (UA + DA') \\ D_C &= C^+ = C \oplus (UBA + DB'A') \end{aligned}$$



Ex 4: Other Sequence Counter

- Count sequence:

$0 \rightarrow 4 \rightarrow 7 \rightarrow 2 \rightarrow 3 \rightarrow 0 \rightarrow \dots$

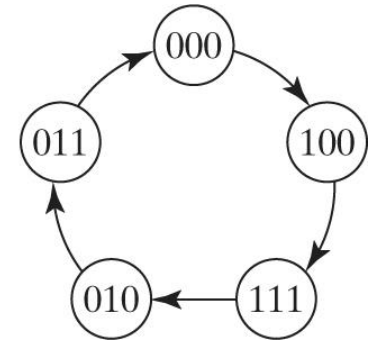
- Not used:

1, 5, 6: these states don't have next states (they are "don't cares")

FIGURE 12-22

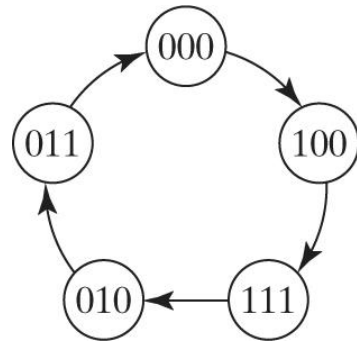
Transition Graph
for Counter

© Cengage Learning 2014





Ex 4: Other Sequence Counter



Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

$$T = Q^+ \oplus Q$$

C	B	A	C^+	B^+	A^+			
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						



Ex 4: Other Sequence Counter



Ex 4: Other Sequence Counter



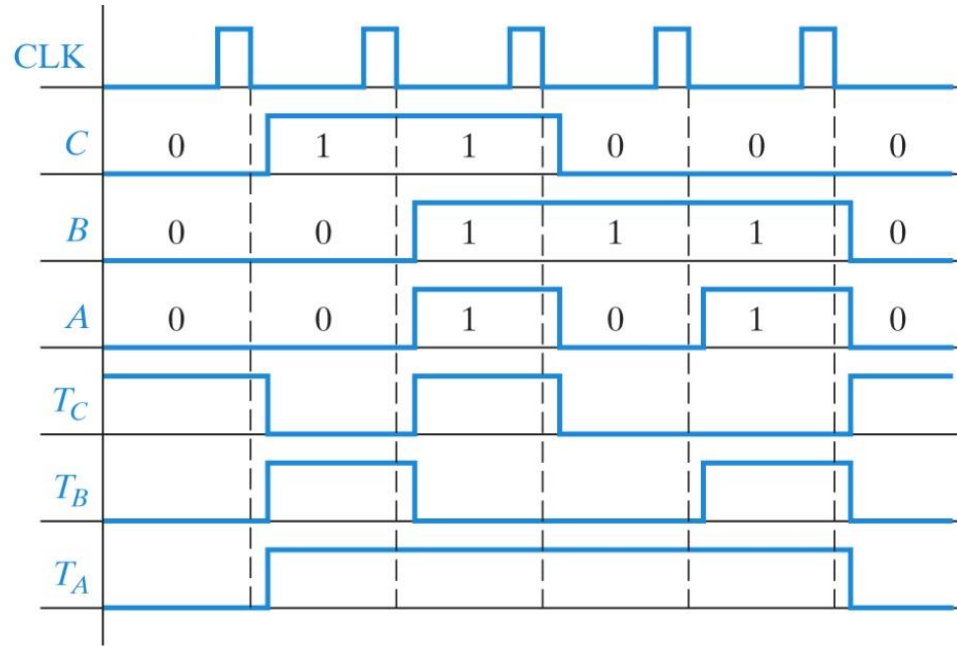
Ex 4: Other Sequence Counter

- Could you design the counter if you were given only the timing diagram?

FIGURE 12-25
Timing Diagram
for Figure 12-24

© Cengage Learning 2014

The complete timing diagram shows the counting sequence and the FF excitation signals.





Counter Design with SR/JK FFs

TABLE 12-7

J-K Flip-Flop
Inputs

© Cengage Learning 2014

(a)

J	K	Q	Q ⁺
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(b)

Q	Q ⁺	J	K
0	0	{ 0 0	
		{ 0 1	
0	1	{ 1 0	
		{ 1 1	
1	0	{ 0 1	
		{ 1 1	
1	1	{ 0 0	
		{ 1 0	

(c)

Q	Q ⁺	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



Compare
Excitation
Signals




TABLE 12-5

S-R Flip-Flop
Inputs

© Cengage Learning 2014

(a)

S	R	Q	Q ⁺
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	—
1	1	1	—

— inputs not allowed
— allowed

(b)

Q	Q ⁺	S	R
0	0	{ 0 0	
		{ 0 1	
0	1	1	0
1	0	0	1
1	1	{ 0 0	
		{ 1 0	



(c)

Q	Q ⁺	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0



Ex 5/6: Redesign with SR/JK FFs

Counter sequence: $0 \rightarrow 4 \rightarrow 7 \rightarrow 2 \rightarrow 3 \rightarrow 0 \rightarrow \dots$

C	B	A	C ⁺	B ⁺	A ⁺	S _C	R _C	S _B	R _B	S _A	R _A	C	B	A	C ⁺	B ⁺	A ⁺	J _C	K _C	J _B	K _B	J _A	K _A
0	0	0	1	0	0							0	0	0	1	0	0						
0	0	1	—	—	—							0	0	1	—	—	—						
0	1	0	0	1	1							0	1	0	0	1	1						
0	1	1	0	0	0							0	1	1	0	0	0						
1	0	0	1	1	1							1	0	0	1	1	1						
1	0	1	—	—	—							1	0	1	—	—	—						
1	1	0	—	—	—							1	1	0	—	—	—						
1	1	1	0	1	0							1	1	1	0	1	0						



Ex 5/6: Redesign with SR/JK FFs



Ex 5/6: Redesign with SR/JK FFs



Counter Design Procedure Summary

- 1) Determine counting sequence.
- 2) Determine number (and type) of FFs.
- 3) Construct truth table with state and next state combinations.
- 4) Determine FF input excitations for each state to next state transition and add to truth table.
- 5) Determine FF input excitation equations using K-map.
- 6) Draw the counter circuit logic diagram using the FFs and the combinational logic from the excitation equations.