Project 1

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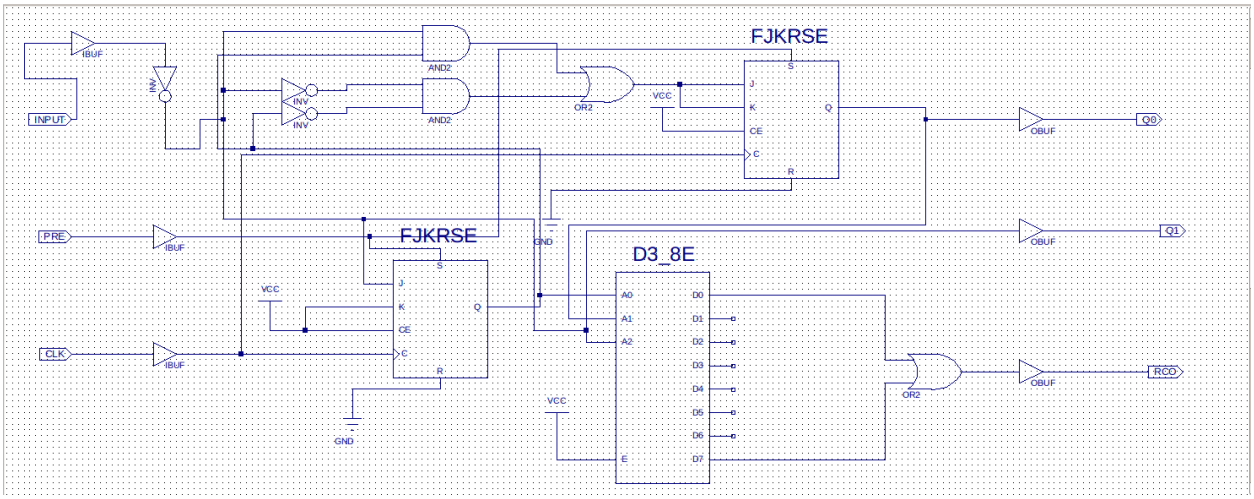
Solutions

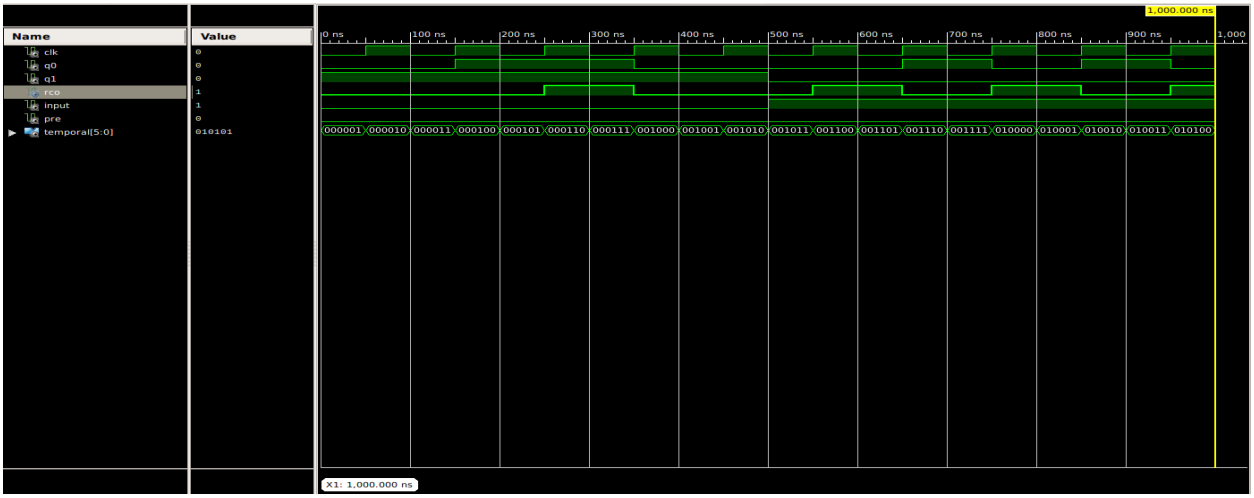
Problem 1

Based on the timing chart above, the circuit appears to be a pulse width extender with toggle using INPUT, and Q0 as the output pulse. PRE acts as a reset input, and when PRE = 1, it sets Q0 and Q1 to 1 as well. RCO appears to act as an XNOR of Q0 and Q1, only outputting 1 when they are the same.

Problem 2

The following graphs were based off of the interpretation that “reverse” operation meant that the inputs would be inverted. The following adjustment did solve this problem.

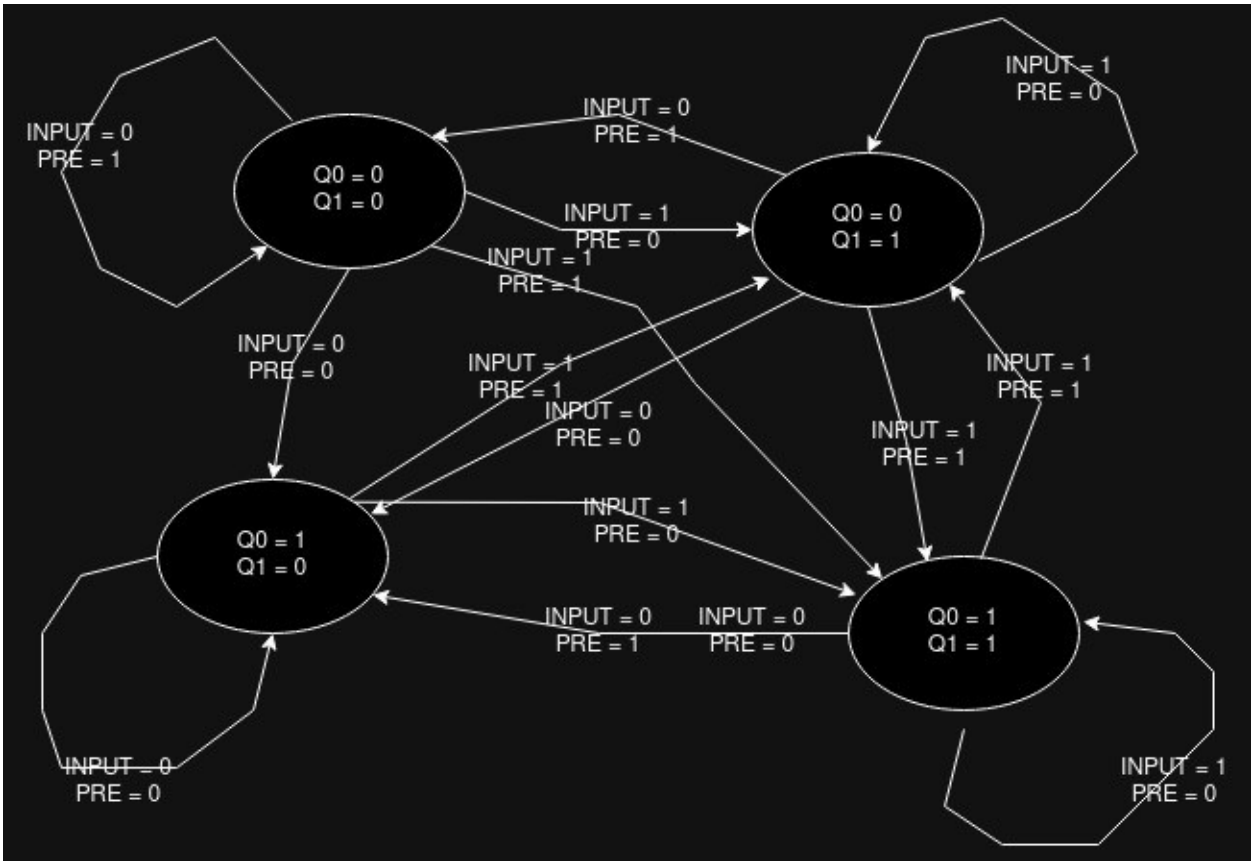




Problem 3

This is a Mealy machine since the INPUT signal runs directly into the output Q1. We do not need to know current states in order to know the value of Q1. Attached below are the State Table and State Diagram.

INPUT	PRE	J2	S2	Q2	AND1	AND2	OR1	S3	Q0	Q1
0	0	0	0	0	0	1	1	1	1	0
0	1	0	1	1	0	0	0	0	Stay	0
1	0	1	0	Toggle	0	0	0	0	Stay	1
1	1	1	1	1	1	0	1	0	Toggle	1



Problem 4

The maximum clock frequency of the circuit according to the timing report is 100MHz. Attached below is the timing report.

Timing Report

Need help reading this report?

Design Name	top
Device, Speed (SpeedFile Version)	XC9536, -5 (3.0)
Date Created	Sat Feb 24 17:17:39 2024
Created By	Timing Report Generator: version P.20131013
Copyright	Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

Summary

Notes and Warnings
Note: This design contains no timing constraints.
Note: A default set of constraints using a delay of 0.000ns will be used for analysis.

Performance Summary	
Min. Clock Period	10.000 ns.
Max. Clock Frequency (fSYSTEM)	100.000 MHz.
Limited by Cycle Time for CLK	
Clock to Setup (tCYC)	10.000 ns.
Pad to Pad Delay (tPD)	8.500 ns.
Setup to Clock at the Pad (tSU)	3.500 ns.
Clock Pad to Output Pad Delay (tCO)	15.000 ns.

Timing Constraints