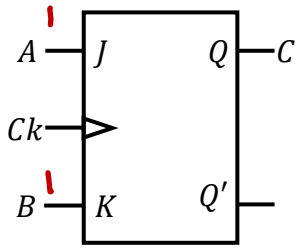
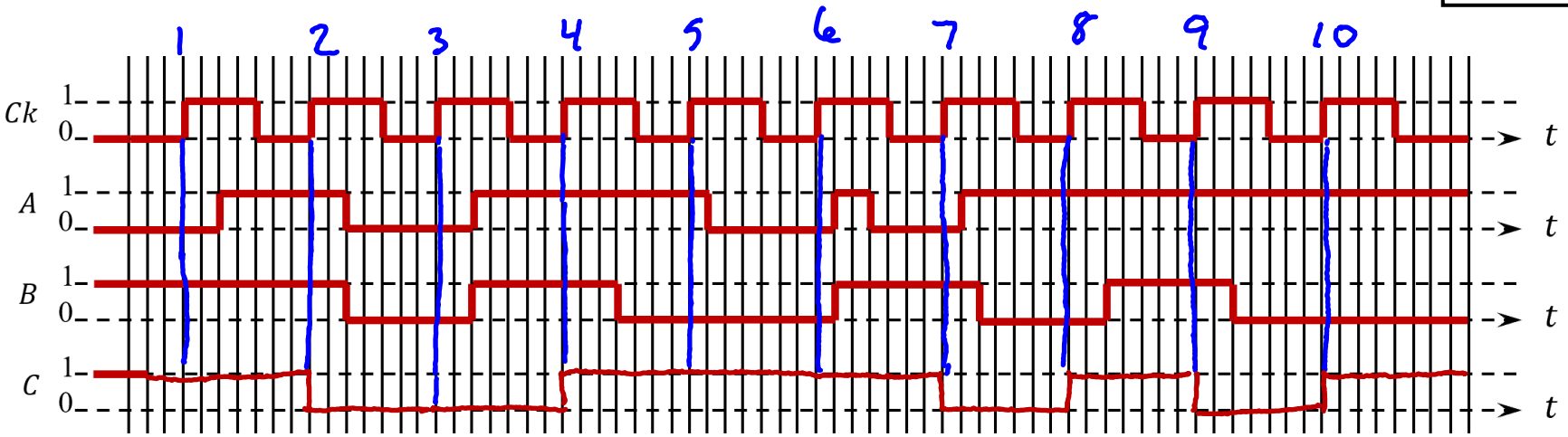
Complete the timing diagram below for the adjacent flip-flop.

For this problem the clock frequency is so low, and hence the clock period is so long, that the delay between the active clock edge and the new flip-flop output is negligible on the time-scale of this diagram.

The thick bar on the left of the timing diagram shows the starting state of the flip-flop.





$Q^+ = AQ' + B'Q$

	Ck	A	A'	B	B'	Q	Q'	C (Q+)
1		0	1	1	0	1	0	1
2		1	0	1	0	1	0	0
3		0	1	0	1	0	1	0
4		1	0	1	0	0	1	1
5		1	0	0	1	1	0	1
6		0	1	0	1	1	0	1
7		0	1	1	0	1	0	0
8		1	0	0	1	0	1	1
9		1	0	1	0	1	0	0
10		1	0	0	1	0	1	1