

ECE 5362 Homework 5

Due 10:20am Oct 16 (Carmen PDF Submission)

1. (80 pts) Implement three additional instructions for the Example Control Unit (Simplified OSIAC 5362). Start with the state machine we did in class, where we have already implemented three instructions for the control unit: **ADD addr**, **Add (X)**, and **JMP addr**. You are to:
 - a. (40 pts) modify the microinstructions that we have discussed in the class by adding three new instructions (see below). *Please add them one by one in the given order for the ease of grading.* Do not change the sequence of the existing microinstructions given in class. Just add conditional branches if necessary. Give a complete (updated) list of microinstructions with state #, control lines, and next state. Note that you should *try to minimize the # of new microinstructions* you use and add any new microinstructions to the end of the existing implementation, just like we did in the class for **Add (X)** and **JMP addr**. You do NOT need to worry about the CVZN condition codes for this homework.
 - b. (40 pts) modify the logic equations given in the class for the encoder circuitry, and give complete, updated list of equations for the following control lines: IPC, OPC, IMAR, IMDR, OMDR, Read, Write, Inhibit, IIR, IA, IB, P1, IT1, IQ, OQ, OX, IAC, OAC. No need to plot any circuit. Also give the updated equations for the state counter control lines: Preset, D4 (the control step counter now has 5 bits), D3, D2, D1, and D0. Please simplify D4, D3, D2, D1, and D0 as much as you can.

The additional instructions are:

| Instruction | Opcode(IR ₁₅₋₁₂) | # of Words | Register Transfer |
|-----------------|------------------------------|------------|------------------------|
| INC addr | 0100 | 2 | [addr] +1 → addr |
| INC (X) | 0101 | 1 | [X] → EA; [EA] +1 → EA |
| INC X | 0110 | 1 | [X] +1 → X |

2. (20 pts) Microprogrammed control can be used for the Example Control Unit, which was discussed in the class. The format for the microinstructions is given as follows:

| F1 | F2 | F3 | F4 | F5 | |
|---------------|------------------|------------------|---------------|-------------------|-----|
| F1 (2 bits) | F2 (3 bits) | F3 (3 bits) | F4 (2 bits) | F5 (bag: 1 bit) | |
| 00: No action | 000: No transfer | 000: No transfer | 00: No action | 0: Do not use BAG | |
| 01: IMAR | 001: IPC | 001: OPC | 01: Read | 1: Use BAG | |
| 10: IMDR | 010: IAC | 010: OAC | 10: Write | | |
| 11: IT1 | 011: IX | 011: OX | | | |
| | 100: ISP | 100: OSP | | | |
| | 101: IIR | 101: OT1 | | | |
| | 110: IQ | 110: OQ | | | |
| | | 111: OMDR | | | |
| F6 | F7 | F8 | F9 | F10 | F11 |

P1 (1 bit) COMP (1 bit) IA (1 bit) IB (1 bit) IN/IZ (1 bit) IC/IV (1 bit)

Assume that a Read or Write to memory only take one clock cycle such that Inhibit is not needed. Also, simply set the IN/IZ (F10) and IC/IV (F11) bits as 0 for this homework.

Give the contents of the microprogramming memory (control store) for all the microinstructions from Problem 1 (designed for the six instructions). Note that the content of location 0 is already given below.

[illegible]