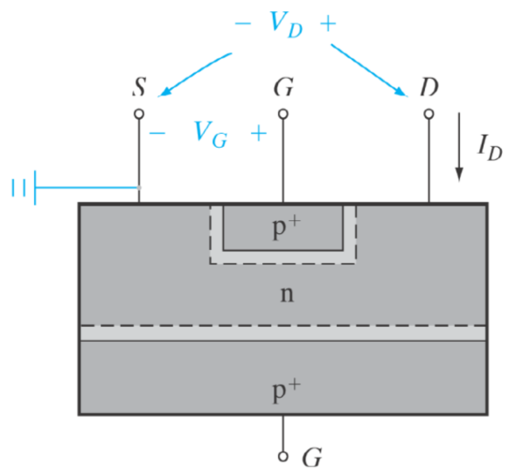
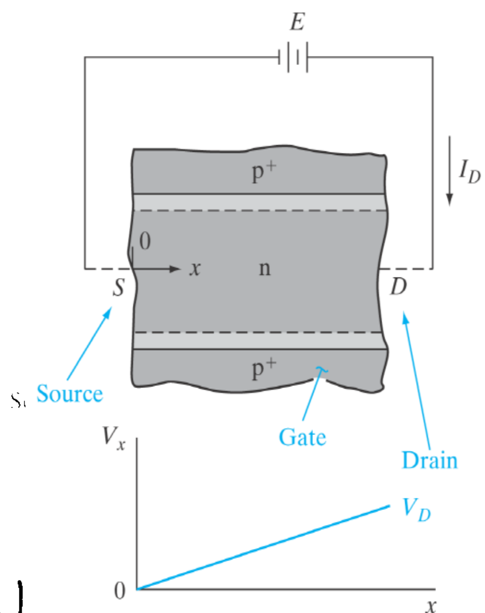
Three-Terminal Devices:

- Field Effect Transistors (FET)
- Bipolar Junction Transistor (BJT)

FET: Voltage-controlled, unipolar (majority carrier)

BJT: Current-controlled, bipolar (majority and minority carrier)





Electrons injected into source, flow through channel, collected at drain.

Potential varies with position in lightly-doped channel: Distributed resistor

Several FET types:

JFET : Junction FET → Gate controls depletion width of reverse-biased junction

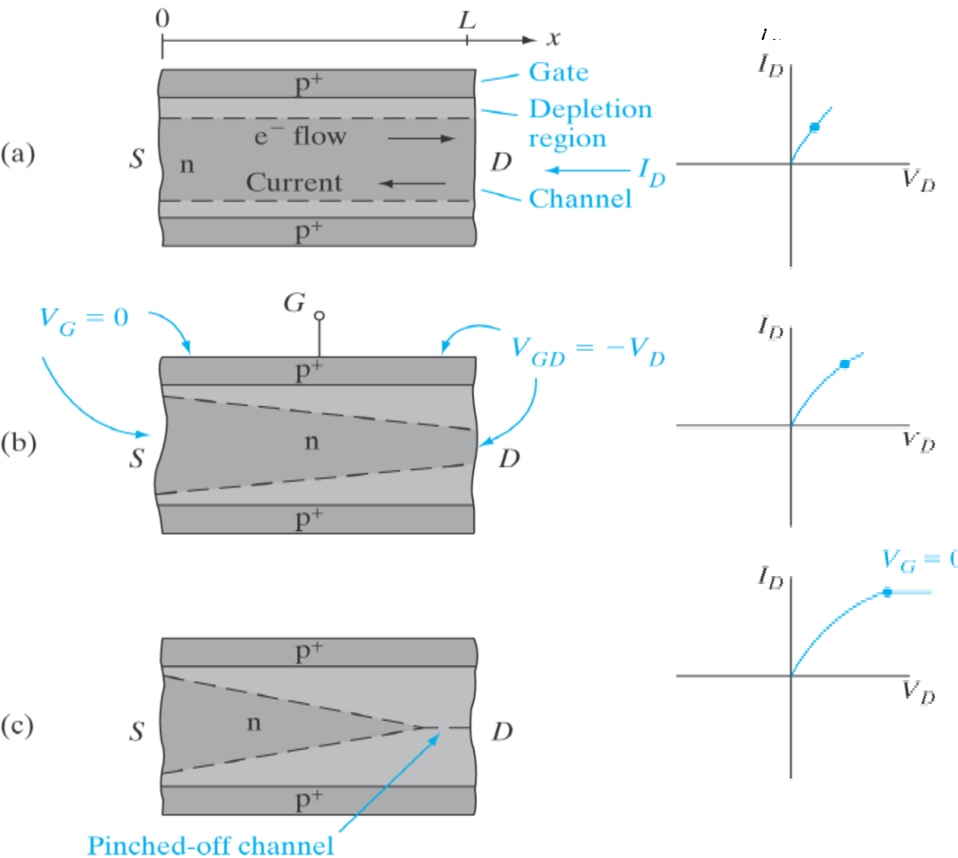
MESFET : Metal-Semiconductor FET : Schottky barrier replaces junction

MISFET : Metal-Insulator-Semiconductor FET

MOSFET : " -oxide- " "

FET Advantage: High impedance in reverse bias → Lower power and higher packing density

How does it work? Apply bias to drain or gate to "pinch off" channel



Low current: Changes in depletion widths are small
→ I-V curve is ~ linear

Higher current: Gate voltage tied to Source. Reverse bias and depletion widths increase with x
→ Increased resistance

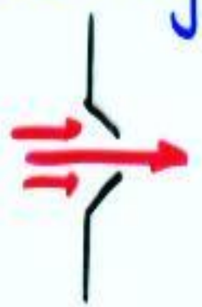
Current beyond "Pinch-off": Depletion widths meet. Channel "pinched" off.

→ Current I_D can't increase as V_D is increased further.

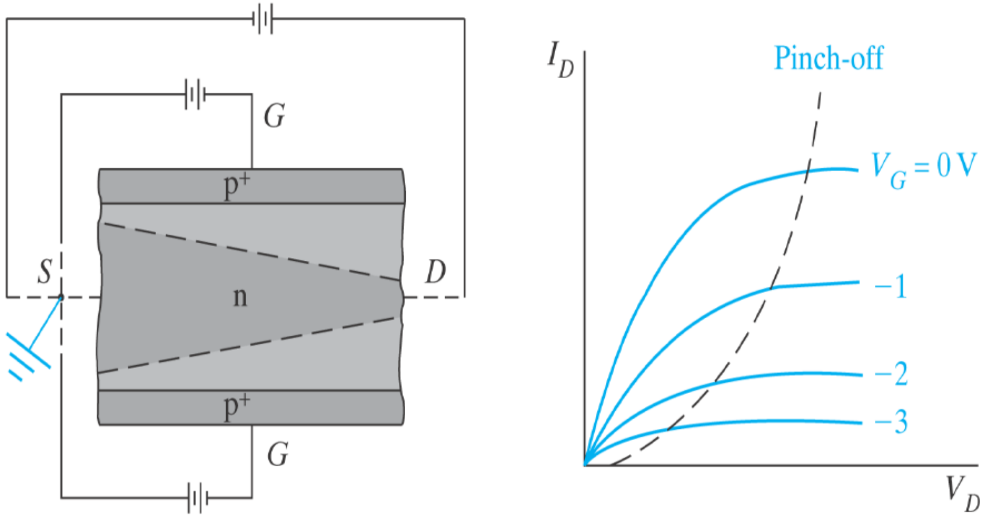
$\frac{dV_D}{dI_D}$ → very big differential resistance

FET Gate Control

"Gate" controls current flow by applying a voltage to widen or constrict a channel.



"Field Effect"



(a) (b)

Family of current-voltage curves for the channels as V_G is varied.

Negative gate bias: V_G increases resistance of channel (more reverse bias)

→ induces

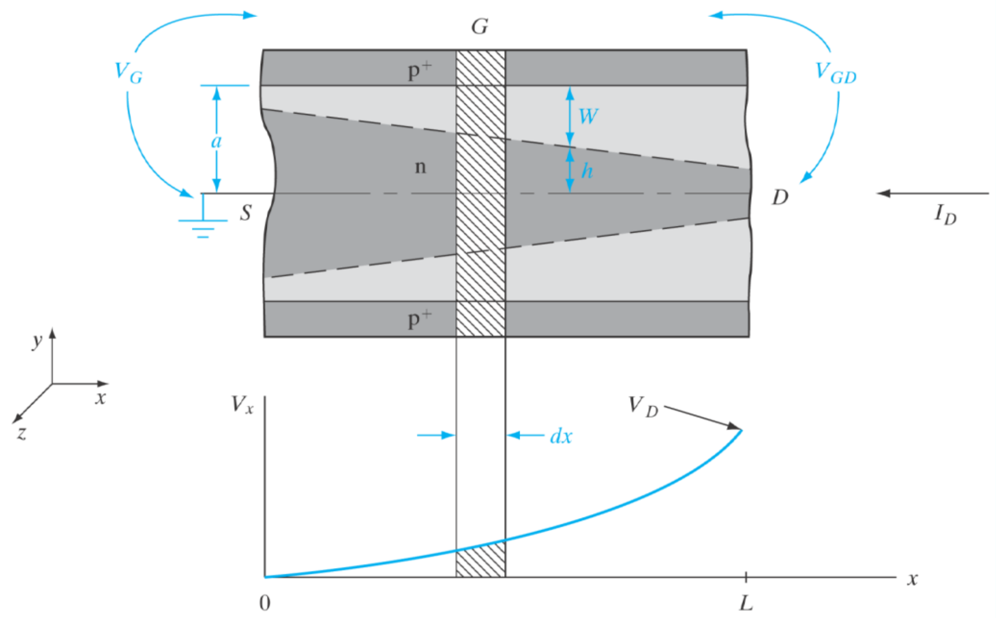
Beyond "pinch-off" voltage, I_D constant with increasing V_D, but controlled by V_G.

Vary V_G →

V_G across reverse bias → high input impedance

Pinch-off Voltage: Calculate reverse bias between n-channel and p^+ gate at drain end of channel

$V_{reverse} = -V_{GD}$ between gate and drain



$$W = \left[\frac{2\epsilon(-V_{GD})}{q\,N_d}\right]^{1/2} \quad \text{at } x = L$$

V_{GD} is negative
(here assume $V_{GD} \gg V_0$ and and $x_p \ll x_n$)

Pinch-off occurs at drain end when

$$h(x=L) = a - W(x=L) = 0$$

$$\left[\frac{2\epsilon V_p}{q N_d}\right]^{1/2} = \boxed{\quad} \quad \text{or} \quad V_p = \boxed{\quad}$$

pinch-off voltage

$$V_p = -V_{GD}(\text{pinch-off}) = -V_G + V_D$$

Lower V_D needed for pinch off when negative V_G applied.

Calculate FET current versus Voltage:

Differential volume of neutral channel

$$= Z \cdot 2h(x) \cdot dx$$

so resistance of volume element R =

channel width

$$dV_x = I_D R = I_D \frac{\rho\, dx}{Z 2h(x)}$$

$$I_D = \frac{Z \cdot 2h(x)}{\rho} \frac{dV_x}{dx}$$

$$h(x) = a - W(x) = a - \left[\frac{2\epsilon(-V_{Gx})}{qN_d}\right]^{1/2} = a\left[1 - \left(\frac{V_x - V_G}{V_p}\right)^{1/2}\right]$$

where $V_{Gx} = V_G - V_x$ and $V_p = qa^2N_d/2\epsilon$

(assumes $h(x)$ doesn't change abruptly)

$$\frac{2Za}{\rho}\left[1-\left(\frac{V_x-V_G}{V_p}\right)^{1/2}\right]dV_x = I_D\,dx \quad \text{to get}$$

$$I_D = G_o V_p\left[\frac{V_D}{V_p}+\frac{2}{3}\left(-\frac{V_G}{V_p}\right)^{3/2}-\frac{2}{3}\left(\frac{V_D-V_G}{V_p}\right)^{3/2}\right]$$

where $G_o \equiv$ is conductance of channel for W negligible (far from pinch-off) and V_G negative

assume I_D (saturation) constant at pinchoff

so $V_D - V_G = V_p$

Substituting into I_D at saturation,

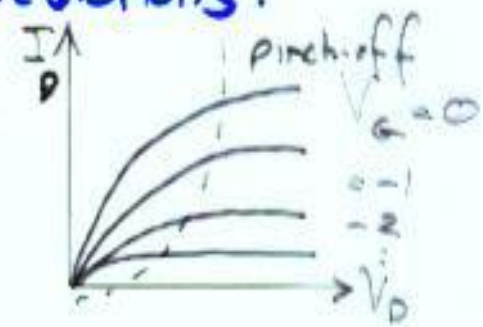
$$I_D(\text{sat.}) = G_o V_p \left[\frac{V_D}{V_p} + \frac{2}{3}\left(-\frac{V_G}{V_p}\right)^{3/2} - \frac{2}{3} \right]$$

$$I_D(\text{sat.}) = G_o V_p \left[\frac{V_G}{V_p} + \frac{2}{3}\left(-\frac{V_G}{V_p}\right)^{3/2} + \frac{1}{3} \right]$$

where $\dfrac{V_D}{V_p} = 1 + \dfrac{V_G}{V_p}$

This agrees with our qualitative predictions:

I_D decreases as V_G becomes more negative.



Represent device biased in saturation region by equivalent circuit where changes in I_D depend on V_G changes.

$$g_m(\text{sat.}) = \frac{\partial I_D(\text{sat.})}{\partial V_G} = G_o\left[1 - \left(-\frac{V_G}{V_P}\right)^{1/2}\right]$$

g_m is mutual transconductance (in A/V or siemens S or mhos)

g_m and g_m/Z are FET figures of merit

Drain current in saturation

$$\underline{I_D(\text{sat.}) \simeq I_{DSS}\left(1 + \frac{V_G}{V_P}\right)^2}$$ found experimentally

where $I_{DSS} = I_D$ for $V_G = 0$