

MOSFET Example:

What is maximum depletion width
for ideal MOS capacitor on p-type Si
doped with $N_A = 10^{15} \text{ cm}^{-3}$?

Solve for $\phi_F =$

$$= 0.0259 \text{ V} \ln \frac{10^{15}}{1.5 \times 10^{10}} = 0.0259 (8.80)$$

$$= \underline{0.23 \text{ V}}$$

$$\text{Solve for } W_m = 2 \sqrt{\frac{\epsilon_s \phi_F}{q N_a}}$$

$$\text{For Si, } \epsilon_s = K\epsilon_0 = 11.8 \times 8.85 \times 10^{-14} \text{ F/cm}$$

$$W_m = 2 \left[\frac{(11.8)(8.85 \times 10^{-14} \text{ F/cm})(0.23 \text{ V})}{(1.6 \times 10^{-19} \text{ C})(10^{15} \text{ cm}^{-3})} \right]^{1/2}$$

$$= \boxed{}$$

$$\approx \boxed{}$$

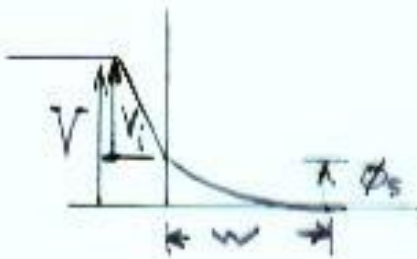
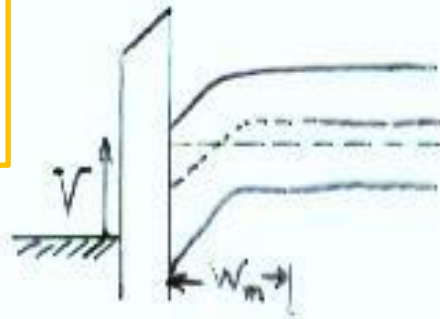
Lower doping increases W_m .

MOS Capacitance - Voltage

$$Q_d = -q N_a W_m =$$

$$V = V_i + \phi_s$$

$$V_T = -\frac{Q_s}{C_i} + \phi_s = -\frac{Q_d}{C_i} + 2\phi_F$$



Applied voltage must be high enough to create Q_d plus the surface potential ϕ_s (inverted).

V_T = minimum voltage to achieve strong inversion *



Very Important for MOS transistors

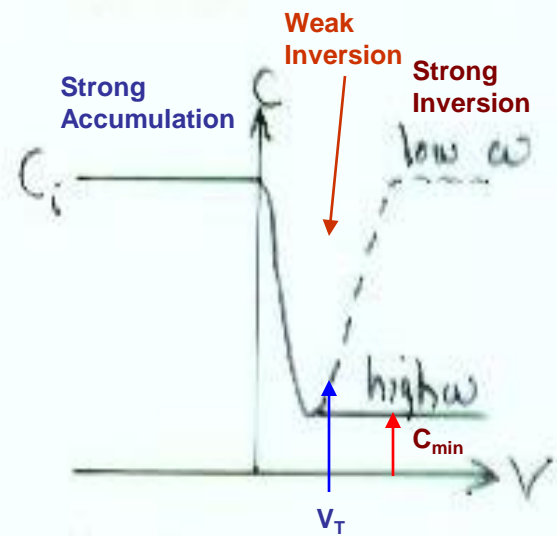
Capacitance-voltage depends on whether accumulation, depletion, or inversion.

*real case:
add $\phi_m - \phi_s$
term)

V negative: Accumulation — looks like parallel plate capacitor
 $C_i = \epsilon_i / d$ dominates.

V positive: Depletion — add depletion layer $C_d = \frac{\epsilon_s}{W}$
 in series with C_i

C_i  C_d  Total $C =$

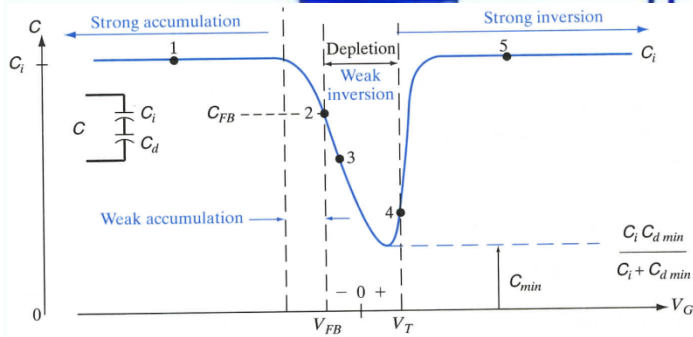


As W grows, C_d decreases $\rightarrow C$ decreases.

Beyond inversion, charge increases.

Becomes like parallel plate capacitor again, but with opposite charge.

Calculate major points on a C-V curve



$$\epsilon_i / \epsilon_0 = 3.9 \text{ for SiO}_2$$

$$d = 100 \text{ \AA} = 10^{-6} \text{ cm}; \quad N_a = 10^{15}$$

$$V_T = -\frac{Q_d}{C_i} + 2\phi_F$$

$$C_i = \frac{\epsilon_i}{d} = \frac{(3.9)(8.85 \times 10^{-14} \text{ F/cm})}{10^{-6} \text{ cm}} = \underline{3.45 \times 10^{-7} \text{ F/cm}^2}$$

$$Q_d = -q N_a W_m = -(1.6 \times 10^{-19} \text{ C})(10^{15} \text{ cm}^{-3})(0.387 \times 10^{-4} \text{ cm})$$

$$= -0.62 \times 10^{-8} \text{ C/cm}^2$$

$$V_T = \frac{0.62 \times 10^{-8} \text{ C/cm}^2}{3.45 \times 10^{-7} \text{ F/cm}^2} + 2(0.23 \text{ V}) = 0.478$$

0.018 V

at V_T :

$$C_d = \frac{\epsilon_s}{W_m} = \frac{(11.8)(8.85 \times 10^{-14} \text{ F/cm})}{(0.387 \times 10^{-4} \text{ cm})} = \underline{2.70 \times 10^{-8} \text{ F/cm}}$$

$$C_{\min} = \frac{C_i C_d}{C_i + C_d} = \frac{34.5 \times 2.70 \times 10^{-16}}{(34.5 + 2.70) \times 10^{-8}} = \underline{2.5 \times 10^{-8} \text{ F/cm}}$$

C_d is close to C_{\min} since C_d dominates total C as W grows with depletion

Note: Want low V_T so keep C_i large and d small.

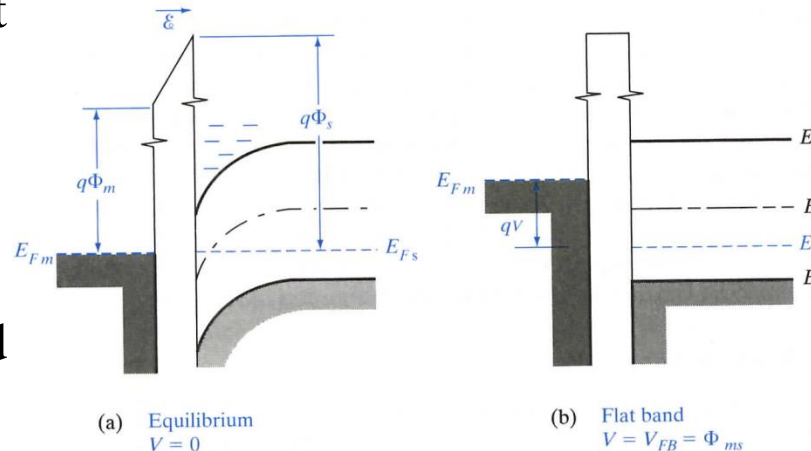
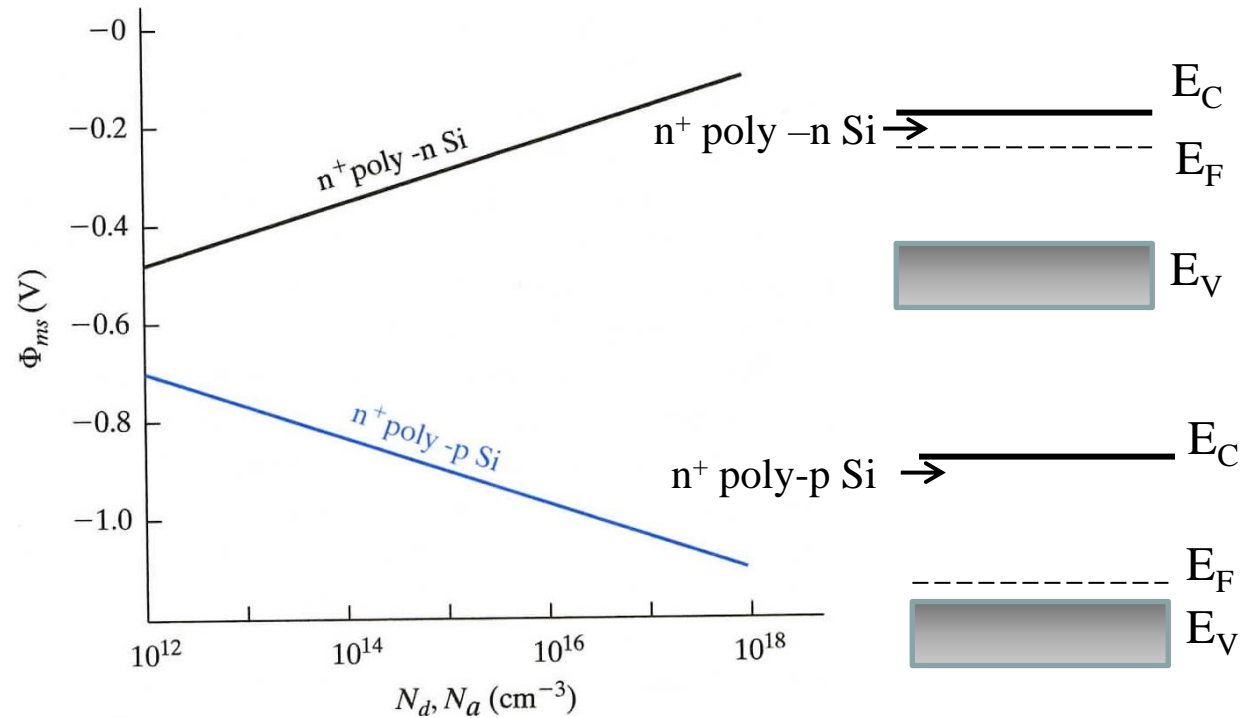
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Effect of Real Surfaces: Work Function Difference

Heavily doped n+ - poly acts as a metal electrode

Work function difference causes Si bands to bend without external bias voltage

Lower metal ϕ_m causes Si bands to bend down in order for E_{Fm} and E_{Fs} to align

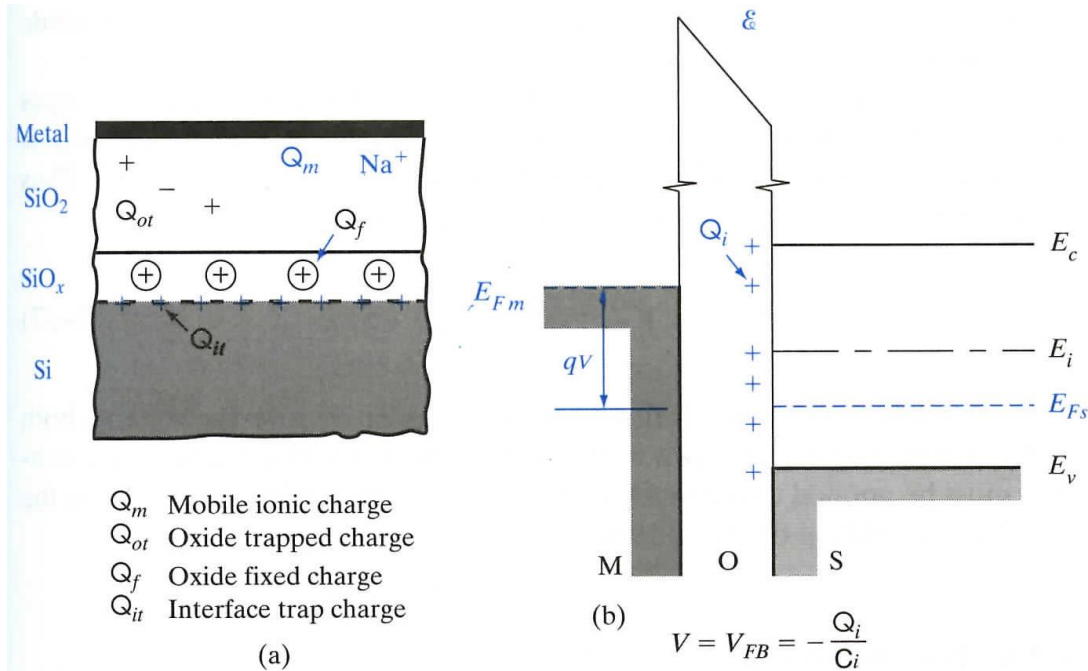


Just to reach flat bands requires negative applied voltage $V = V_{FB} = \Phi_{ms}$

Effect of Real Surfaces: Interface Charge

Trapped charge near MOS interface: (1) Traps inside SiO_2 , (2) Traps at SiO_2/Si or SiO_x/Si interface (dangling bonds), (3) Mobile ions (Na^+)
Can alter applied bias V_G ; Can vary with applied voltage, time, and temperature

Eliminating interface traps: a major focus of semiconductor industry



Positive interface trapped charge induces negative charges in semiconductor, requiring negative gate voltage to achieve flat band condition

Threshold Voltage

$$V_T = \Phi_{ms} - (Q_i/C_i) - (Q_d/C_i) + 2\phi_F$$

$$V_T = \left| \begin{array}{c|c|c|c} \Phi_{ms} & -\frac{Q_i}{C_i} & -\frac{Q_d}{C_i} & +2\phi_F \\ \hline (-) & (-) & \begin{array}{l} (+) \text{ n channel} \\ (-) \text{ p channel} \end{array} & \begin{array}{l} (+) \text{ n channel} \\ (-) \text{ p channel} \end{array} \end{array} \right|$$

$$(kT/q) \ln(N_a/n_i)$$

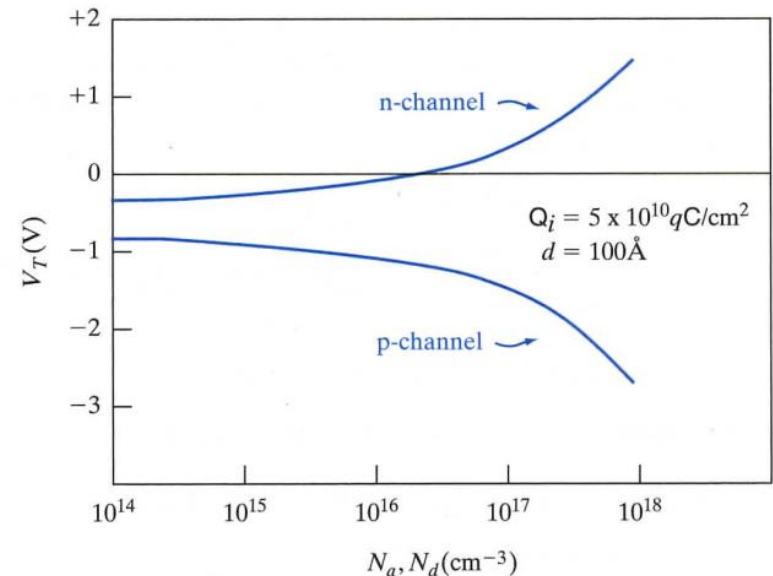
$$\Phi_m = \Phi(\text{poly-Si}) = \chi_{Si} + (E_C - E_F) \sim \chi_{Si}$$

$$\Phi_s = \Phi_{Si} = \chi_{Si} + E_G/2 + kT \ln(p_0/n_i)$$

$$(E_i - E_F)$$

Threshold voltage V_T depends on:

- Doping
- interface capacitance C_i ,
- interface charge Q_i ,



As substrate p-doping increases, Φ_s increases, $\Phi_m - \Phi_s$ decreases, and V_T decreases

As substrate n-doping increases, Φ_s decreases, $\Phi_m - \Phi_s$ increases, and V_T increases

'Real' Example: Threshold Voltage

n+ poly-Si gate on P-Si substrate with $N_a = 5 \times 10^{15} \text{ cm}^{-3}$
(n-channel MOS transistor) $d(\text{SiO}_2) = 100 \text{ \AA}$

$$Q_i = 4 \times 10^{10} \text{ qC/cm}^2$$

Find C_i and C_{\min} (C-V characteristics), W_m , V_{FB} and V_T

$$\phi_F = \frac{kT}{q} \ln \frac{N_a}{n_i} = 0.0259 \ln \frac{5 \times 10^{15}}{1.5 \times 10^{10}} = 0.329 \text{ V}$$

$$W_{\max} = \frac{2 \left[\frac{11.8 \times 8.85 \times 10^{-14} \times 0.329}{1.6 \times 10^{-19} \times 5 \times 10^{15}} \right]^{1/2}}$$

$$= \dots$$

From Fig. 6-17, $\Phi_{ms} \approx \dots$

$$Q_i = 4 \times 10^{10} \times 1.6 \times 10^{-19} = \dots$$

$$C_i = \frac{3.9 \times 8.85 \times 10^{-14}}{0.1 \times 10^{-5} \text{ cm}} = \dots$$

$$C_i = \frac{3.9 \times 8.85 \times 10^{-14}}{0.1 \times 10^{-5} \text{ cm}} =$$

$$V_{FB} = \boxed{} = -0.95 - 6.4 \times 10^{-9} / 3.45 \times 10^{-5}$$

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$$Q_d = -1.6 \times 10^{-19} \times 5 \times 10^{15} \times 4.15 \times 10^{-5}$$

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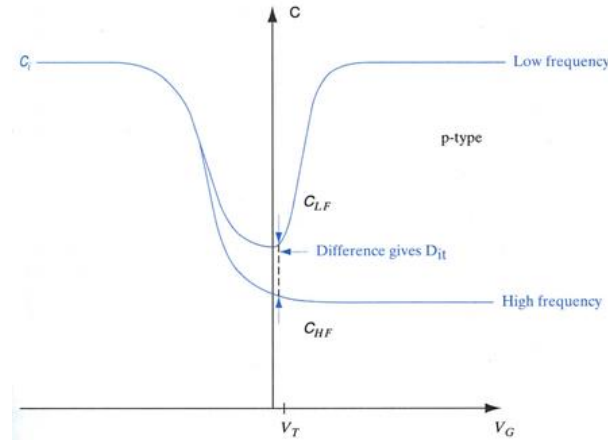
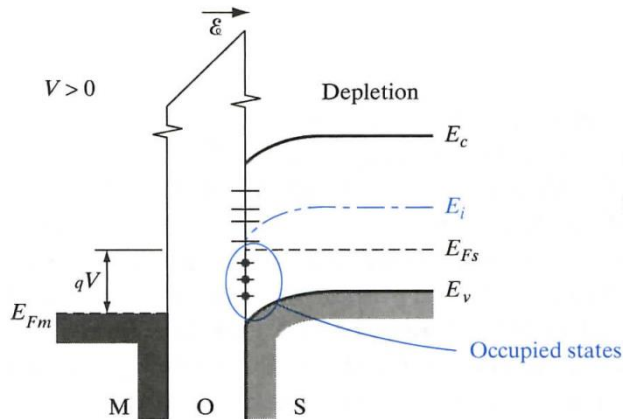
$$V_T = -0.969 + \frac{3.32 \times 10^{-8}}{3.45 \times 10^{-7}} + 0.658$$

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$$C_d = \frac{11.8 \times 8.85 \times 10^{-14}}{4.15 \times 10^{-5}} =$$

$$C_m = \frac{3.45 \times 10^{-7} \times 2.5 \times 10^{-8}}{3.45 \times 10^{-7} + 2.5 \times 10^{-8}} =$$

MOS C-V analysis: can measure insulator d, doping, and V_T from C-V plots



Substrate type:

P-type if $C(\text{hi-}\omega)$

large for $V_G < 0$ and
small for $V_G > 0$

Opposite for N-type

Detailed derivation shows:

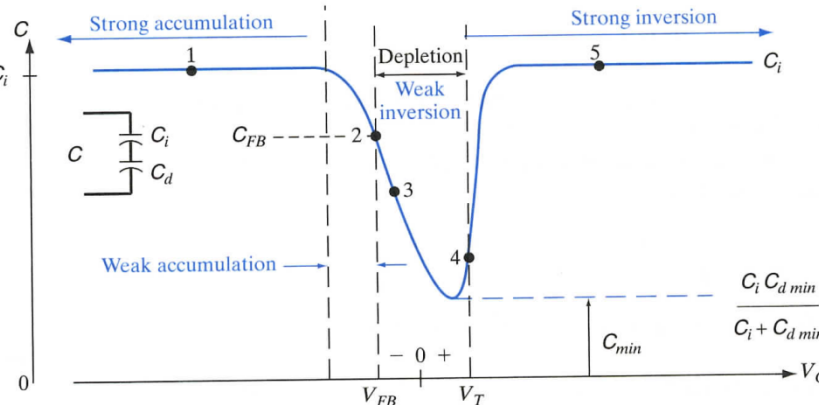
$$D_{it} = (1/q) [(C_i C_{LF}/C_i - C_{LF}) - (C_i C_{HF}/C_i - C_{HF})] \text{ cm}^{-2} \text{ eV}^{-1}$$

Get insulator d from:

$C_i = \epsilon_i/d$ in accumulation
or strong LF inversion
since know ϵ_i (SiO_2) =
 $3.9 \epsilon_0$

Get C_{dmin} from: LF C-V and

$$C_{min} = C_i C_{dmin} / (C_i + C_{dmin})$$



And finally:

$$V_T = \Phi_{ms} - (Q_i/C_i) - (Q_d/C_i) + 2 \phi_F$$

Can calculate what V_T should be from C-V plot

Get N_a from: $f(C_{dmin})$

(Streetman eq. 6-39),
which gives:

$$\phi_F = (kT/q) \ln(N_a/n_i)$$

$$Q_d = -2(\epsilon_s N_a \phi_F)$$

$$\Phi_s, \Phi_{ms}, L_D = \sqrt{(\epsilon_s (kT/q^2 p_0))}$$

$$\text{and } C_{debye} = \epsilon_s / L_D$$

Can show:

$$C_{FB} = (1/C_{debye}) + (1/C_i)$$

to get V_{FB} and Q_i from

$$V_{FB} = \Phi_{ms} - (Q_i/C_i)$$