the flip-flop be set to 1, and under what conditions must it be reset?" The flip-flop must be set to 1 if $Q = 0$ and $T = 1$.

Therefore, $S =$ _____. In a similar manner, determine the equation for $R$ and draw the circuit which converts an S-R flip-flop to a T flip-flop.

(c) Work Problem 11.10.

**10.** When you are satisfied that you can meet the objectives of this unit, take the readiness test.

# Latches and Flip-Flops

## 11.1 Introduction

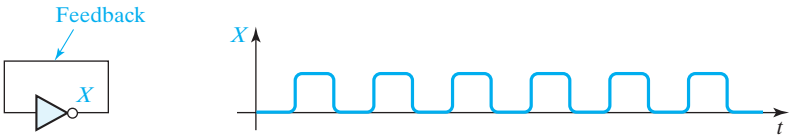
Sequential switching circuits have the property that the output depends not only on the present input but also on the past sequence of inputs. In effect, these circuits must be able to "remember" something about the past history of the inputs in order to produce the present output. Latches and flip-flops are commonly used memory devices in sequential circuits. Basically, latches and flip-flops are memory devices which can assume one of two stable output states and which have one or more inputs that can cause the output state to change. Several common types of latches and flip-flops are described in this unit.

In Units 12 through 16, we will discuss the analysis and design of synchronous digital systems. In such systems, it is common practice to synchronize the operation of all flip-flops by a common clock or pulse generator. Each of the flip-flops has a clock input, and the flip-flops can only change state in response to a clock pulse. The use of a clock to synchronize the operation of several flip-flops is illustrated in Units 12 and 13. A memory element that has no clock input is often called a latch, and we will follow this practice. We will then reserve the term flip-flop to describe a memory device that changes its output in response to a clock input and not in response to a data input.

The switching circuits that we have studied so far have not had feedback connections. By feedback we mean that the output of one of the gates is connected back into the input of another gate in the circuit so as to form a closed loop. In order to construct a switching circuit that has memory, such as a latch or flip-flop, we must introduce feedback into the circuit. For example, in the NOR-gate circuit of Figure 11-3(a), the output of the second NOR gate is fed back into the input of the first NOR gate. Sequential circuits must contain feedback, but not all circuits with feedback are sequential. There are a few circuits containing feedback that are combinational.

**FIGURE 11-1**






(a) Inverter with feedback (b) Oscillation at inverter output

In simple cases, we can analyze circuits with feedback by tracing signals through the circuit. For example, consider the circuit in Figure 11-1(a). If at some instant of time the inverter input is 0, this 0 will propagate through the inverter and cause the output to become 1 after the inverter delay. This 1 is fed back into the input, so after the propagation delay, the inverter output will become 0. When this 0 feeds back into the input, the output will again switch to l, and so forth. The inverter output will continue to oscillate back and forth between 0 and 1, as shown in Figure 11-1(b), and it will never reach a stable condition. An oscillator can be created using any odd number of inverters. The oscillator waveform has a high and a low time that is the sum of the propagation times of the inverters. For example, with $n$ inverters and with all having the same delay, the oscillator waveform high time is $(n + 1)/2$ times the high-to-low inverter propagation delay plus $(n - 1)/2$ times the low-to-high inverter propagation delay.

**FIGURE 11-2**




(a) (b)

Next, consider a feedback loop which has two inverters in it, as shown in Figure 11-2(a). In this case, the circuit has two stable conditions, often referred to as stable states. If the input to the first inverter is 0, its output will be 1. Then, the input to the second inverter will be 1, and its output will be 0. This 0 will feed back into the first inverter, but because this input is already 0, no changes will occur. The circuit is then in a stable state. As shown in Figure 11-2(b), a second stable state of the circuit occurs when the input to the first inverter is 1 and the input to the second inverter is 0. The simple loop of two inverters lacks any external means of initializing the state to one of the stable states. The set-reset latches in the next section have inputs for this initialization.

## 11.2 Set-Reset Latch

We can construct a simple latch by introducing feedback into a NOR-gate circuit, as seen in Figure 11-3(a). As indicated, if the inputs are $S = R = 0$, the circuit can assume a stable state with $Q = 0$ and $P = 1$. Note that this is a stable condition of the circuit because $P = 1$ feeds into the second gate forcing the output to be $Q = 0$, and $Q = 0$ feeds into the first gate allowing its output to be 1. Now if we change $S$ to 1, $P$ will become 0. This is an unstable condition or state of the circuit because both the inputs and output of the second gate are 0; therefore $Q$ will change to 1, leading to the stable state shown in Figure 11-3(b).

**FIGURE 11-3**



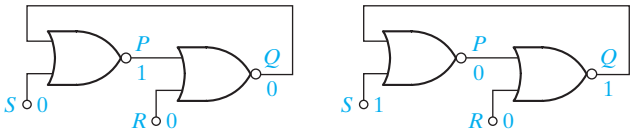
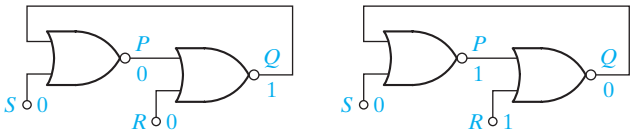



**FIGURE 11-4**






If $S$ is changed back to 0, the circuit will not change state because $Q = 1$ feeds back into the first gate, causing $P$ to remain 0, as shown in Figure 11-4(a). Note that the inputs are again $S = R = 0$, but the outputs are different than those with which we started. Thus, the circuit has two different stable states for a given set of inputs. If we now change $R$ to 1, $Q$ will become 0 and $P$ will then change back to 1, as seen in Figure 11-4(b). If we then change $R$ back to 0, the circuit remains in this state and we are back where we started.

This circuit is said to have memory because its output depends not only on the present inputs, but also on the past sequence of inputs. If we restrict the inputs so that $R = S = 1$ is not allowed, the stable states of the outputs $P$ and $Q$ are always complements, that is, $P = Q'$. To emphasize the symmetry between the operation of the two gates, the circuit is often drawn in *cross-coupled* form (see Figure 11-5(a)). As shown in Figures 11-3(b) and 11-4(b), an input $S = 1$ *sets* the output to $Q = 1$, and an input $R = 1$ *resets* the output to $Q = 0$. When used with the restriction that $R$ and $S$ cannot be 1 simultaneously, the circuit is commonly referred to as a set-reset ($S$-$R$) latch and given the symbol shown in Figure 11-5(b). Note that although $Q$ comes out of the NOR gate with the $R$ input, the standard S-R latch symbol has $Q$ directly above the $S$ input.

If $S = R = 1$, the latch will not operate properly, as shown in Figure 11-6. The notation $1 \rightarrow 0$ means that the input is originally 1 and then changes to 0. Note that when $S$ and $R$ are both 1, $P$ and $Q$ are both 0. Therefore, $P$ is not equal to $Q'$, and this violates a basic rule of latch operation that requires the latch outputs to be complements. Furthermore, if $S$ and $R$ are simultaneously changed back to 0, $P$ and $Q$ may both change to 1. If $S = R = 0$ and $P = Q = 1$, then after the 1's propagate through the gates, $P$ and $Q$ will become 0 again, and the latch may continue to oscillate if the gate delays are equal.

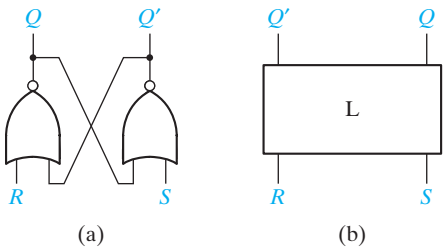



**FIGURE 11-5**
S-R Latch



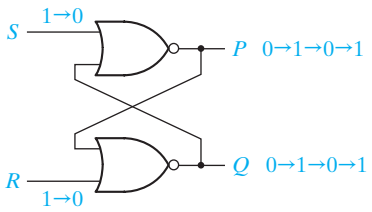



**FIGURE 11-6**
Improper S-R Latch Operation



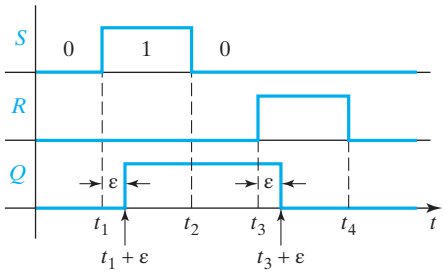



**FIGURE 11-7**
Timing Diagram for S-R Latch



Figure 11-7 shows a timing diagram for the S-R latch. Note that when $S$ changes to 1 at time $t_1$, $Q$ changes to 1 a short time ($\varepsilon$) later. ($\varepsilon$ represents the response time or delay time of the latch.) At time $t_2$, when $S$ changes back to 0, $Q$ does not change. At time $t_3$, $R$ changes to 1, and $Q$ changes back to 0 a short time ($\varepsilon$) later. The duration of the $S$ (or $R$) input pulse must normally be at least as great as $\varepsilon$ in order for a change in the state of $Q$ to occur. If $S = 1$ for a time less than $\varepsilon$, the gate output will not change and the latch will not change state.

Theoretically, the two-inverter circuit of Figure 11-2 and the set-reset of Figure 11-3 can exist in a third stable state. This is the situation where the voltage level at the output of the two inverters or gates is approximately halfway between

the voltage levels for a logic 0 and a logic 1. This state is referred to as a *metastable* state. It is metastable because any noise existing in the circuit will cause the circuit to transition to one of the truly stable states. However, certain events can cause the latch to enter the metastable state for a short time. The simultaneous change in $S$ and $R$ from 1 to 0 in the set-reset latch can cause the latch to enter the metastable state. Also, starting with $Q = 0$ and applying a pulse on $S$ with a length on the borderline between being too short to cause $Q$ to change and just long enough to cause $Q$ to change may cause the circuit to enter the metastable state.

Even though a circuit in the metastable state will quickly enter a stable state, events causing the circuit to enter the metastable state must be avoided. First, the stable state entered from the metastable state is unpredictable. Second, any gates or latches with an input that is in the metastable state will respond unpredictably; the gate or latch may respond as if the input is a logic 0 or it may respond as if the input is a logic 1. Metastable behavior is discussed further in the next sections.

When discussing latches and flip-flops, we use the term *present state* to denote the state of the $Q$ output of the latch or flip-flop at the time any input signal changes, and the term *next state* to denote the state of the $Q$ output after the latch or flip-flop has reacted to the input change and stabilized. If we let $Q(t)$ represent the present state and $Q(t + \varepsilon)$ represent the next state, an equation for $Q(t + \varepsilon)$ can be obtained from the circuit by conceptually breaking the feedback loop at $Q$ and considering $Q(t)$ as an input and $Q(t + \varepsilon)$ as the output. Then for the S-R latch of Figure 11-3

$$Q(t + \varepsilon) = R(t)'[S(t) + Q(t)] = R(t)'S(t) + R(t)'Q(t) \tag{11-1}$$

and the equation for output $P$ is

$$P(t) = S(t)'Q(t)' \tag{11-2}$$

Normally we write the next-state equation without including time explicitly, using $Q$ to represent the present state of the latch and $Q^+$ to represent the next state:

$$Q^+ = R'S + R'Q \tag{11-3}$$

$$P = S'Q' \tag{11-4}$$

These equations are mapped in the next-state and output tables of Table 11-1. The stable states of the latch are circled. Note that for all stable states, $P = Q'$ except when $S = R = 1$. As discussed previously, this is one of the reasons why $S = R = 1$ is disallowed as an input combination to the S-R latch. Making $S = R = 1$ a don't-care combination allows simplifying the next-state equation, as shown in Figure 11-8(a). After plotting Equation (11-3) on the map and changing two entries to don't-cares, the next-state equation simplifies to

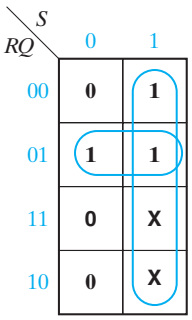
$$Q^+ = S + R'Q \qquad (SR = 0) \tag{11-5}$$

**TABLE 11-1** S-R Latch Next State and Output

| Present State | Next State $Q^+$ | | | | Present Output $P$ | | | |
|---|---|---|---|---|---|---|---|---|
| | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* |
| *Q* | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 0 | ⓪ | ⓪ | ⓪ | 1 | 1 | 1 | 0 | 0 |
| 1 | ① | 0 | 0 | ① | 0 | 0 | 0 | 0 |

**FIGURE 11-8**
Derivation of $Q^+$ for an S-R Latch






(a) $Q^+$ map

| S | R | Q | $Q^+$ | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | |
| 0 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 1 | |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 0 | – | Inputs not allowed |
| 1 | 1 | 1 | – | |

(b) Truth table

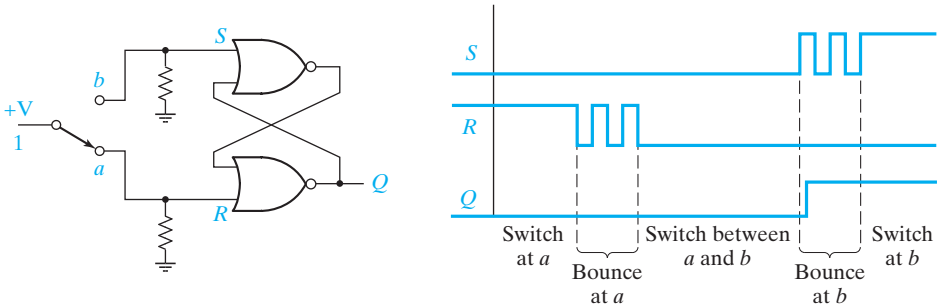
In words, this equation tells us that the next state of the latch will be 1 either if it is set to 1 with an $S$ input, or if the present state is 1 and the latch is not reset. The condition $SR = 0$ implies that $S$ and $R$ cannot both be 1 at the same time. An equation that expresses the next state of a latch in terms of its present state and inputs will be referred to as a *next-state equation*, or *characteristic equation*. Note that the characteristic equation is not necessarily the same as the next-state equation derived from the circuit. They both give the functional behavior of the latch (or FF). However, the characteristic equation is a minimal equation and it takes into account any disallowed input combinations. The next-state equation derived from the circuit is not necessarily minimal and it does not take into account any disallowed input combinations. Compare Equations (11-3) and (11-5).

Another approach for deriving the characteristic equation for an S-R latch is based on constructing a truth table for the next state of $Q$ We previously discussed the latch operation by tracing signals through the gates, and the truth table in Figure 11-8(b) is based on this discussion. Plotting $Q^+$ on a Karnaugh map gives the same result as Figure 11-8(a).

The S-R latch is often used as a component in more complex latches and flip-flops and in asynchronous systems. Another useful application of the S-R latch is for debouncing switches. When a mechanical switch is opened or closed, the switch contacts tend to vibrate or bounce open and closed several times before settling down to their final position. This produces a noisy transition, and this noise can interfere with the proper operation of a logic circuit. The input to the switch in Figure 11-9 is connected to a logic 1 (+V). The pull-down resistors connected to contacts $a$ and $b$

**FIGURE 11-9**
Switch Debouncing with an S-R Latch



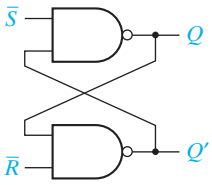


assure that when the switch is between $a$ and $b$ the latch inputs $S$ and $R$ will always be at a logic 0, and the latch output will not change state. The timing diagram shows what happens when the switch is flipped from $a$ to $b$. As the switch leaves $a$, bounces occur at the $R$ input; when the switch reaches $b$, bounces occur at the $S$ input. After the switch reaches $b$, the first time $S$ becomes 1, after a short delay the latch switches to the $Q = 1$ state and remains there. Thus $Q$ is free of all bounces even though the switch contacts bounce. This debouncing scheme requires a *double throw* switch that switches between two contacts; it will not work with a *single throw* switch that switches between one contact and open.

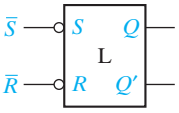
An alternative form of the S-R latch uses NAND gates, as shown in Figure 11-10. We will refer to this circuit as an $\overline{S}$-$\overline{R}$ latch, and the table describes its operation. We have labeled the inputs to this latch $\overline{S}$ and $\overline{R}$ because $\overline{S} = 0$ will set $Q$ to 1 and $\overline{R} = 0$ will reset $Q$ to 0. If $\overline{S}$ and $\overline{R}$ are 0 at the same time, both the $Q$ and $Q'$ outputs are forced to 1. Therefore, for the proper operation of this latch, the condition $\overline{S} = \overline{R} = 0$ is not allowed.

**FIGURE 11-10**
$\overline{S}$-$\overline{R}$ Latch






(a)




(b)

| $\overline{S}$ | $\overline{R}$ | $Q$ | $Q^+$ | |
|---|---|---|---|---|
| 1 | 1 | 0 | 0 | |
| 1 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 0 | |
| 1 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 1 | |
| 0 | 0 | 0 | – | Inputs not allowed |
| 0 | 0 | 1 | – | |

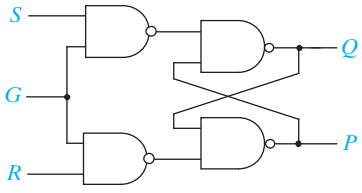
(c)

## 11.3 Gated Latches

Gated latches have an additional input called the gate or enable input. When the gate input is inactive, which may be the high or low value, the state of the latch cannot change. When the gate input is active, the latch is controlled by the other inputs and operates as indicated in the preceding section. A NAND-gate version of a gated S-R latch is shown in Figure 11-11.

**FIGURE 11-11**
NAND-Gate Gated S-R Latch





The next-state equation is

$$Q^+ = SG + Q(R' + G')$$

and the equation for the $P$ output is

$$P = Q' + RG$$

The next-state and output tables are shown in Table 11-2. When $G = 0$, the circuit is always in a stable state; when $G = 1$, $S = 1$ sets the latch and $R = 1$ resets the latch. Note that $P = Q'$ whenever the latch is in a stable state except for the input combination $G = S = R = 1$; consequently, as for the basic latch, the $S = R = 1$ input combination is disallowed.

**TABLE 11-2**
Next-State and Output of Gated S-R Latch



Next State $Q^+$

| Present State | $G = 0$ | | | | $G = 1$ | | | |
|---|---|---|---|---|---|---|---|---|
| | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* |
| *Q* | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 0 | ⓪ | ⓪ | ⓪ | ⓪ | ⓪ | ⓪ | 1 | 1 |
| 1 | ① | ① | ① | ① | ① | 0 | ① | ① |

Present Output P

| Present State | $G = 0$ | | | | $G = 1$ | | | |
|---|---|---|---|---|---|---|---|---|
| | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* | *SR* |
| *Q* | 00 | 01 | 11 | 10 | 00 | 01 | 11 | 10 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

Another reason for disallowing the $S = R = 1$ input combination is illustrated by considering a change in $G$ from 1 to 0 with $S = R = 1$. When $G$ changes, both inputs to the basic S-R latch change from 0 to 1, as shown in Figure 11-12. This causes both gates in the basic S-R latch to attempt to change from 1 to 0; a race condition exists and the propagation delays of the gates determine whether the latch stabilizes with $Q = 0$ or $Q = 1$. This was illustrated in Figure 11-6 for the simple NOR-gate latch.

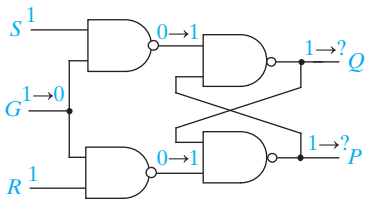



**FIGURE 11-12**
Race Condition in the Gated S-R Latch

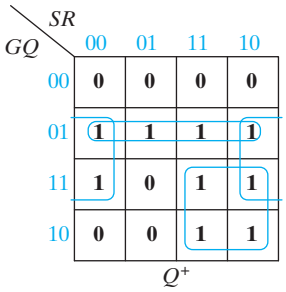


It is also instructive to examine this problem from a different viewpoint. If the equation for $Q^+$ is plotted on a Karnaugh map (Figure 11-13), it is evident that $Q^+$ has a static 1-hazard for the input combinations $G = 1, S = 1, R = 1, Q = 1$ and

$G = 0, S = 1, R = 1, Q = 1$. Consequently, when $G$ changes from 1 to 0 between these two input combinations, it is possible for $Q$ to change from 1 to 0 and, because of the feedback, to cause $Q$ to remain at $Q = 0$. This is simply a different interpretation of the race condition described above. Of course, the static 1-hazard exists for $G$ changing from 0 to 1 and, again, $Q$ may change to 0, but in this case $Q$ is forced back to 1 by the $S = R = 1$ input values. So, for this change, the hazard may cause a glitch in $Q$, but it cannot cause the latch to stabilize with $Q = 0$.

**FIGURE 11-13**
Karnaugh Map for $Q^+$



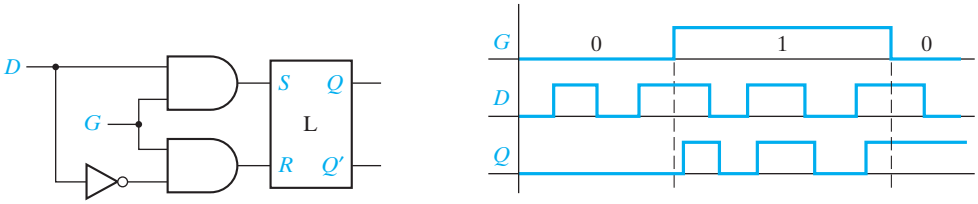



There is another restriction regarding gated S-R latches. The $S$ and $R$ inputs must not be changing or contain glitches while $G = 1$. For example, assume $Q = 0$ when $G$ changes from 0 to 1 and $S = 0$ and $R = 0$. If $S$ and $R$ remain at 0 until $G$ returns to 0, then $Q$ remains at 0. However, if $S$ contains a 1 glitch, maybe due to a static 1-hazard in its circuit, then $Q$ may be forced to a 1 and will remain there after $G$ becomes 0. A similar problem occurs if $S$ does not change from 1 to 0 until after $G$ changes to 1. This is referred to as the 1's catching problem. A NOR-gate version of the gated S-R latch has a 0's catching problem.

Another gated latch is the gated D latch. It can be obtained from a gated S-R latch by connecting $S$ to $D$ and $R$ to $D'$. Figure 11-14(a) shows this construction using a basic S-R latch, two AND gates and an inverter; the NAND-gate, gated S-R latch in Figure 11-11 can be converted to a gated D latch with the addition of an inverter. As indicated in Figure 11-14(b), $Q$ of the gated $D$ latch remains unchanged while $G$ is inactive, $G = 0$ in this case, and $Q$ becomes equal to the $D$ after some delay when $G$ is active. The delay is due to the propagation delay of the gates. This latch is also referred to as a *transparent latch* since $Q$ becomes equal to $D$ while $G$ is active. Figure 11-15 shows the state table and characteristic equation for the gated $D$ latch.

**FIGURE 11-14**
Gated D Latch





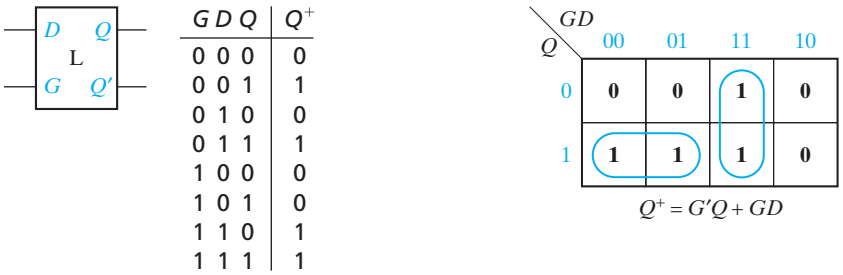



**FIGURE 11-15**
Symbol and Truth Table for Gated Latch



Most digital systems use a clock signal to synchronize the change in outputs of the system's flip-flops to an edge of the clock signal, either the positive (0 to 1) or the negative (1 to 0) edge of the clock. It is tempting to think that gated latches could be used as flip-flops where the clock signal is connected to the gate inputs of the latches. However, this is not a practical approach. The following example illustrates the difficulty. In the circuit of Figure 11-16, it seems that when the Clk is 1 the next value of $Q$ should be $Q'$ when the input $x = 1$ and should be $Q$ when $x = 0$. However, when Clk = 1 and $x = 1$, $D = Q'$ causes $Q$ to change and, if Clk remains 1, the change in $Q$ will feed back and cause $Q$ to change again. If Clk remains at 1, $Q$ will oscillate. Consequently, the circuit will only operate as intended if Clk remains at 1 for a short time; it has to 1 just long enough to allow $Q$ to change but short enough to prevent the change from feeding back and causing a second change. With a single latch, it may be possible to control the clock high time so the latch operates as intended, but in a system with several latches, the variation in gate delays would make it impossible to provide the correct clock width to all latches.

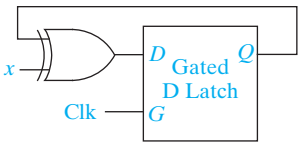



**FIGURE 11-16**
Unreliable Gated D Latch Circuit



To avoid this timing problem, more complicated flip-flops restrict the flip-flop outputs to only change on an edge of the clock, and the outputs cannot change at other times even if the inputs change. If the inputs to the flip-flop only need to be stable for a short period of time around the clock edge, then we refer to the flip-flop as *edge-triggered*. (See the discussion of setup and hold times in the next section.) The term *master-slave* flip-flop refers to a particular implementation that uses two gated latches in such a way that the flip-flop outputs only change on a clock edge. However, master-slave flip-flops are not necessarily edge-triggered flip-flops because they may require the flip-flop inputs to be stable at times during the clock period other than just around the clock edge. The S-R, J-K, and T master-slave flip-flops in later sections are examples. The master-slave D flip-flop of the next section is an exception; it uses the master-slave implementation and it is also edge triggered.