Homework 3: Counters and Sequential Circuit Analysis

Solve the **four** following problems. Show all your work/process. Please neatly write or type your answers, and please scan or upload your answers in a single PDF file to the assignment submission on Carmen. Answers may be graded for correctness, thoroughness, completion, or some combination.

3.1 Consider a 4-bit counter which counts in the following sequence:

0000, 0001, 0010, 0011, 0100, 0110, 1000, 1001, 1010, 1100, 1110, 1111, 0000, …

a. Design the counter using D flip-flops. Derive the excitation equations and draw the circuit.

b. Design the counter using J-K flip-flops. Derive the excitation equations and draw the circuit.

c. Design the counter using the LS163A (74x163) 4-bit binary counter shown below in Figure 1. Derive the excitation equations for CLR, LD, D, C, B, and A, and draw the circuit. Assume both ENP and ENT are connected to power (set to high level). Assume CLR has precedence over LD. Draw a clock signal into the CLK input and the connection to power for ENP and ENT.

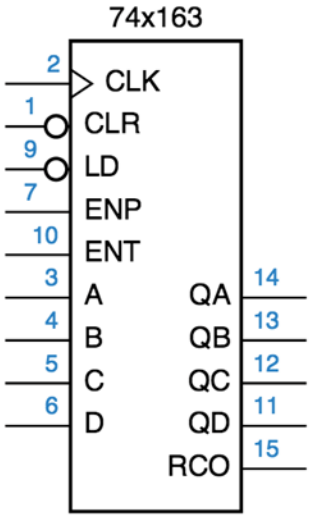

Figure 1: LS163A 4-bit synchronous counter block diagram.

3.2 A sequential circuit contains a register of four flip-flops. Initially a binary number N is stored in the flip-flops ($0000 \leq N \leq 1011$). After a single clock pulse is applied to the circuit, the register should contain $N + 0100$. In other words, the function of the sequential circuit is to add 4 to the contents of a 4-bit register. Design the circuit using T flip-flops. Derive the excitation equations and draw the circuit.

3.3 Consider the sequential circuit shown in Figure 2.

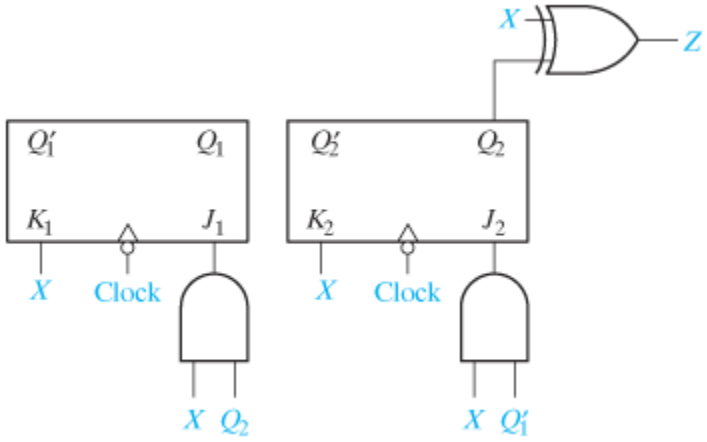

Figure 2: Sequential circuit for problem 3.3.

a. Is this a Mealy machine or a Moore machine? Explain how you know.

b. Derive the excitation equations, characteristic equations, and output equation for this circuit.

c. Construct a state/output table for this circuit.

d. Construct a state diagram for this circuit.

e. Construct a timing diagram for this circuit for the input sequence X = 10011. Show the clock, X, Q_1, Q_2, and Z signals. Assume that X changes midway between falling and rising clock edges. Initially, $Q_1 = Q_2 = 0$ and $X = 1$.

For parts (f) through (i), use the timing data shown in the tables at the end of this document.

f. Compute the maximum clock frequency f_{max} for this circuit. Show all paths which need to be considered and their associated delays.

g. Compute the setup time t_{su}^{X} for the input X for this circuit. Show all paths which need to be considered and their associated delays.

h. Compute the hold time t_{h}^{X} for the input X for this circuit. Show all paths which need to be considered and their associated delays.

i. Compute the maximum propagation delay to the output $t_{pd}^{X \to Z}$ for the input X for this circuit. Show all paths which need to be considered and their associated delays.

3.4 Consider the sequential circuit shown in Figure 3.

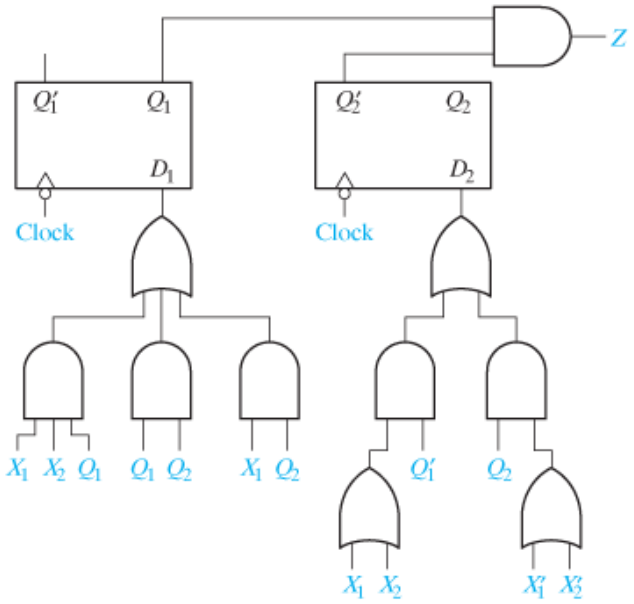

Figure 3: Sequential circuit for problem 3.4.

a. Is this a Mealy machine or a Moore machine? Explain how you know.

b. Derive the excitation equations, characteristic equations, and output equation for this circuit.

c. Construct a state/output table for this circuit.

d. Construct a state diagram for this circuit.

For parts (e) through (h), use the timing data shown in the tables at the end of this document. Assume there is no delay associated with obtaining the complemented versions of X_1 and X_2. Assume the delay through the three-input OR gate is equal to **twice** the delay of a two-input OR gate (LS32).

e. Compute the maximum clock frequency f_{max} for this circuit. Show all paths which need to be considered and their associated delays.

f. Compute the setup time $t_{su}^{X_1}$ for the input X_1 for this circuit. Show all paths which need to be considered and their associated delays.

g. Compute the hold time $t_h^{X_1}$ for the input X_1 for this circuit. Show all paths which need to be considered and their associated delays.

h. Compute the maximum propagation delay to the output $t_{pd}^{CLK \to Z}$ for this circuit. Show all paths which need to be considered and their associated delays.

Combinational Parts

Chip	t_{pLH} (ns)	t_{pHL} (ns)	Comments
'LS04, 'LS00, 'LS10, 'LS20	15	15	Inverter, 2-, 3-, 4-input NAND
'LS08, 'LS11	15	20	2-, 3-input AND
'LS02, 'LS27	15	15	2-, 3-input NOR
'LS32	22	22	2-input OR
'LS86			2-input XOR
2 levels	23	17	Other input low
3 levels	30	22	Other input high
'LS138			3-to-8 Decoder
$A, B, C, \rightarrow Y$ (2 levels)	20	41	$A \rightarrow Y_0, Y_2, Y_4, Y_6$ or $B \rightarrow Y_0, Y_1, Y_4, Y_6$ or $C \rightarrow Y_0, Y_1, Y_2, Y_3$
$A, B, C \rightarrow Y$ (3 levels)	27	39	Other cases
$G2A, G2B \rightarrow Y$	18	32	
$G1 \rightarrow Y$	26	38	
'LS139			2-to-4 Decoder
$A, B \rightarrow Y$ (2 levels)	20	33	$A \rightarrow Y_0, Y_2$ or $B \rightarrow Y_0, Y_1$
$A, B \rightarrow Y$ (3 levels)	29	38	Other cases
$G \rightarrow Y$	24	32	

'LS74 - D Type Positive-Edge-Triggered Flip-Flops

Data	t_{pLH}	t_{pHL}	t_s	t_h
$CLR, PR, CLK \rightarrow Q$	25	40		
D			20	5
$f_{max} = 25$ Mhz				

'LS109 - $J - \bar{K}$ Type Positive-Edge-Triggered Flip-Flops

Data	t_{pLH}	t_{pHL}	t_s	t_h
$CLR, PR, CLK \rightarrow Q$	25	40		
J, K			35	5
$f_{max} = 25$ Mhz				