Lecture Outline

Reminders to self:

- ❑ Turn on lecture recording to Cloud
- ❑ Turn on Zoom microphone

- Last Lecture
  - Continued Analysis of clocked sequential circuits
    - Analysis of Moore machine by Transition Tables & State Graphs
    - Designed a 2-flip-flop Moore machine using State Graph & Transition Table
    - Started Analysis of Mealy machine by Transition Tables & State Graphs
- Today's Lecture
  - Continue Analysis of clocked sequential circuits
    - Finish Analysis of Mealy machine by Transition Tables & State Graphs
    - Timing charts from State Tables & Graphs
  - General models for clocked sequential circuits
  - Start design of clocked sequential circuits

Handouts and Announcements

- Announcements
  - Homework Problem HW 13-2
    - I expect to post on Carmen this afternoon
    - Due 11:59pm Thursday 3/30
  - Homework Reminder
    - HW 12-5 now past due (11:25am today)
    - HW 13-1 Due: 11:25am Wednesday 3/29
  - Read for Friday: pages 463-472, 149-151
  - Participation Quiz 10 available 12:25pm today
    - Due 12:25pm tomorrow
    - Available additional 24hr with late penalty

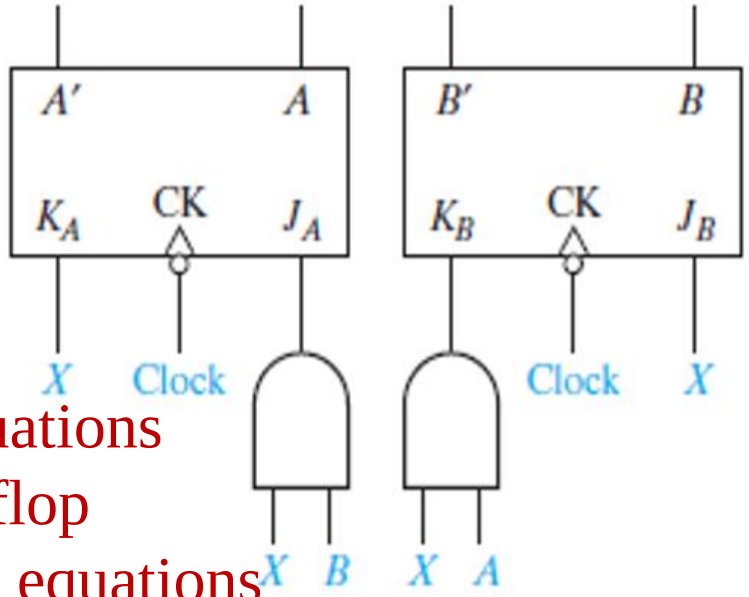
Handouts and Announcements

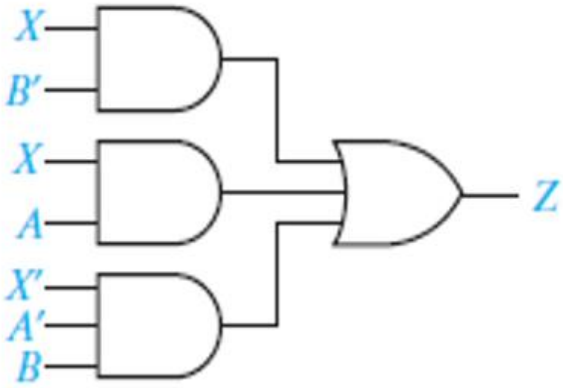
- Announcements
  - Mini-Exam 5 Reminder
    - Available 5pm Monday 3/27 through 5:00pm Tuesday 3/28
    - Due in Carmen PROMPTLY at 5:00pm on 3/28
    - Designed to be completed in ~36 min, but you may use more
    - When planning your schedule:
      - I recommend building in 10-15 min extra
      - To allow for downloading exam, signing and dating honor pledge, saving solution as pdf, and uploading to Carmen
    - I also recommend not procrastinating
  - Exam review topics available on Carmen
  - Sample Mini-Exams 6 and 7 from Au20 also available

Analysis by Transition Tables & Graphs

Repeat Mealy example (last lecture) using these techniques:

- $J_A = XB$
- $K_A = X$
- $J_B = X$
- $K_B = XA$





2. Derive next-state equations for each flip-flop from its input equations (using flip-flop next-state relations)

$$Z = XB' + XA + X'A'B$$

J-K: $Q^+ = JQ' + K'Q$

- $A^+ = XBA' + X'A$
- $B^+ = XB' + (XA)'B = XB' + X'B + A'B$

Example we were analyzing last lecture – 2nd last slide

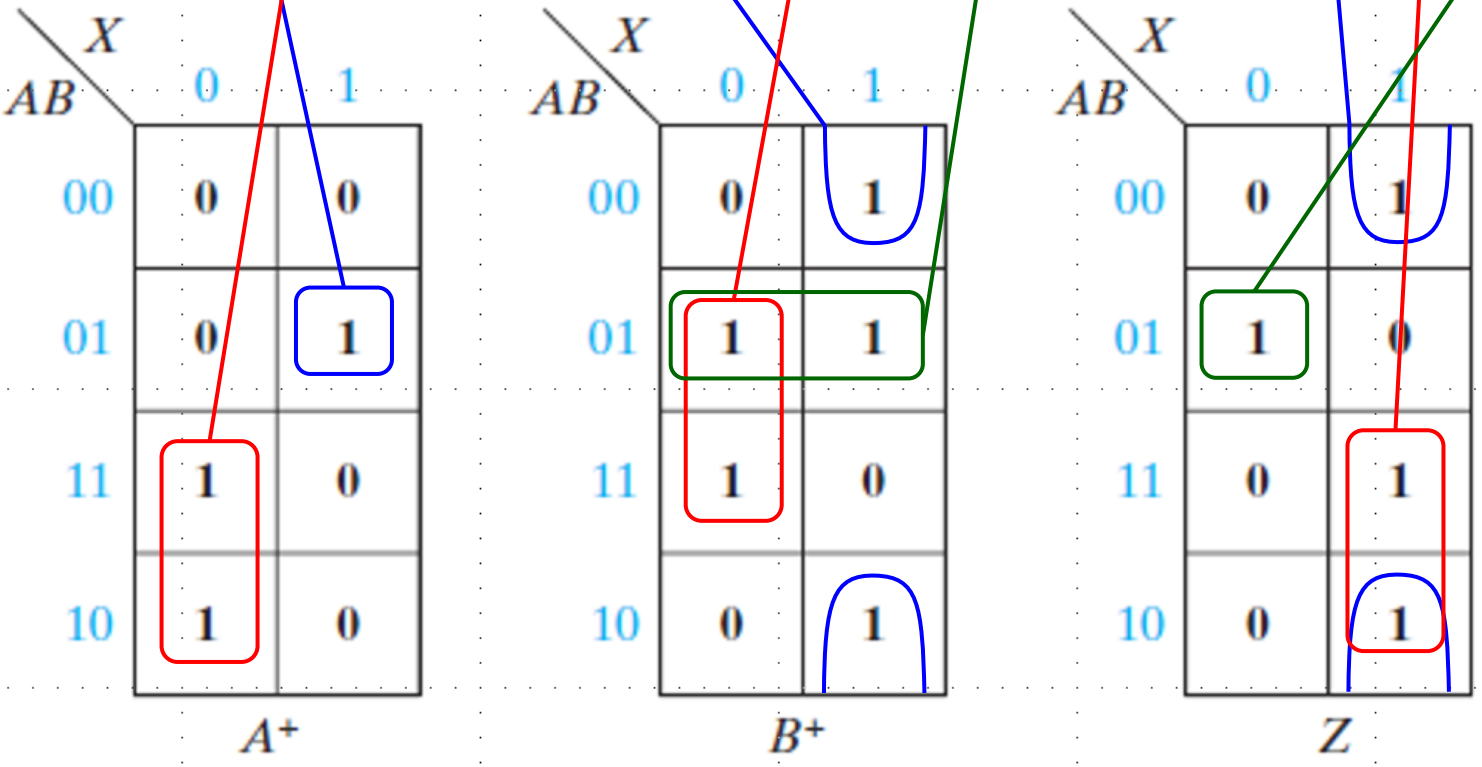
Analysis by Transition Tables & Graphs

Repeat Mealy example (last lecture) using these techniques:

3. Plot a next-state map for each flip-flop

- $A^+ = XBA' + X'A$
- $B^+ = XB' + (XA)'B = XB' + X'B + A'B$

$Z = XB' + XA + X'A'B$



Where we ran out of time last lecture

Analysis by Transition Tables & Graphs

Repeat Mealy example (last lecture) using these techniques:

4. Combine these maps to form the transition table that gives the next state of the flip-flop as a function of current state and circuit inputs

AB \ X	0	1
00	0	0
01	0	1
11	1	0
10	1	0

A^+

AB \ X	0	1
00	0	1
01	1	1
11	1	0
10	0	1

B^+

AB \ X	0	1
00	0	1
01	1	0
11	0	1
10	0	1

Z

AB	A^+B^+ X = 0	1	Z X = 0	1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

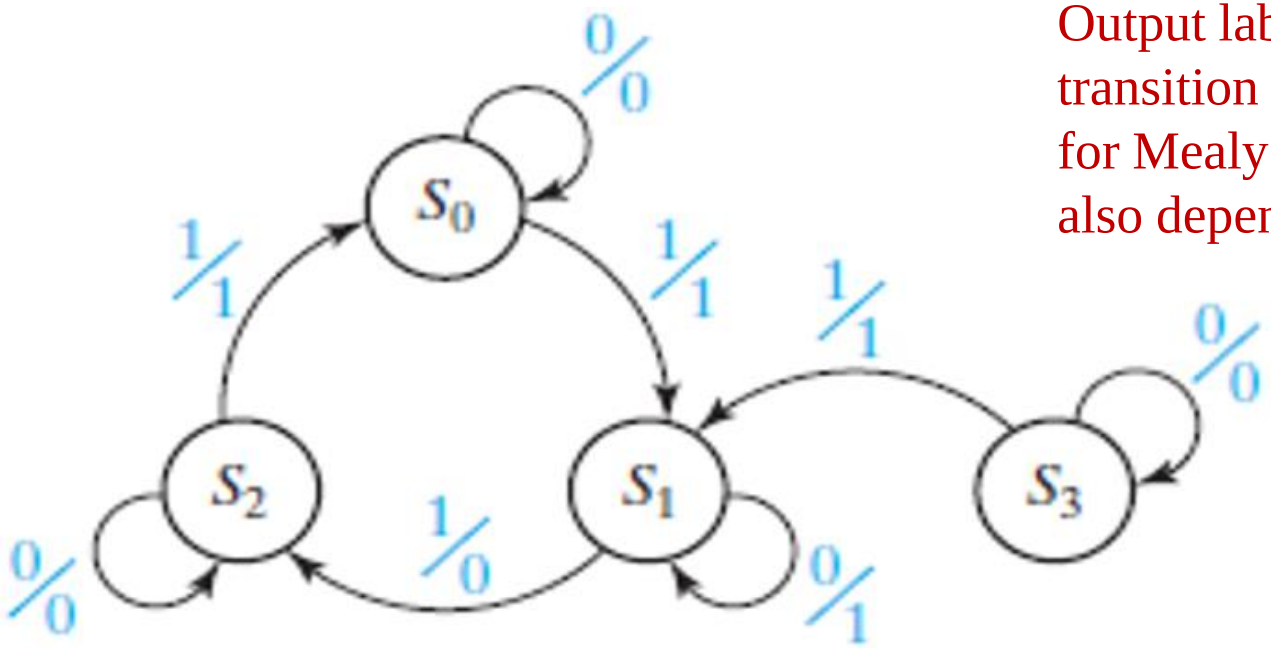
Present State	Next State X = 0	1	Present Output X = 0	1
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

Analysis by Transition Tables & Graphs

Repeat Mealy example (last lecture) using these techniques:

AB	A^+B^+ X = 0	1	Z X = 0	1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

Present State	Next State X = 0	1	Present Output X = 0	1
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1



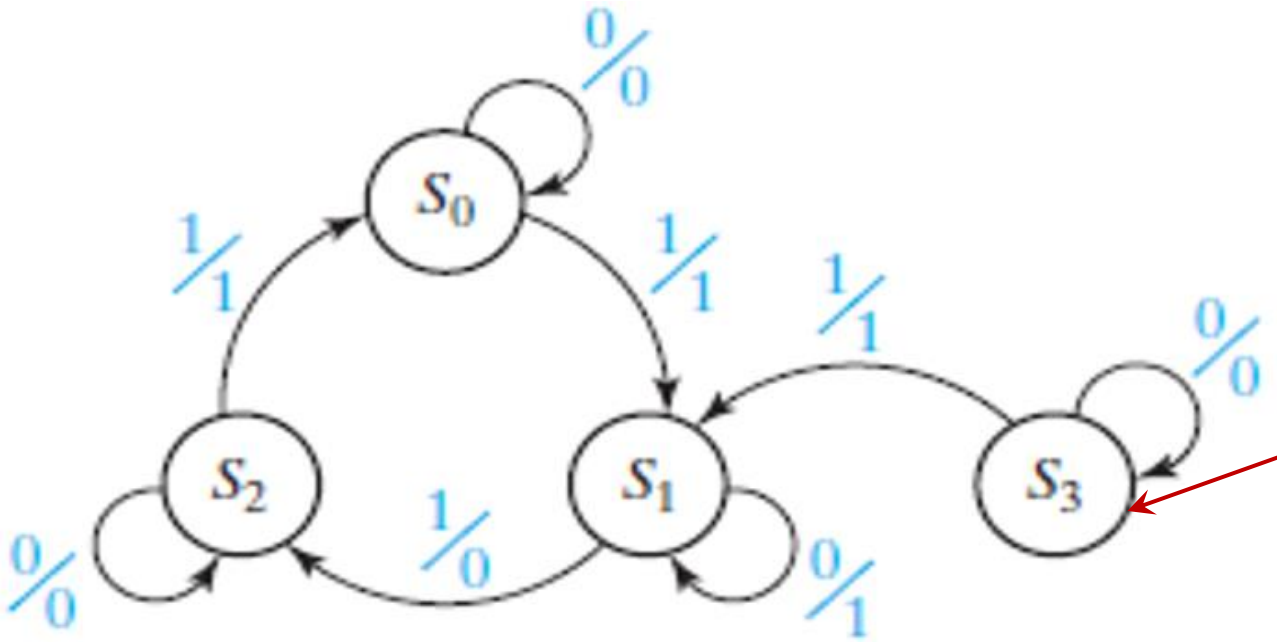
Output labeled on transition arrows since for Mealy machine output also depends on input

Analysis by Transition Tables & Graphs

Repeat Mealy example (last lecture) using these techniques:

	A^+B^+		Z	
AB	$X=0$	1	$X=0$	1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

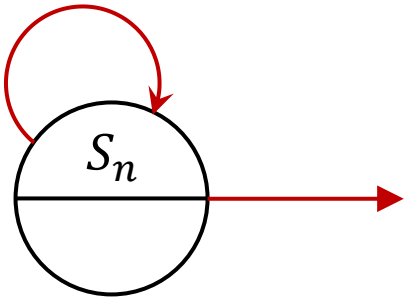
Present State	Next State		Present Output	
	$X=0$	1	$X=0$	1
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1



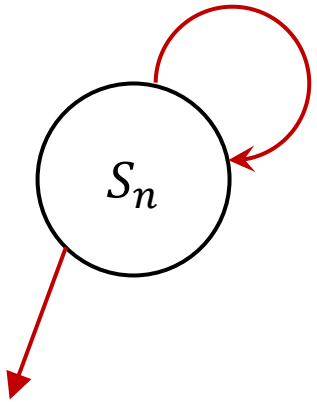
But look at S_3 out here without any transitions pointing into it

Comparison of Moore vs Mealy State Graphs

Moore:



Mealy:



- This labeling assumes that output is only on active clock edge
- Recall that doing so eliminates errors due to
- Thus no provision for extra input changes that produce false outputs included on state graphs

State Tables & Graphs

Procedure to Construct and Interpret Timing Charts:

1. Remember that a state change can only occur after the active edge of the clock
2. The input should normally be stable immediately before and after the clock edge
   - Before: For longer than at least the time
   - After: For longer than at least the time

   See D flip-flop lecture or Figure 11-20 in textbook
3. Output changes:
   - Moore: only when state change
   - Mealy: can change when input changes, as well as when state changes
     - False output may occur between when state changed and when input changes to next value
     - Output may be temporarily incorrect until new input value is applied
4. False outputs difficult to determine from state graphs. When constructing timing charts for Mealy circuits use either:
   - Signal tracing, or
   - State tables

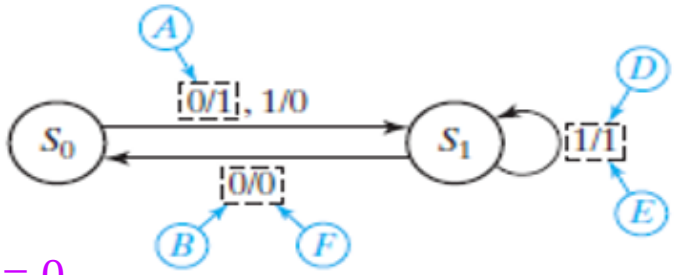
Procedure to Construct and Interpret Timing Charts:

5. When using a Mealy state table to make a timing chart:
   a) For first input, read present output and plot it
   b) Read next state and plot it, following active edge of clock
   c) Go to row in table corresponding to next state, read output from old input column, and plot it (this may be a false output)
   d) Change to next input and repeat steps a), b) and c)
      - Including step c) assumes a fully detailed timing chart is being constructed
      - Step c) may be omitted if goal is just the correct output sequence.
6. For Mealy circuits the best time to read output is just before active clock edge
   - Input must be stable at that time
   - Thus output will be correct then

State Tables & Graphs

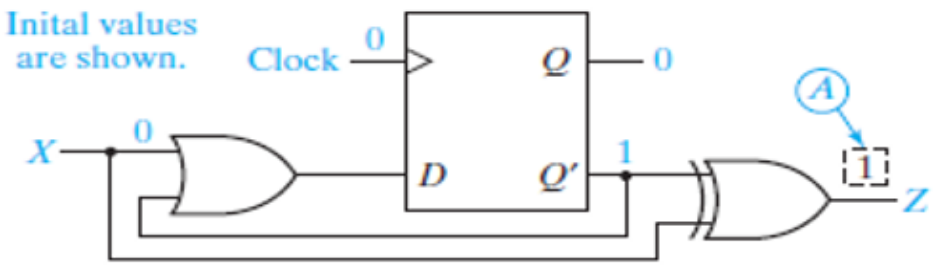
TopHat

Is this Moore or Mealy?



Q		X = 0	1	0	1
0	S_0	S_1	S_1	1	0
1	S_1	S_0	S_1	0	1

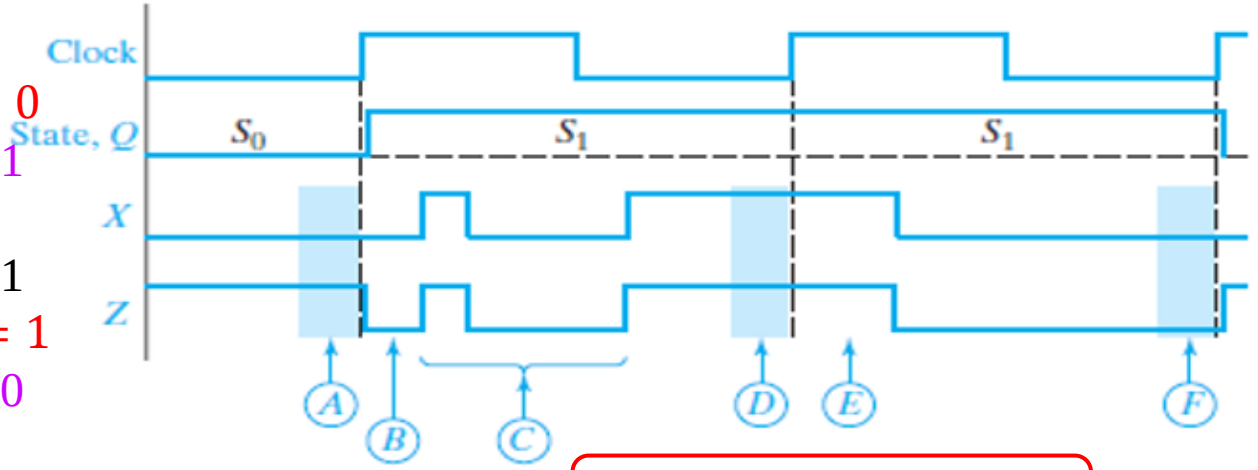
A. State S_0, input = 0
   Output $Z = 1$
B. State S_1, input = 0
   False output $Z = 0$
C. State S_1, input = 1
   False output $Z = 1$



Using input & output just before active clock edge:
$X =$
$Z =$

input = 0
False output $Z = 0$

D. State S_1, input = 1
   Output $Z = 1$
E. State S_1, input = 1
   False Output $Z = 1$
F. State S_1, input = 0
   Output $Z = 0$
   (To State S_0)



Read X and Z in shaded area (before rising edge of clock).

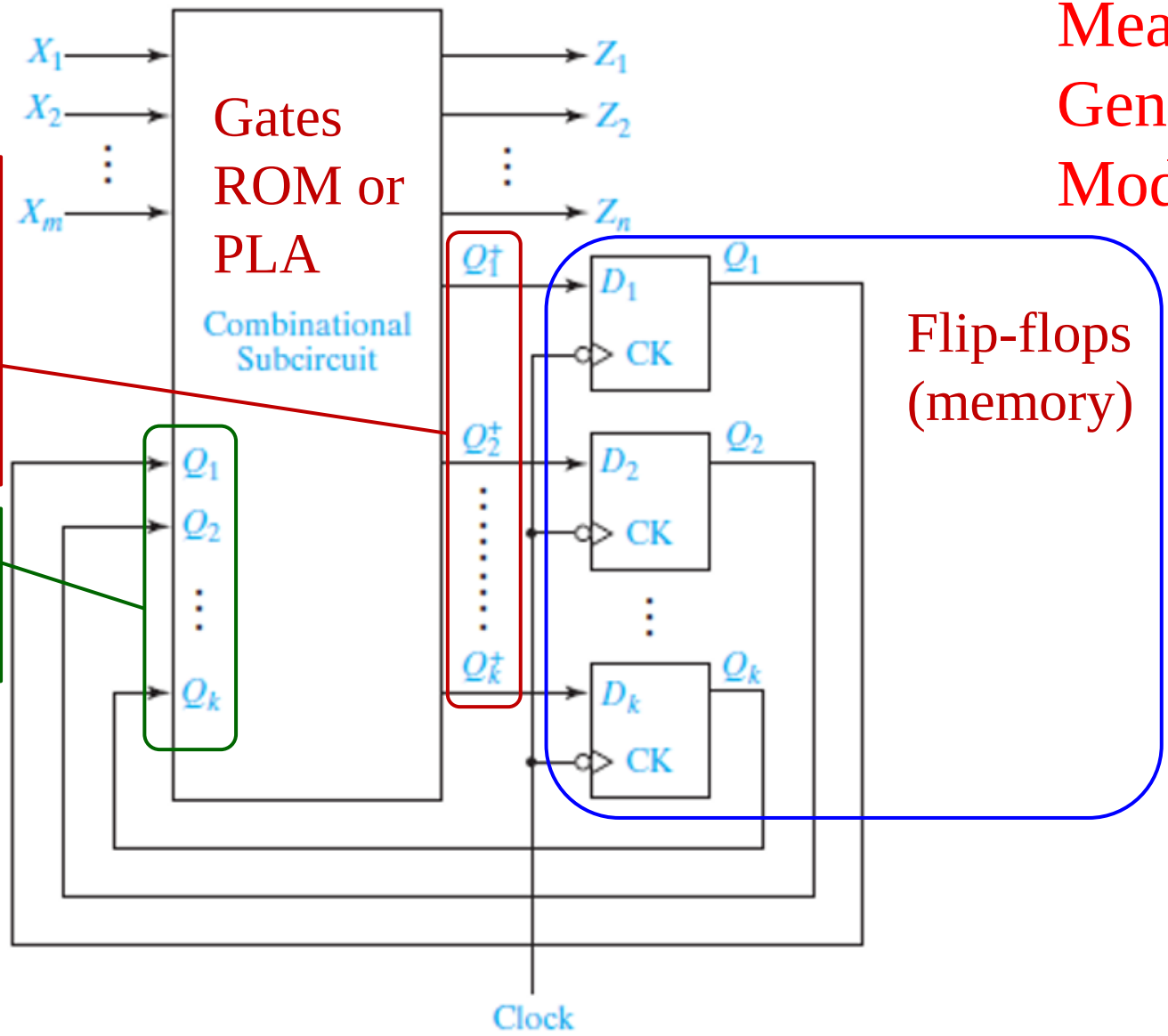
General Models for Sequential Circuits

- A sequential circuit can be divided into two parts
  - Flip-flops (which serve as)
  - Combinational logic (which realizes)
- Combinational logic may be implemented
  - With gates (all of our examples so far)
  - With a , or
  - With a or

Alternative approaches previously introduced for implementing combinational logic

General Models for Sequential Circuits

Mealy General Model



- k flip-flop input functions , or
- $2k$ input functions

$2k$ flip-flop outputs

Flip-flops (memory)

General Models for Sequential Circuits

- Determining minimum clock period
  - Must allow for
    - Propagation delay, t_p, from active clock edge until flip-flop outputs are stable
    - Longest propagation delay through combinational logic, t_c
    - Flip-flop setup time, t_{su}: time before active clock edge that inputs must be valid
  - Assuming the inputs are stable no later than $t_c + t_{su}$ before the active clock edge, the minimum clock period is

$$T_{clk}(min) = t_p + t_c + t_{su}$$

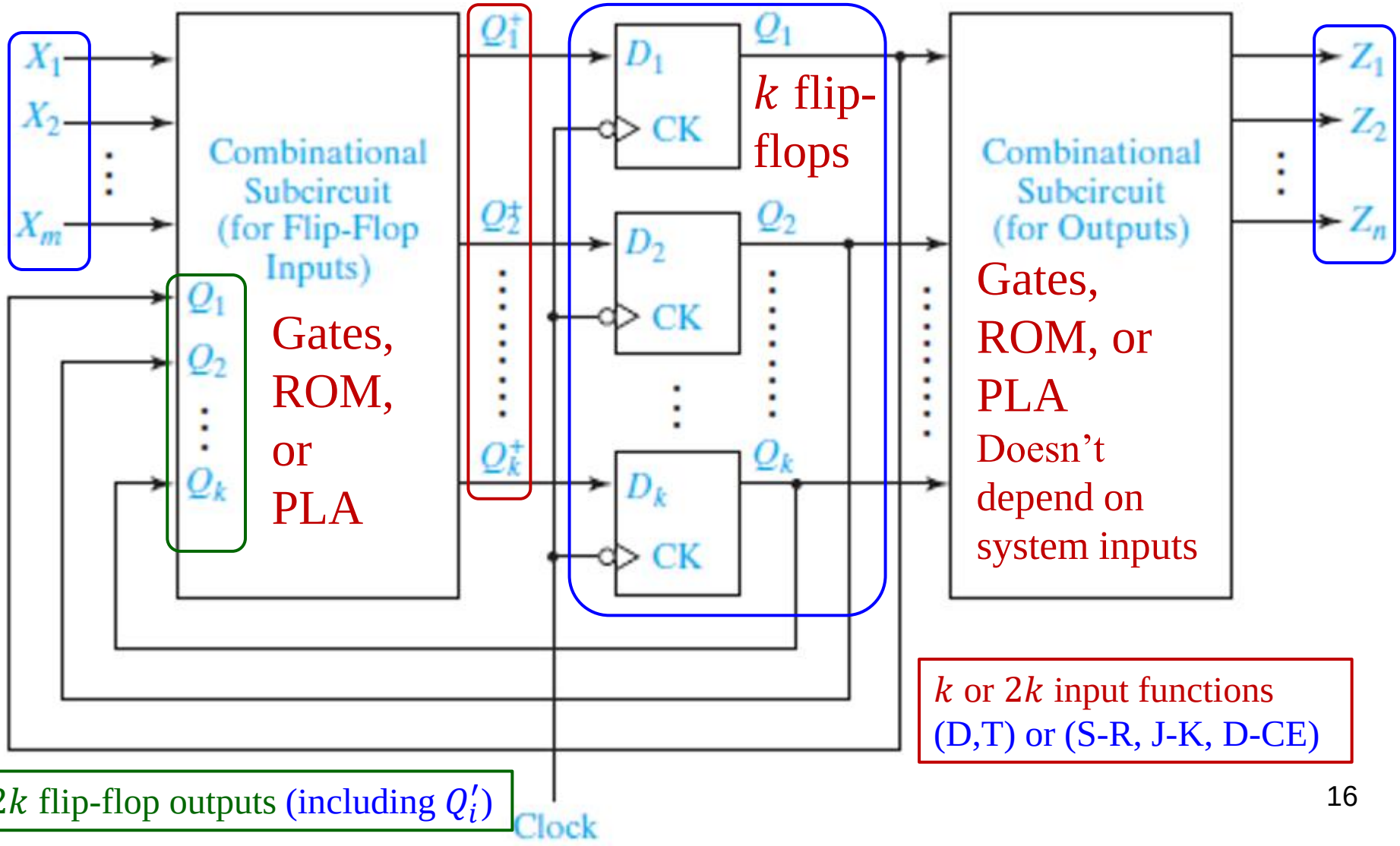
  - If the inputs are not stable that soon, then the time required for the inputs to be stable, t_x, is $> t_p$ and must replace t_p

$$T_{clk}(min) = t_x + t_c + t_{su}$$

  - Clock signals also travel different distances and may arrive at different times
    - Characterized by clock skew, t_{sk}
    - May have to be added to period, or put constraints on t_p and t_c
    - This is an FYI – varies with details of situation. Be aware clock skew exists.

General Models for Sequential Circuits

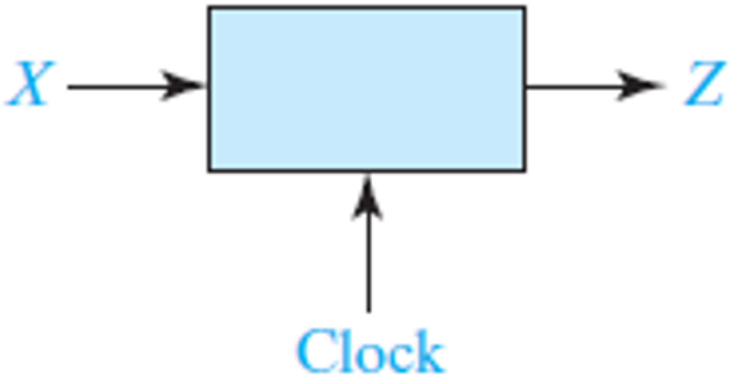
Moore General Model



Mealy Design Example: Sequence Detector

- Sequence Detector Description:
  - Circuit that
    - Examines a serial string of 0's and 1's applied to the X input
    - Generates an output $Z = 1$ only when a prescribed input sequence occurs
  - Assume that the input X will change only between clock pulses
  - For this example, the prescribed input sequence is 101
    - Any input sequence ending in 101 produces $Z = 1$
    - If output $Z = 1$ you know that the last three serial input bits were 101
  - Circuit will not reset when a 1 output occurs
  - Sample input/output sequence:

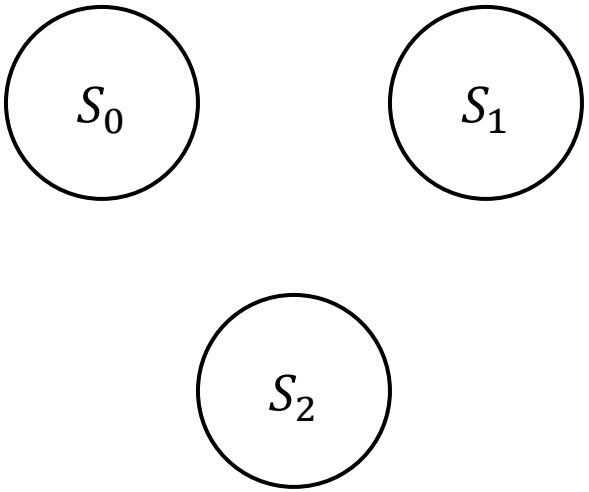
Block Diagram



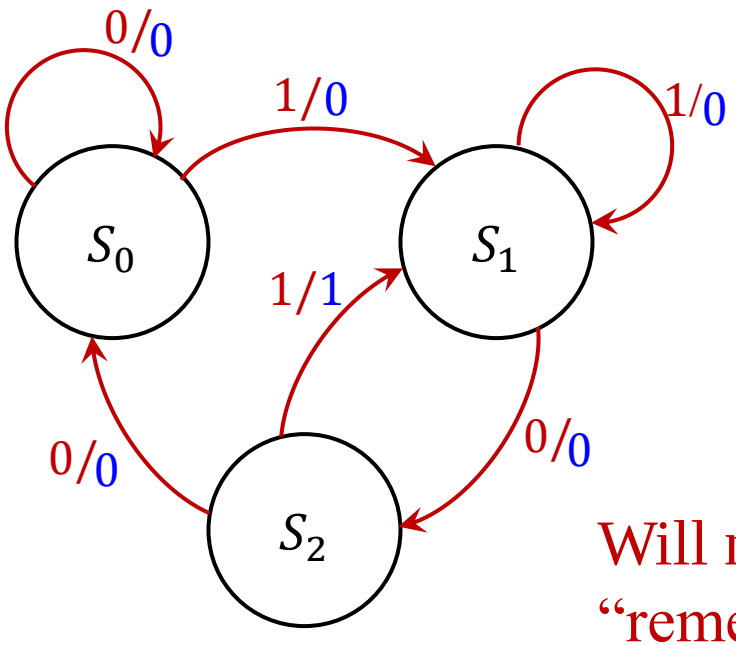
$X =$	0	0	1	1	0	1	1	0	0	1	0	1	0	1	0	0
$Z =$	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0
(time:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15)

Mealy Design Example: Sequence Detector

- Sequence Detector: Any input sequence ending in 101 produces Z=1
  - Initially start circuit in a reset state S_0
  - Since prescribed sequence does not start with 0, if in S_0 and zero received, then
  - If in S_0 and 1 received, must remember that. Go to new state
  - If in S_1 and 0 received, must remember that "10" has been received.
  - If in S_1 and 1 received, still have only first "1" bit in "101" pattern.
  - If in S_2 and 0 received, "00" isn't desired pattern, nor first "1".
  - If in S_2 and 1 received
    - Have full "101" pattern:
    - And have first "1" of next pattern
    -
    - This is the only transition for which should be output
  - Outputs for all other transitions should be



Mealy Design Example: Sequence Detector



The State Table can be created from the State Graph

Present State	Next State $X=0$	Next State $X=1$	Present Output $X=0$	Present Output $X=1$
S_0	S_0	S_1	0	0
S_1	S_2	S_1	0	0
S_2	S_0	S_1	0	1

Will need two flip-flops to "remember" three states

Remember, output is present as soon as X changes. Present before state change at active clock edge.

The Transition Table can be created from the State Table

AB	A^+B^+ $X=0$	A^+B^+ $X=1$	Z $X=0$	Z $X=1$
00	00	01	0	0
01	10	01	0	0
10	00	01	0	1

Mealy Design Example: Sequence Detector

D Flip-Flop Next-State Maps and the Output Map can be created from the Transition Table

Transition Table

	A^+B^+		Z	
AB	$X=0$	$X=1$	$X=0$	$X=1$
00	00	01	0	0
01	10	01	0	0
10	00	01	0	1

AB \ X	0	1
00	0	0
01	1	0
11	X	X
10	0	0

$A^+ = X'B$

AB \ X	0	1
00	0	1
01	0	1
11	X	X
10	0	1

$B^+ = X$

AB \ X	0	1
00	0	0
01	0	0
11	X	X
10	0	1

$Z = XA$

Mealy Design Example: Sequence Detector

$A^+ = X'B$ $B^+ = X$ $Z = XA$