In the last part of the lecture of 3/22, continued during the lecture of 3/24, the design of a Mealy machine sequence detector was reviewed.

For this problem you are to design another sequence detector. Design constraints:

1. It must be a Moore machine.
2. The sequence it must detect in a serial string of 1s and 0s at input Y is “100”.
3. You may assume that the values arriving at input Y are properly synchronized with the clock.
4. The output must be $Z = 1$ when the prescribed sequence is detected, and 0 otherwise.
5. The circuit does not have to automatically reset when a 1 output occurs. (Return to initial state only when appropriate for sequence detection.)
6. It is possible to implement the design with only four states and two flip-flops. Since we generally do not want to implement designs that require more resources than are necessary, you MUST not use more than two flip-flops in your design.
7. Name the flip-flops A and B, and use the following state-name definitions: $S_0\ (AB = 00)$, $S_1\ (AB = 01)$, $S_2\ (AB = 10)$, $S_3\ (AB = 11)$
8. Use S_0 for the initial state. It is up to you to decide what each of the other state-names mean with respect to the input sequence. Since you have some freedom of choice you must clearly articulate what each state-name means. See slide 6 of the 3/29 lecture, for example.
9. Logic must be implemented with no more than two levels and use only AND gates and OR gates (and a single inverter if you need to generate Y' from the Y input).

Please submit:

a) Your design for the State Graph, with documentation of what each State means (see item 8 above).

b) Corresponding State Table

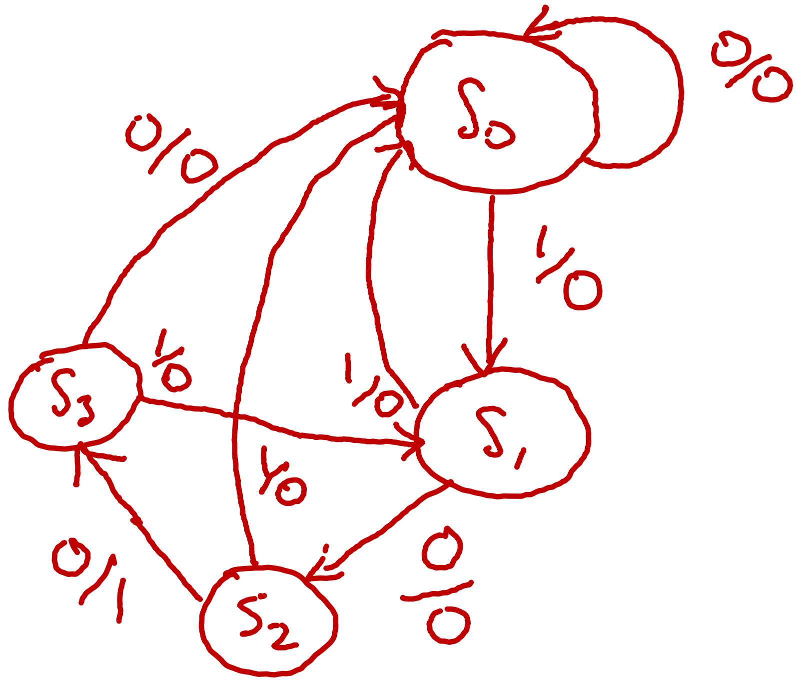
c) Corresponding Transition Table

d) Corresponding flip-flop Next-State Maps and expressions derived therefrom.

e) Circuit diagram

ps. The Mealy machine sequence detector described in lecture only required three states. But as mentioned in an earlier lecture, it is typical for a Moore machine to require more states to accomplish the same task.

a)



b)

Present state	next state $X=0$	next state $X=1$	Present Output $X=0$	Present Output $X=1$
S_0	S_0	S_1	0	0
S_1	S_2	S_0	0	0
S_2	S_3	S_0	1	0
S_3	S_0	S_1	0	0

c)

AB	A^+B^+ $X=0$	A^+B^+ $X=1$	Z $X=0$	Z $X=1$
00	00	01	0	0
01	10	00	0	0
10	11	00	1	0
11	00	01	0	0

d)

AB \ Y	0	1
00	0	0
01	1	0
11	1	0
10	0	0

$A^+ = BY'$

AB \ Y	0	1
00	0	1
01	0	0
11	1	0
10	0	1

$B^+ = B'Y + ABY'$

AB \ Y	0	1
00	0	0
01	0	0
11	1	0
10	0	0

$Z^+ = ABY'$

e)