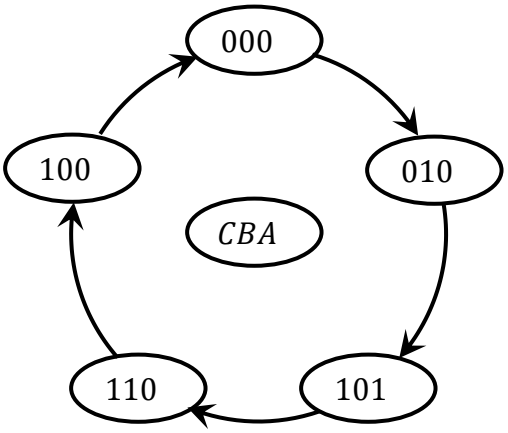
This is a 15 point problem

The final goal of this problem is design of two three-bit synchronous counter circuits to implement the count sequence shown in the adjacent transition graph.

The first circuit will use S-R flip-flops.

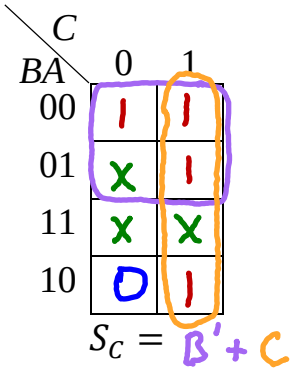
The second circuit will use J-K flip-flops.



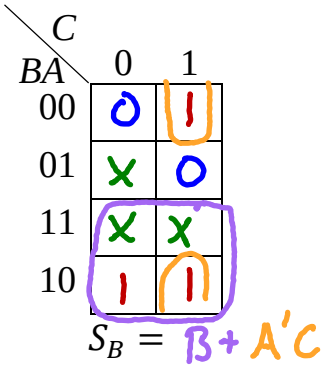
C	B	A	C^+	B^+	A^+	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	0	1	0	1	1	0	1	1	1
0	0	1	X	X	X	X	X	X	X	X	X
0	1	0	1	0	1	0	1	1	0	0	1
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	0	0	0	1	0	1	1	1	1
1	0	1	1	1	0	1	1	0	1	1	0
1	1	0	1	0	0	1	1	1	0	1	1
1	1	1	X	X	X	X	X	X	X	X	X

Complete this transition table for the next state of each S-R flip-flop and the inputs for each S-R flip-flop to implement the prescribed count sequence. Do not change any headings or values typed into the table.

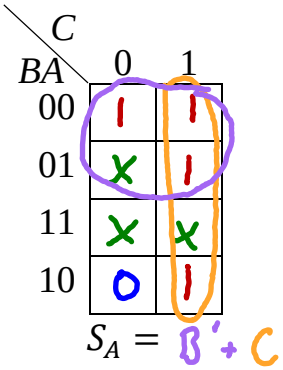
Complete these Karnaugh maps and determine the fully reduced sum of products expression for each of the flip flop inputs. Do not change any of the labels on the K-maps.



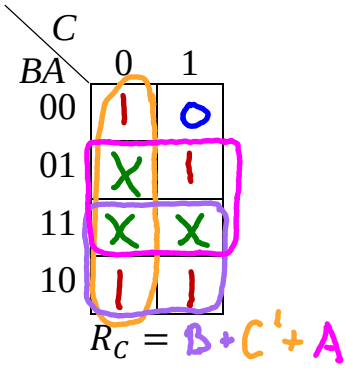
$S_C = B' + C$



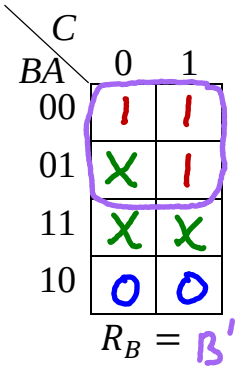
$S_B = B + A'C$



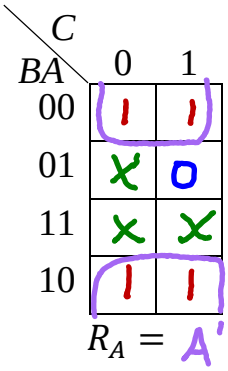
$S_A = B' + C$



$R_C = B + C' + A$



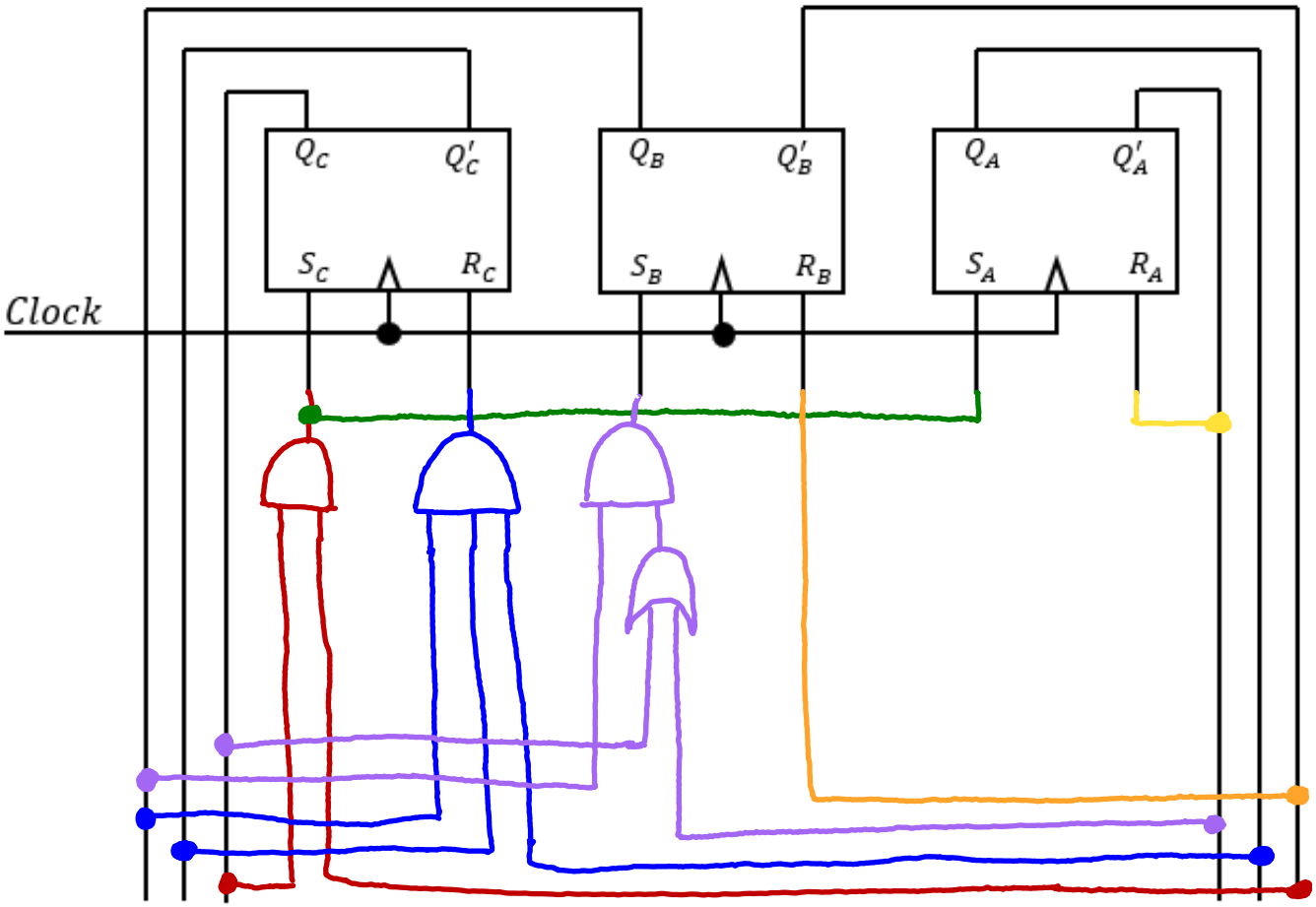
$R_B = B'$



$R_A = A'$

Use logic gates to complete this circuit drawing to implement the prescribed counter sequence.

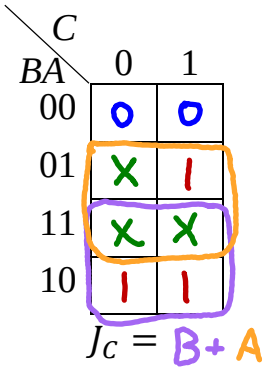
1 point of this part of the problem is reserved for having a minimal design. That is, a design that uses the fewest number of logic gates. In order to receive any of this point your circuit must implement the correct count sequence. Note that this part of the problem entails designing a multiple output logic circuit. You may be able to reduce the gate count by algebraically manipulating the SOP expressions into other forms.



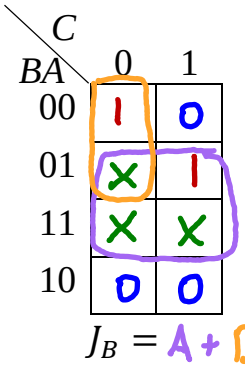
C	B	A	C^+	B^+	A^+	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	1	0	0	1	1	0	0	1
0	0	1	X	X	X	X	X	X	X	X	X
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	0	0	0	0	1	0	1	0	1
1	0	1	1	1	0	1	0	1	0	0	1
1	1	0	1	0	0	1	0	0	1	0	1
1	1	1	X	X	X	X	X	X	X	X	X

Complete this transition table for the next state of each J-K flip-flop and the inputs for each J-K flip-flop to implement the prescribed count sequence. Do not change any headings or values typed into the table.

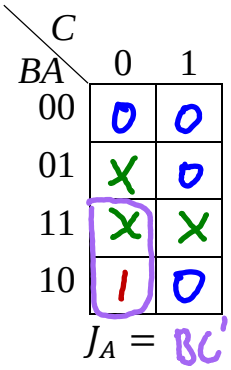
Complete these Karnaugh maps and determine the fully reduced sum of products expression for each of the flip flop inputs. Do not change any of the labels on the K-maps.



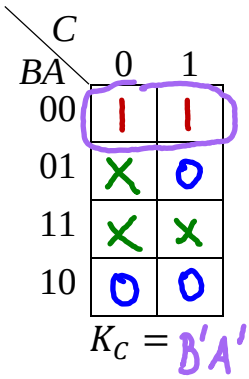
$J_C = B + A$



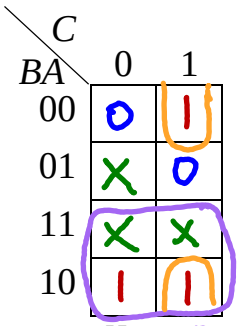
$J_B = A + B'C'$



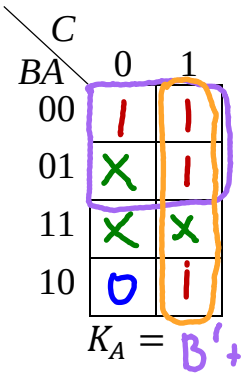
$J_A = BC'$



$K_C = B'A'$



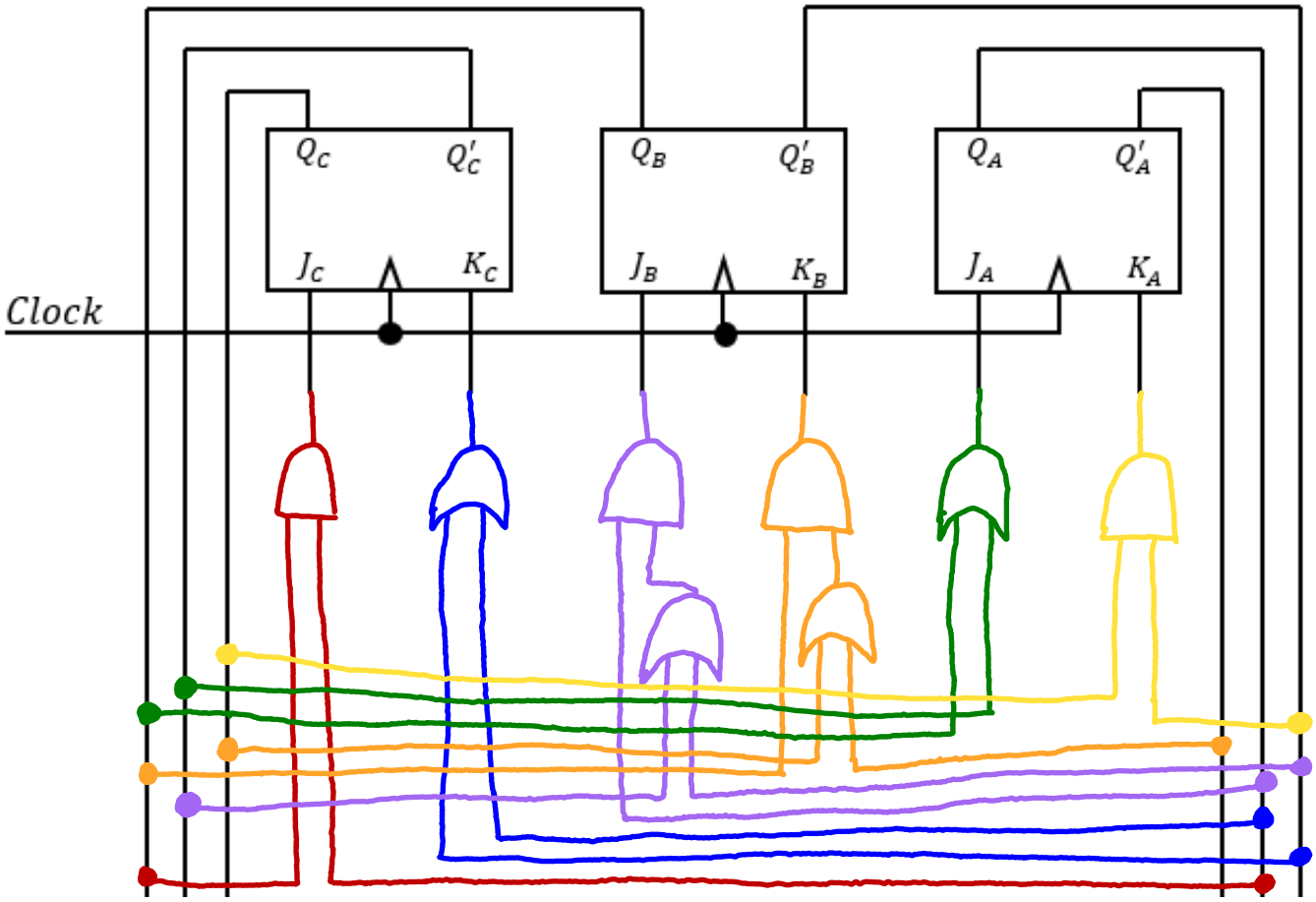
$K_B = B + A'C$



$K_A = B' + C$

Use logic gates to complete this circuit drawing to implement the prescribed counter sequence.

1 point of this part of the problem is reserved for having a minimal design. That is, a design that uses the fewest number of logic gates. In order to receive any of this point your circuit must implement the correct count sequence. Note that this part of the problem entails designing a multiple output logic circuit. You may be able to reduce the gate count by algebraically manipulating the SOP expressions into other forms.



Briefly comment on the similarities and/or differences between these two designs.

The SR latch is much more efficient, particularly on the B and A gates