The is a Mealy machine design problem. Note that difference from Homework Problem 13-3.

For this problem you are to design another sequence detector. Design constraints:

1. It must be a Mealy machine.
2. The sequence it must detect in a serial string of 1s and 0s at input Y is "100".
3. You may assume that the values arriving at input Y are properly synchronized with the clock.
4. The output must be $Z = 1$ when the prescribed sequence is detected, and 0 otherwise.
5. The circuit does not have to automatically reset when a 1 output occurs. (Return to initial state only when appropriate for sequence detection.)
6. You MUST not use more than two flip-flops in your design.
7. Name the flip-flops A and B. One of the objectives of this problem is for you to see, though comparison with HW 13-3, that the same operation can be completed with fewer states in a Mealy machine than in a Moore machine. Thus, you may not use more than three states for your design. However, since two flip-flops can realize four states you may use S_0 and any two of the other three, with these state-name definitions: S_0 $(AB = 00)$, S_1 $(AB = 01)$, S_2 $(AB = 10)$, S_3 $(AB = 11)$
8. Use S_0 for the initial state. It is up to you to decide what each of the other state-names mean with respect to the input sequence. Since you have some freedom of choice it is up to you to clearly articulate what each state-name means. See slide 6 of the 3/29 lecture, for example.
9. Logic must be implemented with no more than two levels and use only AND gates and OR gates (and a single inverter if you need to generate Y' from the Y input).

Please submit:

a) Your design for the State Graph, with documentation of what each State means (see item 8 above).

b) Corresponding State Table

c) Corresponding Transition Table

d) Corresponding flip-flop Next-State Maps and expressions derived therefrom.

e) Circuit diagram