ECE 3030 Spring 2025
HOMEWORK ASSIGNMENT NO. 9
DUE: Thursday, April 10th 11.59 pm SpeedGrader.

1. Assume that the JFET shown in Lecture 31, slide 7 is Si and has p^+ regions doped with 10^{18} acceptors/cm^3 and a channel with 10^{16} donors/cm^3. The channel half-width *a* is 1 um. Calculate the pinch-off voltage V_P and the built-in voltage V_{bi}, that is, the contact potential V_0. What voltage V_{GD} is required to cause pinch-off when V_o is included? Note: $-V_{GD}$ (pinch-off) is defined as the "threshold voltage" V_T. With V_G = -3 V, at what value of V_D does the current saturate? [Hint: New Gate Voltage $V_G \rightarrow V_G - V_0$]

2. If the ratio Z/L = 10 for the JFET of Problem 1 and μ_n = 1000 cm^2/V-s, calculate $I_D(sat)$ for V_G = 0, -2, -4, and –6 V. Plot $I_D(sat)$ vs. $V_D(sat)$.

3. For the JFET of Problem 2, plot I_D vs. V_D for the same four values of V_G. Terminate each plot at the point of saturation.

4. (Extra Credit: 15 Points) Use the expressions for I_D and I_D(sat.) on slides 10 and 11 of Lecture 31 respectively to calculate and plot ($I_D(V_D,V_G)$ at 300 K for a Si JFET with a = 1000 Å, $N_D = 7 \times 10^{17}$ cm^{-3}, Z = 100 μm , and L = 5 μm. Allow V_D to range from 0 to 5 V, and allow V_G to take on the values 0, -1, -2, -3, -4, and -5 V.

5. Find the maximum depletion width, minimum capacitance C_i, and threshold voltage for an *ideal* MOS capacitor with a 10-nm gate oxide (SiO_2) on p-type Si with $N_a = 10^{16}$ cm^{-3}.

6. (Extra Credit: 15 Points) An Al-gate p-channel MOS transistor is made on an n-type Si substrate with $N_d = 5 \times 10^{17}$ cm^{-3}. The SiO_2 thickness is 100 Å in the gate region, and the effective interface charge Q_i is 5×10^{10} qC/cm^2.
   (a) Find W_m, V_{FB}, and V_T.
   (b) Sketch the C-V curve for this device and give important numbers for the scale.