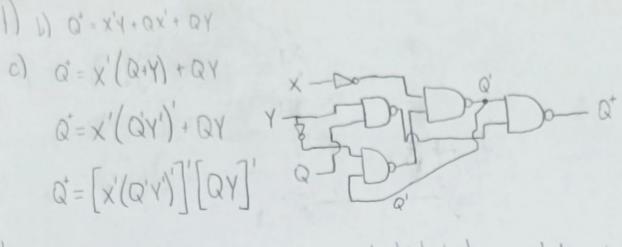
Homework 01: Latches and Flip-Flops

Solve the four following problems. Show all your work/process. Please neatly write or type your answers, and please scan or upload your answers in a single PDF file to the assignment submission on Carmen. Answers may be graded for correctness, thoroughness, completion, or some combination.

- 1.1 An XY latch has two inputs X and Y, and one state variable Q. It operates as follows: *
 - If X = Y, the latch state does not change $(Q^+ = Q)$.
 - If X = 0 and Y = 1, the latch state becomes $1(Q^+ = 1)$.
 - If X = 1 and Y = 0, the latch state becomes 0 ($Q^+ = 0$).
 - a. Construct the state table for this XY latch. Circle the stable states.
 - b. Derive the characteristic equation (next-state equation) for this XY latch. O = XY + QX + QY



d) No because each transition with potential between-states has only predictable outputs for those between states

00 = 11 always between state of

Yes because going from 00 to 11 could either have a between state of 01 or 10, which results in 1 or 0.

e) Output of [x'(Q'Y')] because it determines

 $\frac{N_0}{2}$ Q = ((AB)'P)'

	P		AB	
()	00	0 01	11	10 D
4	111	101	OK	1

4)	p+		AB		
0/		001	011	11	10
	00	X	X	X	X
	0001	1	1)	X	
	01 11	X	X	0	X
	10	11	0	10)	1

C) No, because the stable states define a path for each transition so they are all stable.

d) No, because ABQP = 0010 outputs P=1 = 1010 outputs P=1

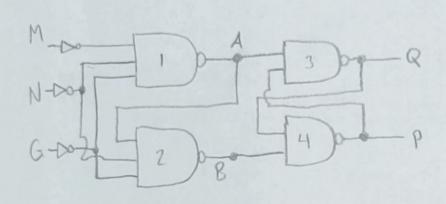
both of which Q'=0

3) a) on spreadsheet

b) No, but only when B=1, which looks P next into being 0, even when Q=0

c) on spreadsheet

 $A = (M+N+G)' \rightarrow ((M'N')+G)' \rightarrow (((M'N')G')')' \rightarrow A = M'N'G' = (MNG)'$ $B = (A+N+G)' \rightarrow ((A'N')+G)' \rightarrow (((A'N)G')')' \rightarrow B = A'N'G' = (ANG)'$ $Q = (A+P)' \rightarrow Q = A'P' = (AP)'$ $P = (B+Q)' \rightarrow P = B'Q' = (BQ)'$



3a								
					Α	В	Q	P Next
	M	N	G	Р	!(M+N+G)	!(A+N+G)	!(A+P)	!(Q+B)
	0	0	0	0	1	0	0	1
	0	0	0	1	1	0	0	1
	0	0	1	0	0	0	1	0
	0	0	1	1	0	0	0	1
	0	1	0	0	0	0	1	0
	0	1	0	1	0	0	0	1
	0	1	1	0	0	0	1	0
	0	1	1	1	0	0	0	1
	1	0	0	0	0	1	1	0
	1	0	0	1	0	1	0	0
	1	0	1	0	0	0	1	0
	1	0	1	1	0	0	0	1
	1	1	0	0	0	0	1	0
	1	1	0	1	0	0	0	1
	1	1	1	0	0	0	1	0
	1	1	1	1	0	0	0	1



1.4 Complete the following timing diagram for the rising-edge-triggered D flip-flop shown in Figure 3. Assume Q begins at 1. Make sure any propagation delays are clear on your diagram.

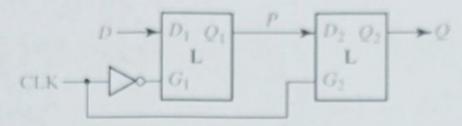


Figure 3: Rising-edge-triggered controller-responder D flip-flop circuit.

