1

Branch_if_[R5]=[R6] LOOP

	Stage 2	Stage 3	Stage 4	Stage 5
RA	20	20	20	20
RB	X	15	15	15
RZ	X	X	0	0
RY	X	X	X	0
PC	2000	2000	2000	2004

Call_Register R6

	Stage 2	Stage 3	Stage 4	Stage 5
RA	15	15	15	15
RB	X	X	X	X
RZ	X	15	15	15
RY	X	X	15	15
PC	2004	2004	2004	15

2

	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7	Cycle 8
IR	Subtract	Store	Branch R5>R4	Misprediction	Subtract	Store	Branch R5>	Subtract
PC	804	808	800		804	808	800	804
RA	1	60	70		1	60	70	1
RB	50	10	10		70	10	10	70
RZ	49	70	X		69	70	X	69
RY	49	70	800		69	70	800	69
R6	49	49	49		69	69	69	69
R5	50	70	70		70	70	70	70
R4	10	10	10		10	10	10	10

Cycle 9
Store
808
60
10
70
70
69
70
10

3

a. direct mapped cache

Block	1st Pass
0	0x2E0->0x208->0x190->0x2E0->0x338
4	0x2E4->0x20C->0x194->0x2E4->0x33C->0x1AC->0x194
	2nd Pass
0	0x338->0x2E0->0x208->0x190->0x2E0->0x338
4	0x194->0x2E4->0x20C->0x194->0x2E4->0x33C->0x1AC->0x194
	3rd Pass
0	0x338->0x2E0->0x208->0x190->0x2E0->0x338
4	0x194->0x2E4->0x20C->0x194->0x2E4->0x33C->0x1AC->0x194
	4th Pass
0	0x338->0x2E0->0x208->0x190->0x2E0->0x338
4	0x194->0x2E4->0x20C->0x194->0x2E4->0x33C->0x1AC->0x194

hit	0
miss	48

ratio 0

b. associative mapped cache

Block	1st Pass	2nd Pass	3rd Pass	4th Pass
0	0x2E0	0x2E0	0x2E0	0x2E0
1	0x2E4	0x2E4	0x2E4	0x2E4
2	0x208->0x1AC	0x1AC->0x33C	0x33C->0x338	0x338
3	0x20C	0x20C->0x208->0x1AC	0x1AC->0x33C	0x33C
4	0x194	0x194	0x194	0x194
5	0x190	0x190->0x20C	0x20C->0x208->0x1AC	0x1AC
6	0x338	0x338->0x190	0x190->0x20C	0x20C->0x208->0x1AC
7	0x33C	0x33C->0x338	0x338->0x190	0x190

hit	3	6	6	6
miss	9	6	6	6

ratio 4/9

c. 2 way set associative mapped cache

	Block	1st Pass
0	0	0x2E0->0x208->0x194->0x2E0->0x338->0x1AC
	1	0x2E4->0x20C->0x190->0x2E4->0x33C->0x194
		2nd Pass
0	0	0x1AC->0x2E0->0x208->0x194->0x2E0->0x338->0x1AC

1 0x194->0x2E4->0x20C->0x190->0x2E4->0x33C->0x194
3rd Pass
0 0 0x1AC->0x2E0->0x208->0x194->0x2E0->0x338->0x1AC
1 0x194->0x2E4->0x20C->0x190->0x2E4->0x33C->0x194
4th Pass
0 0 0x1AC->0x2E0->0x208->0x194->0x2E0->0x338->0x1AC
1 0x194->0x2E4->0x20C->0x190->0x2E4->0x33C->0x194

hit 0
miss 48

ratio 0

d. 2 way set associative mapped cache - 2 words per block

Block 1st Pass
0 0 0x2E0->0x194->0x338
0x2E4->0x190->0x33C
1 0x208->0x2E0->0x1AC
0x20C->0x2E4->0x194
2nd Pass
0 0 0x338->0x2E0->0x194->0x338
0x33C->0x2E4->0x190->0x33C
1 0x1AC->0x208->0x2E0->0x1AC
0x194->0x20C->0x2E4->0x194
3rd Pass
0 0 0x338->0x2E0->0x194->0x338
0x33C->0x2E4->0x190->0x33C
1 0x1AC->0x208->0x2E0->0x1AC
0x194->0x20C->0x2E4->0x194
4th Pass
0 0 0x338->0x2E0->0x194->0x338
0x33C->0x2E4->0x190->0x33C
1 0x1AC->0x208->0x2E0->0x1AC
0x194->0x20C->0x2E4->0x194

hit 0
miss 48

ratio 0

Addr. (12)	0x2E0	0x2E4	0x208	0x20C	0x194	0x190	0x2E0	0x2E4	0x338	0x33C	0x1AC	0x194
decimal	736	740	520	524	404	400	736	740	824	828	428	404
mod 8	0	4	0	4	4	0	0	4	0	4	4	4
mod 4	0	0	0	0	0	0	0	0	0	0	0	0