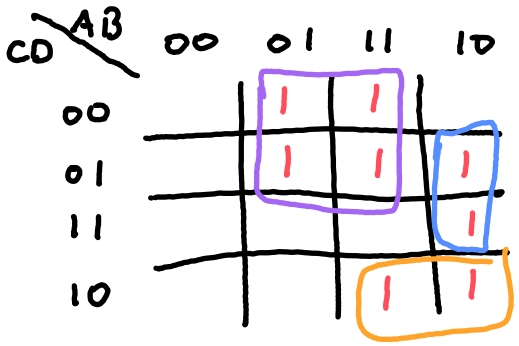
Draw a logic circuit that uses only 2-input NAND gates to implement the following function. Your circuit must use the minimum number of 2-input NAND gates. Since you are limited to only 2-input NAND gates you may need to use more than two levels of logic.

$$F(A,B,C,D) = ABCD' + ABC' + AB'C'D + A'BC' + AB'C$$

For this problem the output of the previous block of the system has each of A, A', B, B', C, C', D and D' available as inputs to your circuit on the wires that are shown below.

Note that the problems specifies that you use only 2-input NAND gates. If your design requires inverters (NOT gates), then you must implement them using 2-input NAND gates, and they count in the total number of gates you used.



$BC' + AB'D + ACD'$

$(BC' + (AB')(D) + (AC)D'$