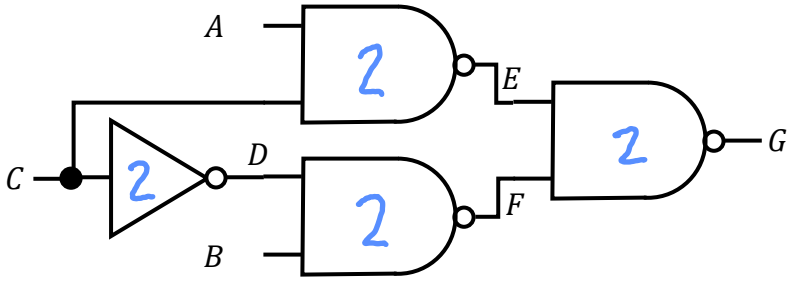
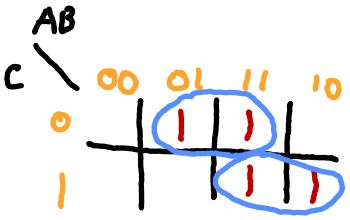


In this problem inverters have a propagation delay of 2 ns, 2-input gates have a propagation delay of 2 ns, and 3-input gates have a propagation delay of 6 ns.

The vertical lines in the timing diagrams indicate 2 ns increments in time.

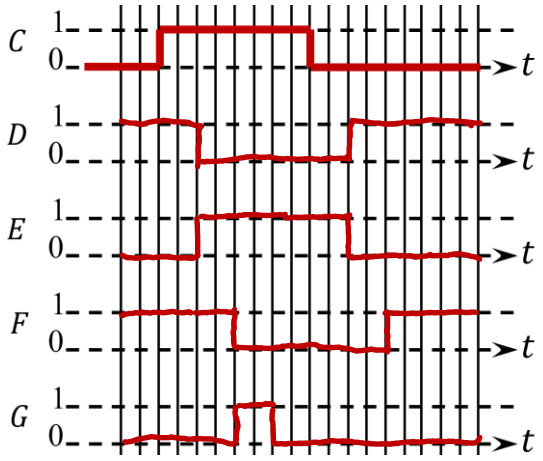
a) Determine the SOP expression for $G(A,B,C)$ in the circuit above. Complete a K-map and use it in your analysis of this circuit for potential static-1 hazards. Explain the details of your findings.

$AC + BC'$

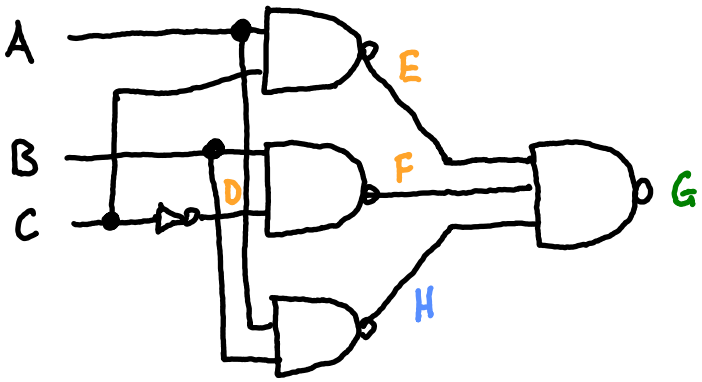


b) Complete the following timing diagram for this circuit with $A = B = 1$. If any potential static-1 hazards found in part a) have produced any glitches in the output then circle the glitches in your timing diagram. If there were no glitches, explicitly say so here.

No glitches



c) Add another NAND gate to the circuit to address the potential static-1 hazard. Draw the new circuit, and label the output of the new NAND gate "H".



d) Complete the timing diagram for your new circuit with $A = B = 1$. Circle any glitches in the output. If there were no glitches, explicitly say so here.

No glitches