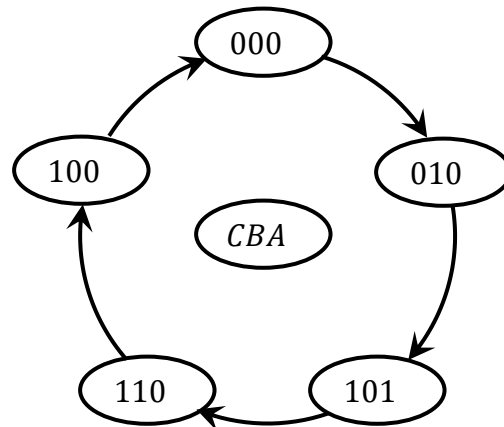The final goal of this problem is design of a three-bit synchronous counter circuit using T flip-flops, to implement the count sequence shown in the adjacent transition graph.

Complete this transition table for the next state of each flip-flop (C^+, B^+, A^+) and the input for each flip-flop (T_C, T_B, T_A) to implement the prescribed count sequence. Do not change any headings or values typed into the table.

C	B	A	C^+	B^+	A^+	T_C	T_B	T_A
0	0	0	0	1	0	0	1	0
0	0	1	X	X	X	X	X	X
0	1	0	1	0	1	1	1	1
0	1	1	X	X	X	X	X	X
1	0	0	0	0	0	1	0	0
1	0	1	1	1	0	0	1	1
1	1	0	1	0	0	0	1	0
1	1	1	X	X	X	X	X	X

Complete these Karnaugh maps and determine the fully reduced sum of products expression for each of the flip flop inputs. Do not change any of the labels on the K-maps.

T_C map (C across: 0, 1; BA down):

BA \ C	0	1
00	0	1
01	X	0
11	X	X
10	1	0

$$T_C = A'B'C + BC'$$

T_B map (C across: 0, 1; BA down):

BA \ C	0	1
00	1	0
01	X	1
11	X	X
10	1	1

$$T_B = B + AB' + C'$$

T_A map (C across: 0, 1; BA down):

BA \ C	0	1
00	0	0
01	X	1
11	X	X
10	1	0

$$T_A = BC' + A$$

Continued on next page

Use logic gates to complete this circuit drawing to implement the prescribed counter sequence.

1 point of this part of the problem is reserved for having a minimal design. That is, a design that uses the fewest number of logic gates. In order to receive any of this point your circuit must implement the correct count sequence. Note that this part of the problem entails designing a multiple output logic circuit. You may be able to reduce the gate count by algebraically manipulating the SOP expressions into other forms.