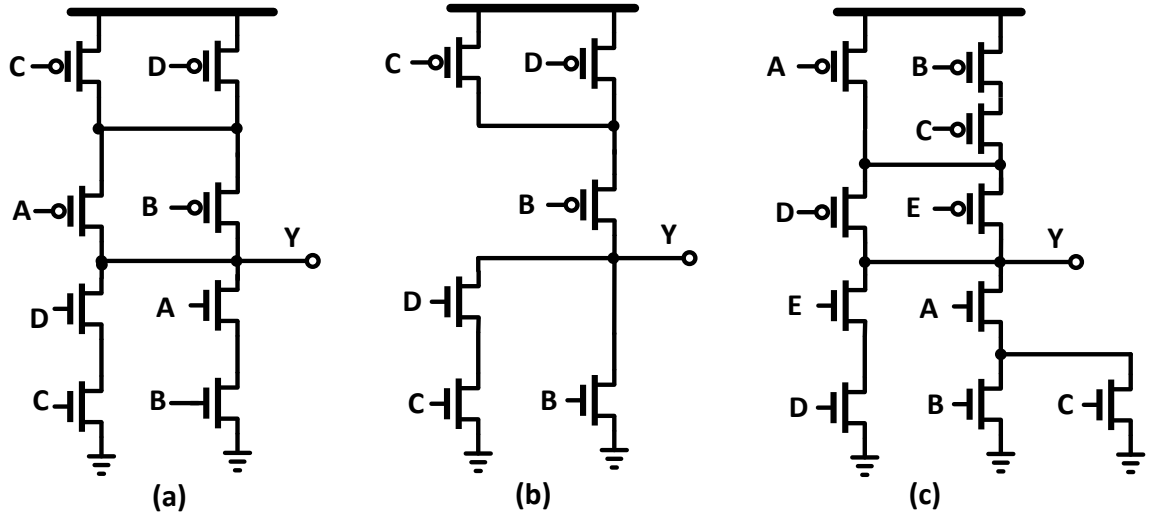
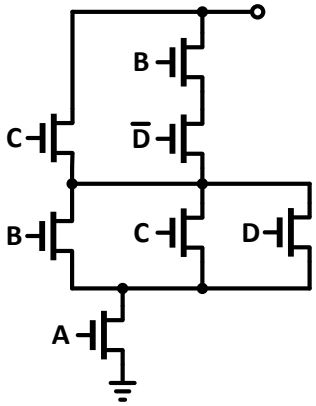
Autumn 2024 – ECE 5020
Homework 3

Due: 09/25/2024

1. For the following schematics
   i. Write Y in terms of the inputs (What logic function does it perform?)
   ii. Size the schematics to have same drive strength as a 2/1 inverter.
   iii. Show how they could be constructed with just INV, NAND and NOR gates (logic construction before you took ECE 5020).



2. Consider the pulldown network.
   a. What logic function does it perform?
   b. Construct its pull up (dual) network.
   c. Size it to have same drive strength as a 2/1 inverter.



3. Construct a static complementary CMOS logic for the following expressions.

(a) $Y = \overline{A}+B + (S+C)D + R(\overline{C}+\overline{D})$

(b) $Y = \overline{A(B+C)+BAC}$

(c) $Y = \overline{ABC(D+E) + C(B+A)}$