Homework 01: Latches and Flip-Flops

Solve the **four** following problems. Show all your work/process. Please neatly write or type your answers, and please scan or upload your answers in a single PDF file to the assignment submission on Carmen. Answers may be graded for correctness, thoroughness, completion, or some combination.

1.1 An XY latch has two inputs X and Y, and one state variable Q. It operates as follows:

- If $X = Y$, the latch state does not change ($Q^+ = Q$).
- If $X = 0$ and $Y = 1$, the latch state becomes 1 ($Q^+ = 1$).
- If $X = 1$ and $Y = 0$, the latch state becomes 0 ($Q^+ = 0$).

a. Construct the state table for this XY latch. Circle the stable states.

b. Derive the characteristic equation (next-state equation) for this XY latch.

c. Derive a circuit for this XY latch which has only four two-input NAND gates and two inverters. Draw the circuit.

d. Are there any transitions between input combinations which might cause unreliable operation for this XY latch? If so, which transitions? Explain and verify your answer.

e. In your circuit of part (c), is there a gate output which is usable as the complement of Q? If so, which output? (You can label it on your circuit and refer to the label.) Explain and verify your answer.

1.2 Figure 1 shows an AB latch circuit with two inputs A and B, one state variable Q, and another output P.

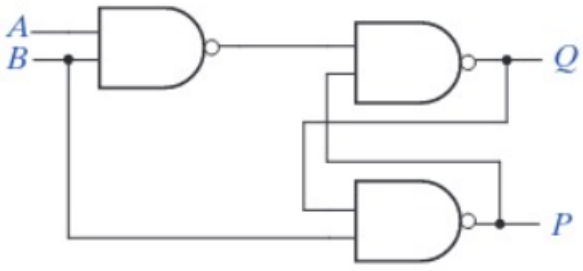

Figure 1: AB latch with state Q and output P.

a. Derive the characteristic equation (next-state equation) for this AB latch. The equation should be in terms of only the present state Q and the inputs A and B.

b. Construct the state table for this AB latch. Circle the stable states.

c. Are there any transitions between input combinations which might cause unreliable operation for this AB latch? If so, which transitions? Explain and verify your answer.

d. Is the output P usable as the complement of Q? Explain and verify your answer.

1.3 Figure 2 shows a gated latch circuit with gate signal G, two other inputs M and N, one state variable Q, another output P, and two labeled intermediate gate outputs A and B.

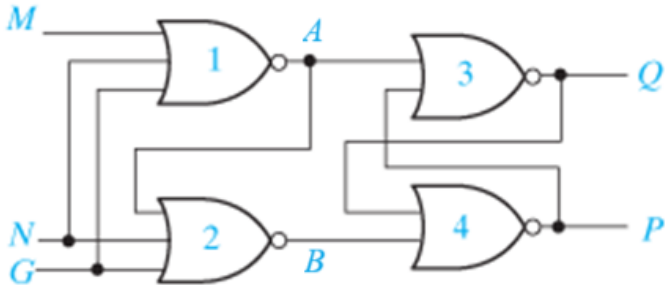

Figure 2: Gated latch with gate input G, other inputs M and N, intermediate outputs A and B, state Q, and output P.

a. Construct a truth table for this circuit with every combination of values for G, M, N, and Q. Include columns for the intermediate outputs A and B, the output P, and the next state Q^+. From this truth table, construct a K-map and derive the next-state equation for this circuit. The equation should be in terms of only the present state Q and the inputs G, M, and N.

b. Is the output P usable as the complement of Q? Verify your answer.

c. For the Figure 2 circuit, assume that Gate 1 has a propagation delay of 30 ns and Gates 2, 3, and 4 have propagation delays of 10 ns. Construct a timing diagram for the circuit for the following situation:

- Initial conditions at time 0 ns: $M = N = Q = 0, G = 1$
- Input change at time 10 ns: G changes from 1 to 0

Show signals for G, M, N, A, B, P, and Q on the timing diagram.

d. Derive a circuit for this gated latch which has only four NAND gates (either two-input or three-input) and three inverters. Draw the circuit.

1.4 Complete the following timing diagram for the rising-edge-triggered D flip-flop shown in Figure 3. Assume Q begins at 1. Make sure any propagation delays are clear on your diagram.

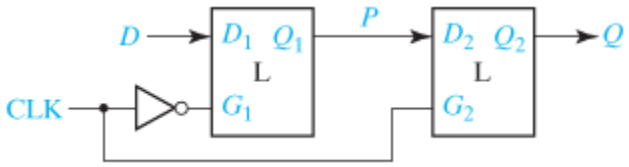

Figure 3: Rising-edge-triggered controller-responder D flip-flop circuit.