



Lecture Outline

Reminders to self:

- ☐ Turn on lecture recording to Cloud
- ☐ Turn on Zoom microphone

- Last Lecture

- Finished Shift Registers
- Started Counters
 - Three-bit synchronous binary counter
 - Brief look at binary ripple counter (not synchronous)
 - Formal design procedures

- Today's Lecture

- Review HW 11-1
- Continue Counters
 - Other count sequences
 - Counter design with other types of flip-flops (D first)
 - Up and Down counter



Handouts and Announcements

- Announcements
 - Homework Problems 12-2 and 12-3
 - Posted on Carmen this morning
 - Due: 11:59pm Thursday 3/9
 - Homework Reminder
 - HW 12-1 posted on Carmen 3/1
 - Due: 11:25am Wednesday 3/8
 - Read for Monday: No new reading assignment
Previous assignment was pages 395-402
 - Mini-Exam 3 regrade continuing
 - A-some C regraded
 - W-Z regraded



Handouts and Announcements

- Announcements

- Mini-Exam 4 Reminder

- Available 5pm Monday 3/6 through 5:00pm Tuesday 3/7
- Due in Carmen PROMPTLY at 5:00pm on 3/7
- Designed to be completed in ~36 min, but you may use more
- When planning your schedule:
 - I recommend building in 10-15 min extra
 - To allow for downloading exam, signing and dating honor pledge, saving solution as pdf, and uploading to Carmen
- I also recommend not procrastinating

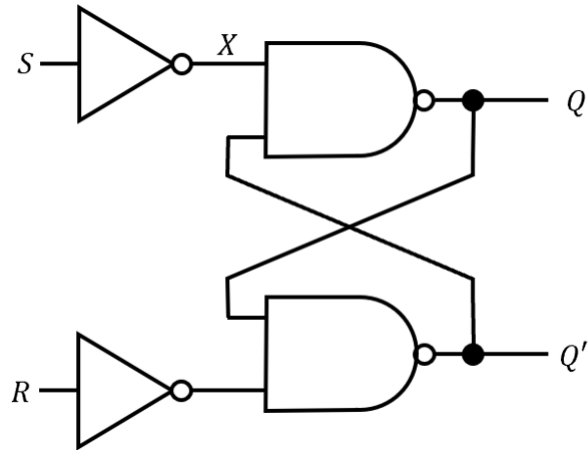
- Exam review topics available on Carmen

- Sample Mini-Exams 5 and 6 from Au20 also available



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Homework 11-1



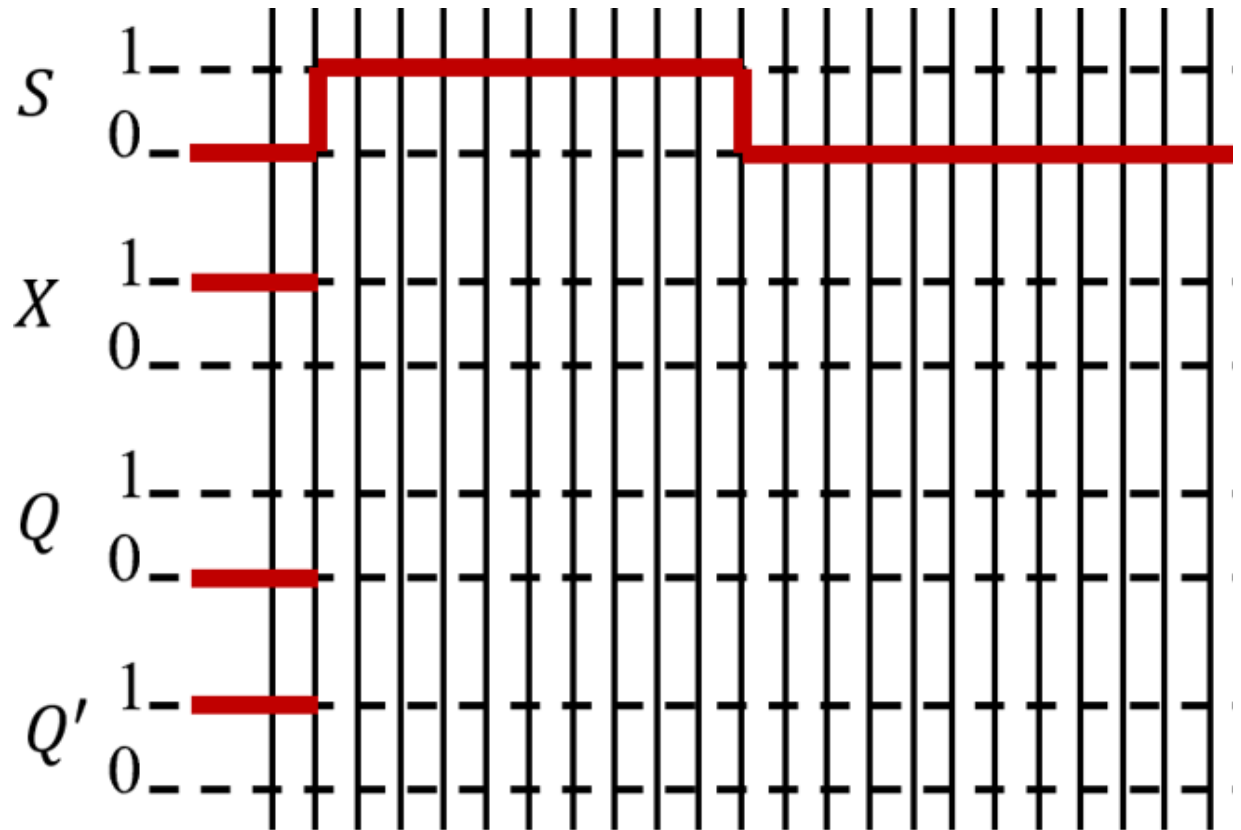
The inverters have a propagation delay of 3 ns.

The two-input NAND gates have a propagation delay of 4 ns.

Complete the timing diagrams for each of the input pulses shown for Part a) and Part b).

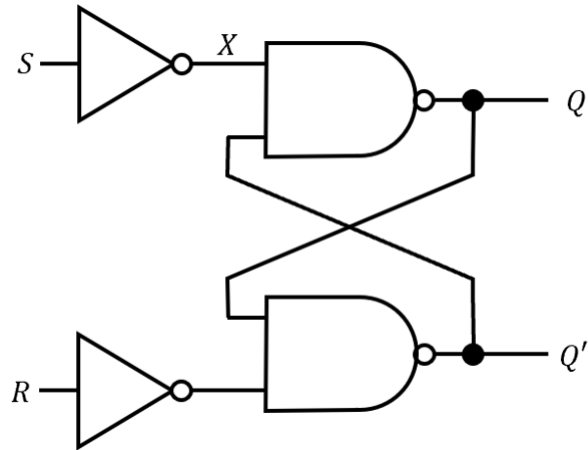
The vertical lines are spaced 1 ns apart.

The reset input has $R = 0$ at all times in this problem.





Homework 11-1



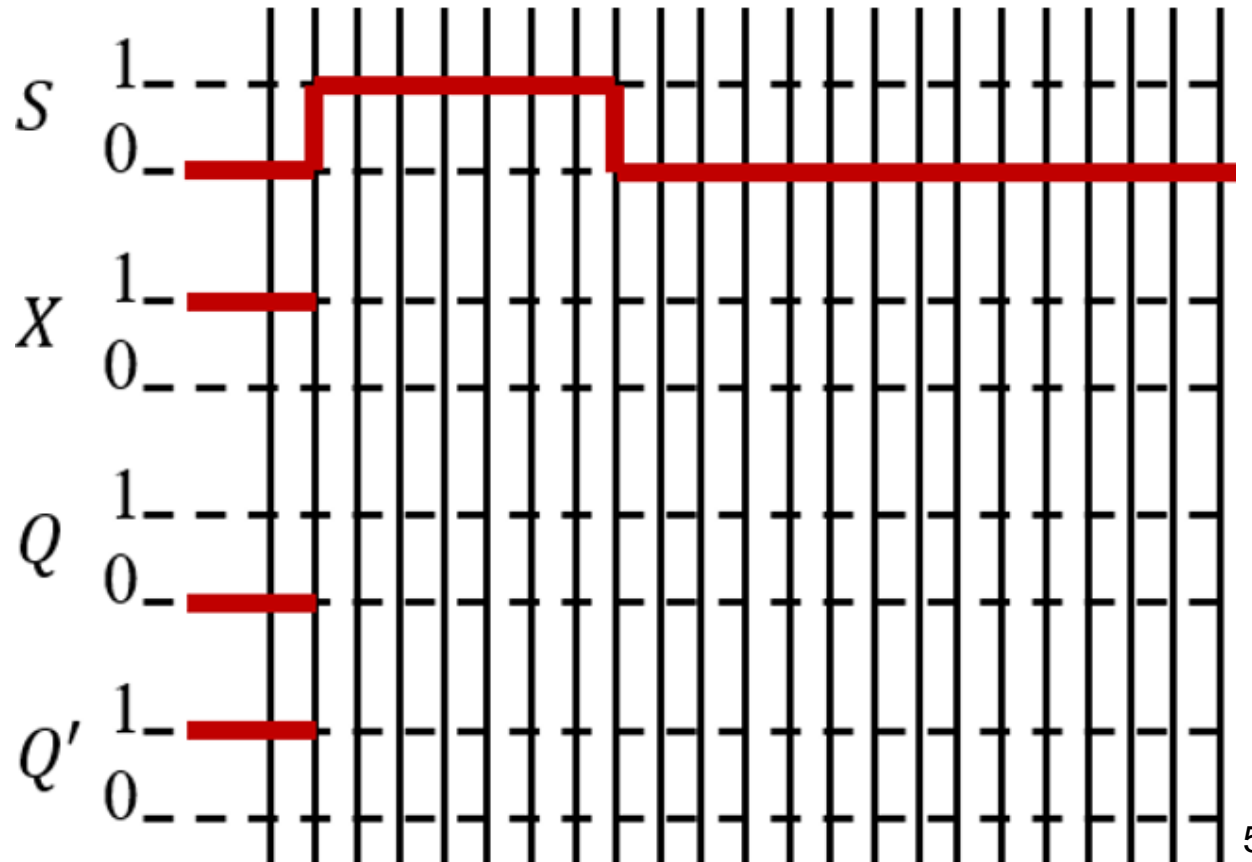
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The two-input NAND gates have a propagation delay of 4 ns.

Complete the timing diagrams for each of the input pulses shown for Part a) and Part b).

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The reset input has $R = 0$ at all times in this problem.





Counters

- Implementation of the 3-bit binary counter using D flip-flops: $Q^+ = D$
- $D_A = A^+$; $D_B = B^+$; $D_C = C^+$
- Inspecting the transition table to fill the K-maps

$BA \backslash C$	0	1
00	1	1
01	0	0
11	0	0
10	1	1

$BA \backslash C$	0	1
00	0	0
01	1	1
11	0	0
10	1	1

$$D_B = AB' + A'B \\ = A \oplus B$$

$$D_C = A'C + B'C + ABC' \\ = C(A' + B') + ABC' \\ = C(AB)' + C'(AB) \\ = C \oplus AB$$

$BA \backslash C$	0	1
00	0	1
01	0	1
11	1	0
10	0	1

Present State			Next State		
C	B	A	C^+	B^+	A^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0



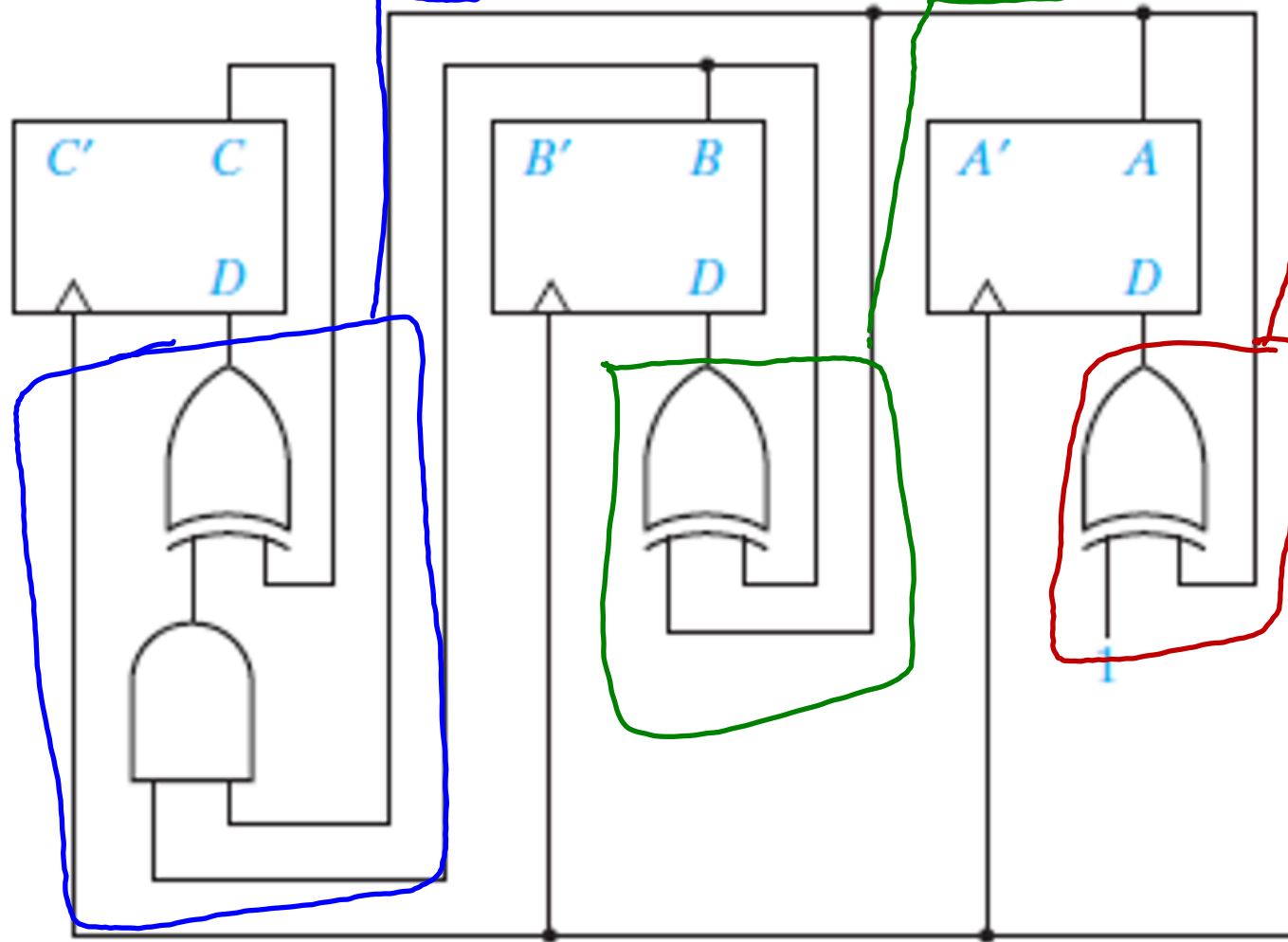
Counters

- Implementation of the 3-bit binary counter using D flip-flops

$$D_C = C \oplus AB;$$

$$D_B = A \oplus B;$$

$$D_A = A' = A \oplus 1$$



- This figure from textbook uses same XOR input structure to D_A as for D_B and D_C to invert A
- An inverter could be used instead
- On the A' output of the flip flop
- See last paragraph of Section 11.7 for conversion of D flip-flop to T flip-flop using XOR



Counters

4-bit BCD counter using T flip-flops

D	C	B	A	D ⁺	C ⁺	B ⁺	A ⁺	T _D	T _C	T _B	T _A
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1
1	0	1	0	-	-	-	-	X	X	X	X
1	0	1	1	-	-	-	-	X	X	X	X
1	1	0	0	-	-	-	-	X	X	X	X
1	1	0	1	-	-	-	-	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X

Remember the requirement for counters with T flip-flops from last lecture:

$T = 1$ whenever next state is different from current state

$$T_A(D, C, B, A) = 1$$

$$T_B(D, C, B, A) = \sum m(1, 3, 5, 7) + \sum d(10, 11, 12, 13, 14, 15)$$

$$T_C(D, C, B, A) = \sum m(3, 7) + \sum d(10, 11, 12, 13, 14, 15)$$

$$T_D(D, C, B, A) = \sum m(7, 9) + \sum d(10, 11, 12, 13, 14, 15)$$



4-bit BCD counter using T flip-flops

$$T_A(D, C, B, A) = 1$$

$$T_B(D, C, B, A) = \sum m(1, 3, 5, 7) + \sum d(10, 11, 12, 13, 14, 15)$$

$$T_C(D, C, B, A) = \sum m(3, 7) + \sum d(10, 11, 12, 13, 14, 15)$$

$$T_D(D, C, B, A) = \sum m(7, 9) + \sum d(10, 11, 12, 13, 14, 15)$$

T_D

	00	01	11	10
00	m_0		X	
01	m_1		X	i
11	etc	1	X	X
10	m_2		X	X

$$T_D = AD + ABC$$



Counters

Hw 12-3

4-bit BCD counter using T flip-flops

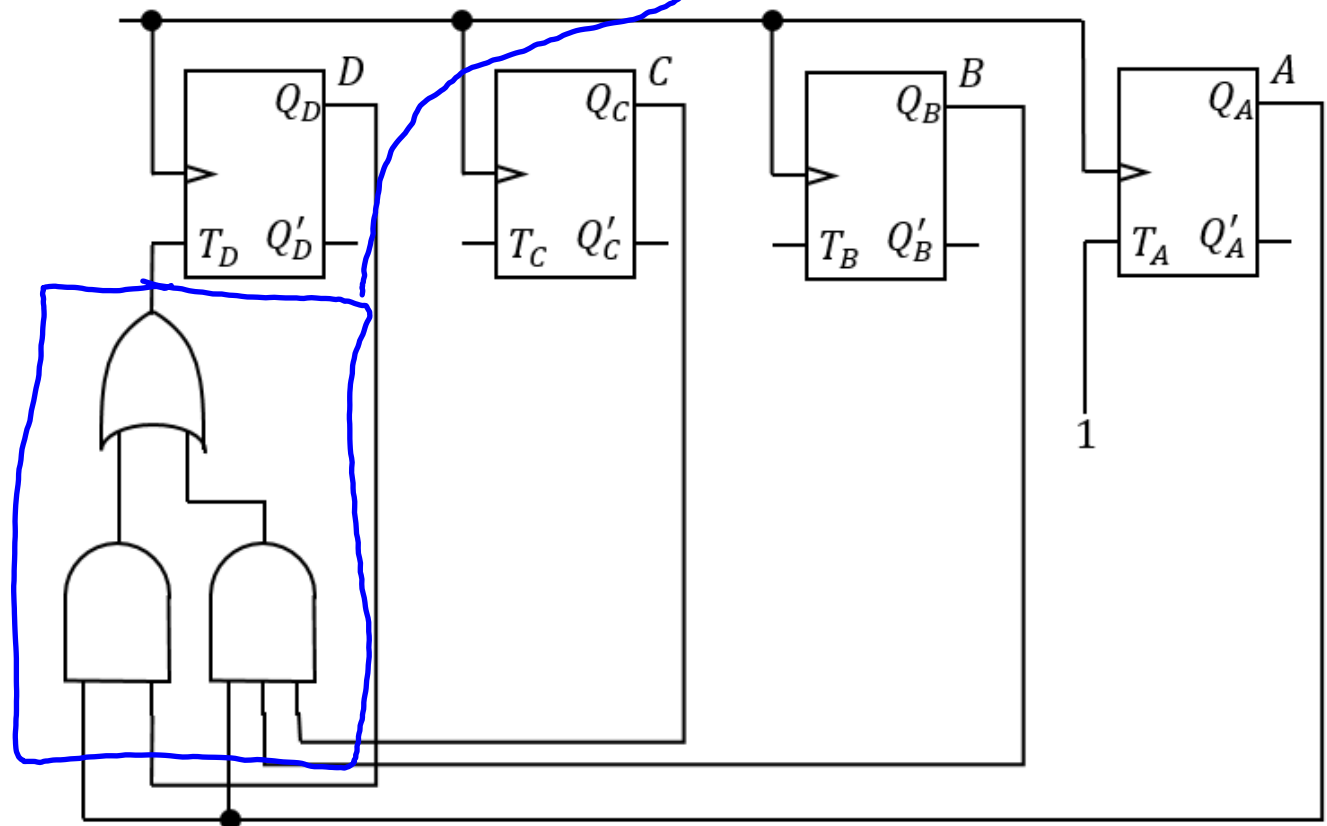
$$T_A(D, C, B, A) = 1$$

$$T_B(D, C, B, A) = \sum m(1, 3, 5, 7) + \sum d(10, 11, 12, 13, 14, 15)$$

$$T_C(D, C, B, A) = \sum m(3, 7) + \sum d(10, 11, 12, 13, 14, 15)$$

$$T_D(D, C, B, A) = \sum m(7, 9) + \sum d(10, 11, 12, 13, 14, 15) = AD + ABC$$

The design of
the rest of this
BCD counter
is left as
homework



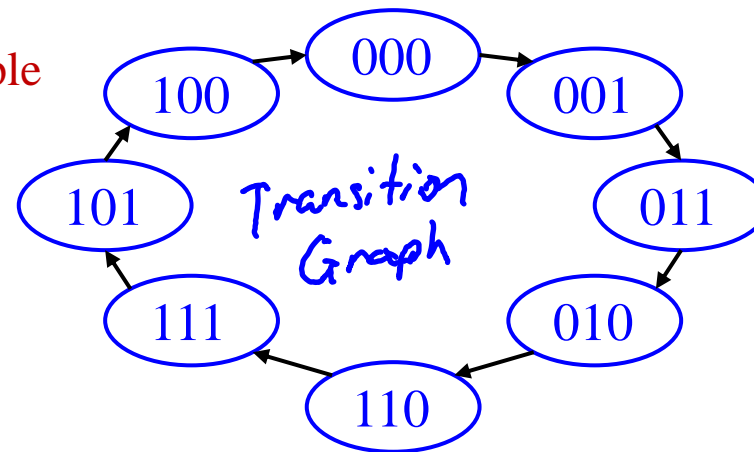


Counters

3-bit Gray-Code counter using T flip-flops

Count sequence does not have to be straight binary: Gray-Code as an example

C	B	A	C ⁺	B ⁺	A ⁺	T _C	T _B	T _A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	0	0
0	1	1	0	1	0	0	0	1
1	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1
1	1	0	1	1	1	0	0	1
1	1	1	1	0	1	0	1	0



$$T_A(C, B, A) = \sum m(0, 3, 5, 6)$$

$$T_B(C, B, A) = \sum m(1, 7)$$

$$T_C(C, B, A) = \sum m(2, 4)$$



Counters

$$T_A(C, B, A) = \sum m(0, 3, 5, 6)$$

$$T_B(C, B, A) = \sum m(1, 7)$$

$$T_C(C, B, A) = \sum m(2, 4)$$

$BA \backslash C$		0	1
00	1		
01			1
11	1		
10			1

- Note that each of the 8 minterms appears exactly once.
- No Reduction for SOP form
- But do you see the useful pattern?

$BA \backslash C$		0	1
00			
01	1		
11			1
10			

$BA \backslash C$		0	1
00			1
01			
11			
10	1		

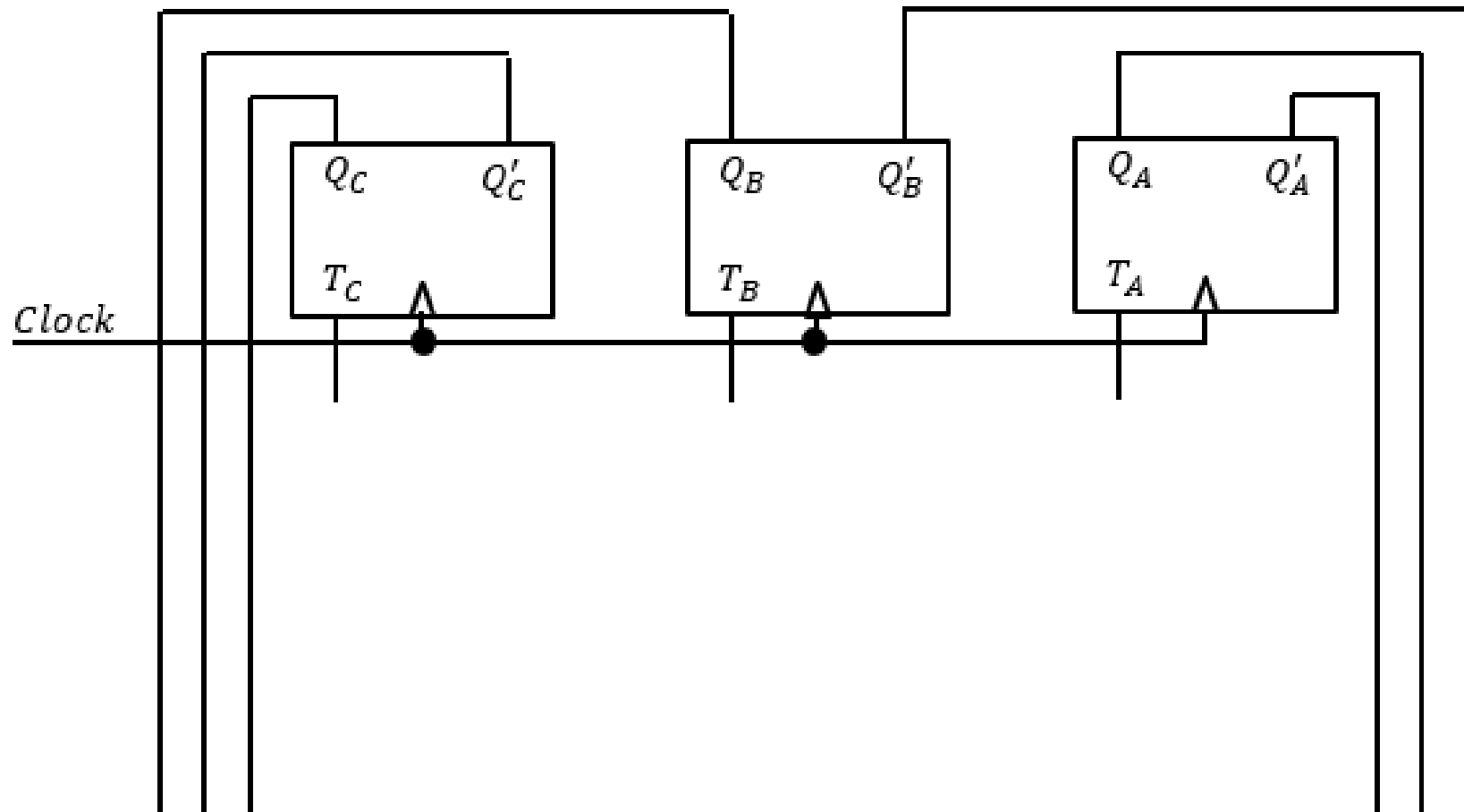


Counters

$$T_C = C'BA' + CB'A'$$

$$T_B = C'B'A + CBA$$

$$T_A = C'B'A' + C'BA + CB'A + CBA'$$





Counters

3-bit Binary Up-Down counter using D flip-flops

Bi-directional Transition Graph

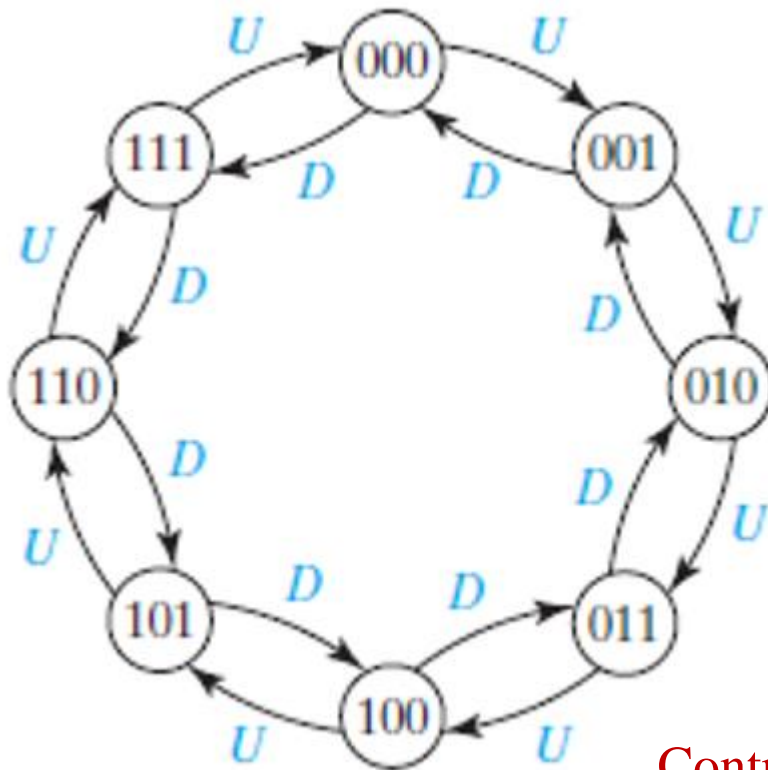


Table of Present and Next States for both directions

CBA	$C^+B^+A^+$	
	U	D
000	001	111
001	010	000
010	011	001
011	100	010
100	101	011
101	110	100
110	111	101
111	000	110

Control Bits U and D

- $U = D = 0 \Rightarrow$
- $U = 1; D = 0 \Rightarrow$
- $U = 0; D = 1 \Rightarrow$
- $U = D = 1 \Rightarrow$ **not allowed**



Counters

3-bit Binary Up-Down counter using D flip-flops

CBA	$C^+ B^+ A^+$	
	U	D
000	001	111
001	010	000
010	011	001
011	100	010
100	101	011
101	110	100
110	111	101
111	000	110

Next state of A is A' either Up or Down

$$D_A = A^+ = A \oplus (U + D)$$

$$D_B = B^+ = B \oplus (UA + DA')$$

$$D_C = C^+ = C \oplus (UAB + DA'B')$$

When $U = 1, D = 0$ these equations reduce to the same expressions on slides 6 & 7

When $U = 0, D = 1$ these equations reduce to

$$D_A = A^+ = A \oplus 1 = A'$$

$$D_B = B^+ = B \oplus A'$$

$$D_C = C^+ = C \oplus A'B'$$



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Counters

3-bit Binary Up-Down counter using D flip-flops

$$D_A = A^+ = A \oplus (U + D)$$

$$D_B = B^+ = B \oplus (UA + DA')$$

$$D_C = C^+ = C \oplus (UAB + DA'B')$$

