XILINX CPLD Reports XC9500

Fitter Report | Timing Report

Timing Report

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Timing Report

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Design Name	top
Device, Speed (SpeedFile Version)	XC9536, -5 (3.0)
Date Created	Sat Feb 24 17:17:39 2024
Created By	Timing Report Generator: version P.20131013
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Summary

Notes and Warnings
Note: This design contains no timing constraints.
Note: A default set of constraints using a delay of 0.000ns will be used for analysis.

Performance Summary	
Min. Clock Period	10.000 ns.
Max. Clock Frequency (fSYSTEM)	100.000 MHz.
Limited by Cycle Time for CLK	
Clock to Setup (tCYC)	10.000 ns.
Pad to Pad Delay (tPD)	8.500 ns.
Setup to Clock at the Pad (tSU)	3.500 ns.
Clock Pad to Output Pad Delay (tCO)	15.000 ns.

Timing Constraints