Autumn 2024 – ECE 5020
Homework 6

Due: 10/30/2024

1. Using the inverter you designed in HW4/5
    a. Create schematic and symbol for the flip flop below. Pick reasonable sizes for the transmission gate. [Build T-gate→MUX→FF].
    b. Build a testbench to simulate the setup time, hold time and clk-to-Q delay for the flip flop. Use approach discussed in lecture on 10/16 (You may the methodology on pages 308-9 of the textbook alternatively).

    c. (**grad students only**) Draw the layout for flip flop. You may use two cell heights to ease layout. Check DRC, LVS and run QRC.
    d. (**grad students only**) Simulate the setup time, hold time and clk-to-Q delay of the extracted cell. How do the measurements compare pre- and post-layout?