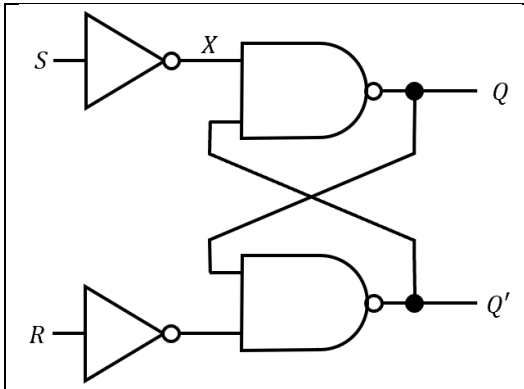


The inverters have a propagation delay of 3 ns.

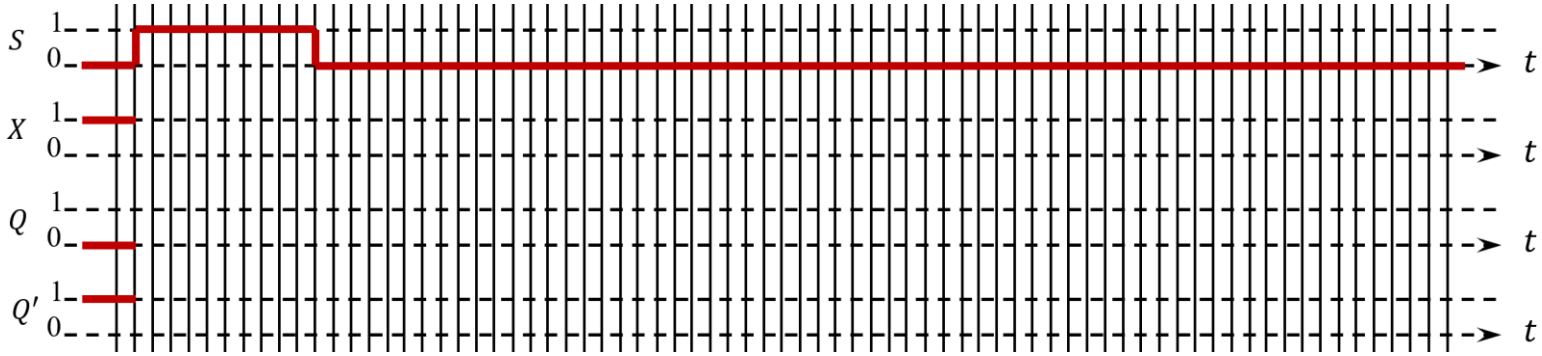
The two-input NAND gates have a propagation delay of 4 ns.

Complete the timing diagrams for each of the input pulses shown for Part a) and Part b).

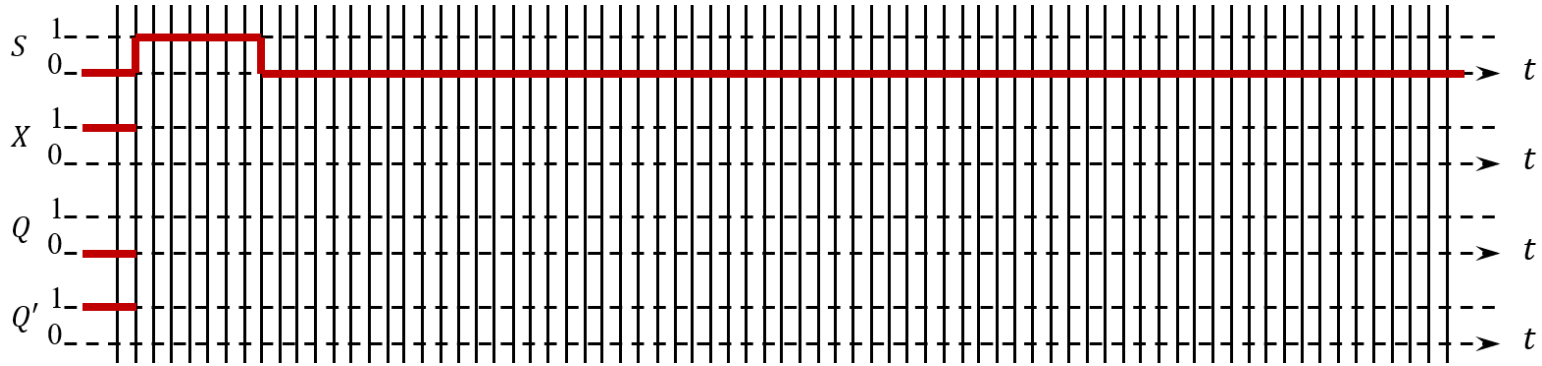
The vertical lines are spaced 1ns apart.

The reset input has $R = 0$ at all times in this problem.

a)



b)



c) What is the minimum pulse width (in integer units of ns) that must be applied to the S input for the output of this latch to be properly set?