Lecture Outline

Reminders to self:

- ❑ Turn on lecture recording to Cloud
- ❑ Turn on Zoom microphone

- Last Lecture
  - Continued Counters
    - Finished 3-bit Gray-Code counter from last Friday's lecture
    - Up and Down counter
    - Counter design with other types of flip-flops (SR)
- Today's Lecture
  - Continue Counters
    - Finish counter design with other types of flip-flops (SR and JK)
    - Analysis of Counter Circuits – verifying design does the expected

Handouts and Announcements

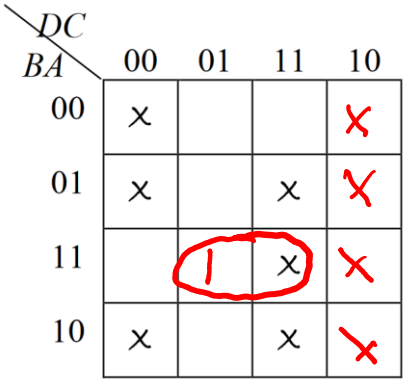
- Announcements
  - Homework Problem 12-5
    - Posted on Carmen yesterday
    - Due: 11:25am Wednesday 3/22
  - Homework Reminder
    - HWs 12-2 & 12-3 Due: 11:59pm Thursday 3/9
    - HW 12-4 Due: 11:59pm Tuesday 3/21
  - Read for Friday: pages 425-432
  - Mini-Exam 3 regrade continuing
    - A-some C regraded
    - Some P-Z regraded

Counters

4-bit Excess-3 counter using SR flip-flops

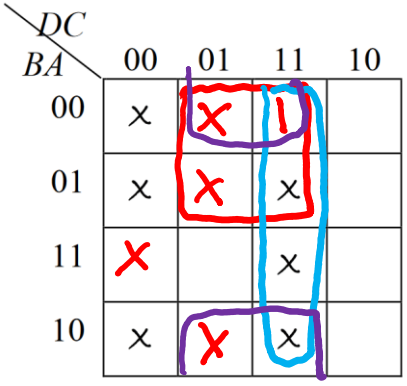
D	C	B	A	D^+	C^+	B^+	A^+	S_D	R_D	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X						
0	1	0	0	0	1	0	1	0	X						
0	1	0	1	0	1	1	0	0	X						
0	1	1	0	0	1	1	1	0	X						
0	1	1	1	1	0	0	0	1	0						
1	0	0	0	1	0	0	1	X	0						
1	0	0	1	1	0	1	0	X	0						
1	0	1	0	1	0	1	1	X	0						
1	0	1	1	1	1	0	0	X	0						
1	1	0	0	0	0	1	1	0	1						
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0



$S_D = ABC$

1 gate
3 inputs



$R_D = B'C$

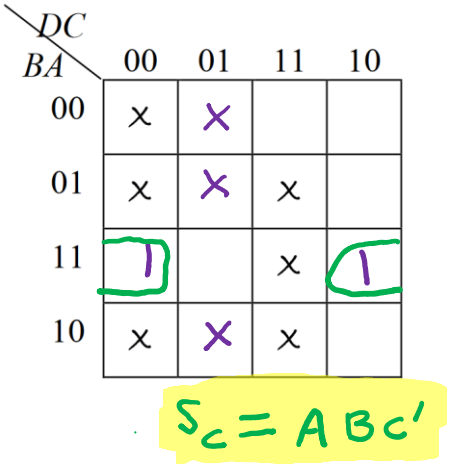
or $R_D = CD$
or $R_D = A'C$

1 gate
2 inputs

Counters

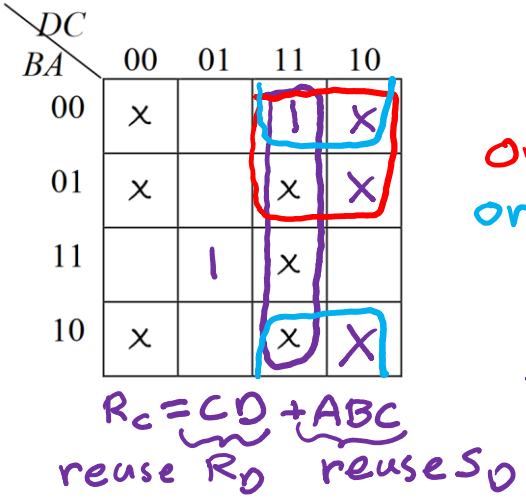
4-bit Excess-3 counter using SR flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	S_D	R_D	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X	1	0				
0	1	0	0	0	1	0	1	0	X	X	0				
0	1	0	1	0	1	1	0	0	X	X	0				
0	1	1	0	0	1	1	1	0	X	X	0				
0	1	1	1	1	0	0	0	1	0	0	1				
1	0	0	0	1	0	0	1	X	0	0	X				
1	0	0	1	1	0	1	0	X	0	0	X				
1	0	1	0	1	0	1	1	X	0	0	X				
1	0	1	1	1	1	0	0	X	0	1	0				
1	1	0	0	0	0	1	1	0	1	0	1				
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X



Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

1 gate
3 inputs



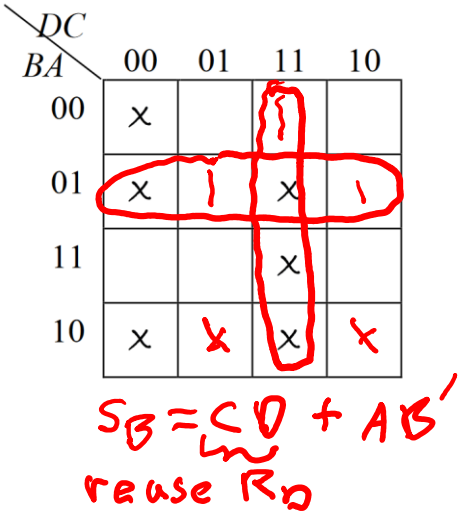
or $R_C = B'D + ABC$
or $R_C = A'D + ABC$

1 new gate
2 new inputs

Counters

4-bit Excess-3 counter using SR flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	S_D	R_D	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X	1	0	0	1		
0	1	0	0	0	1	0	1	0	X	X	0	0	X		
0	1	0	1	0	1	1	0	0	X	X	0	1	0		
0	1	1	0	0	1	1	1	0	X	X	0	X	0		
0	1	1	1	1	0	0	0	1	0	0	1	0	1		
1	0	0	0	1	0	0	1	X	0	0	X	0	X		
1	0	0	1	1	0	1	0	X	0	0	X	1	0		
1	0	1	0	1	0	1	1	X	0	0	X	X	0		
1	0	1	1	1	1	0	0	X	0	1	0	0	1		
1	1	0	0	0	0	1	1	0	1	0	1	1	0		
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X

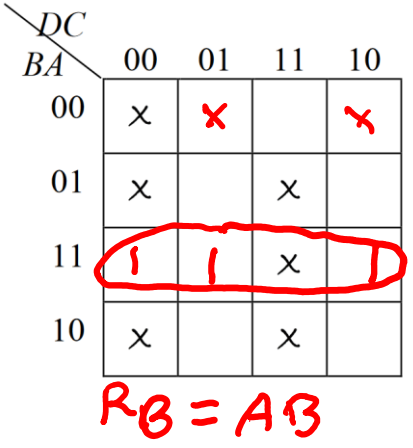


$S_B = C\overline{D} + A\overline{B}'$

reuse R_D

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

2 new gates
4 new inputs



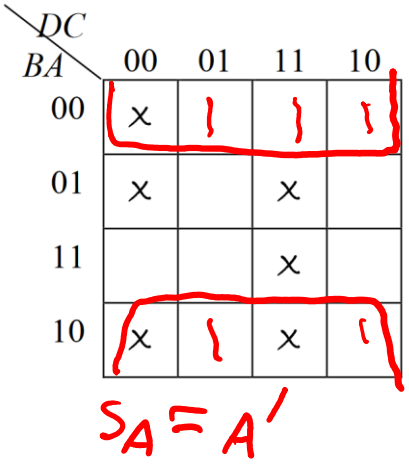
$R_B = AB$

1 new gate
2 new inputs

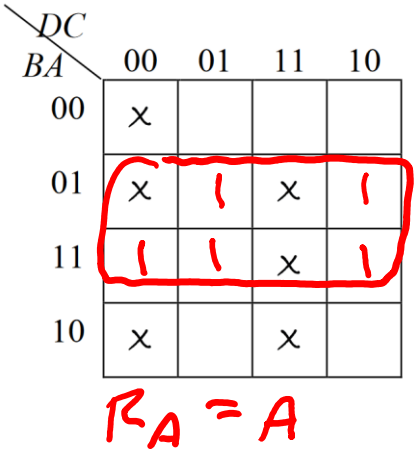
Counters

4-bit Excess-3 counter using SR flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	S_D	R_D	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X	1	0	0	1	0	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	0
0	1	0	1	0	1	1	0	0	X	X	0	1	0	0	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	0
0	1	1	1	1	0	0	0	1	0	0	1	0	1	0	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	0
1	0	0	1	1	0	1	0	X	0	0	X	1	0	0	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	0
1	0	1	1	1	1	0	0	X	0	1	0	0	1	0	1
1	1	0	0	0	0	1	1	0	1	0	1	1	0	1	0
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X



Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0



Total
7 gates
16 inputs

Counter design using J-K flip-flops

- Very similar to S-R
- Except now $J = K = 1$ is allowed, for the Toggle operation

Circuit Analysis TT

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Q	Q^+	J	K
0	0	0	0
		0	1
0	1	1	0
		1	1
1	0	0	1
		1	1
1	1	0	0
		1	0

Circuit Design TT

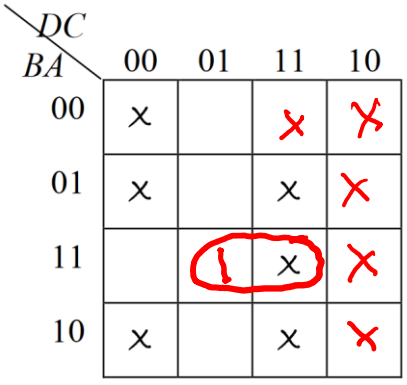
Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Toggle for $J = K = 1$ allows change of these from 0 to Don't Care

Counters

4-bit Excess-3 counter using JK flip-flops

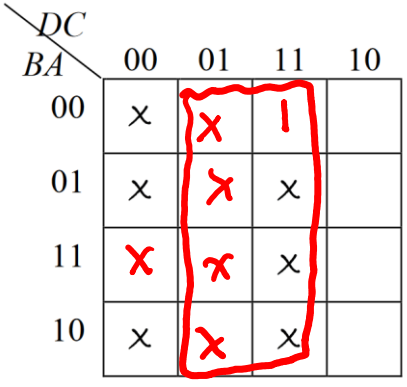
D	C	B	A	D^+	C^+	B^+	A^+	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X						
0	1	0	0	0	1	0	1	0	X						
0	1	0	1	0	1	1	0	0	X						
0	1	1	0	0	1	1	1	0	X						
0	1	1	1	1	0	0	0	1	X						
1	0	0	0	1	0	0	1	X	0						
1	0	0	1	1	0	1	0	X	0						
1	0	1	0	1	0	1	1	X	0						
1	0	1	1	1	1	0	0	X	0						
1	1	0	0	0	0	1	1	X	1						
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X



$J_D = ABC$

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

1 gate
3 inputs

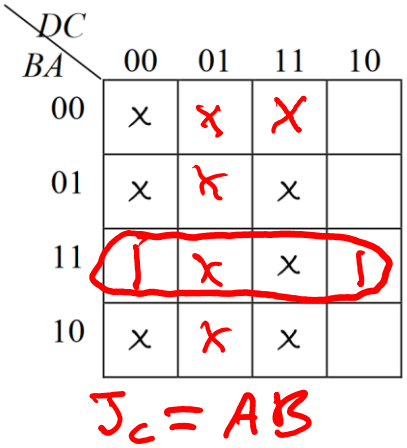


$K_D = C$

Counters

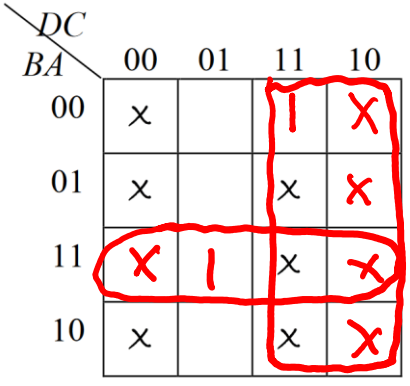
4-bit Excess-3 counter using JK flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X	1	X				
0	1	0	0	0	1	0	1	0	X	X	0				
0	1	0	1	0	1	1	0	0	X	X	0				
0	1	1	0	0	1	1	1	0	X	X	0				
0	1	1	1	1	0	0	0	1	X	X	1				
1	0	0	0	1	0	0	1	X	0	0	X				
1	0	0	1	1	0	1	0	X	0	0	X				
1	0	1	0	1	0	1	1	X	0	0	X				
1	0	1	1	1	1	0	0	X	0	1	X				
1	1	0	0	0	0	1	1	X	1	X	1				
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X



Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

1 gate
2 inputs

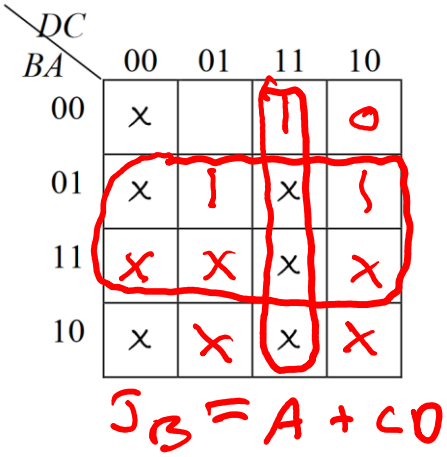


1 new gate
2 new inputs

Counters

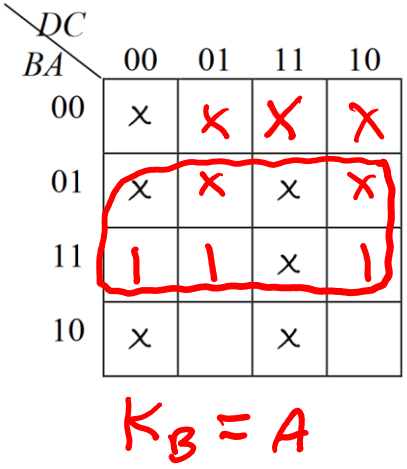
4-bit Excess-3 counter using JK flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1		
0	1	0	0	0	1	0	1	0	X	X	0	0	X		
0	1	0	1	0	1	1	0	0	X	X	0	1	X		
0	1	1	0	0	1	1	1	0	X	X	0	X	0		
0	1	1	1	1	0	0	0	1	X	X	1	X	1		
1	0	0	0	1	0	0	1	X	0	0	X	0	X		
1	0	0	1	1	0	1	0	X	0	0	X	1	X		
1	0	1	0	1	0	1	1	X	0	0	X	X	0		
1	0	1	1	1	1	0	0	X	0	1	X	X	1		
1	1	0	0	0	0	1	1	X	1	X	0	1	X		
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X



Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

2 new gates
4 new inputs

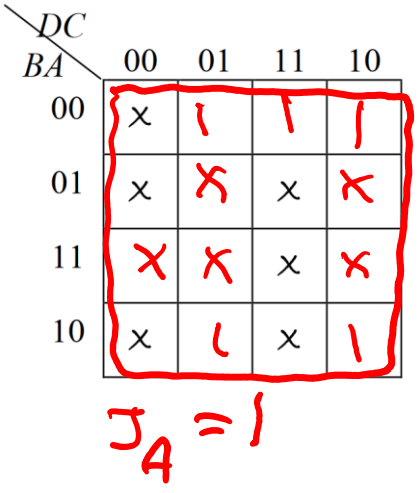


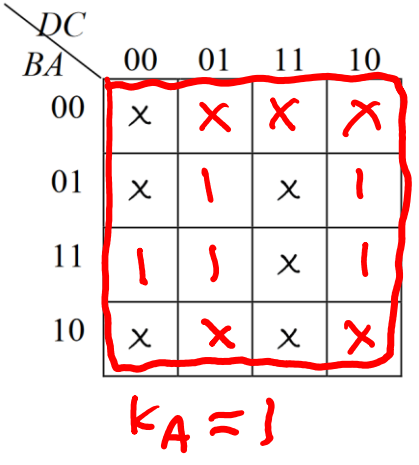
Counters

4-bit Excess-3 counter using JK flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	1	0	0	X	0	1	X	X	1	X	1
1	1	0	0	0	0	1	1	X	1	X	0	1	X	1	X
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0





Total
5 gates
11 inputs

Counters

4-bit Excess-3 counter using J-K flip-flops vs T or SR

- Using T flip-flops: 6 gates, 13 inputs
- Using S-R flip-flops: 7 gates, 16 inputs
- Using J-K flip-flops: 5 gates, 11 inputs

J-K is not always minimal

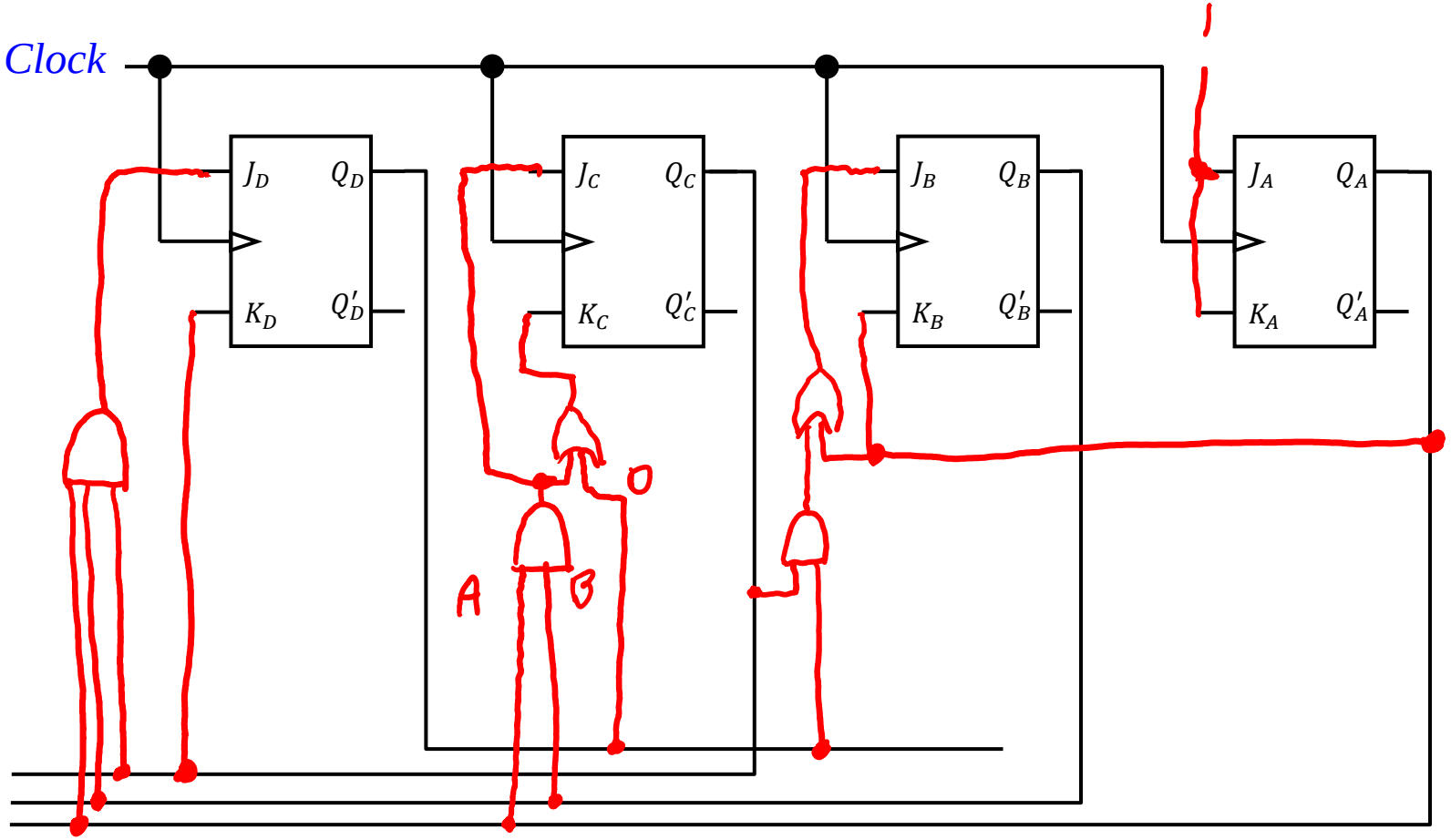
Different types of flip-flops will yield minimal designs for different count sequences

Watch for things like this in Homework 12-4

Counters

4-bit Excess-3 counter using J-K flip-flops

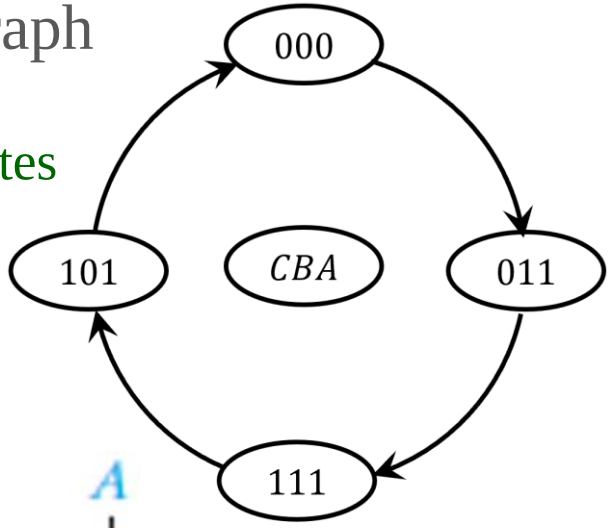
$J_D = ABC$ $K_D = C$ $J_C = AB$ $K_C = AB + D$ $J_B = A + CD$ $K_B = A$ $J_A = 1$ $K_A = 1$

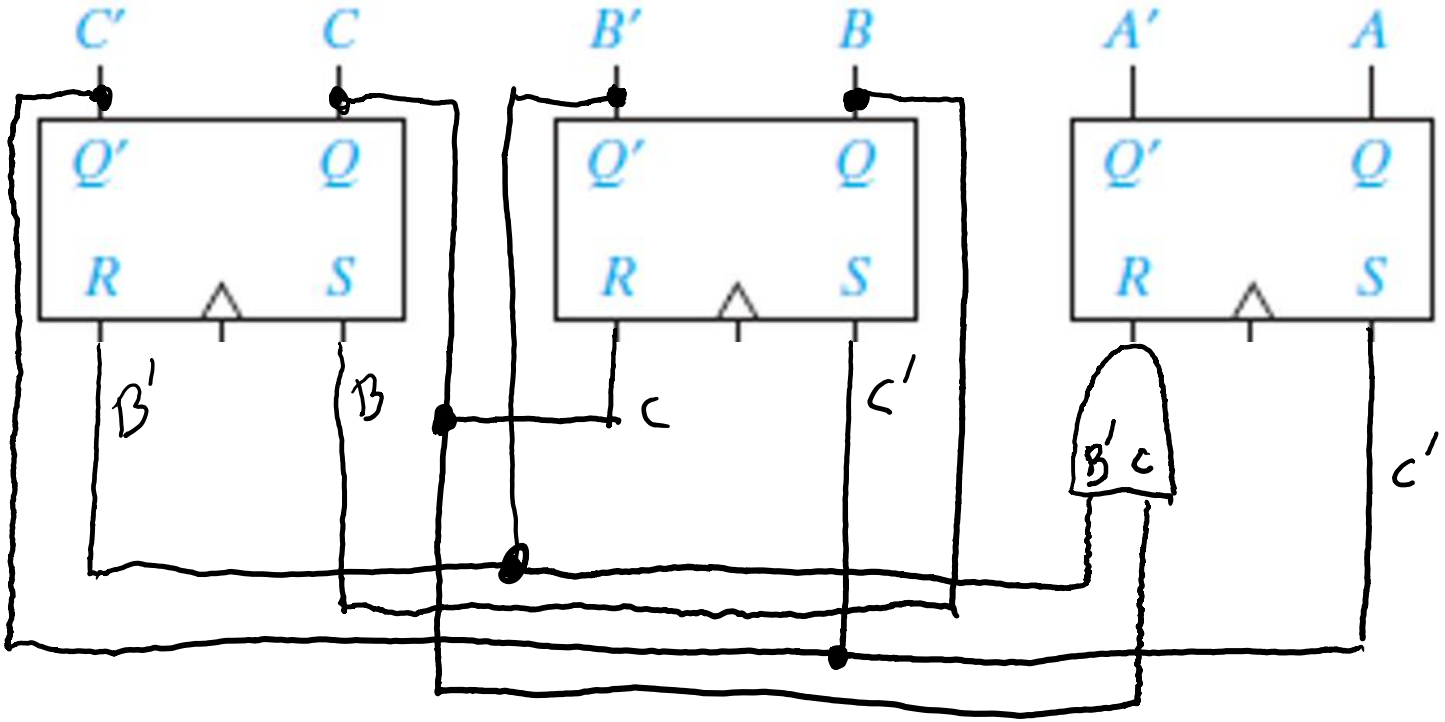


Counters

A 3-bit counter was designed for this transition graph

1. Verify the design counts the correct sequence
2. And what happens if the counter starts in one of the states not in this sequence? (Secondary transition graph?)





Counters

C	B	A	S_C	R_c	S_B	R_B	S_A	R_A	C^+	B^+	A^+
0	0	0	0	1	1	0	1	0	0	1	1
0	0	1	0	1	1	0	1	0	0	1	1
0	1	0	1	0	1	0	1	0	1	1	1
0	1	1	1	0	1	0	1	0	1	1	1
1	0	0	0	1	0	1	0	1	0	0	0
1	0	1	0	1	0	1	0	1	0	0	0
1	1	0	1	0	0	1	0	0	1	0	0
1	1	1	1	0	0	1	0	0	1	0	1

3-bit counter: verification of count sequence

$S_C(C,B,A) = B$

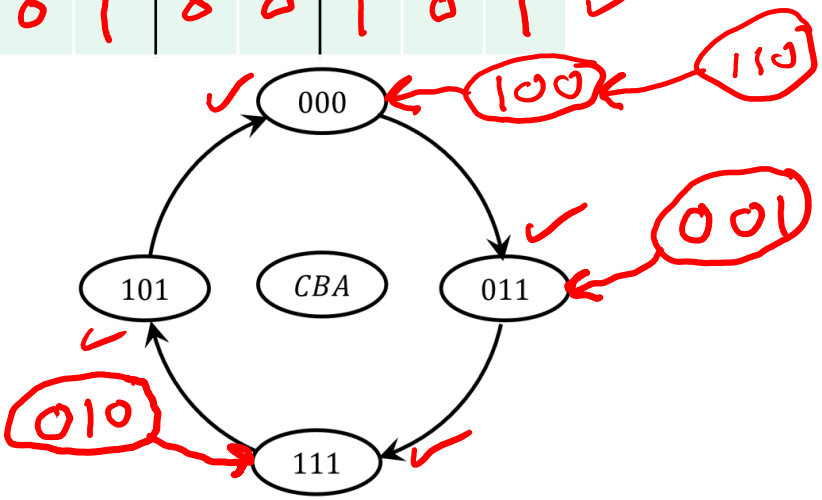
$R_C(C,B,A) = B'$

$S_B(C,B,A) = C'$

$R_B(C,B,A) = C$

$S_A(C,B,A) = C'$

$R_A(C,B,A) = B'C$



Counters

- Is possible that Don't Cares during design result in $R = S = 1$ for one or more bits of states not in count sequence
- Shows up in analysis of all states
- Could leave such a state by more than one path
- Not predictable which path will be followed
- But for correctly designed counter either path eventually leads to main count loop