Homework 4

Solve the **five** following problems, and show your work/process. Please neatly write or type your answers, and please scan or upload your answers in a single PDF file to the assignment submission on Carmen.

4.1 A microprocessor has an 8-bit address output bus with signals $A7$, $A6$, …, $A0$ (with $A7$ as the MSB and $A0$ as the LSB).

Using these address output signals, we want to control two peripheral devices ("first device" and "second device"). Each peripheral device has an active-low enable input EN_L and 3 address control inputs $A2$, $A1$, $A0$ (with $A2$ as the MSB and $A0$ as the LSB). The address control input signals select which output port of the peripheral device is activated. Thus, each peripheral device can control $2^3 = 8$ output ports. Note that the address control inputs are not the same as the output ports.

We want to map the 8 output ports of the first device to the microprocessor addresses 10010000 to 10010111, and we want to map the 8 output ports of the second device to the microprocessor addresses 10011000 to 10011111.

Use a 3-to-8 decoder (74x138) to implement this mapping. This decoder has three control inputs C, B, A (with C as the MSB and A as the LSB), one active-high enable input $G1$ and two active-low enable inputs $G2A\_L$ and $G2B\_L$, and eight selectable inverted outputs $Y0$, $Y1$, …, $Y7$ (with $Y0$ representing 000 and $Y7$ representing 111).

Use Figure 1 to draw connections among the outputs and inputs of the four chips in such a way to achieve this mapping. **<u>Do not use any additional gates.</u>** You may connect to power or ground.

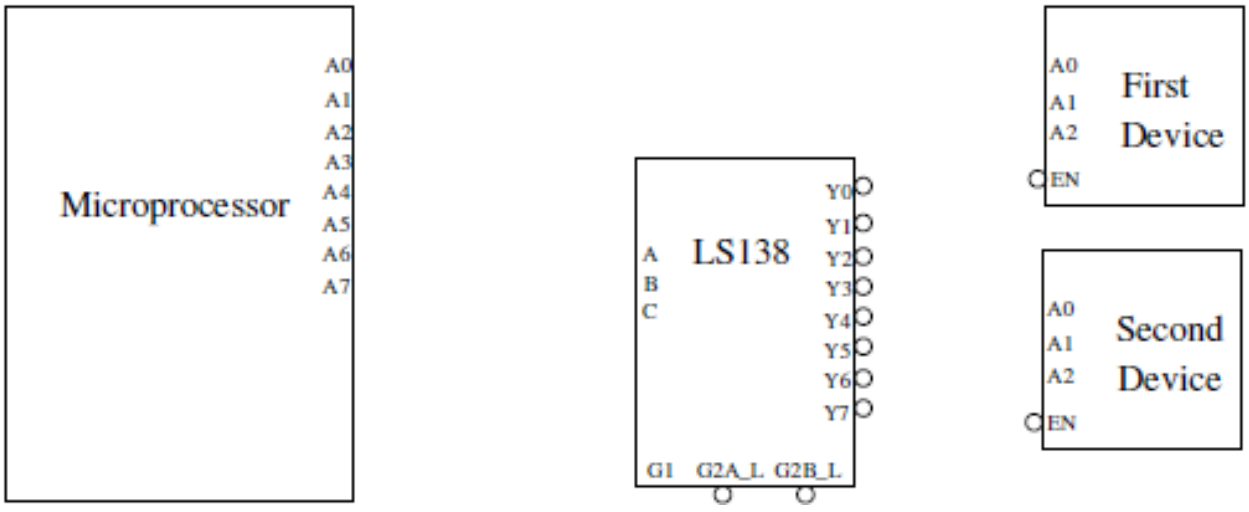

Figure 1: Microprocessor, 3-to-8 decoder, and two peripheral devices to implement address-to-port mapping.

4.2 Figure 2 shows a sequential circuit consisting of a System Controller (labeled and outlined with a dashed box), one 74LS161 counter, and some combinational logic.

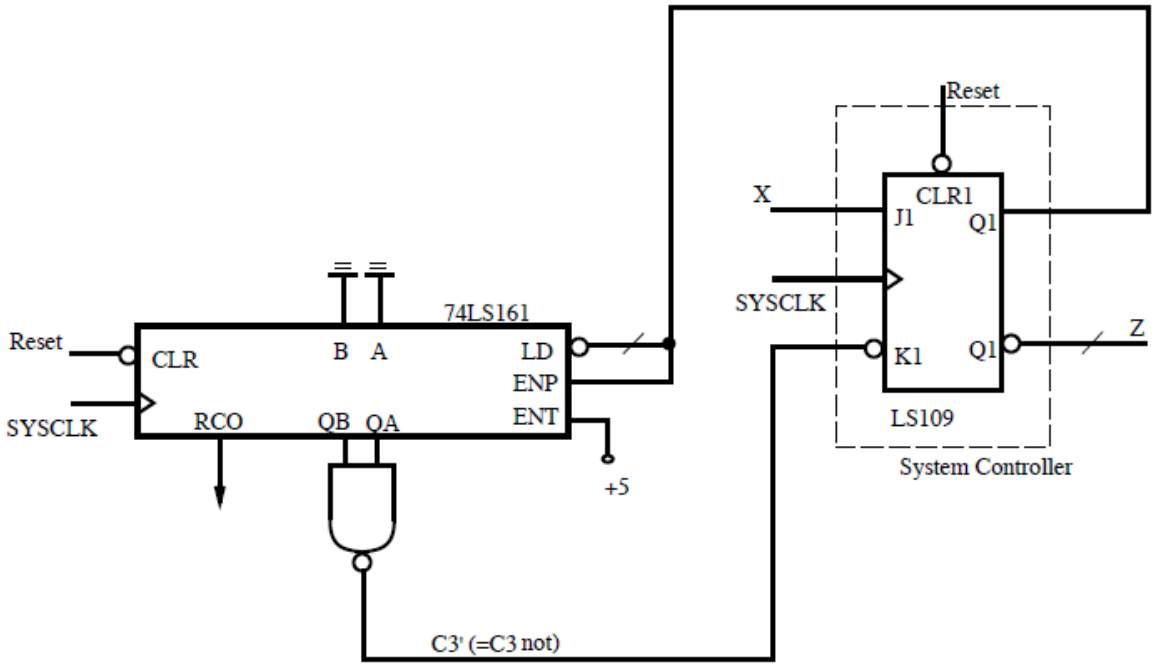

Figure 2: Sequential circuit with System Controller, 74LS161 counter, and combinational logic.

The System Controller has four external inputs: X, $C3'$, $SYSCLK$, and $Reset$. It has one external output: Z. The System Controller state is represented by $Q1$ of the JK flip-flop.

The 74LS161 counter has several inputs, and only two bits are used, QB and QA.

Analyze the System Controller by performing the following steps:

a. Derive the excitation equations ($J1$, $K1$), next-state equation ($Q1^+$), and output equation (Z) for the System Controller. The equations should be in terms of the external inputs X and $C3$, and the state $Q1$.

b. Construct a variable-entered state/output table for the System Controller. The state/output table should only have columns for $Q1$, $J1$, $K1$, $Q1^+$, and Z. The external inputs X and $C3$ should be variables to enter into the table.

c. Construct a state diagram for the System Controller. Use numeric coding for the state labels, but use variables for the external inputs X and $C3$ and the output Z. The internal excitation signals $J1$ and $K1$ should not appear in the state diagram.

d. Calculate the maximum clock frequency f_{max} for the **entire** circuit. Show all paths which need to be considered and their associated delays, and indicate the critical path (the path which determines the maximum clock frequency). Use the timing data in the tables at the end of this document. For the 74LS161, use the 74LS163 data.

4.3 Table 1 shows a state/output table for a sequential circuit state machine with one input X and one output Z.

Table 1: State/output table for a sequential circuit.

P.S. S	Output Z	N.S. S^+ X=0	N.S. S^+ X=1
A	0	B	D
B	0	C	D
C	1	B	D
D	0	B	C

a. Draw the state diagram given this state/output table. Use the same state labels as in the table.

b. Write at least 1 complete sentence describing the function of this circuit based on your state diagram.

c. Based on Table 1, finish the design of the sequential circuit. Use two D flip-flops with state variables Q_2Q_1 and state assignments $A = 00$, $B = 01$, $C = 11$, and $D = 10$. Derive the excitation equations for D_2 and D_1 and the output equation for Z, and draw the circuit.

4.4 Consider the design of a sequential circuit with two inputs, $INIT$ and X, and one Moore-type output, Z. As long as $INIT$ is asserted, Z remains 0. Once $INIT$ is negated, Z should remain 0 until X has been 0 for two consecutive inputs and 1 for two consecutive inputs. The two 0s can come before the two 1s, or the two 1s can come before the two 0s, and the pairs do not have to occur immediately next to each other. Then Z should go to 1 and remain 1 until $INIT$ is asserted again. Assume that once $INIT$ is negated, it will not be asserted again until sometime after Z goes to 1. Also, when $INIT$ is negated, the value of X at that time should be considered as the first possible 0 or 1 of a pair instead of waiting another clock cycle before looking at X.

a. Draw the state diagram. (Hint: No more than ten states are required.)

b. Construct a state description table. This should include one column for your state labels and another column for you to write a description of each state.

4.5 Consider the design of a sequential circuit with one input X and two outputs $UNLK$ and $HINT$. If and only if the input sequence $X = 10010001$ occurs, then the $UNLK$ output should be 1 **coincident** with the last 1 in the sequence. Otherwise, $UNLK$ should be 0. If and only if the current value of X is the correct next value in the sequence to move closer to $UNLK = 1$, then the $HINT$ output should be 1 **coincident** with that value of X. Otherwise, $HINT$ should be 0. Overlaps are allowed with the input sequence.

a. Draw the state diagram. (Hint: No more than ten states are required.)

b. Construct a state description table. This should include one column for your state labels and another column for you to write a description of each state.

c. Construct a state/output table. This should have one column for the present state (with your state labels from your diagram), three columns for the next state and $UNLK$ and $HINT$ outputs when $X = 0$, and three columns for the next state and $UNLK$ and $HINT$ outputs when $X = 1$.

Combinational Parts

Chip	t_{pLH} (ns)	t_{pHL} (ns)	Comments
'LS04, 'LS00, 'LS10, 'LS20	15	15	Inverter, 2-, 3-, 4-input NAND
'LS08, 'LS11	15	20	2-, 3-input AND
'LS02, 'LS27	15	15	2-, 3-input NOR
'LS32	22	22	2-input OR
'LS86			2-input XOR
2 levels	23	17	Other input low
3 levels	30	22	Other input high
'LS138			3-to-8 Decoder
$A, B, C, \rightarrow Y$ (2 levels)	20	41	$A \rightarrow Y_0, Y_2, Y_4, Y_6$ or $B \rightarrow Y_0, Y_1, Y_4, Y_6$ or $C \rightarrow Y_0, Y_1, Y_2, Y_3$
$A, B, C \rightarrow Y$ (3 levels)	27	39	Other cases
$G2A, G2B \rightarrow Y$	18	32	
$G1 \rightarrow Y$	26	38	
'LS139			2-to-4 Decoder
$A, B \rightarrow Y$ (2 levels)	20	33	$A \rightarrow Y_0, Y_2$ or $B \rightarrow Y_0, Y_1$
$A, B \rightarrow Y$ (3 levels)	29	38	Other cases
$G \rightarrow Y$	24	32	

'LS74 - D Type Positive-Edge-Triggered Flip-Flops

Data	t_{pLH}	t_{pHL}	t_s	t_h
$CLR, PR, CLK \rightarrow Q$	25	40		
D			20	5
$f_{max} = 25$ Mhz				

'LS109 - $J - \bar{K}$ Type Positive-Edge-Triggered Flip-Flops

Data	t_{pLH}	t_{pHL}	t_s	t_h
$CLR, PR, CLK \rightarrow Q$	25	40		
J, K			35	5
$f_{max} = 25$ Mhz				

'LS163 - 4-bit Binary Counter

Data	t_{pLH}	t_{pHL}	t_s	t_h
$CLK \rightarrow Q$	24	27		
$CLK \rightarrow RCO$	35	35		
$ENT \rightarrow RCO$	14	14		
$CLR \rightarrow Q$		28		
D, C, B, A, ENP, ENT, LD			20	0
$f_{max} = 25$ Mhz				