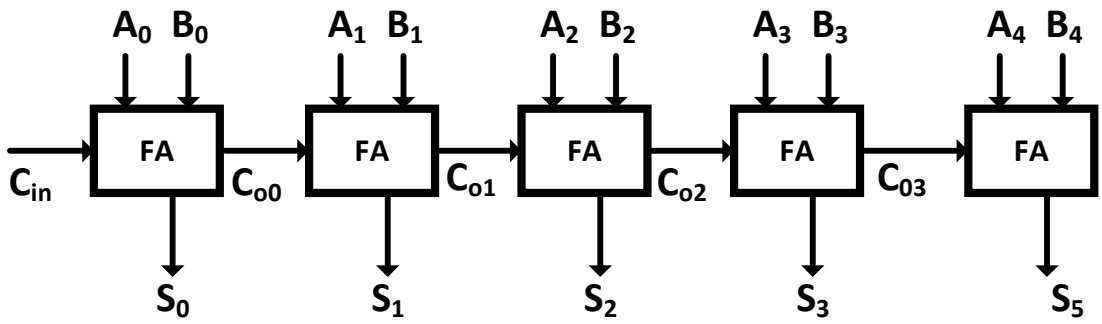
Autumn 2024 – ECE 5020
Homework 7

Due: 11/06/2024 (or project)- Work in Groups

1. Design a 8bit ripple carry adder and measure its delay.
    a. Create schematic and symbol for Generate (G) and Propagate (P) blocks using an XOR (new – choose between static complementary 12 transistor version and PTL 6 transistor version) and logic cells you designed in HW4.
    b. Create schematic and symbol of a 1-bit full adder using the P, G, XOR and logic cells from HW4. Measure the delay for the sum and carry paths.
    c. Use the 1-bit full adder from (b) to create a schematic and symbol for a 8-bit ripple-carry adder. Simulate the critical path delay of the adder.
    d. (**grad students only**) Draw the layout for XOR. Extract and redo the simulation in (c) with the av_extracted view of XOR. How much worse is the critical path delay?



2. Design an 8bit barrel shifter that can implement up to 7 right shifts.
    a. Create schematic and symbol for a 2-to-1 multiplexer if you did not do so in HW6.
    b. Use the 2-to-1 MUX from (a) to create a schematic and symbol for an arithmetic shifter can do multiplication by 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 and 1/128. Simulate the shifter to show the correct number of shifts in each of the above cases. Measure the critical path delay. Turn in your schematics and simulation results.
    c. (**grad students only**) Draw the layout for the MUX and shifter. Extract and redo the simulation in (b) with the av_extracted view. How much worse is the critical path delay?