THE OHIO STATE UNIVERSITY

COLLEGE OF ENGINEERING

ECE 3561
Advanced Digital Design
Class 30: Sequential Circuit Design 8 – Equations

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Sequential Circuit Design Process

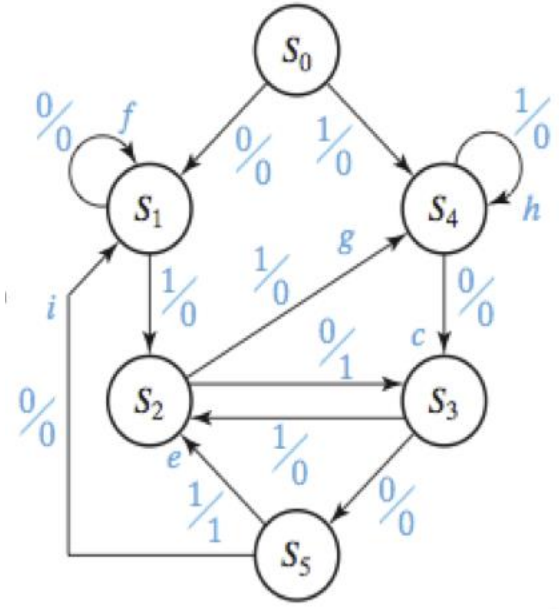
1) **State / Output Diagram / Table**
2) **Minimization of Number of States**
3) **State Variable Assignment**
4) Transition / Output Table
5) Selection of Flip Flop Types
6) Excitation Table
7) Excitation Equations
8) Output Equations
9) Logic Diagram

State Assignment Procedure Summary

1) Apply Guideline 1 to the state table to identify adjacency relationships for states that have the same next state for a given input.
2) Apply Guideline 2 to the state table to identify adjacency relationships for the next states of the same state.
3) Apply Guideline 3 to the state table to identify adjacency relationships for states that have the same output.
4) Assign the initial/start state to the "all 0s" square in the assignment map.
5) Place states in the assignment map to satisfy as many adjacency relationships as possible with this priority:
   - First: relationships from Guidelines 1 and 2 which occur multiple times
   - Second: remaining relationships from Guidelines 1 and 2
   - Third: relationships from Guideline 3
6) Iterate and/or move states as needed to determine "best" mapping which best satisfies the adjacency relationships.

State Assignment Example 3

- Consider this previous state machine (detects 010 or 1001)



	NEXT STATE		OUTPUT	
Present State	**X=0**	**X=1**	**X=0**	**X=1**
S0	S1	S4	0	0
S1	S1	S2	0	0
S2	S3	S4	1	0
S3	S5	S2	0	0
S4	S3	S4	0	0
S5	S1	S2	0	1

State Assignment Example 3

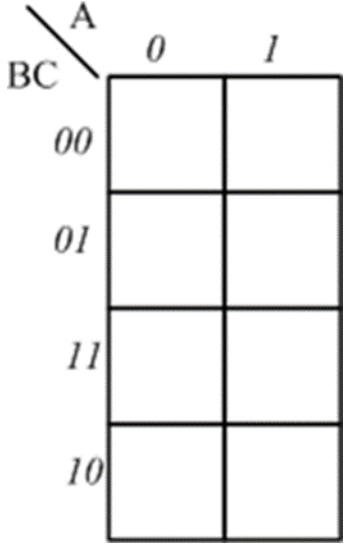
- Apply the three guidelines:

	NEXT STATE		OUTPUT	
Present State	**X=0**	**X=1**	**X=0**	**X=1**
S0	S1	S4	0	0
S1	S1	S2	0	0
S2	S3	S4	1	0
S3	S5	S2	0	0
S4	S3	S4	0	0
S5	S1	S2	0	1

State Assignment Example 3

- Enter S0 as the initial state and then enter states into the state assignment map to satisfy as many adjacency relationships as possible given the priorities

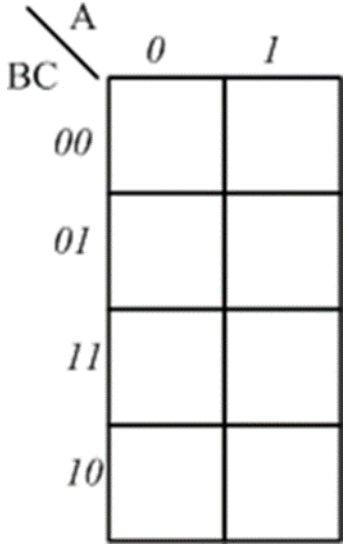
	NEXT STATE		OUTPUT	
Present State	**X=0**	**X=1**	**X=0**	**X=1**
S0	S1	S4	0	0
S1	S1	S2	0	0
S2	S3	S4	1	0
S3	S5	S2	0	0
S4	S3	S4	0	0
S5	S1	S2	0	1



State Assignment Example 3

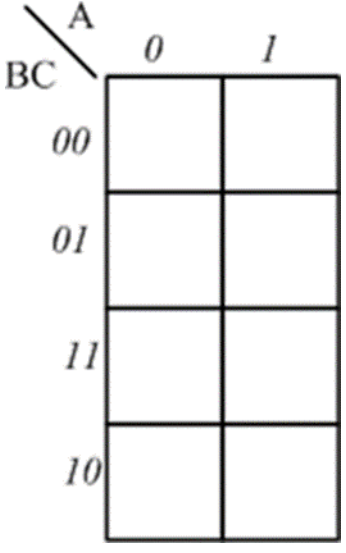
- Here is one possible assignment mapping

	NEXT STATE		OUTPUT	
Present State	**X=0**	**X=1**	**X=0**	**X=1**
S0	S1	S4	0	0
S1	S1	S2	0	0
S2	S3	S4	1	0
S3	S5	S2	0	0
S4	S3	S4	0	0
S5	S1	S2	0	1



State Assignment Example 3

- Then enter the state assignments into the state table

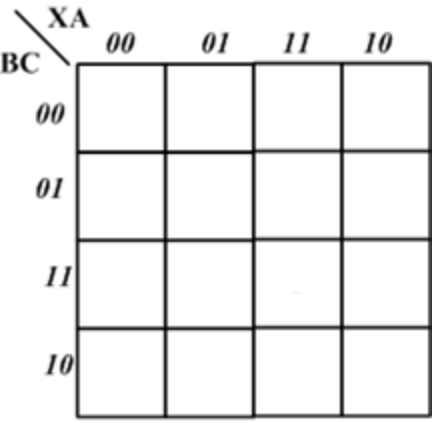


Present State	Next State		Output	
ABC	X =0	X=1	X=0	X=1
S0 000	S1	S4	0	0
S1	S1	S2	0	0
S2	S3	S4	1	0
S3	S5	S2	0	0
S4	S3	S4	0	0
S5	S1	S2	0	1

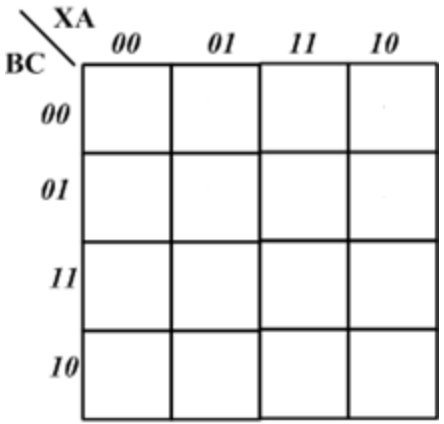
State Assignment Example 3

- Then generate K-maps and the equations/logic. Use D flip-flops.

Present State	Next State		Output	
ABC	X =0	X=1	X=0	X=1
S0 000	S1	S4	0	0
S1	S1	S2	0	0
S2	S3	S4	1	0
S3	S5	S2	0	0
S4	S3	S4	0	0
S5	S1	S2	0	1



A =



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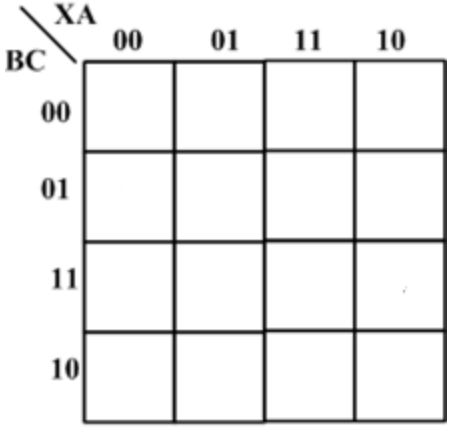

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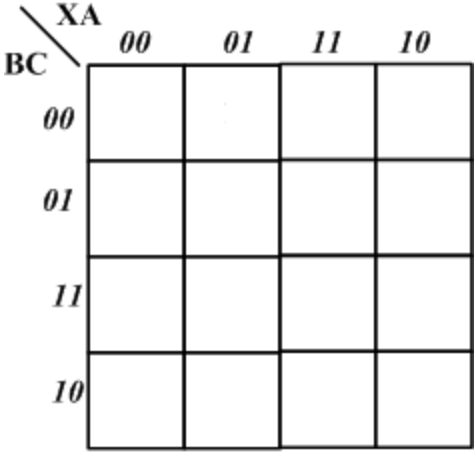

Z =

State Assignment Example 3

- Total circuit cost:
  - 3 D flip-flops
  - X complement: 1 gate
  - A excitation logic: 2 gates
  - B excitation logic: 1 gate
  - C excitation logic: 2 gates (but 1 is reused from A)
  - Z combinational logic: 3 gates
  - Total = 3 FFs + 7 gates

State Assignment Example 3

Draw the circuit!