Lecture Outline

Reminders to self:

- ❑ Turn on lecture recording to Cloud
- ❑ Turn on Zoom microphone

- Last Lecture
  - Reviewed HW 11-1 (SR Latch timing diagram)
  - Continued Counters
    - Other count sequences (3-bit binary, BCD, 3-bit Gray-Code)
    - Counter design with other types of flip-flops (D first)
- Today's Lecture
  - Continue Counters
    - Finish 3-bit Gray-Code counter from last lecture
    - Up and Down counter
    - Counter design with other types of flip-flops (SR and JK today)

Handouts and Announcements

- Announcements
  - Homework Problem 12-4
    - Posted on Carmen Sunday evening
    - Due: 11:59pm Tuesday 3/21
  - Homework Reminder
    - HW 12-1 Due: 11:25am Wednesday 3/8
    - HWs 12-2 & 12-3 Due: 11:59pm Thursday 3/9
  - Read for Wednesday: pages 412, 418-424
  - Mini-Exam 3 regrade continuing
    - A-some C regraded
    - Some S-Z regraded

Handouts and Announcements

- Announcements
  - Mini-Exam 4 Reminder
    - Available 5pm Monday 3/6 through 5:00pm Tuesday 3/7
    - Due in Carmen PROMPTLY at 5:00pm on 3/7
    - Designed to be completed in ~36 min, but you may use more
    - When planning your schedule:
      - I recommend building in 10-15 min extra
      - To allow for downloading exam, signing and dating honor pledge, saving solution as pdf, and uploading to Carmen
    - I also recommend not procrastinating
  - Exam review topics available on Carmen
  - Sample Mini-Exams 5 and 6 from Au20 also available

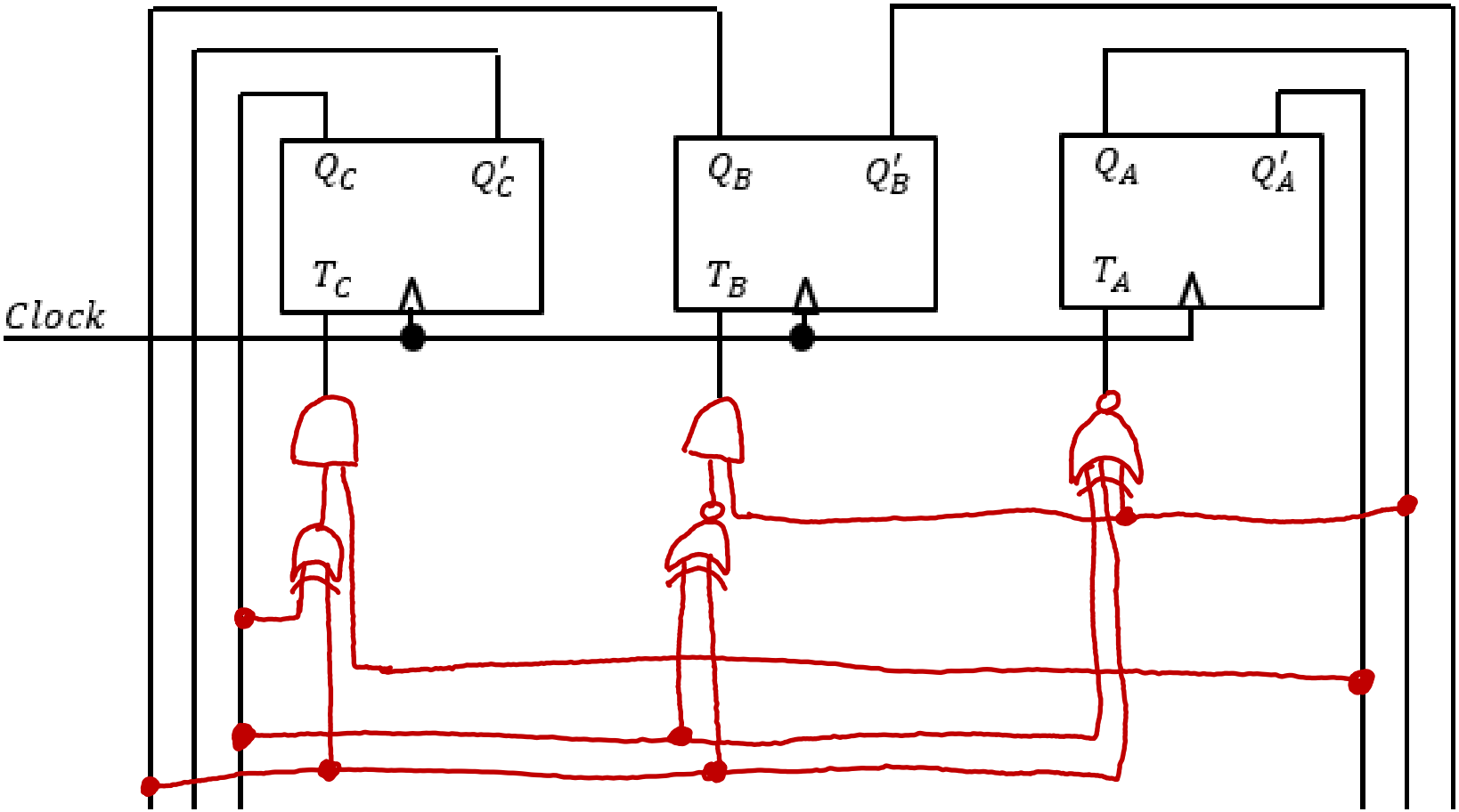
Counters

$T_C = C'BA' + CB'A' = A'(BC' + B'C) = A'(B \oplus C)$

$T_B = C'B'A + CBA = A(BC + B'C') = A(\overline{B \oplus C})$

$T_A = C'B'A' + C'BA + CB'A + CBA' = A(B \oplus C) + A'(\overline{B \oplus C}) = \overline{A \oplus B \oplus C}$ 3-input XNOR

Where we left off last lecture



Counters

3-bit Binary Up-Down counter using D flip-flops

Bi-directional Transition Graph

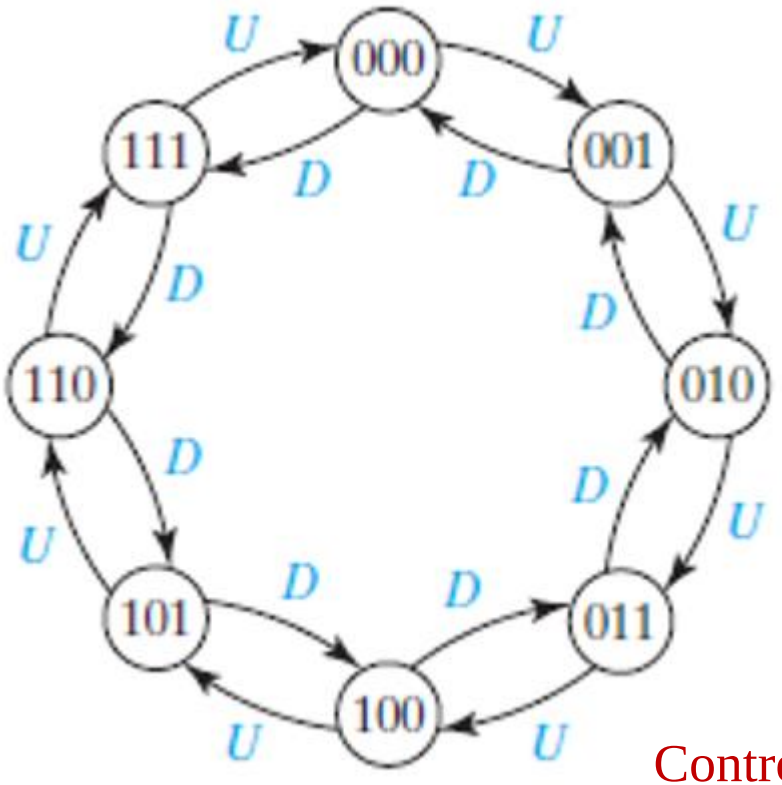


Table of Present and Next States for both directions

	$C^+B^+A^+$	
CBA	U	D
000	001	111
001	010	000
010	011	001
011	100	010
100	101	011
101	110	100
110	111	101
111	000	110

Control Bits U and D

- $U = D = 0$ ⇨ no count
- $U = 1; D = 0$ ⇨ count up
- $U = 0; D = 1$ ⇨ count down
- $U = D = 1$ ⇨ **not allowed**

Counters

3-bit Binary Up-Down counter using D flip-flops

	$C^+B^+A^+$	
CBA	U	D
000	001	111
001	010	000
010	011	001
011	100	010
100	101	011
101	110	100
110	111	101
111	000	110

Next state of A is A' either Up or Down

$D_A = A^+ = A \oplus (U + D)$

$D_B = B^+ = B \oplus (UA + DA')$

$D_C = C^+ = C \oplus (UAB + DA'B')$

When $U = 1, D = 0$ these equations reduce to the same expressions on slides 6 & 7 of last lecture

When $U = 0, D = 1$ these equations reduce to

$D_A = A^+ = A \oplus 1 = A'$ (A always changes)

$D_B = B^+ = B \oplus A'$ (B changes when A=0)

$D_C = C^+ = C \oplus A'B'$ (C changes when A=B=0)

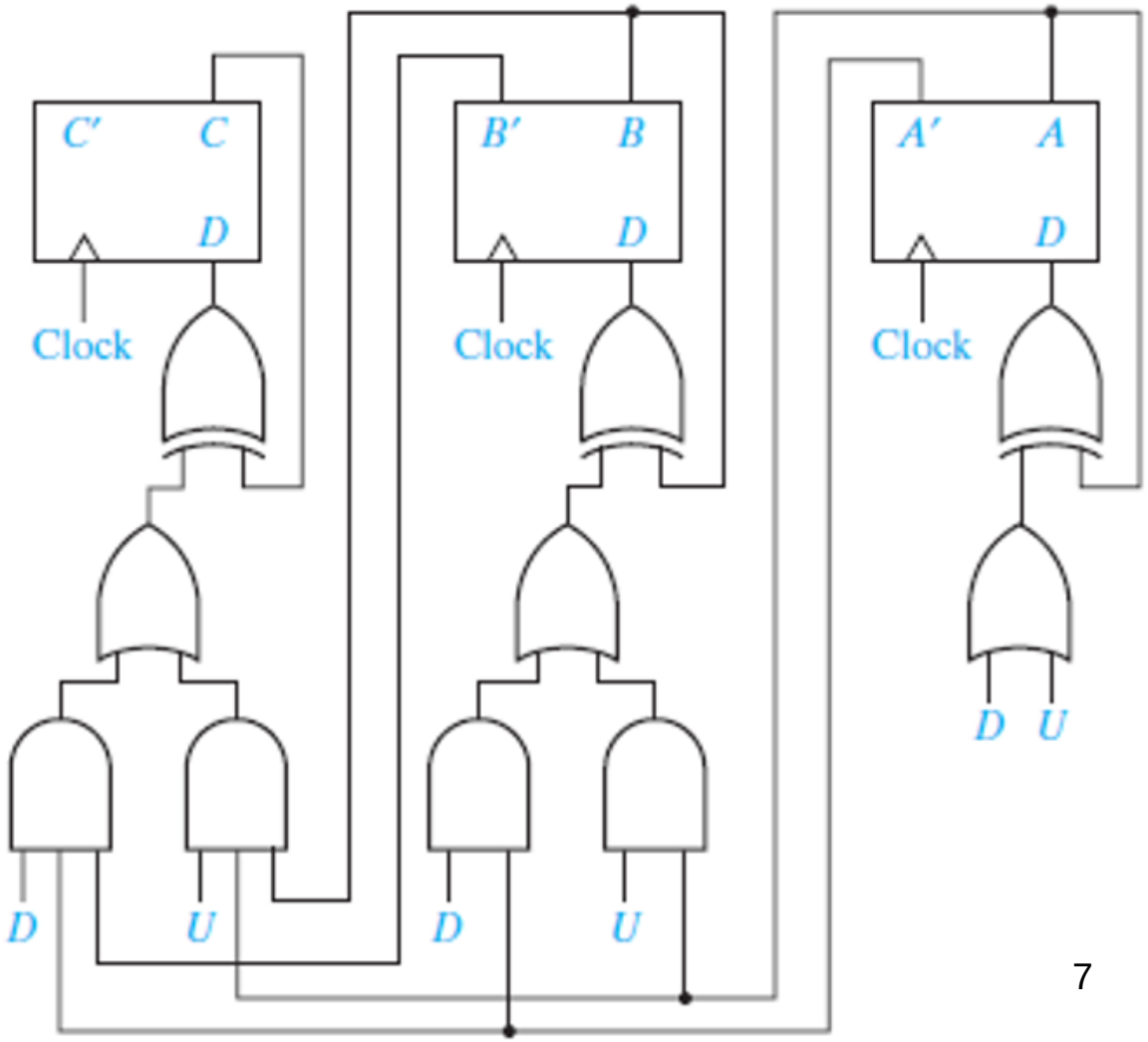
Counters

3-bit Binary Up-Down counter using D flip-flops

$D_A = A^+ = A \oplus (U + D)$

$D_B = B^+ = B \oplus (UA + DA')$

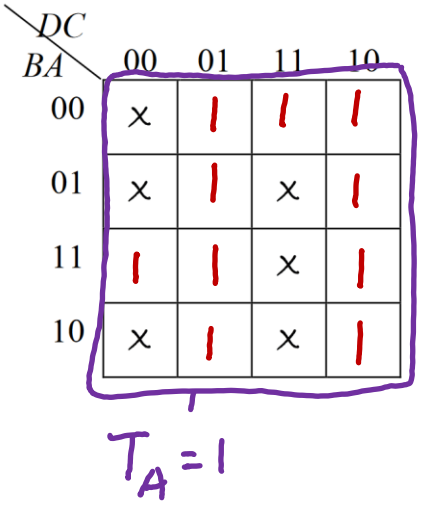
$D_C = C^+ = C \oplus (UAB + DA'B')$

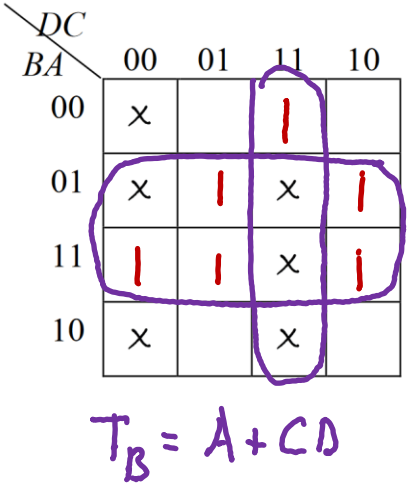


Counters

4-bit Excess-3 counter using T flip-flops (next states in table 1-2 in textbook)

D	C	B	A	D^+	C^+	B^+	A^+	T_D	T_C	T_B	T_A
0	0	0	0	-	-	-	-	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X
0	0	1	1	0	1	0	0		1	1	1
0	1	0	0	0	1	0	1				1
0	1	0	1	0	1	1	0			1	1
0	1	1	0	0	1	1	1				1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1				1
1	0	0	1	1	0	1	0			1	1
1	0	1	0	1	0	1	1				1
1	0	1	1	1	1	0	0		1	1	1
1	1	0	0	0	0	1	1	1	1	1	1
1	1	0	1	-	-	-	-	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X

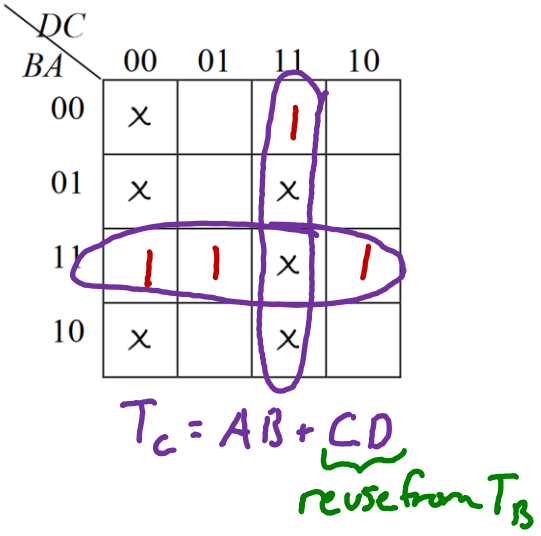


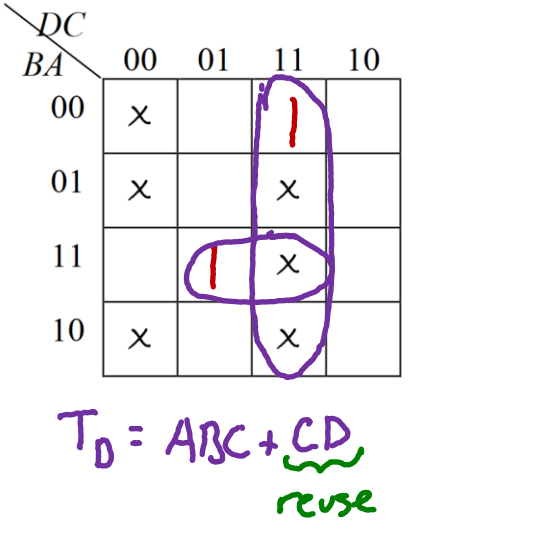


Decimal Digit	Excess-3 Code
0	0011
1	0100
2	0101
3	0110
4	0111
5	1000
6	1001
7	1010
8	1011
9	1100

4-bit Excess-3 counter using T flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	T_D	T_C	T_B	T_A
0	0	0	0	-	-	-	-	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X
0	0	1	1	0	1	0	0		1	1	1
0	1	0	0	0	1	0	1				1
0	1	0	1	0	1	1	0			1	1
0	1	1	0	0	1	1	1				1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1				1
1	0	0	1	1	0	1	0			1	1
1	0	1	0	1	0	1	1				1
1	0	1	1	1	1	0	0		1	1	1
1	1	0	0	0	0	1	1	1	1	1	1
1	1	0	1	-	-	-	-	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X





Counter design using S-R flip-flops

- When using T or D flip-flops: single input to design
- For S-R (and J-K): two inputs to design
  - Previously we used S, R, and current Q to predict next state Q^+
  - Flip it around: use current Q and desired Q^+ to design needed S and R
  - First look at changing state
  - Then look at holding same state

Circuit Analysis TT

S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	– } inputs not
1	1	1	– } allowed

Q	Q^+	S	R
0	0	0	0
		0	1
0	1	1	0
1	0	0	1
1	1	0	0
		1	0

Present $Q = 0$ / desired $Q^+ = 0$:
But R could be or value

Present $Q = 0$ / desired $Q^+ = 1$: set operation

Present $Q = 1$ / desired $Q^+ = 0$: reset operation

Present $Q = 1$ / desired $Q^+ = 1$:
But S could be or value

Counter design using S-R flip-flops

- When using T or D flip-flops: single input to design
- For S-R (and J-K): two inputs to design
  - Previously we used S, R, and current Q to predict next state Q^+
  - Flip it around: use current Q and desired Q^+ to design needed S and R
  - First look at changing state
  - Then look at holding same state

Q	Q^+	S	R	
0	0	0	0	S must = 0; don't care which value R has
		0	1	
0	1	1	0	same
1	0	0	1	
1	1	0	0	R must = 0; don't care which value S has
		1	0	

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Counters

4-bit Excess-3 counter using SR flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	S_D	R_D	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0								
0	1	0	0	0	1	0	1								
0	1	0	1	0	1	1	0								
0	1	1	0	0	1	1	1								
0	1	1	1	1	0	0	0								
1	0	0	0	1	0	0	1								
1	0	0	1	1	0	1	0								
1	0	1	0	1	0	1	1								
1	0	1	1	1	1	0	0								
1	1	0	0	0	0	1	1								
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

BA \ DC	00	01	11	10
00	X			
01	X		X	
11			X	
10	X		X	

BA \ DC	00	01	11	10
00	X			
01	X		X	
11			X	
10	X		X	

Counters

4-bit Excess-3 counter using SR flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	S_D	R_D	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X						
0	1	0	0	0	1	0	1	0	X						
0	1	0	1	0	1	1	0	0	X						
0	1	1	0	0	1	1	1	0	X						
0	1	1	1	1	0	0	0	1	0						
1	0	0	0	1	0	0	1	X	0						
1	0	0	1	1	0	1	0	X	0						
1	0	1	0	1	0	1	1	X	0						
1	0	1	1	1	1	0	0	X	0						
1	1	0	0	0	0	1	1	0	1						
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X

DC / BA	00	01	11	10
00	X			
01	X		X	
11			X	
10	X		X	

DC / BA	00	01	11	10
00	X			
01	X		X	
11			X	
10	X		X	

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

4-bit Excess-3 counter using SR flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	S_D	R_D	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X	1	0				
0	1	0	0	0	1	0	1	0	X	X	0				
0	1	0	1	0	1	1	0	0	X	X	0				
0	1	1	0	0	1	1	1	0	X	X	0				
0	1	1	1	1	0	0	0	1	0	0	1				
1	0	0	0	1	0	0	1	X	0	0	X				
1	0	0	1	1	0	1	0	X	0	0	X				
1	0	1	0	1	0	1	1	X	0	0	X				
1	0	1	1	1	1	0	0	X	0	1	0				
1	1	0	0	0	0	1	1	0	1	0	1				
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

BA \ DC	00	01	11	10
00	×			
01	×		×	
11			×	
10	×		×	

BA \ DC	00	01	11	10
00	×			
01	×		×	
11			×	
10	×		×	

Counters

4-bit Excess-3 counter using SR flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	S_D	R_D	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X	1	0	0	1		
0	1	0	0	0	1	0	1	0	X	X	0	0	X		
0	1	0	1	0	1	1	0	0	X	X	0	1	0		
0	1	1	0	0	1	1	1	0	X	X	0	X	0		
0	1	1	1	1	0	0	0	1	0	0	1	0	1		
1	0	0	0	1	0	0	1	X	0	0	X	0	X		
1	0	0	1	1	0	1	0	X	0	0	X	1	0		
1	0	1	0	1	0	1	1	X	0	0	X	X	0		
1	0	1	1	1	1	0	0	X	0	1	0	0	1		
1	1	0	0	0	0	1	1	0	1	0	1	1	0		
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

BA \ DC	00	01	11	10
00	×			
01	×		×	
11			×	
10	×		×	

BA \ DC	00	01	11	10
00	×			
01	×		×	
11			×	
10	×		×	

Counter design using J-K flip-flops

- Very similar to S-R
- Except now $J = K = 1$ is allowed, for the operation

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Q	Q^+	J	K
0	0	0	0
		0	1
0	1	1	0
		1	1
1	0	0	1
		1	1
1	1	0	0
		1	0

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Toggle for $J = K = 1$ allows change of these from 0 to

Counters

4-bit Excess-3 counter using JK flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0								
0	1	0	0	0	1	0	1								
0	1	0	1	0	1	1	0								
0	1	1	0	0	1	1	1								
0	1	1	1	1	0	0	0								
1	0	0	0	1	0	0	1								
1	0	0	1	1	0	1	0								
1	0	1	0	1	0	1	1								
1	0	1	1	1	1	0	0								
1	1	0	0	0	0	1	1								
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X

DC / BA	00	01	11	10
00	x			
01	x		x	
11			x	
10	x		x	

DC / BA	00	01	11	10
00	x			
01	x		x	
11			x	
10	x		x	

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Counters

4-bit Excess-3 counter using JK flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X						
0	1	0	0	0	1	0	1	0	X						
0	1	0	1	0	1	1	0	0	X						
0	1	1	0	0	1	1	1	0	X						
0	1	1	1	1	0	0	0	1	X						
1	0	0	0	1	0	0	1	X	0						
1	0	0	1	1	0	1	0	X	0						
1	0	1	0	1	0	1	1	X	0						
1	0	1	1	1	1	0	0	X	0						
1	1	0	0	0	0	1	1	X	1						
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

BA \ DC	00	01	11	10
00	×			
01	×		×	
11			×	
10	×		×	

BA \ DC	00	01	11	10
00	×			
01	×		×	
11			×	
10	×		×	

Counters

4-bit Excess-3 counter using JK flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X	1	X				
0	1	0	0	0	1	0	1	0	X	X	0				
0	1	0	1	0	1	1	0	0	X	X	0				
0	1	1	0	0	1	1	1	0	X	X	0				
0	1	1	1	1	0	0	0	1	X	X	1				
1	0	0	0	1	0	0	1	X	0	0	X				
1	0	0	1	1	0	1	0	X	0	0	X				
1	0	1	0	1	0	1	1	X	0	0	X				
1	0	1	1	1	1	0	0	X	0	1	X				
1	1	0	0	0	0	1	1	X	1	X	0				
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

BA \ DC	00	01	11	10
00	×			
01	×		×	
11			×	
10	×		×	

BA \ DC	00	01	11	10
00	×			
01	×		×	
11			×	
10	×		×	

Counters

4-bit Excess-3 counter using JK flip-flops

D	C	B	A	D^+	C^+	B^+	A^+	J_D	K_D	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	0	1	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	0	-	-	-	-	X	X	X	X	X	X	X	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1		
0	1	0	0	0	1	0	1	0	X	X	0	0	X		
0	1	0	1	0	1	1	0	0	X	X	0	1	X		
0	1	1	0	0	1	1	1	0	X	X	0	X	0		
0	1	1	1	1	0	0	0	1	X	X	1	X	1		
1	0	0	0	1	0	0	1	X	0	0	X	0	X		
1	0	0	1	1	0	1	0	X	0	0	X	1	X		
1	0	1	0	1	0	1	1	X	0	0	X	X	0		
1	0	1	1	1	1	0	0	X	0	1	X	X	1		
1	1	0	0	0	0	1	1	X	1	X	0	1	X		
1	1	0	1	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	0	-	-	-	-	X	X	X	X	X	X	X	X
1	1	1	1	-	-	-	-	X	X	X	X	X	X	X	X

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

BA \ DC	00	01	11	10
00	X			
01	X		X	
11			X	
10	X		X	

BA \ DC	00	01	11	10
00	X			
01	X		X	
11			X	
10	X		X	

4-bit Excess-3 counter using J-K flip-flops vs T or SR

- Using T flip-flops:
- Using S-R flip-flops:
- Using J-K flip-flops:

J-K is not always minimal

Different types of flip-flops will yield minimal designs for different count sequences

Watch for things like this in Homework 12-4

Counters

4-bit Excess-3 counter using J-K flip-flops

$J_D = ABC$ $\quad K_D = C$

$J_C = AB$ $\quad K_C = AB + D$

$J_B = A + CD$ $\quad K_B = A$

$J_A = 1$ $\quad K_A = 1$