Chapter 3. Pipelining and Parallel Processing

Exercise Solution

Exercise 1. (a) Sample period T_{sample} of the given DFG is

$$T_{sample} = 4T \tag{3.1}$$

So the maximum achievable sample rate is

$$f_{sample} = \frac{1}{T_{sample}} = \frac{1}{4T} \tag{3.2}$$

(b) The pipelining levels are shown by the dashed lines in Figure 3.1. 9 registers are required.

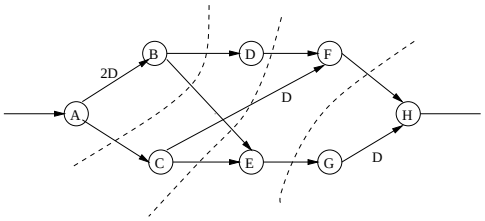

Fig. 3.1 Pipelining levels for Exercise 1(b)

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Exercise Solution

Problem2. (a). The critical path is $M_1 - A_2 - M_2 - A_1 - M_3 - A_3 - A_4$ as shown by the dashed line in Figure 3.1(a). The latency is one clock cycle=10u.t

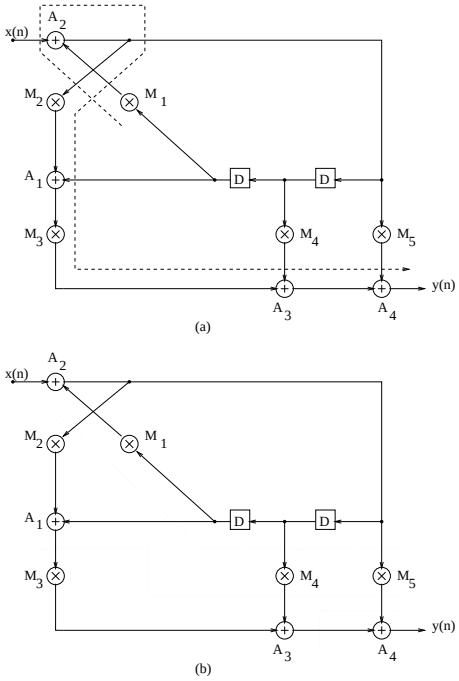

Fig. 3.1 (a). Critical Path Illustration for Exercise 1 (b). Pipelined IIR filter for Exercise 2

(b). Pipelining latches are placed on the dotted lines in Figure 3.1(b). As can be seen, the critical path is one multiply and one add, which is 3 time units. The latency is four clock cycles=$4 \times 3 = 12$u.t

■

Problem5 (a). The pipelining cutset is shown by the dashed line in Figure 3.2(a). Number of delays needed for pipelining=$n + 2n + 1 = 3n + 1$
(b). The block filter architecture is illustrated in Figure 3.2(b). Sample period=$T/3$. Sample rate f_{sample}=3/T. Number of delays needed for pipelining=$9n + 3$

$$y(3k) = ax(3k) + bx(3k-2) + cx(3k-3) \tag{3.1}$$

$$\begin{aligned} y(3k+1) &= ax(3k+1) + bx(3k-1) + cx(3k-2) \\ y(3k+2) &= ax(3k+2) + bx(3k) + cx(3k-1) \end{aligned}$$

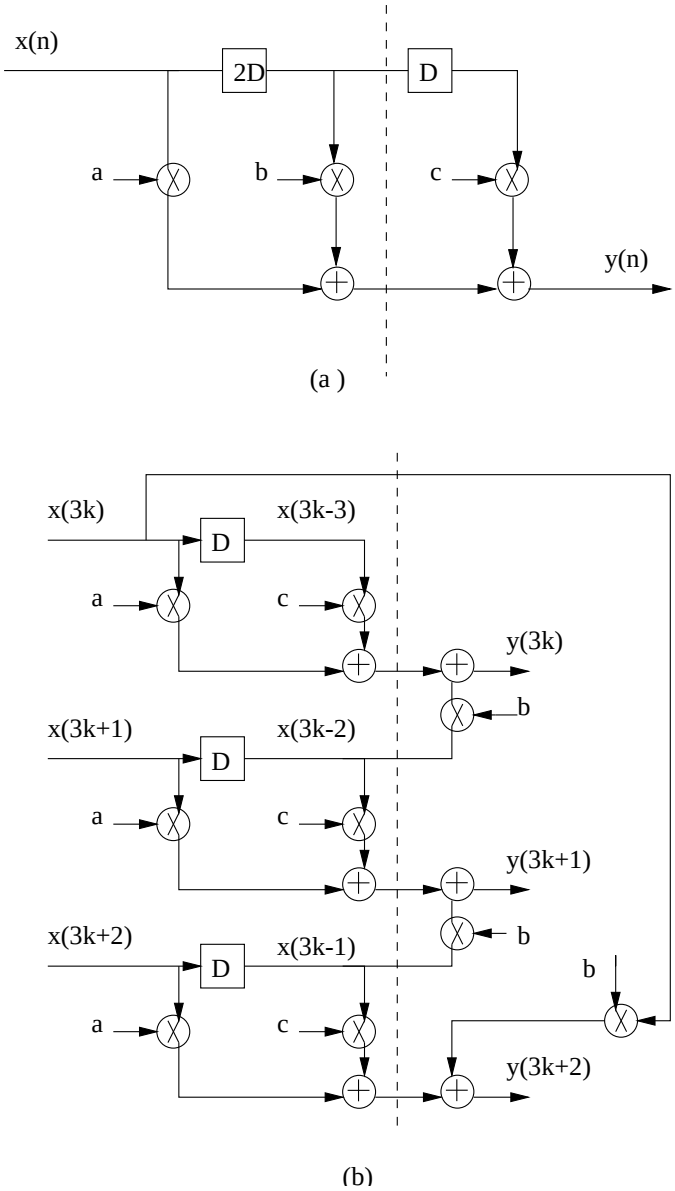

Fig. 3.2 (a):Pipeline of direct-form; (b):Block filter architecture for Exercise 5

Exercise 9. Suppose M level pipelining is needed. Let β be the supply voltage reduction factor, i.e., the supply voltage can be reduced to βV_0 for the pipelined system. From text, the power reduction factor is β^2. Therefore, we have

$$\beta^2 \leq \frac{1}{5}. \tag{3.2}$$

Suppose that the pipelined system and the original system have the same sample rate, we have

$$M = \frac{\beta(V_0 - V_t)^2}{(\beta V_0 - V_t)^2}. \tag{3.3}$$

Take $\beta = \sqrt[2]{0.2} = 0.447$, then

$$M = \lceil \frac{0.447(5 - 0.4)^2}{(0.447 \times 5 - 0.4)^2} \rceil = \lceil 2.8 \rceil = 3. \tag{3.4}$$

Therefore, the system should be pipelined at 3 level. Substitute $M = 3$ into (3.3) and solve for $\beta = 0.427$. The supply voltage for pipelined system is $\beta V_0 = 2.14$ Volts. ■

Exercise 12. Since pipelining level M=4 and block size L=4,we have

$$16(\beta V_0 - V_t)^2 = \beta(V_0 - V_t)^2 \tag{3.5}$$

Substitute V_0=5 Volts and V_t=0.4 Volts in to (3.5), we have

$$\beta^2 - 0.2129\beta + 0.0064 = 0. \tag{3.6}$$

Solving for β, we get

$$\beta = 0.176675, \ or \ \beta = 0.03622. \tag{3.7}$$

$\beta = 0.03622$ is disgarded since $0.03622V_0 = 0.181$ Volts, which is less than the threshold voltage. Therefore, the supply voltage for the parallel pipelined system is $\beta V_0 = 0.883$ Volts. The power ratio is

$$Ratio = \beta^2 = 3.12\%. \blacksquare \tag{3.8}$$