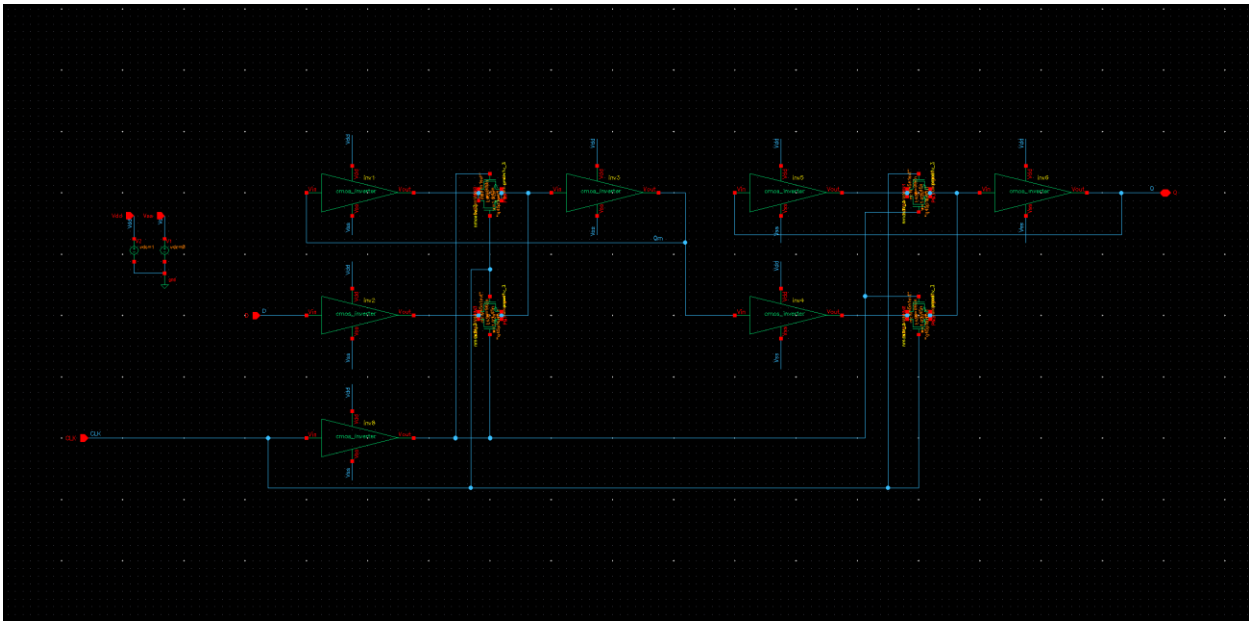
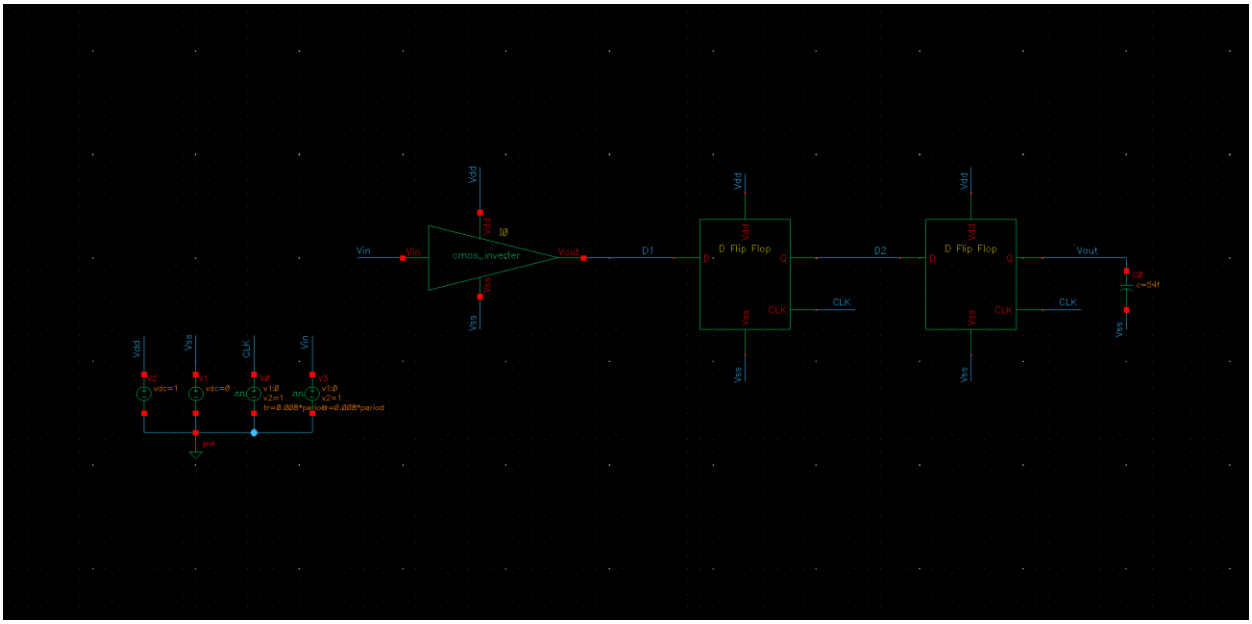
# Homework 6

## Flip Flop



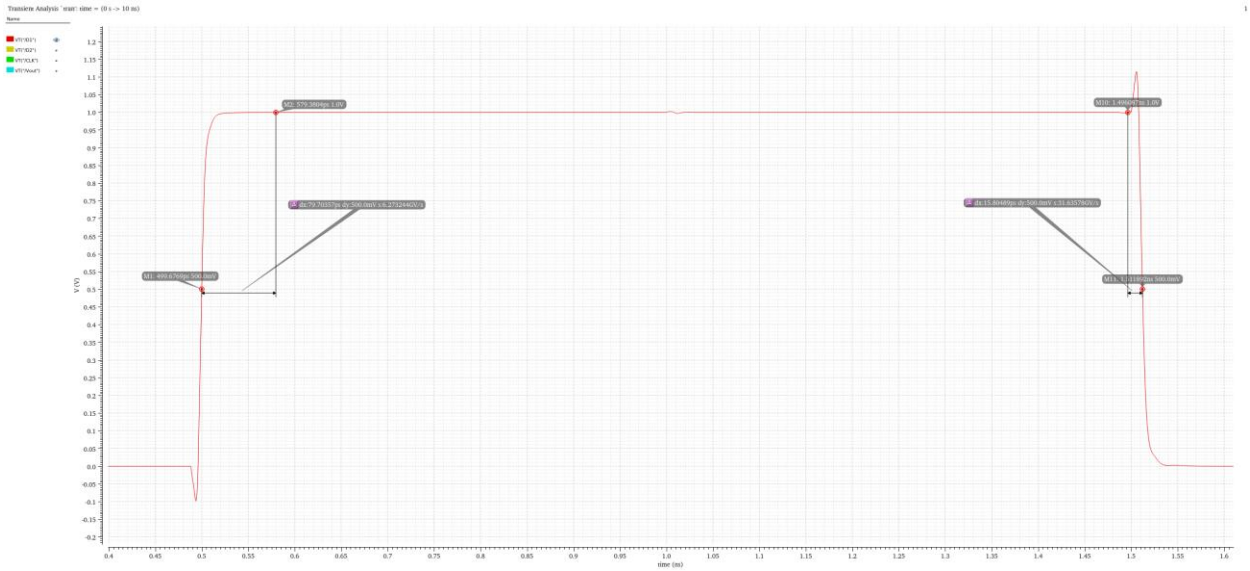
*1.92um PMOS, 0.96um NMOS*

## Flip Flop Test Bench




*54fF Capacitor on Vout*

## Setup Time & Hold Time



$$t_{su} = 79.7ps, \qquad t_h = 15.8ps$$

## CLK to Q time (Falling and Rising Q)

$$t_{cqf} = 40.4ps, \qquad t_{cqr} = 32.6ps$$