ECE 5560 Advanced Hardware Architecture Design Techniques
Course Project

Spring 2025

In the project, you need to conduct thorough literature survey and/or design digital hardware implementation architectures for one of the following topics.

1. High-speed, small-area, low-power, and/or reconfigurable parallel linear feedback shift registers (LFSRs)
2. Hardware accelerator for machine learning
3. Hardware accelerator for fully homomorphic encryption
4. Hardware architecture for post-quantum cryptography
5. A topic of your choice that is relevant to the material of this course. Prior approval from the instructor is needed.

The project report is due 11:59pm EST on April 23, 2025. . The report is limited to 15-page, single-column, and 12-pt font. Please submit your report in either Microsoft Word or PDF format to Carmen.

You may have discussions with other students. However, you must work on your own design and submit your own report.

The grading will be done based on novelty, overall quality, and relevance.

You do not have to write Verilog/VHDL codes or synthesize your design to prove the advantage. Critical path analysis, area requirement comparison, and power consumption estimation similar to what have been discussed in our classes can be used to compare your design with previous work.

Related papers and previous designs can be found by searching the keywords in IEEExplore. Many papers on hardware architecture design are published in the following journals and conferences.

IEEE Transactions on Circuits and Systems-I, II
IEEE Transactions on VLSI Systems
IEEE Transactions on Computers
IEEE International Symposium on Circuits and Systems
IEEE Workshop on Signal Processing Systems
IEEE International Conference on Acoustics, Speech, and Signal Processing