Important

In order to receive credit for this exam you must comply with the policies stated on this page, and you must be able to sign the integrity commitment at the bottom of this page.

You are permitted to use the textbook for this course during the exam.

You are permitted to use your own personal course notes for ECE 2060 during the exam.

You are permitted to use the ECE 2060 Carmen site for this course (the lecture section Carmen site - Class Number 9487) during the exam.

You are permitted to use the equation sheet that is provided with the exam.

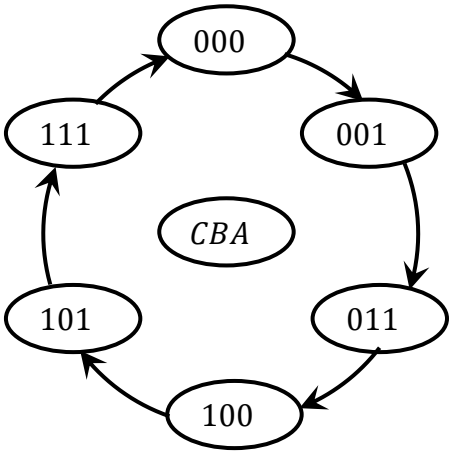
You are permitted to use a calculator.

Integrity Commitment: By signing below I attest that:

1. I will not obtain help from any other person, by any means. The work and answers I submit for the exam will be the product of my effort alone.
2. I will not use any resources other than those stated above (no other books, no other notes, no other online materials or resources, etc.)
3. I will not share my work with anyone else by any means until after the solutions to the exam have been posted on Carmen.

Signature: 	Date: 3/28
Print Name: Gage Farmer	

1. [35 points] The overall goal of this problem is design of a three-bit synchronous counter circuit using T flip-flops, to implement the count sequence shown in the adjacent transition graph.



The logic you design may use only AND and OR gates and may not exceed two levels from flip-flop outputs to flip-flop inputs.

2pts of the problem are reserved for having a minimal design. That is, a design that uses the fewest number of logic gates and inputs. To receive any of those points your circuit must implement the correct count sequence, use only the prescribed types of gates, and not exceed two levels.

a) (10pts) Complete this truth table for the next state of each flip-flop (C^+, B^+, A^+) and the input for each flip-flop (T_C, T_B, T_A) to implement the prescribed count sequence. Do not change any headings or values typed into the table.

C	B	A	C^+	B^+	A^+	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	X	X	X	X	X	X
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	1	0	1	0
1	1	0	X	X	X	X	X	X
1	1	1	0	0	0	1	1	1

b) (10pts) Complete these Karnaugh maps and determine the fully reduced sum of products expression for each of the flip flop inputs. Do not change any of the labels on the K-maps.

BA \ C	0	1
00	0	0
01	0	0
11	1	1
10	X	X

$T_C =$ B

BA \ C	0	1
00	0	0
01	1	1
11	1	1
10	X	X

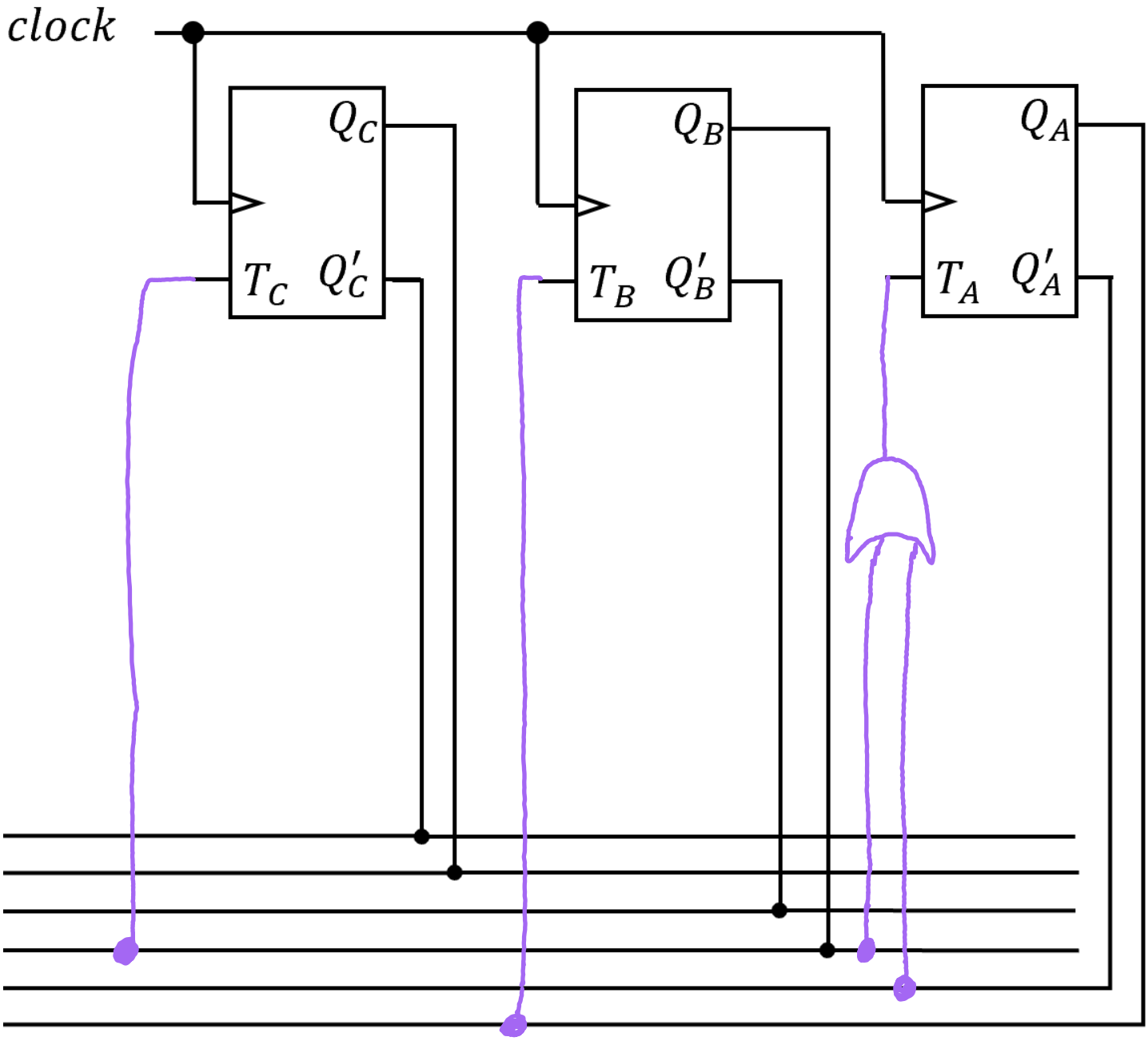
$T_B =$ A

BA \ C	0	1
00	1	1
01	0	0
11	1	1
10	X	X

$T_A =$ B + A'

c) (10pts) Use only AND and OR logic gates to implement the inputs for the flip-flops. Complete this circuit drawing to implement the prescribed counter sequence. Your logic circuits may not exceed two levels from flip-flop outputs to flip-flop inputs.

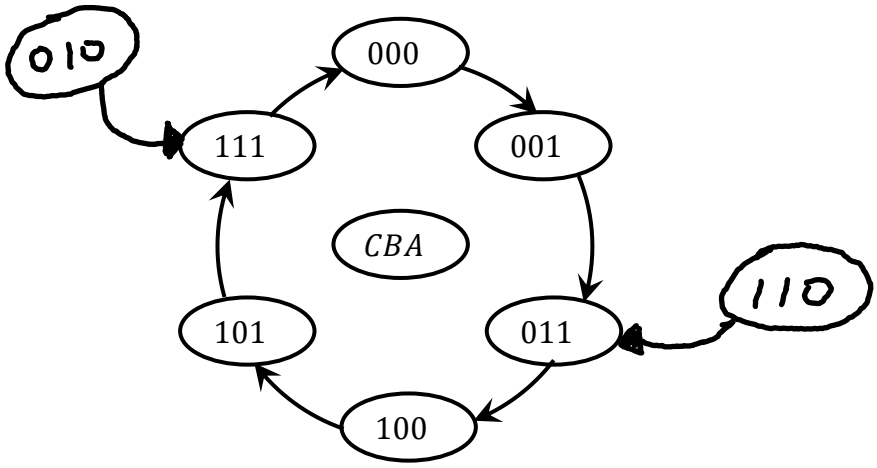
2pts of the problem are reserved for having a minimal design. That is, a design that uses the fewest number of logic gates and inputs. To receive any of those points your circuit must implement the correct count sequence, use only the prescribed types of gates, and not exceed two levels.



d) (5pts) Complete the table below and add the 010 and 110 states to the transition graph below for the way that it is implemented by your circuit. Do not change any headings or values typed into the table.

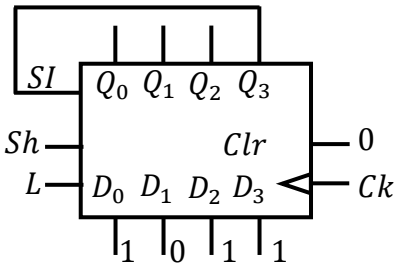
- 5 pts for an answer that is consistent with your circuit and correct for the problem.
- 3pts for an answer that is consistent with your circuit but incorrect for the problem.

C	B	A	T_C	T_B	T_A	C^+	B^+	A^+
0	1	0	1	0	1	1	1	1
1	1	0	1	0	1	0	1	1



Note: (Not needed to work the problem.) This count sequence is weighted 3-1-1 encoding of decimal 0 through 5. That is, it is 60% of the weighted 6-3-1-1 encoding studied in Chapter 1 for decimal 0 through 9. If your design is done correctly your circuit counts 0 through 5 decimal in weighted 3-1-1 encoding. My first draft of this problem was the full 6-3-1-1 counter, but with four flip-flops and four 4-variable K-Maps I determined it made the exam too long for the 36-minute goal.

2. [15 points] A Shift Register is wired as shown. Its operation is described by the adjacent table.



Mode Control					
Sh	***L***	Q_0^+	Q_1^+	Q_2^+	Q_3^+
0	0	Q_0	Q_1	Q_2	Q_3
0	1	D_0	D_1	D_2	D_3
1	×	SI	Q_0	Q_1	Q_2

The register is initially in the cleared state. The top two rows in the table below show the values of the Mode Control inputs at the time of a sequence of rising clock edges. Fill in the remaining cells of the table with the values of the register outputs after the rising clock edges.

Sh	1	0	1	1	0	1	0	1	0
L	1	1	0	1	1	1	0	0	1
Q_0	0	1	1	1	1	1	1	1	1
Q_1	0	0	1	1	0	1	1	1	0
Q_2	0	1	0	1	1	0	0	1	1
Q_3	0	1	1	0	1	1	1	0	1

Equation Sheet

$$X + 0 = X$$
$$X + 1 = 1$$
$$X \cdot 1 = X$$
$$X \cdot 0 = 0$$

$$X + X = X$$
$$X \cdot X = X$$

$$(X')' = X$$

$$X + X' = 1$$
$$X \cdot X' = 0$$

$$XY = YX$$
$$X + Y = Y + X$$

$$(XY)Z = X(YZ) = XYZ$$

$$(X + Y) + Z = X + (Y + Z)$$
$$= X + Y + Z$$

$$X(Y + Z) = XY + XZ$$
$$X + YZ = (X + Y)(X + Z)$$

$$\overline{X + Y} = \bar{X}\bar{Y}$$
$$\overline{XY} = \bar{X} + \bar{Y}$$

Half Adder

$$S = X'Y + XY' = X \oplus Y$$
$$C = XY$$

Full Adder

$$S = X \oplus Y \oplus C_{in}$$
$$C_{out} = XY + XC_{in} + YC_{in}$$

$$Q^+ = S + R'Q \ (SR = 0)$$
$$Q^+ = D$$
$$Q^+ = JQ' + K'Q$$
$$Q^+ = TQ' + T'Q$$

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0