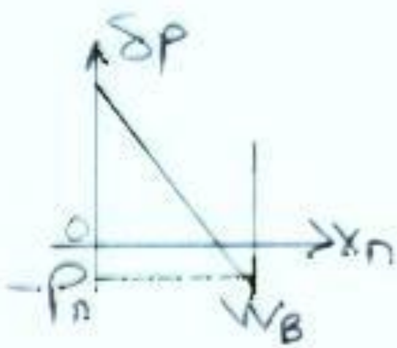
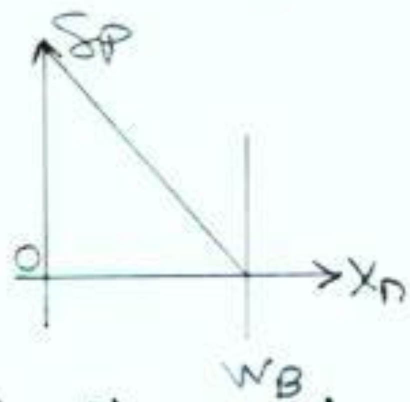
Saturation Regime

V_{EB} forward $\quad V_{CB} = 0$ or forward

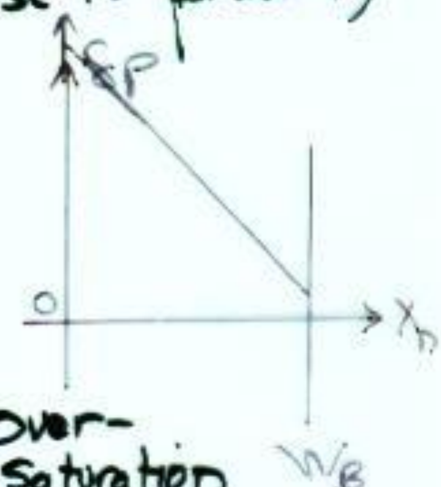
(onset as V_{CB} crosses 0 from reverse to forward)



normal



Saturation onset



over-saturation

How does collector junction BC get forward biased? $\rightarrow$

Load line fixed by R_L and V_{cc}

- Increasing i_B moves intersection to higher i_c and lower $-v_{CE}$
- At high enough i_B, i_c = saturation = 8mA = fixed and v_{CE} very small
- Higher i_B $\rightarrow$ i_c

  BC forward $\rightarrow$ state

Look at another way :

- To maintain neutrality, a given stored charge is required to compensate a given i_B so an increase in i_B forces an increase in area under $\delta p(x_n)$ vs. x_n distribution 

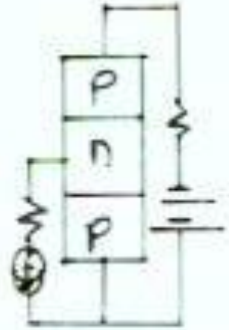
- Also - i_C increases as $i_C = \beta i_B$ up to saturation and V_{CB} forced from reverse to forward to supply it.

Oversaturation for switching

→ More charge in base, but same current (same slope)

→

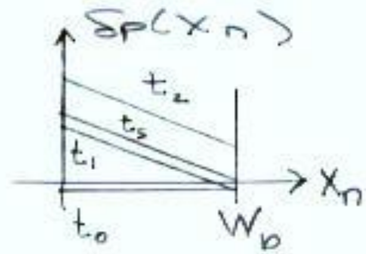
Switching Cycle



Regime	Emitter	Collector	State
t_0 = cutoff			
t_1 = normal active			
t_s = saturation onset			
t_2 = oversaturation (final)			

Hole Distribution

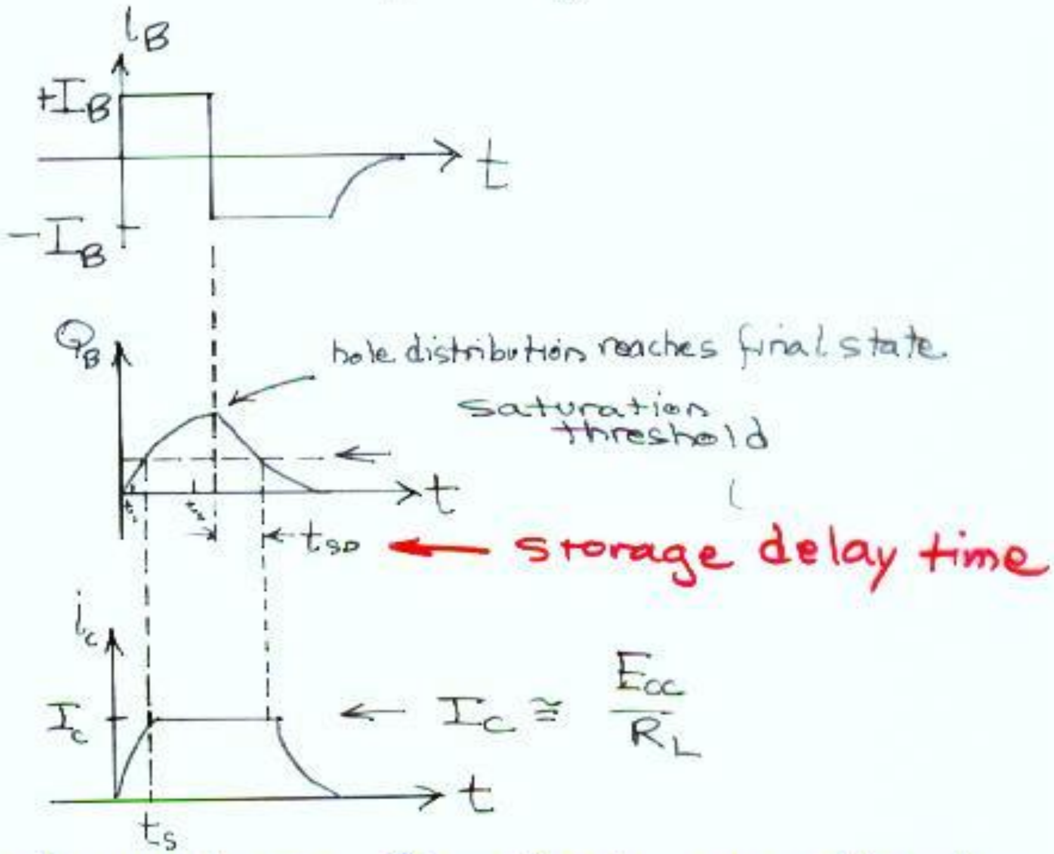
t_s = saturation t



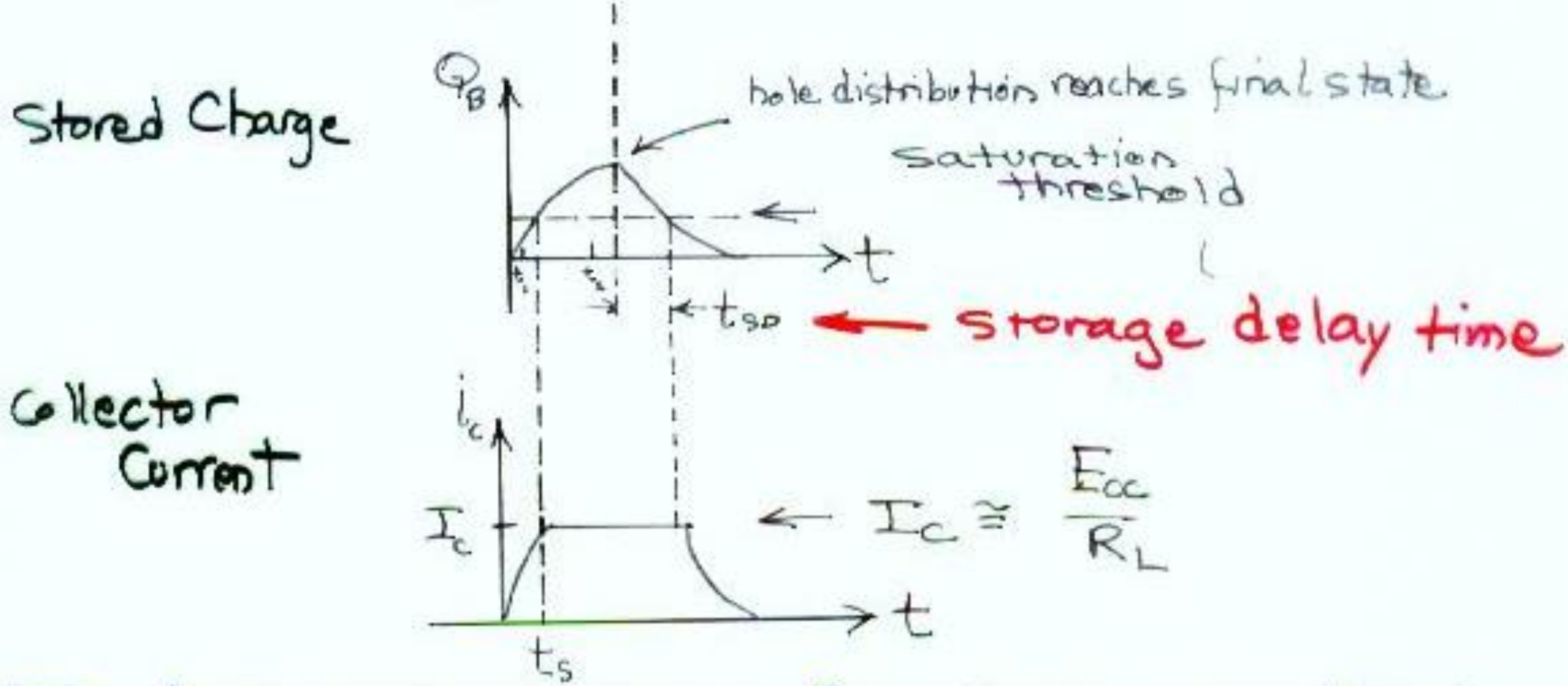
Base Current

Stored Charge

Collector Current



I_c does not increase for $t > t_s$ even though Q_B continues to increase.



I_C does not increase for $t > t_s$ even though Q_B continues to increase.

t_{so} = storage delay time — too much Q!

Tricks to shorten switching delay:

- lower τ_p by adding recombination centers
- Schottky clamp – excess charge pulled off around BC

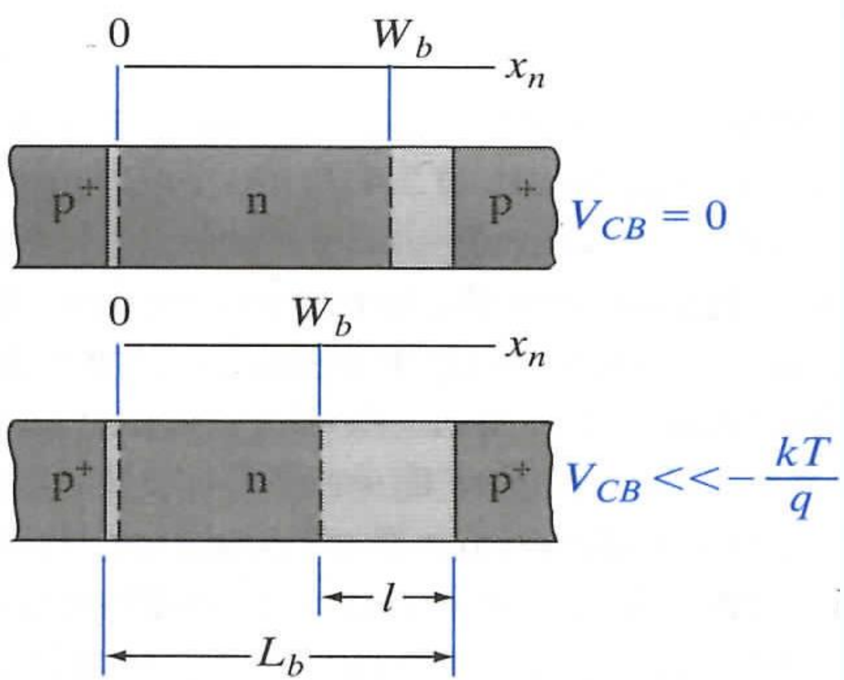
→ Vclamped 10x faster

Secondary Effects

(extra drift, adds field, speeds up τ transit)

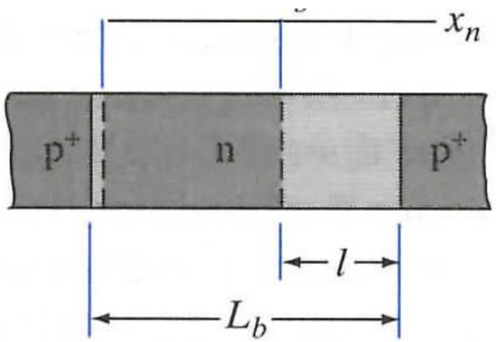
Base Narrowing

- Bias voltage can affect base W_b



$W_b \simeq L_b - l$

$l \propto \sqrt{V_{BC}}$



$V_{CB} << -\frac{kT}{q}$

$W_b \simeq L_b - l$

$l \propto \sqrt{V_{BC}}$

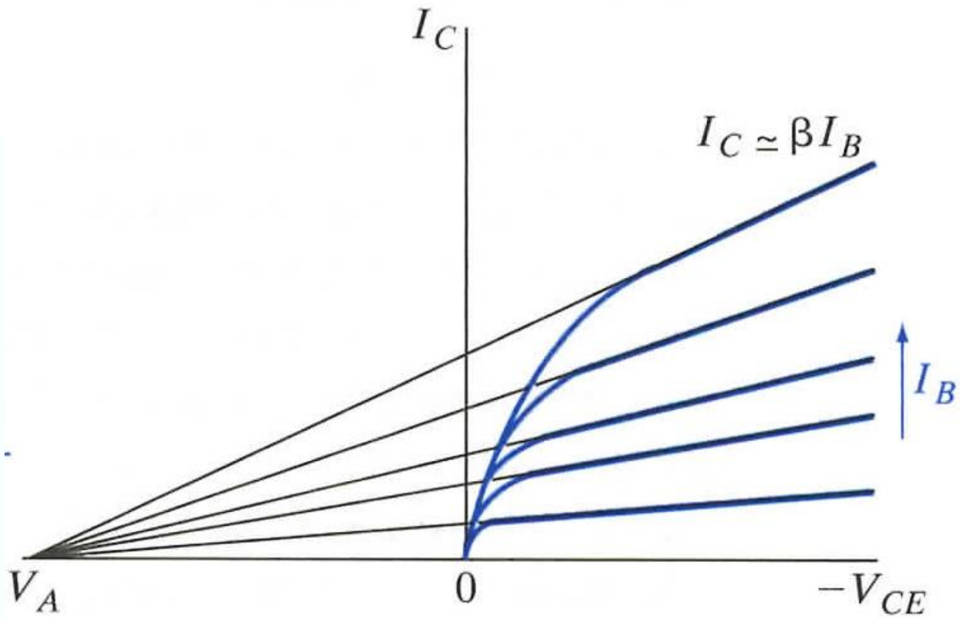
Reverse bias in lightly-doped n-type base extends significantly into base

→

OSU Grad ?

with collector voltage.

$\frac{i_C}{i_B} = \beta$ =



Effect extrapolates to zero when base width effect cancelled out by V

Extrapolate to Early Voltage V_A

- For high enough reverse V, $W_b \rightarrow \sim 0$

→ holes swept directly from E to C; no transistor action.

(avoid by graded doping, light at E, heavy at C)

Slope due to 3 phenomena:

1. Surface current around CB junction
2. Less recombination in base as W shrinks
3. Depletion region widens so generation current increases (apparent only at small I_E)

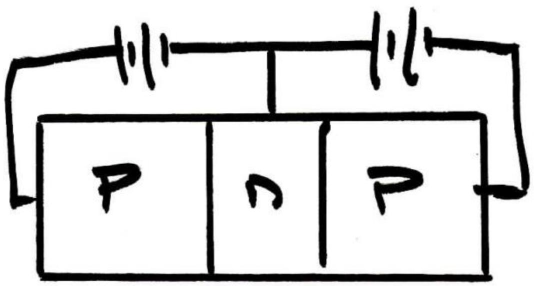
so charge swept into base and emitter generates more I_C.

$\beta = \frac{\tau_p}{\tau_t}$ so as $\tau_t \rightarrow \infty$, $\beta \rightarrow 0$

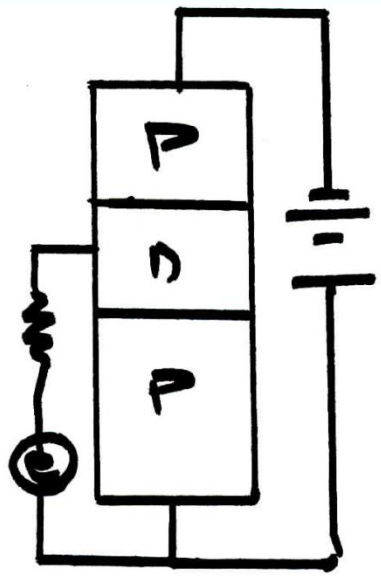
and Early Effect is gone!

So V_A equivalent to ∞ W_b (no base modulation)

Note difference between common-base
and common-emitter configurations



Amplification



Switching, Variable Gain

Other Effects

Avalanche Breakdown -

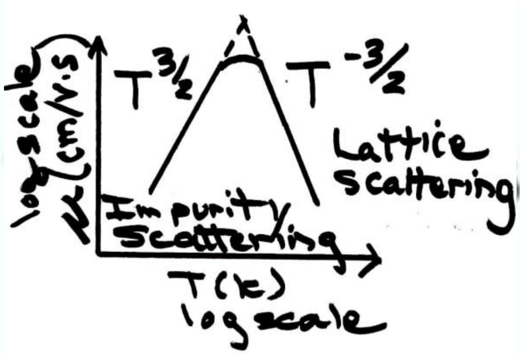
Larger in common-emitter configuration than in common-base configuration since avalanche at CB demands more i_B → more avalanche.

Injection Dependence on Thermal Effects -

(significant for low I_E

- τ_p increases with temperature
- competing effects on gain, β :

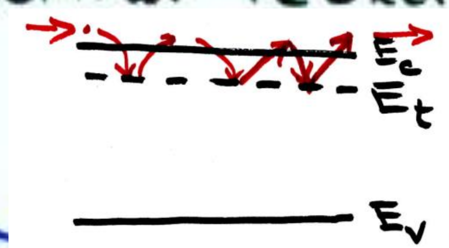
Lattice scattering increases as $T^{+3/2}$



μ decreases as $T^{-3/2}$

$D = \frac{kT}{q}\mu$ decreases, τ_t increases.

<u>But</u> thermal reexcitation increases τ_p



overall

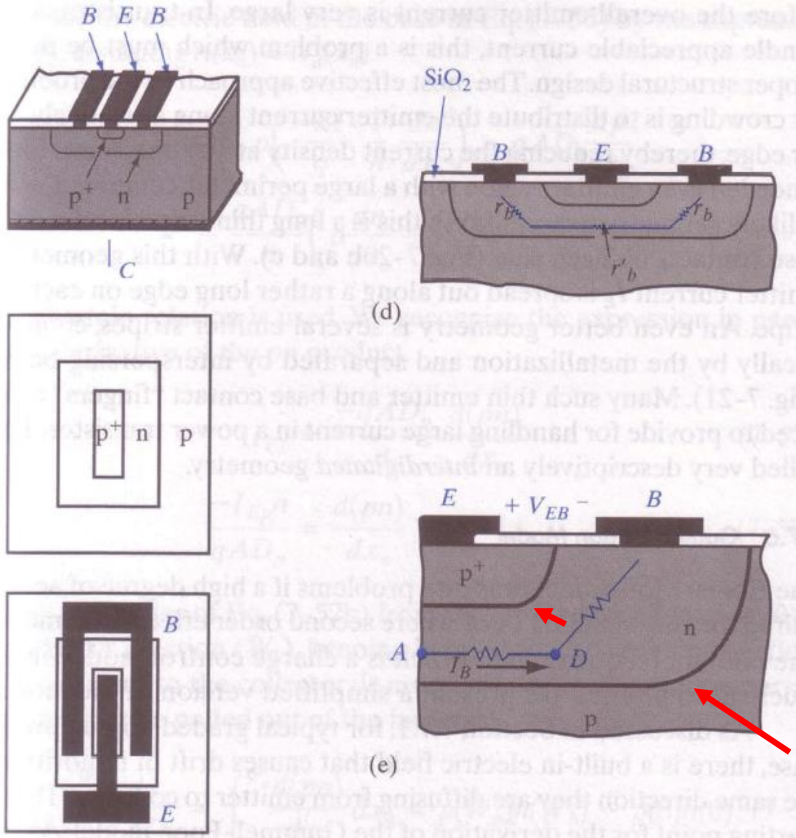
So $\beta = \frac{\tau_p}{\tau_t}$ increases overall.

Could draw larger I_C as T increases

→ Thermal Runaway!

Base Resistance and Emitter Crowding

- Base resistance varies with base geometry
- Under forward bias, emitter injection varies as bias varies with location:



Voltage drop occurs across r_b'

$$V_{EA} = V_{EB} - I_B(R_{AD} + R_{DB})$$

$$V_{ED} = V_{EB} - I_B(R_{DB})$$

Forward bias largest at edge of emitter

→ Emitter Crowding: High injection near corners of emitter.

Design for large emitter edge to distribute emitter current and reduce density.

Frequency Limitations

7.8.2, 7.8.3 (7.8.4, 5th)

Transit time across the base often limits high frequency.

$$\beta \simeq \frac{\operatorname{csch} W_b/L_p}{\tanh W_b/2L_p} = \quad = \frac{2D_p\tau_p}{W_b^2} \equiv \frac{\tau_p}{\tau_t}$$

$$\tau_t =$$

Decrease base width or increase μ.

Example: $W_b = 1\mu m$ $D_p \sim 10 cm^2/sec$ for Si

so $\tau = 0.5 \times 10^{-9}$ sec

$f_{max} \sim \frac{1}{2\pi \tau_t} \sim 320$ MHz (actually lower due to other limitations)

$f_T \equiv (2\pi \tau_{delay})^{-1}$

$W_b \rightarrow 0.1\mu m$, $f_{max} \rightarrow 32$ GHz

or increase D_p (μ)

But small size → lower power rating

→ frequency - power tradeoff

Also, since $\beta = \frac{\tau_p}{\tau_t}$, higher gain with shorter W_b

→ gain - power tradeoff.