ECE5560 Spring 2025

HW 4

Reading:

Section 3.2, 3.3, 3.4

Problems:

1) Problem 1 of Chapter 3. Note the following definition

   Sample rate=$\frac{1}{sample\ period}$
   Sample period= time needed to process a sample.
   For this DFG, since one sample is processed in each clock cycle, sample rate =1/clock period.

2) Problem 2 of Chapter 3 in the textbook. Also compare the latency of the filter before and after the pipelining.

3) Problem 5 (a)(b) of Chapter 3 in the textbook. Assume that the multiplication of two n-bit numbers generates a product of 2n bits. The addition of two n-bit numbers generates a sum of n+1 bits. How many delay elements are needed for pipelining in each architecture? (block size of three in this problem means that the parallel processing factor is three)

4) Problem 9 of Chapter 3

5) Problem 12 of Chapter 3