ECE 5362 – Homework 4

1.

a) ot5, ib, comp, p1, oadder
b) Can't read from and write to the same register in 1 cycle
c) oa, p1, oadder
d) Can't read from and write to the same register in 1 cycle
e) rac = 1, rn = 2, comp, p1
f) Can't write and read to the combinational circuit in 1 cycle
g) Can't have two values on the bus during 1 cycle
h) Can't have two values on the bus during 1 cycle
i) comp, oa, oadder
j) oadder, ot2, it4
k) Can't remove value from IR
l) write, oa, p1, oadder, wac = 1, wn = 0, it5

2.

Address	Data	Function	op2	sad/op1	dad	S	D
0x00	0x22X0	MOVE SP, -(X)	b0010	b0000	b0011	b10	b01
0x01	0x1F02	SUB #20, SP	b0001	b1111	b0000	b00	b10
0x02	0x0014	#20	b0000	b0000	b0001	b01	b00
0x03	0x1108	ADD (SP), AC	b0001	b0001	b0000	b10	b00
0x04	0x4404	EXG -2(X), AC	b0100	b0100	b0000	b01	b00
0x05	0x0321	NEG (X)+	b0000	b0011	b0010	b00	b01
0x06	0x3601	MOVE #DATA, X	b0011	b0110	b0000	b00	b01
0x07	0x0017	#DATA	b0000	b0000	b0001	b01	b11
0x08	0x0000	CLR AC	b0000	b0000	b0000	b00	b00
0x09	0x0750	JSR FUNC	b0000	b0111	b0101	b00	b00
0x0A	0x000C	#FUNC	b0000	b0000	b0000	b11	b00
0x0B	0x0000	HALT	b0000	b0000	b0000	b00	b00
0x0C	0x3500	MOVE DATA, AC	b0011	b0101	b0000	b00	b00
0x0D	0x00CD	DATA	b0000	b0000	b1100	b11	b01
0x0E	0x0100	INC AC	b0000	b0001	b0000	b00	b00
0x0F	0x0201	DEC X	b0000	b0010	b0000	b00	b01
0x10	0x0081	BPL LOOP	b0000	b0000	b1000	b00	b01
0x11	0x000F	LOOP	b0000	b0000	b0000	b11	b11
0x12	0x0550	JMP END	b0000	b0101	b0101	b00	b00
0x13	0x0015	END	b0000	b0000	b0001	b01	b01
0x14	0xFFFF	CLRC	b0000	bFFFF	b0000	bFF	bFF
0x15	0x0080	RTS	b0000	b0000	b1000	b00	b00
0x16	0x0000						
0x17	0x00CD	DATA					
Address	Data	Function					
0x00	0x0000	AC					
0x01	0x0000	X					
0x02	0x0000	SP					
0x03	0x0000	PC					
0x04	0x0000	CVZN					

3.

Address	Data	Reg	Function	s	d
0x00	0xFF00	AC			
0x01	0x000F	X			
0x02	0x0012	SP			
0x03	0x0000	PC			
0x04	0x0000	CVZN			
0x05	0x0411		complement	[[X]]	
0x06	0x4104		exchange	[[X]]	AC
0x07	0x0421		complement	(X)+	
0x08	0x4204		exchange	(X)+	AC
0x09	0x0432		complement	_-(SP)	
0x0A	0x4031		exchange	AC	_-(X)
0x0B	0x0442		complement	n(SP)	
0x0C	0xFFFF		n	0xFFFF	
0x0D	0x4042		exchange	AC	n(SP)
0x0E	0xFFFE		n	0xFFFE	
0x0F	0x4050		exchange	AC	n
0x10	0x000F		n	0x000F	
0x11	0x0450		complement	n	
0x12	0x0010		n	0x0010	
0x13	0x0000		halt		
0x14	0x0001		CLR	x	
0x15	0x00FF		data	0x00FF	
0x16	0x0002		CLR	SP	

Summary.1:

```
memory write:: FFFF->M(   F)
  At end of instruction 1
    ac     x    sp    pc    cvzn
  FF00     F    12     1    0000
 memory write:: 0000 ->M(   F )
  At end of instruction 2
    ac     x    sp    pc    cvzn
  0000     F    12     2    0000
 memory write:: FF00 ->M(   F)
  At end of instruction 3
    ac     x    sp    pc    cvzn
  0000    0001  12     3    0000
 memory write:: FFFF ->M( FFFF )
  At end of instruction 4
    ac     x    sp    pc    cvzn
  0001    0000  12     4    0000
```

```
 memory write:: FFFF ->M( FFFF )
  At end of instruction 5
    ac     x    sp    pc    cvzn
  0001    0000  000E   5    0000
 memory write:: FFFF ->M( FFFF )
  At end of instruction 6
    ac     x    sp    pc    cvzn
  FFFF    0001  11     6    0001
 memory write:: FFFF ->M( FFFF )
  At end of instruction 7
    ac     x    sp    pc    cvzn
  FFFF    10    11     8    0001
 memory write:: FFFF ->M( 0010 )
  At end of instruction 8
    ac     x    sp    pc    cvzn
  000F    10    11     A    0001
 memory write:: FFFF ->M( 000F )
  At end of instruction 9
    ac     x    sp    pc    cvzn
  FFFF    10    11     C    0001
 memory write:: 000F ->M( 000F )
  At end of instruction 10
    ac     x    sp    pc    cvzn
  FFFF    10    11     E    0000
```