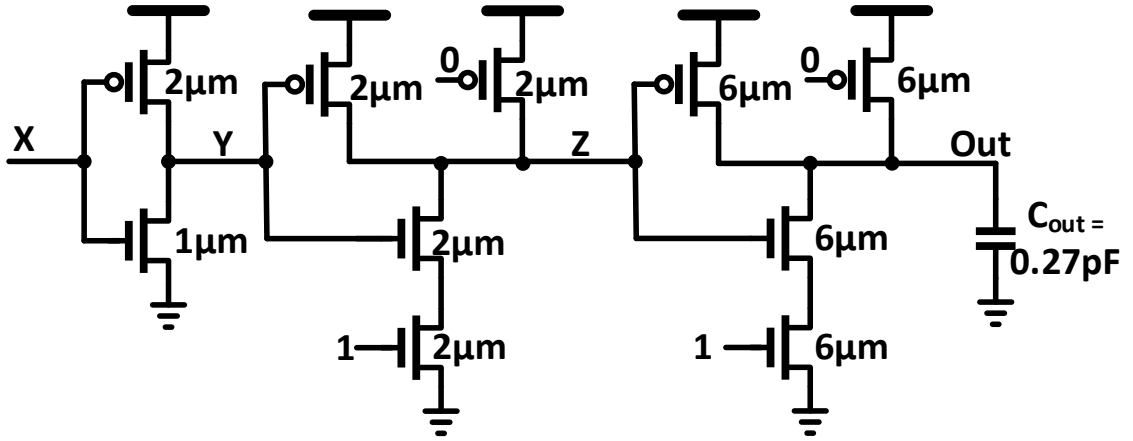
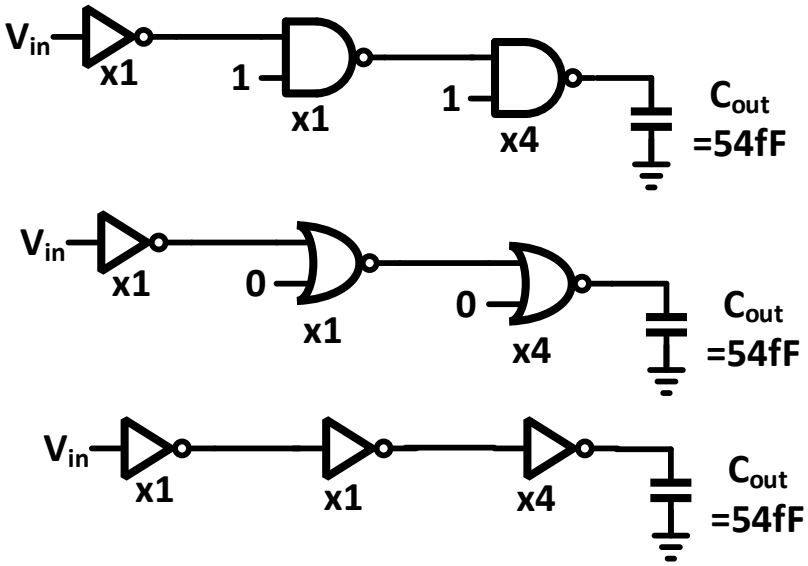
Autumn 2024 – ECE 5020
Homework 4

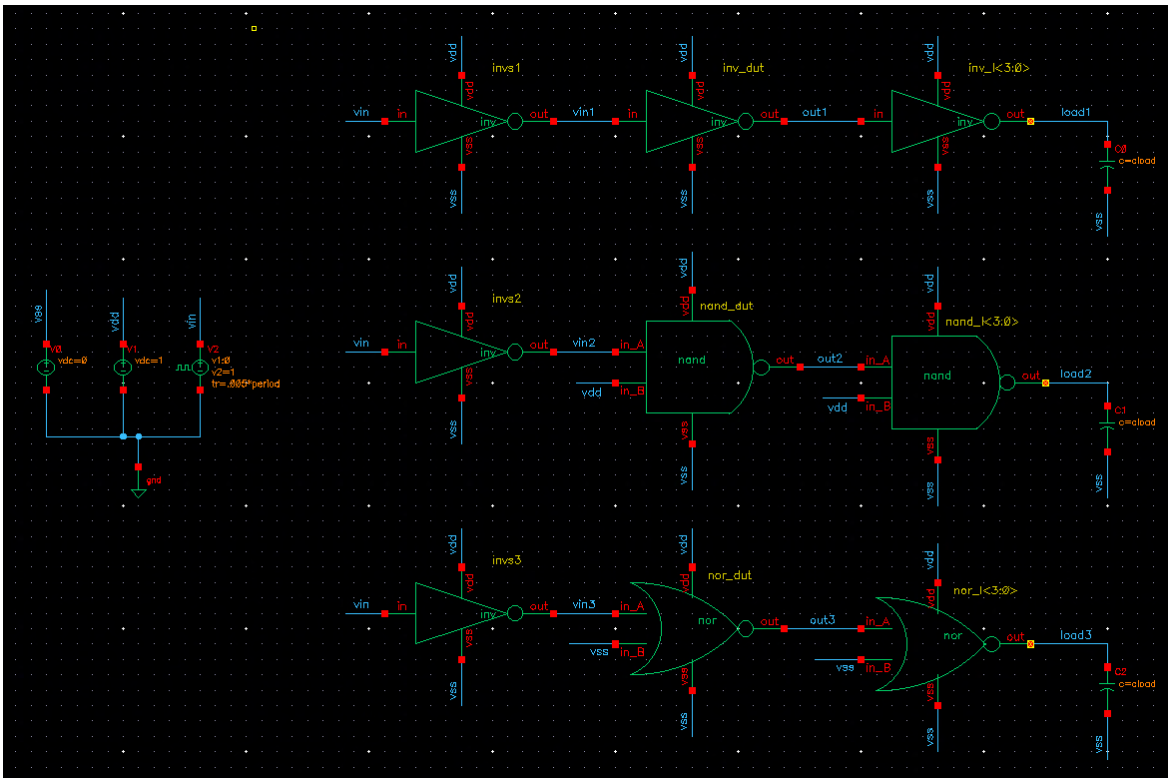
Due: 10/02/2024

1.
   a. Sketch a 3-input NOR gate and size the transistors to equal pull-up and pull-down strengths as a unit inverter (W_p = 2um, W_n =1um). Show why the logical effort is 7/3.
   b. Repeat the above exercise for a 3-input NAND. What is the logical effort?
2. For the logic chain below
   a. Calculate the total delay given the annotated sizes.
   b. Resize to minimize delay. What is the new delay?
   c. If you can add an even number of inverters, what is the number of stages that yields the minimum delay?



3. **(Simulation)** Sketch 2-input NAND and NOR gates and size the transistors to have equal pull-up and pull-down strengths similar to the inverter of HW 2 (W_p = 1.92um, W_n =0.96um).
   a. Create schematics and symbols for the NAND and NOR circuits in Cadence Virtuoso as you did for the inverter.
   b. Build a testbench to simulate FO4 delays for the inverter, NAND and NOR (see the figure on page 2). Do the results match you expectations? [Use 1GHz as the input frequency, with 8ps rise/fall times. The FO4 delay is the measured delay (t_p) between the input and output of the middle x1 device]
   c. Hand in your sized INV, NAND and NOR sketches and the measured FO4 delays from your simulations.


Vin
x1
1
x1
1
x4
Cout
=54fF
Vin
x1
0
x1
0
x4
Cout
=54fF
Vin
x1
x1
x4
Cout
=54fF


invs1
inv_dut
inv_I<3:0>
invs2
nand_dut
nand_I<3:0>
invs3
nor_dut
nor_I<3:0>
vin
vin1
out1
vin2
out2
vin3
out3
load1
load2
load3
vdd
vss
gnd
vdc=0
vdc=1
v1:0
v2=1
tr=.005*period