Draw a 2-level NAND-NAND logic circuit that implement the following functions with the minimum number of gates. Note that is says 2-level, not 2-input – this problem does not have a fan-in limit.

$F(A,B,C,D) = A'B' + B'D + A'C'D'$ $G(A,B,C,D) = AC' + AB'D + C'D'$

The output of the previous block of the system has each of A, A', B, B', C, C', D and D' available as inputs to your circuit on the wires shown below.