ECE 5560 Project Example
Implementation Architectures of Linear Feedback Shift Registers

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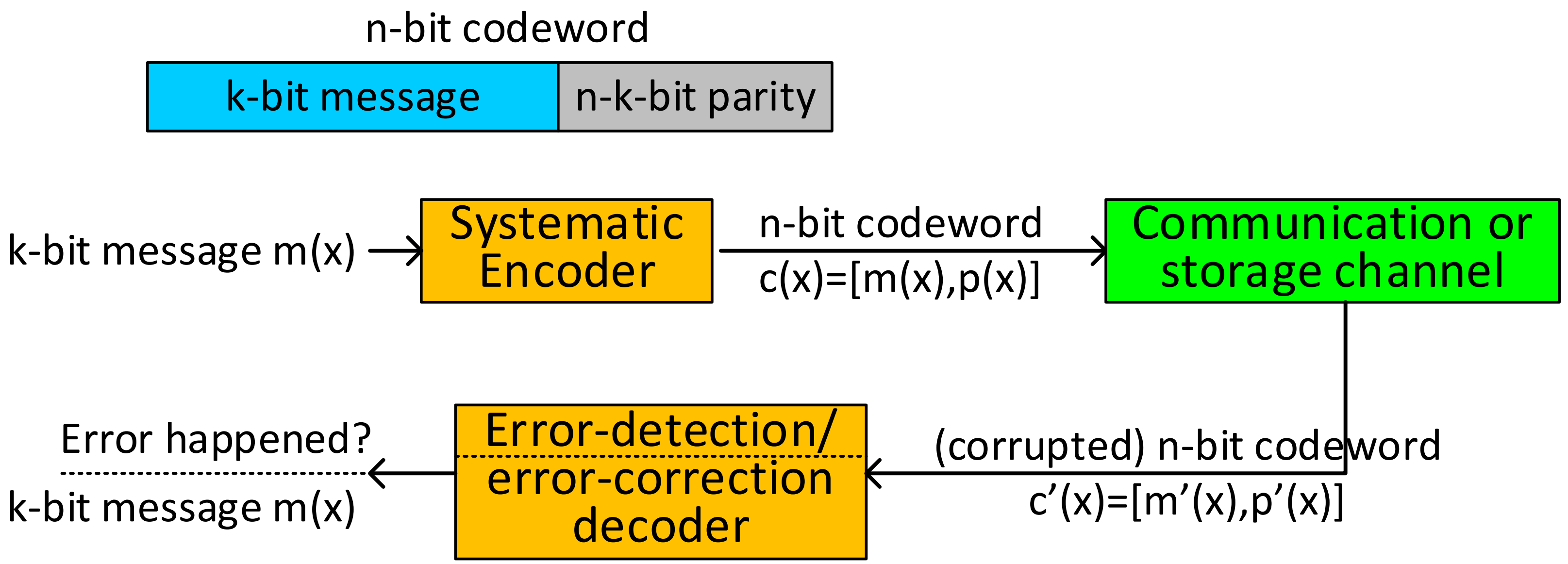
Applications of Linear Feedback Shift Registers (LFSRs)

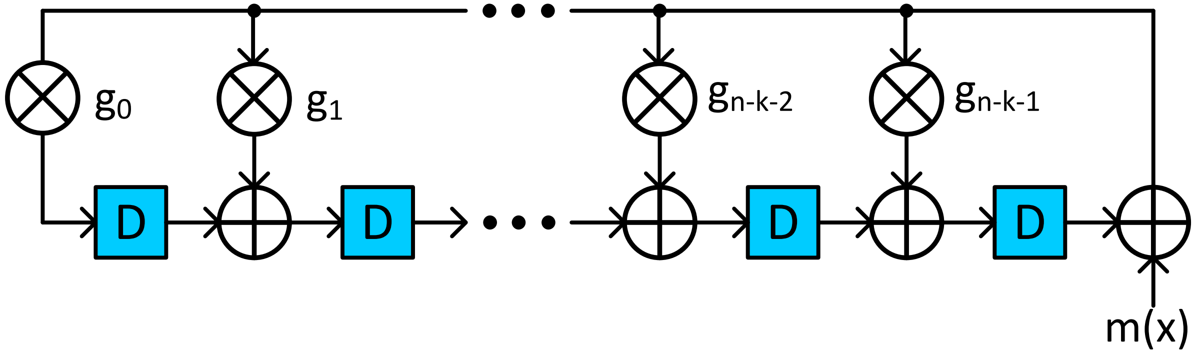
- Used in many digital communication and storage systems
  - Encoder and decoder of cyclic redundancy check (CRC) code for error detection
  - Encoder of Bose–Chaudhuri–Hocquenghem (BCH) codes for error correction



Architecture of Serial LFSRs

- Generator polynomial: $g(x)$, $\deg\big(g(x)\big) = n - k$
- BCH and CRC encoders: compute parity polynomial $p(x) = m(x)x^{n-k}\ mod\ g(x)$
- CRC decoder: compute $p''(x) = m'(x)x^{n-k} mod\ g(x)$; if $p''(x) = p'(x)$, then no error occurred

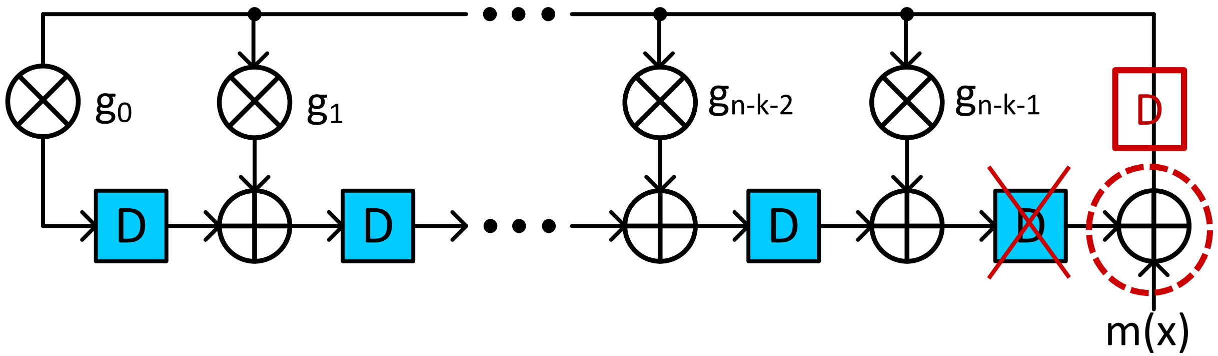
Serial LFSR



- $g(x) = g_0 + g_1 x + \cdots g_{n-k-1} x^{n-k-1} + x^{n-k}$
- Each multiplier is replaced by a wire or no connection when $g(x)$ is binary
- $m_{k-1}, m_{k-2,} \cdots, m_0$ are sent in serially
- $p(x)$ is located in the registers after the message bits are sent in

Parallel LFSRs for Long BCH Encoders

- $\deg(g(x))$ can be several hundreds for long BCH codes used in optimal communications and data storage
- A register is needed at the output of the right-most XOR gate to address the large fanout issue
- Parallel LFSRs are needed to achieve high speed in many systems



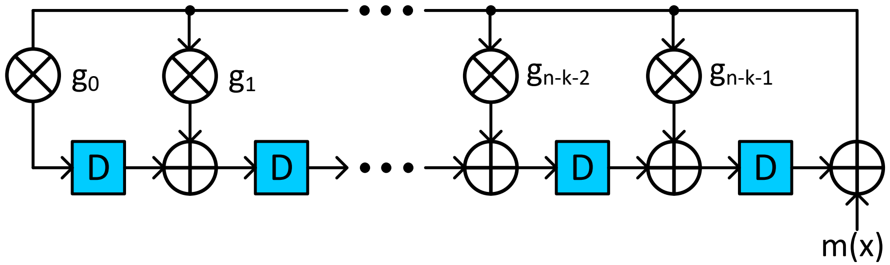
- How can I have enough registers between the two right-most XORs so that retiming can be applied in the unfolded architecture to move at least one register to the output of each copy of the right-most XOR?
- What is the iteration bound of the LFSR? Can I improve the iteration bound and hence reduce the achievable clock period by manipulating the generator polynomial?

References: [1-3]

Parallel LFSRs for CRC

- $\deg(g(x)) \leq 32$ for CRC
- Need high-speed, small-area, and/or low-power implementations

Serial LFSR



- Denote the register state at clock cycle t by

$$r(t) = [r_{n-k-1}(t), r_{n-k-2}(t), \cdots, r_0(t)]'$$

$$\downarrow$$

$$r(t+1) = A \times r(t) + b \times m(t)$$

$$\mathbf{A} = \begin{bmatrix} g_{n-k-1} & 1 & 0 & \cdots & 0 \\ g_{n-k-2} & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & 0 \\ g_1 & 0 & 0 & \cdots & 1 \\ g_0 & 0 & 0 & \cdots & 0 \end{bmatrix}$$

$$\rightarrow$$

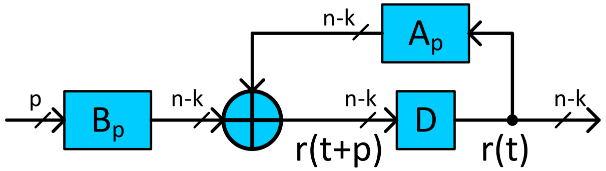
$$r(t+p) = A^p \times r(t) + \mathrm{B_p} \times m_p(t)$$

$$B_p = [A^{p-1}b, \cdots Ab, b]$$

$$m_p(t) = [m(t), \cdots, m(t+p-2), m(t+p-1)]'$$

$$b = [g_{n-k-1}, g_{n-k-2}, \cdots, g_0]'$$

p-parallel LFSR



Transformed Parallel LFSRs

$$r(t+p) = A^p \times r(t) + \mathrm{B_p} \times m_p(t)$$

$$\Big\downarrow \; r(t) = T \times r_T(t)$$

$$r_T(t+p) = A_{pT} \times r_T(t) + \mathrm{B_{pT}} \times m_p(t)$$

$$A_{pT} = T^{-1} \times A^p \times T$$

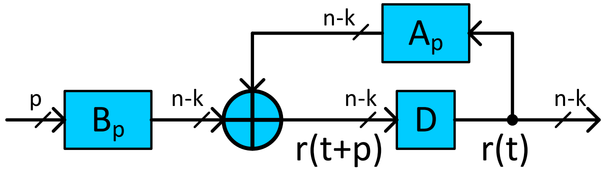
$$B_{pT} = T^{-1} \times B_p$$

- Transformation can be designed to reduce
  - critical path
  - gate count
  - power consumption

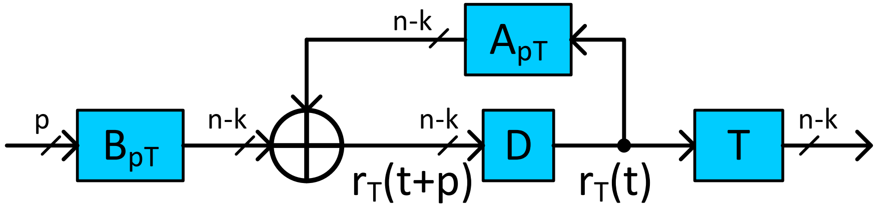
- Can we design a better transformation that leads to a faster, smaller, and/or lower-power design?

References: [4]-[10]

p-parallel LFSR



Transformed p-parallel LFSR



Other Variations of Parallel LFSR Architectures

- LFSR function is interpreted as recursive filtering
- Parallel LFSRs are derived by parallel processing techniques for recursive filters

References: [11][12]

- LFSRs with various generator polynomials $g_1(x), g_2(x), \cdots, g_r(x)$ need to be implemented in the same system
- The generator polynomials satisfy the constraints that $g_i(x)$ divides $g_j(x)$ if $\deg\left(g_i(x)\right) < \deg(g_j(x))$
- Multi-mode LFSRs share hardware units to implement all required polynomial divisions

References: [13]

References

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