AMERICAN INTERNATIONAL UNIVERSITY–BANGLADESH (AIUB)
FACULTY OF SCIENCE & TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
DIGITAL LOGIC AND CIRCUITS LABORATORY

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OEL REPORT ON

Deriving logic equations and truth table from a given statement or expression and construction of combinational circuits with only 2 input NAND gates.

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THEORY:

From any given logic statement, it is possible to construct a digital logic circuit. The first step in this process is to construct a truth table and then determine a standard SOP (Sum of product) or POS (product of sum). Here, we did for SOP equation. At the same time, it is also possible to derive a logic expression from a given combinational circuit diagram by observing the individual logic operations performed in the circuit and matching them with their corresponding logic gates. Expressions are simplified using Boolean algebra and De Morgan's law or K-Map to reduce the number of gates used. Then the circuit is implemented in the breadboard using gate ICs and observed whether the output verifies the truth table of the given statement.

Boolean algebra:

Boolean Algebra is a mathematical system based on logic that utilizes a set of rules and laws to simplify and reduce complex Boolean expressions, enabling the analysis and optimization of digital gates and circuits with variables that can only take on the values of 0 or 1.

Sum of Products (SOP):

When two or more product terms are summed by Boolean addition, the resulting expression is a sum of product. Implementing an SOP expression simply requires ORing the outputs of two or more AND gates. Product term is produced by an AND operation, and the sum (addition) of two or more product terms is produced by an OR operation. Therefore, an SOP expression can be implemented by AND-OR logic in which the outputs of a number (equal to the number of product terms in the expression of AND gates connect to the inputs of an OR gate. A standard SOP expression is one in which all the variables in the domain appear in each product term. Ex. Standard SOP expressions are important in constructing truth-tables and in Karnaugh map simplification method. The SOP expression is equal to 1 only if one or more of the product terms in the expression are equal to 1.

Karnaugh Map:

Karnaugh map or K-map is a map of a function used in a technique used for minimization or simplification of a Boolean expression. It results in a smaller number of logic gates and inputs to be used during the fabrication. Booleans expression can be simplified using Boolean algebraic theorems but there are no specific rules to make the most simplified expression. However, K-map can easily minimize the terms of a Boolean function. Unlike an algebraic method, K-map is a pictorial method, and it does not need any Boolean algebraic theorems. K-map is basically a diagram made up of squares. Each of these squares represents a min-term of the variables. If n = number of variables, then the number of squares in its K-map will be 2n. K-map is made using the truth table. In fact, it is a special form of the truth table that is folded upon itself like a sphere. Every two adjacent squares of the k-map have a difference of 1-bit including the corners. Karnaugh map can produce Sum of product (SOP) or product of Sum (POS) expression considering which of the two (0,1) outputs are being grouped in it. The grouping of 0's result in Product of Sum expression & the grouping of 1's result in Sum of Product expression. The expression produced by K-map may be the most simplified expression but not unique. There can be more than 1 simplified expression for a single function, but they all perform the same.

Apparatus:

- Digital trainer board.
- IC or Integrated Circuits:
    1. 7432 (1 pcs)
    2. 7408 (2pcs)
    3. 7404 (1pcs)
- Connecting wires.

Experimental Procedure:

a) At first, we used the output F to form standard SOP expression.
b) Then we minimized the SOP expression using Boolean algebra and K-Map. Perform hardware implementation of the circuit and compare with your truth table output.

Data Table:

F (A, B, C, D) = Σ (0, 2, 3, 4, 6, 7, 8, 9, 10, 12, 14, 15)

Truth table-

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Expression for SOP-

F = A'B'C'D' + A'B'CD' + A'B'CD + A'BC'D' + A'BCD' + A'BCD + AB'C'D' + AB'C'D + AB'CD' + ABC'D' + ABCD' + ABCD

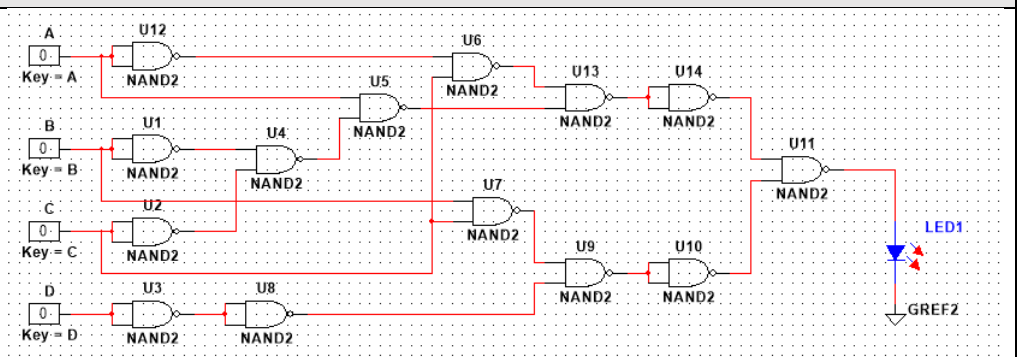
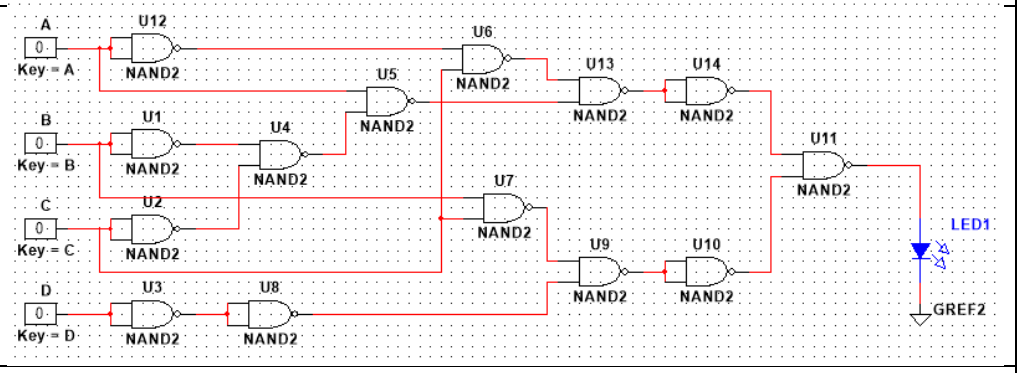
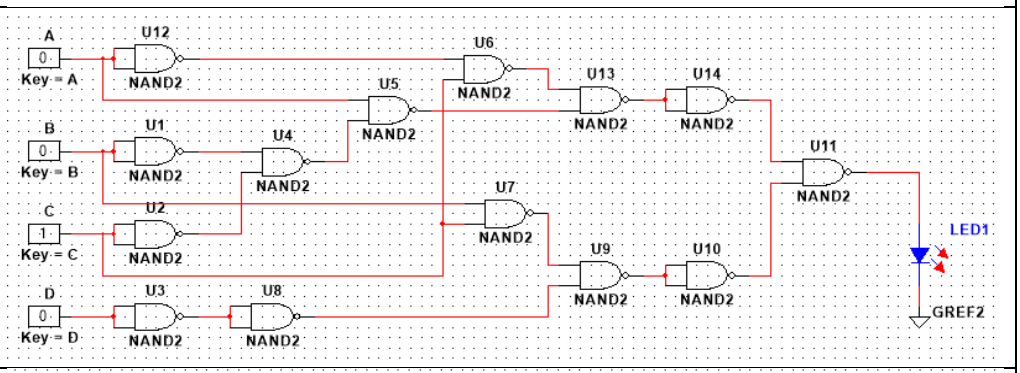
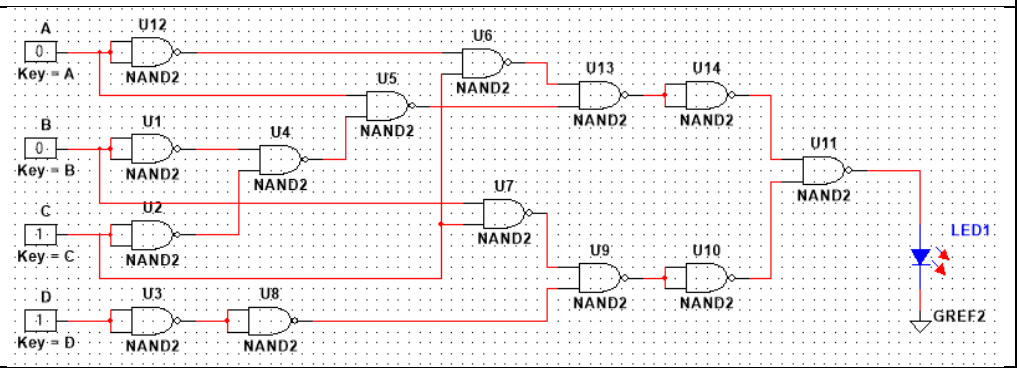
Minimizing the SOP expression using K-Map–

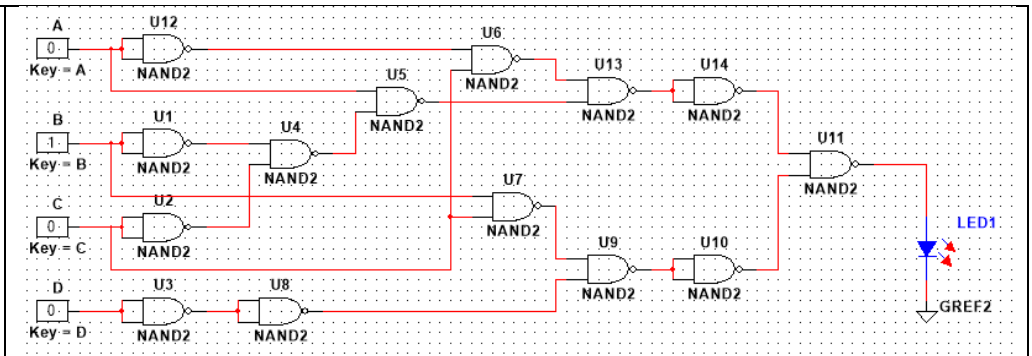
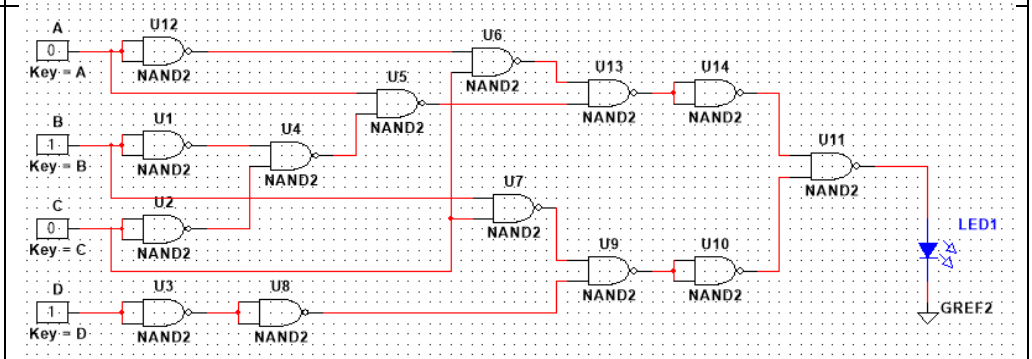
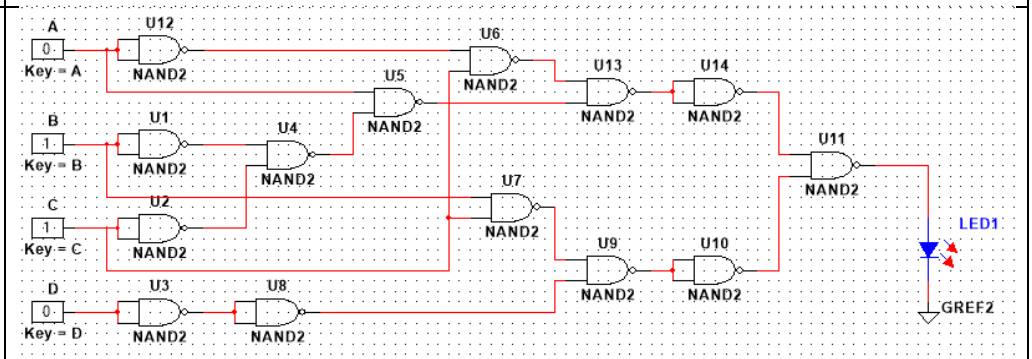
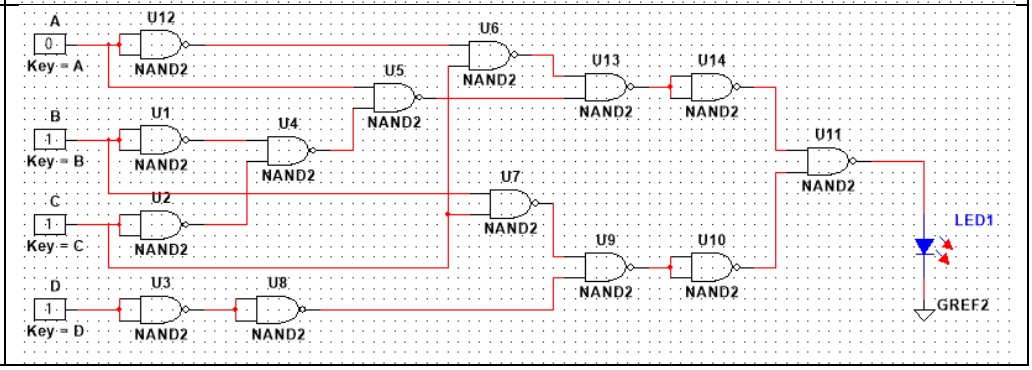
AB \ CD	00	01	11	10
00	1	0	1	1
01	1	0	1	1
11	1	0	1	1
10	1	1	0	1

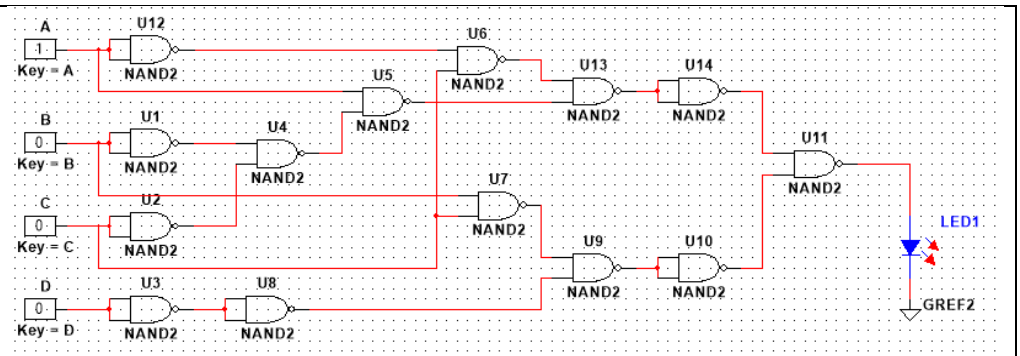
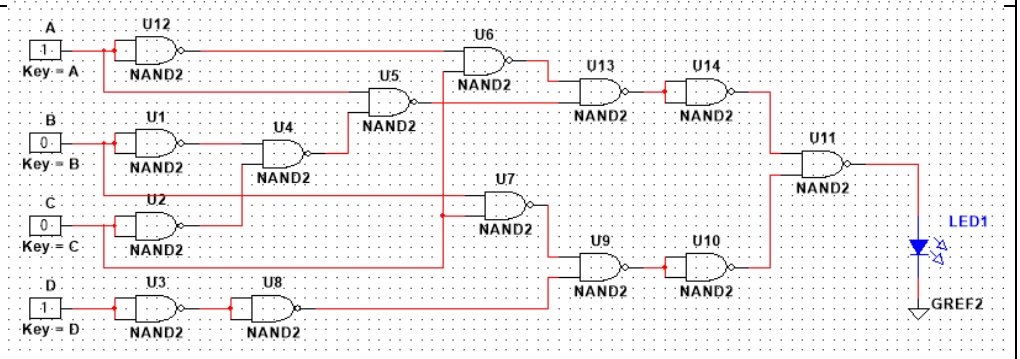
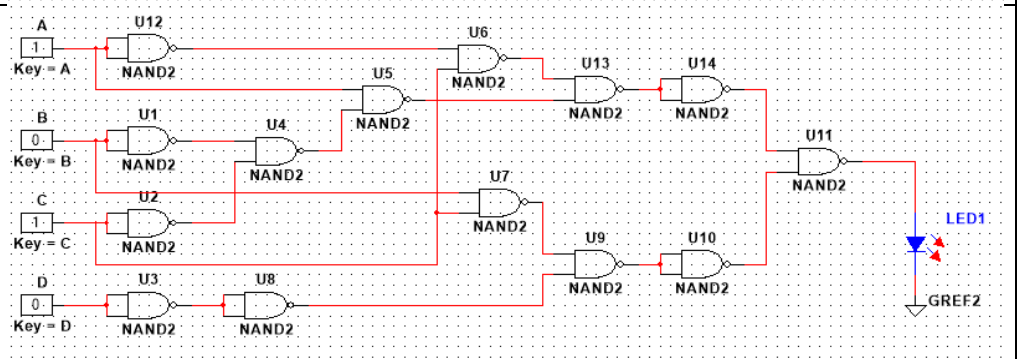
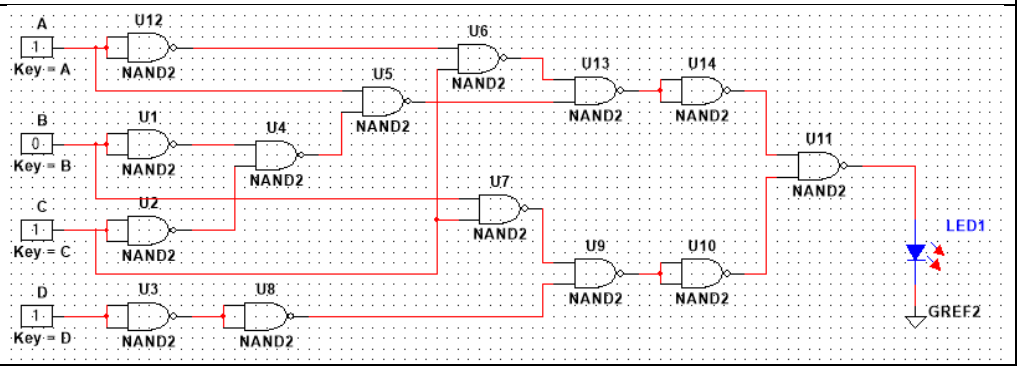
Minimized SOP expression, F = AB'C' + A'C + BC+ D'

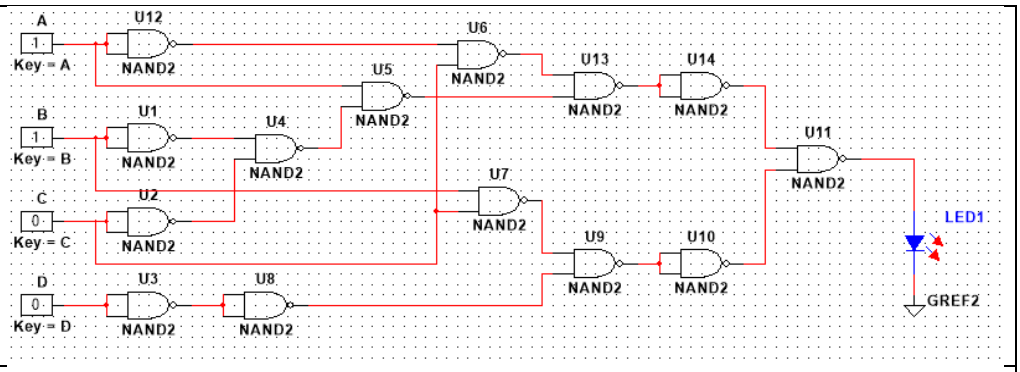
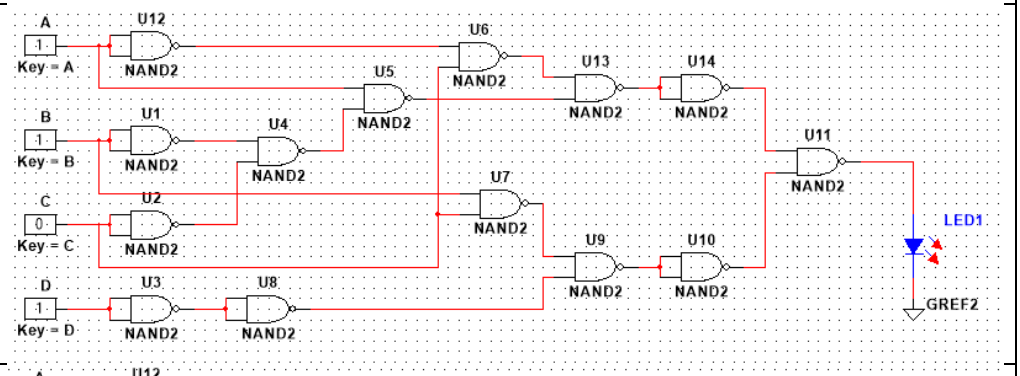
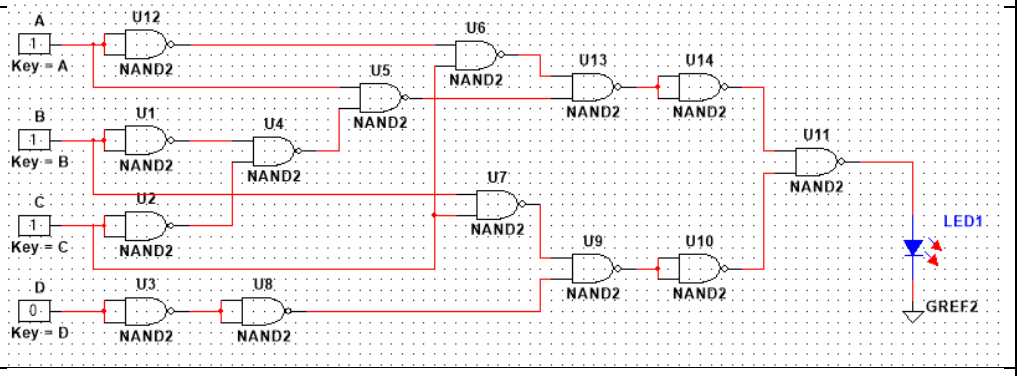
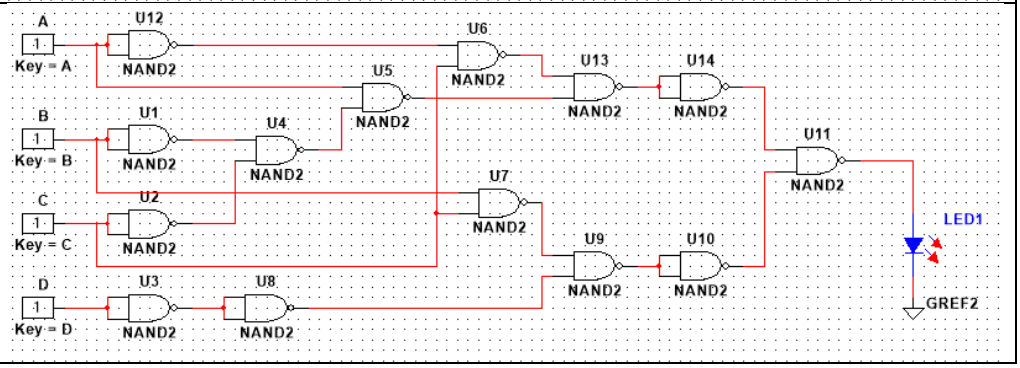
F= AB'C' + C (A' + B) + D'

Simulation:

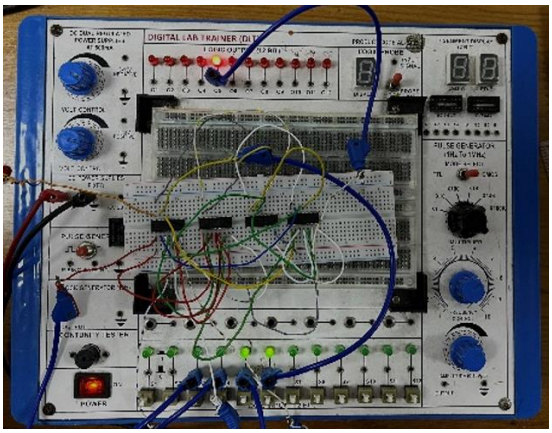
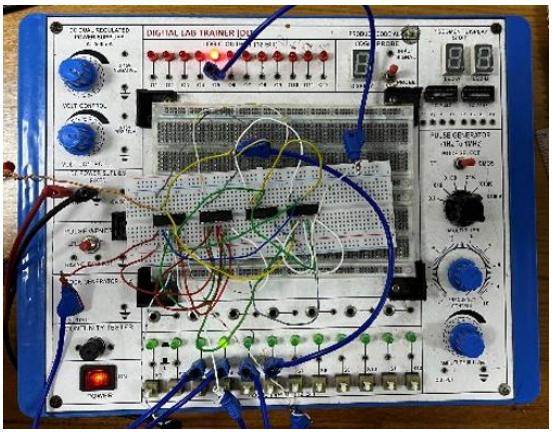
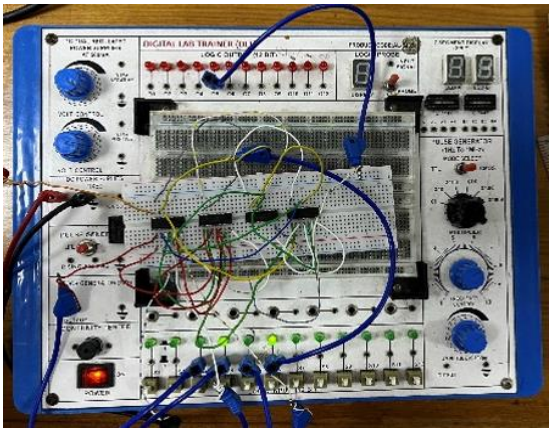
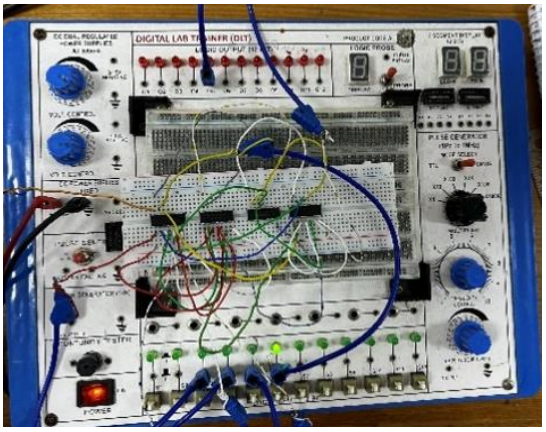
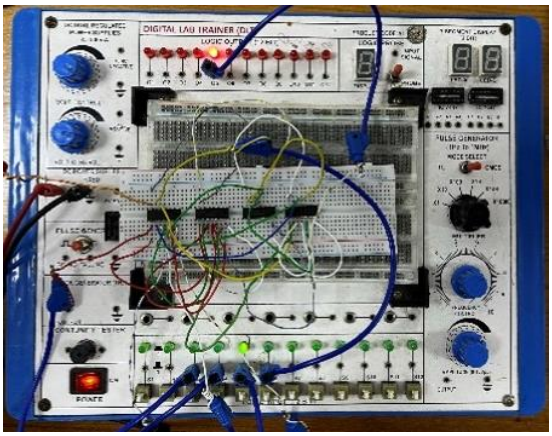
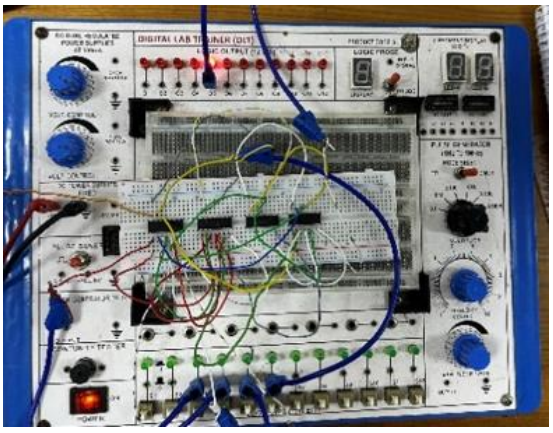
A	B	C	D	F	Simulation
0	0	0	0	1	
0	0	0	1	0	
0	0	1	0	1	
0	0	1	1	1	

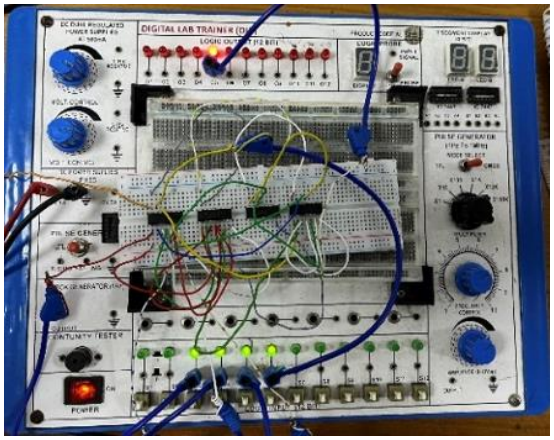
0	1	0	0	1	
0	1	0	1	0	
0	1	1	0	1	
0	1	1	1	1	

1	0	0	0	1	
1	0	0	1	1	
1	0	1	0	1	
1	0	1	1	0	

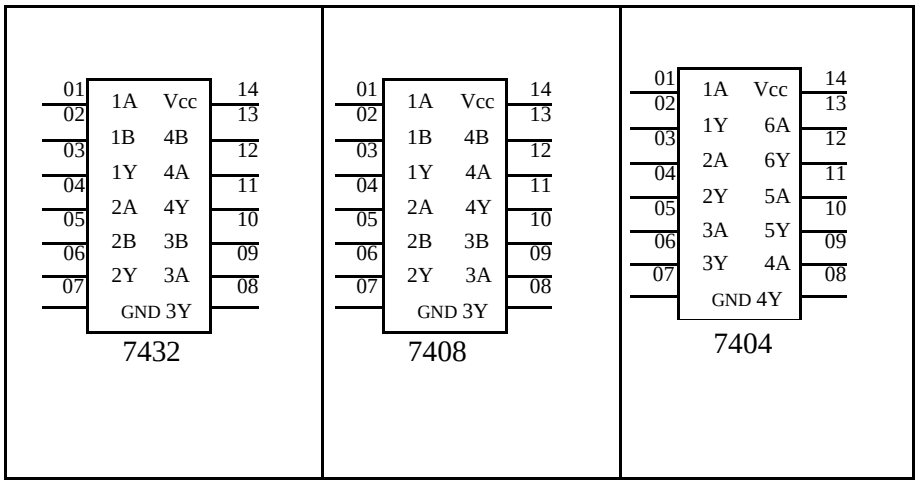
1	1	0	0	1	
1	1	0	1	0	
1	1	1	0	1	
1	1	1	1	1	

Hardware Implementation:



IC Configuration:



Discussion and Result:

The theory and expression part of the excrement were tricky to solve. A little mistake can lead to a big problem. During the experiment we encountered some difficulties such as bread board have some issue all the pin holes weren't working. The pin arrangement of all gates was not the same which also causes some issues but after checking the PIN arrangement Of the ICs twice before assembling the circuit will help to avoid this problem. Some gates also cause some issues, after changing the ICs solves the problem. Incorrect connections can also be very likely to happen as there are lots of connections to make. To solve the problem all the connections should be checked more than once.

Reference:

"Digital Fundamentals" by Thomas L. Floyd

- www.tutorialspoint.com
- www.electronics-tutorials.ws
- www.faculty.kfupm.edu.sa