

American International University – Bangladesh (AIUB)

Faculty of Engineering

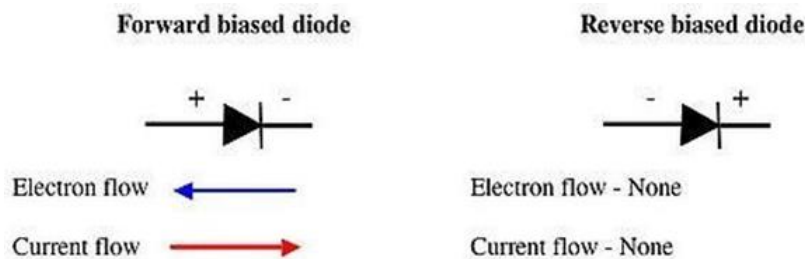
EEE 3102: Digital Logic and Circuits Laboratory

Title: Construction of Diode and Transistor Logic Gates

Part I: Construction of Diode Logic Gates

Introduction:

A diode is a two-terminal electrical device that allows current to flow in one direction but not the other. It is like a pipe with an internal valve that allows water to flow freely in one direction but shuts down if the water tries to flow in another direction. The diode's two terminals are called the anode and cathode. In the diode symbol, the arrow points from the anode (the flat part of the triangle) toward the cathode (the point of the triangle).



The device operates by allowing current to flow from the anode to the cathode, basically in the direction of the triangle. Recall that current is defined to flow from the more positive voltage toward the more negative voltage (electrons flow in the opposite direction). If the diode's anode is at a higher voltage than the cathode, the diode is said to be forward biased, its resistance is very low, and current flows. If the anode is at a lower voltage than the cathode, the diode is reverse-biased, its resistance is very high, and no current flows. The diode is not a perfect conductor, so there is a small voltage drop, approximately 0.7 V, across it.

In this group of experiments, we will implement some logic functions using the DL circuits and discover the potential benefits and problems of using the DL logic.

Theory and Methodology:

Diode Logic OR Gate:

A Diode Logic (DL) OR gate consists of nothing more than diodes (one for each input signal) and a resistor. Here, the 10 k Ω resistor (R) is added to provide a ground reference for the output signal. If there are no input signals connected to the diodes, the output will be ground, or logic 0. Thus, an open input is equivalent to a logic 0 input and will have no effect on the operation of the rest of the circuit. It is possible to add any number of input diodes to this circuit, each with its separate input signal. However, two inputs are quite sufficient to demonstrate the operation of the circuit.

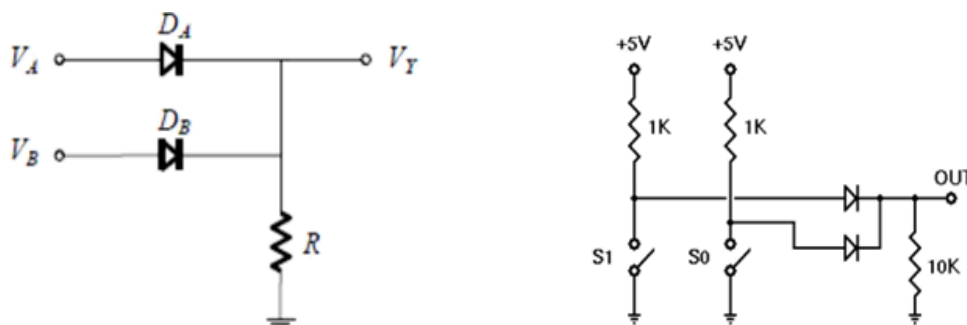


Fig. 1 DL OR Gate

Assuming the diodes are ideal, the voltage-based truth table as given in Table 1 (a) is obtained. The corresponding logic-based or binary truth table is given in Table 1 (b):

Table 1: (a) Voltage-based truth table, (b) Logic-based or binary truth table of DL OR gate

V_A (volt)	V_B (volt)	V_Y (volt)	A	B	Y
0	0	0	0	0	0
0	5	5	0	1	1
5	0	5	1	0	1
5	5	5	1	1	1

Diode Logic AND Gate:

A Diode Logic AND gate consists of diodes (one for each input signal) and a resistor. As with the DL OR gate, the 10K Ω resistor (R) provides a reference connection. Unlike the OR gate, however, this is a reference to +5 volts, rather than to ground. If there are no input signals connected to the diodes, the output will be +5 volts, or logic 1. Thus, an open input will not affect the rest of the circuit, which will continue to operate normally. As with DL-OR gates, it is possible to add any number of input diodes to this circuit, each with its separate input signal. However, two inputs are quite sufficient to demonstrate the operation of the circuit.

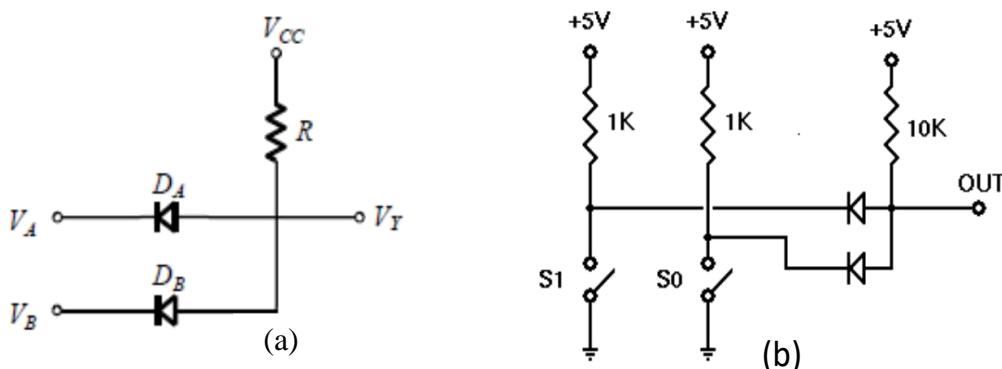


Fig. 2 DL AND Gate

Assuming the diodes are ideal, the voltage truth table of the above AND gate is as given in Table 2 (a). The corresponding logic truth table is in Table 2(b).

Table 2: (a) Voltage-based truth table, (b) Logic-based or binary truth table of DL AND gate

V_A (volt)	V_B (volt)	V_Y (volt)	A	B	Y
0	0	0	0	0	0
0	5	0	0	1	0
5	0	0	1	0	0
5	5	5	1	1	1

Apparatus:

- (1) 10 k Ω ohm resistor (Color band: brown-black-orange).
- (2) 1N914/1N4002 diodes or equivalent.
- (3) Connecting wires.
- (4) Trainer Board

Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply the correct voltage (within V_{CC}) to turn on the diodes/transistors and/or chip, otherwise it may get damaged!

Experimental Procedure:

1. Construct the DL-OR gate on your breadboard as shown in Fig. 1. Then draw a Truth Table similar to the one provided and fill in your experimental results.
2. Construct the DL-AND gate on your breadboard as shown in Fig. 2. Then draw a Truth Table similar to the one provided and fill in your experimental results.

Results and Discussions:

Students will summarize the experiment and discuss it as a whole. Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. Discuss any mistakes you might have made while conducting the investigation and describe ways the study could have been improved.

Report:

1. What is wired logic?
2. Students must install PSpice/LTSpice/ PSIM software and MUST present the simulation results using transistors to the instructor before the start of the experiment.
3. For, each of the above set-ups, describe in words what the data means. Did your results match the expected ideal outputs? If not, explain why?
4. Why are diode logic gates not suitable for cascading operations?

Part 2: Construction of Bipolar Transistor Logic Gate

Introduction:

A bipolar transistor is a three-terminal semiconductor device. Under the control of one of the terminals, called the base, current can flow selectively from the collector terminal to the emitter terminal.



Fig. 3: Bipolar Junction Transistor (BJT) circuit symbols

In this experiment, we examine how to build logic gates from Bipolar Junction Transistors (BJT) using the RTL, DTL, and TTL design.

Theory and Methodology:

Resistor-Transistor Logic (RTL):

Resistor-Transistor Logic (RTL) is a large step beyond Diode Logic (DL). Basically, RTL replaces the diode switch with a transistor switch. If a +5 V signal (logic 1) is applied to the base of the transistor (through an appropriate resistor to limit base-emitter forward voltage and current), the transistor turns fully on and grounds the output signal. If the input is grounded (logic 0), the transistor is off and the output signal is allowed to rise to + 5 V. In this way, the transistor not only inverts the logical sense of the signal but also ensures that the output voltage will always be a valid logic level under all circumstances. Because of this, RTL circuits can be cascaded indefinitely, whereas DL circuits cannot be cascaded reliably at all.

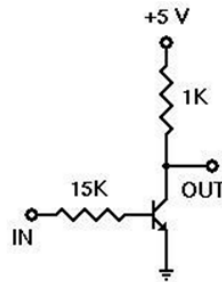


Fig. 4: RTL Inverter

Diode-Transistor Logic (DTL):

Diode-Transistor Logic (DTL) is a class of digital circuits built from Bipolar Junction Transistors (BJT), diodes, and resistors; it is the direct ancestor of Transistor-Transistor Logic (TTL). DTL offers better noise margins and greater fan-outs than RTL but suffers from low speed (especially in comparison to TTL). RTL allows the construction of NOR gates easily, but NAND gates are relatively more difficult to get from RTL. DTL, however, allows the construction of simple NAND gates from a single transistor, with the help of several diodes and resistors.

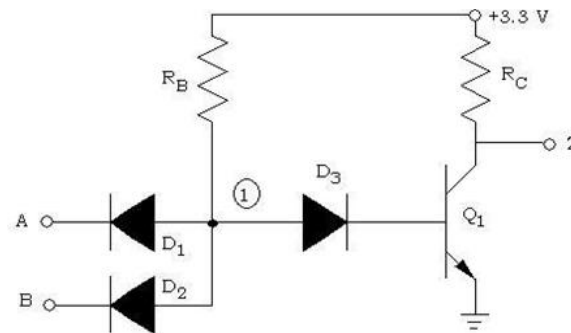


Fig. 5: 2-input DTL NAND Gate

Transistor-Transistor Logic:

We can think of a bipolar transistor as two diodes placed very close together, with the point between the diodes being the transistor base. Thus, we can use transistors in place of diodes to obtain logic gates that can be implemented with transistors and resistors only; this is called Transistor-Transistor Logic (TTL).

One problem that DTL doesn't solve is its low speed, especially when the transistor is being turned off. Turning off a saturated transistor in a DTL gate requires it to first pass through the active region before going into cut-off. Cut-off, however, will not be reached until the stored charge in its base has been removed. The dissipation of the base charge takes time if there is no available path from the base to the ground. This is why some DTL circuits have a base resistor that's tied to the ground, but even this requires some trade-offs. Another problem with turning off the DTL output transistor is the fact that the effective capacitance of the output needs to charge up through R_C before the output voltage rises to the final logic '1' level, which also consumes a relatively large amount of time. TTL, however, solves the speed problem of DTL elegantly.

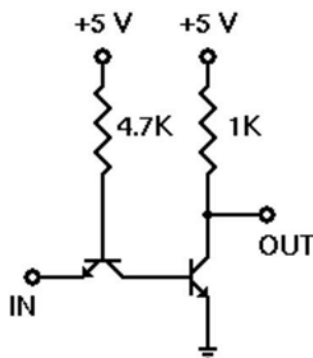


Fig. 6: TTL Inverter

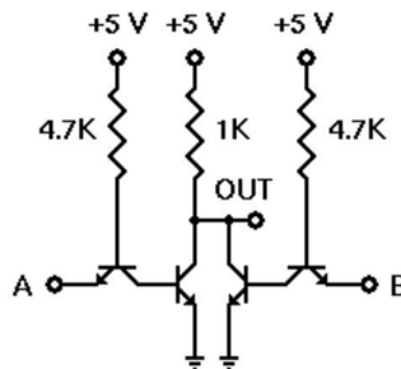


Fig. 7: 2-input TTL NOR gate

Emitter-Coupled Logic (ECL):

The operation of Emitter-Coupled Logic (ECL) is that whenever the HIGH input is given to any one of the ECL circuits, it will make the transistors ON. So, this will pull the output, V_o , down to LOW.

Similarly, when the LOW input value is given to all the transistors' input then it will make all the transistors OFF. So, it will make the output, V_o be pulled up to the HIGH value because of the drop within $640\ \Omega$ resistance.

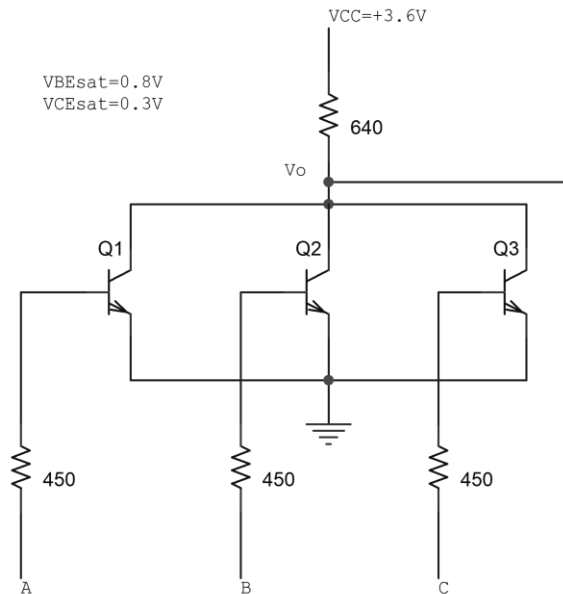
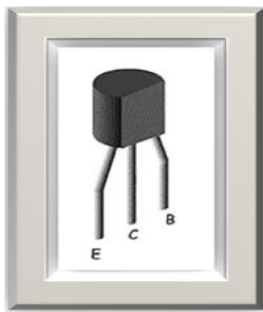


Fig. 8 A 3-input ECL NOR gate

BJT Pin Configuration:



Pre-Lab Homework:

Explain how n-p-n BJT transistors work.

Students must install PSpice/LTSpice/PSIM software and must present the simulation results using transistors to the instructor before the start of the experiment.

Apparatus:

1. 2N4124 NPN silicon transistor (or equivalent).
2. Resistors ($15\ \text{k}\Omega$, $1\ \text{k}\Omega$, $4.7\ \text{k}\Omega$)
3. Connecting wires.
4. Trainer Board

Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply the appropriate voltage (within V_{CC}) to turn on the transistors and/or chip, otherwise it may get damaged.

Experimental Procedures:

- (1) Set up the circuit for the RTL inverter as shown in Fig. 6.
- (2) For each input combination, find the output and place them in a Truth Table. The Truth Table should have two sets of outputs- one ideal and one experimental.
- (3) Repeat steps 1 and 2 for the circuit set-up of Figs. 7 and 8.

Results and Discussions:

Students will summarize the experiment and discuss it as a whole. Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. Discuss any mistake you might have made while conducting the investigation and describe ways the study could have been improved.

Report:

1. For each of the above set-ups, describe in words what the data means. Did your results match the expected ideal outputs? If not, explain why?
2. Design a 4-input RTL OR gate and explain its operation.
3. Design a 3-input TTL NAND and NOR gates and explain their operation.
4. Design a 3-input DTL NAND gate and explain its operation.
5. Design a 3-input ECL OR gate and explain its operation.
6. For all these circuits show their PSPICE/LTSPICE/PSIM Simulations.

Reference(s):

1. Thomas L. Floyd, *Digital Fundamentals*, 9th Edition, 2006, Prentice Hall, India.
2. Boylestad, Robert L. *Electronic Devices and Circuit Theory*. Pearson Education, India, 2009.