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FACULTY OF SCIENCE & TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
DIGITAL LOGIC AND CIRCUITS LABORATORY

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Section: Q Group:2 Exp. No. :03

LAB REPORT ON

Design of adder, subtractor and comparator circuits.

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ABSTRACT:

The purpose of this experiment is to learn the design and behavior of adder, subtractor and comparator logic circuits. Adders and subtractors are the most basic and most important part of digital electronics.

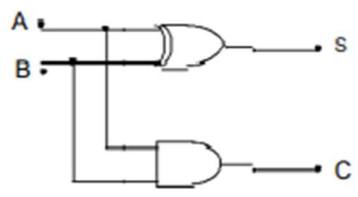
THEORY:

Part I (Adder and Subtractor):

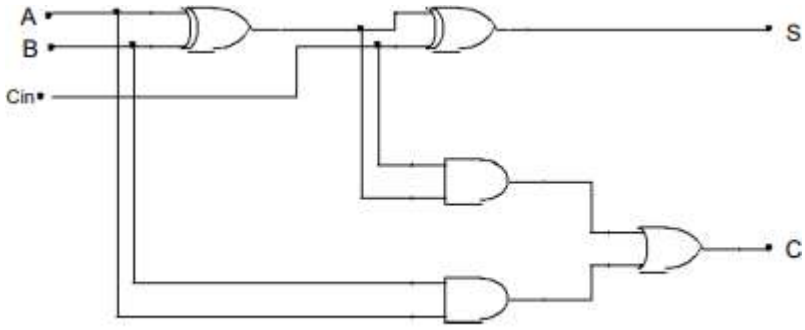
Adders and subtractors are digital circuits which can add and subtract binary digits. They are the most important part in the design of Arithmetic Logic Unit (ALU). In this experiment different types of adders and subtractors will be designed and their behavior will be observed.

Methodology:

An adder or summer is a combinational circuit that adds binary numbers. There are mainly two kinds of adders, half adder and full adder. The half adder can add only two single bits of binary digit and outputs the sum of the bits and a carry which is the overflow of the sum. A full adder can add two single bit digits and one carry bit which is the overflow of the sum of the previous stage of addition and outputs the sum and the carry.



Half Adder



Full Adder

Truth table for half adder:

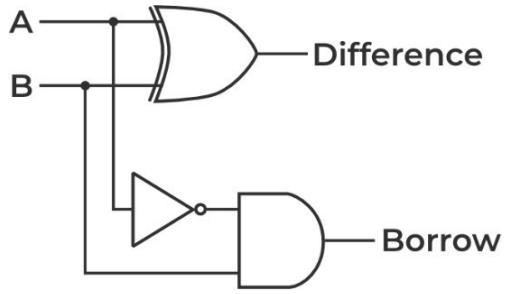
INPUT		OUTPUT	
A	**B**	**S**	**C**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth table for full adder:

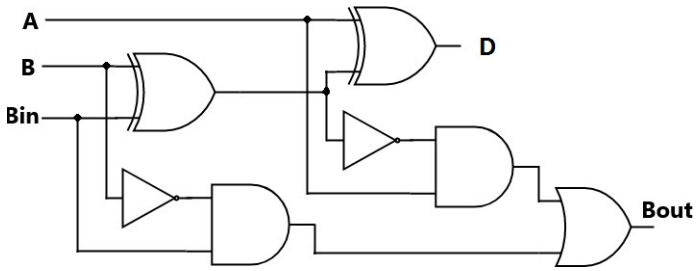
INPUT			OUTPUT	
A	**B**	**C_{in}**	**S**	**C**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A subtractor is also a combinational circuit that calculates the difference of two binary digits. This is done by taking the two's complement of the subtrahend and then adding it with the minuend. So, the subtractor circuit can be designed with the help of adder circuits. Like adders, there are two types of subtractor circuits, half subtractor and full subtractor.

A half subtractor performs a subtraction between two single bits and produces their difference and another output called borrow. A full subtractor performs a subtraction of two single bits, considering a borrow bit. It outputs the difference of the subtraction and a borrow bit.



Half Subtractor



Full Subtractor

Truth table for half Subtractor:

INPUT		OUTPUT	
A	**B**	**D**	**B**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth table for full Subtractor:

INPUT			OUTPUT	
A	**B**	B_{in}	**D**	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Using Full Adder blocks for addition of n- bit systems:

Full adder blocks can be connected or summation of n-bit systems. To design a 2-bit full adder, two I bit full adders are connected in parallel connection as shown in the figure below. The same process Can used for designing n-bit Full Adder for addition of words having a length of n-bits.

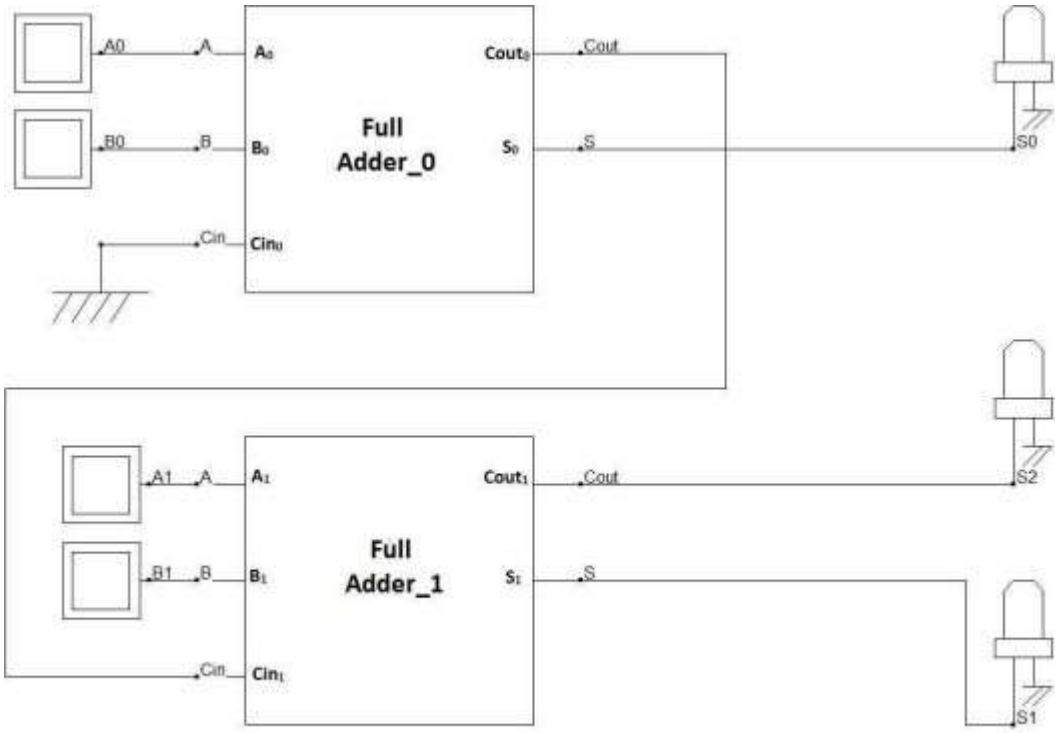


Fig. 1.3: 2-bit Full adder design using 1 bit full adder blocks

Here, the LSB of both word A and B (AO and BO) are connected in the first stage full adder block and Cin of this block (CinO) is connected to ground (as there is no carry in available at the initial stage). The MSB of both word A and B (A1 and B 1) are connected in the first stage full adder block and Cin Of this block (Cin) is connected to the previous Stage Cout (Cout). Summation output for the ISB is available

from the first Stage Sum (SO). The next Stage block outputs Sum (Sl) and carry out (Cout) provide the MSBs for the next Stage output (Sl and S2).

Part II (Comparator):

A magnitude comparator is a device that takes in two sets of inputs in its input and compares them to provide an output, if they are equal, greater than or less than the other. In this experiment I-bit comparator will be designed at first and using the I-bit comparator block, 2-bit comparator will be designed.

Methodology:

Magnitude Comparators are combinational logic circuits that take 2 sets of data as its inputs and test whether the value represented by one binary word is greater than, less than, or equal to the value represented by another binary word.

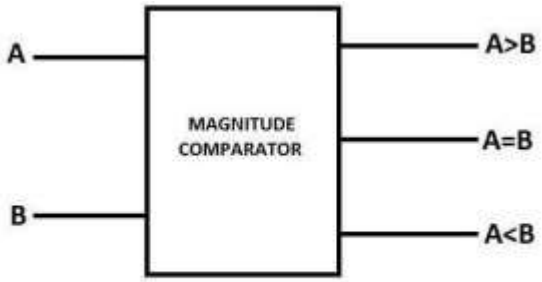


Fig.2.1: Block Diagram of 1 Bit Magnitude Comparator

Depending on the input combination for a 1-bit magnitude comparator, following behavior table can be developed using the logic expressions.

A=B if, A=B=0 or A=B=1;
A>B if A=1 and B=0;
A<B if A=0 and B=1;

		A=B	A>B	A<B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

The SOP expressions for the output lines can be written as

(A=B)= A'B'+AB;
(A<B)=A'B;
(A>B)=A'B;

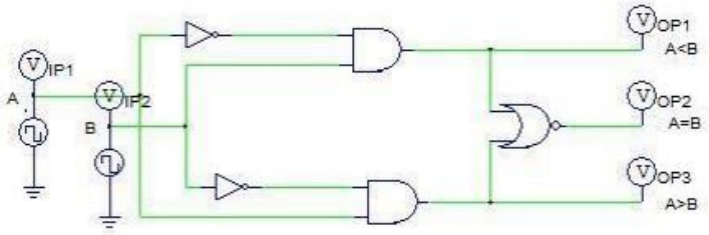


Fig.2.2: 1-Bit Comparator

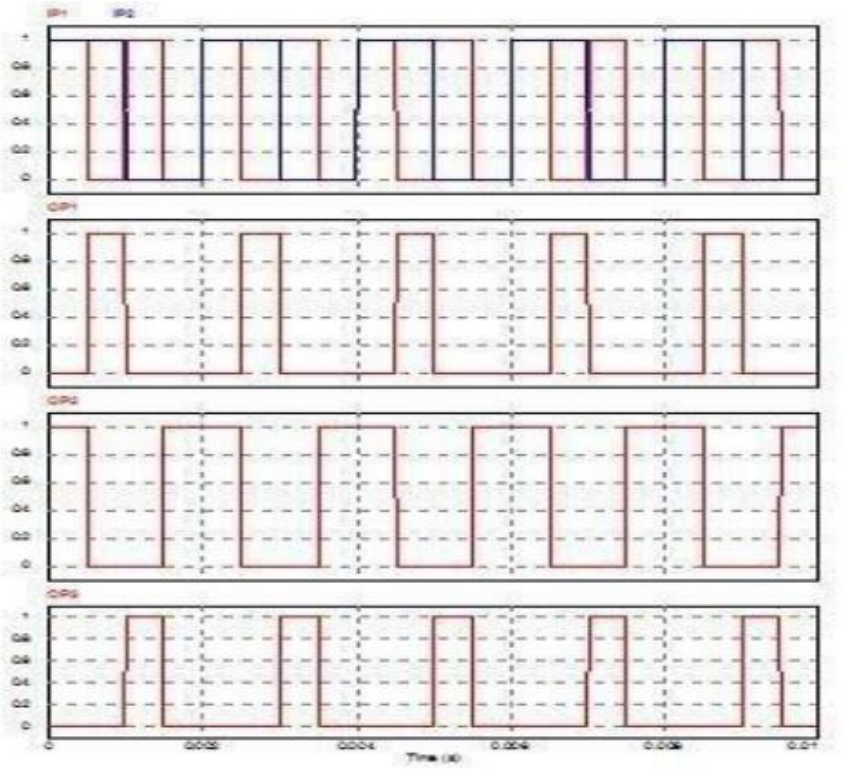


Fig.2.3: Timing Diagram for 1-Bit

Comparator 2 Bit Comparator design using 1 bit block: Using 1-bit blocks, n-bit Magnitude comparator can be designed.

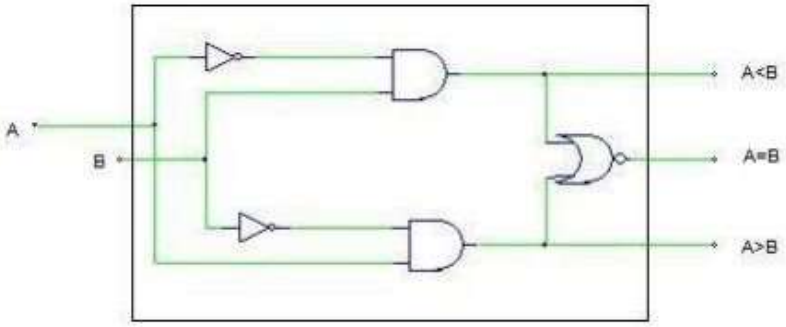


Fig.2.4: 1-Bit Comparator Block

Designing a 2-bit comparator using 1-bit blocks:

Let us consider 2 words,

Word A -> A1A0

Word B-> B1B0

For comparing, the following process is used as writing the logic equations.

For A=B,

If (A1=B1) & (A0=B0), then (A=B);

For A>B,

If (A1>B1) then (A>B) or

If (A1=B1) & (A0>B0),

then (A>B);

For A<B,

If(A1<B1) then (A<B) or

If(A1=B1) & (A0<B0), then (A<B)

A	B	A=B	A>B	A<B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

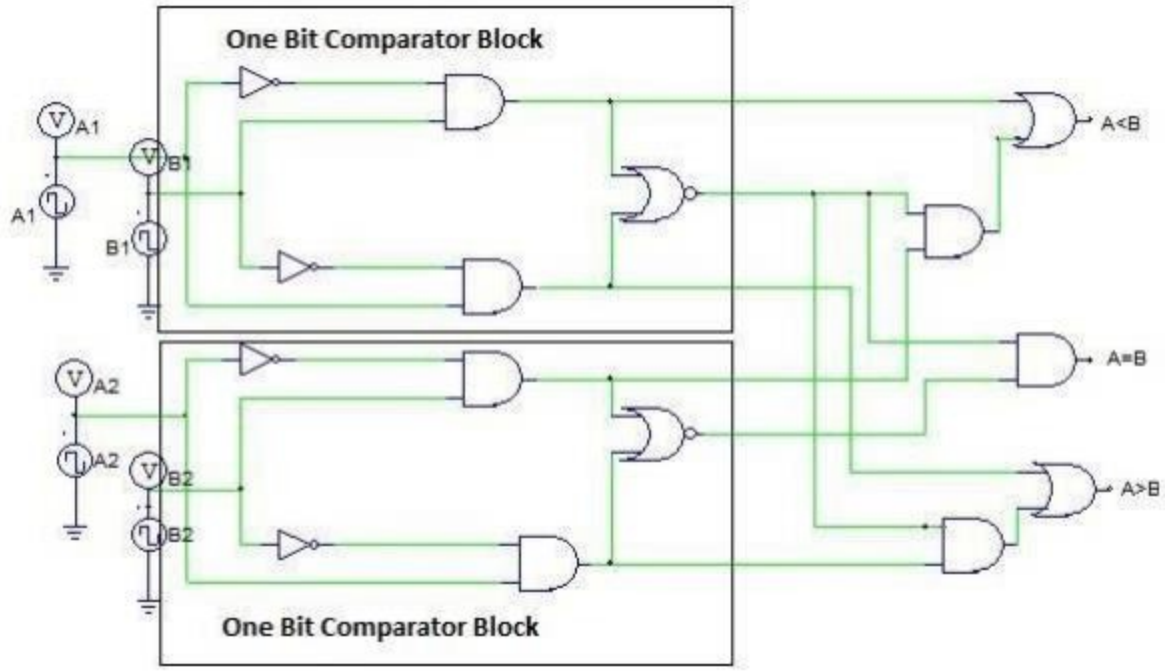


Fig.2.5: 2-Bit Comparator using 1_bit Comparator Block

Apparatus:

- Digital trainer board.
- IC or Integrated Circuits:
    1. 7486(2pcs)
    2. 7408 (2pcs)
    3. 7404 (2pcs)
    4. 7431(2 pcs)
    5. 7483(1 pcs)
- Connecting wires.
- LEDs
- Switches

Precautions:

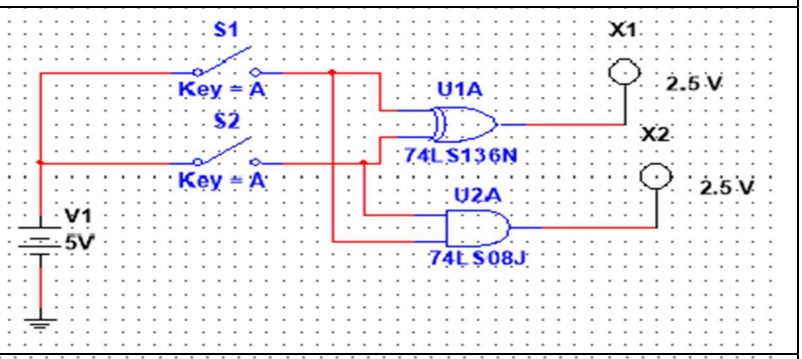
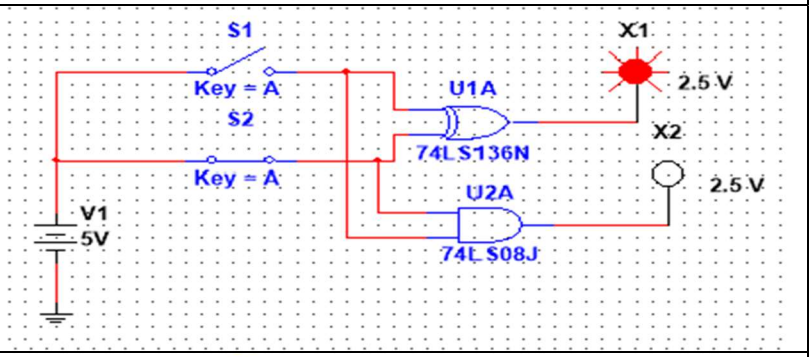
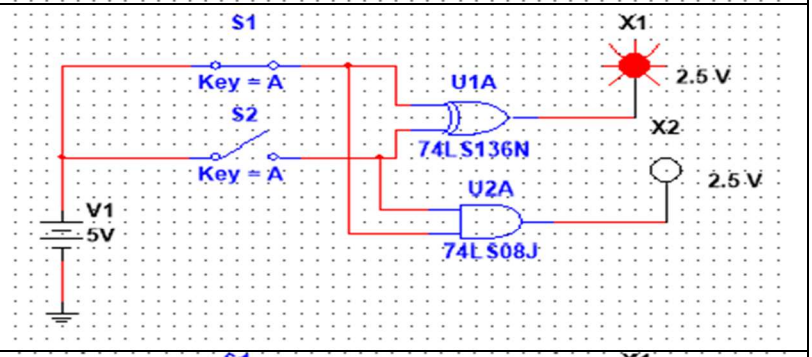
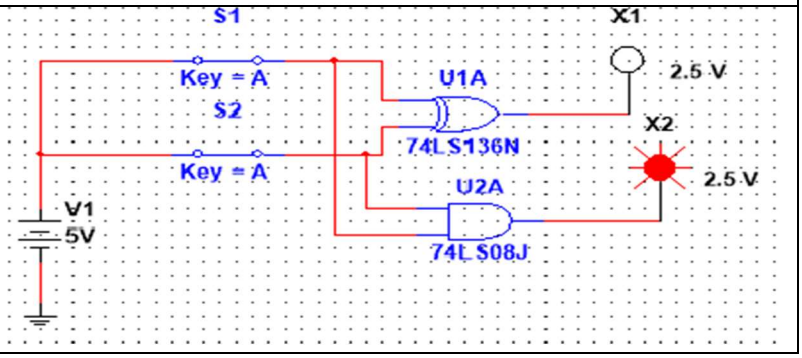
1.Make sure that all the LEDs and the toggle switches of the trainer board are working properly.
2.Do not short any connections. Short connection can produce heat (due to high current flow) which is harmful for the components.

Experimental Procedure:

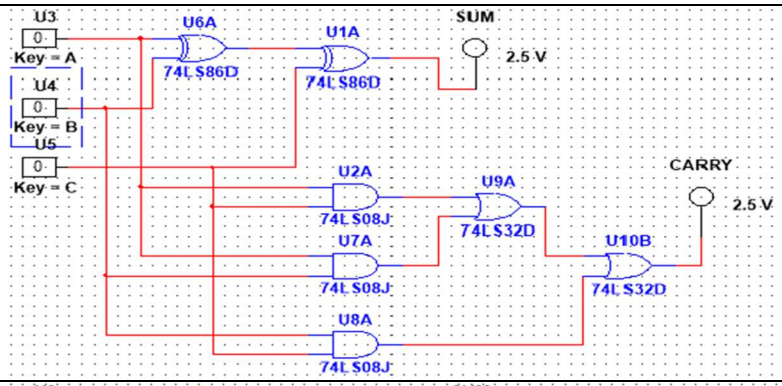
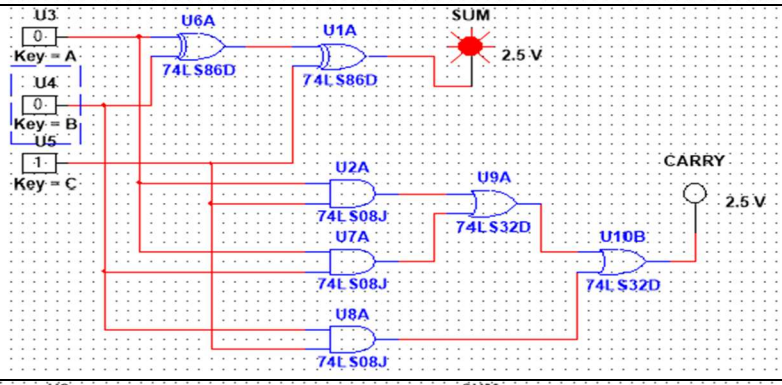
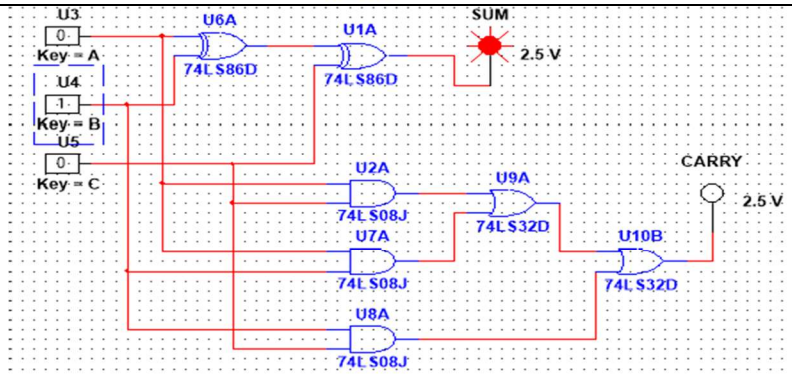
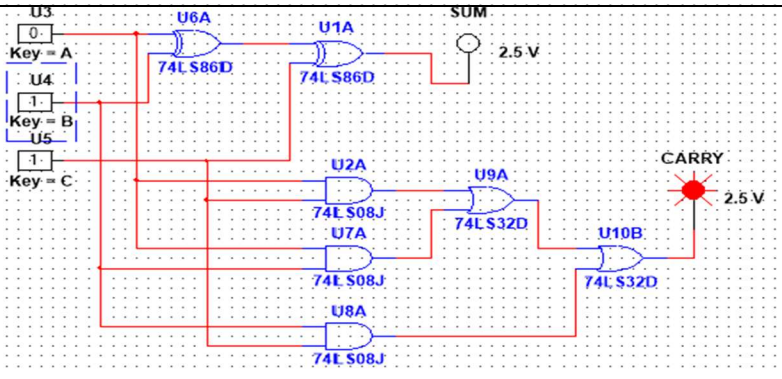
1. we have, Determined the output and the truth tables of the logic circuits for full adder and half subtractor given in the theory and methodology part.
2. We have determined which gates and how many of them are required, check, and detect all the IC
numbers.
3.Careful1y placed the ICs on the Trainer Board and bias them by connecting them to the +5 volt
DC supply and ground.
4.Connected those using wires according to the logic diagram; connected the outputs to the
and we have noted down the outputs by giving different inputs according to the
derived truth table.

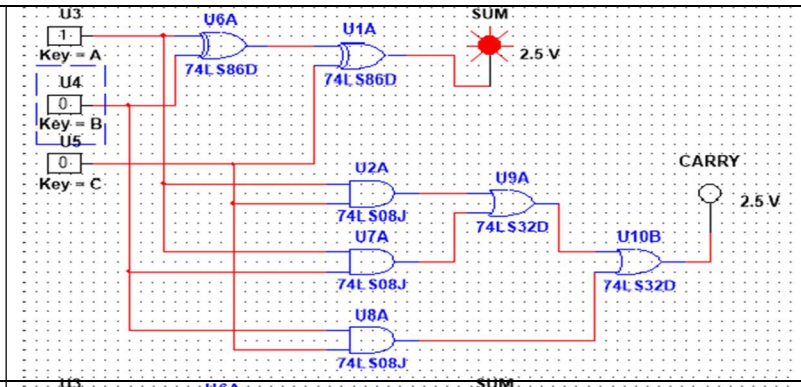
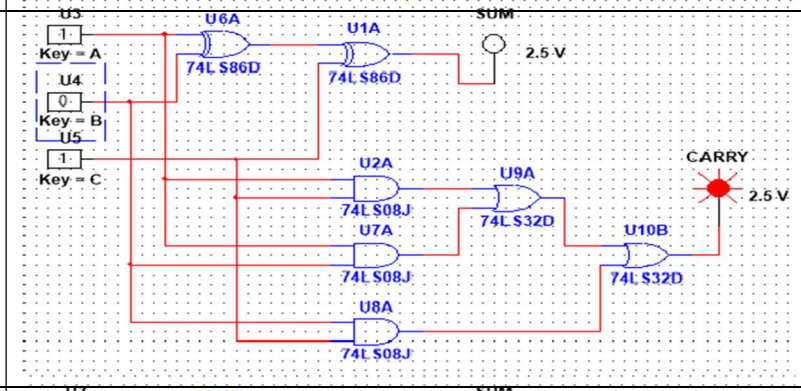
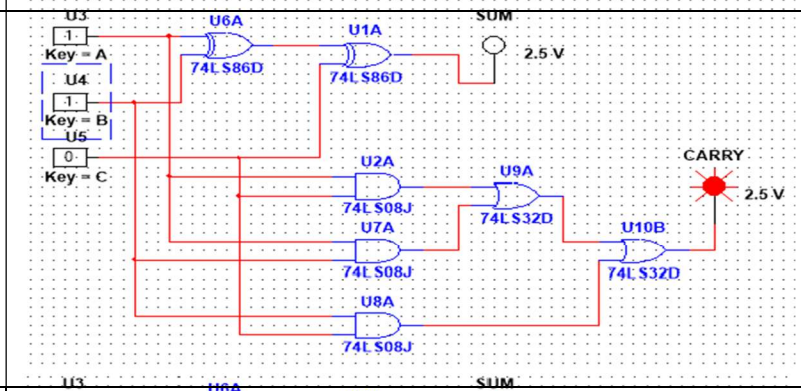
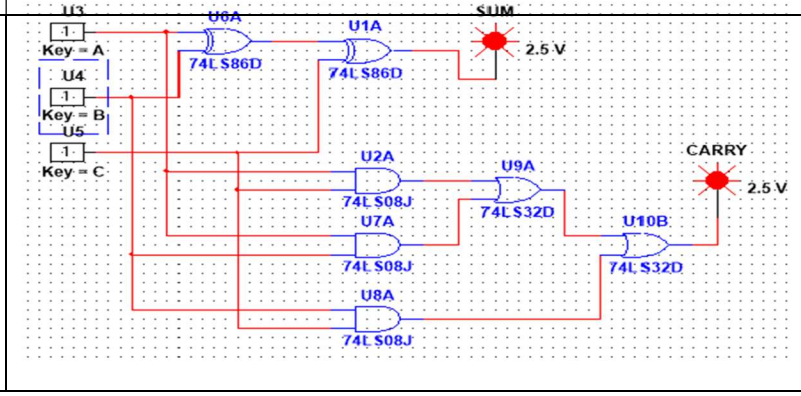
Simulation & Measurement:

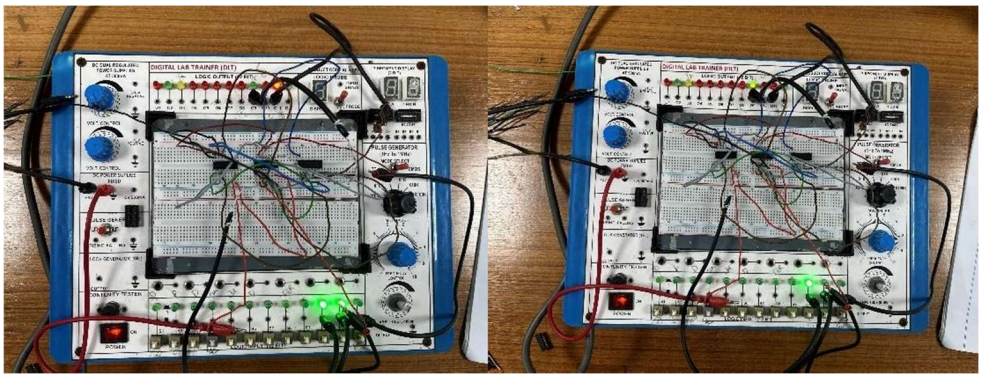
Half -Adder:

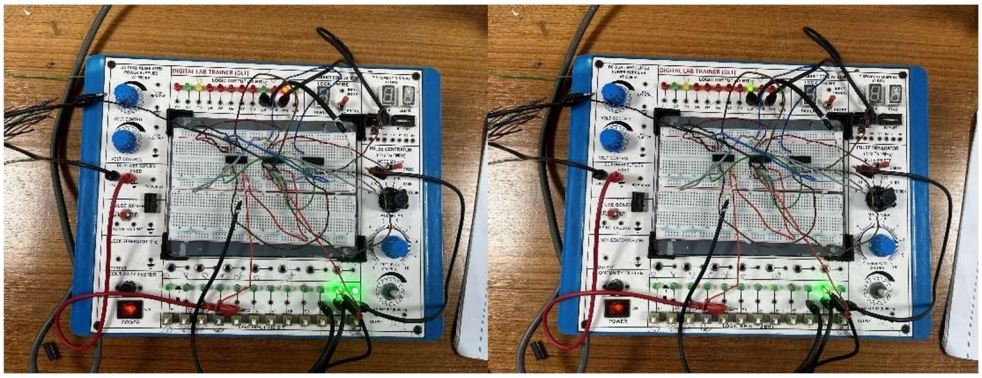
A	B	S	C	Simulation
0	0	0	0	
0	1	1	0	
1	0	1	0	
1	1	0	1	

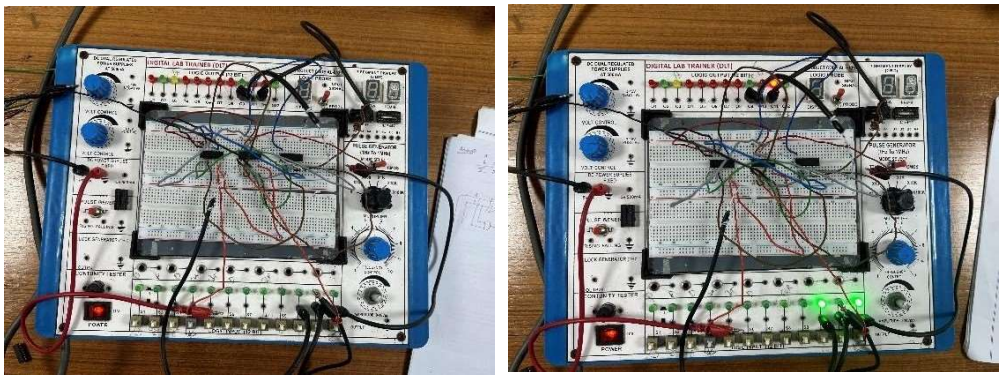
Full-Adder:

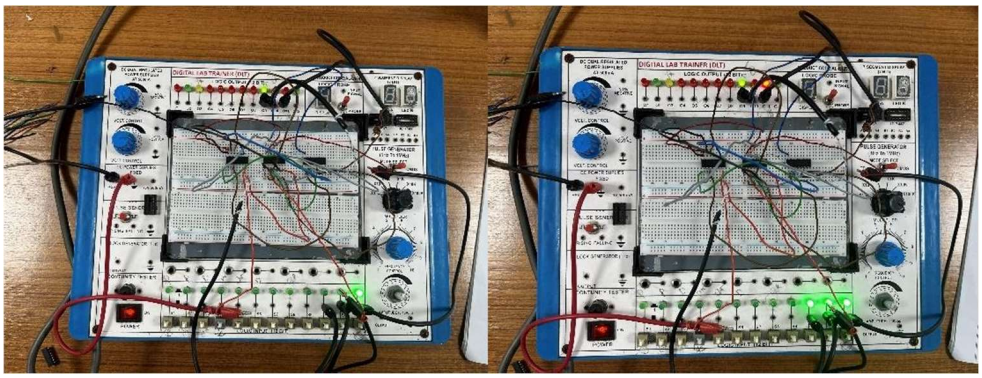
A	B	C_{in}	S	C	Simulation
0	0	0	0	0	
0	0	1	1	0	
0	1	0	1	0	
0	1	1	0	1	

1	0	0	1	0	
1	0	1	0	1	
1	1	0	0	1	
1	1	1	1	1	

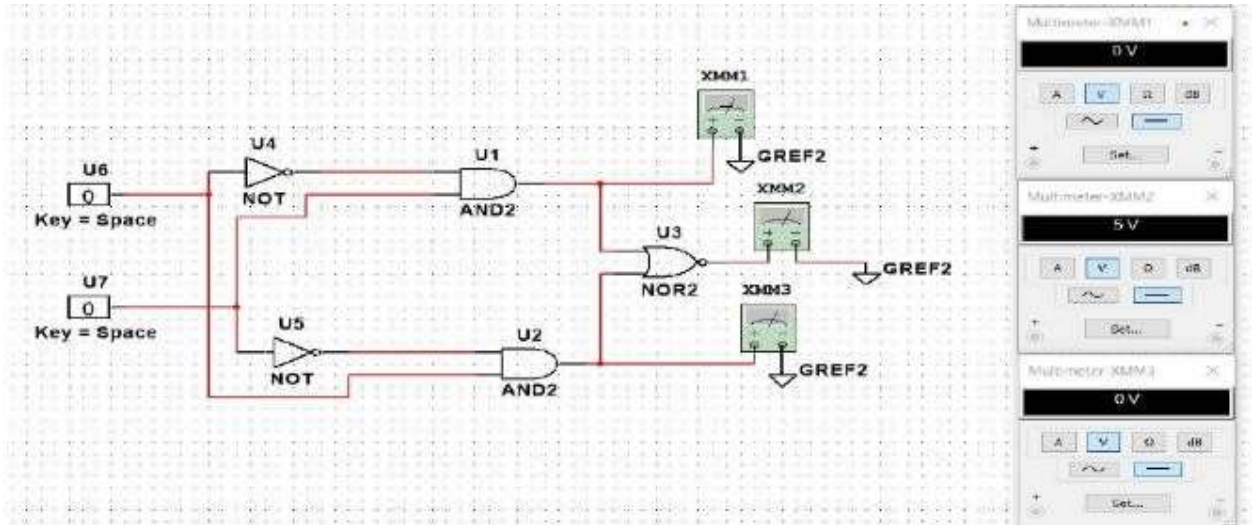


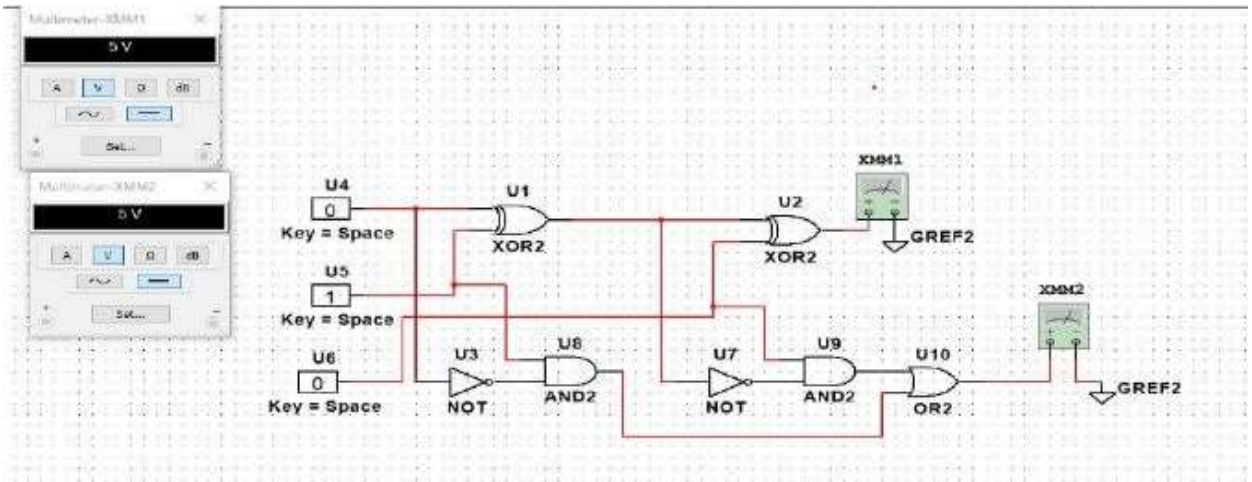


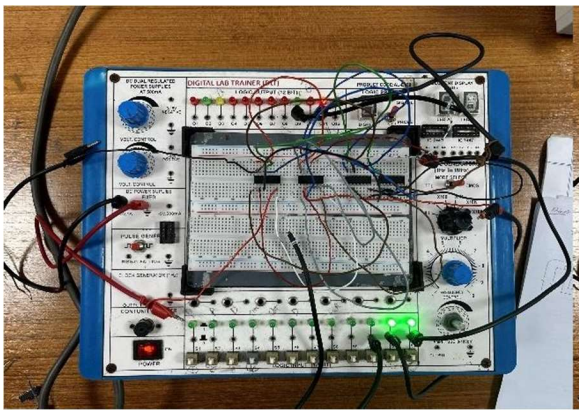
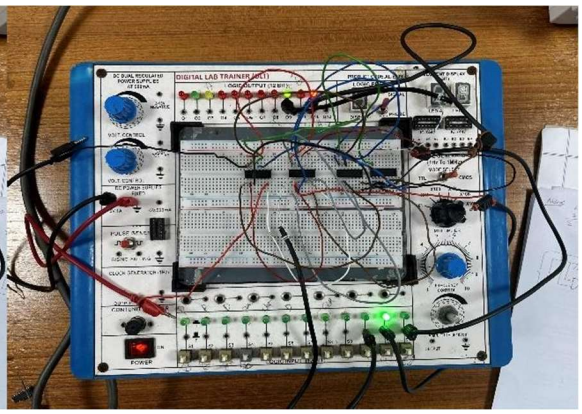
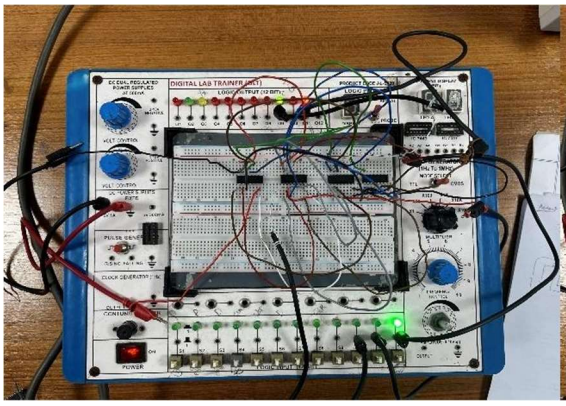
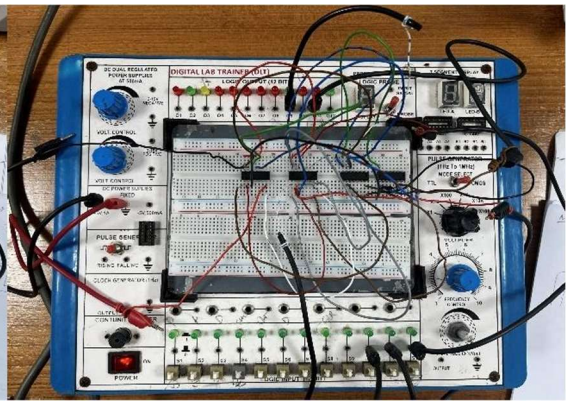


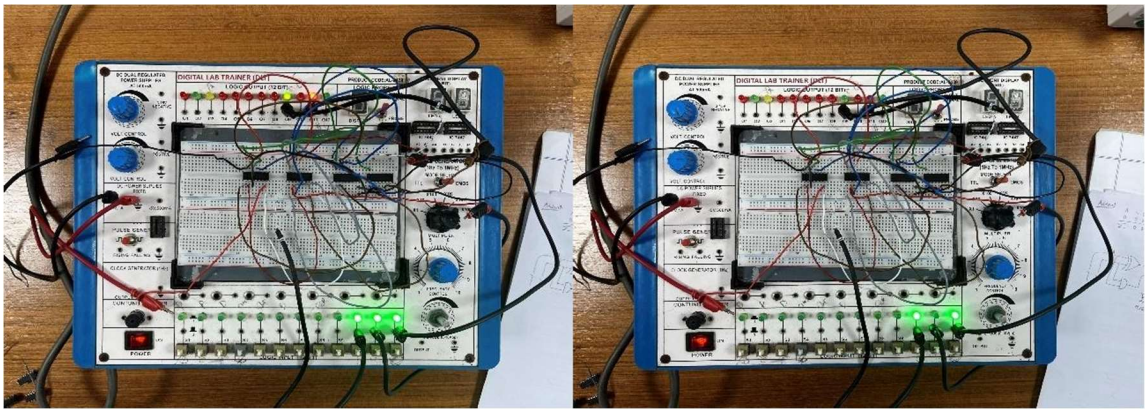


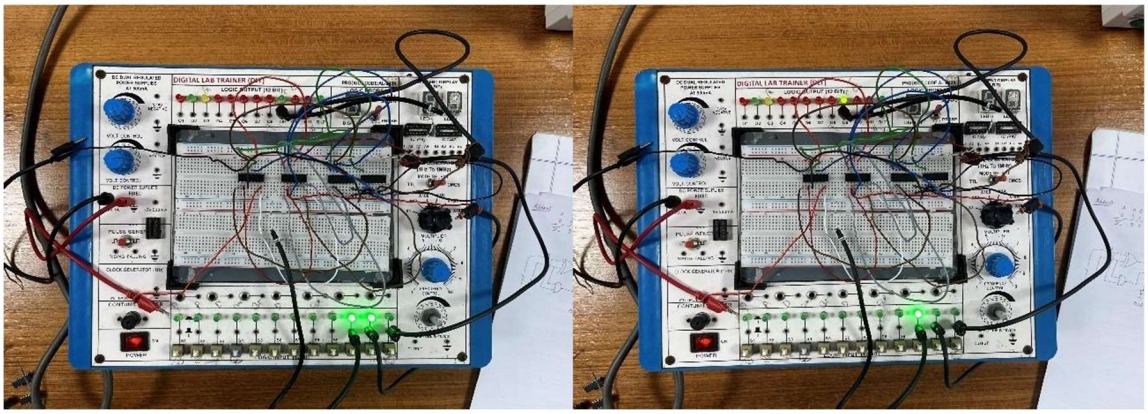
Full Subtractor:



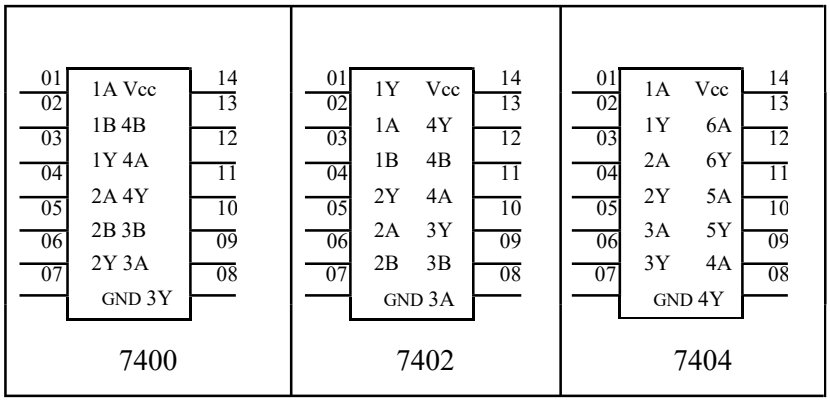


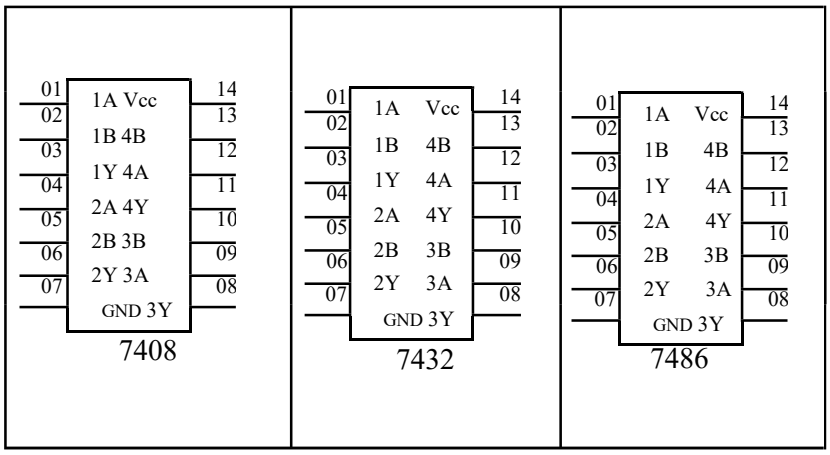







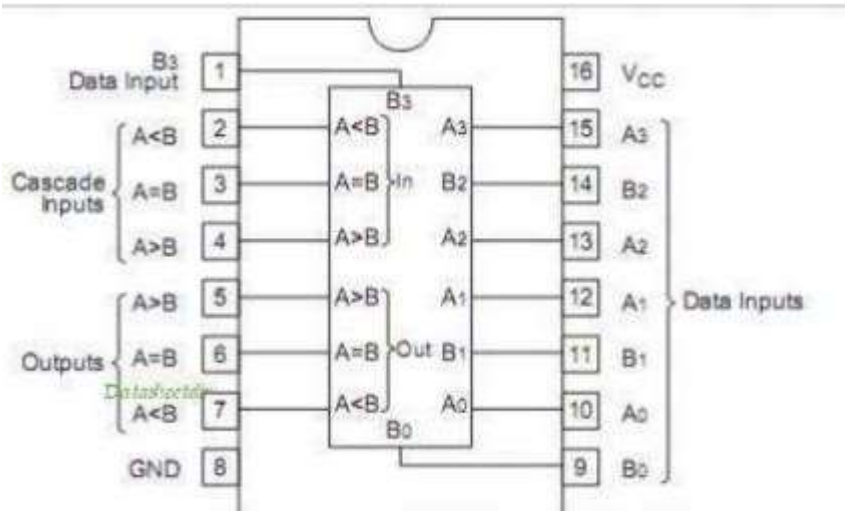


IC PIN Configuration:





IC PIN CONFIGURATION FOR 74LS85:



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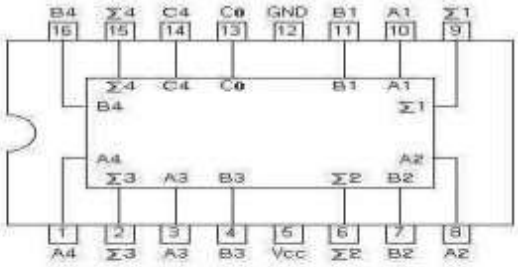

Fig. : 4-bit Full Adder IC pin configuration

Discussion:

Half and full adders and subtractors and I -bit Magnitude Comparators are the combinational circuit. Adders are used not only within the arithmetic logic but also in other parts of the processor. A subtractor are often designed using an equivalent approach as that of an adder Magnitude Comparators are used in central processing units (CPUs) and microcontrollers (MCUs)- We will implement the circuit within the trainer board and match the theoretically obtained truth table by matching outputs for individual input configuration- Design of a half, full adder and subtractor and I-bit Magnitude Comparators circuits are the important topic for digital logic design. During this experiment, we implemented the half and full adder and subtractors and 1 bit Magnitude Comparators circuits using NI Multisim software.

Reference:

"Digital Fundamentals" by Thomas L. Floyd

- www.tutorialspoint.com
- www.electronics-tutorials.ws
- www.faculty.kfupm.edu.sa