AMERICAN INTERNATIONAL UNIVERSITY–BANGLADESH (AIUB)

FACULTY OF SCIENCE & TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

DIGITAL LOGIC AND CIRCUITS LABORATORY

FALL 2023-2024

Section: Q Group: 2

LAB REPORT ON

Studying different digital logic gates and designing basic logic gates using universal gates.

Supervised By

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Submitted By:

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S.M. MUJAHID SOUROV	22-49679-3	Experimental Data, Analysis, Result
MD. ATIK ISHRAK SUJON	22-46684-1	Procedure, Multisim, MS Word
TRIDIB SARKAR	22-46444-1	Discussion writing & Reference collecting

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ABSTRACT:

In this experiment, we gained knowledge about the characteristics of various logic gates and developed familiarity with digital trainer boards and digital integrated circuits (ICs). We successfully created different gates using universal gates and comprehended logical expressions and the application of universal gates in integrated circuits.

THEORY:

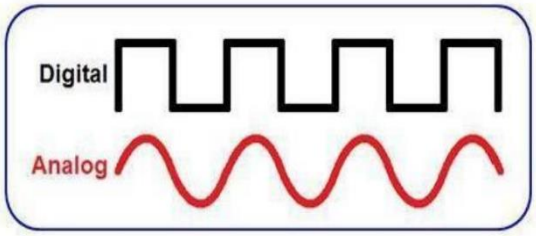
Part I

Basic Logic IC's:

An integrated circuit, also known as an IC, chip, or microchip, consists of electronic circuits condensed onto a small semiconductor plate called a "chip," typically made of silicon. This allows for a significantly smaller size compared to discrete circuits composed of separate components. The trainer board used in this experiment utilizes various integrated circuits to execute distinct logical operations.

Methodology:

In this experiment, we compared Digital signals and analog signals in that they were encoded in binary (0 and 1) format, meaning each bit was represented by two distinct amplitudes.



Codes were often used to keep the information secret or break it into pieces manageable by technology. Digital signals could be processed by digital circuit components, using less bandwidth and electromagnetic interference. Information storage was easier in digital systems than in analog ones. The noise immunity of digital systems allowed data to be stored and retrieved without degradation. ICs had two main advantages over discrete circuits: cost and performance. A logic gate was an elementary building block of a digital circuit, with two inputs and one output.

Operation	Expression
AND	Y = AB
OR	Y = A+B
NOT	Y = A'
XOR	Y = AB' + A'B
NAND	Y= A' + B'
NOR	Y= A' B'

AND Operation:

The AND operation produces a high if all the inputs are high. Here is the symbol and Truth Table of AND gate.

Fig1.1: Symbol of AND gate

Truth Table:

Input, A	Input, B	Output, F
0	0	0
0	1	0
1	0	0
1	1	1

Pin configuration for IC-74HC08N:

74HC series devices are designed to work with a 5V power supply, allowing voltages from 2V to 5V for most circuits.

OR Operation:

The OR operation produces a high output when any of the inputs are high. Here is the symbol and Truth Table of OR gate.

Fig 1.2: Symbol of OR gate

Truth Table:

Input, A	Input, B	Output, F
0	0	0
0	1	1
1	0	1
1	1	1

Pin configuration for IC-74HC32N:

74HC32 is a Quad 2-input OR gate with low current consumption and wide voltage range, with high noise immunity characteristics.

NOT Operation:

The NOT operation is implemented by an inverter to change one logic level to another. Here is the symbol and Truth Table of NOT gate.

Fig1.3: Symbol of NOT gate

Truth Table:

Input, A	Output, F
0	1
1	0

Pin configuration for IC-74HC04N:

The 74HC04 is a hex inverter with six inverters, clamp diodes, current limiting resistors, and CMOS input level.

XOR Operation:

The XOR gate acts like a logical "either/or" gate, with the output being high if either input is high, low if both inputs are low, or 0 if both inputs are the same. Here is the symbol and Truth Table of XOR gate.

Fig 1.6: Symbol of XOR gate

Truth Table:

Input, A	Input, B	Output, F
0	0	0
0	1	1
1	0	1
1	1	0

Pin configuration for IC-74HC86N:

HC86 is a quad 2-input XOR gate with advanced silicon gate CMOS technology, low power consumption and high noise immunity. It has a voltage range of 2V-5V and an input current of 1A.

Part II:

Study of Universal Gates:

Universal Gates are Logic Gates that can be used to create any Logic Gate, such as NOT, AND, OR, XOR, XNOR, etc. NAND and NOR Gates are examples of Universal Gates.

The objective of this lab is to implement different logic functions using universal gates.

NAND operation:

The NAND gate acts as an AND gate followed by a NOT gate, resulting in a high output if both inputs are high. Here is the symbol and Truth Table of NAND gate.

Fig 1.4: Symbol of NAND gate

Truth Table:

Input, A	Input, B	Output, F
0	0	1
0	1	1
1	0	1
1	1	0

Pin configuration for IC-74HC00N:

The device code HC00 is compatible with Standard CMOS outputs, with an operating voltage range of 2.0-5 V and low input current of 1.0 A.

NOR operation:

The NOR gate is a combination OR gate followed by an inverter with a low output if both inputs are low. Here is the symbol and Truth Table of NOR gate.

Fig 1.5: Symbol of NOR gate

Truth Table:

Input, A	Input, B	Output, F
0	0	1
0	1	0
1	0	0
1	1	0

Pin configuration for IC-74HC02N:

The 74HC02 is a high-speed Si-gate CMOS device with a quadrature 2 -input NOR function and a low input current of 1.0 A.

Apparatus:

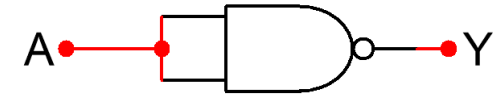
- Digital trainer board.
- IC or Integrated Circuits (7400,7402,7404,7408,7432,7486)
- Power supply.
- Connecting wires.
- LEDs (green and red)

Experimental Procedure:

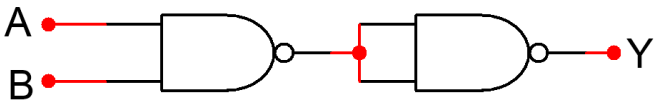
- Ensured all components needed were ready to use.
- Digital trainer board was set up first and provided with a power source relevant to each of the IC(4V).
- Each IC of different logic gates were chosen to place on the digital trainer board.
- Excluding the 1st and 14th IC connection we tried specific sequences according to the specific logic gates to create logic output.
- One power switch for NOT gate and two switches for other gates were always connected to the IC sequence diagram input.
- One red LED was connected with the IC sequence diagram output. AND green LEDS were connected to the input.
- According to the truth table of different logic gates. Variations were performed.

Circuit Diagram:

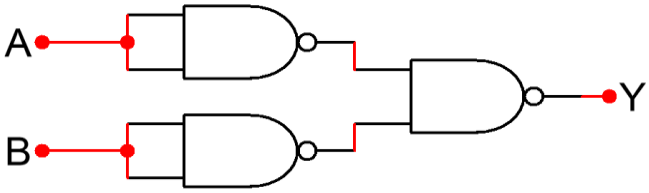
Implementing AND gate, OR gate & NOT gate using NAND gate:



NOT gate using NAND gates



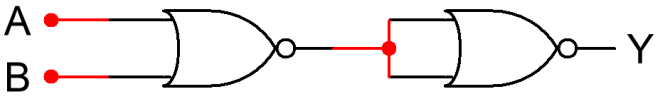
AND gate using NAND gates



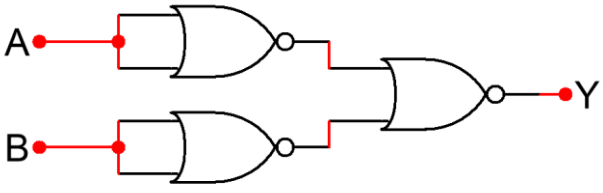
OR gate using NAND gates

Implementing AND gate, OR gate & NOT gate using NOR gate:

NOT gate using NOR gates



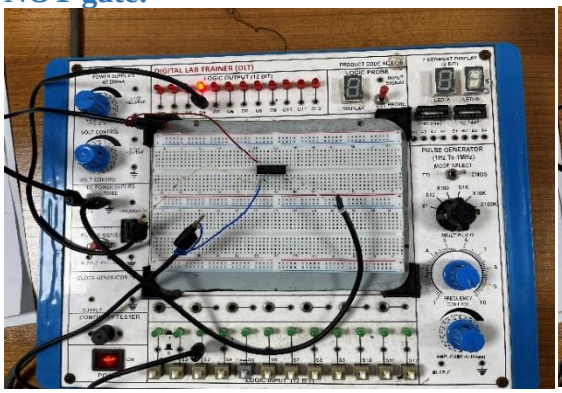
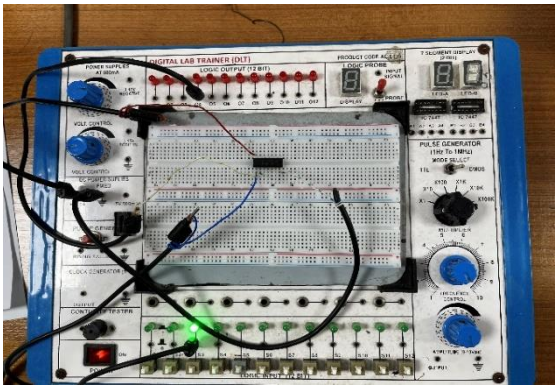
OR gate using NOR gates



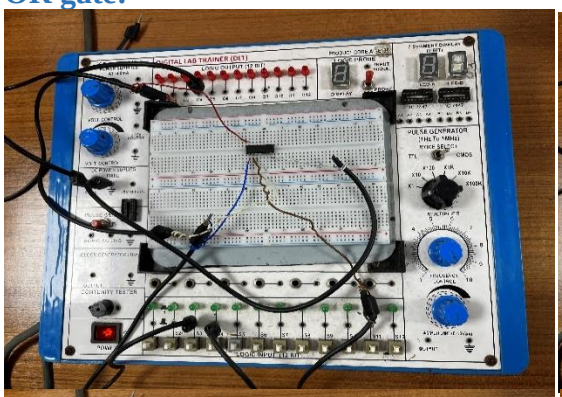
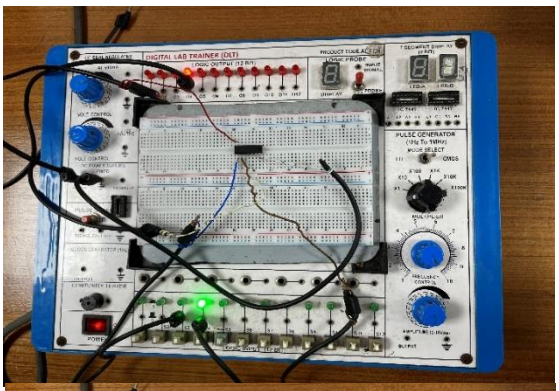
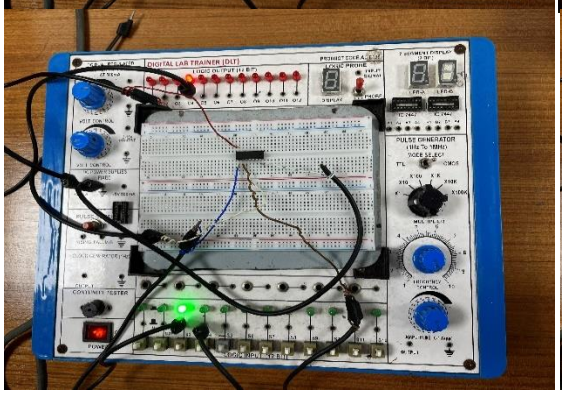
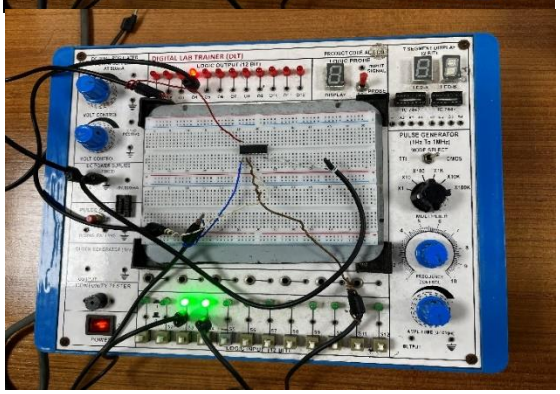
AND gate using NOR gates

Images:

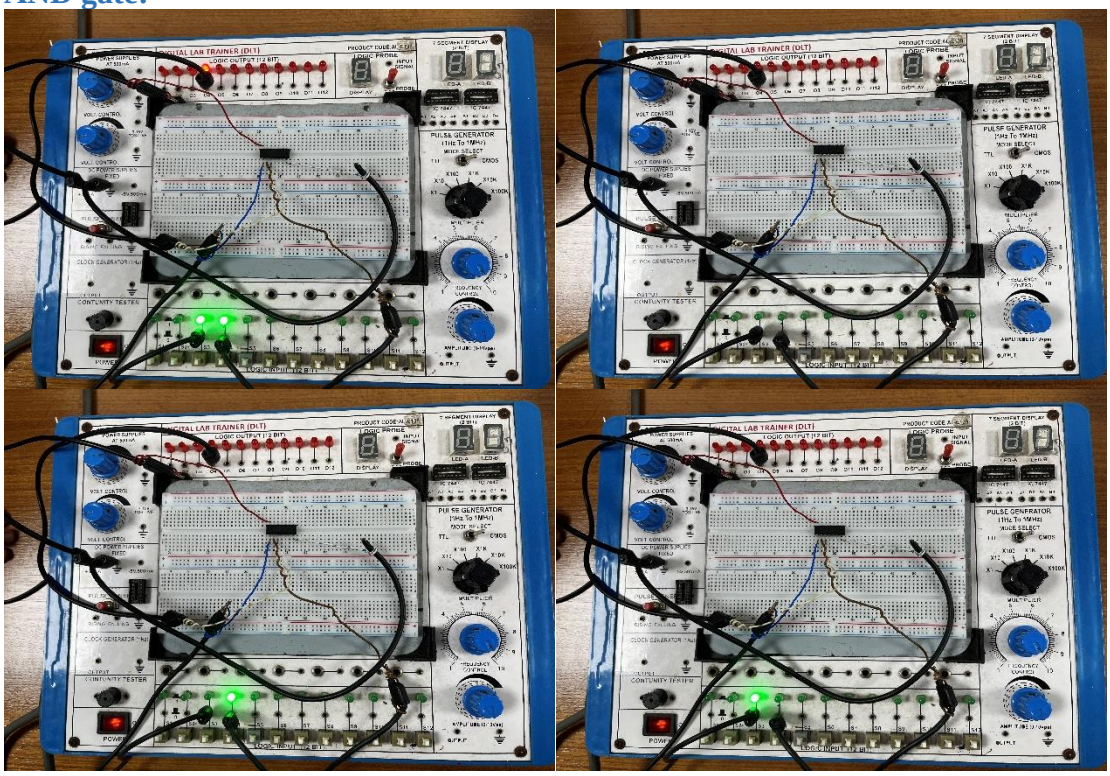
NOT gate:

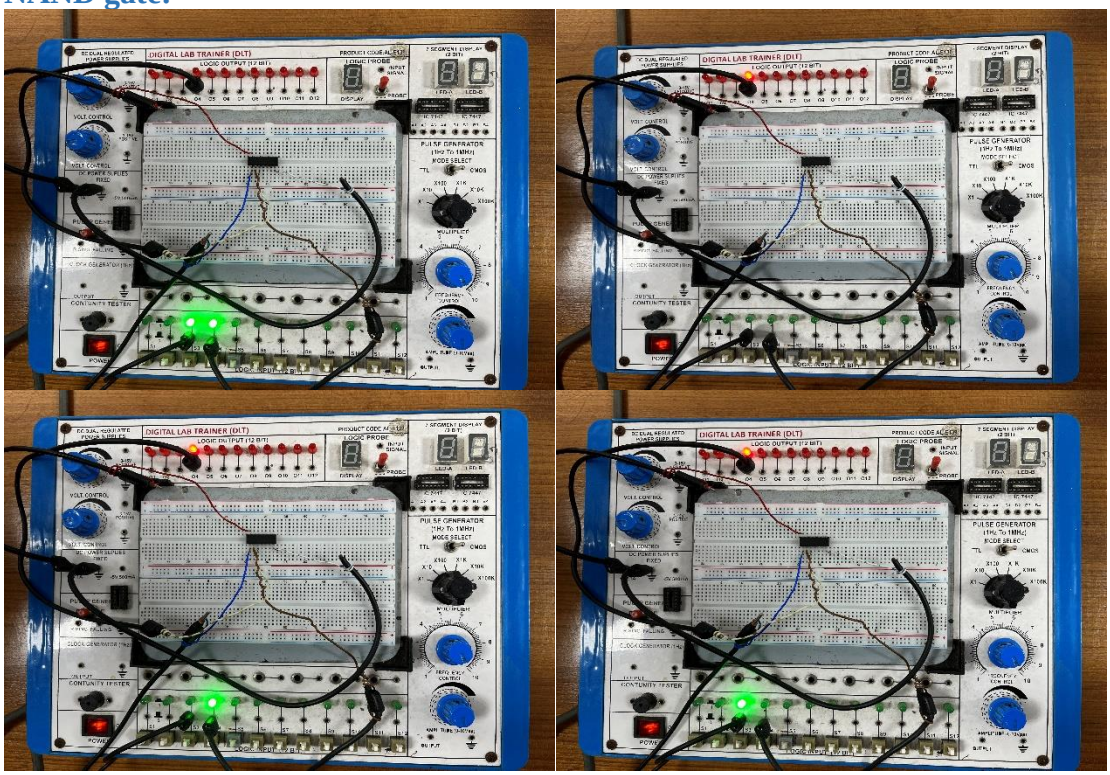
OR gate:

AND gate:

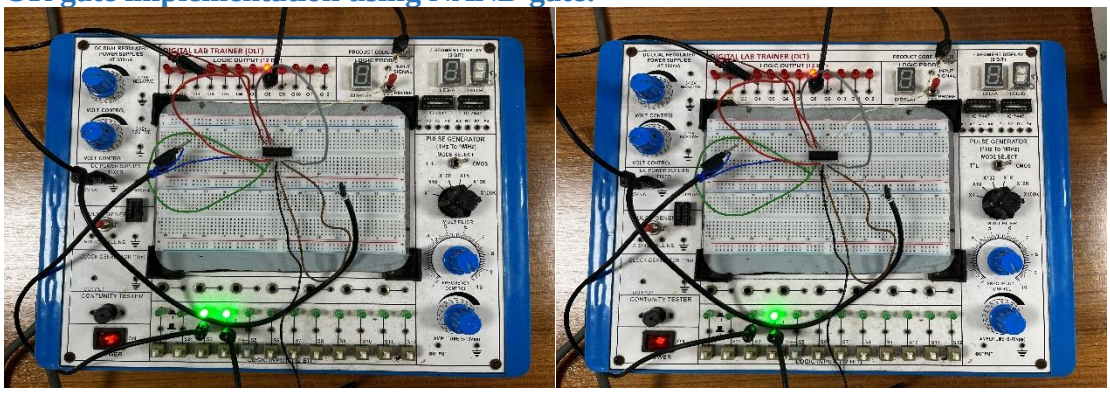


NAND gate:

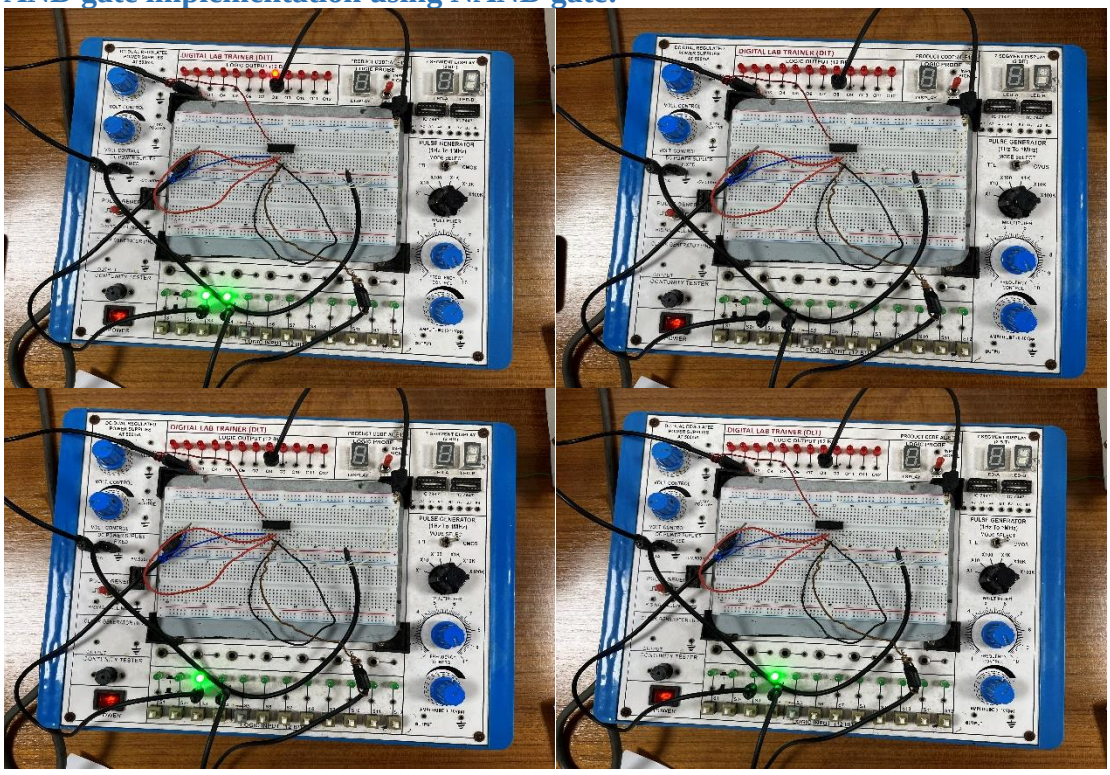


NOT gate implementation using NAND gate:

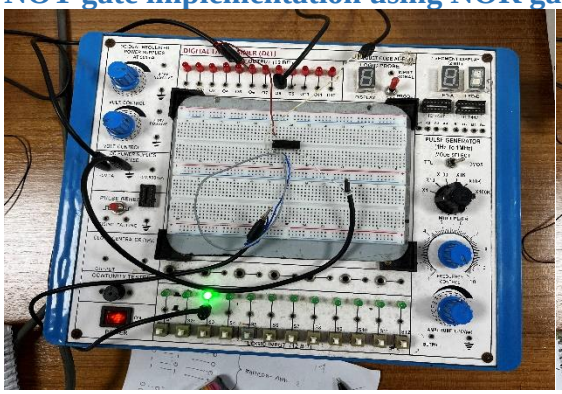
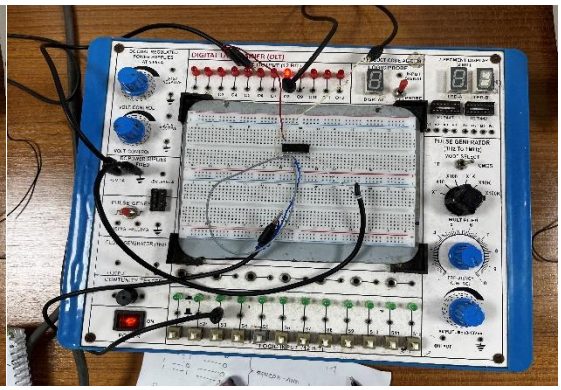
OR gate implementation using NAND gate:



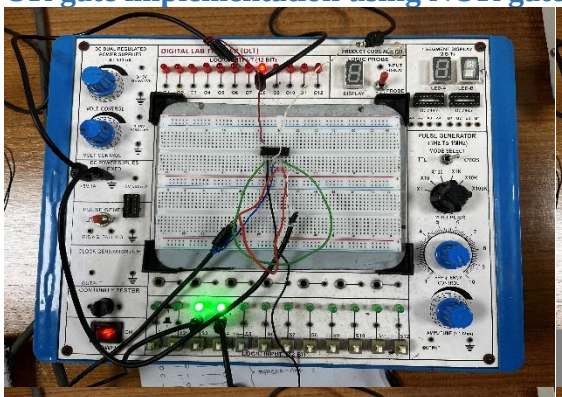
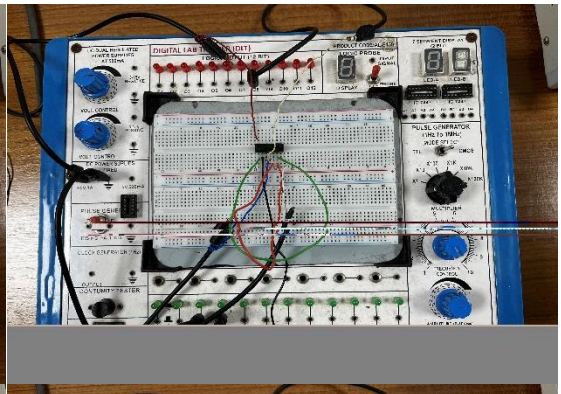
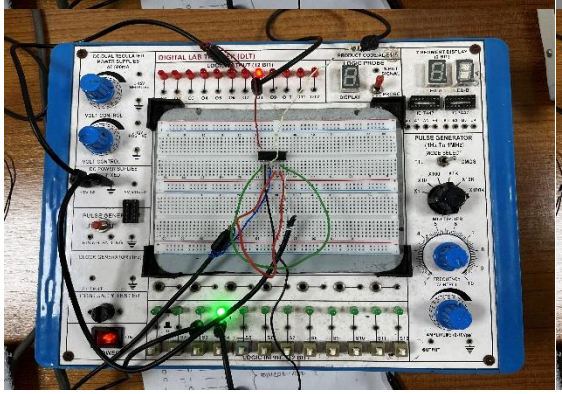
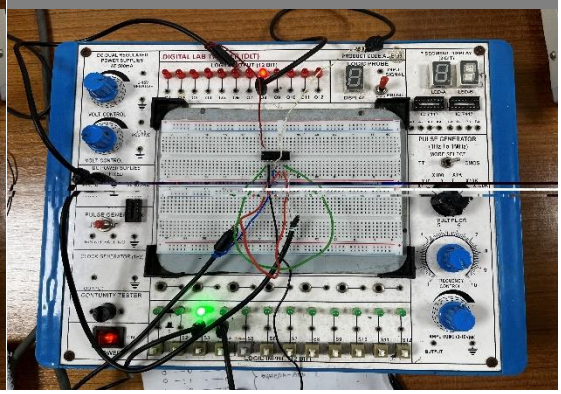
AND gate implementation using NAND gate:



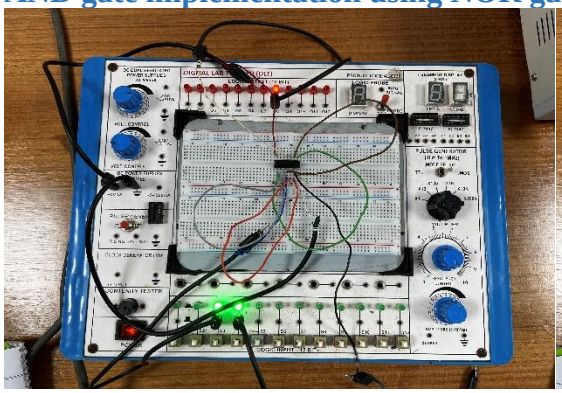
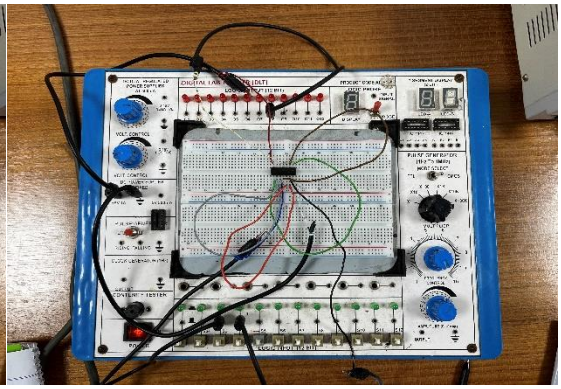
NOT gate implementation using NOR gate:

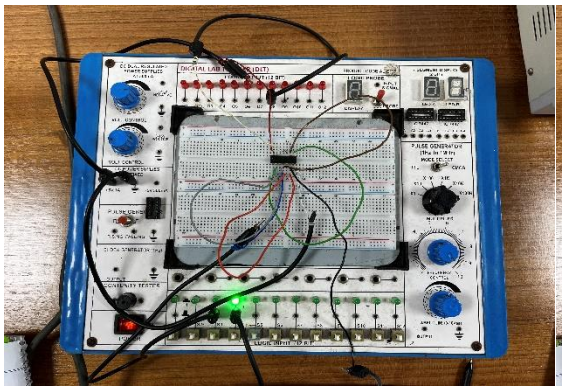



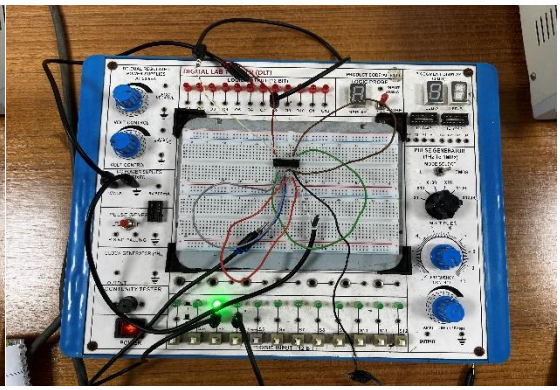
OR gate implementation using NOR gate:

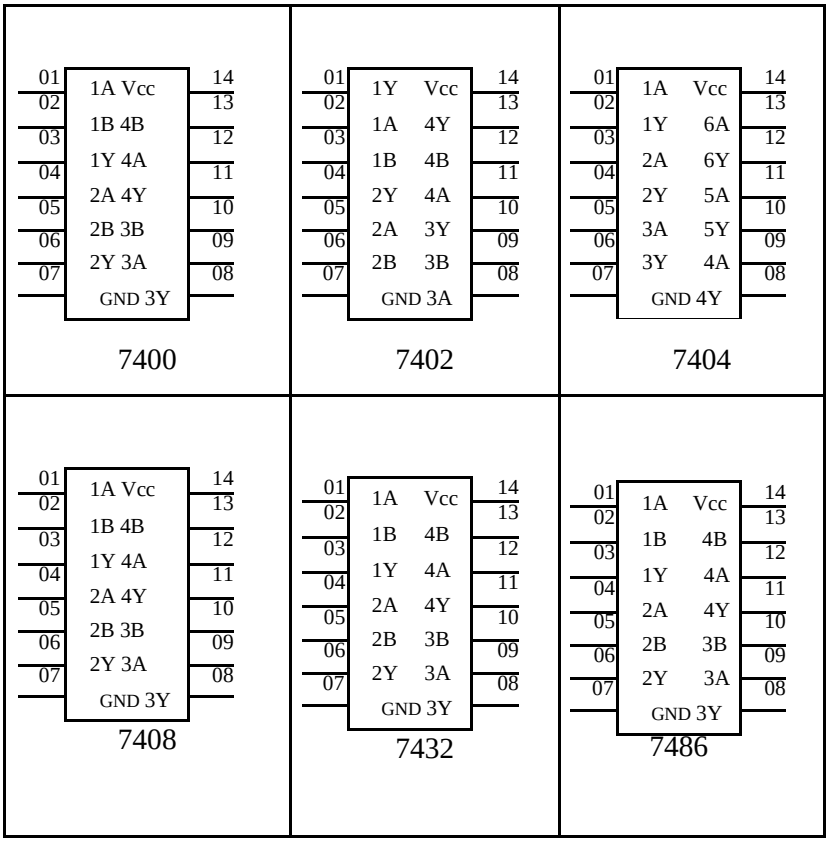
AND gate implementation using NOR gate:





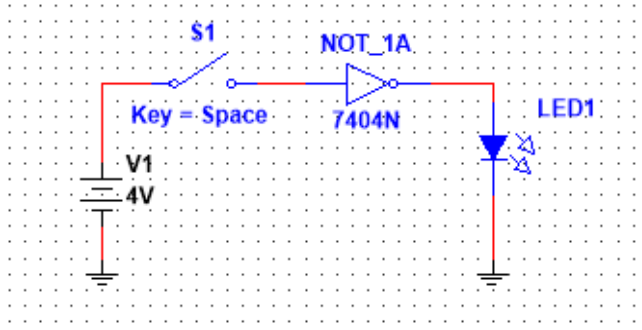
IC Configuration:

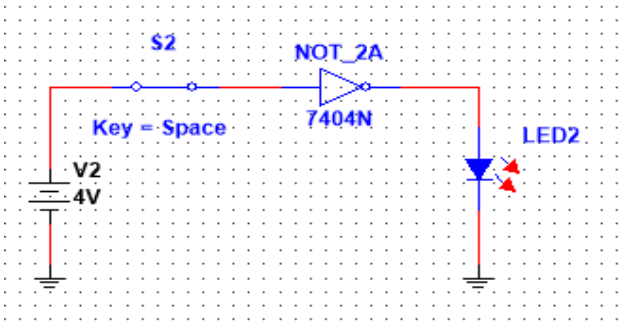


MULTISIM:

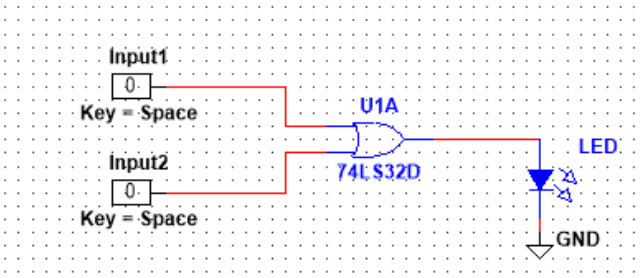
PART I:

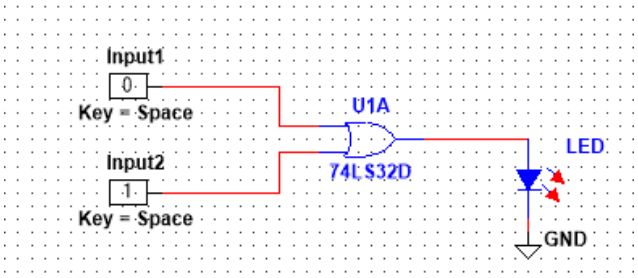
Simulation for NOT gate:

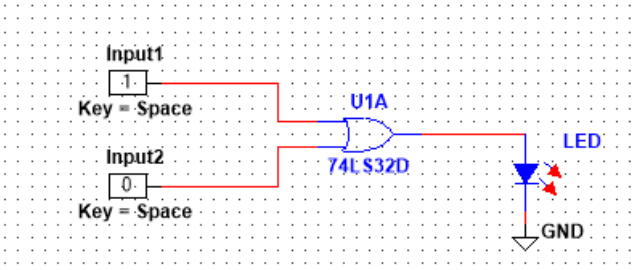


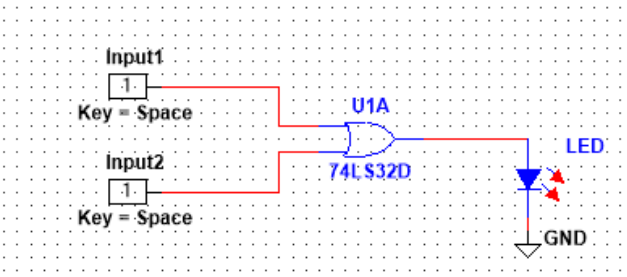


Simulation for OR gate:

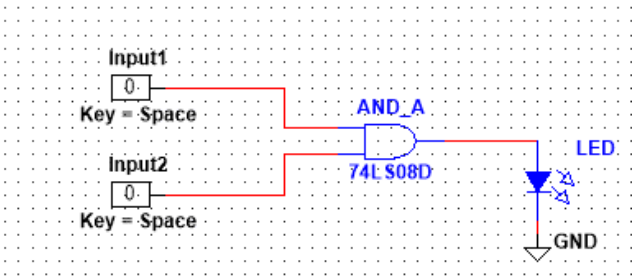


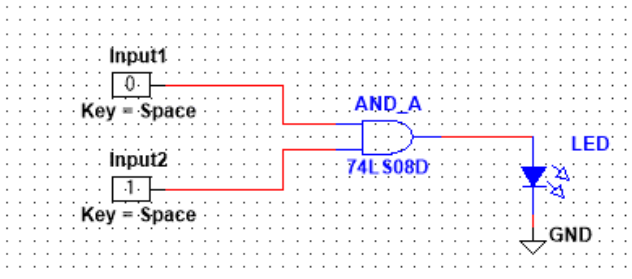


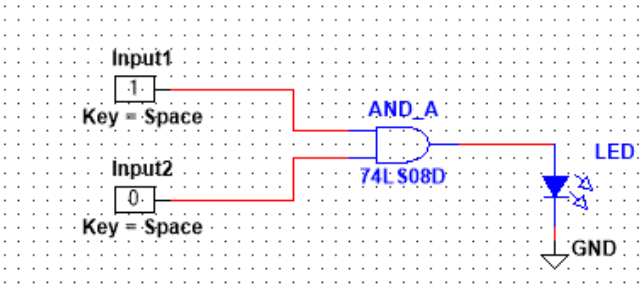


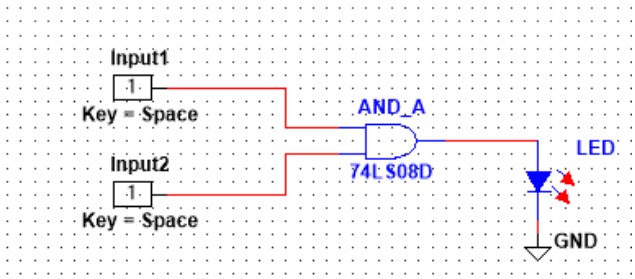


Simulation for AND gate:

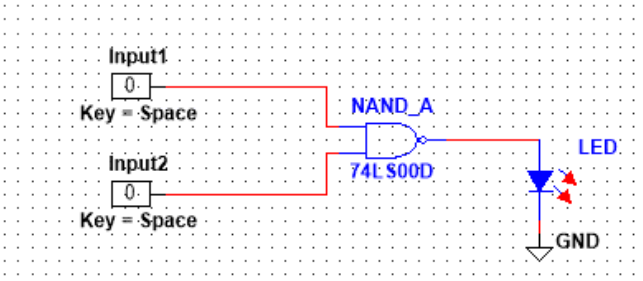


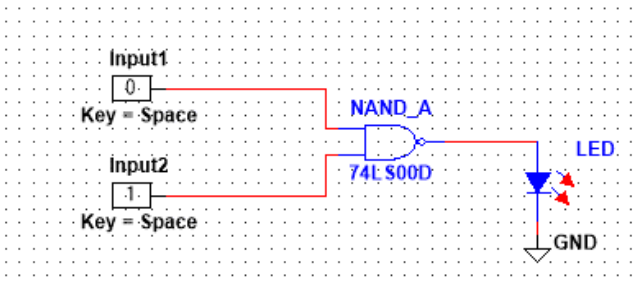


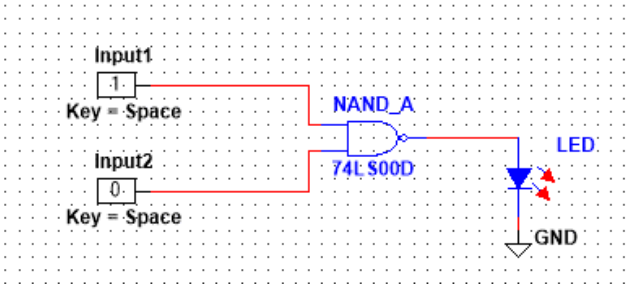


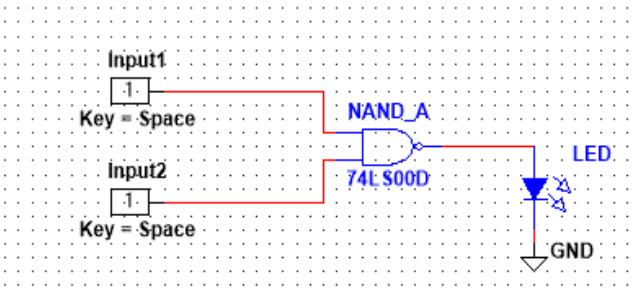


Simulation for NAND gate:

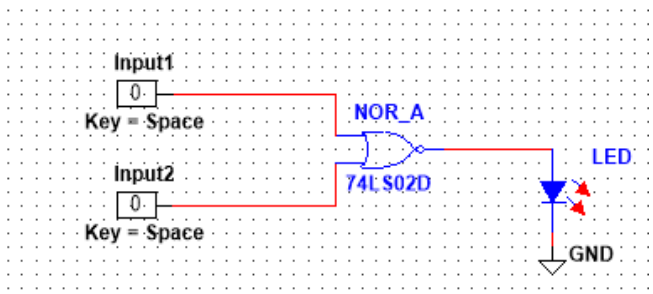


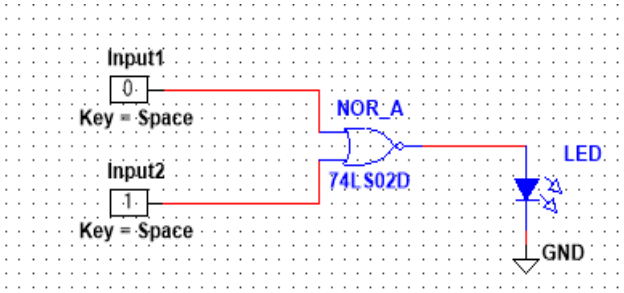


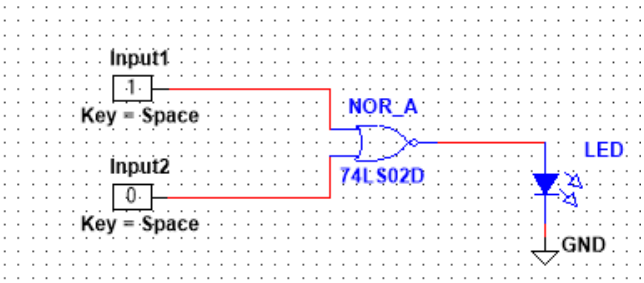


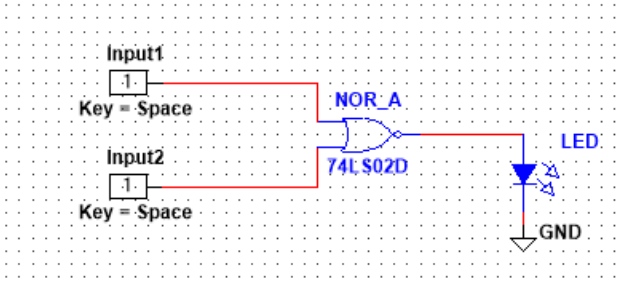


Simulation for NOR gate:

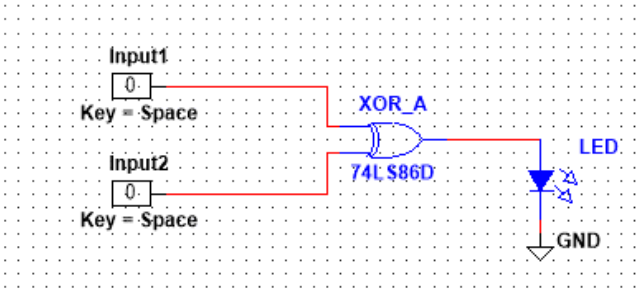


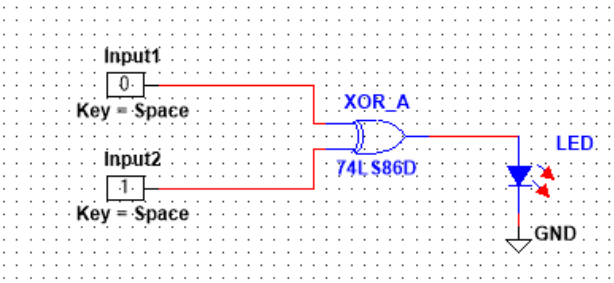


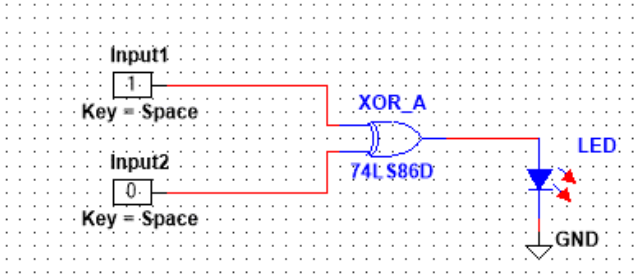


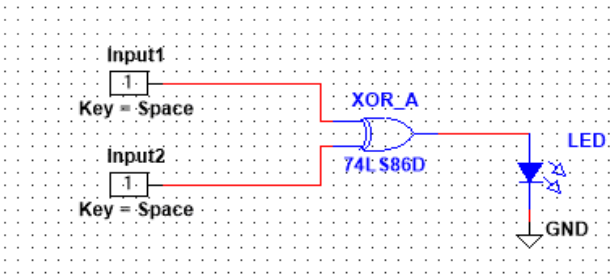


Simulation for X-OR gate:



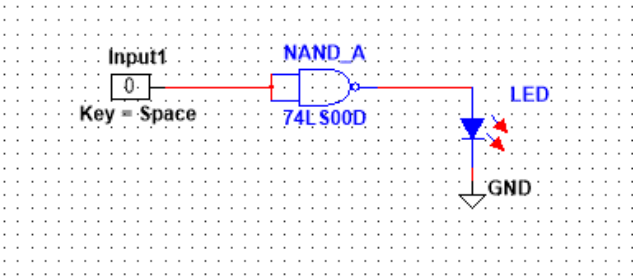


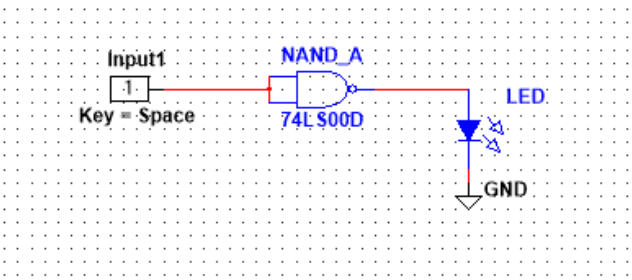




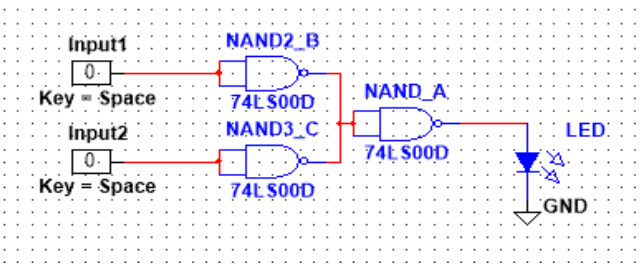
PART II:

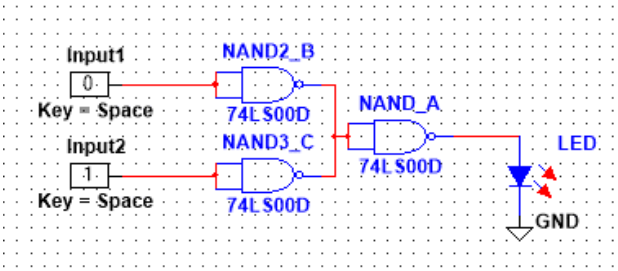
Implementing NOT gate using NAND gate:

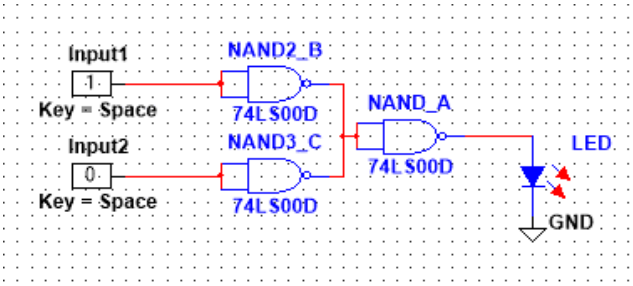


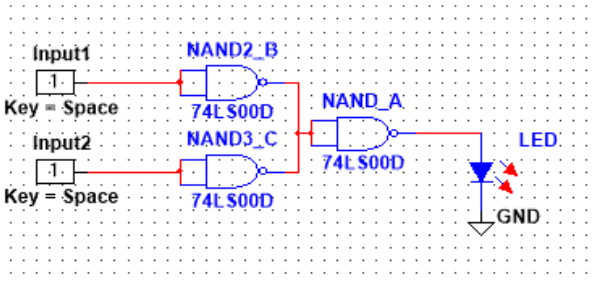


Implementing OR gate using NAND gate:

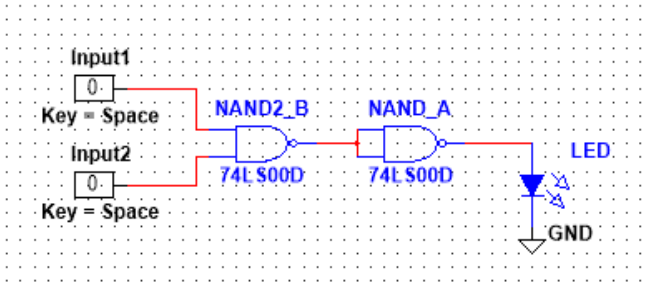


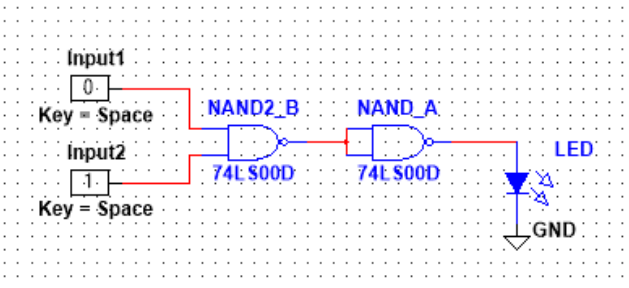


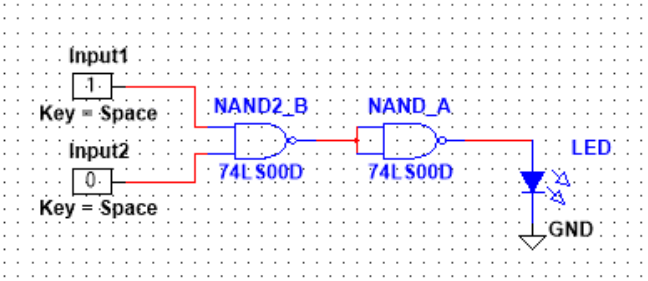


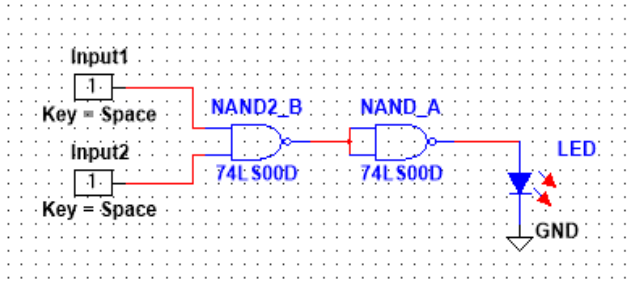


Implementing AND gate using NAND gate:

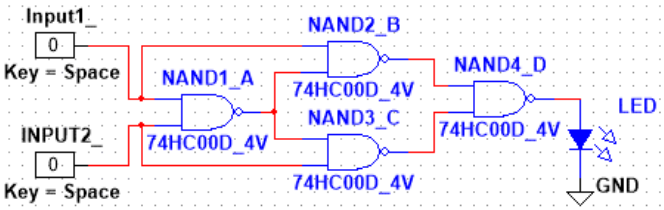


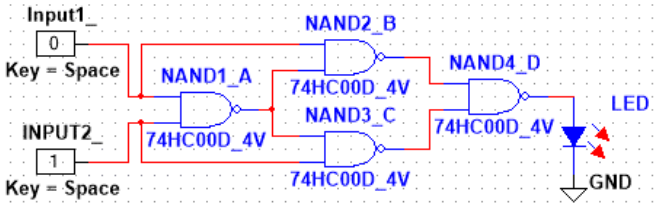


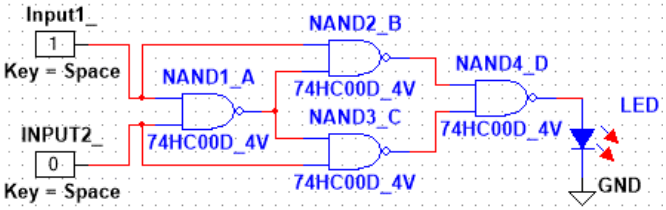


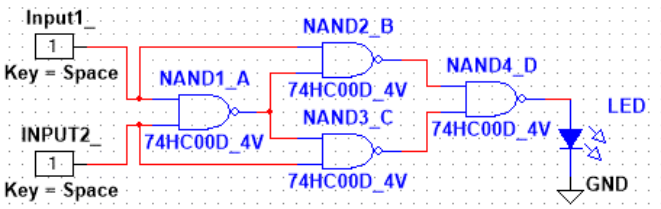


Implementing XOR gate using NAND gate:

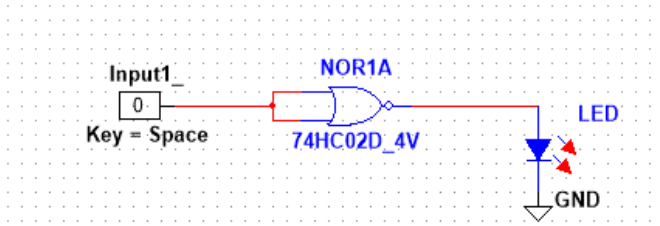


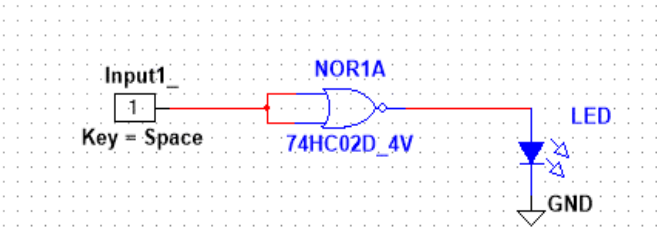




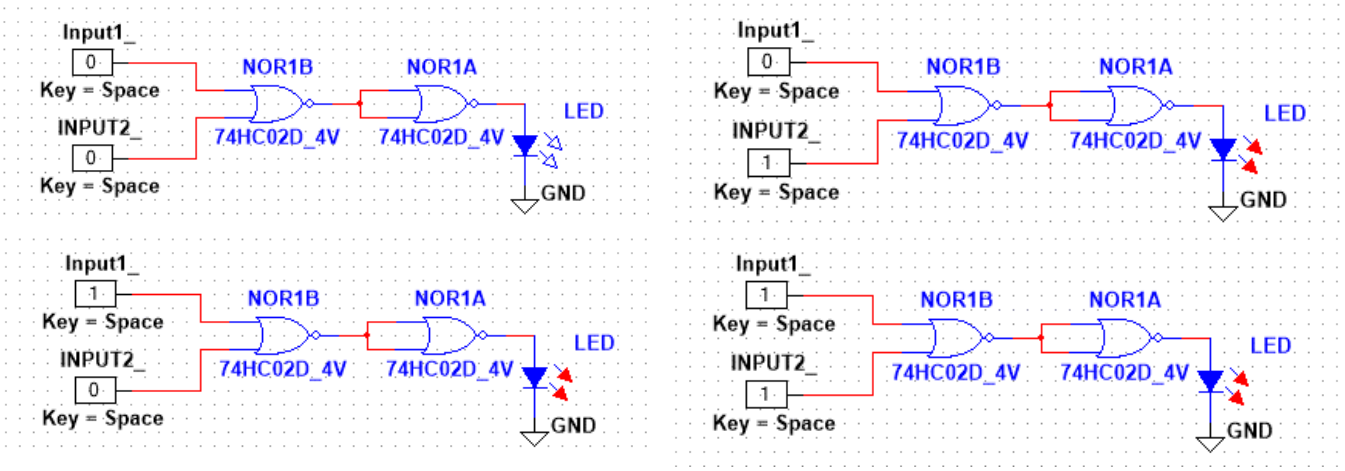


Implementing NOT gate using NOR gate:

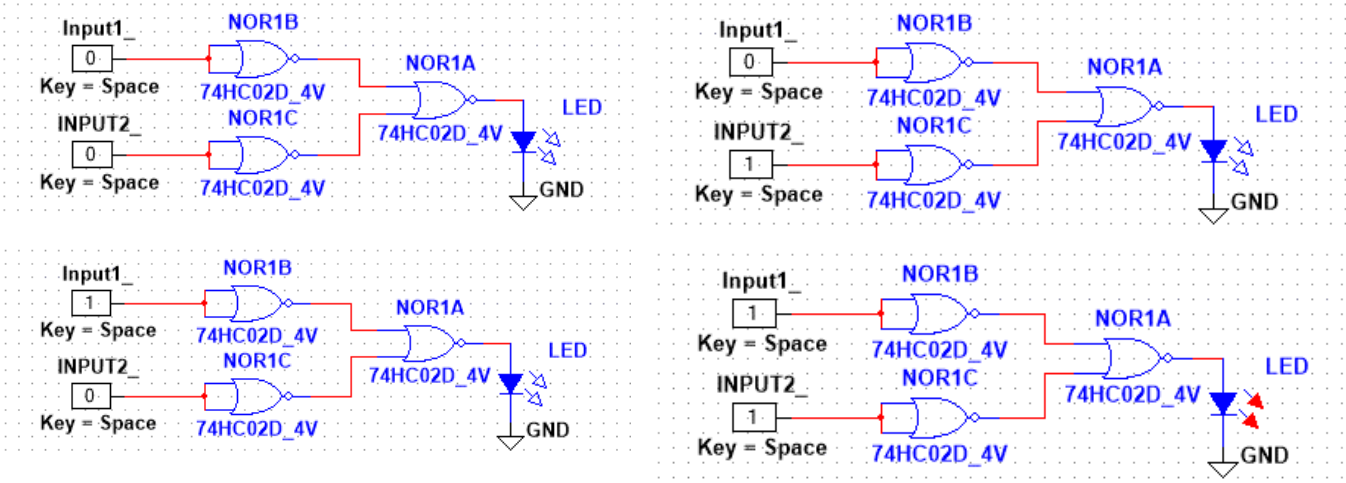




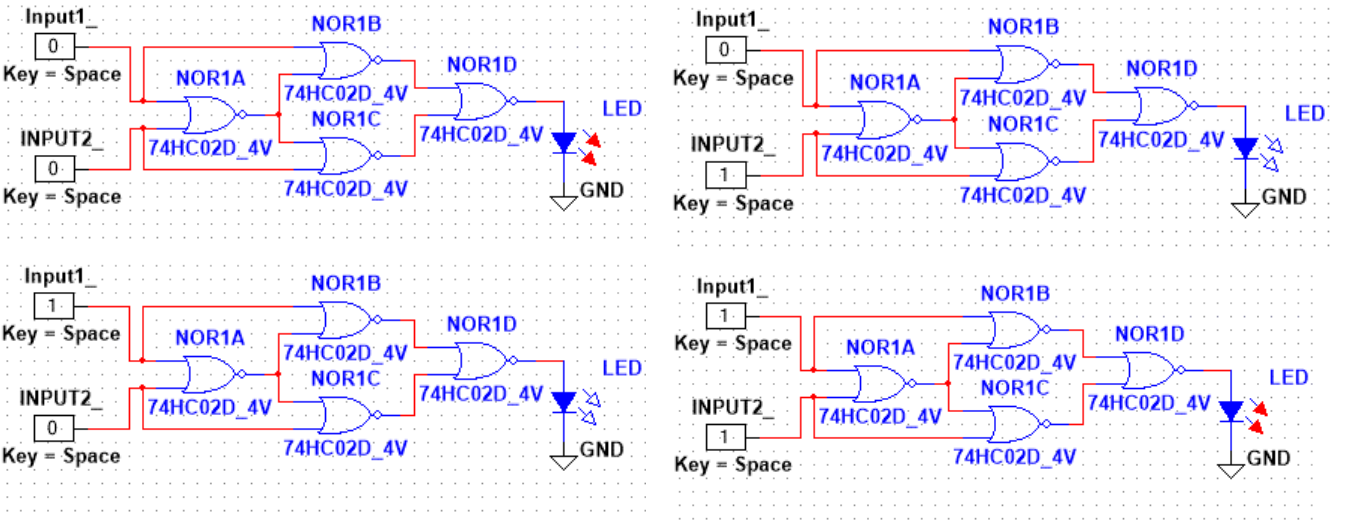
Implementing OR gate using NOR gate:



Implementing AND gate using NOR gate:



Implementing XOR gate using NOR gate:



Discussion and Conclusion:

In this experiment, we have used Multisim software for Simulations. While using this, we faced some problems. Overall, using the software to locate the solution was simple, and a beginner's ability to draw a circuit was average. Firstly, we need to understand truth-table and the design oflogic gates. Afterward, we can decide how to prepare for working with Multisim Software. We have successfully and error-free assembled all the components in the breadboard. We have successfully verified that there are no issues in connecting the circuit wires. At last, the Truth-table for the logic gates were verified by the results and simulations and they matched with each other.

Reference:

"Digital Fundamentals" by Thomas L. Floyd

- www.tutorialspoint.com
- www.electronics-tutorials.ws
- www.faculty.kfupm.edu.sa