American International University – Bangladesh (AIUB)
Faculty of Engineering
Department of CSE, EEE, and CoE

EEE3102 Digital Logic and Circuits LAB
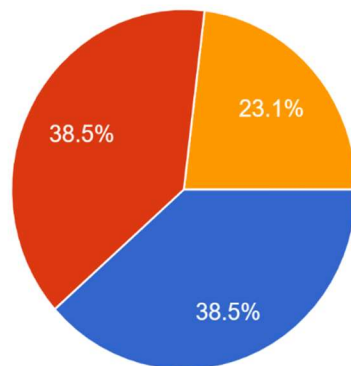# PROJECT PROPOSAL FORM

SEMESTER: Summer 2023-2024
PROJECT TITLE: 0 to 99 Counter Circuit

Survey to develop a process for complex engineering problems with a wide range of conflicting requirements (pie chart):

If you were to use the "0 to 99 Counter Circuit" for a specific purpose, what would it be?
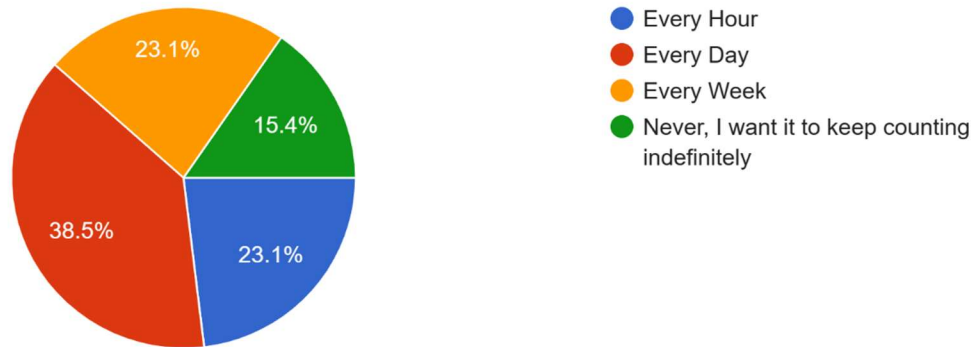
13 responses

- ● Keeping track of completed workouts
- ● Counting down to a special event
- ● Monitoring the number of days since a significant life event
- ● Just as a quirky piece of home decor

23.1%
38.5%
38.5%

How often would you want the "0 to 99 Counter Circuit" to reset and start counting from zero?

13 responses

- ● Every Hour
- ● Every Day
- ● Every Week
- ● Never, I want it to keep counting indefinitely

What color scheme would you prefer for the circuit's casing and design?

14 responses

- ● Classic Black & White
- ● Vibrant Rainbow Colors
- ● Futuristic Silver & Blue
- ● Steampunk Antique Brass

Which feature is a must-have for your "0 to 99 Counter Circuit"?

15 responses

- ● Sound Effects with Each Count
- ● Wireless Remote Control
- ● Bluetooth Connectivity to a Smartphone App
- ● Built-in Mini Game

If you were to use the "0 to 99 Counter Circuit" for a specific purpose, what would it be?

14 responses

- ● Keeping track of completed workouts
- ● Counting down to a special event
- ● Monitoring the number of days since a significant life event
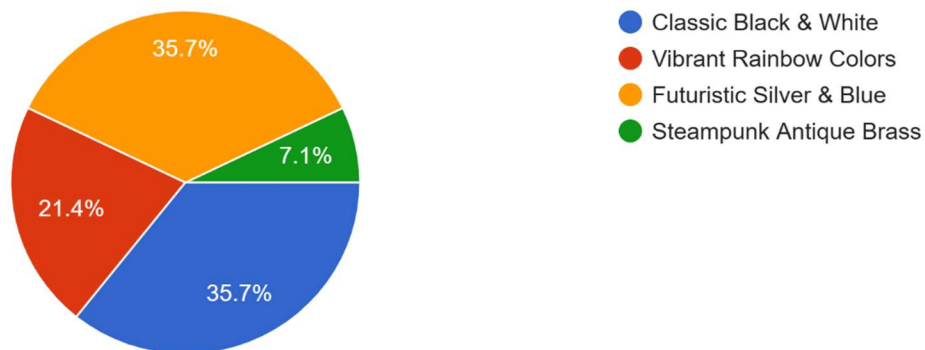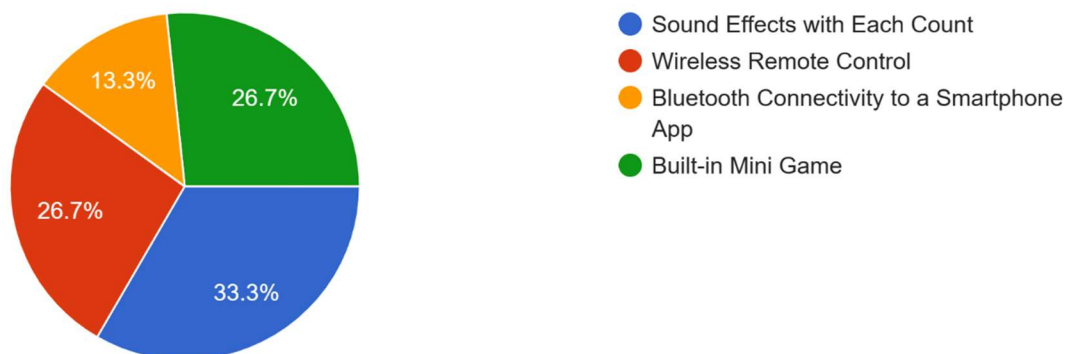- ● Just as a quirky piece of home decor
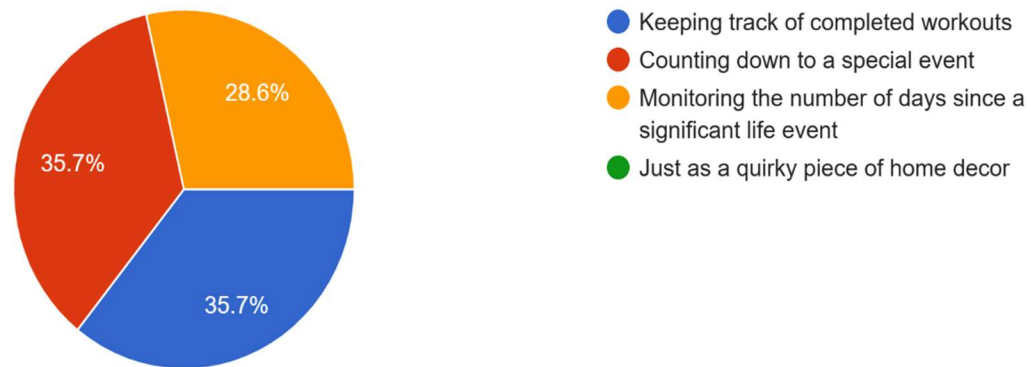
<u>AIMS AND OBJECTIVE OF THE PROJECT</u>

The primary aim of the "0 to 99 counter circuit" project is to create a highly precise counting system that reliably tallies from 0 to 99 without any discrepancies. This circuit will feature a user-friendly display interface, ensuring easy and accurate readability of the counted values. Our objective is to design a compact, space-efficient circuit with intuitive controls, making it suitable for integration into a wide range of electronic projects. We will implement error-checking mechanisms to minimize counting errors and provide rigorous testing and calibration for consistent performance. Comprehensive documentation will be produced to guide users in building and operating the circuit. The design will emphasize flexibility for seamless integration into other systems and maintain cost-effectiveness by choosing affordable, widely available components without compromising quality.

EXPERIMENTAL BLOCK DIAGRAM:
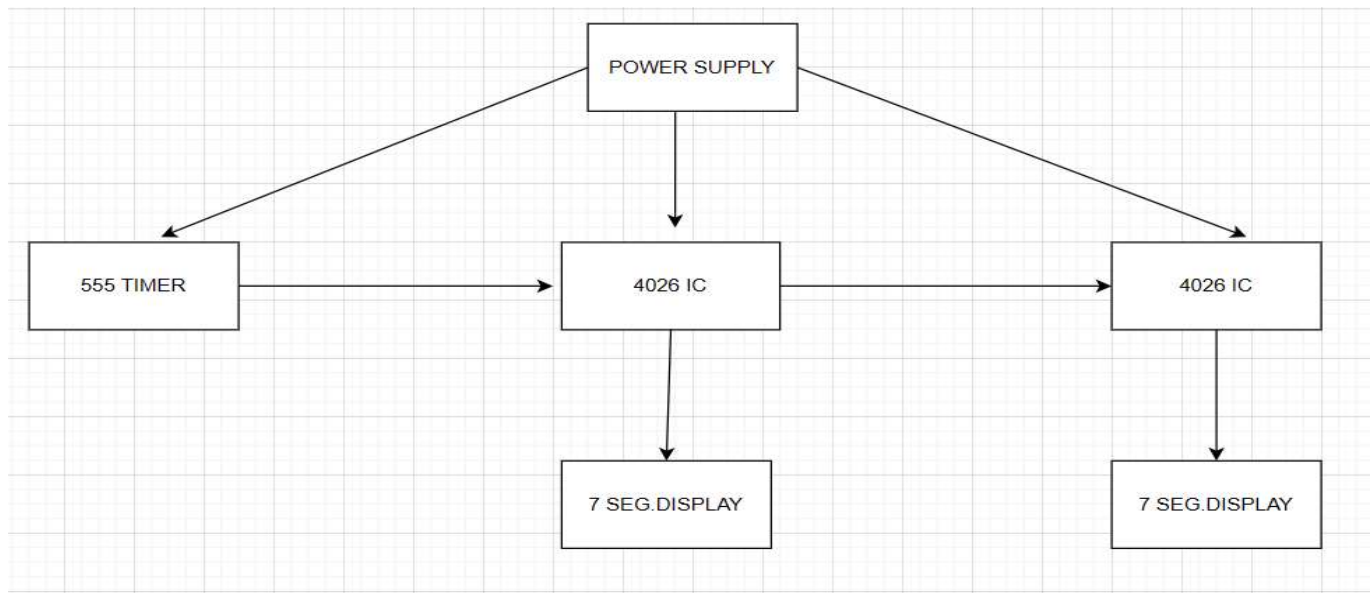
PROJECT TIMELINE (GANTT CHART):

Task	DAY 1	DAY 2	DAY 3	DAY 4	DAY 5	DAY 6	DAY 7
Project planning	x						
Component sourcing		x	x				
Prototype build				x			
Testing and debugging					x		
Final integration					x	x	
Documentation							x

REFERENCES:

[1] M. H. Bhuyan and Q. D. M. Khosru, "Linear Asymmetric Pocket Profile Based Pinch Off Voltage Model for Nano Scale n-MOSFET," Proceedings of the IEEE sponsored International Conference on Electrical, Computer and Communication Engineering (ICECCE2017), organized by the Chittagong University of Engineering and Technology (CUET), Cox's Bazar, Bangladesh, 16-18 February 2017, pp. 28-32.

FACULTY USE ONLY

**COURSE TEACHER'S NAME
DATE**

COURSE TEACHER'S SIGNATURE

GROUP MEMBERS

(Maximum 6 students are permitted to carry out a single Project. However, depending on the capability of the students, 4 students may be allowed but not less than that)

NAME: TRIDIB SARKAR ID: 22-46444-1 PROGRAM: CSE EMAIL: sarkartridib886@gmail.com	NAME: S.M. MUJAHID SOUROV ID: 22-49679-3 PROGRAM: CSE EMAIL: smmujahidsourov@gmail.com
NAME: NUSHRAT JAHAN ID: 22-46149-1 PROGRAM: CSE EMAIL: nushratjahanohi@gmail.com	NAME: MD. FAHIM MURSHED ID: 22-46695-1 PROGRAM: CSE EMAIL: fahimmorshed86@gmail.com
NAME: MD. ATIK ISHRAK SUJON ID: 22-46684-1 PROGRAM: CSE EMAIL: 22-46684-1@student.aiub.edu	
REMARKS (for OFFICE use only)	

Course Outcome Mapping with the Course Project Proposal:

COs/CLOs	Details	K	P	A	Assessed Program Outcome Indicator	BNQF Indicator	Assessment Techniques
CO1	Apply proper information and concepts of different logic gates, digital ICs, transistors, and timers to implement logical circuits considering a wide range of conflicting requirements.	K3	P1, P2, P6		P.a.3.C3	FS.1	Course Project Proposal Form

Course Name:	Digital Logic and Circuits Lab	**Course Code:**	EEE 3102
Semester:	Fall 2023-2024	**Section:**	Q
Faculty Member:	DR. TANBIR IBNE ANOWAR		

Course Project Title:	0 to 99 Counter Circuit
Project Group No.	02

SL	Student ID #	Student Name	Obtained Marks
1.	NUSHRAT JAHAN	22-46149-1	
2.	TRIDIB SARKAR	22-46444-1	
3.	MD. FAHIM MURSHED	22-46695-1	
4.	S.M. MUJAHID SOUROV	22-49679-3	
5.	MD. ATIK ISHRAK SUJON	22-46684-1	

Assessment Materials and Marks Allocation:

COs	Assessment Materials	POIs	Marks
CO1	Course Project Proposal form	P.a.3.C3	20

Assessment Rubrics

COs-POIs	Excellent [17-20]	Proficient [13-16]	Good [9-12]	Acceptable [5-8]	Unacceptable [1-4]	No Response [0]	Secured Marks
CO1 P.a.3.C3	The survey developed as a process for complex engineering problems considering a wide range of conflicting requirements and implementation process is clear and challenging for future project implementation.	The survey developed as a process for complex engineering problems considering a wide range of conflicting requirements, but the conflicting requirements are less in number and implementation process is clear and challenging for future project implementation.	The survey developed as a process for complex engineering problems considering a wide range of conflicting requirements, but the conflicting requirements are less in number and implementation process is not so clear but seems challenging for future project implementation.	The survey developed as a process for complex engineering problems considering a wide range of conflicting requirements, but the conflicting requirements are fewer in number and implementation process is not so clear and seems less challenging for future project implementation.	The survey developed as a process for complex engineering problems considering a wide range of conflicting requirements, but the conflicting requirements are very few in number and implementation process is not clear at all and seems impractical for future project implementation.	No Response	
Comments						**Total marks (20)**	