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DIGITAL LOGIC AND CIRCUITS LABORATORY

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Group: 02, Section: Q

LAB REPORT ON:

Design of a Digital to Analog Converter

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Title: Design of a Digital to Analog Converter

Introduction:

This lab describes the design of a Digital to Analog Converter (DAC). Two types of design are shown in this lab, binary weighted DAC and R/2R ladder DAC design. Finally, student will compare both the design to conclude which design is efficient and why.

Theory and Methodology:

In any communication system, the analog signal which is in the form of physical variables is converted to digital value by ADC. This digital signal is converted back to Analog signal for further processing i.e. Analog signal is necessary to drive Motors, temperature controller etc.

Binary Weighted Digital-to-Analog Converter:

In this type of Converter, every digital input bit that needs to be converted, requires one resistor or current source. These resistors are connected across the inputs and the summing point. The output is generated through this Summing Amplifier Circuit. **Fig. 1** below shows a typical Binary Weighted Resistor Converter Circuit which consists of an Op-Amp, four resistors which are connected at the input terminal of Op-amp along with the Feedback Resistor. These Resistors at the input terminal are called as Variable Resistors. Here, A, B, C, D are the digital inputs where 'D' is at MSB and 'A' is at LSB. and V is the output Analog Voltage. [1]

The output of the Summing Amplifier circuit is given by the equation:

$$V_{out} = -R_f \left(\frac{D_3}{R} + \frac{D_2}{2R} + \frac{D_1}{4R} + \frac{D_0}{8R} \right)$$
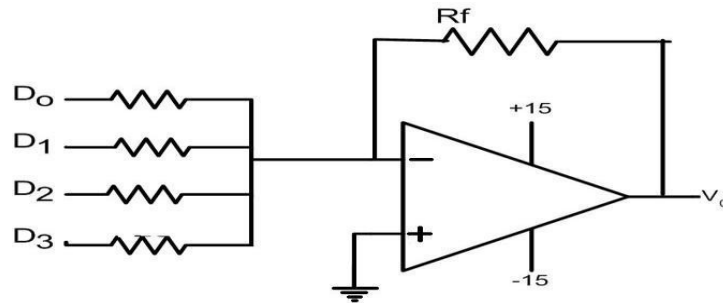

Fig1: Binary Weighted Digital to Analog converter.

R/2R Ladder Digital-to-Analog Converter:

This type of Converter has only two values of Resistors, R and 2R. The conversion speed reduces in this type of DAC due to parasitic capacitance. It is the simplest type of DAC where the switch between ground and inverting input of the Op-amp is controlled by the input bit. **Fig. 2** shows Binary Ladder or R–2R Ladder DAC. To understand its working, let us consider only the Resistors in the network, omitting Op-amp and assuming the input to be DCBA = 1000. Now the output for the reduced network is given by-

$$\text{output} = \left(\frac{2R}{2R+2R}\right) \times (+V) = \frac{V}{2}$$

Similarly, with the change in the input bits, the voltage will be V/4, V/2, V/16...... etc. Now, adding the Op-amp to the circuit, V4 becomes the input to the non-inverting Amplifier whose Gain is defined by the equation:

$$A_V = -R/2R = -1/2$$

Hence the output voltage of R–2R Ladder DAC is given by the equation:

$$V_O = -R \times \left(\frac{D}{2R} + \frac{C}{4R} + \frac{B}{8R} + \frac{A}{16R}\right)$$

In binary-weighted DAC, we need exact multiples of the resistors (R, 2R, 4R, 8R, 16R). For this reason, DAC of higher bits, the construction becomes practically infeasible. R-2R DAC solves this problem. Its construction only requires resistors of value R and 2R.
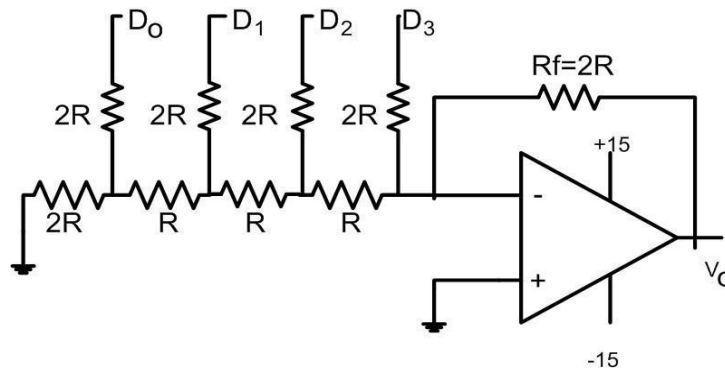

Fig 2: R/2R Ladder DAC

Apparatus:

1) IC741 OPAMP
2) Resistors as required
3) Trainer Board
4) Multimeter

Precautions:

Never turn on the DC source before the circuit is placed correctly and checked carefully. Check for short circuits in the circuit.

Experimental Procedure:

1. The Binary Weighted Digital to Analog converter was set up on the trainer board as shown in Fig1.
2. The sequence 1000, 0100, 0010, 0001 were put into D0, D1, D2 and D3 respectively and the output was observed on the Multimeter.
3. The R/2R ladder was setup on the trainer board again.
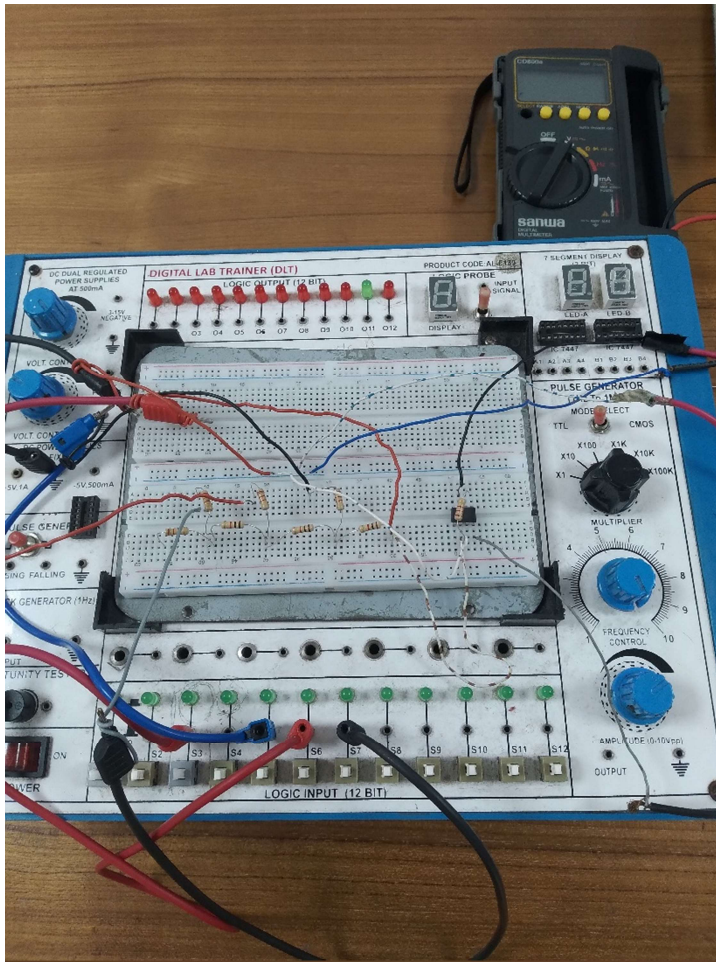4. Step 2 was repeated for R/2R DAC.

Experimental and Measurement:

Binary Weighted DAC:
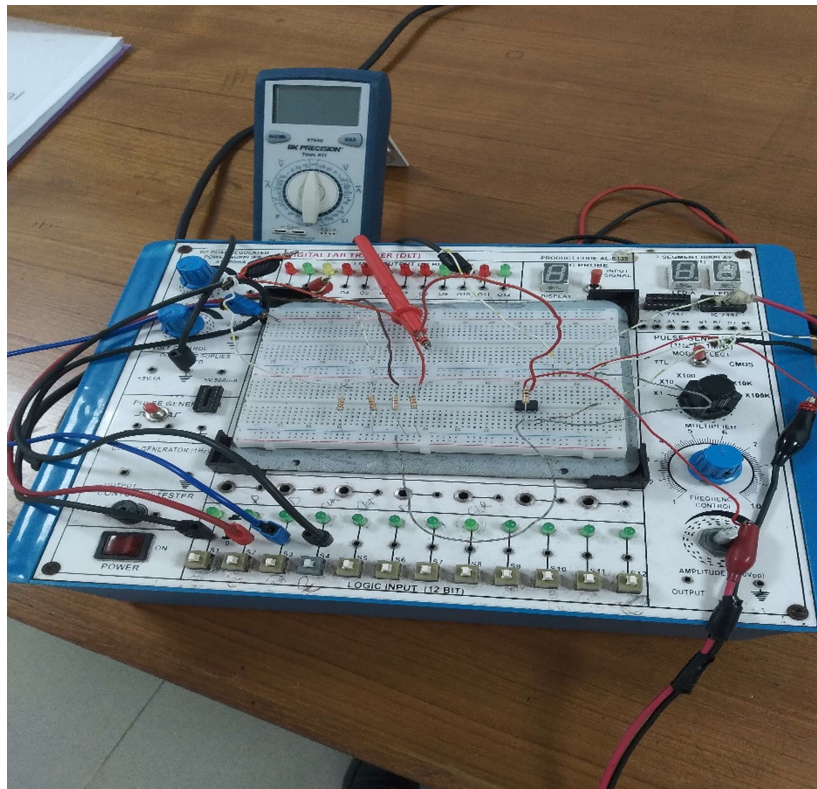
$D_0 = 8.2K$
$D_1 = 4.7 K$
$D_2 = 2.2 K$
$D_3 = 1 K$
$R_f = 1 K$

Fig. 3: Experimental Design of Binary Weighted Digital to Analog converter

R/2R Ladder DAC:

2R =2.2 K
R = 1 K

Fig 4: Experimental Design of R/2R Ladder DAC

Simulation and Measurement:

Binary Weighted DAC:

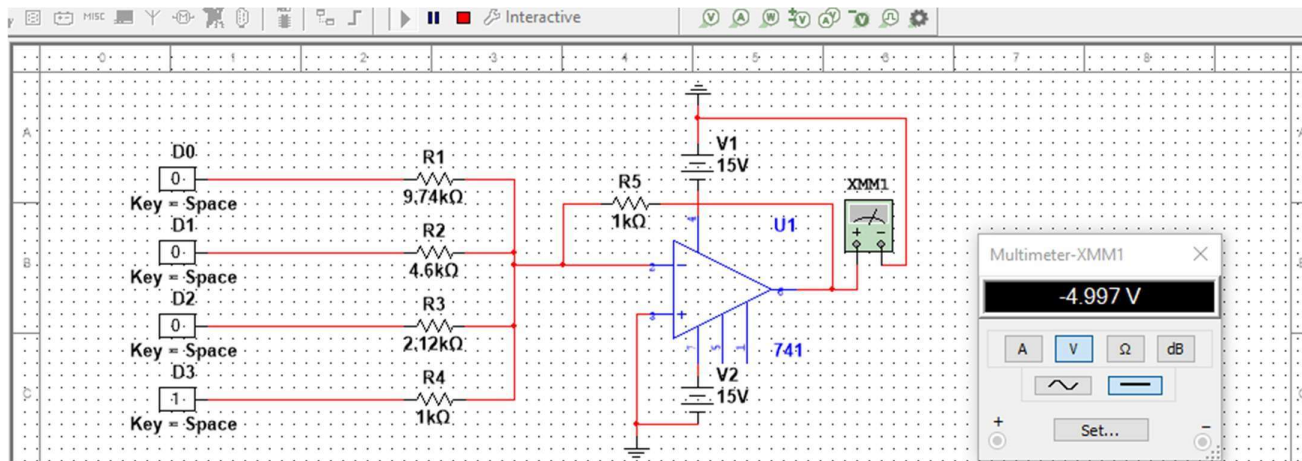

Fig. 5: Simulation of Binary Weighted Digital to Analog converter

Table 1: Truth table of simulation output for Binary Weighted DAC

Digital Inputs				Analog Output
D_3	D_2	D_1	D_0	Voltage (V_{out})
0	0	0	0	0V
0	0	0	1	-0.58V
0	0	1	0	-1.03V
0	0	1	1	-1.62V
0	1	0	0	-2.28V
0	1	0	1	-2.87V
0	1	1	0	-3.30V
0	1	1	1	-3.89V
1	0	0	0	-4.98V
1	0	0	1	-5.58V
1	0	1	0	-6.02V
1	0	1	1	-6.61V
1	1	0	0	-7.27V
1	1	0	1	-7.85V
1	1	1	0	-8.29V
1	1	1	1	-8.87V

R/2R Ladder DAC:

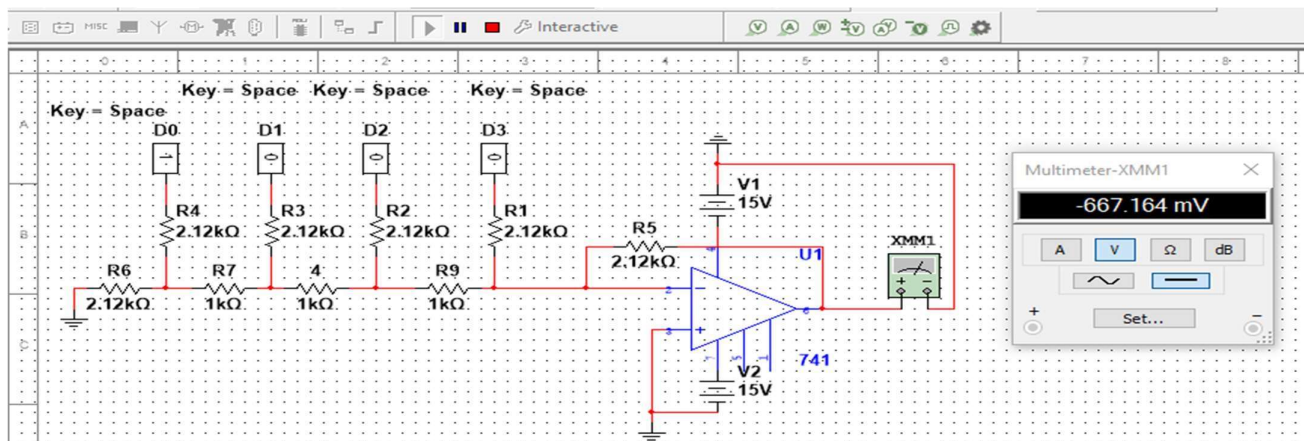
Fig 6: Simulation of R/2R Ladder DAC

Table 2: Truth table of simulation output for R/2R Ladder DAC

Digital Inputs				Analog Output
D_3	D_2	D_1	D_0	Voltage (V_{out})
0	0	0	0	0V
0	0	0	1	-1.50V
0	0	1	0	-2.55V
0	0	1	1	-2.66V
0	1	0	0	-3.72V
0	1	0	1	-4.20V
0	1	1	0	-5.24V
0	1	1	1	-12.40V
1	0	0	0	-12.39V
1	0	0	1	-12.38V
1	0	1	0	-12.39V
1	0	1	1	-12.39V
1	1	0	0	-12.39V
1	1	0	1	-12.39V
1	1	1	0	-12.39V
1	1	1	1	-12.38V

Discussion and Conclusion:

The main principle of this experiment was to familiar with Digital to Analog Converter. The basic theory was discussed about DAC. In the hardware implementation part, we faced difficulties to implement the R/2R Ladder DAC, the course teacher helped to make it clear. Anyway, all kind of DAC were behaved perfect during simulation period and the overall outcome was excellent.

Reference:

1. Thomas L. Floyd, *Digital Fundamentals*, 9th Edition, 2006, Prentice Hall