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DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
DIGITAL LOGIC AND CIRCUITS LABORATORY
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LAB REPORT ON

Construction Logic Gates using various MOS transistors.

Supervised By

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Introduction:

In this experiment, we'll learn how to build fundamental digital logic gates using MOSFETs, diodes, and resistors. Discover the essential role of MOSFETs in harnessing the output voltage of general-purpose logic ICs (4 to 5V) and ensuring their proper operation. Through practical examples, we'll construct Diode-Resistor Logic (DRL) AND gates and Diode-Transistor Logic (DTL) NAND gates, unraveling the intricacies of simple digital logic gate design.

Part I: Construction of MOSFET Logic Gates:

MOSFET:

MOSFET's operate the same as JFET's but have a gate terminal that is electrically isolated from the conductive channel. As well as the Junction Field Effect Transistor (JFET), there is another type of Field Effect Transistor available whose Gate input is electrically insulated from the main current carrying channel. The MOSFET is a type of semiconductor device called an Insulated Gate Field Effect Transistor. The most common type of insulated gate FET which is used in many different types of electronic circuits is called the Metal Oxide Semiconductor Field Effect Transistor or MOSFET for short.

CMOS:

The term CMOS stands for "Complementary Metal Oxide Semiconductor". This is one of the most popular technologies in the computer chip design industry and it is broadly used today to form integrated circuits in numerous and varied applications. Today's computer memories, CPUs, and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices. One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application-specific integrated circuits (ASICs).

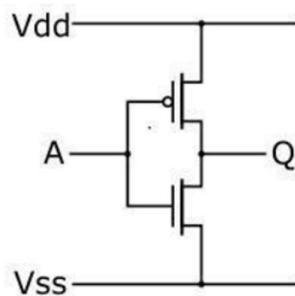


Figure 1: CMOS Inverter

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS

logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

Some advantages of CMOS over TTL are:

- CMOS gate inputs draw far less current than TTL inputs, because MOSFETs are voltage-controlled, not current-controlled, devices.
- CMOS gates can operate on a much wider range of power supply voltages than TTL: typically, 3 to 15 volts versus 4.75 to 5.25 volts for TTL.
- CMOS transistors are smaller in size and provide less power dissipation than NMOS transistors.

In this experiment, we first designed some logic circuit designs using NMOS. Then, we implemented the same logic circuits using CMOS and tried to identify potential design advantages of CMOS over NMOS.

Theory and Methodology:

NMOS Inverter with Ohmic/ Resistive Load:

Considering an ideal scenario, when a HIGH (+5V) is applied to the input, the NMOS transistor turns ON and current flows from Vdd to ground; thus, output voltage, $V_o = 0V$. Similarly, if a LOW (0V) is applied to the input, the NMOS remains in its OFF state. As a result, the current from Vdd has no path to ground. The output voltage is +5V.

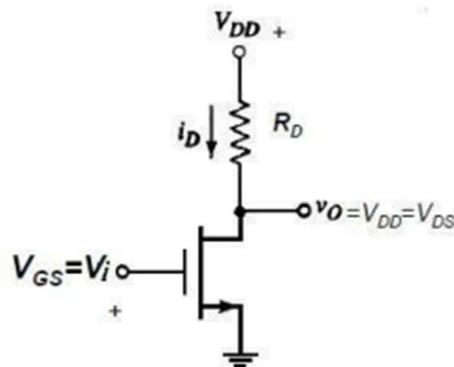


Figure 2: NMOS Inverter with Ohmic/Resistive Load

NMOS Inverter with NMOS Enhancement Transistor Load:

One disadvantage of designing NMOS logic circuits with ohmic load is that even when the NMOS is OFF, there is static power dissipation due to the resistor. A better design is to use an enhancement-type NMOS as load. They are “normally-off” devices and it takes an applied voltage between gate and drain of the correct polarity to bias them on. Thus, static power consumption is avoided.

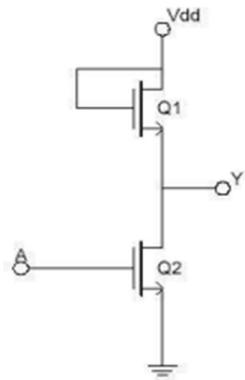


Figure 3: NMOS Inverter with NMOS Load

NMOS NAND Gate:

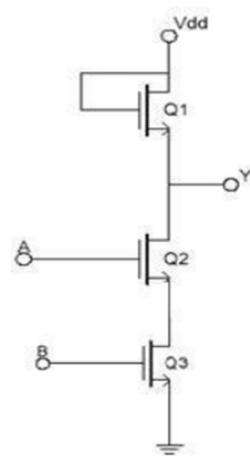


Figure 4: NMOS NAND Gate

NMOS NOR Gate:

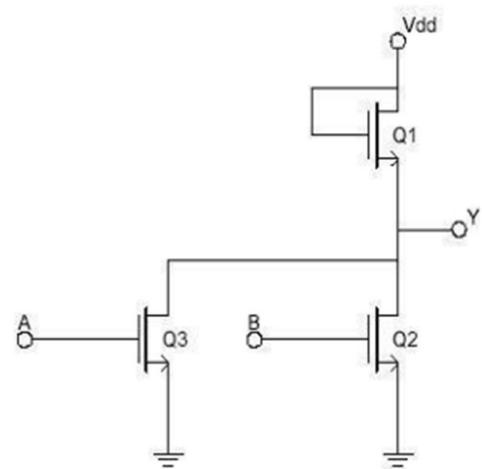


Figure 5: NMOS NOR Gate

CMOS Logic:

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor. In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (V_{ss} or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named V_{dd}).

CMOS Inverter:

The inverter circuit as shown in the figure below. It consists of PMOS and NMOSFET. Input A serves as the gate voltage for both transistors. The NMOS transistor has input from V_{ss} (ground) and the PMOS transistor has input from V_{dd} . The terminal Y is output. When a high voltage ($\sim V_{dd}$) is given at input terminal (A) of the inverter, the PMOS becomes an open circuit, and NMOS switched OFF so the output will be pulled down to V_{ss} .

When a low-level voltage ($<V_{dd}$, $\sim 0v$) applied to the inverter, the NMOS switched OFF and PMOS switched ON. So, the output becomes V_{dd} or the circuit is pulled up to V_{dd} .

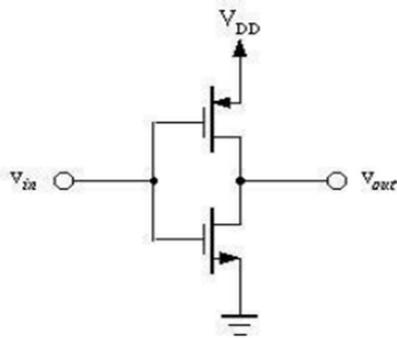


Figure 6: CMOS Inverter

CMOS NAND Gate:

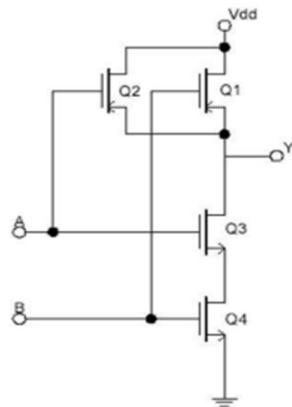


Figure 7: CMOS NAND Gate

CMOS NOR Gate:

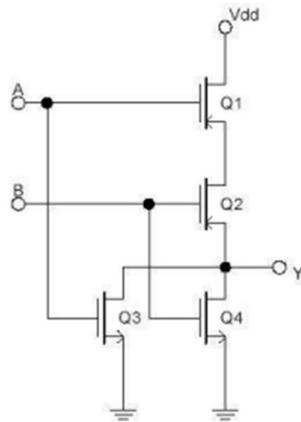
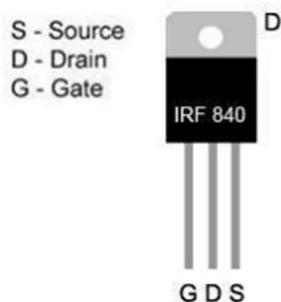


Figure 8: CMOS NOR Gate

MOSFET pin configuration:



Part II: Designing a Half Adder using CMOS:

Adder:

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations. Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or one's complement is being used to represent negative numbers; it is trivial to modify an adder into an adder-subtractor. Other signed number representations require a more complex adder.

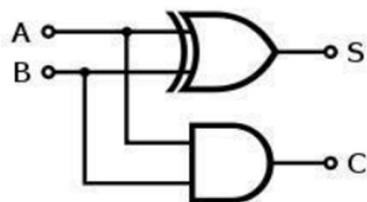


Figure 9: Half adder logic diagram

The half adder adds two single binary digits A and B. It has two outputs, sum (S) and carry (C). The carry signal represents an overflow into the next digit of a multi-digit addition. The value of the sum is $2C+S$. The simplest half-adder design, pictured above, incorporates an XOR gate for S and an AND gate for C. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder. The half-adder adds two input bits and generate carry and sum which are the two outputs of half-adder. The input variables of a Half adder are called the Augend and addend bits. The output variables are the Sum and Carry.

The Truth table and equations for the Half adder are:

$$S = A \oplus B$$

$$C = AB$$

Table 1: Half adder

A	B	A+B	S	C
0	0	0	0	0
0	1	1	1	0
1	0	1	1	0
1	1	2	0	1

Theory and Methodology:

To design any logic circuit first the truth table is needed to be established using different combinations of logic '0' and '1' to get the desired output. After that the gate level design is found from which transistor level design is done using desired transistors. Here CMOS is used for the transistor level design of the Half Adder. The whole process is given step wise below:

Half Adder:

Gate Level Design:

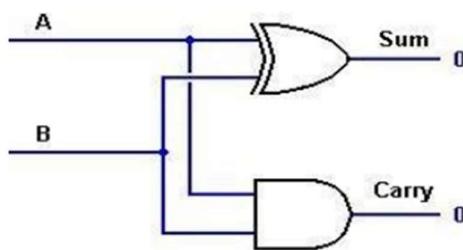


Figure 10 : Logic diagram of a Half Adder.

$$\begin{aligned} \text{Equation of Sum} &= A \text{ (XOR) } B \\ &= A\bar{B} + \bar{A}B \end{aligned}$$

$$\begin{aligned} \text{This equation can be rewritten as} &= \overline{\overline{A}\bar{B}} + \overline{\overline{A}B} \\ &= \overline{AB} + \overline{\overline{A}\bar{B}} \end{aligned}$$

$$\text{Equation of Carry} = AB$$

Apparatus:

- 1) MOSFET (PMOS, NMOS)
- 2) Connecting wires.
- 3) Trainer Board.

Precautions:

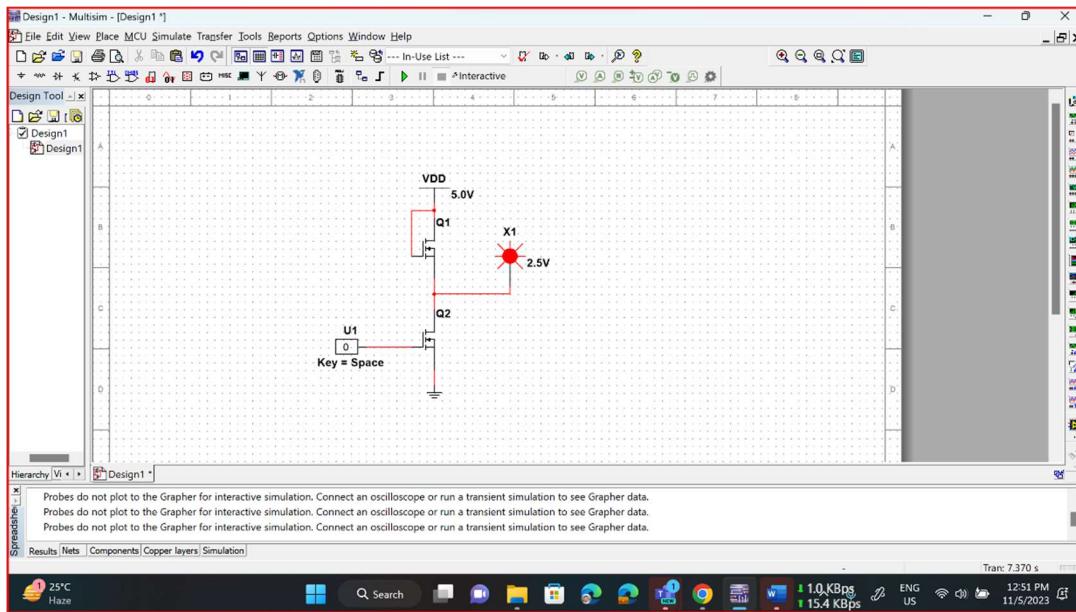
We checked all connections after setting up the circuit and make sure that applied only enough voltage(within VDD) to turn on the transistors and/or chip, otherwise it may get damaged.

Experimental Procedure:

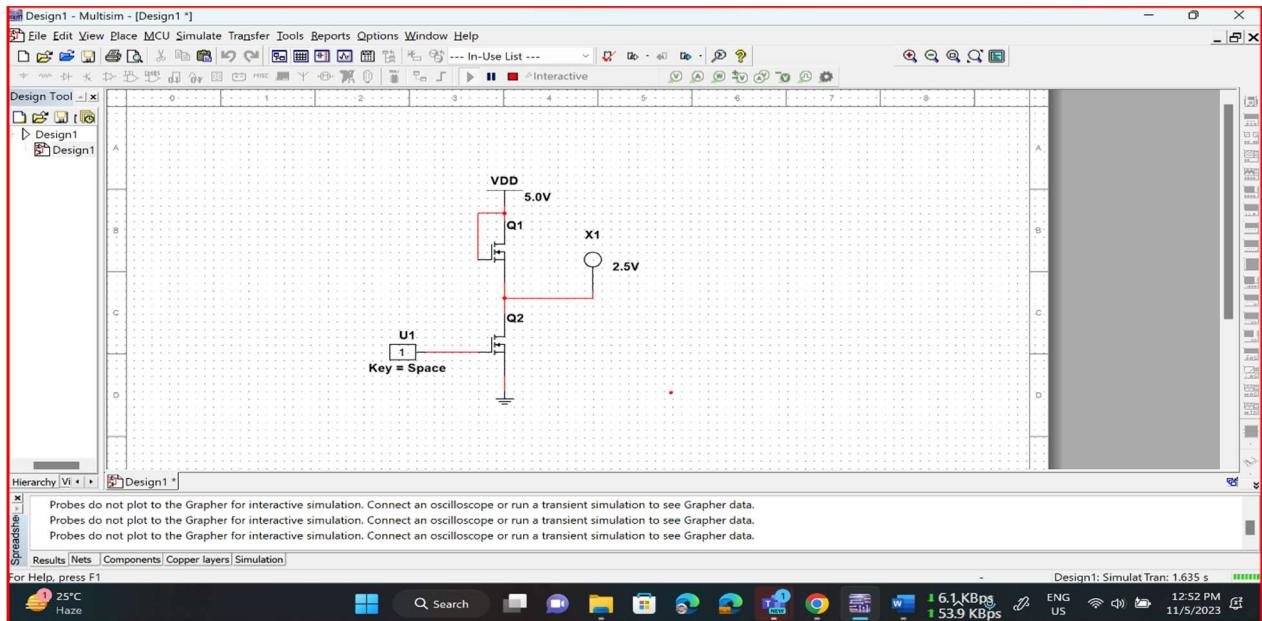
1. AT first, we constructed the circuit for NMOS INVERTER as shown in the Figure.
2. For each input combination, we find the outputs and put them in a truth table. We have two sets of outputs in the truth table - a standard and an experimental one.
3. We constructed each circuit set-up from the given figure.

Simulation and Measurement:

NMOS Inverter with NMOS Load:



NMOS Inverter with NMOS Load

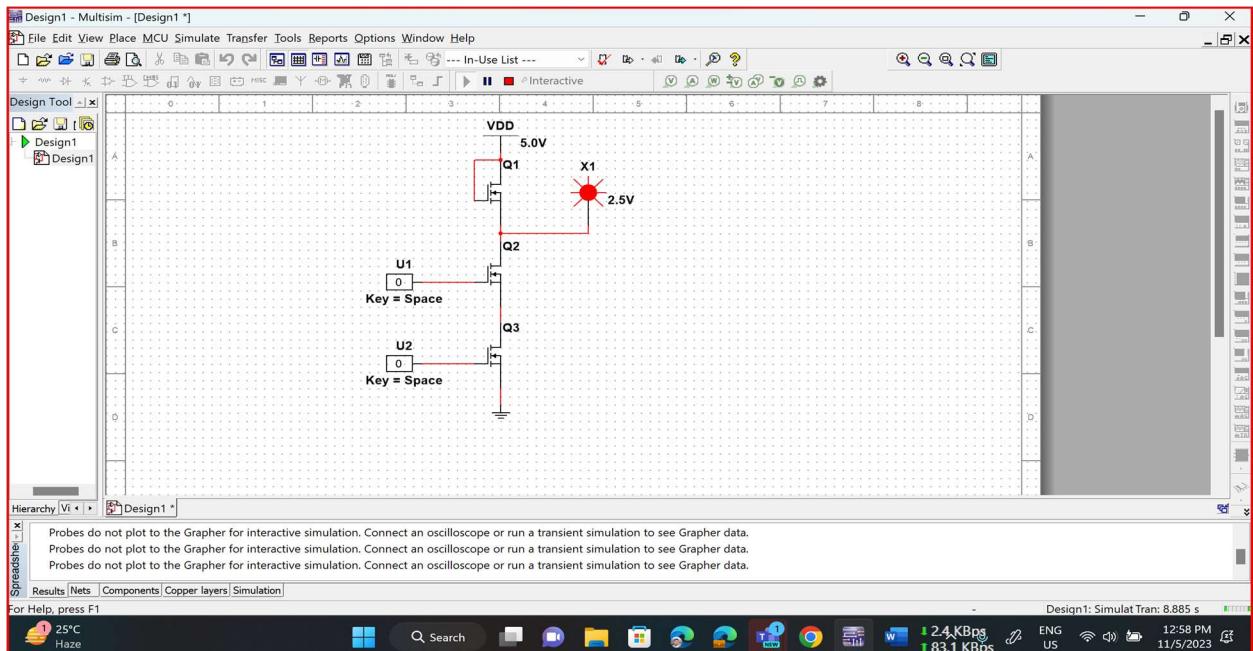


NMOS Inverter with NMOS Load

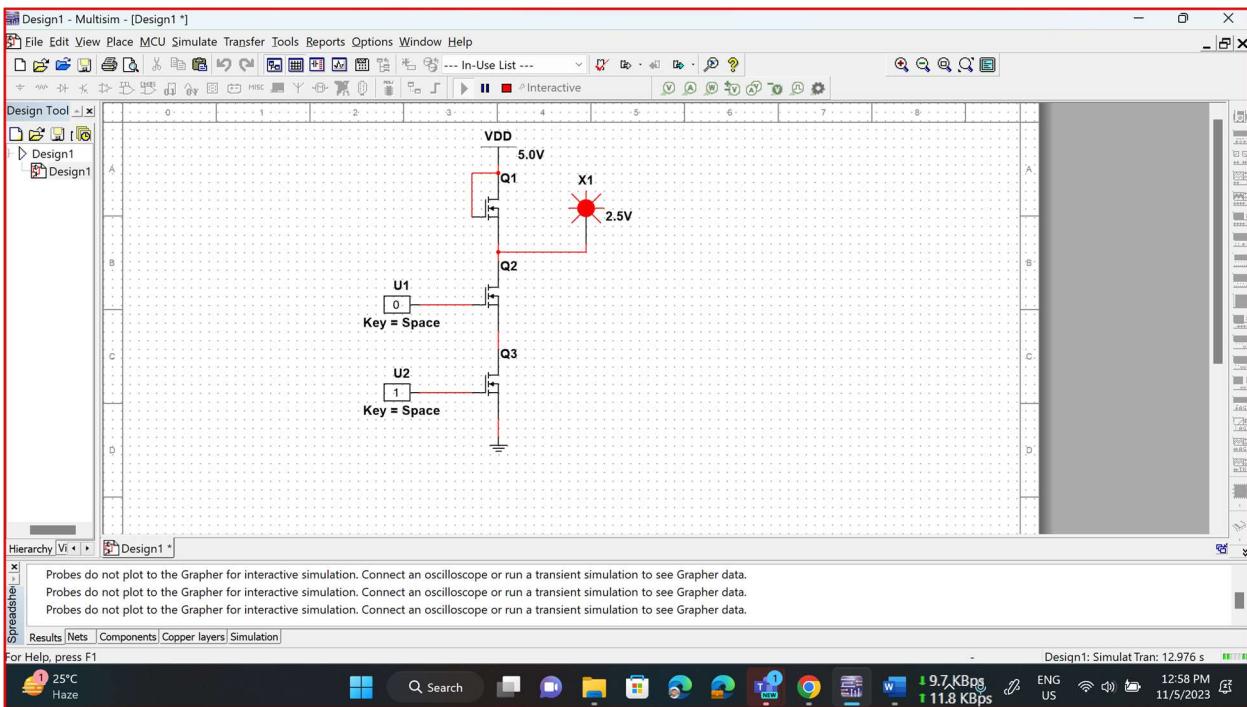
Truth table of NMOS INVERTER GATE:

Input	Output
0	1
1	0

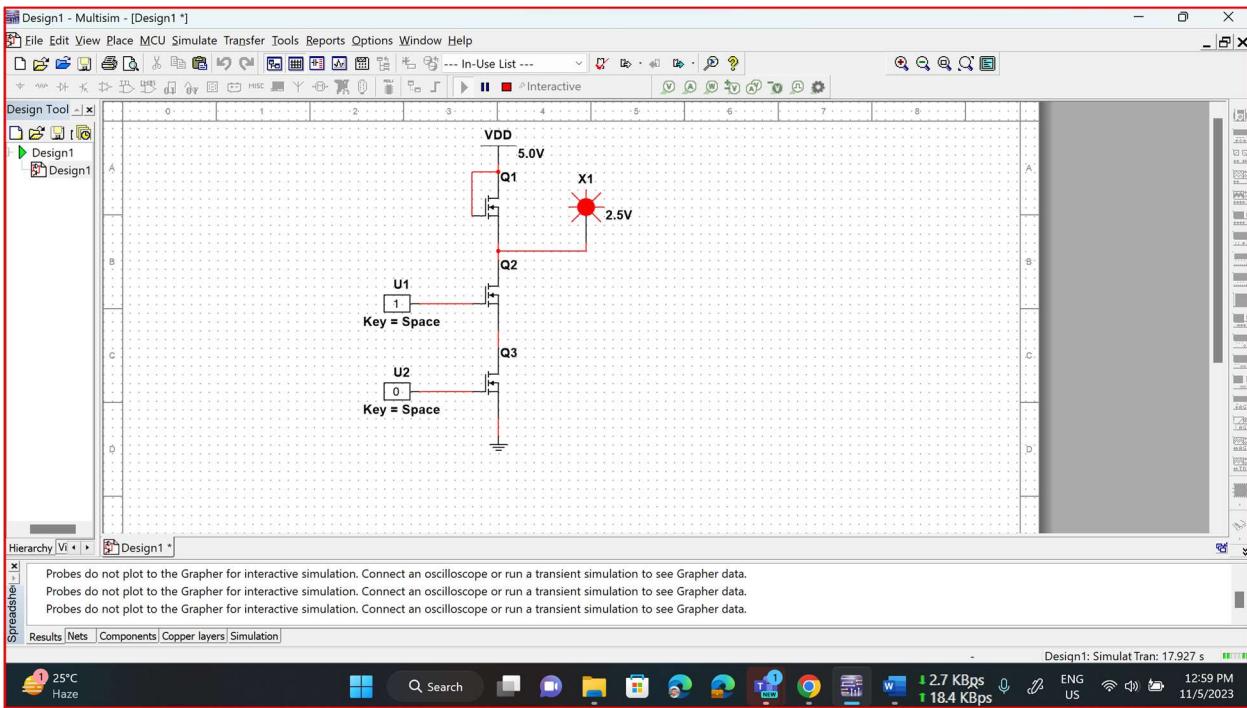
NMOS NAND Gate:



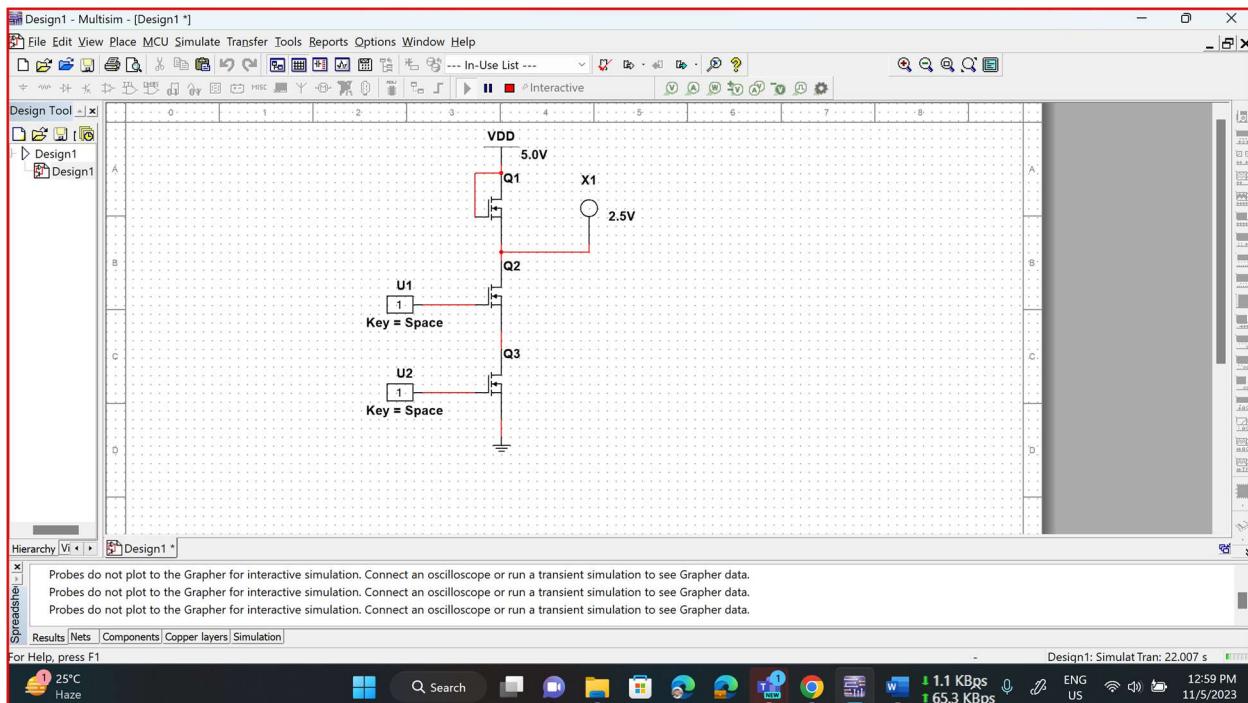
NMOS NAND Gate



NMOS NAND Gate



NMOS NAND Gate

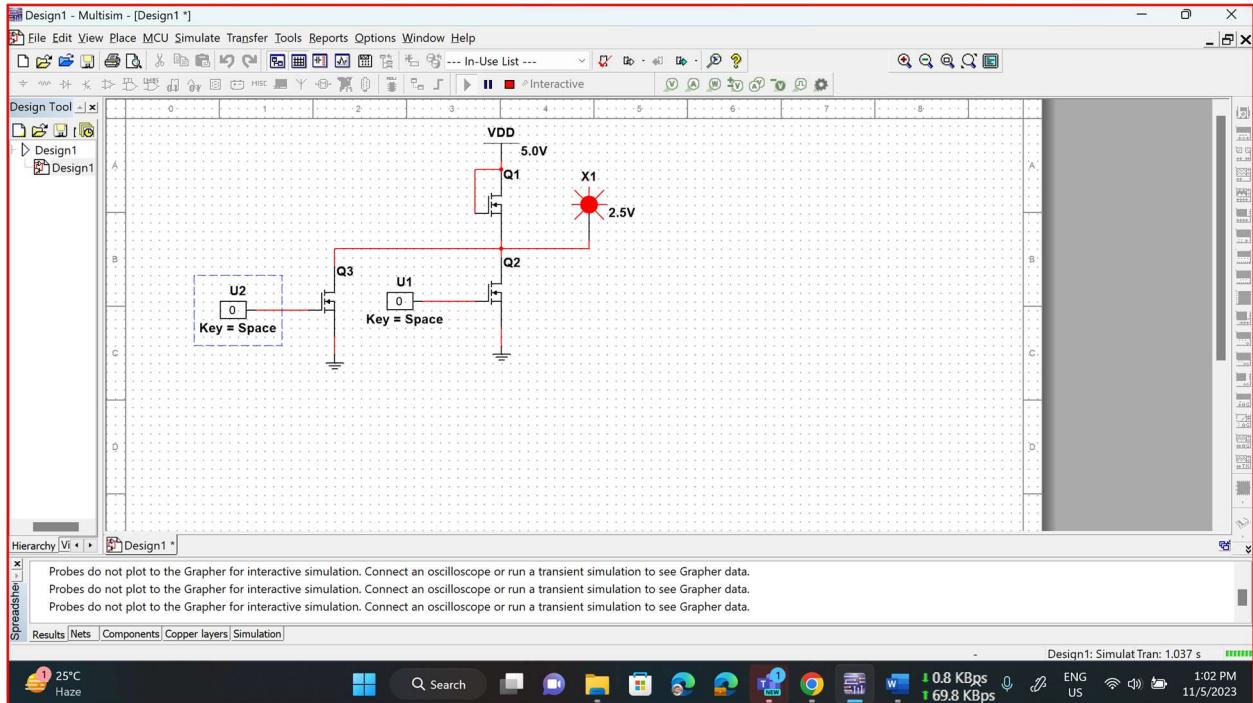


NMOS NAND Gate

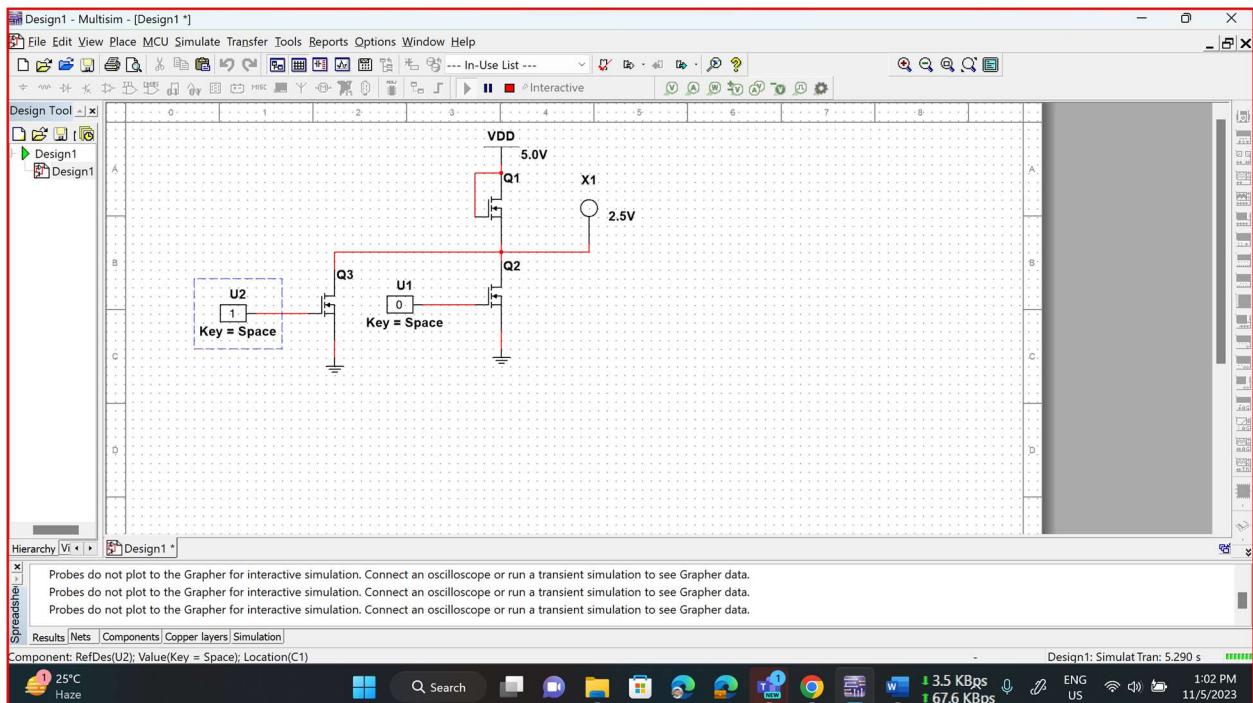
Truth table of NMOS NAND GATE:

Input		Output
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

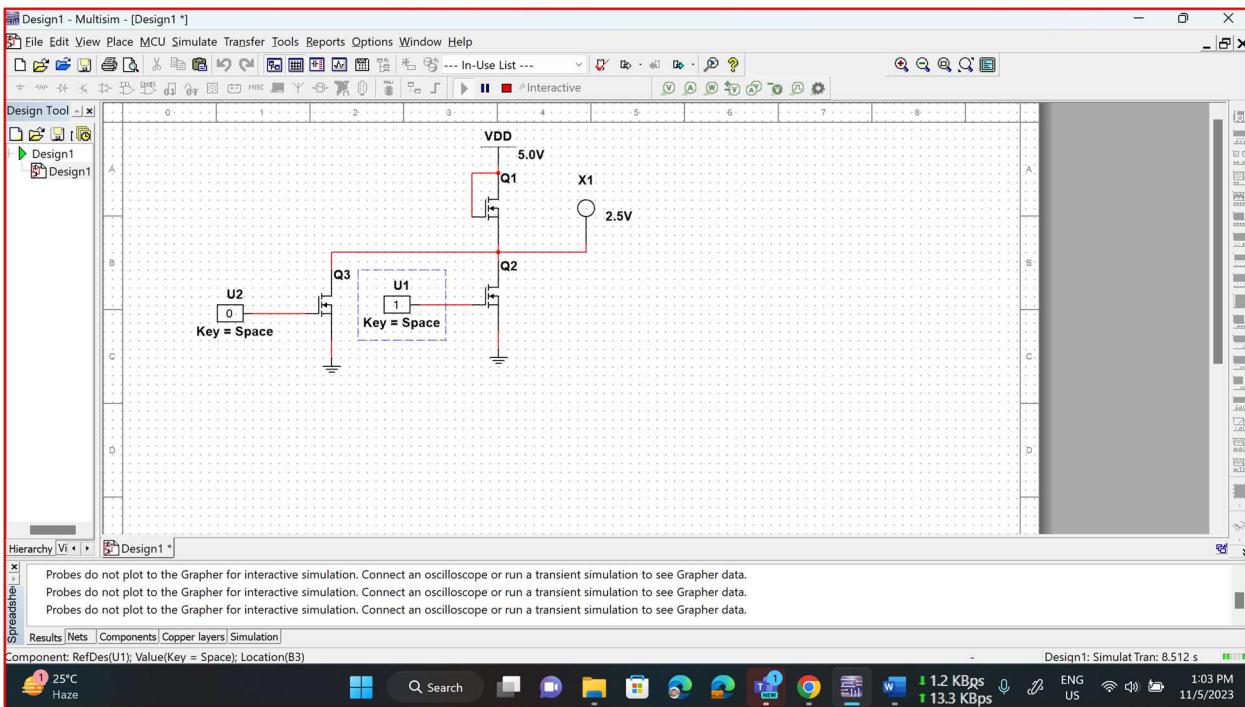
NMOS NOR Gate:



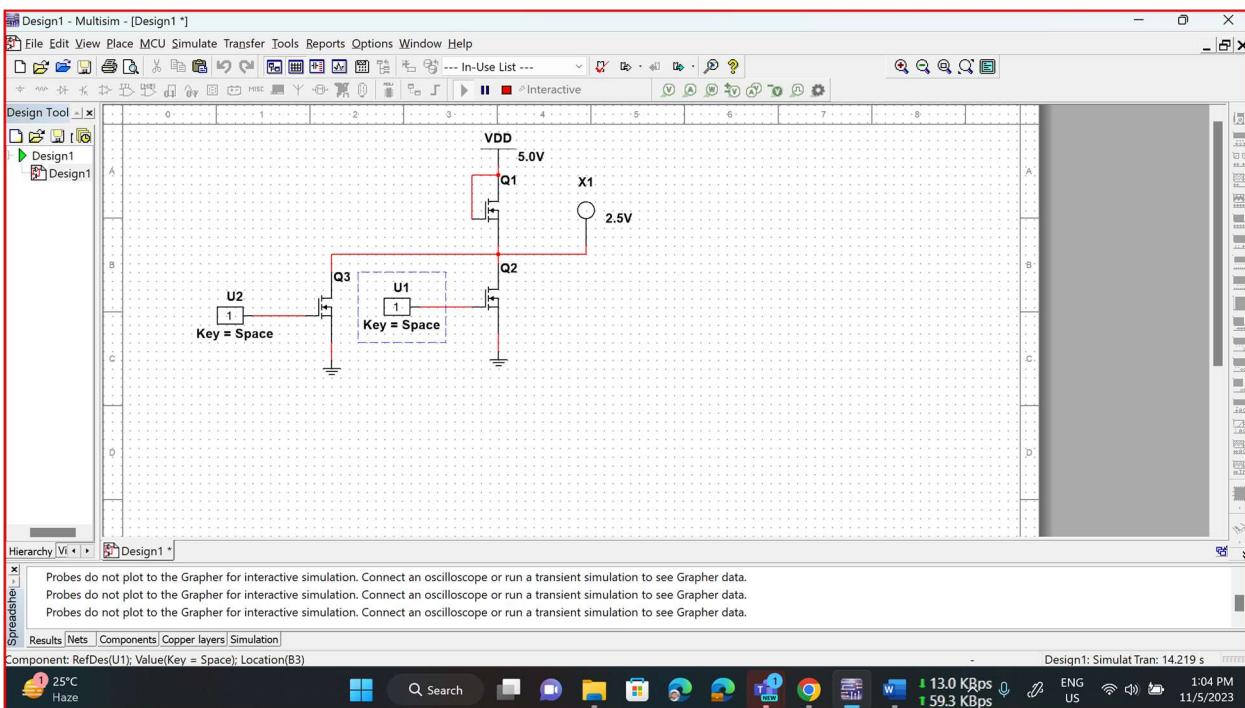
NMOS NOR Gate



NMOS NOR Gate



NMOS NOR Gate

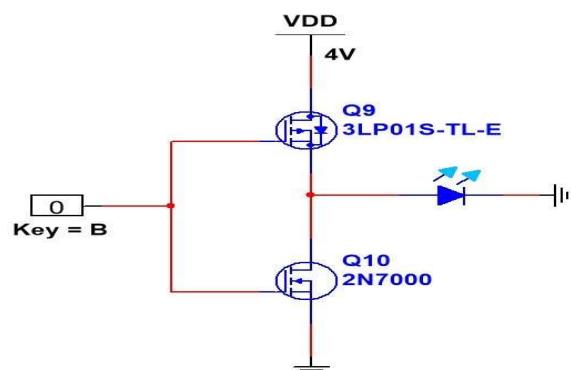


NMOS NOR Gate

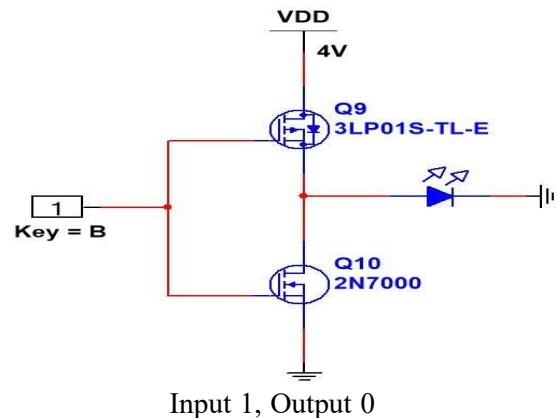
Truth table of NMOS NOR GATE:

Input		Output
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

CMOS INVERTER:



Input 0, Output 1

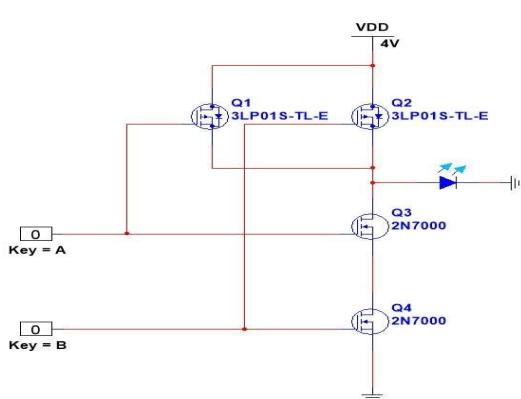


Input 1, Output 0

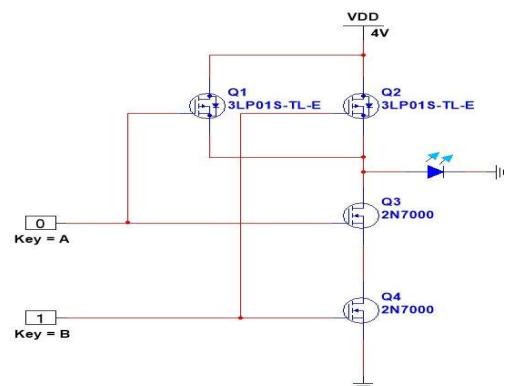
Truth table of CMOS INVERTER:

Input	Output
0	1
1	0

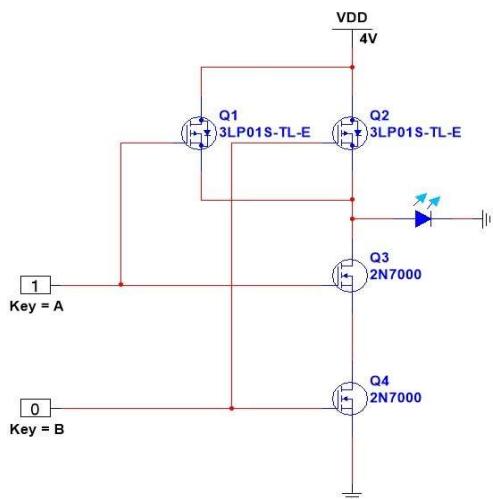
CMOS NAND GATE:



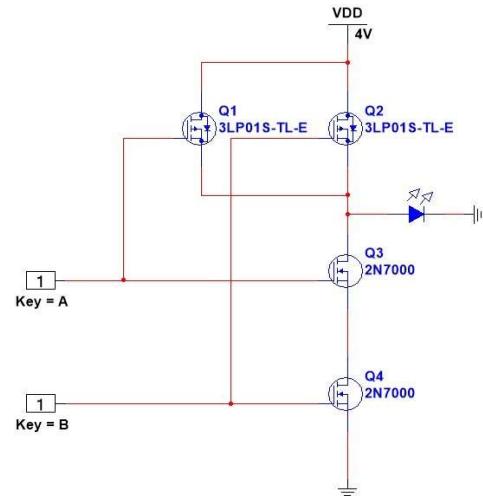
Input A=0, B=0, Output 1



Input A=0, B=1, Output 1



Input A=1, B=0, Output 1

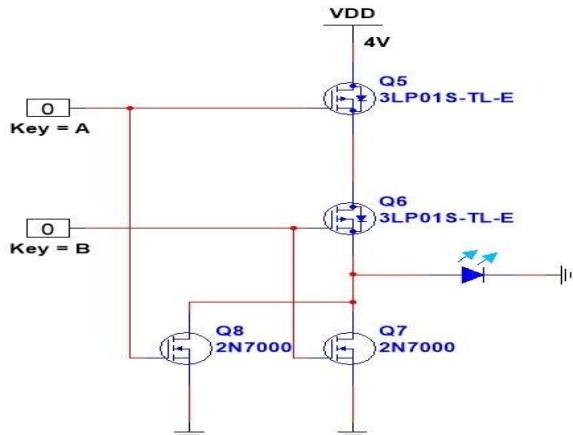


Input A=1, B=1, Output 0

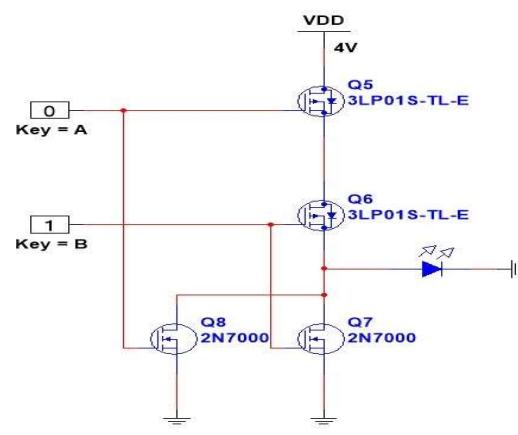
Truth table of CMOS NAND GATE:

Input		Output
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

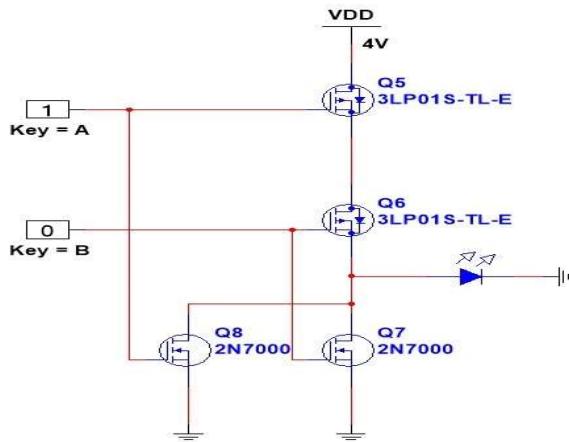
CMOS NOR GATE:



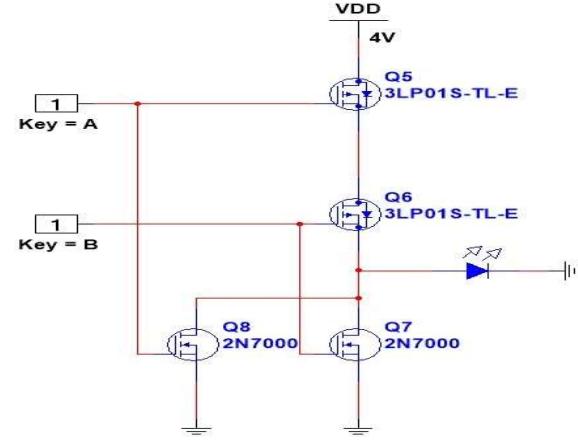
Input A=0, B=0, Output 1



Input A=0, B=1, Output 0



Input A=1, B=0, Output 0

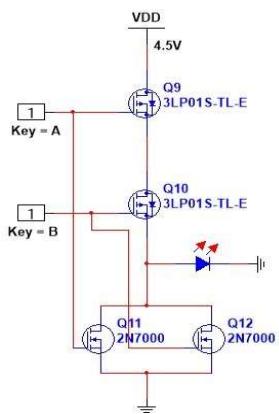


Input A=1, B=1, Output 0

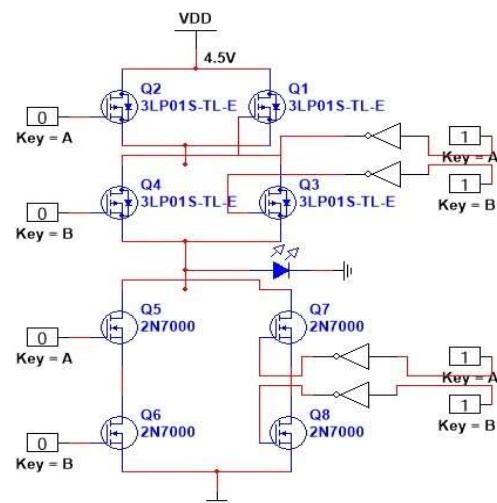
Truth table of CMOS NOR GATE:

Input		Output
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

HALF ADDER USING CMOS:



Carry with A=1, B=1, Output=1



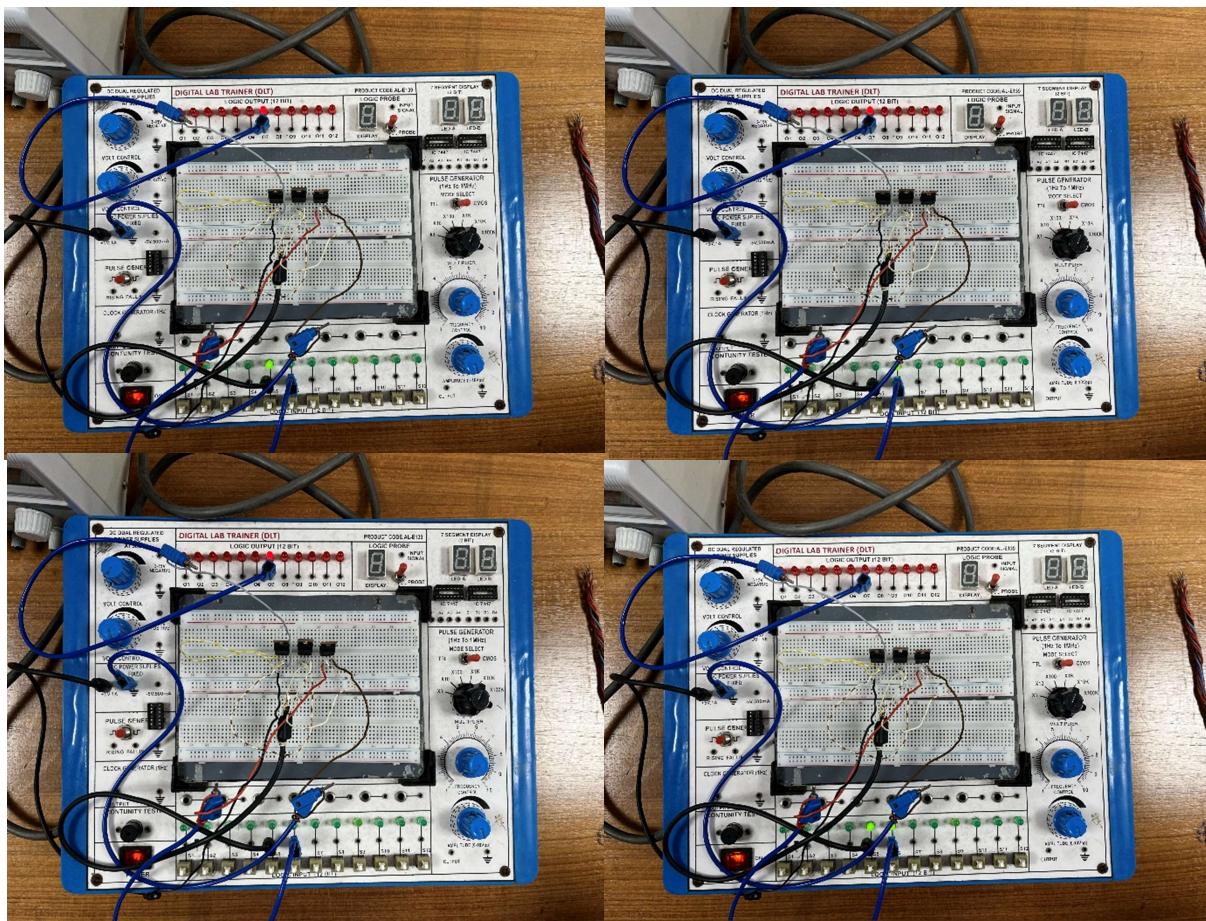
Sum with Input A=0, B=0, Output=0

Truth table of CMOS HALF ADDER:

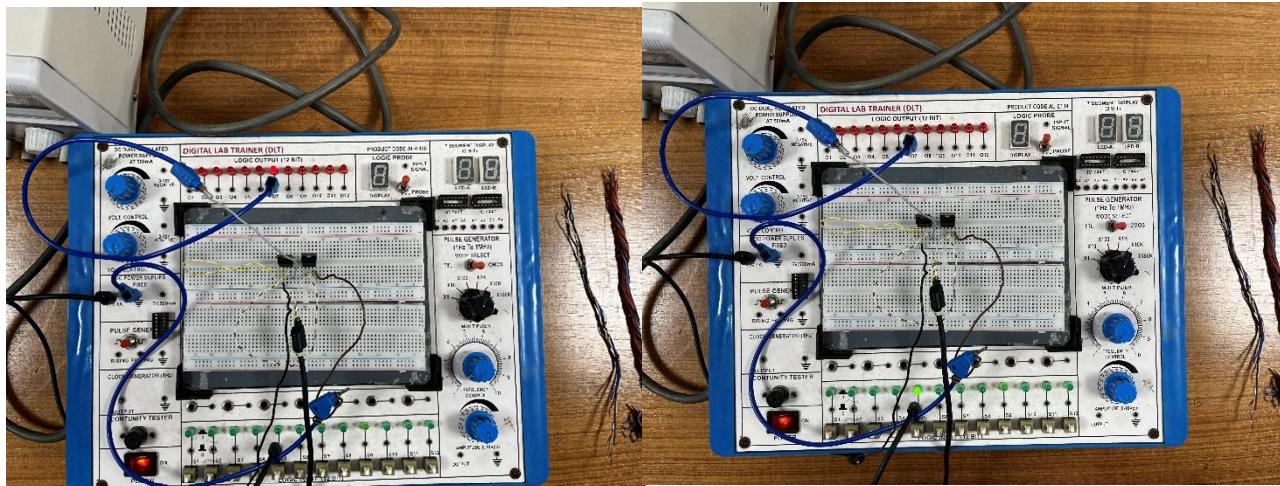
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Experimental Circuit Diagram:

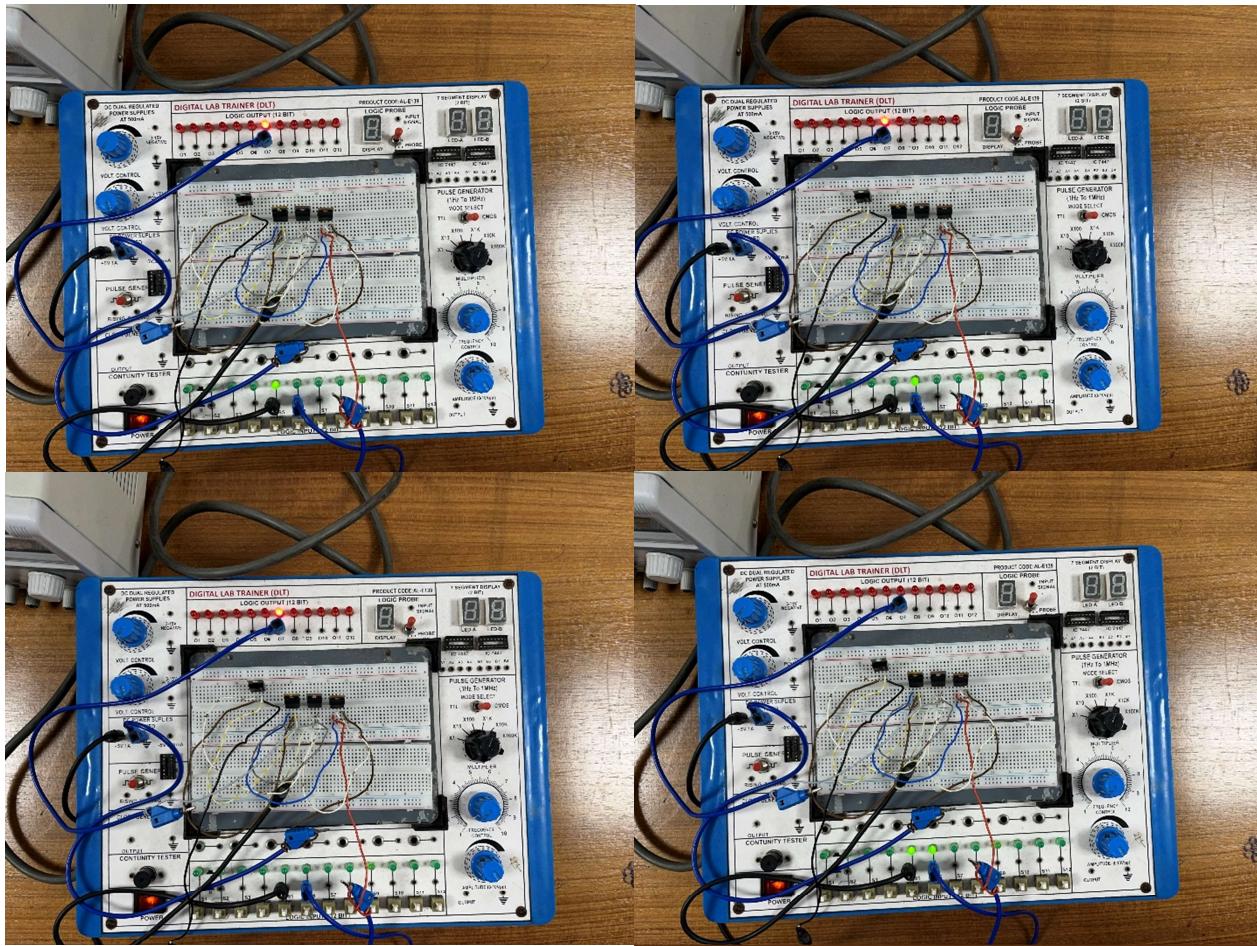
NMOS NAND:



CMOS INVERTER:



CMOS NAND:



Results & Discussion:

In this experiment, we designed and constructed various MOSFET-based logic gates, including NMOS NOR, CMOS NAND, CMOS Inverter, and CMOS NOR gate using PMOS and NMOS transistors. These gates are sensitive to high voltage, and during the experiment, we encountered a heating issue and initial errors. However, we successfully addressed and resolved these challenges. We performed simulations using Multisim software and found that the simulated and experimental outcomes matched, which confirmed the accuracy of our findings. The successful verification through simulations further validates the reliability and functionality of our constructed circuits. This experiment highlights the practical application of MOSFETs in logic gate design and underscores the importance of simulation tools in validating real-world experiments.

Reference:

1. Thomas L. Floyd, *Digital Fundamentals*, 9th Edition, 2006, Prentice Hall.
2. Link: <http://www.techpowerup.com/articles/overclocking/voltmods/21>

Questions and Answers:

Qs1. For each of the above set-ups, describe in words what the data means. Did your results match the expected ideal outputs? If not, explain why?

1. **Ans:** For inverter setup the output truth table interprets that if inputs HIGH, output will be low and if input low, output will be high.

The NAND gate has an output that is normally at logic high and only goes to logic low when all of its inputs are at logic high.

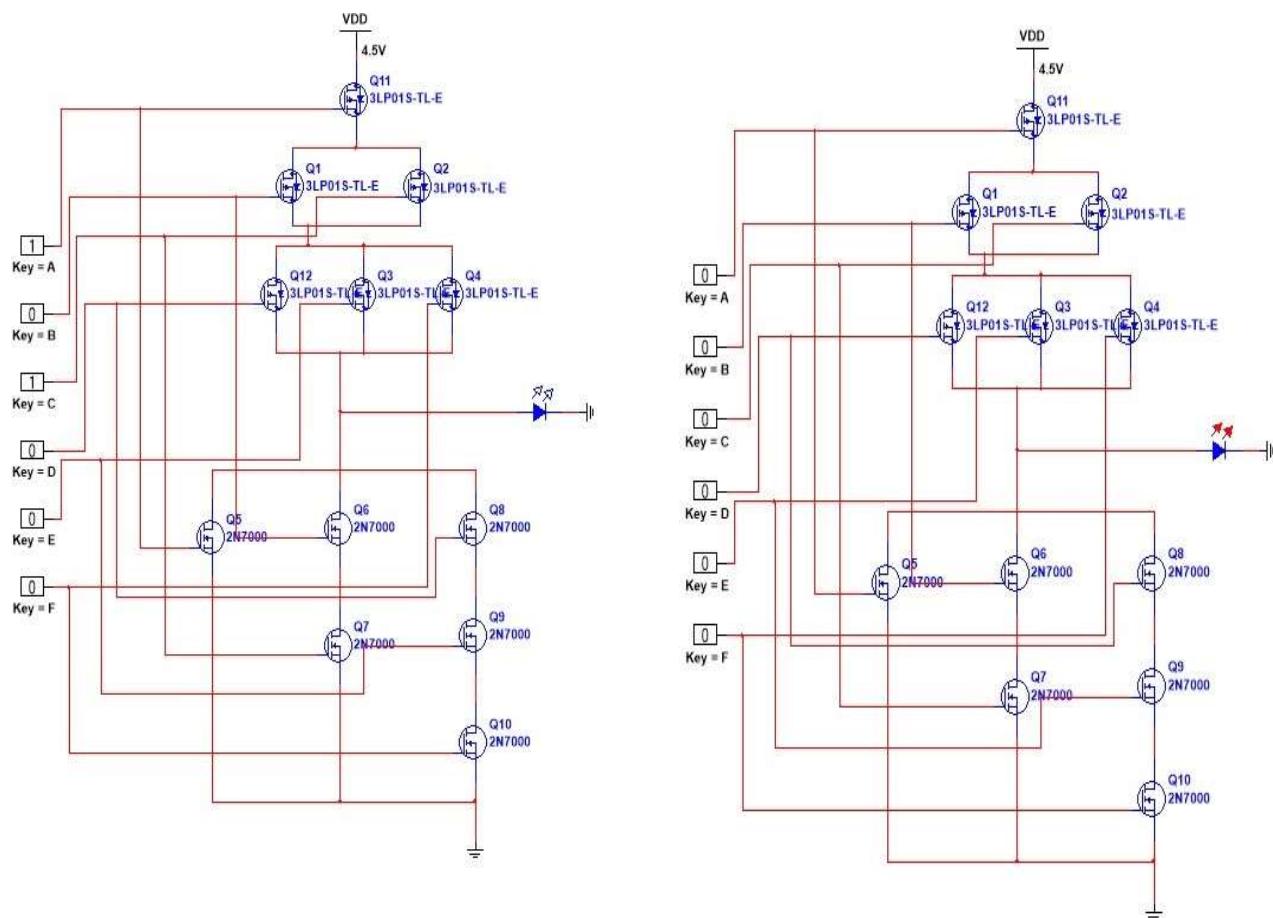
For NOR Gate, A HIGH output (1) results if both the inputs to the gate are LOW (0); if one or both input is HIGH (1), a LOW output (0) results. NOR is the result of the negation of the OR operator.

Yes, the truth table clearly shows us that the results matched with the expected ideal outputs.

Qs2. Implement logic function $V_{out} = \overline{(A + BC + DEF)}$ using: (a) NMOS (b) CMOS

IMPLEMENTATION OF LOGIC FUNCTION:

Output= $\overline{(A + BC + DEF)}$ using CMOS,



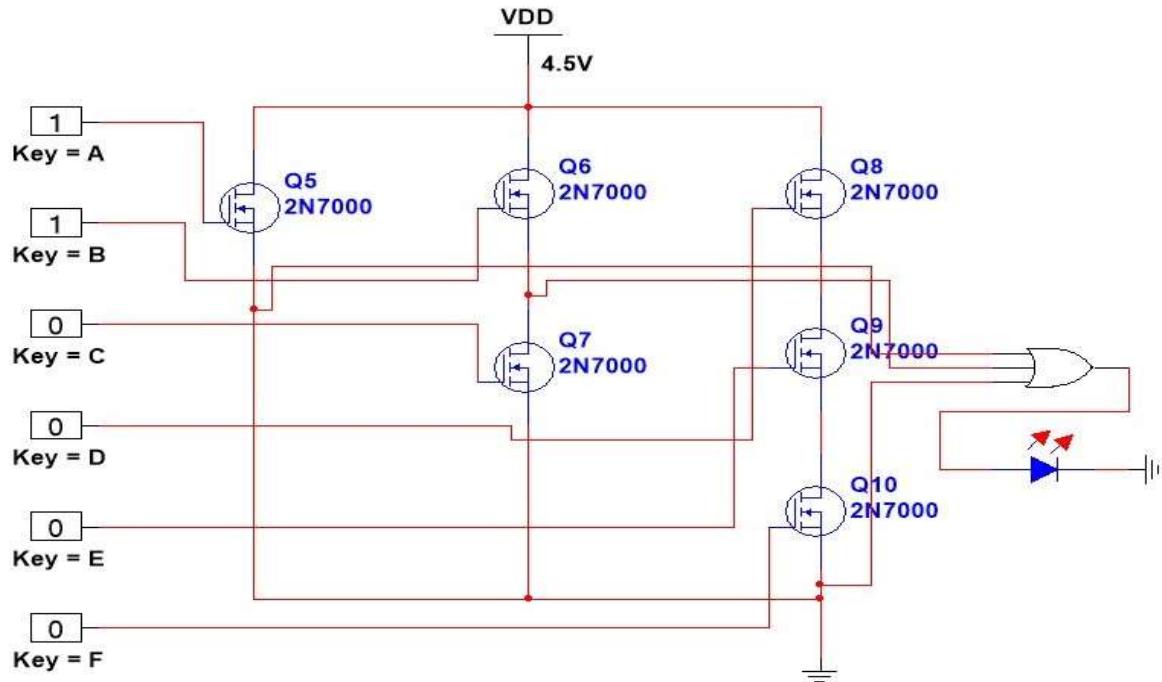
Input A=1, B=0, C= 1

D, E, F = 0,

Output= 0

Input A, B, C, D, E, F= 0,
Output= 1

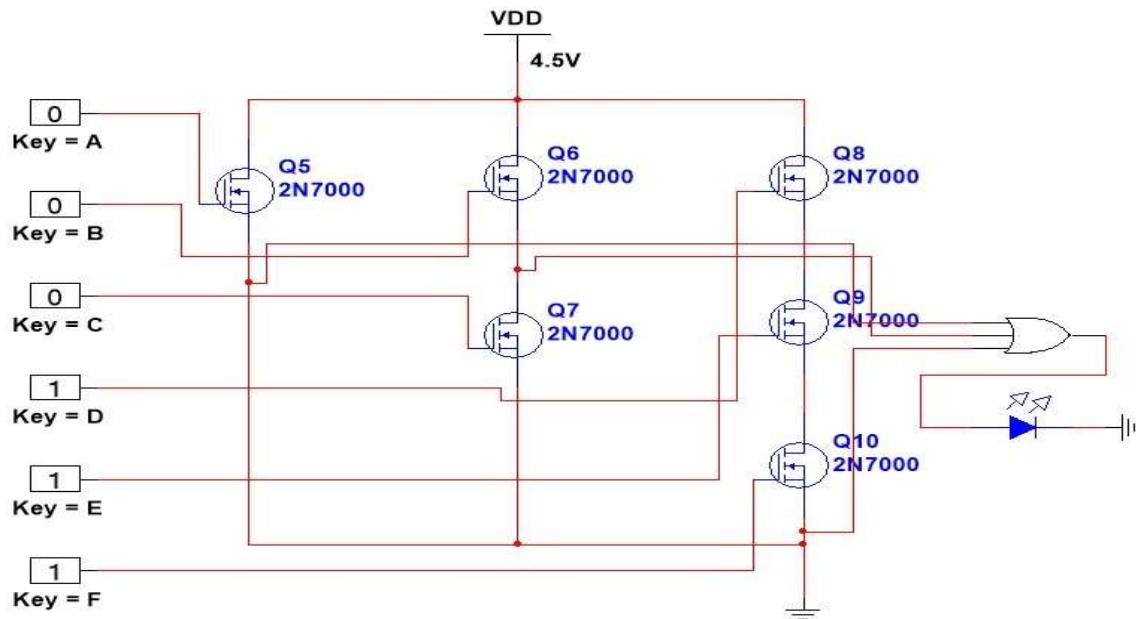
Output= $\overline{(A + BC + DEF)}$ using NMOS,



Input A=1, B=1,

C, D, E, F= 0,

Output= 1



Input A, B, C=0

D, E, F= 0

Output= 0