AMERICAN INTERNATIONAL UNIVERSITY–BANGLADESH (AIUB)

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

DIGITAL LOGIC AND CIRCUITS LABORATORY

FALL 2023-2024

Group: 02, Section: Q

LAB REPORT ON

Study of Different Flip-Flops.

Supervised By

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Date of Submission: 8th December, 2023

Introduction:

The basic building blocks of combinational logic circuits are gates. In particular, AND, OR, and NOT gates (however, there are also, XOR, NAND, NOR, XNOR gates too).
The basic building blocks of sequential logic circuits are flip flops. Flip flops are devices that use a clock. Each flip flop can store one bit. There are different types of flip-flops. D flip-flop, T flip-flop, J-K flip-flop etc.

Theory and Methodology:

Basically, a flip flop has two/three inputs. One input is a control input. For a D flip flop, the control input is labeled D. For a T flip flop, the control input is labelled T. For J-K flipflop the control inputs are J and K. The other input is the clock.

The clock input is usually drawn with a triangular input. These flip-flops are positive edge- triggered flip flops. This means that the flip flops can only change output values when the clock is at a positive edge. There are also negative edges triggered flip flops, which change on a negative edge. In this theory section, we consider only positive edge-triggered flip flops.

When the clock is not at a positive edge, then the output value is held. That is, it does not change. A flip flop also has two outputs, **Q** and **Q'**. The output is really the bit that's stored. Thus, the flip flop is always outputting one bit of information.

But one might wonder "Doesn't it have two bits of information? **Q** and **Q'**?" If we have two bits, we have four possible values. However, **Q'** is the negation of **Q** which means you only have two possible outputs: **Q = 0, Q' = 1** or **Q = 1, Q' = 0**. Since the second output is always negated from the first, you don't get any additional storage. But what is the necessity of the negated output? The design of flip- flop gives **Q'** basically for free, so that's why flip flops have both the regular output and the negated output.

D Flip-Flop:

The Q output of a D flip-flop synchronously follows the state of its D input during a rising clock edge (or falling edge if the clock is active low). This property gives it the name "D flip-flop" as it effectively captures and delays the value of the D input by one clock cycle. Essentially, the D flip-flop can be seen as a fundamental building block for memory cells, behaving like a zero-order hold or delay line for data.

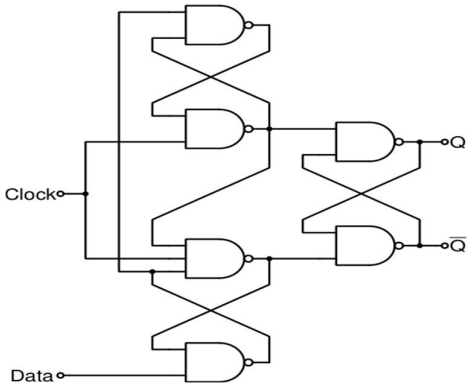


Figure 1: Logic circuit a positive edge triggered D flip-flop without preset and clear capability.

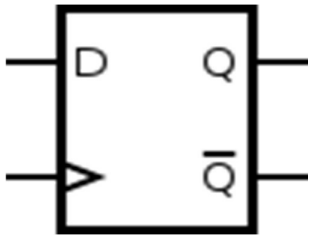


Figure 2: Graphical Symbol of a positive edge triggered D flip-flop without preset and clear capability.

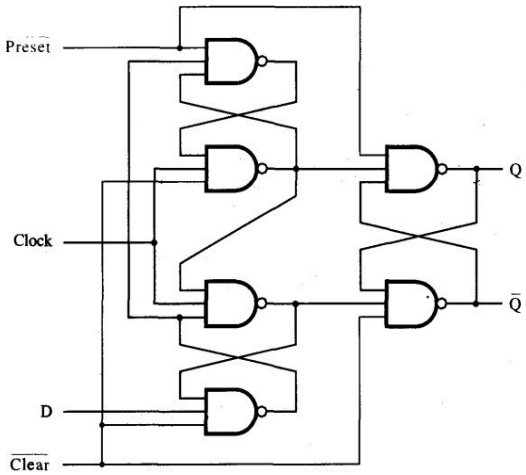


Figure 3: Logic circuit a positive edge triggered D flip-flop with preset (active low) and asynchronous clear (active low) capability.

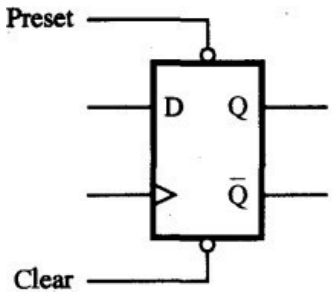


Figure 4: Graphical symbol of a positive edge triggered D flip-flop with preset (active low) and asynchronous clear (active low) capability.

J-K Flip Flop:

The J-K flip-flop can be understood as an extension of the gated S-R flip-flop, featuring an added clock input circuitry to prevent undesirable output states when both S and R inputs are set to logic level "1." This clocked input introduces four distinct input combinations for the J-K flip-flop: "logic 1," "logic 0," "no change," and "toggle." The symbol representing a J-K flip-flop is quite like that of an S-R bistable Latch.

We can show the characteristics of a J-K in the table given below.

Table 1:

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	~ Q(t)

J-K flip-flops can be designed easily using D flip-flops.

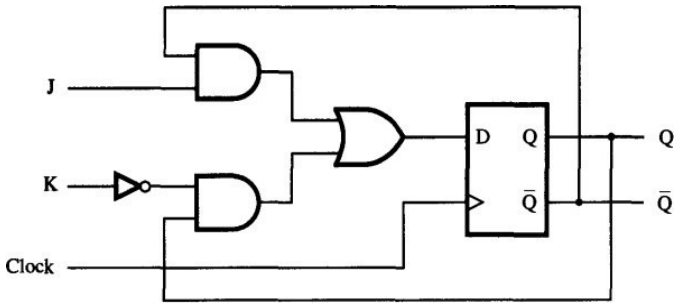


Figure 5: J-K flip-flop using D flip-flop.

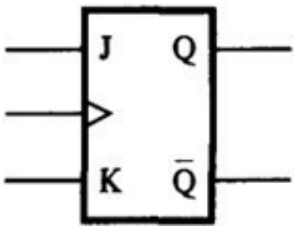


Figure 6: Graphical Symbol of J-K flip-flop.

T Flip-Flop:

The T flip-flop, also known as the toggle flip-flop, is a type of two-input flip-flop. It receives input from both the toggle (T) and clock (CLK) signals. When the toggle input is set to a HIGH state, the T flip-flop changes its current state (toggles) in response to the application of the clock signal. However, if the toggle input is set to a LOW state, the T flip-flop maintains its previous state without any changes. In summary, the T flip-flop behaves as a state-changing device when the toggle input is active, but it acts as a memory element when the toggle input is inactive.

A T flip-flop can be designed easily by making J and K short of a J-K flip flop.

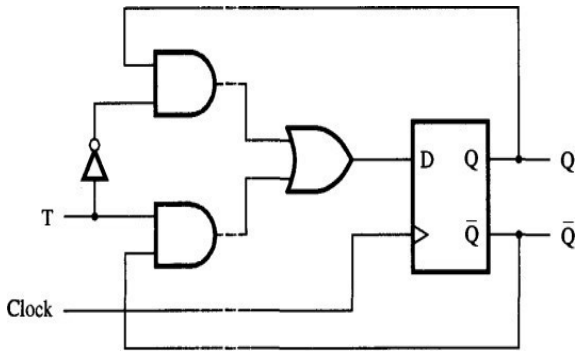


Figure 7: T flip-flop using D flip-flop.

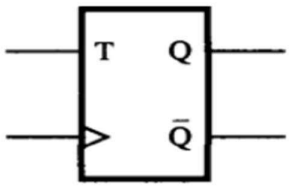


Figure 8: Graphical Symbol of T flip-flop.

There are built-in ICs for D flip-flop and J-K flip-flop. IC-7474 contains 2 D flip-flop. The pin configuration of IC-7474 is given below.

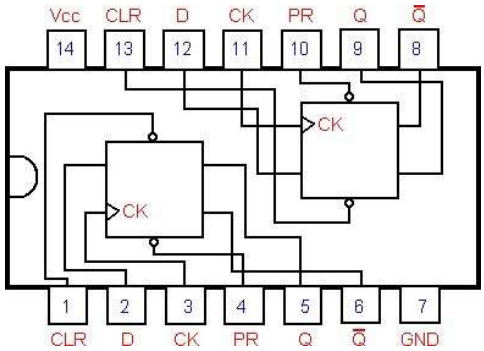


Figure 9: IC-7474

Apparatus:

IC: 7404 (NOT Gate), 1[pcs]

7408 (AND Gate), 2[pcs]

7432 (OR Gate), 1[pcs]

7400 (NAND Gate), 6[pcs]

7474 (D flip-flop), 1[pcs]

7476 (J-K flip-flop), 1[pcs]

Precaution:

We never make the ‘Preset’ and ‘Clear’ both active at a time. Otherwise, we may get erroneous results.

Experimental Procedure:

In this experiment, the circuits depicted in figures were implemented on the online simulator trainer board, and the input-output characteristics were observed. The clock was generated using a pulse switch. Timing diagrams were generated from the implemented circuits.

Simulation and Measurement:

J-K flip-flop design using D flip-flop:

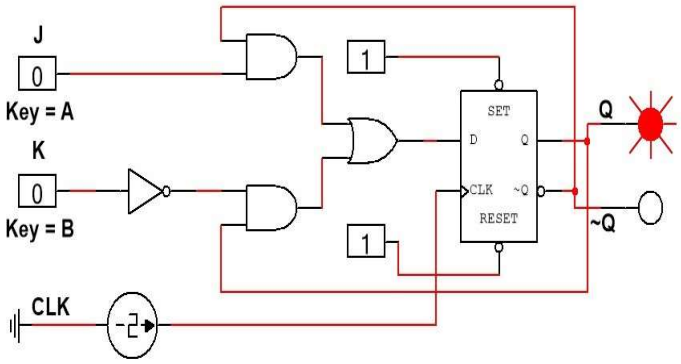


Figure 10: For Input J = 0, K= 0; Output Memory

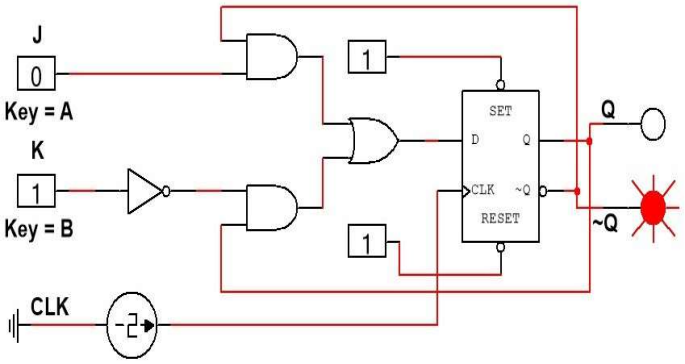


Figure 11: For Input J = 0, K= 1; Output is 0

Truth Table for J-K flip-flop

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	~ Q(t)

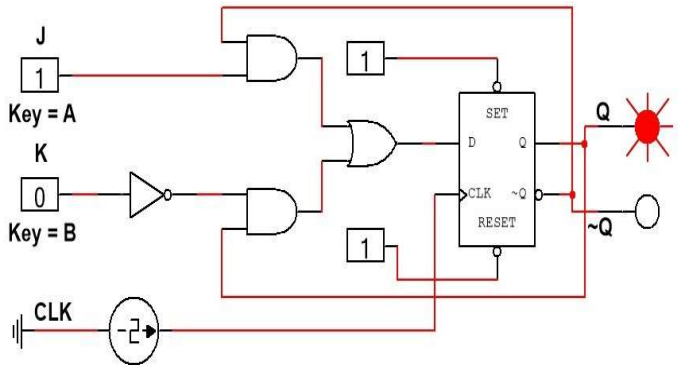


Figure 12: For Input J = 1, K= 0; Output is 1

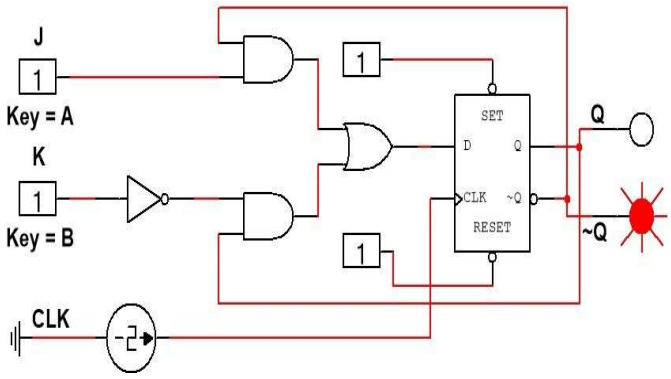


Figure 13: For Input J = 1, K= 1; Output Toggle

T flip-flop design using D flip flop:

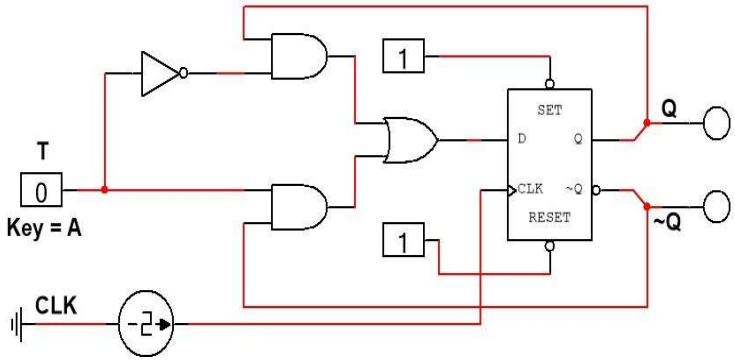


Figure 14: For Input T = 0, Q= 0; Output ~Q is 0

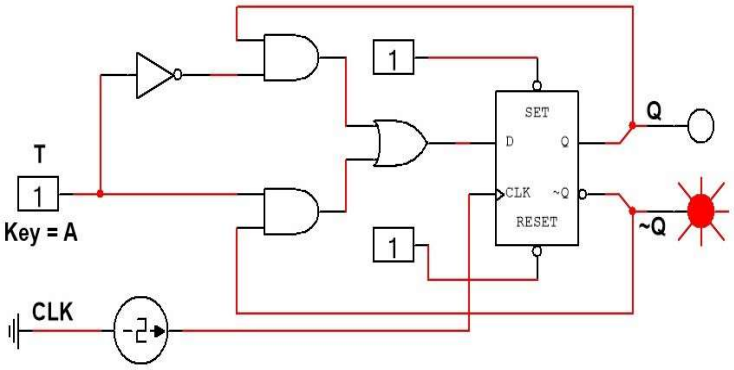


Figure 15: For Input T = 1, Q= 0; Output ~Q is 1

Truth Table for T flip-flop

T	Q	Q`
0	0	0
1	0	1
0	1	0
1	1	0

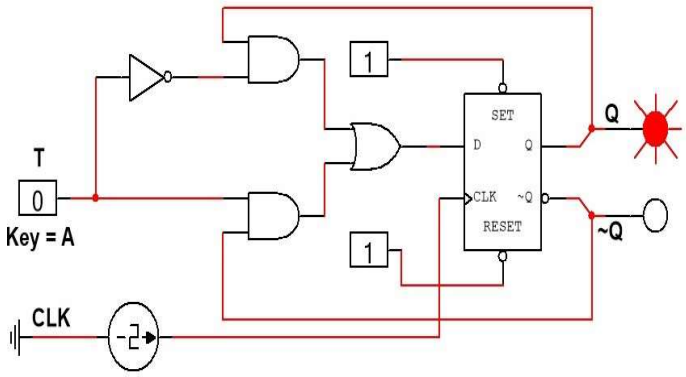


Figure 16: For Input T = 0, Q= 1; Output ~Q is 0

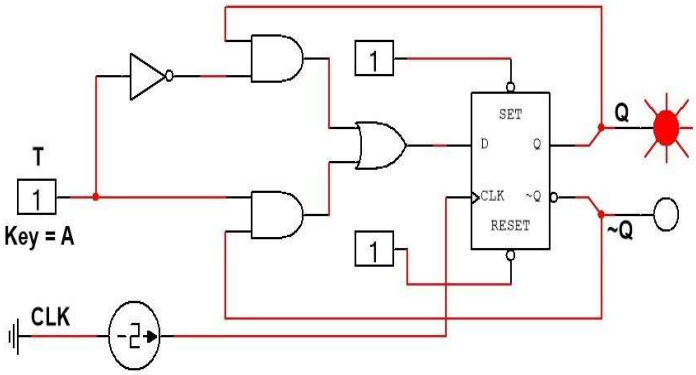


Figure 17: For Input T = 1, Q= 1; Output ~Q is 0

D flip-flop design without PRESET and CLEAR:

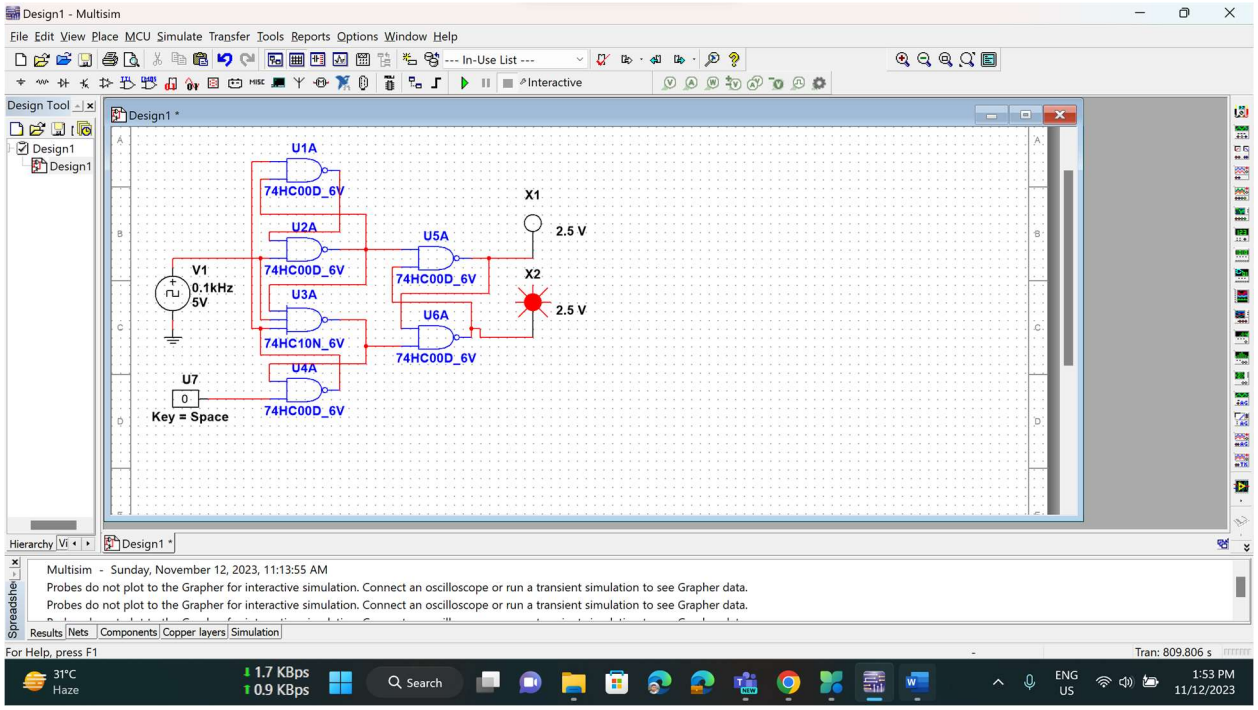


Figure-18: Simulation for logic circuit of a positive edge triggered D flip-flop without preset and clear capability.

Truth Table for D flip-flop:

Input D_n	Output Q_{n+1}
0	0
1	1

D flip-flop design with PRESET(active low) and CLEAR(active low):

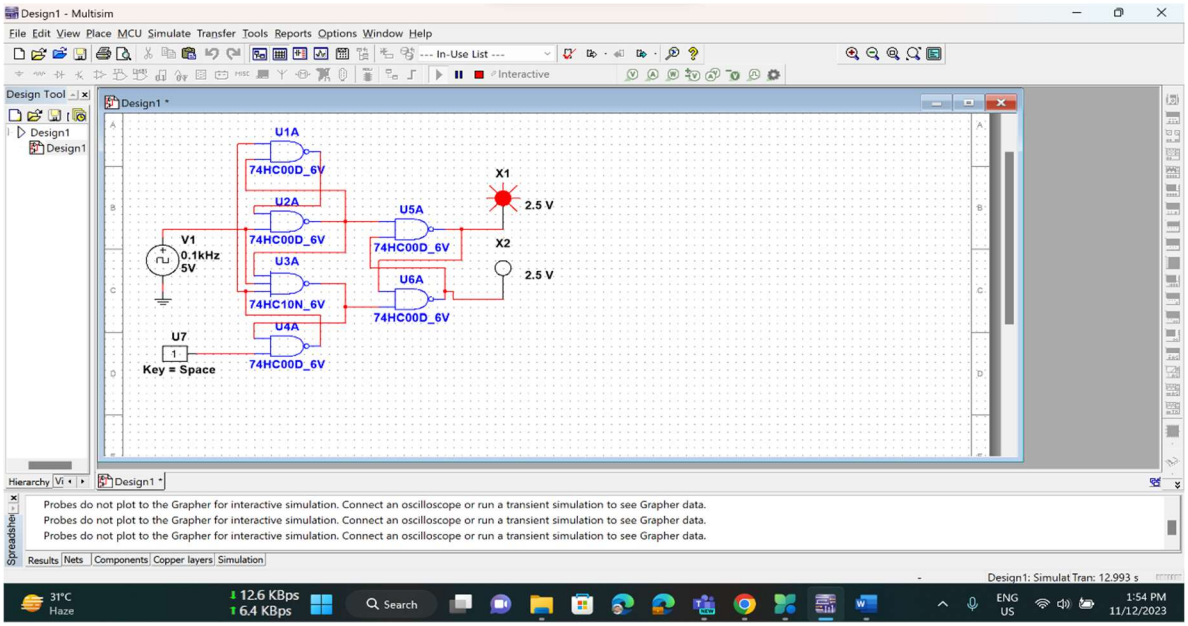


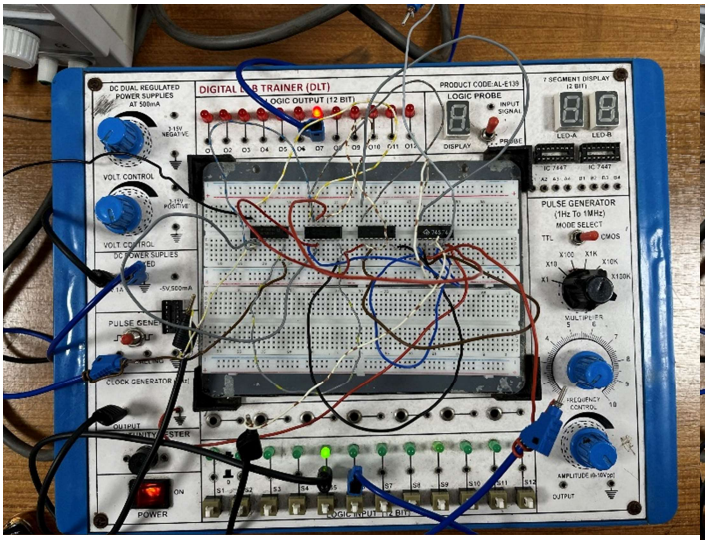
Figure-19: Simulation for logic circuit of a positive edge triggered D flip-flop with preset (active low) and asynchronous clear (active low) capability.

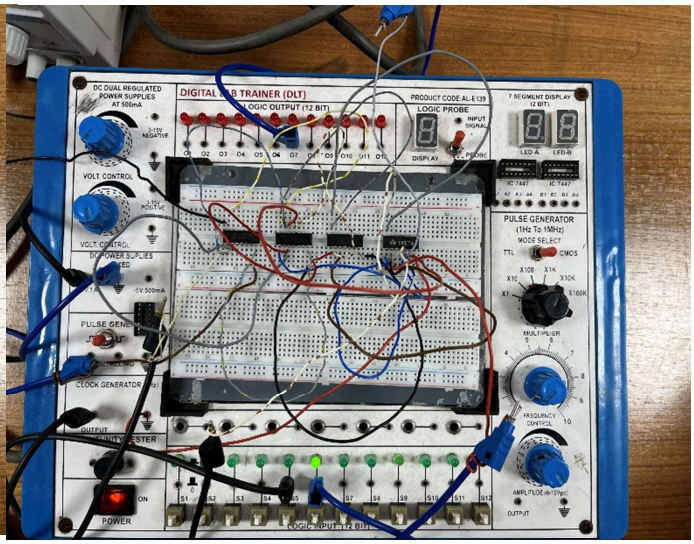
Truth Table for D flip-flop:

Input D_n	Output Q_{n+1}
0	0
1	1

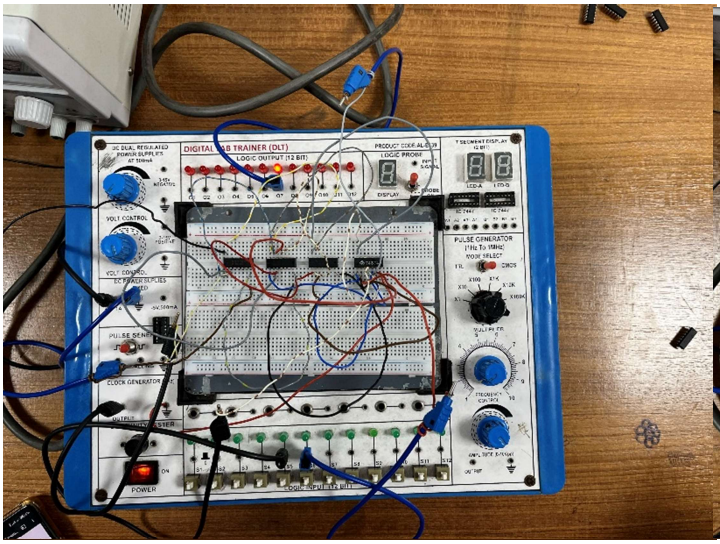
Experimental Circuit Diagram:

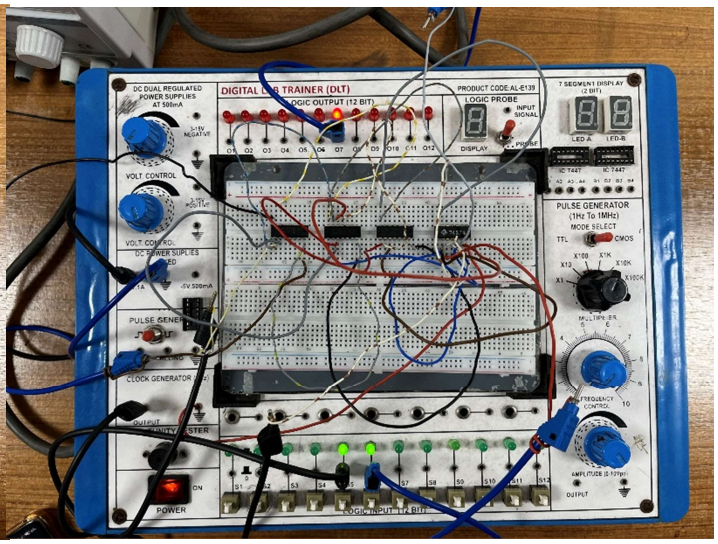
D Fllip-Flop:





J-K Flip Flop (using d-flip flop):





Discussion and Conclusion:

In this experiment, we explored various types of flip-flops by applying different combination of inputs (0, 1) and observed the outcomes (set, reset, no change, toggle). Through the experiment, we became familiar with positive-edge triggered D flip-flops with and without 'Preset' and 'Clear' capabilities, as well as J-K and T flip-flops. Moreover, we successfully designed a D flip-flop with active-low 'Preset' and 'Clear' pins, enabling storage and output of data when the clock input is high. We used Multisim software for the simulation part. When doing simulation, we faced some error but later on fixed them. This experiment deepened our understanding of various flip-flops and their behavior under different conditions, empowering us to design and analyze flip-flops for specific applications based on clock triggers and input characteristics.

References:

1. "Fundamentals of Digital Logic with verilog design" by – Brown &Vranesic
2. www.wikipedia.org
3. http://www.cs.umd.edu/class/spring2003/cmsc311/Notes/Seq/flip.html