AMERICAN INTERNATIONAL UNIVERSITY–BANGLADESH (AIUB)
FACULTY OF ENGINEERING
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
DIGITAL LOGIC AND CIRCUITS LABORATORY

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Group: 02, Section: Q

LAB REPORT ON

Implementation of Asynchronous and synchronous counters using flip-flops.

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Introduction:

Counters are combinations of flip-flops arranged so that they can remember how many clock pulses have been applied over some specified interval. The flip-flops are often interconnected so that only a portion of their available binary states can be supported. If there are N flip-flops being used in a counter, the number of states available is 2N. If the counter proceeds cyclically through K of these states, where $K \leq 2N$, it is said to be a modulo K (or MOD K) counter. Some applications will require a separate output to indicate each of the counter's states, alternatively, other applications may require only one output pulse for every Kth state. Counters are classified into two broad categories according to the way they are clocked: asynchronous and synchronous. In asynchronous counters, commonly called ripple counters, the first flip-flop is clocked by the external clock pulse and then each successive flip flop is clocked by the output of the preceding flip-flop. In synchronous counters, the clock input is connected to all the flip-flops so that they are clocked simultaneously. The objective of this experiment is designing of the following counters using J-K Flip-Flops (IC 74LS76)

(a) n-bit Binary Asynchronous Counter.

(b) n-bit Binary Synchronous Counter.

Theory and Methodology:

Asynchronous Counter:

In asynchronous counter, a clock pulse drives FF0. Output of FF0 drives FF1 which then drives the FF2 flip flop. All J and K inputs are connected to Logic 1. Therefore, each flip flop will toggle with negative transition at its clock input. The 3-bit MOD-8 asynchronous counter consists of 3 JK flip flops. Overall propagation delay time is the sum of individual delays. Initially all flip flops are reset to produce 0. The output condition is Q2Q1Q0 = 000.

When the first clock pulse is applied, the FF0 changes state on its negative edge. Therefore, Q2Q1Q0 = 001. On the negative edge of second clock pulse flip flop FF0 toggles. Its output changes from 1 to 0. This being negative change, FF1 changes state. Therefore, Q2Q1Q0 = 010. Similarly, the output of flipflop FF2 changes only when there is negative transition at its input when fourth clock pulse is applied.

The output of the flip flops is a binary number equivalent to the number of clock pulses received. The output conditions are as shown in the truth table. On the negative edge of eighth pulse, counter is reset. The counter acts as a frequency divider. FF0 divides clock frequency by 2, FF1 divides clock frequency by 4, FF2 divides clock frequency by 8. If n flip flops are cascaded, we get 2n output conditions. the largest binary number counted by n cascaded flip flops has a decimal equivalent of $2n-1$. MOD-8 counter has count of the largest binary number 111 which has decimal equivalent of $2^3-1 = 7$.

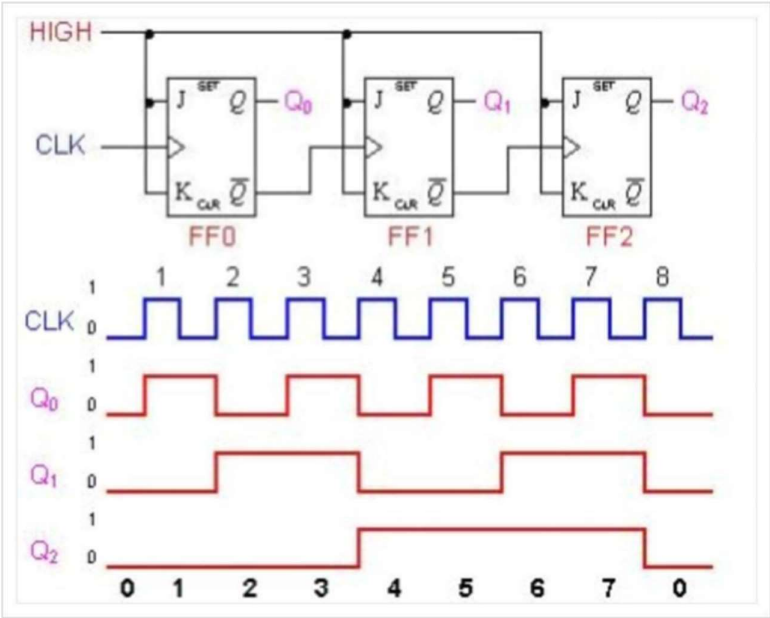

Fig 1: 3-bit Asynchronous counter and its timing diagram

Synchronous Counter:

Synchronous Counters are so called because the clock input of all the individual flip-flops within the counter are all clocked together at the same time by the same clock signal. Unlike asynchronous counters whose output of one stage is connected directly to the clock input of the next counter stage in the chain. The synchronous counter has its stages all clocked together at the same time. The problem with Asynchronous counters is that they suffer from what is known as "Propagation Delay" in which the timing signal is delayed a fraction through each flip-flop. However, with the Synchronous Counter, the external clock signal is connected to the clock input of EVERY individual flip-flop within the counter so that all of the flip-flops are clocked together simultaneously (in parallel) at the same time giving a fixed time relationship. In other words, changes in the output occur in "synchronization" with the clock signal. The result of this synchronization is that all the individual output bits change state at the same time in response to the common clock signal with no ripple effect and therefore, no propagation delay.

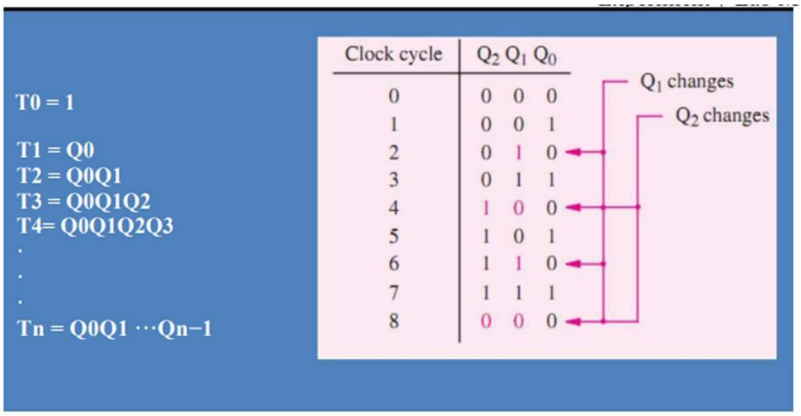

Figure 2

The Circuit diagram of a four-bit counter based on these expressions is given in Figure 3. Figure 4 gives a timing diagram. It shows that the circuit behaves as a modulo-16 up-counter. Because all changes take place with the same delay after the active edge of the Clock signal, the circuit is called a synchronous counter.

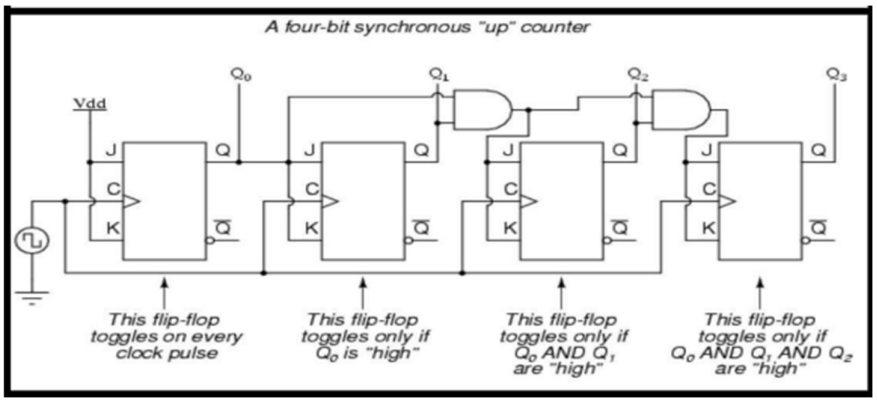

Fig 3: A four-bit Synchronous Up Counter

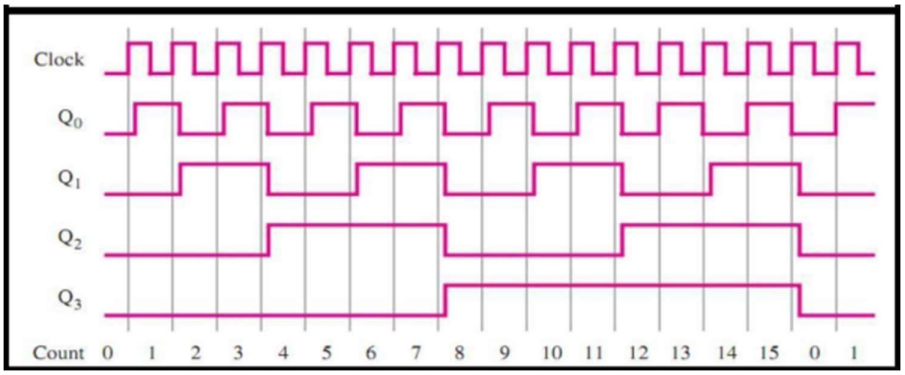

Fig 4: The timing diagram of a four-bit Synchronous Up Counter

Pin Configuration of 7473 and 7408

There are 2 J-K Flip Flops in one IC. Here is the pin configuration of the IC 7473:

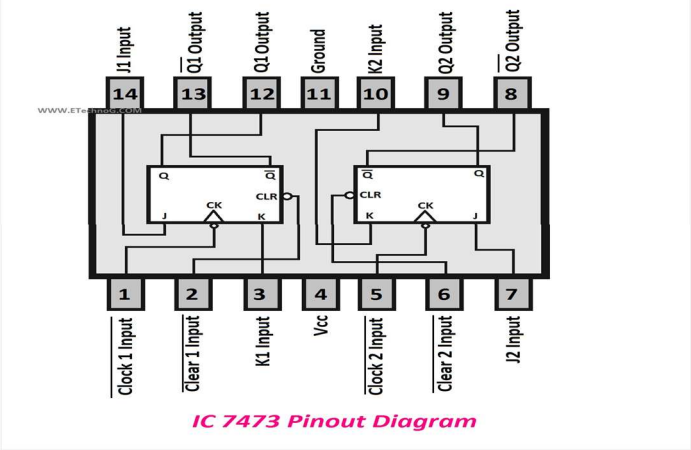

Fig 5: IC 7473

IC 7408 contains 4 AND gates in it. The pin configuration is shown below:

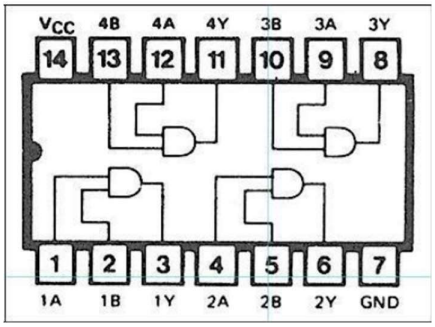

Fig 6: IC 7408

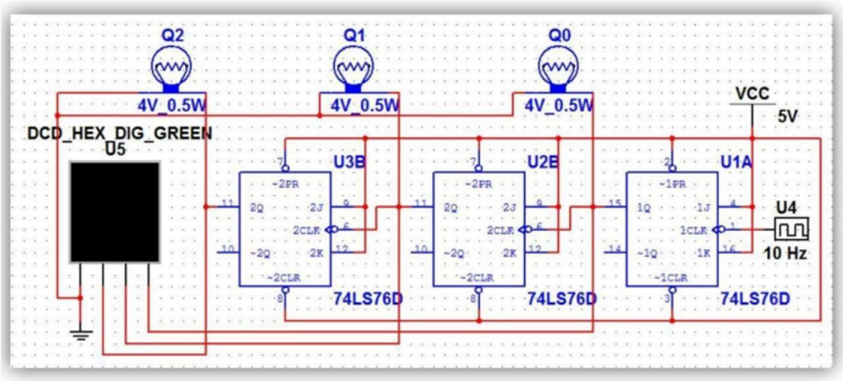

Fig 7: 3-bit Asynchronous Counter

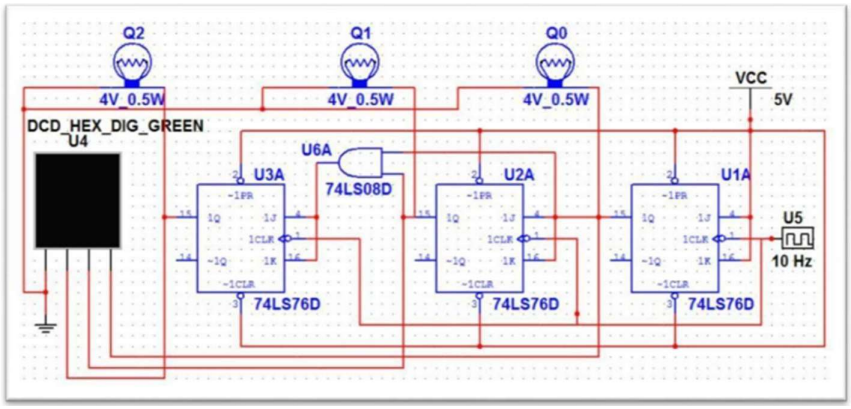

Fig 8: 3-bit Synchronous Counter

Apparatus:

- IC 7473 (JK Flip Flop)
- IC 7408 (AND IC)
- Trainer Board
- Connecting Wires

Precautions:

- Before preparing the circuits, we checked all the ICs (7473 & 7408) to make sure they are all working properly.
- We were careful about the biasing of JK Flip Flops.
- We made sure that we connected the preset and clear pins with Vcc.
- We tried to use as less wire as possible and made sure there was no loose connection.

Experimental Procedure

Part 1: 3-bit Asynchronous Counter

1. We constructed the circuit on the bread board as shown in Figure.
2. We used the trainer board's signal generator for the clock pulse and power supply for biasing the Flip Flops.
3. We observed the output results, recorded them and also took some pictures for our lab report.

Part 2: 3-bit Synchronous Counter

1. We constructed the circuit on the bread board as shown in Figure.
2. We used the trainer board's signal generator for the clock pulse and power supply for biasing the Flip Flops.
3. We observed the output results, recorded them and also took some pictures for our lab report.

Simulation and Measurement:

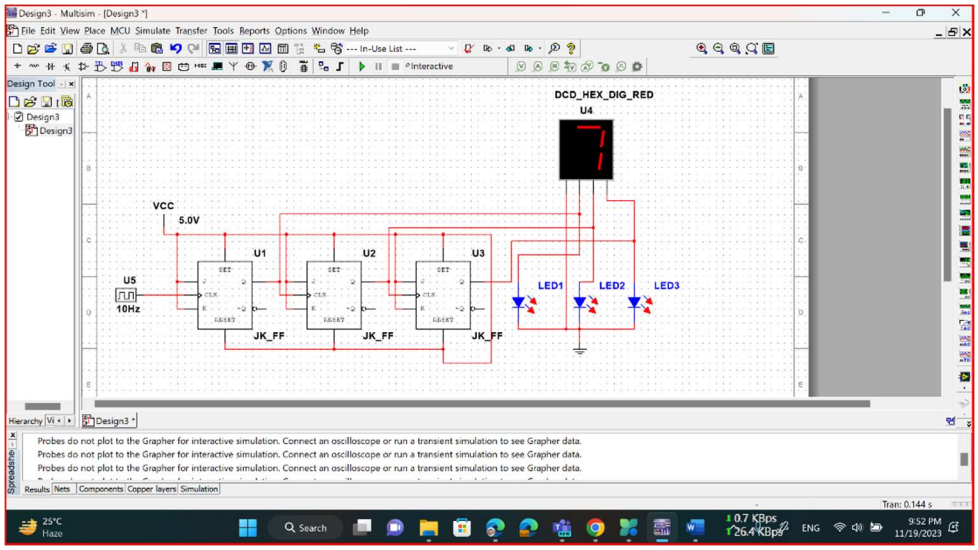

Figure 9: 3-bit Asynchronous up Counter

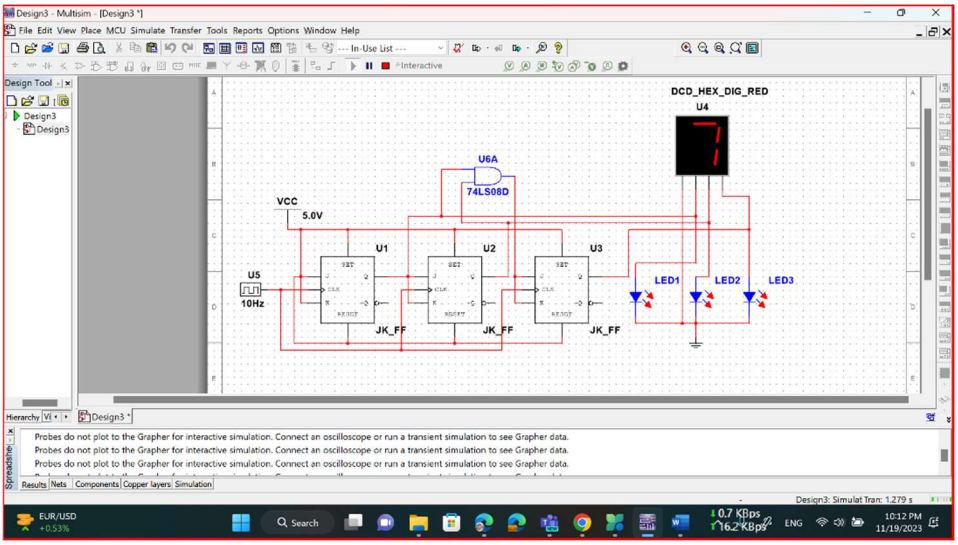

Figure 10: 3-bit Synchronous up Counter

Truth Table:

Counter State	Q_2	Q_1	Q_0
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

Table 1: 3-bit asynchronous counter

State	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

Table 2: 4-bit Synchronous counter

Discussion and Conclusion:

The main objectives of this experiment were to be familiar with J-K flip-flop, to know the working principle of J-K flip-flop and to know how flip-flop can be used to design a counter.At the very beginning of this experiment the core concept of flip-flop was discussed. The difference between asynchronous and synchronous counter was also distinguished. After thatthe timing diagram and clock cycle table was explained for both asynchronous and synchronous counter.

In the simulation part 3-bit asynchronous and synchronous counter was designed following thelab manual and by running the circuit the output was checked. Besides, 4-bit asynchronous and synchronous up counter was also simulated using MULTISIM online version as toggling the logic state in MULTISIM online version is easy and efficient. 3-bit asynchronous down counter and MOD 10 synchronous up counter was also designed as well. All the simulation circuit were run and the output were matched with the theoretical knowledge. No discrepancywas found in the output values.

As we now know about flip-flop and how they can be used to design counter, also we were able to design the 3-bit and 4-bit asynchronous and synchronous counter and also the Mod 10synchronous up counter using flip-flop; it can be said that the objectives of this experiment have been accomplished successfully.

References:

i) Thomas L. Floyd, “Digital Fundamentals”, Ninth Edition.

Questions and Answers:

1. Design of a 4-bit Asynchronous Up- Counter.

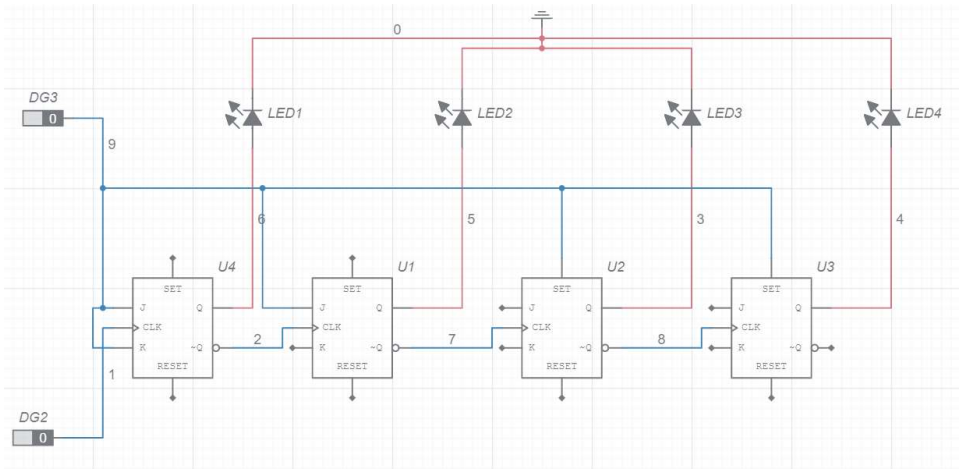

Figure 11: Simulation circuit of 4-bit Asynchronous Up- Counter

2. Design of a 4-bit Synchronous Up- Counter.

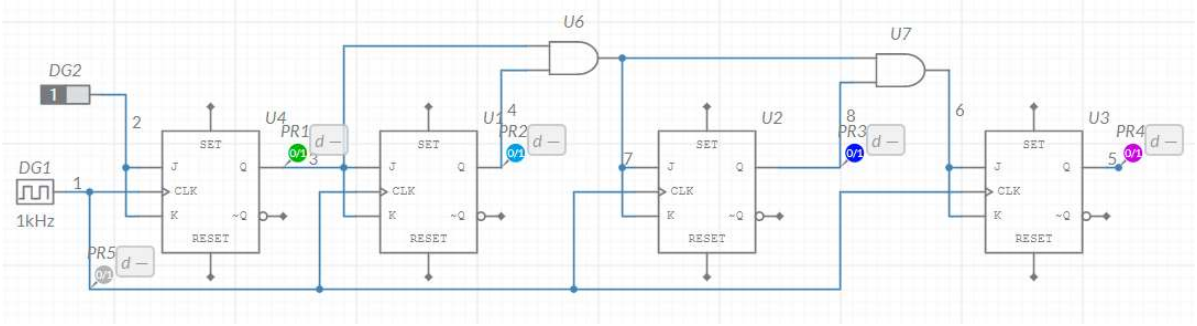

Figure 12: Simulation circuit of 4-bit Synchronous Up- Counter

Output:

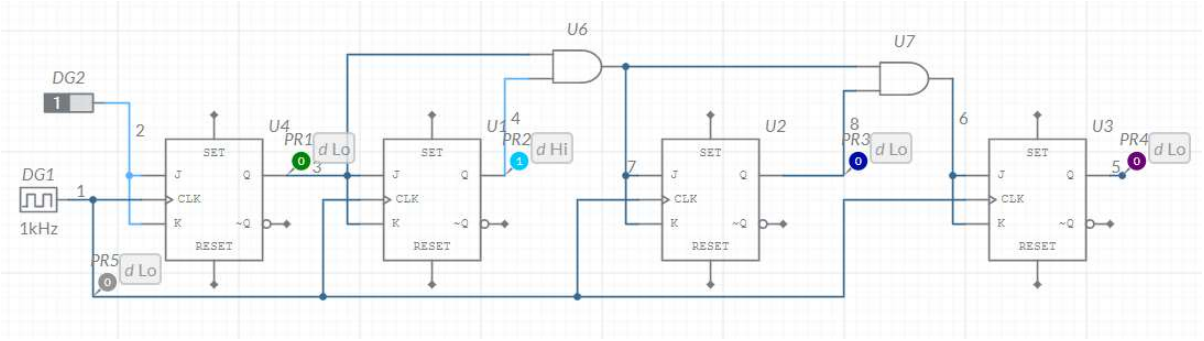

Figure 13: Output of the simulated circuit of 4-bit synchronous Up- Counter

Bonus Mark:

1. Design of a 3-bit Asynchronous down counter.

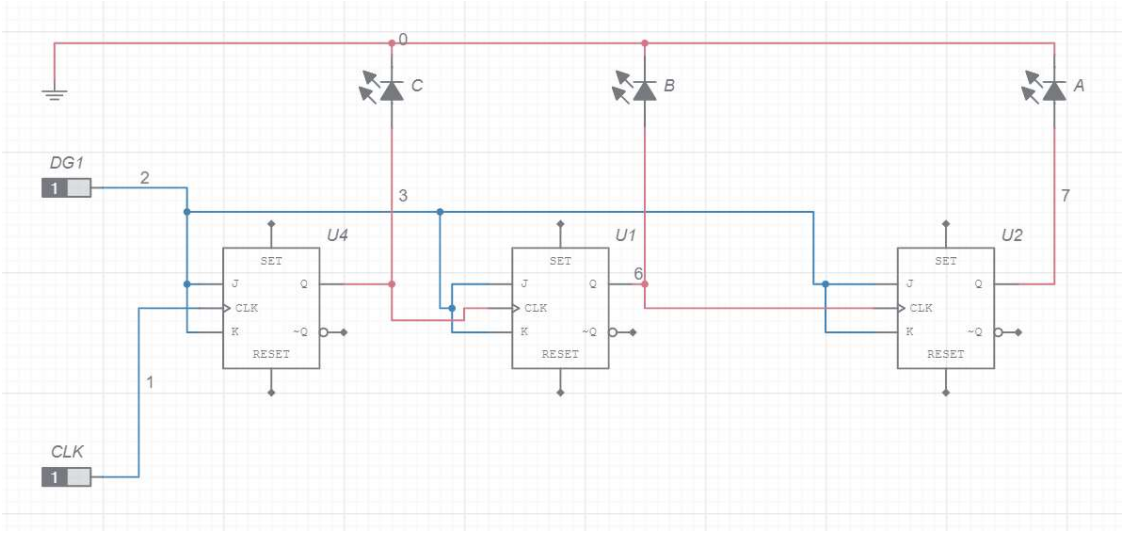

Figure 14: Simulation circuit of 3-bit Asynchronous Down- Counter

2. Design of a Mod 10 Synchronous up counter.

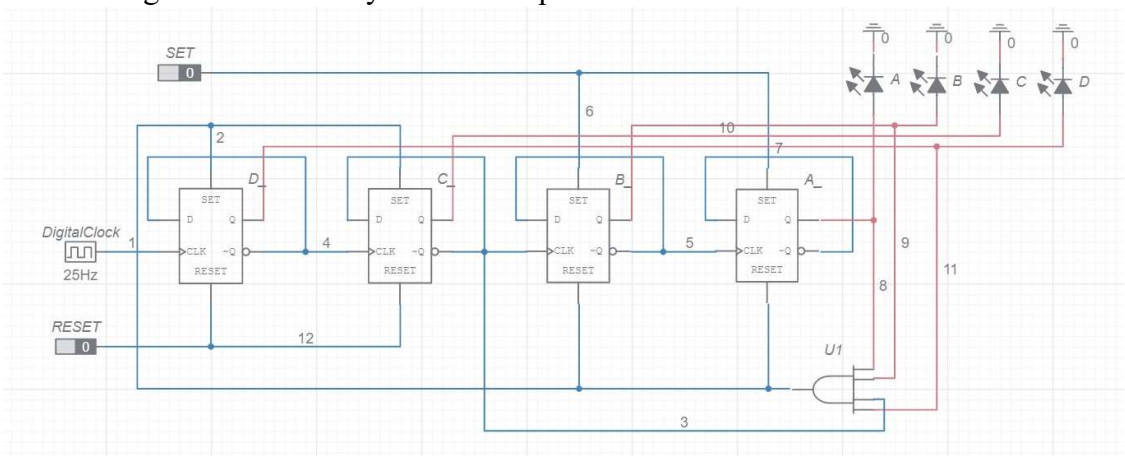

Figure 15: Simulation circuit of Mod 10 Synchronous up counter

Output:

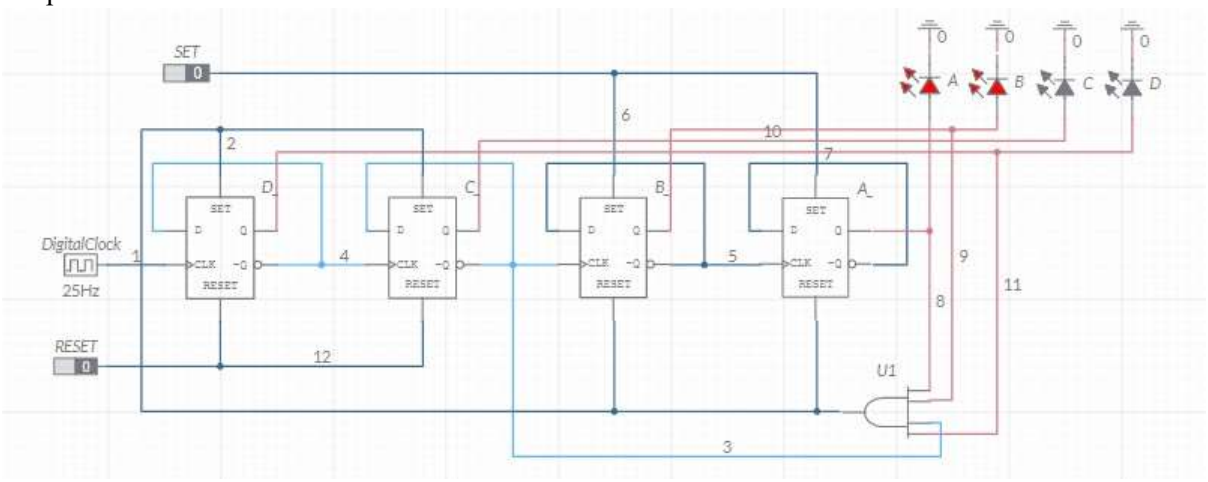

Figure 16: Output of the simulated circuit of Mod 10 Synchronous up counter