TOGETHER WE CAN ACHIEVE MORE

COURSE NAME: DLC LAB (DESIGN OF ADDER, SUBTRACTOR AND COMPARATOR CIRCUITS)

SEMESTER: SUMMER 22-23

SOLVED BY

Christopher Andrew Guda

Table of Contents:

Abstract:

The goal of this experiment is to learn about the design and operation of logic circuits such as adders, subtractors, and comparators. Adders and subtractors are the most fundamental and critical components of digital electronics.

Objectives:

- To get introduced and understand behavior of adder, subtractor and comparator logic circuits.
- To understand the Boolean expression for the above mentioned circuits.
- To understand BIT system of the comparator logic circuits.

Theory:

Many digital systems are built around adder, subtractor, and comparator circuits. They are intended to conduct simple arithmetic operations and to compare the magnitude of two digital signals.

Adder circuits: An adder circuit conducts binary number addition. A complete adder is the basic building block of an adder circuit; it adds three binary inputs (A, B, and carry-in) and creates two binary outputs (sum and carry-out). To perform the addition of bigger binary integers, full adders can be cascaded. The resulting sum is the binary representation of the input integers' arithmetic addition.

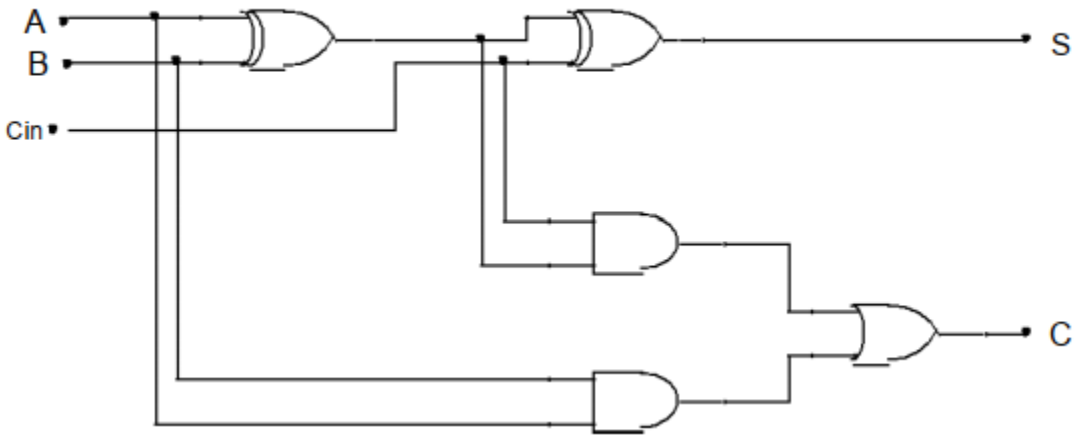

Figure 1: Full Adder Circuit

The Boolean Expression is:

$$S = A \oplus B \oplus Cin$$

$$Cout = Cin\,(A \oplus B) + AB$$

Subtractor Circuit: A subtractor circuit conducts binary number subtraction. With a few tweaks, it is similar to an adder circuit. A subtractor circuit complements the subtract and adds an additional input (borrow-in) to the full adder. During subtraction, the borrow-in signal handles the borrowing operation. The resulting difference is the binary representation of the input integers' arithmetic subtraction.

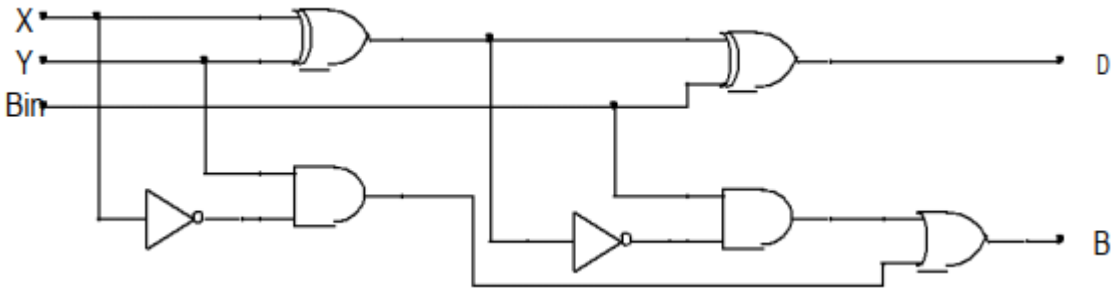

Figure 2: Full Subtractor Circuit

The Boolean expression is:

$$D = X \oplus Y \oplus Bin$$
$$Bout = X'Y + X'Bin + YBin$$

Comparator Circuit: A comparator circuit compares the magnitude of two binary integers and outputs a binary output indicating which is greater. There are two inputs and one output on the comparator circuit. If the first input is bigger, the output is '1'; otherwise, the output is '0'. The comparator circuit is frequently used in digital systems for sorting, searching, and other applications that need binary number comparison.

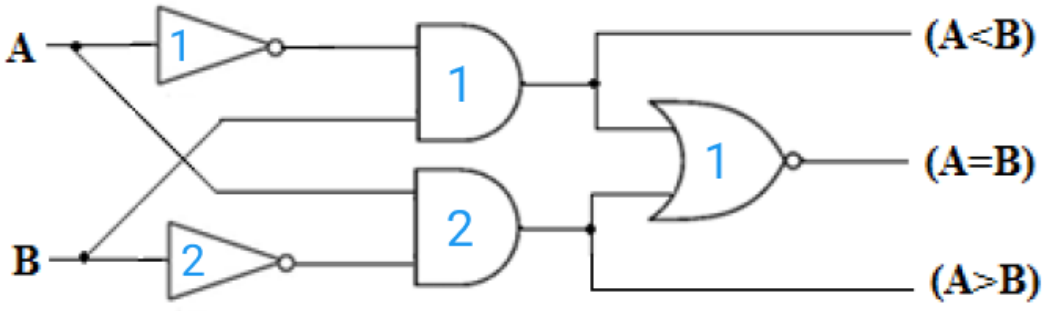

Figure 3.1: 1-bit comparator circuit diagram

The SOP expressions for the 1-bit comparator circuit is as the following:

(A = B) = A'B'+AB
(A < B) = AB'
(A > B) = A'B

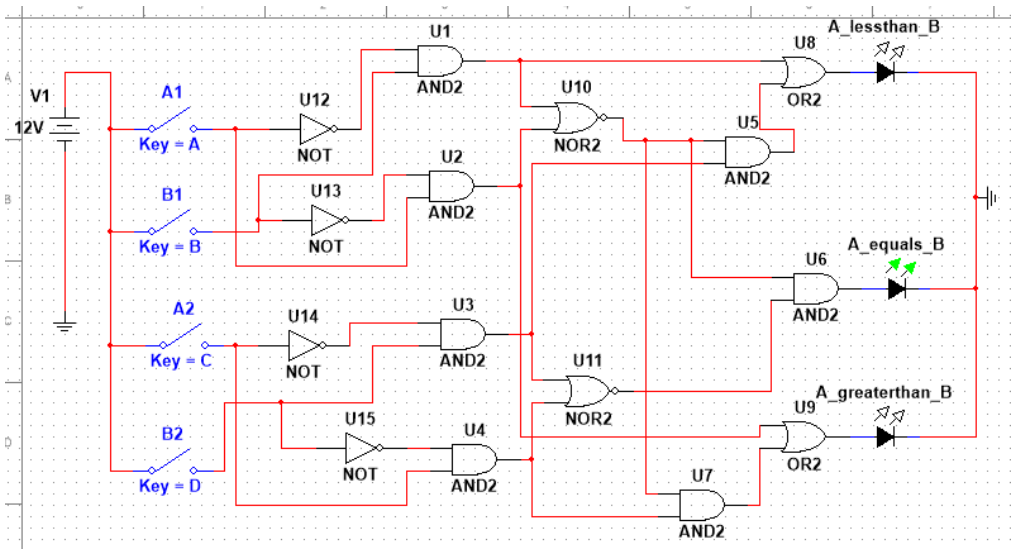

Figure 3.2: 2-bit comparator circuit using two 1-bit comparator blocks

Apparatus:

1. Digital trainer board
2. IC 7408:2pcs
3. IC 7404:2pcs
4. IC 7486:2pcs
5. IC 7431:2pcs
6. IC 7483:1pcs
7. Connecting wires

Experimental Procedure with Data & Simulations:

1. A full adder circuit was constructed as per requirement, and shown in figure 4. The data table for the full adder has been provided below.

Table 1: Truth table found from laboratory experiment for full adder.

A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

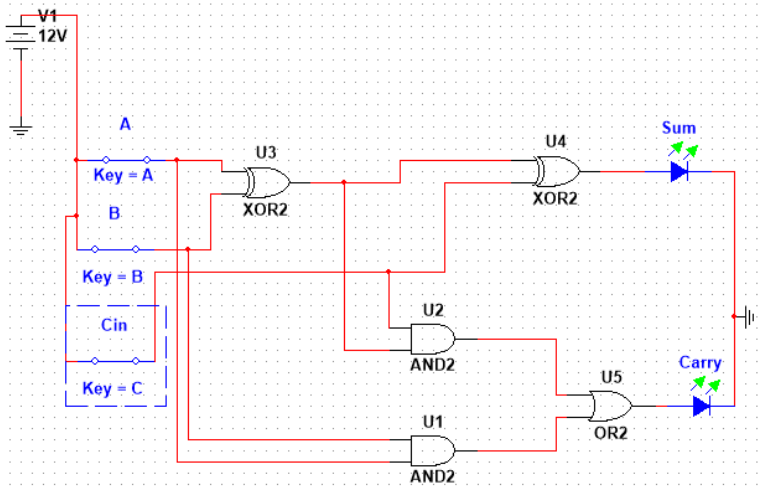

Figure 4: Circuit simulation of full adder circuit

2. A full subtractor circuit was constructed as per requirement, shown in figure 5. The data table for the full subtractor circuit has been given below.

Table 2: Truth table found from laboratory experiment for full subtractor.

A	B	B_{in}	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

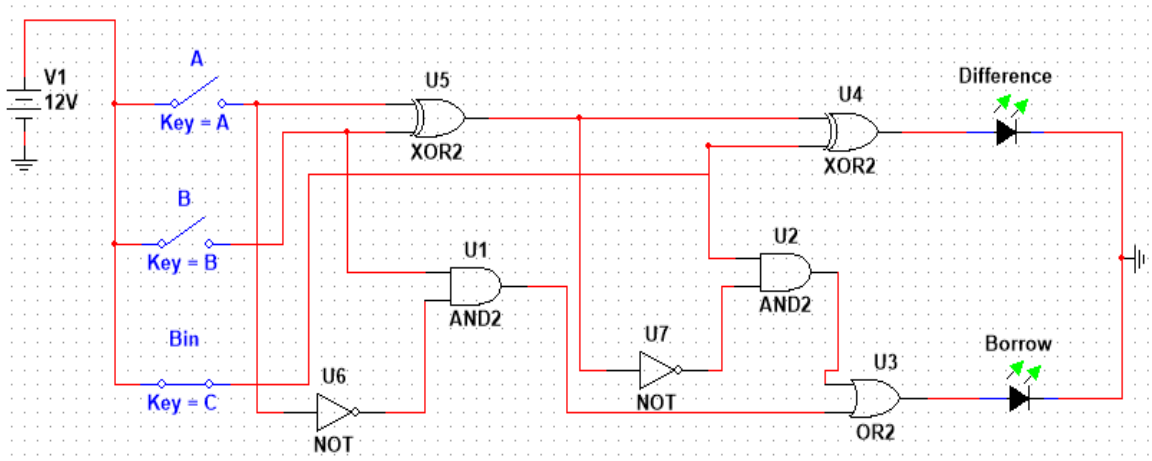

Figure 5: Circuit Simulation for full subtractor circuit.

3. A 2-bit comparator circuit was constructed as per figure 3.2, and shown in figure 6. The data table for the 2-bit comparator has been given below.

Table 3: Truth table found from laboratory experiment for 2-bit comparator.

A1	A2	B1	B2	A = B	A > B	A < B
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	1	0
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	0	1	0
1	1	1	1	1	0	0

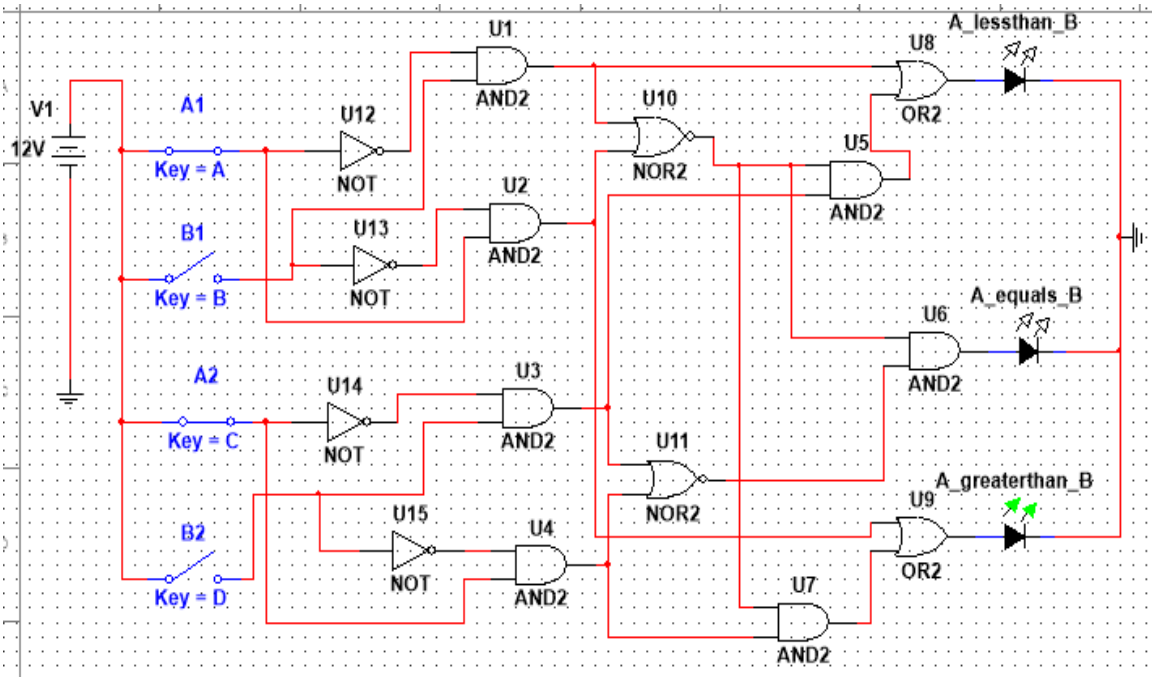

Figure 6: Circuit simulation for 2-bit comparator circuit.

4. A 4-bit full adder was constructed using Multisim simulation software shown in figure 7, where 7483 4-bit adder IC was used and the truth table shown in table 4. Since a 4-bit adder is basically four 1-bit adders in cascade, truth table for only 1 adder has been shown.

Table 4: Truth table for 4-bit adder circuit.

A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

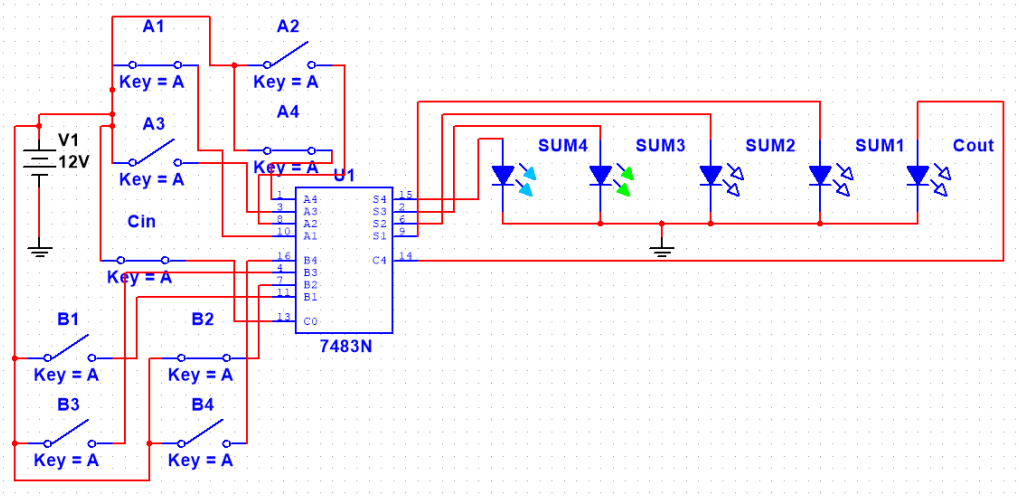

Figure 7: 4-bit full adder using 7483 IC.

Hardware Setup:

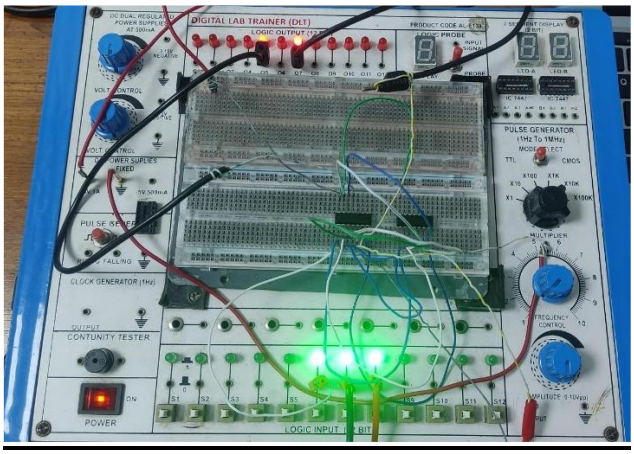

Figure 8: Full Adder

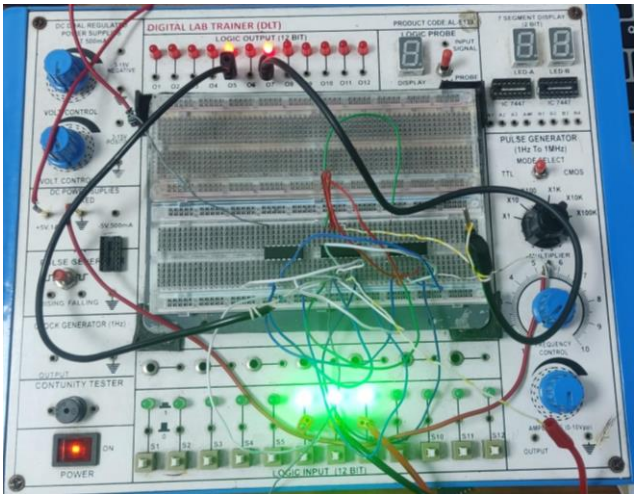

Figure 9: Full Subtractor

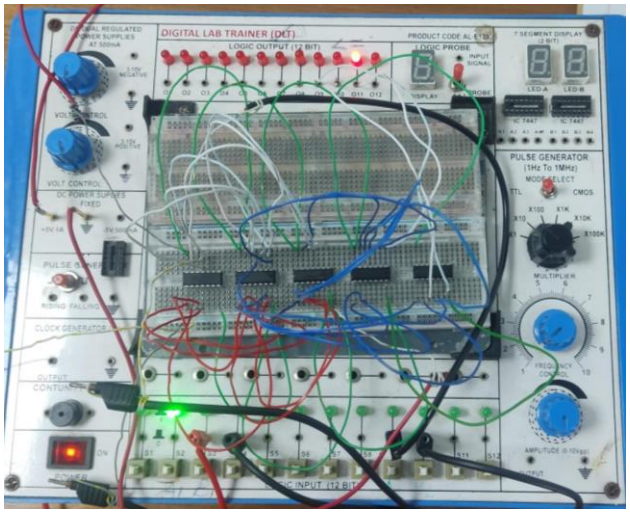

Figure 10: 2-bit comparator using two 1-bit comparator blocks

Results:

1. Figure 8 shows the hardware implementation of the full added circuit. The simulation is given in figure 4.
2. Figure 9 shows the hardware implementation for the full subtractor circuit. The simulation is given in figure 5.
3. Figure 10 shows the hardware implementation for the 2-bit comparator. The simulation is given in figure 6.
4. Figure 7 shows the connection and simulation for the lab manual required 4 bit full adder using IC 7483.

Discussions:

1. Adder, subtractor and comparator circuits all can be cascaded for ease of use and for easier scaling of operations.
2. In some cases, where the use of basic logic gates becomes too complex and time consuming, IC-s such as 7483 adder IC or 4008 comparator IC can be used for simplifying the circuit.
3. An issue was faced during the experiment, where the 2-bit comparator circuit during hardware implementation did not properly show a single logic output. The issue was rectified during simulations. No issues with the circuit design was found through simulations.

Answer to Questions:

1. Design a full adder circuit for performing 3-bit binary addition.

   Ans: Figure 11 shows the 3-bit full adder circuit.

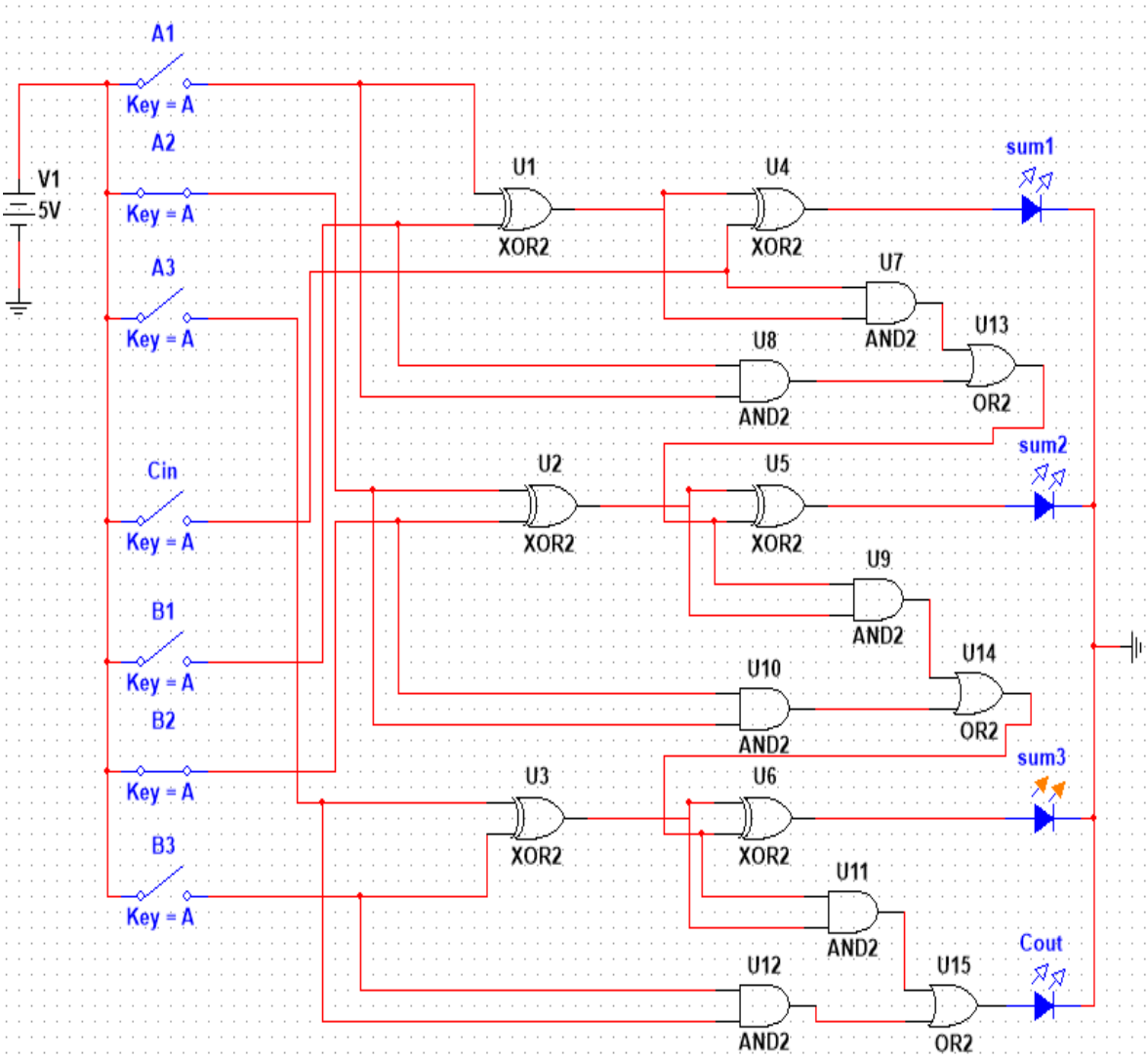

Figure 11: 3-bit full adder circuit

2. Design a full subtractor circuit for performing 3-bit binary subtractor.

   Ans: Figure 12 shows the 3-bit subtractor circuit.

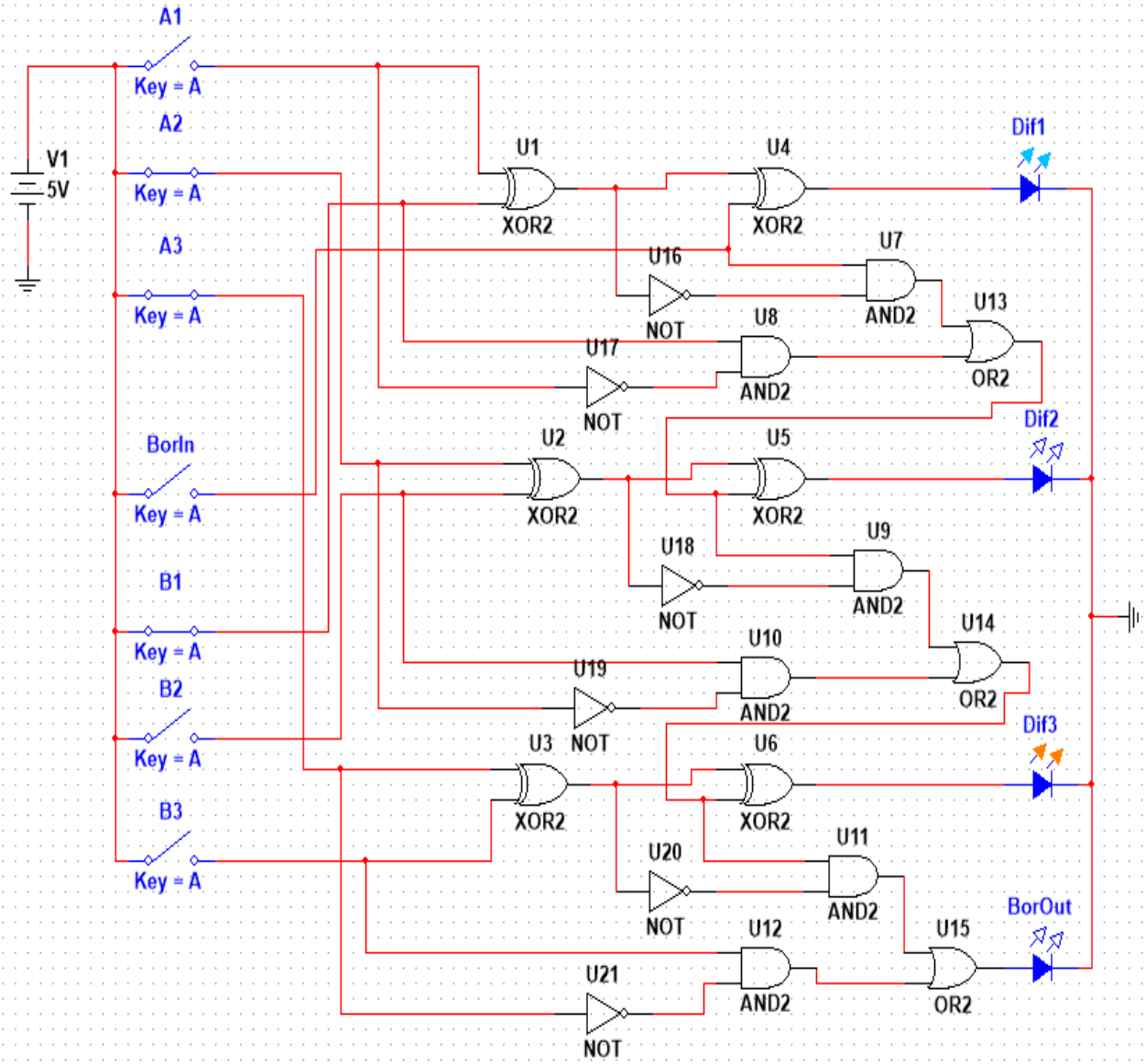

Figure 12: 3-bit full subtractor circuit.

3. Design an 8-bit full adder using 4-bit full adder IC 4008 from PSIM.

   Ans: An 8-bit full adder was designed and shown in figure 13 using two 4-bit adder IC using Multisim.

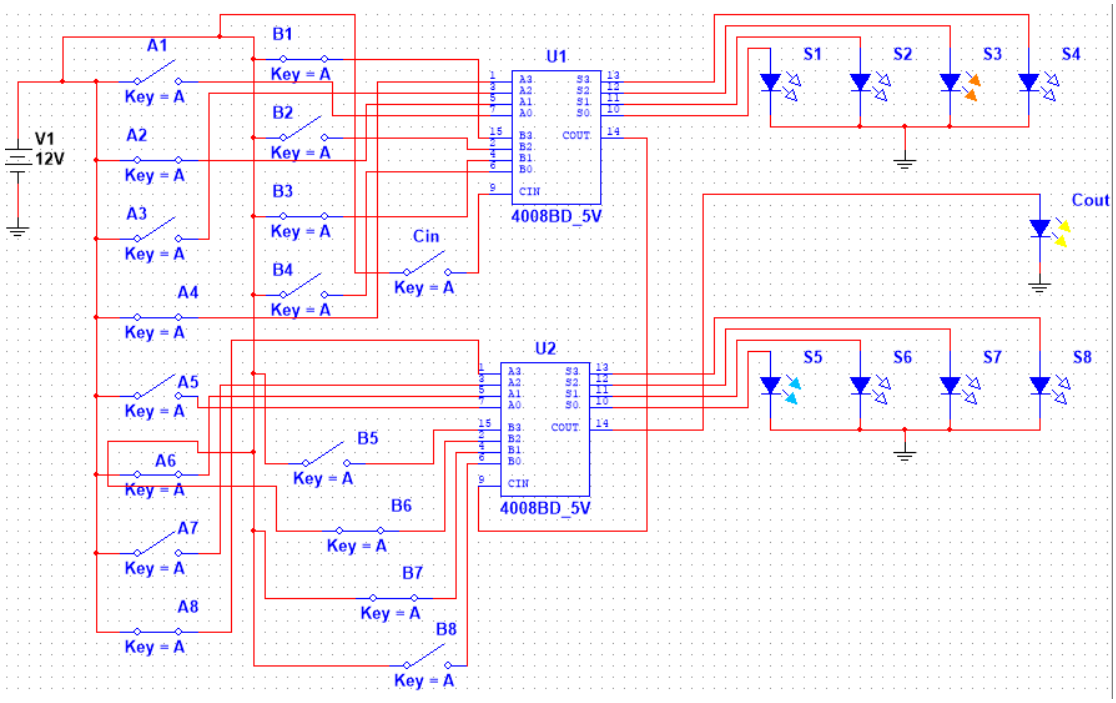

Figure 13: 8-bit full adder circuit using two 4-bit adder IC.

4. Design a comparator circuit for comparing two words, each of 3 bits of input using 1 bit block.

Ans: The comparator circuit is given in figure 14. The 7485N 4 bit comparator IC was used with its last remaining pins being disconnected.

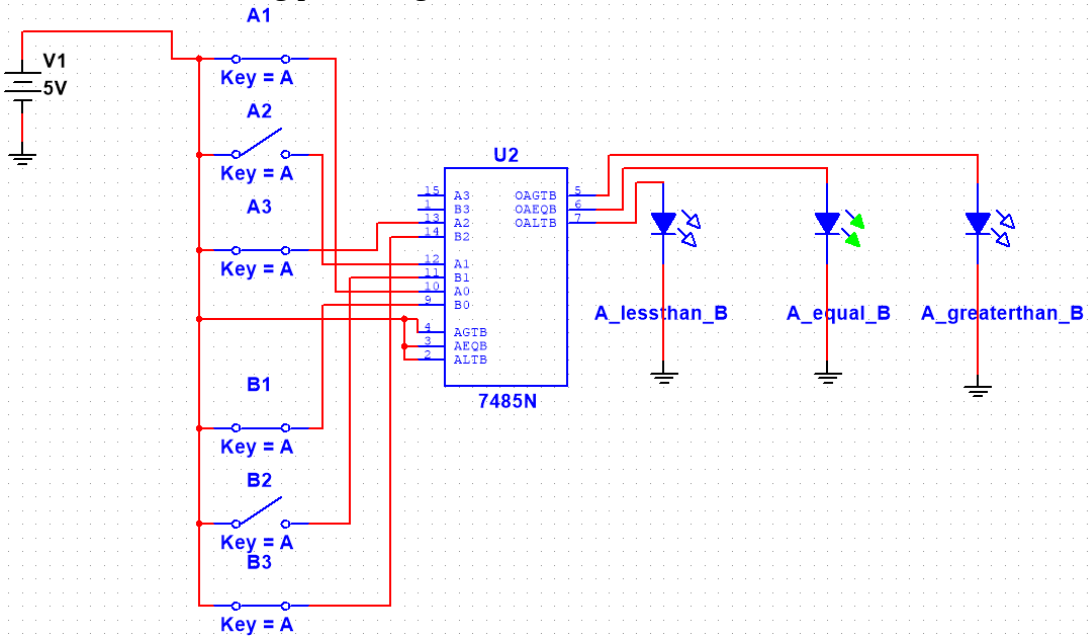

Figure 14: Simulation and design of a 3-bit comparator circuit using 7485 N IC.

References:

1. http://www.circuitstoday.com/half-adder-and-full-adder
2. AIUB DLC lab manual.

GROUP: https://www.facebook.com/groups/860221227407452
PAGE: https://www.facebook.com/acsaiub

https://www.youtube.com/channel/UCC3KjA8kstFtM-2CxVr-jcg