AMERICAN INTERNATIONAL UNIVERSITY – BANGLADESH (AIUB)
Faculty of Engineering
Department of Electrical and Electronic Engineering

Course Name: EEE4103 Microprocessor and Embedded Systems

Semester: Fall 2023-24 **Term**: Final **Quiz**: 03F **Total Marks**: 10 **Time**: 20 Minutes

Question Mapping with Course Outcomes:

Item	COs	POIs	K	P	A	Marks	Obtained Marks
Q1	CO1	P.a.4.C.3	K4			5	
Q2	CO1	P.a.4.C.3	K4			5	
					Total:	10	

Student Information:

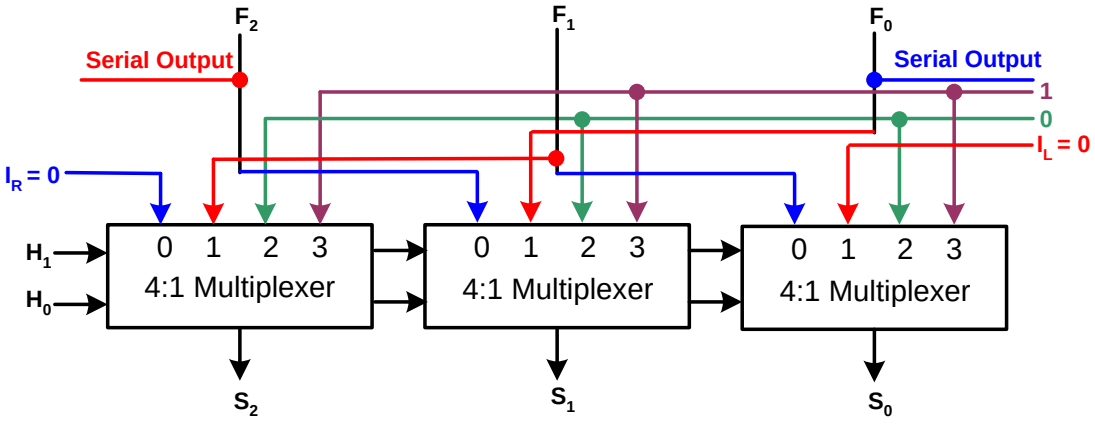
Student Name:	Solve Sheet			Section:	B
Student ID #:	Solve Sheet	Date:	04.12.2023	Department:	

1. Design a 3-bit shifter for the four shifting operations listed in the following Table: [5]

Binary Code	The function of selection variables					
	A	B	D	F with C_{in} = 0	F with C_{in} = 1	H
0 0	Input Data	Input Data	None	A	A+1	Shift Right with I_R=0
0 1	R1	R1	R1	A+B	A+B+1	Shift Left with I_L=0
1 0	R2	R2	R2	A+B'	A+B'+1	0's to the output Bus
1 1	R3	R3	R3	A-1	A	1's to the output Bus

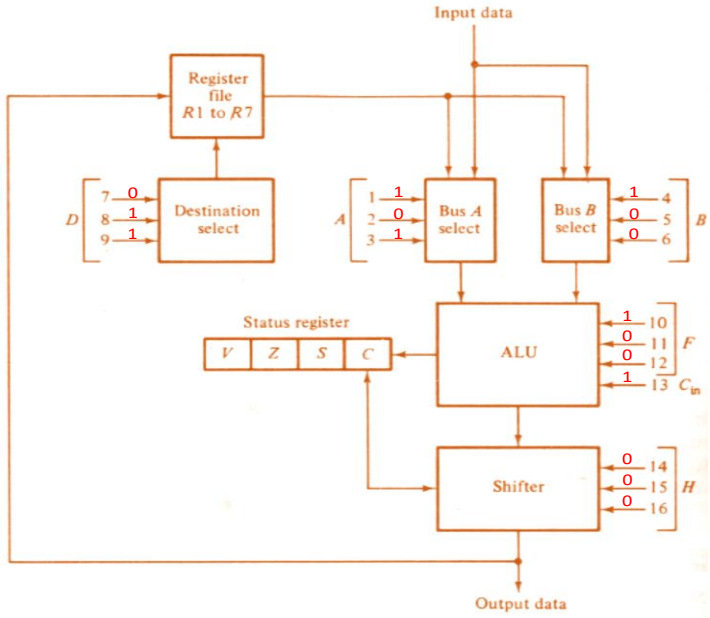
Answer:

The designed shifter is given below:



2. Determine the outputs of the register after completing the operation of the following figure based on the data of the register file. Determine the condition bit values for *C* and *Z*. [5]

Register	Contents							
R0	1	0	0	1	1	0	0	0
R1	0	0	0	0	0	1	0	1
R2	1	1	0	1	0	1	0	0
R3	0	0	0	0	1	1	0	0
R4	0	1	0	0	0	0	1	1
R5	0	0	1	0	1	0	0	1
R6	1	0	0	1	0	0	0	1
R7	0	0	0	0	1	0	0	0



Answer:

The control word is as follows based on the data available in the above figure:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A			B			D			F			C_{in}	H		
Source 1			Source 2			Destination			Function			Carry	Shift		
1	0	1	1	0	0	0	1	1	1	0	0	1	0	0	0
R5			R4			R3			R5 OR R4			X	No Shift		

Now, from the function table below, we find that this diagram will do the logical operation, OR between the R5 and R4 register and store it into the R3 register, i.e. the microoperation is R3 ← R5 OR R4.

TABLE 9-8 Functions of control variables for the processor of Fig. 9-16

Binary code	Function of selection variables					
	A	B	D	F with $C_{in} = 0$	F with $C_{in} = 1$	H
0 0 0	Input data	Input data	None	$A, C \leftarrow 0$	$A + 1$	No shift
0 0 1	R1	R1	R1	$A + B$	$A + B + 1$	Shift-right, $I_R = 0$
0 1 0	R2	R2	R2	$A - B - 1$	$A - B$	Shift-left, $I_L = 0$
0 1 1	R3	R3	R3	$A - 1$	$A, C \leftarrow 1$	0's to output bus
1 0 0	R4	R4	R4	$A \vee B$	—	—
1 0 1	R5	R5	R5	$A \oplus B$	—	Circulate-right with C
1 1 0	R6	R6	R6	$A \wedge B$	—	Circulate-left with C
1 1 1	R7	R7	R7	$\bar{A}$	—	—

The contents of R5 and R4 data from the above tables are given below. After the logical OR operation, the destination register (R3) data will be changed as follows:

Register	Contents after the Logical Operation							
R3 (*R3 ← R5 OR R4*)	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**1**
R4	0	1	0	0	0	0	1	1
R5	0	0	1	0	1	0	0	1

The condition bit values for *C* and *Z* will remain zero as the logical operation doesn't change the Carry flag bit and the Zero flag bit becomes one only if the zero is zero.