American International University – Bangladesh
Faculty of Engineering
Department of Electrical and Electronic Engineering

Course Name:	Microprocessor and Embedded Systems	**Course Code:**	EEE 4103
Semester:	Spring 23-24	**Section:**	F
Faculty Name:	Md Sajid Hossain		

Assignment No:	3 **(individual submission consisting of 30 marks)**

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[Sec: F]-Submission Link (MS forms): https://forms.office.com/r/zurGRhwBMW			
[Sec: Q]-Submission Link (MS forms): https://forms.microsoft.com/r/T6ZX6zhpFu			
Submission Date:	**06 May, 2024**	**Due Date:**	**EXAM DAY**

Assessment Rubrics:

COs-POIs	Excellent [28-30]	Proficient [25-27]	Good [20-24]	Acceptable [10-19]	Unacceptable [1-9]	No Response [0]	Secured Marks
CO3 P.a.4.C.3	All the problems are solved correctly. The simulation processes are clearly described, and results are generated by combining all possible input patterns with appropriate outcomes. All necessary drawings and computations are shown.	All the problems are solved correctly. The simulation processes are clearly described, and results are generated by combining all possible input patterns with appropriate outcomes. A few necessary drawings and computations are missing.	All the problems are solved correctly. The simulation processes are not clearly described, and results are generated by combining all possible input patterns with appropriate outcomes. Some necessary drawings and computations are missing.	All the problems are not solved correctly. The simulation processes are not clearly described, and results are generated by combining several wrong input patterns with inappropriate outcomes. Some necessary drawings and computations are missing.	All the problems are not solved correctly. The simulation processes are not described, and results are generated by combining mostly wrong input patterns with inappropriate outcomes. Almost all the necessary drawings and computations are missing.	No responses at all	
Comments					**Total marks (30)**		

Questions:

1. Prepare a design of 2-bit ALU for the operations listed in Table 1 [10]

Table 1: For Questions 1 and 2 and 3

Binary Code	Function of selection variables					
	A	**B**	**F with C_{in} = 1**	**F with C_{in} = 0**	**D**	**H**
0 0 0	Input Data	Input Data	A+1	A, C←0	None	1's to the output Bus
0 0 1	R1	R1	A, C←1	A-1	R1	Shift Right with I_R=0
0 1 0	R2	R2	A+B′+1	A+B′	R2	-
0 1 1	R3	R3	A+B+1	A+B	R3	Circulate Left with Carry
1 0 0	R4	R4	A U B	A U B	R4	0's to the output Bus
1 0 1	R5	R5	A′	A′	R5	No Shift
1 1 0	R6	R6	A ∩ B	A ∩ B	R6	Circulate Right with Carry
1 1 1	R7	R7	A XOR B	A XOR B	R7	Shift Left with I_L=0

2. Design a 3-bit shifter circuit for the listed shift functions provided in Table 1. [5]

3. Develop the control words in binary and hexadecimal formats using the information provided in Table 1 for the following micro-operations: [10]

   i. R7←R3+R4
   ii. R4←3(R4 – 0)/3
   iii. R3←SHL R3
   iv. Output←R5
   v. R5←R1
   vi. R2←0
   vii. R6←Input
   viii. R6←R4-R2
   ix. R2←SHR R5
   x. R3←CRC R7

One example is shown as follows:

Micro-operation	***A***	***B***	***D***	***F***	***C_{in}***	***H***	In Hex
R5← CRC (R3+R4)	**011**	**100**	**101**	**011**	**0**	**110**	72B6h

The necessary bits for the control word are presented in Table 2.

Table 1: 16-bit control word sequence

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A			*B*			*D*			*F*			C_{in}	*H*		

4. Show the flow chart for *counting the number of 1's* in register, R3, and storing the count in register R7. Assume that the starting address is 9. If register, R3 contains the data 10011011 then what would be the contents of register, R7 after this micro-operation is completed? [5]

Ans. to the ques. no: 1

S_2	S_1	S_0	C_{in}	F	X	Y	Z
0	0	0	1	A + 1	A	0	1
0	0	0	0	F = A (When C_{in} = 0)	A	0	0
0	0	1	1	F = A (When C_{in} = 1)	A	All 1's	1
0	0	1	0	A - 1	A	All 1's	0
0	1	0	1	$A + \bar{B} + 1$	A	$\bar{B}$	1
0	1	0	0	$A + \bar{B}$	A	$\bar{B}$	0
0	1	1	1	A + B + 1	A	B	1
0	1	1	0	A + B	A	B	0
1	0	0	X	A ∪ B	A+B	0	0
1	0	1	X	$\bar{A}$	A	1	0
1	1	0	X	A ∩ B	$A+\bar{B}$	$\bar{B}$	0
1	1	1	X	A XOR B	A	B	0

K-map for 'X':

S_2S_1 \ S_0	0	1
00	A	A
01	A	A
11	$A+\bar{B}$	A
10	A+B	A

$X = A + \bar{B}S_2S_1\bar{S_0} + BS_2\bar{S_1}\bar{S_0}$

K-map for 'Y':

S_2S_1 \ S_0	0	1
00	0	1
01	$\bar{B}$	B
11	$\bar{B}$	B
10	0	1

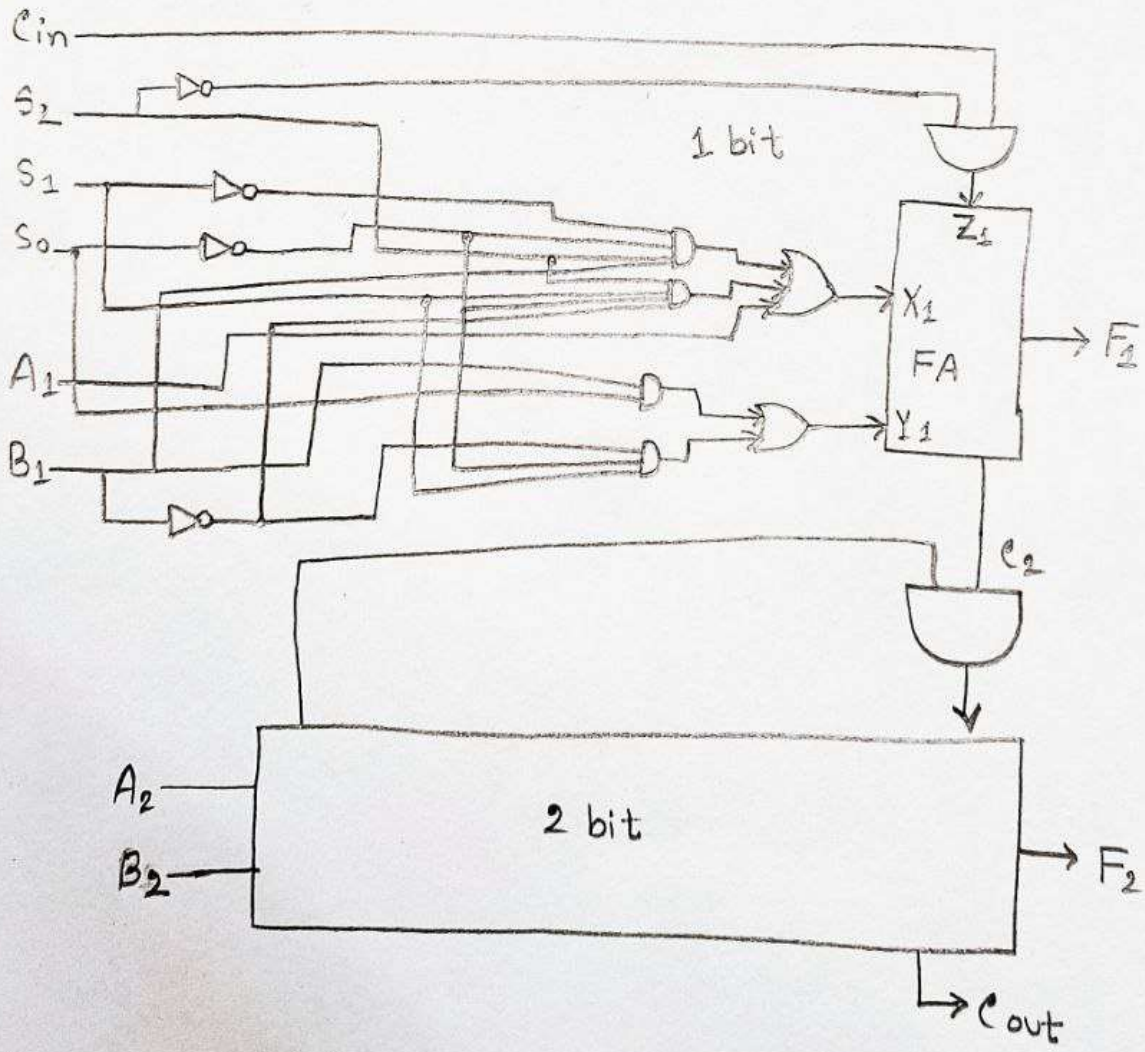
$Y = \bar{B}S_1\bar{S_0} + BS_0$

K-map for 'Z':

S_2S_1 \ S_0	0	1
00	C_{in}	C_{in}
01	C_{in}	C_{in}
11	0	0
10	0	0

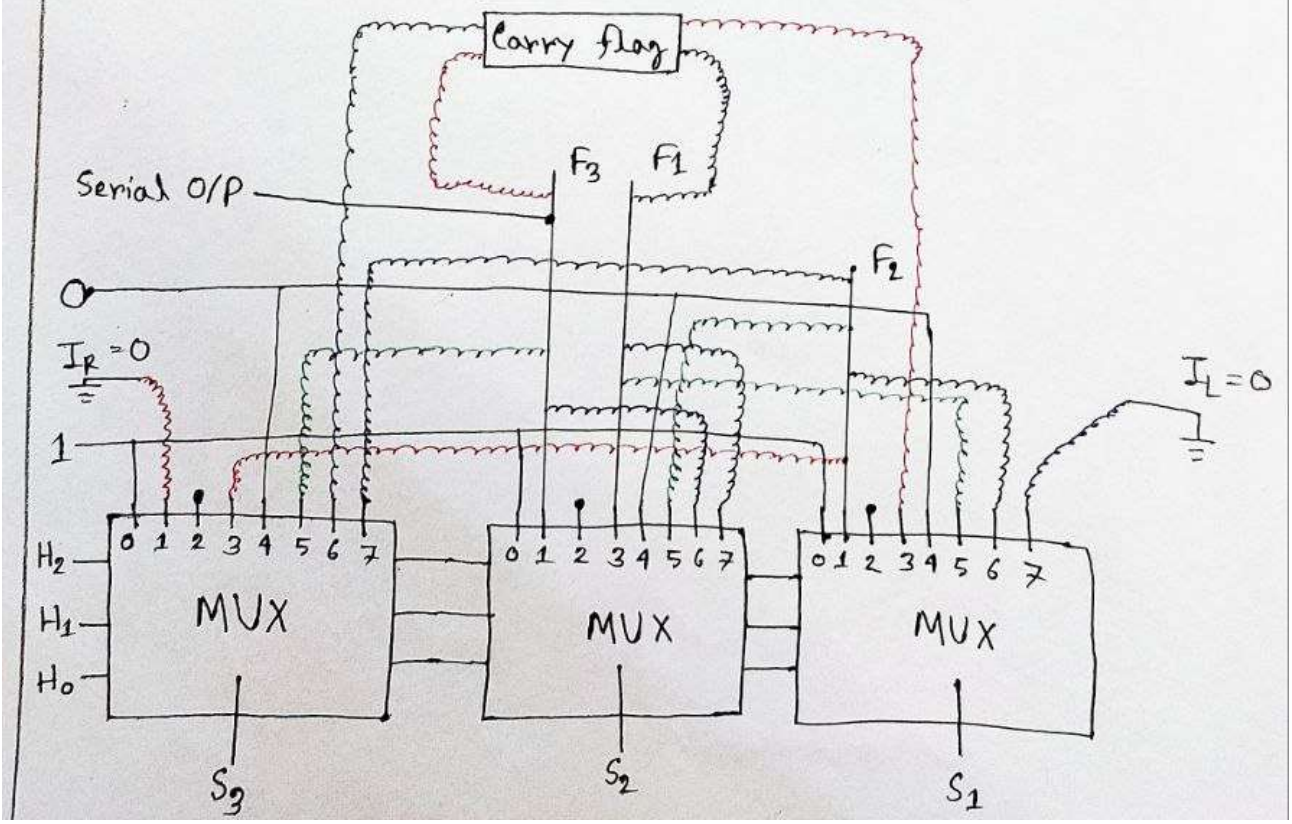
$$Z = C_{in}\overline{S_2}$$

Diagram:



Ans. to the ques. no: 2

Decimal	H_2	H_1	H_0	Functions
0	0	0	0	1's to the output bus
1	0	0	1	shift Right with $I_R = 0$
2	0	1	0	—
3	0	1	1	Circulate left with carry
4	1	0	0	0's to the output bus
5	1	0	1	No shift
6	1	1	0	Circulate right with carry
7	1	1	1	shift left with $I_L = 0$



Ans. to the ques no: 3

16 bit control words generation

(i) $R_7 \leftarrow R_3 + R_4$

(ii) $R_4 \leftarrow 3(R_4 - 0)/3$

(iii) $R_3 \leftarrow$ SHL R3

(iv) Output $\leftarrow$ R5

(v) R5 $\leftarrow$ R1

(vi) R2 $\leftarrow$ 0

(vii) R6 $\leftarrow$ Input

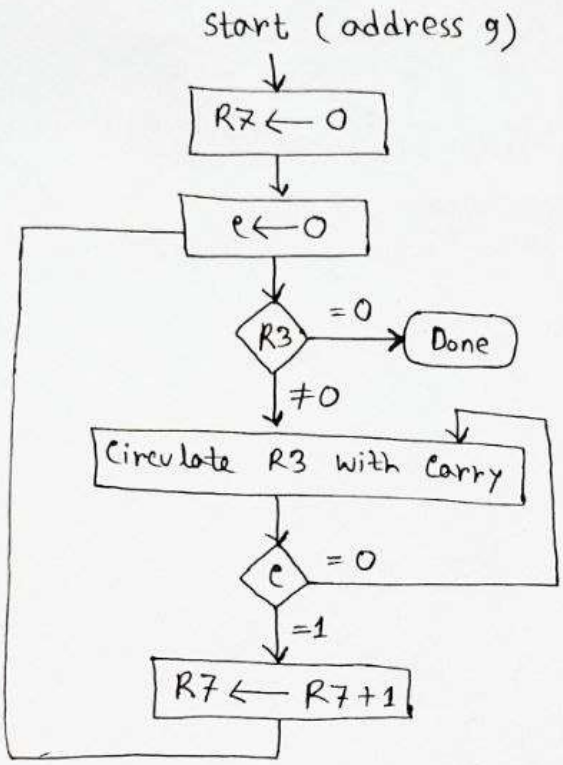
(viii) R6 $\leftarrow$ R4 - R2

(ix) R2 $\leftarrow$ SHR R5

(x) R3 $\leftarrow$ CRC R7

Number	A	B	D	F	Cin	H	In HEX
(i)	011	100	111	011	0	101	73B5
(ii)	011	011	011	100	0	111	6DC7
(iii)	100	000	100	000	0	101	8205
(iv)	101	000	000	000	0	101	A005
(v)	001	000	101	000	0	101	2285
(vi)	000	000	010	000	0	100	0104
(vii)	000	000	110	000	0	101	0305
(viii)	100	010	110	010	1	101	8B2D
(ix)	101	101	010	100	0	001	B541
(x)	111	111	011	100	0	110	FDC6

Ans. to the ques. no: 4:



Given,
R3 = 10011011
R7 = 5 (101)
↓
need to prove

R3 =	1 0 0 1 1 0 1 1	e = 0	R7 = 0
R3 =	1 1 0 0 1 1 0 1	1 0	R7 = 0+1 = 1
R3 =	0 1 1 0 0 1 1 0	1 0	R7 = 1+1 = 2
R3 =	0 0 1 1 0 0 1 1	0	
R3 =	0 0 0 1 1 0 0 1	1 0	R7 = 2+1 = 3
R3 =	0 0 0 0 1 1 0 0	1 0	R7 = 3+1 = 4
R3 =	0 0 0 0 0 1 1 0	0	
R3 =	0 0 0 0 0 0 1 1	0	
R3 =	0 0 0 0 0 0 0 1	1 0	R7 = 4+1 = 5

(Proved)