Assembler Programming of Atmega328P

Language Options to Program Atmega328P

- **Higher Level Languages (HLP)** – mostly machine independent.

  - C/C++

  - Wiring. This is nothing but higher level abstractions implemented using functions written in C/C++ to make the microcontroller programming easier. Arduino IDE uses Wiring.

- **Assembly Language (ALP)** – machine dependent.

ALP needs more effort as compared to HLP because it requires the knowledge of the instruction set of the MCU in addition to the knowledge of the internal architecture

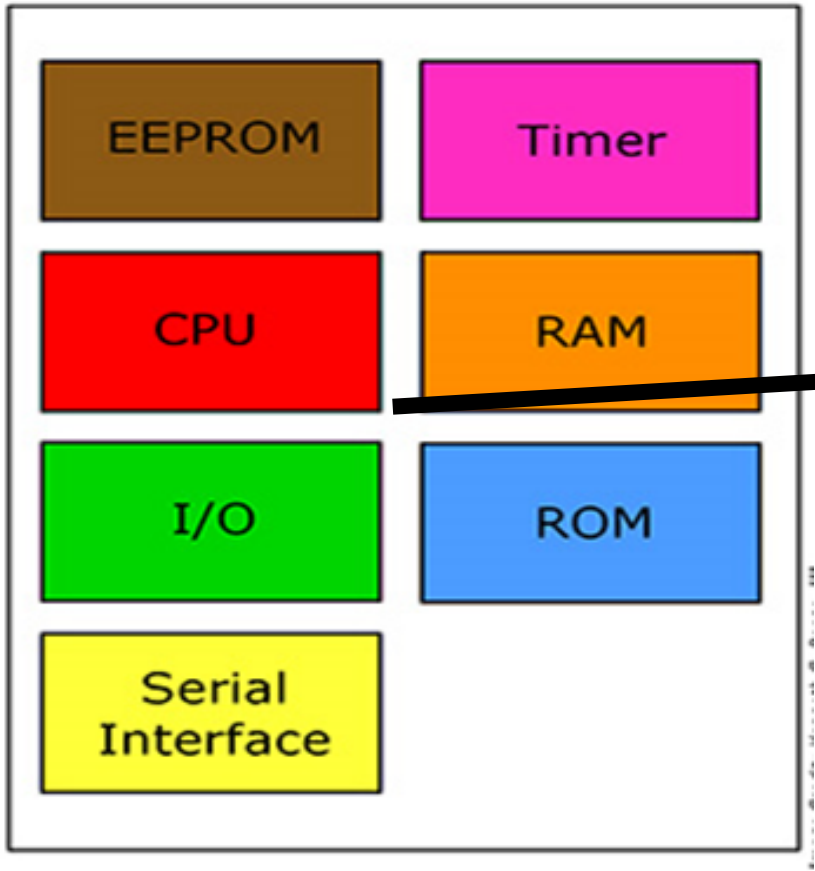
Machine dependent code optimization is limited to a specific hardware platform. Machine independent code optimization is applicable to any hardware platform. Machine independent code optimization makes it easier to port the code to other platforms.

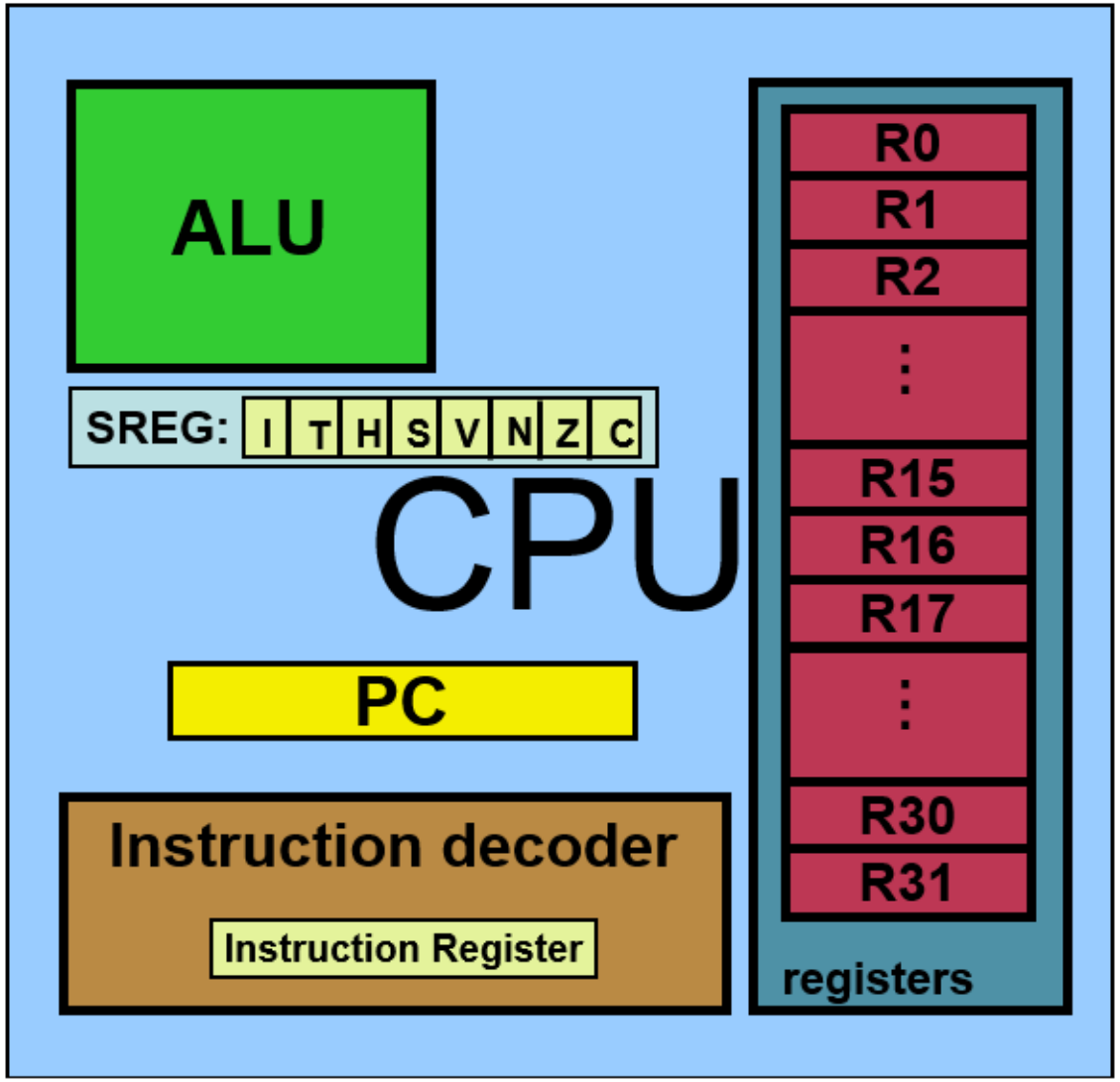
Why Assembly Language?

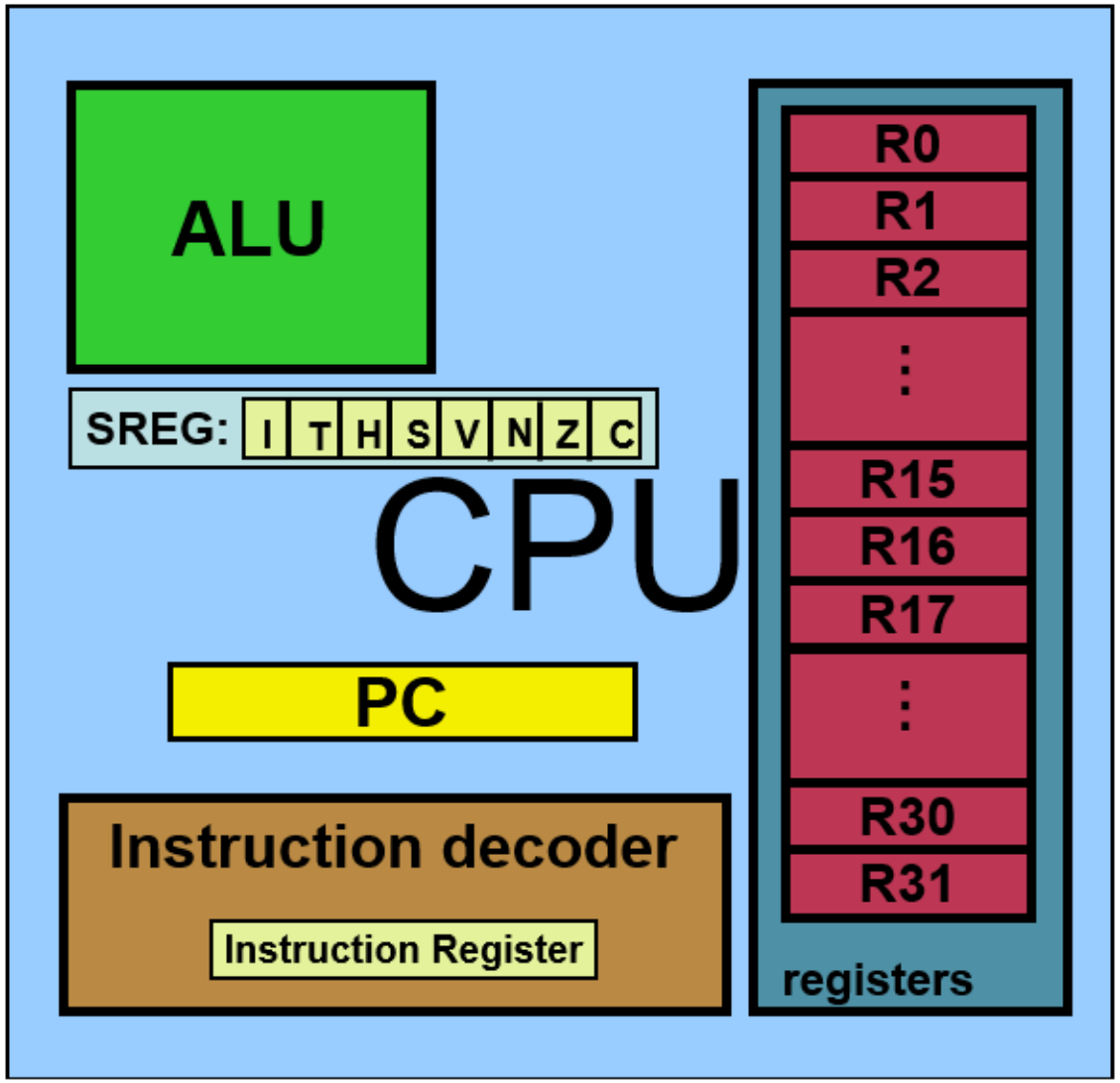
- To directly manipulate hardware
- To access specialized processor instructions
- To access machine-dependent registers and I/O
- Programs written in assembly can execute faster. It helps in writing highly optimized code (shortest, fastest program). This is very essential in time-critical and space-critical applications.
- Assembly access is also sometimes used when creating bootloaders
- Assembly gives direct access to all the hardware blocks inside the MCU which may not be possible by HLP.
- Assembly helps in better understanding of the internal architecture of MCU
- Knowledge of Assembly helps in detecting bugs in a machine language program by translating the machine code back into mnemonics using a disassembler which is a software that performs the translation.

ATEMGA328P CPU

Microcontroller: CPU on a single chip.







AVR Architecture of CPU

- ALU
- 32 General Purpose Register (each 8-bit)
- Program Counter (PC)
- Instruction Decoder
- Status Register (SREG)

AVR is a family of microcontrollers developed since 1996 by Atmel, acquired by Microchip Technology in 2016. Atmel says that the name AVR is not an acronym and does not stand for anything in particular. However, it is commonly accepted that AVR stands for -

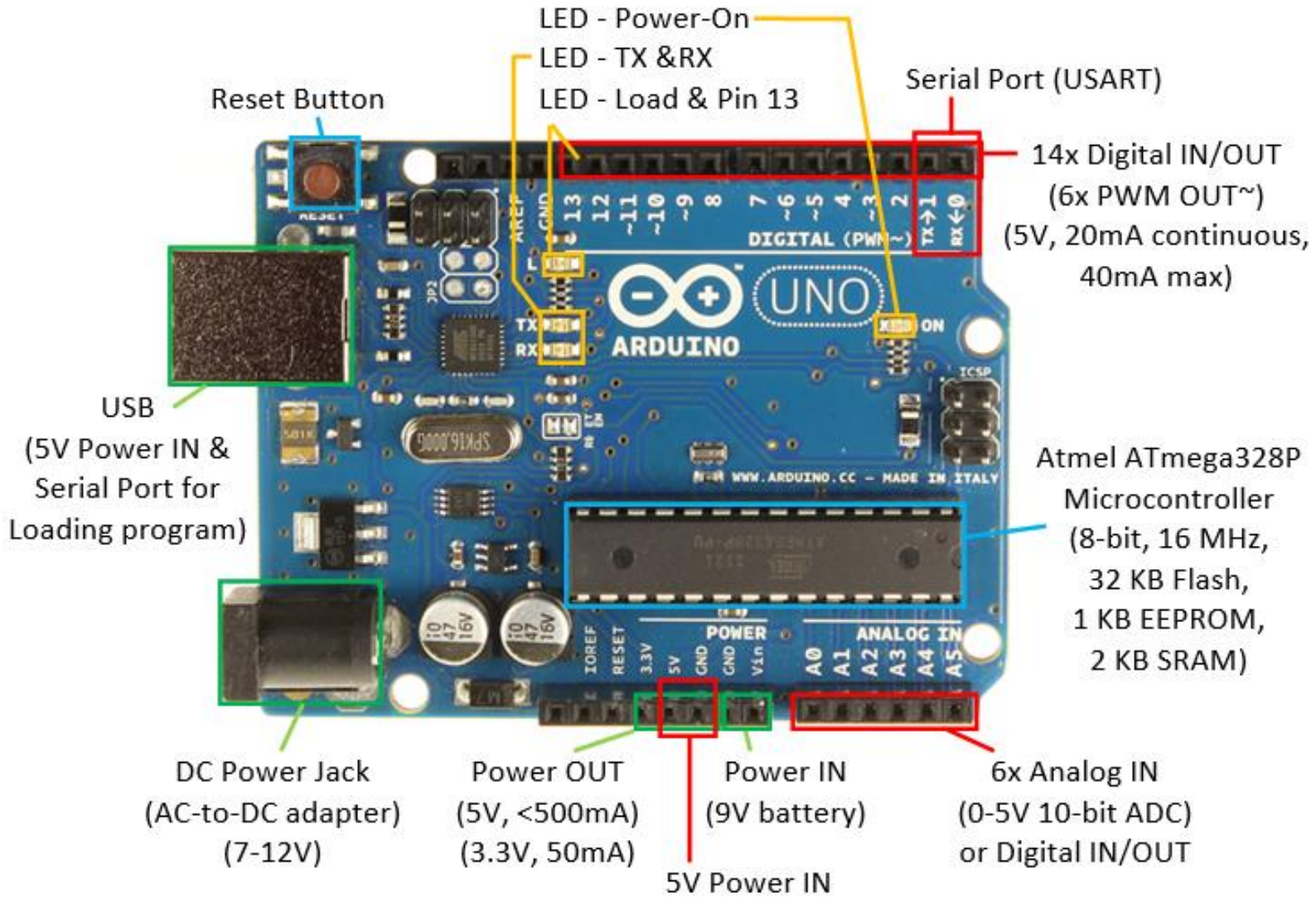
AVR = Alf and **V**egard's **R**ISC processor

Status Register

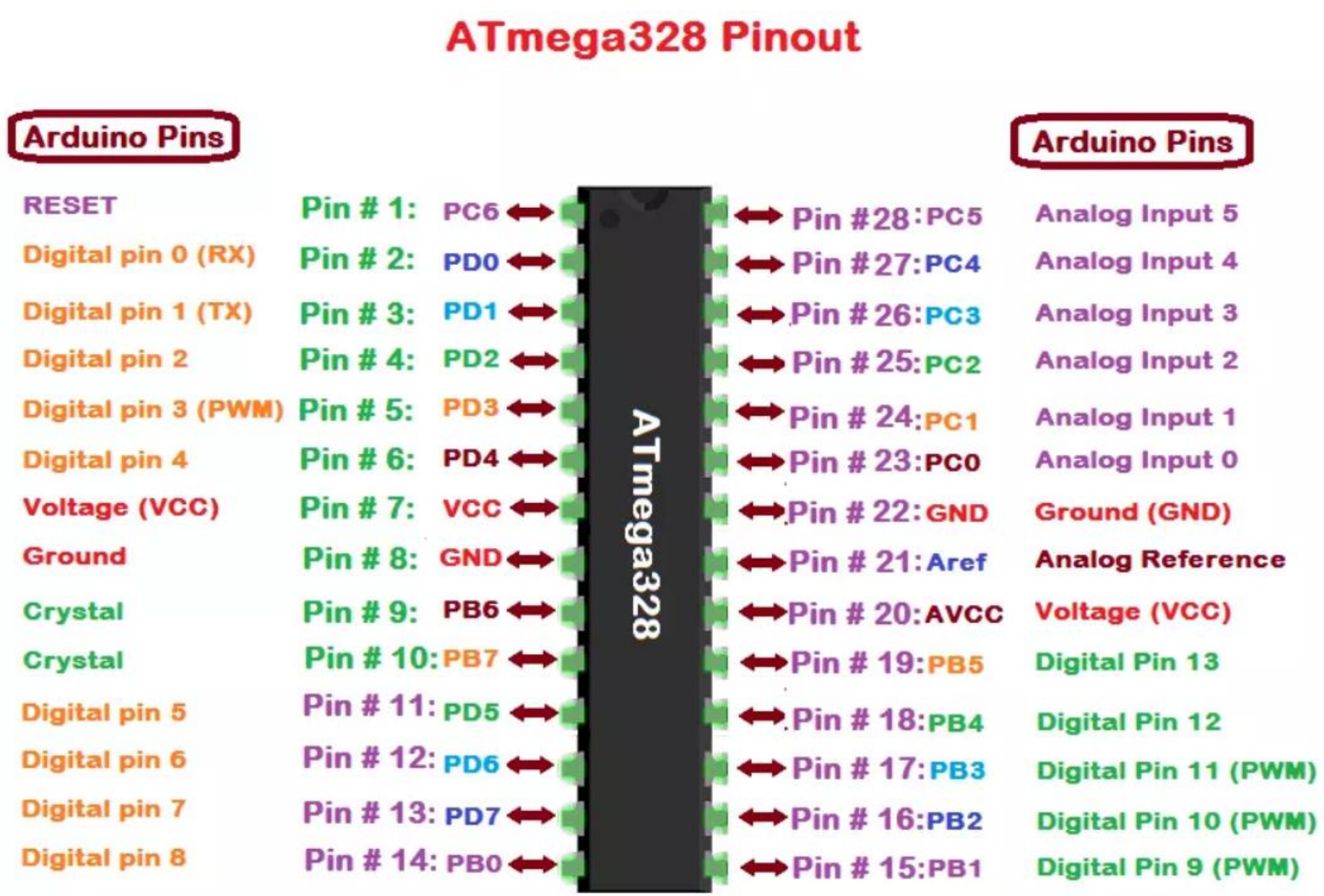
Bit	7	6	5	4	3	2	1	0	
0x3F (0x5F)	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- C = Carry Flag, This flag is set whenever there is a carry out from the D7 bit after an arithmetic operation(Addition, subtraction, increment, decrement etc). This flag bit is affected after an 8-bit addition or substruction.
- Z = Zero Flag, This flag is affected after an arithmetic or logic operation. If the result is zero than Z = 1, else Z = 0.
- N = Negative Flag, It reflects the result of an arithmetic operation. If the D7 bit of the result is zero then N = 0 and the result is positive. Else N = 1 and the result is negative.
- V = Overflow Flag,
- S = Sign Flag,
- H = Half Carry Flag, This bit is set if there is a carry from D3 to D4 bit after ADD or SUB instruction.
- T = Bit Copy Storage. Used as a temporary storage for bit. It can be used to copy a bit from a GPR to another GPR.
- I = Global Interrupt Enable

Overview of Arduino UNO Board



ATmega328P Pinout



Data Direction Register Method

To assign **input- 0**

To assign **output- 1**

DDRB= 0x 05;

Or **DDRB**= 0b 00000101; PB0 and PB2 are output pin while rest are input.

To write High-1

To write Low-0

PORTB= 0x01;

PORTB= 0b00000001; write PB0 as high.

DDRB Register

PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0	0	0	0	0	1	0	1

PORTB Register

PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0	0	0	0	0	0	0	1

Classification of Atmega328P Instructions

There are 141 instructions in the instruction set of Atmega328P. They are classified as —

1. Arithmetic and Logic Instructions.
2. Branch Instructions
3. Data Transfer Instructions
4. Bit and Bit Test Instructions
5. MCU Control Instructions

Instruction Type	No. of Instructions
Arithmetic	17
Shift and Rotate	5
Bit-wise Operations	12
Compare Operations	4
Branching	27
Subroutine Calls	6
I/O Instructions	6
Moving Data	29
SREG Bit Operations	18
Program Memory Instructions	11
MCU Control Instructions	6
Total	141

Instruction set summary

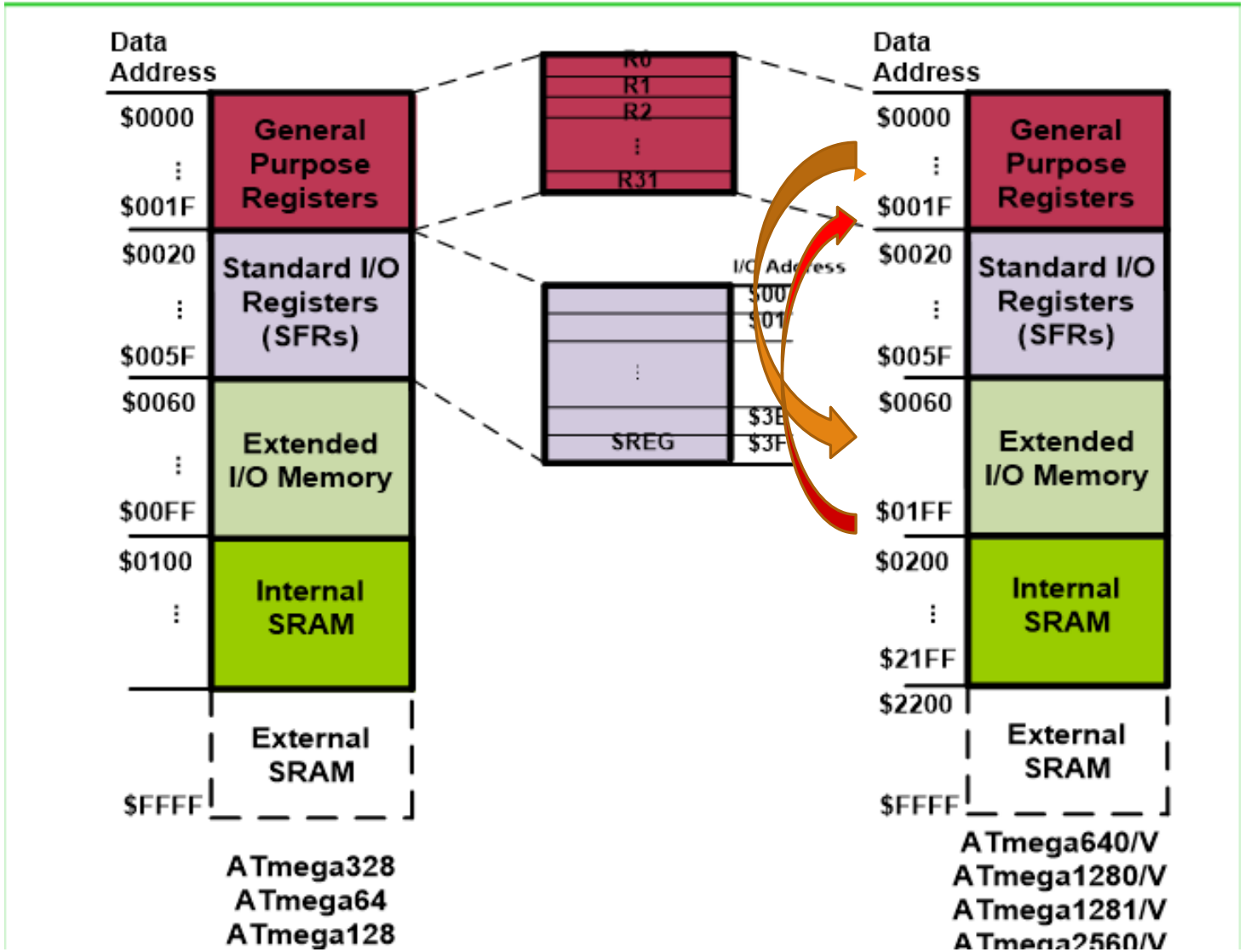
Mnemonics	Operands	Description	Operations	Flags	Clocks
ADD	Rd,Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd,Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
SUB	Rd,Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd,k	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
AND	Rd,Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
OR	Rd,Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 - Rd	Z,C,N,V,H	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd - 1	Z,N,V	1
MUL	Rd,Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2

Instruction set summary

Mnemonics	Operands	Description	Operations	Flags	Clocks
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space location k	Rd← [k]	None	1
IN	Rd, P	From In Port P/ address to Rd register	Rd ← P	None	1
OUT	P, Rr	From Rr register to Out Port P/ address	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
NOP		No Operation	None	1	
BREAK		Break	For On-chip Debug Only	None	N/A

Instruction set summary

Mnemonics	Operands	Description	Operations	Flags	Clocks
STS	k, Rr	Store Rr to data space location k.	k ← Rr	None	1
SBI	A, b	Sets a specified bit in an I/O Register	Sets the b no. bits of A register	None	1
CBI	A, b	Resets a specified bit in an I/O Register	Resets the b no. bits of A register	None	1
SBIC	A, b	Skip if Bit in I/O Register is Cleared/ Reset	If b no bit of A register is 0, then skip PC by 2 or 3.	None	1
SBIS	A, b	Skip if Bit in I/O Register is set	If b no bit of A register is 1, then skip PC by 2 or 3.	None	1
RJUMP	K	Relative jump	PC← PC+K+1	None	1



STS 0x60, R0

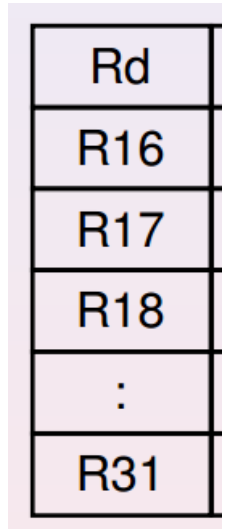
LDS R31, 0x01FF

Example of Instruction – LDI Rd,K

LDI Rd,K Operation: Rd ←K

Loads an 8-bit constant K directly into the register Rd.

Rd is any one of the registers from R16 to R31



Program Counter: PC ← PC+1

This instruction belongs to Data Transfer Group.

Status flags are not affected by any instruction in this group.

N.B: A program counter (PC) is a register in a computer processor that contains the address (location) of the instruction being executed at the current time

Example of Instruction – ADD Rd,Rr

ADD Rd,Rr Operation: Rd ←Rd + Rr

Adds two registers Rd and Rr and places the sum in the register Rd.

Rd and Rr can be any GPR

Program Counter: PC ← PC+1

This instruction belongs to Arithmetic Logical Group.

Flags Affected : All except I and T.

Rd or Rr
R0
R1
R2
R3
:
R31

Example of Instruction – JMP k

JMP k Operation: PC ←k

- Jump to an address within the entire program memory
- This is an unconditional jump instruction
- Program Counter: PC ← k
- This instruction belongs to Branch Group.
- Flags Affected : None

Example of Instruction – AND Rd,Rr

```
ldi r16, 0b10101010     ; Load binary value 10101010 into register r16
ldi r17, 0b11001100     ; Load binary value 11001100 into register r17

; Perform bitwise AND operation
and r16, r17            ; r16 = r16 & r17
```

```
10101010   ; Binary representation of r16
AND
11001100   ; Binary representation of r17
------------------
10001000   ; Result stored in r16
```

SBI DDRB, 3;

DDRB Register

PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0	0	0	0	0	1	0	0

CBI DDRB, 5;

DDRB Register

PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
1	1	1	0	1	1	1	1

SBIC R7, 5;

R7 Register

8	7	6	5	4	3	2	1
1	1	1	0	1	1	1	1

PC=PC+2 or 3

SBIS R8, 5;

R8 Register

PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0	0	0	1	0	0	0	0

PC=PC+2 or 3

Mnemonics	Operands	Description	Operations
STS	k, Rr	Store Rr to data space location k.	k ← Rr
SBI	A, b	Sets a specified bit in an I/O Register	Sets the b no. bits of A register
CBI	A, b	Resets a specified bit in an I/O Register	Resets the b no. bits of A register
SBIC	A, b	Skip if Bit in I/O Register is Cleared/ Reset	If b no bit of A register is 0, then skip PC by 2 or 3.
SBIS	A, b	Skip if Bit in I/O Register is set	If b no bit of A register is 1, then skip PC by 2 or 3.
RJUMP	K	Relative jump	PC← PC+K+1

Example: State the contents of R20, R21, and data memory location of 0x120 after the following program.

```
LDI R20, 5;
LDI R21, 2;
ADD R20,R21;
ADD R20,R21;
STS 0X120, R20;
```

Solution:

```
LDI R20, 5;          //R20=5
LDI R21, 2;          //R21=2
ADD R20,R21;         //R20=R20+R21=5+2=7
ADD R20,R21;         //R20= 7+2=9
STS 0X120, R20;      //0x120 = 9
```

R20= 9

R21= 2

0x120= 9

Example: State the contents of RAM location of $212, $213, $214, $215 and $216 after the following program.

```
LDI R16, 0x99
STS 0x212, R16
LDI R16, 0x85
STS 0x213, R16
LDI R16, 0x3F
STS 0x214, R16
LDI R16, 0x63
STS 0x215, R16
LDI R16, 0x12
STS 0x216, R16
```

Solution	
0x212	0x99
0x213	0x85
0x214	0x3F
0x215	0x63
0x216	0x12

Thank You