**American International University – Bangladesh**

**Faculty of Engineering**

**Department of Electrical and Electronic Engineering**

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| **Course Name:** | Microprocessor and Embedded Systems | **Course Code:** | | EEE 4103 |
| **Semester:** | Spring 23-24 | **Section:** | | F |
| **Faculty Name:** | Md Sajid Hossain | | | |
|  |  |  | |  |
| **Assignment No:** | 3 **(individual submission consisting of 30 marks)** | | | |
|  |  |  | |  |
| **Student Name:** | **TRIDIB SARKAR** | | | |
| **Student ID:** | **22-46444-1** | **Program Name:** | | **BSC in CSE** |
|  |  |  | |  |
| **[Sec: F]-Submission Link (MS forms):** [**https://forms.office.com/r/zurGRhwBMW**](https://forms.office.com/r/zurGRhwBMW)  **[Sec: Q]-Submission Link (MS forms):** [**https://forms.microsoft.com/r/T6ZX6zhpFu**](https://forms.microsoft.com/r/T6ZX6zhpFu) | | | | |
| **Submission Date:** | **06 May, 2024** | **Due Date:** | **EXAM DAY** | |

**Assessment Rubrics:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| COs-POIs | Excellent  [28-30] | Proficient  [25-27] | Good  [20-24] | Acceptable  [10-19] | Unacceptable  [1-9] | No Response  [0] | Secured Marks |
| **CO3**  **P.a.4.C.3** | All the problems are solved correctly. The simulation processes are clearly described, and results are generated by combining all possible input patterns with appropriate outcomes. All necessary drawings and computations are shown. | All the problems are solved correctly. The simulation processes are clearly described, and results are generated by combining all possible input patterns with appropriate outcomes. A few necessary drawings and computations are missing. | All the problems are solved correctly. The simulation processes are not clearly described, and results are generated by combining all possible input patterns with appropriate outcomes. Some necessary drawings and computations are missing. | All the problems are not solved correctly. The simulation processes are not clearly described, and results are generated by combining several wrong input patterns with inappropriate outcomes. Some necessary drawings and computations are missing. | All the problems are not solved correctly. The simulation processes are not described, and results are generated by combining mostly wrong input patterns with inappropriate outcomes. Almost all the necessary drawings and computations are missing. | No responses at all |  |
| **Comments** |  | | | | **Total marks (30)** |  | |

**Questions:**

1. Prepare a design of 2-bit ALU for the operations listed in Table 1 [10]

**Table 1:** For Questions 1 and 2 and 3

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Binary Code** | **Function of selection variables** | | | | | | |
| **A** | **B** | **F with**  **Cin = 1** | **F with**  **Cin = 0** | **D** | **H** |
| 0 0 0 | Input Data | Input Data | A+1 | A, C0 | None | 1’s to the output Bus |
| 0 0 1 | R1 | R1 | A, C1 | A-1 | R1 | Shift Right with IR=0 |
| 0 1 0 | R2 | R2 | A+B′+1 | A+B′ | R2 | - |
| 0 1 1 | R3 | R3 | A+B+1 | A+B | R3 | Circulate Left with Carry |
| 1 0 0 | R4 | R4 | A Ս B | A Ս B | R4 | 0’s to the output Bus |
| 1 0 1 | R5 | R5 | A′ | A′ | R5 | No Shift |
| 1 1 0 | R6 | R6 | A Ո B | A Ո B | R6 | Circulate Right with Carry |
| 1 1 1 | R7 | R7 | A XOR B | A XOR B | R7 | Shift Left with IL=0 |

1. Design a 3-bit shifter circuit for the listed shift functions provided in Table 1. [5]
2. Develop the control words in binary and hexadecimal formats using the information provided in Table 1 for the following micro-operations: [10]

|  |  |
| --- | --- |
| 1. R7R3+R4 | 1. R43(R4 0)/3 |
| 1. R3SHL R3 | 1. OutputR5 |
| 1. R5R1 | 1. R20 |
| 1. R6Input | 1. R6R4-R2 |
| 1. R2SHR R5 | 1. R3CRC R7 |

One example is shown as follows:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-operation | ***A*** | ***B*** | ***D*** | ***F*** | ***Cin*** | ***H*** | In Hex |
| R5🡨 CRC (R3+R4) | **011** | **100** | **101** | **011** | **0** | **110** | 72B6h |

The necessary bits for the control word are presented in Table 2.

**Table 2: 16-bit control word sequence**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| *A* | | | *B* | | | *D* | | | *F* | | | *Cin* | *H* | | |

1. Show the flow chart for *counting the number of 1’s* in register, R3, and storing the count in register R7. Assume that the starting address is 9. If register, R3 contains the data 10011011 then what would be the contents of register, R7 after this micro-operation is completed? [5]









