Review of Circuit theorems

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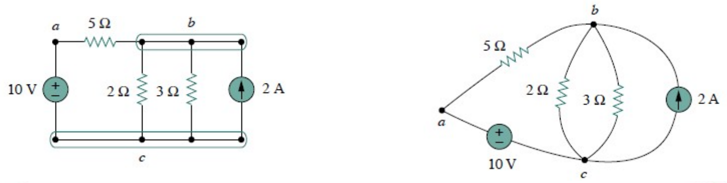
Recommended Text

- Alexander and Sadiku Fundamentals of Electric Circuits 4th Edition.

NODES, BRANCHES, AND LOOPS

A branch represents a single element such as a voltage source or a resistor.

A node is the point of connection between two or more branches.



A loop is any closed path in a circuit.

NODES, BRANCHES, AND LOOPS

- A loop is said to be *independent if it contains a* branch which is not in any other loop. Independent loops or paths result in independent sets of equations.
- Note, the closed path *abca containing the* 2Ω *resistor in* Fig. 1 is a loop. Another loop is the closed path *bcb containing the* 3Ω *resistor and the current source. Although one can identify six loops* in Fig. 1, only three of them are independent.
- A network with *b branches, n nodes, and l independent loops will* satisfy the fundamental theorem of network topology:

$$\boxed{b = l + n - 1}$$

NODES, BRANCHES, AND LOOPS

Two or more elements are in series if they are cascaded or connected sequentially and consequently carry the same current.
Two or more elements are in parallel if they are connected to the same two nodes and consequently have the same voltage across them.

KIRCHHOFF'S LAWS

- Ohm's law by itself is not sufficient to analyze circuits. Ohms law, with Kirchhoff's two laws, present a powerful set of tools for analyzing a large variety of electric circuits.
- KCL (based on the principle of conservation of charge)

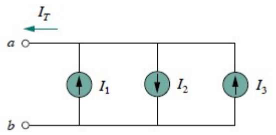
Kirchhoff's current law (KCL) states that the algebraic sum of currents entering a node (or a closed boundary) is zero.

$$\sum_{n=1}^{N} i_n = 0$$

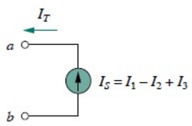
- where N is the number of branches connected to the node and in is the nth current entering (or leaving) the node. By this law, currents entering a node may be regarded as positive, while currents leaving the node may be taken as negative or vice versa

The sum of the currents entering a node is equal to the sum of the currents leaving the node.

KCL ILLUSTATED



$$I_T = I_1 - I_2 + I_3$$



KIRCHHOFF’S VOLTAGE LAW

- KVL (Based on the conservation of energy principle)

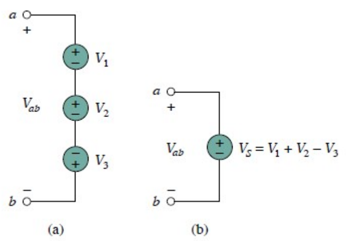
Kirchhoff’s voltage law (KVL) states that the algebraic sum of all voltages around a closed path (or loop) is zero.

$$\sum_{m=1}^{M} v_m = 0$$

- Where *M is the number of voltages in the loop (or the number of branches* in the loop) and v_m *is the mth voltage.*

KVL can be applied in two ways: by taking either a clockwise or a counterclockwise trip around the loop. Either way, the algebraic sum of voltages around the loop is zero.

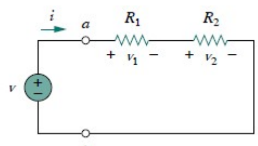
KVL ILLUSTRATED



Sum of voltage drops = Sum of voltage rises

SERIES RESISTORS AND VOLTAGE DIVISION

- Given a cct



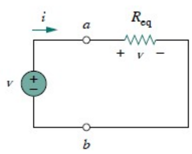
$v_1 = iR_1, \qquad v_2 = iR_2$

- Applying KVL to the loop (moving in the clockwise direction),

$$-v + v_1 + v_2 = 0$$

$$v = v_1 + v_2 = i(R_1 + R_2)$$

$$i = \frac{v}{R_1 + R_2} \quad => \quad v = iR_{eq}$$



The equivalent resistance of any number of resistors connected in series is the sum of the individual resistances.

VOLTAGE DIVISION

- Substituting

$$v = v_1 + v_2 = i(R_1 + R_2)$$

- In $v_1 = iR_1, \qquad v_2 = iR_2$

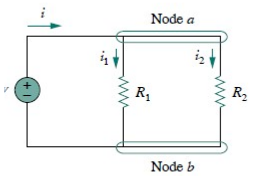
- We get $v_1 = \frac{R_1}{R_1 + R_2} v, \qquad v_2 = \frac{R_2}{R_1 + R_2} v$

- This is called the *principle of voltage division, and the* circuit just considered is called a *voltage divider. In general, if a voltage* divider has *N resistors ($R_1, R_2, \ldots, R_N$) in series with the source voltage v, the nth resistor (R_n) will have a voltage drop of*

$$v_n = \frac{R_n}{R_1 + R_2 + \cdots + R_N} v$$

PARALLEL RESISTORS AND CURRENT DIVISION

- A cct with parallel resistors,



$$v = i_1 R_1 = i_2 R_2$$

$$i_1 = \frac{v}{R_1}, \qquad i_2 = \frac{v}{R_2}$$

Applying KCL at node a gives the total current i as

$$i = i_1 + i_2$$

Substituting Eq.

$$i = \frac{v}{R_1} + \frac{v}{R_2} = v\left(\frac{1}{R_1} + \frac{1}{R_2}\right) = \frac{v}{R_{eq}}$$

where R_{eq} is the equivalent resistance of the resistors in parallel:

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2}$$

or

$$\frac{1}{R_{eq}} = \frac{R_1 + R_2}{R_1 R_2}$$

or

$$\boxed{R_{eq} = \frac{R_1 R_2}{R_1 + R_2}}$$

Current Divider

The equivalent resistance of two parallel resistors is equal to the product of their resistances divided by their sum.

$$v = iR_{eq} = \frac{iR_1R_2}{R_1 + R_2} \qquad i_1 = \frac{v}{R_1}, \qquad i_2 = \frac{v}{R_2}$$

Combining Eqs.

$$\boxed{i_1 = \frac{R_2\, i}{R_1 + R_2}, \qquad i_2 = \frac{R_1\, i}{R_1 + R_2}}$$

Home work

- Read the recommended textbooks discussion on short ccts and open ccts!
- Study relevant examples and attempt practice problems.

CIRCUIT THEORY FUNDAMENTALS

1ST
- OHMS LAW
- V=IR

2ND
- CIRCUIT LAWS
- KCL/KVL
- CURRENT & VOLTAGE DIVIDER

3RD
- METHODS OF ANALYSIS
- MESH/NODAL

4^{TH}
- CIRCUIT THEOREMS
- SUPERPOSITION, MILLMANS, THEVENIN, NORTON'S, SOURCE TRANSFORMATION, MPT

DUALITY

- The concept of duality is a time-saving, effort-effective measure of solving circuit problems. Duality takes its name from dual, meaning double, two or something in two parts.
- Merriam-Webster defines duality as: The quality or state of having two different or opposite parts or elements.
- Electronic circuits have been observed to exhibit duality. Particularly in circuit analysis, two different circuits could have the same equations and solutions, except that the roles of certain complementary elements are interchanged.
- This **interchangeability** is known as the principle of *duality.*

Duality in Circuits

The duality principle asserts a parallelism between pairs of characterizing equations and theorems of electric circuits.

DUAL PAIRS	
Resistance R	*Conductance* G
Inductance L	*Capacitance* C
Voltage v	*Current* i
Voltage source	Current source
Node	Mesh
Series path	Parallel path
Open circuit	Short circuit
KCL	KVL
Thevenin	Nortons

Two circuits are said to be duals of one another if they are described by the same characterizing equations with dual quantities interchanged.

''The usefulness of the duality principle is self-evident. Once we know the solution to one circuit, we automatically have the solution to the dual circuit.''
Note, not all element or variables have duals. Linearity is required for duality to hold i.e. power (non linear) has no dual. Despite being linear, mutual inductance too has no dual! The circuits must be planar too!