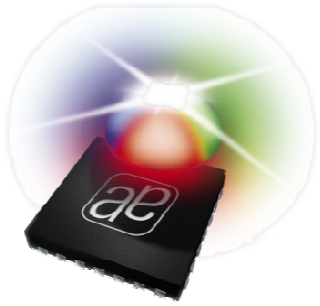
AS3695A

16 channel white LED driver for LCD backlight

Product Specification, Confidential



General Description

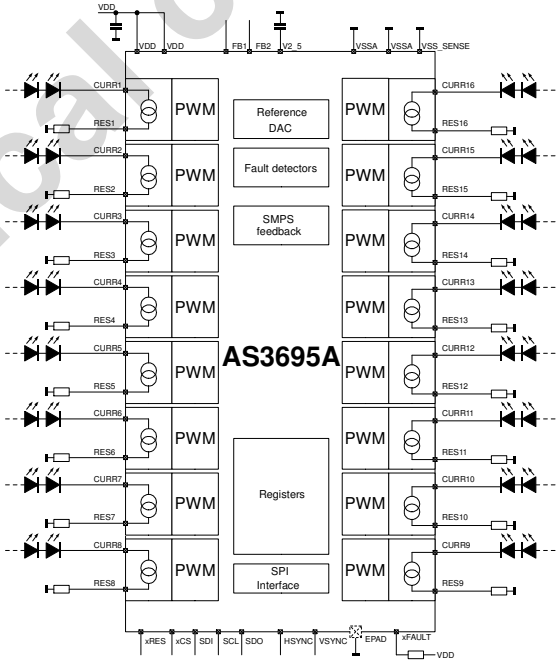
The AS3695A is a 16 channels precision LED driver for use in LCD-backlight panels.
Dynamic power feedback controls the external power supply to guarantee best efficiency. Build in safety features include thermal shutdown as well as open and short LED detection. The device is programmable via serial interface.

- 16 Channel LED driver
- Output voltage max. 30V
- Output current 120mA
- Linear current setting using 10-bit DAC
- Current accuracy ±0.5% @ VDAC=250mV
- Channel to Channel current accuracy ±0.2%
- Output slew rate programmable
- Current programmable with external resistor
- Digital current control with 16 independent PWM generators
- Free programmable 12 bit resolution (period, high time and delay)
- PWM-generator clock
  - Internal RC-oscillator
  - External Clock
- H-Sync, V-Sync inputs to synchronize with TV-set
- Direct PWM mode
- Undervoltage detection (open LED)
- Undervoltage auto-turnoff
- Overvoltage detection (short LED)
- Overvoltage auto-turnoff
- Temperature shutdown
- Register lock/unlock function
- Fault interrupt output
- 2 configurable supply regulation feedback outputs
- SPI interface
- 6kV ESD at current sink inputs
- 2kV ESD an all other pins
- Package QFN48 7x7mm, 0.5mm pitch

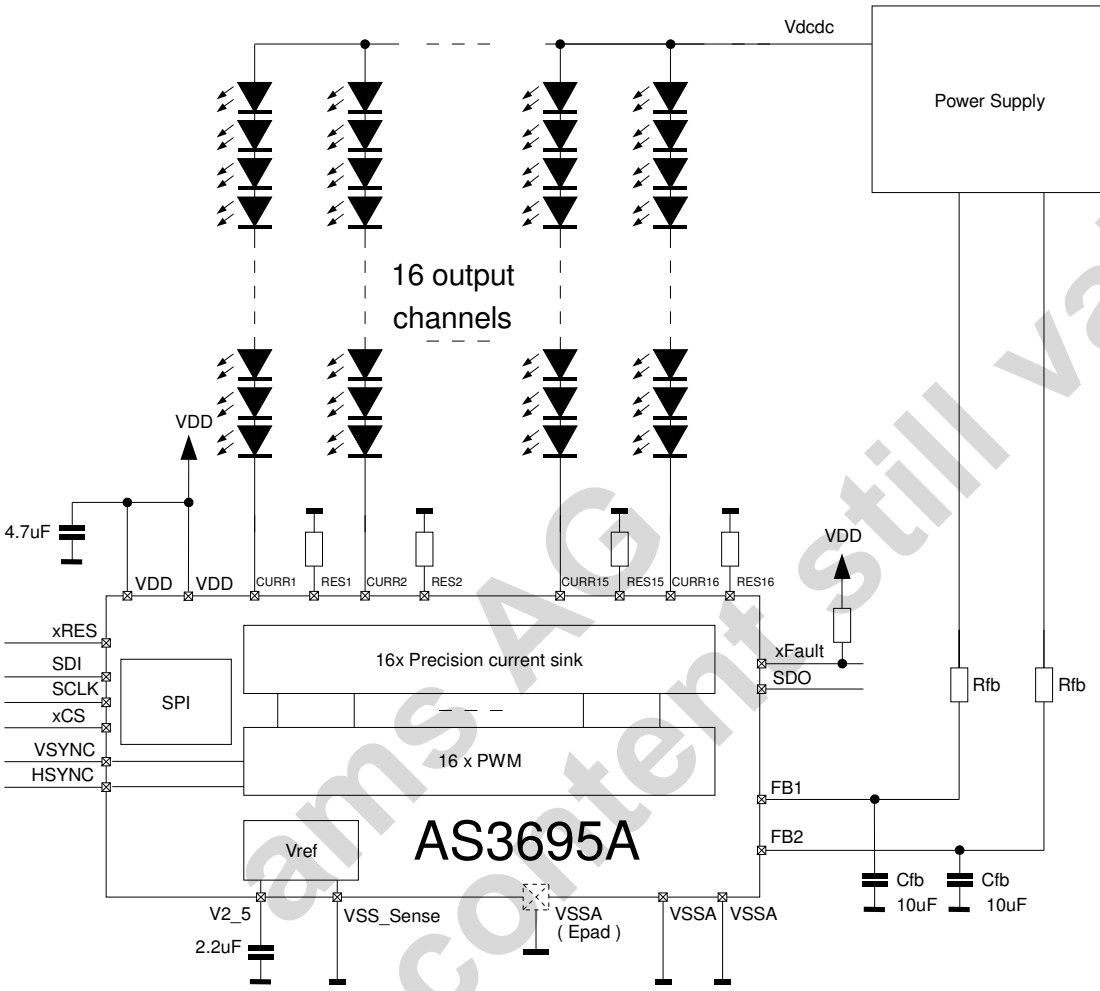
Applications

LED backlighting for LCD – TV sets and monitors

1 Block diagram



2 Typical application



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in Section "Electrical Characteristics" is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit	Note
V_{DDMAX}	Supply voltage	-0.3	7	V	Applicable for pin VDD
V_{IN_5V}	Maximum voltage	-0.3	VDD +0.3V	V	Applicable for 5V pins (1)
V_{IN_30V}	Maximum voltage	-0.3	30	V	Applicable for 30V pins (2)
I_{latch}	Latch-Up immunity	-100	+100	mA	Norm: EIA/JESD78
T_{STRG}	Storage Temperature Range	-55	150	°C	Maximum Junction Temperature
	Humidity	5	85	%	Non condensing
V_{ESD_LV}	Electrostatic Discharge on all 5V pins (1)	-2000	2000	V	Norm: MIL 883 E Method 3015 Human body model
V_{ESD_HV}	Electrostatic Discharge on 30V pins (2) against GND	-6000	6000	V	Norm: MIL 883 E Method 3015 Human body model
T_{BODY}	Body Temperature during Soldering		260	°C	according to IPC/JEDEC J-STD-020C

Note: (1) Pins xRES, SDI, SCLK, SDO, xCS, VSYNC, HSYNC, VDD, xFault, FB1, FB2, RES1-RES16, V2_5
(2) Pins CURR1 – CURR16

3.2 Operating Conditions

3.2.1 General

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Rthja	Thermal resistance junction – ambient	QFN48		30		°C/W
Tcase	Case Temperatur		-20		85	°C
Tj	Junction Temperature		-20		115	°C

3.2.2 Power supply

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Supply Voltage		4.0		5.5	V
VDD_POR	Power on reset level	Circuit stays in power down until VDD_POR is reached.	2.4		2.9	V
IDD_q	Quiescent current	VDD= 5V, Default setting, PWM = 0		20		mA
IDD_r	Supply current	VDD = 5V, HSYNC = 1MHz, Duty = 50%		30		mA
V2_5	Voltage regulator output			2.5		V

3.2.3 Current outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vcurrx	Output voltage pins CURRx				30	V
Icurrx	Output current	VDAC = 0.25V Vcurr = 0.6V			120	mA
Rcurrx	Input resistance in CURRx	PWM = 0 PWM = 1	10 0.1			MΩ MΩ
IResx	Input current pin RESx	URESx = 0.5V URESx = 0.8V			10 100	uA
Iled_250	Trimmed Current accuracy	Trimmed during production ILED =100mA, Temp = 25°C, DACref=800mV, VDAC = 250mV (1) (excluding error of external Rset)	-0.5		+0.5	%
Iled_all FET	Current accuracy External FET	Temp = 25°C, DACref=800mV, VDAC = 200mV to 800mV (2) (excluding error of external Rset)	-1.4		+1.4	%
Ich_250	Channel to channel Current accuracy	ILED =100mA, Temp = 25°C, DACref=800mV, VDAC = 250mV(1) (excluding error of external Rset)		0.2		%
Iled_all FET	Current accuracy	Tjunction = -20°C to +100°C, DACref=800mV, VDAC = 200mV to 800mV (2) (excluding error of external Rset)	-1.5		+1.5	%

Note: (1) It is recommended to use DACref = 800mV in order to achieve specified accuracy
(2) It is not recommended to use DAC-voltages < 200mV in order to minimize influences from PCB-layout and noise.

3.2.4 Feedback circuit, fault detectors

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IFBmax	Feedback current maximum			200		uA
RFBmin	Minim output resistance	VCURRx = 0.2V		200	500	Ω
IFB_g	FB transconductance	IFB_g = ΔI_{FB}/ ΔV_{CURRx}		-2		mA/V
VFB	Feedback voltage trip point	Programmable, Tolerance ±10%		0.6 0.8 1.0 VDAC +0.35		V
Vshort	Short LED detection voltage at Pin Dx	Programmable, Tolerance ±1.2V		2 3 4 5 6 7 8 9 10 11 12		V V V V V V V V V V V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vopen	Open LED detection Voltage at Pin Sx	Programmable, Tolerance ±10%		50 100 200 VDAC/2		mV mV mV V
Tovtemp	Over temperature limit		130	140	150	℃
Thyst	Over termperature hysteresis			10		℃

3.2.5 PWM-generators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Internal Clock for PWM		400	500	600	kHz
f_{HSYNC}	HSYNC frequency		100		2000	kHz
f_{VSYNC}	VSYNC frequency		60		480	Hz

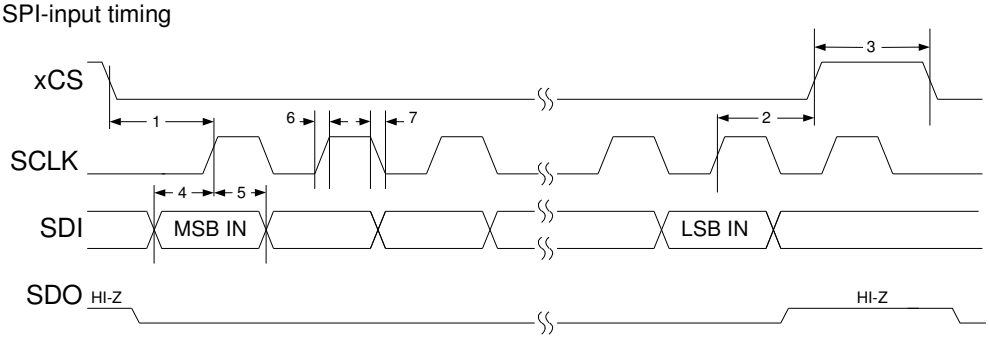
3.2.6 Digital pins

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{IH}	High Level Input voltage	1.3		VDD	V	
V_{IL}	Low Level Input voltage	-0.3		0.8	V	
VoH	High Level output voltage	VDD-0.3			V	I=mA
VoL	Low Level output voltage			VDD-0.3	V	I=mA
VoL_PD	Low level output voltage open drain outputs			VDD-0.3	V	I=mA
R_pu	Input resistance PullUp inputs		300		kΩ	
R_pd	Input resistance PullDown inputs		300		kΩ	

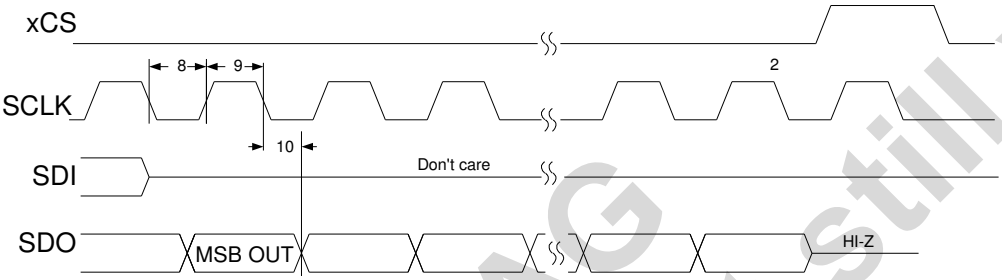
3.2.7 SPI-timings

Symbol	Parameter	Min	Typ	Max	Unit	Note
fsclk	SCLK frequency	0		10	MHz	
t1	xCS setup time	50			ns	
t2	xCS hold time	100			ns	
t3	xCS disable time	100			ns	
t4	SDI setup time	5			ns	
t5	SDI hold time	5			ns	
t6	SCLK rise time	5			ns	
t7	SCLK fall time	5			ns	
t8	SCLK low time	40			ns	
t9	SCLK high time	40			ns	
t10	output valid from SCLK low	10			ns	

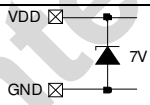
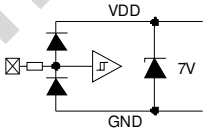
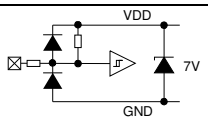
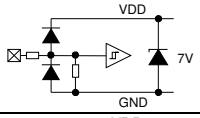
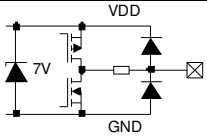
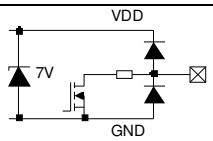
SPI-input timing



SPI-output timing

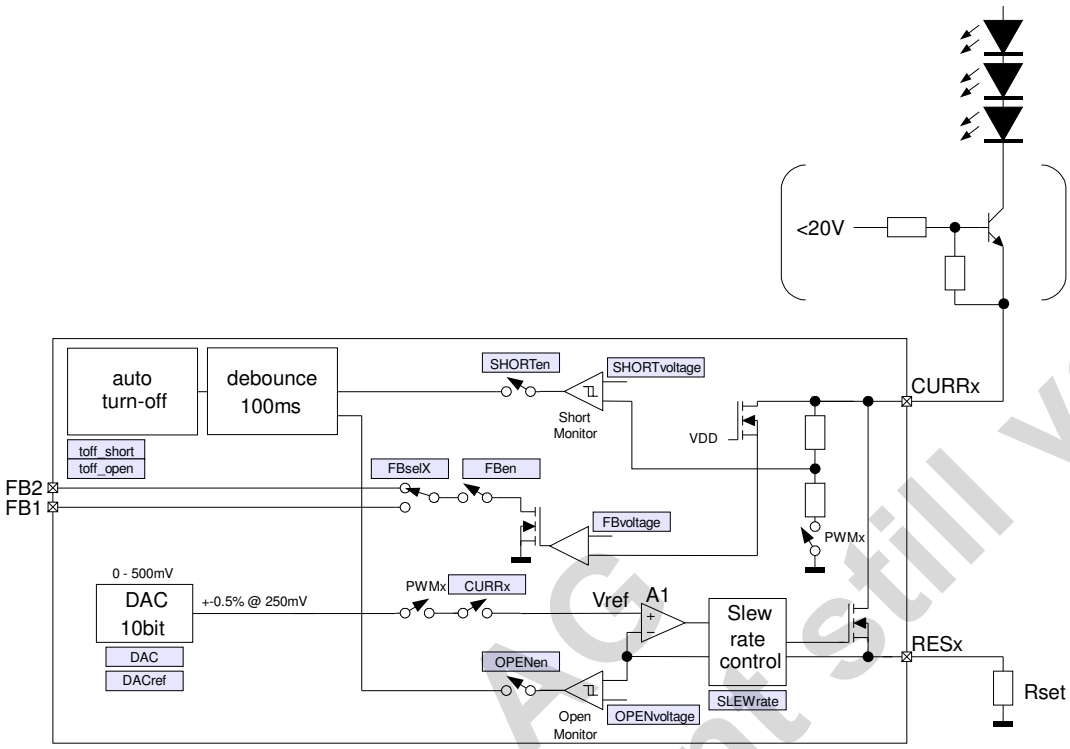


3.3 Pins equivalent circuit

VDD	
Digital inputs	
Digital inputs Pull up	
Digital inputs Pull Down	
Digital outputs push/pull	
Digital output open drain	

4 Detailed Block description

4.1 Current outputs



16x Precision current sink

4.1.1 Precision current sink

All current sinks are built with an internal error amplifier A1 and an internal power transistor. For low EMI radiation the slew rate of the amplifier output voltage can be adjusted between 1us and 9us

4.1.2 Power supply feedback

The voltage on the pins “CURRx” is monitored to adjust the DCDC output voltage. If this voltage is lower than “FBvoltage” a comparator turns on a NMOS transistor which is able to control the output voltage of the external power supply via pin FB1 or pin FB2. The feedback comparator can be assigned to either FB1 or FB2. The power supply feedback can be turned off for all channels by the flag “FBen”. If an output is turned off with the corresponding bit in the CUR_ON_1/2 -registers, the feedback function of this output is also automatically turned off.

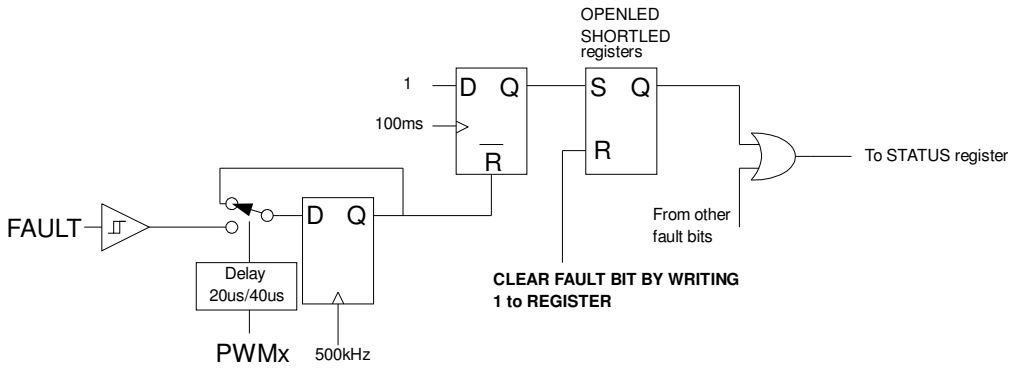
4.1.3 Open LED detection

If a LED-string is broken the voltage at the current setting resistor goes below “OPENvoltage”. This status is detected by a comparator and if this status lasts longer than 100ms a fault is indicated and optionally the output and the corresponding power feedback function is turned off. This feature can also be used for external resistor short detection during production. For proper detection the PWM high time has to be longer than 50us.

4.1.4 Short LED detection

Shorted LEDs in a LED-string will cause higher voltage at pin “CURRx”. A higher voltage during PWM=1 is detected by a comparator and will trigger a “short LED detection” fault. The duration of the fault is accumulated and if the time exceeds 100ms a fault is indicated and optionally the output is turned off. If the high-time of the waveform is shorter than 100ms it will take more periods to trigger this fault. For proper detection the PWM high time has to be longer than 50us.

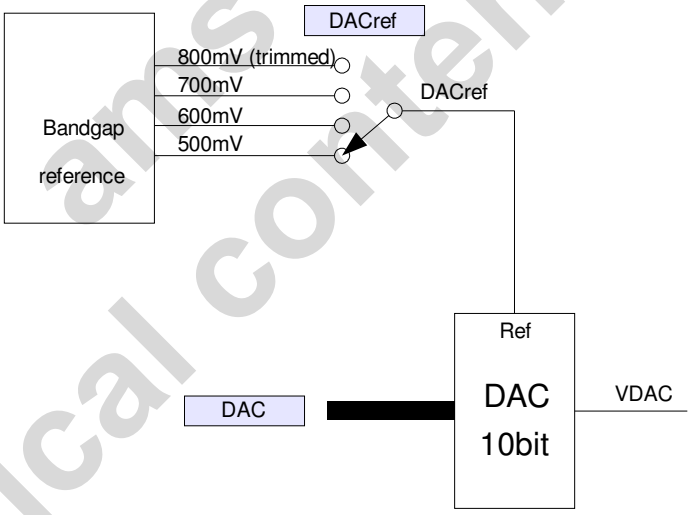
4.1.5 Fault detection



If a Open-LED or Short-LED condition is detected the fault-signal is debounced with an internal 100ms clock. This means that the fault will be indicated in the OPENLED or SHORTLED registers between 100ms and 200ms. In order to clear the bit in these registers a “1” has to be written.

4.1.6 DAC

The reference voltage for the output stage is generated by an internal 10-bit DAC. The DAC reference can be selected between 500mV and 800mV depending on register settings. The DAC is trimmed during production with DACref = 800mV to guarantee an output current accuracy of ±0.5% on every current output.



The DAC output voltage can be calculated with:

$$VDAC = \frac{DACref}{1024} * DAC$$

DAC...10bit data value
DACref...DAC reference voltage 500mV to 800mV

4.1.7 Registers in current output stage

RegAddr: 0x01		CUR_ON_1		
Bit	Name	Description	Default	Access
7:0	CURR1 - CURR8	Enables or disables current outputs 0...output OFF. Pulldown resistor to GND 1...output ON.	00000000	r/w

RegAddr: 0x02		CUR_ON_2		
Bit	Name	Description	Default	Access
7:0	CURR9 - CURR16	Enables or disables current outputs 0...output OFF. Pulldown resistor to GND 1...output ON.	00000000	r/w

RegAddr: 0x03		Fault_1		
Bit	Name	Description	Default	Access
7:3		Not used	00000	r/w
2	Toff_OverT	Automatic Output turn off at overtemperture 0...Do not turn off current outputs on overtemperature 1... Turn off current outputs on overtemperature	1	r/w
1	Toff_Short	Automatic Output turn off on short LED detection 0...Do not turn off current outputs on on short LED detection 1... Turn off current outputs on short LED detection	0	r/w
0	Toff_Open	Automatic Output turn off on open LED detection 0...Do not turn off current outputs on on open LED detection 1... Turn off current outputs on open LED detection	0	r/w

RegAddr: 0x04		Fault_2		
Bit	Name	Description	Default	Access
7:6	OPENvoltage	Trigger voltage for OPEN LED detection 00...50mV 01...100mV 10...200mV 11...VDAC/2	00	r/w
5:2	SHORTvoltage	Trigger voltage for SHORT LED detection 0000...2V 0001...3V 0010...4V 0011...5V 0100...6V 0101...7V 0110...8V 0111...9V 1000...10V 1001...11V 1010...12V 1011 to 1111 ...**do not use**	0000	r/w
1	SHORTen	Enable short LED detection 0...SHORT detection OFF 1...SHORT detection ON	0	r/w
0	OPENen	Enable open LED detection 0...OPEN detection OFF 1...OPEN detection ON	0	r/w

RegAddr: 0x05		Feedback		
Bit	Name	Description	Default	Access
7:6		Not used	00	r/w
5:4	FBvoltage	Feedback regulator trip voltage.This voltage has to be adjusted if current is larger than 70mA or VDAC is higher than 0.25V 00...0.6V 01...0.8V 10...1.0V 11...V-DAC + 0.35V	00	r/w

3	FBboost	Feedback boost option. **FUNCTION DISABLED**	0	r/w
2		Not used	0	r/w
1		Not used	0	r/w
0	FBen	Enable Feedback function for all current outputs. 1...Feedback function enabled 0...Feedback function disabled Note: If a current output is disabled its Feedback function is automatically disabled.	0	r/w

RegAddr: 0x06		**FB_SEL1**		
Bit	**Name**	**Description**	**Default**	**Access**
7:0	FBsel 1 - 8	Select FB-channel for current outputs 1 to 8 0...select FB channel FB1 1... select FB channel FB2	00000000	r/w

RegAddr: 0x07		**FB_SEL2**		
Bit	**Name**	**Description**	**Default**	**Access**
7:0	FBsel 9 - 16	Select FB-channel for current outputs 9 to 16 0...select FB channel FB1 1... select FB channel FB2	00000000	r/w

RegAddr: 0x08		**CURRctrl**		
Bit	**Name**	**Description**	**Default**	**Access**
7:6		Not used.	00	r/w
5:4	DACref	DAC reference voltage 00...500mV 01...600mV 10...700mV 11...800mV this reference is used at factory trimming	00	r/w
3:2		Not used	00	r/w
1:0	SLEWrate	Select slew rate of output drivers 00...9us 01...6us 10...3us 11...1us	00	r/w

RegAddr: 0x09		**SHORTLED1**		
Bit	**Name**	**Description**	**Default**	**Access**
7:0	SHORTLED 1 - 8	Indicates short LED condition on outputs 1 to 8 0...no short LED detected 1... short LED detected	0000000	r/w

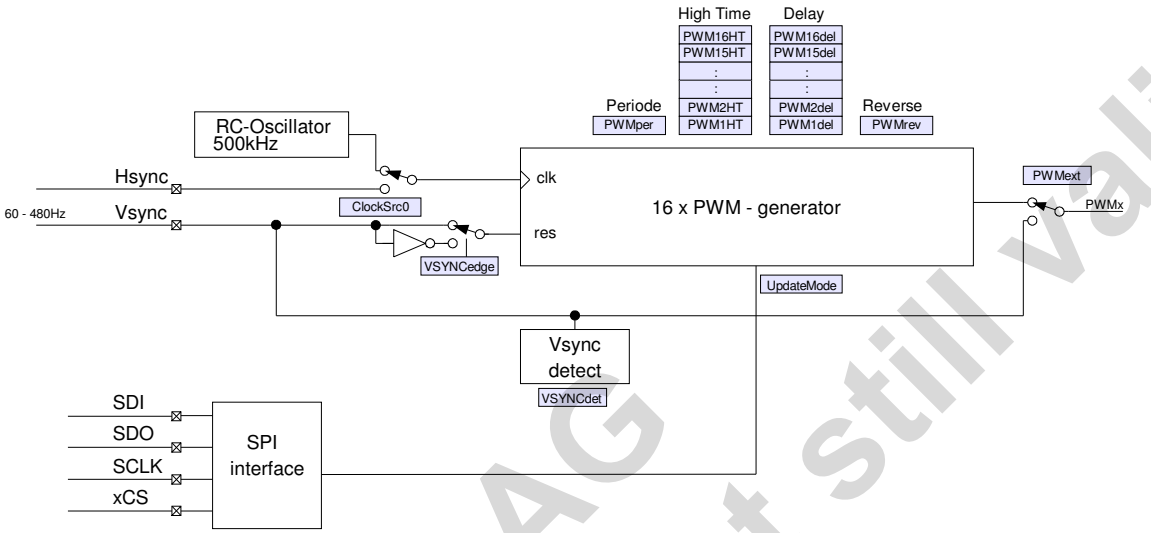
RegAddr: 0x0A		**SHORTLED2**		
Bit	**Name**	**Description**	**Default**	**Access**
7:0	SHORTLED 9 - 16	Indicates short LED condition on outputs 9 to 16 0...no short LED detected 1... short LED detected	0000000	r/w

RegAddr: 0x0B		**OPENLED1**		
Bit	**Name**	**Description**	**Default**	**Access**
7:0	OPENLED 1 - 8	Indicates open LED condition on outputs 1 to 8 0...no open LED detected 1... open LED detected	0000000	r/w

RegAddr: 0x0C		**OPENLED2**		
Bit	**Name**	**Description**	**Default**	**Access**
7:0	OPENLED 9 - 16	Indicates open LED condition on outputs 9 to 16 0...no open LED detected 1... open LED detected	0000000	r/w

RegAddr:		DAC		
0x0E	0x0D			
Bit	Bit	Description	Default	Access
1:0	7:0	DAC[9:0] defines DADC output voltage **DACvoltage = DAC[9:0]*DACref/1024**	1000000000	r/w

4.2 PWM-generators

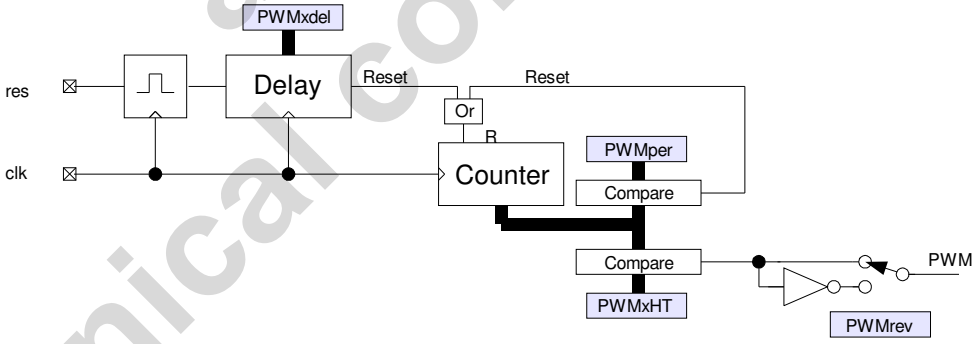


4.2.1 Clock and reset

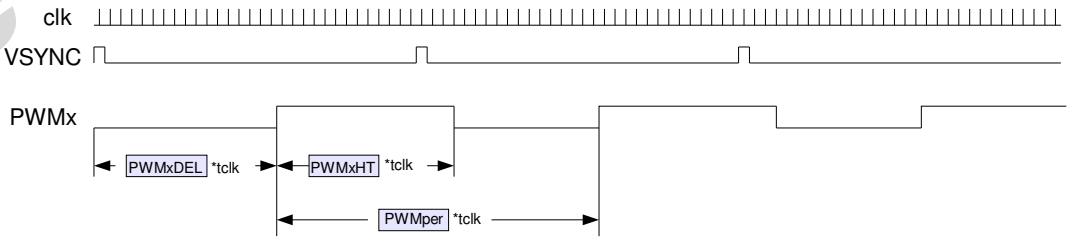
The clock for the build in PWM-generators can be one of two different sources.

1. Internal RC oscillator with 500KHz +-20%
2. External Clock signal. This is usually the HSYNC signal of the TV.

4.2.2 PWM-counter



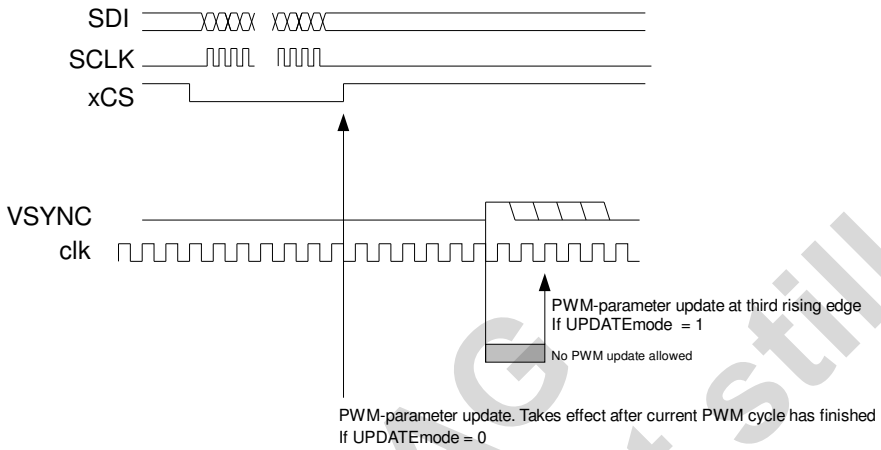
Each PWM-generator is build with a 12bit counter and digital comparators. The counter is counting up with t_{clk} until the value stored in “PWMper” is reached. This resets the counter and starts the next period. While the counter value is below “PWMxHT” the PWM-singal is “1”, the rest of the period the PWM-signal is “0”. The output of each PWM-generator can also be inverted by means of the “PWMrev”.



4.2.3 SPI data update, UPDATEmode bit

The PWM-settings that are programmed via the SPI-Interface take effect depending on the status of the “UPDATEmode”-bit.

If UPDATEmode =1 new data from the serial interface are stored at the next rising edge of VSYNC
If UPDATEmode =0 new data from the serial interface are stored immediately after xCS goes high and will take effect after current PWM cylce is finished. In this mode the values in the PWMxdel registers are ignored. There will be no Delay on the PWM signals.



The PWMxHT-values are double buffered. HighTime values for the next VSYNC can be written even when the current HighTime is not finished.

4.2.4 PWM direct control

The internal signals PWMx can also be direct applied at the VSYNC input if the bit PWMext=1.

4.2.5 VSYNC detect

The VSYNCdet=1 the VSYNC detector monitors the presence of a VSYNC signal. If If the VSYNC signal is missing for more than 100ms the current outputs are temporary turned off.

4.2.6 VSYNC duration

Since the VSYNC input is connected to an edge detector, there is no restriction on the duration of the VSYNC pulse.

4.2.7 Registers in PWM-generators

RegAddr: 0x11		PWMREV1		
Bit	Name	Description	Default	Access
7:0	PWMrev 1 - 8	Selects PWM inverted operation for outputs 1 to 8 0...PWM normal 1... PWM inverted	00000000	r/w

RegAddr: 0x12		PWMREV2		
Bit	Name	Description	Default	Access
7:0	PWMrev 9 - 16	Selects PWM inverted operation for outputs 9 to 16 0...PWM normal 1... PWM inverted	00000000	r/w

RegAddr: 0x13		PWMCTRL		
Bit	Name	Description	Default	Access
7	FaultDetDly	Sets delay time between PWM=1 and fault detection start 0...40us 1...20us	0	r/w
6	DelayStart	Defines when new PWM-Delay value takes effect 0...Delay values are updated every VSYNC pulse 1...Delay values are updated on the next VSYNC pulse only if HighTime or Delay value has been changed.	0	r/w
5			0	r/w
4	VSYNCdet	Enable VSYNC detection 0...VSYNC-detection OFF 1... VSYNC-detection ON. All current outpts are turned off if VSYNC signal is missing for 100ms	0	r/w
3	VSYNCedge	Defines VSYNC trigger edge 0...VSYNC trigger on rising edge 1...VSYNC trigger on falling edge	0	r/w
2	PWMext	Select external or internal PWM signal 0...PWM signal is generated internally 1...PWM signal is applied externally at pin VSYNC	0	r/w
1	UpdateMode	Defines when internal registers are updated 0...Registers updated with rising edge of xCS 1...Registers updated with next VSYNC-edge	0	r/w
0	ClockSrc0	Clock source for internal PWM-generators 0..internal RC oscillator 1...External Pin HSYNC	0	r/w

RegAddr:		PWMperiod		
0x15	0x14			
Bit	Bit	Description	Default	Access
3:0	7:0	PWMper[11:0] sets PWM period	0x00, 0x00	r/w

RegAddr:		PWM1delay		
0x17	0x16			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM1del[11:0] sets PWM1 delay	0x00, 0x00	r/w

RegAddr:		PWM2delay		
0x19	0x18			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM2del[11:0] sets PWM2 delay	0x00, 0x00	r/w

RegAddr:		PWM3delay		
0x1B	0x1A			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM3del[11:0] sets PWM3 delay	0x00, 0x00	r/w

RegAddr:		PWM4delay		
0x1D	0x1C			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM4del[11:0] sets PWM4 delay	0x00, 0x00	r/w

RegAddr:		PWM5delay		
0x1F	0x1E			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM5del[11:0] sets PWM5 delay	0x00, 0x00	r/w

RegAddr:		PWM6delay		
0x21	0x20			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM6del[11:0] sets PWM6 delay	0x00, 0x00	r/w

RegAddr:		PWM7delay		
0x23	0x22			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM7del[11:0] sets PWM7 delay	0x00, 0x00	r/w

RegAddr:		PWM8delay		
0x25	0x24			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM8del[11:0] sets PWM8 delay	0x00, 0x00	r/w

RegAddr:		PWM9delay		
0x27	0x26			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM9del[11:0] sets PWM9 delay	0x00, 0x00	r/w

RegAddr:		PWM10delay		
0x29	0x28			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM10del[11:0] sets PWM10 delay	0x00, 0x00	r/w

RegAddr:		PWM11delay		
0x2B	0x2A			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM11del[11:0] sets PWM11 delay	0x00, 0x00	r/w

RegAddr:		PWM12delay		
0x2D	0x2C			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM12del[11:0] sets PWM12 delay	0x00, 0x00	r/w

RegAddr:		PWM13delay		
0x2F	0x2E			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM13del[11:0] sets PWM13 delay	0x00, 0x00	r/w

RegAddr:		PWM14delay		
0x31	0x30			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM14del[11:0] sets PWM14 delay	0x00, 0x00	r/w

RegAddr:		PWM15delay		
0x33	0x32			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM15del[11:0] sets PWM15 delay	0x00, 0x00	r/w

RegAddr:		PWM16delay		
0x35	0x34			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM16del[11:0] sets PWM16 delay	0x00, 0x00	r/w

RegAddr: 0x36		LOCKUNLOCK		
Bit	Name	Description	Default	Access
7:0	LOCKUNLOCK	MagicByte to lock and unlock writing and reading of registers **Writing into register:** 0xC**X**...unlock register Group1. Writing enabled 0x**X**A...unlock register Group2. Writing enabled 0xCA...unlock register Group1 and Group2. Writing enabled 0xA**X**...lock register Group1. Writing disabled 0x**X**C...lock register Group2. Writing disabled 0xAC...lock register Group1 and Group2. Writing disabled **X**...don't care. All other values do not change the status of lockunlock. **Reading from register:**	0x00	r/w

		0x00.... Group1 and Group2 are locked 0x01...Group1 is unlocked 0x02...Group2 is unlocked 0x03...Group1 and Group2 are unlocked		

RegAddr:		PWM1hightime		
0x38	0x37			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM1HT[11:0] sets PWM1 high time	0x00, 0x00	r/w

RegAddr:		PWM2hightime		
0x3A	0x39			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM2HT[11:0] sets PWM2 high time	0x00, 0x00	r/w

RegAddr:		PWM3hightime		
0x3C	0x3B			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM3HT[11:0] sets PWM3 high time	0x00, 0x00	r/w

RegAddr:		PWM4hightime		
0x3E	0x3D			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM4HT[11:0] sets PWM4 high time	0x00, 0x00	r/w

RegAddr:		PWM5hightime		
0x40	0x3F			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM5HT[11:0] sets PWM5 high time	0x00, 0x00	r/w

RegAddr:		PWM6hightime		
0x42	0x41			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM6HT[11:0] sets PWM6 high time	0x00, 0x00	r/w

RegAddr:		PWM7hightime		
0x44	0x43			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM7HT[11:0] sets PWM7 high time	0x00, 0x00	r/w

RegAddr:		PWM8hightime		
0x46	0x45			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM8HT[11:0] sets PWM8 high time	0x00, 0x00	r/w

RegAddr:		PWM9hightime		
0x48	0x47			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM9HT[11:0] sets PWM9 high time	0x00, 0x00	r/w

RegAddr:		PWM10hightime		
0x4A	0x49			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM10HT[11:0] sets PWM10 high time	0x00, 0x00	r/w

RegAddr:		PWM11hightime		
0x4C	0x4B			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM11HT[11:0] sets PWM11 high time	0x00, 0x00	r/w

RegAddr:		PWM12hightime		
0x4E	0x4D			
Bit	Bit	Description	Default	Access
3:0	7:0	PWMHT12[11:0] sets PWM12 high time	0x00, 0x00	r/w

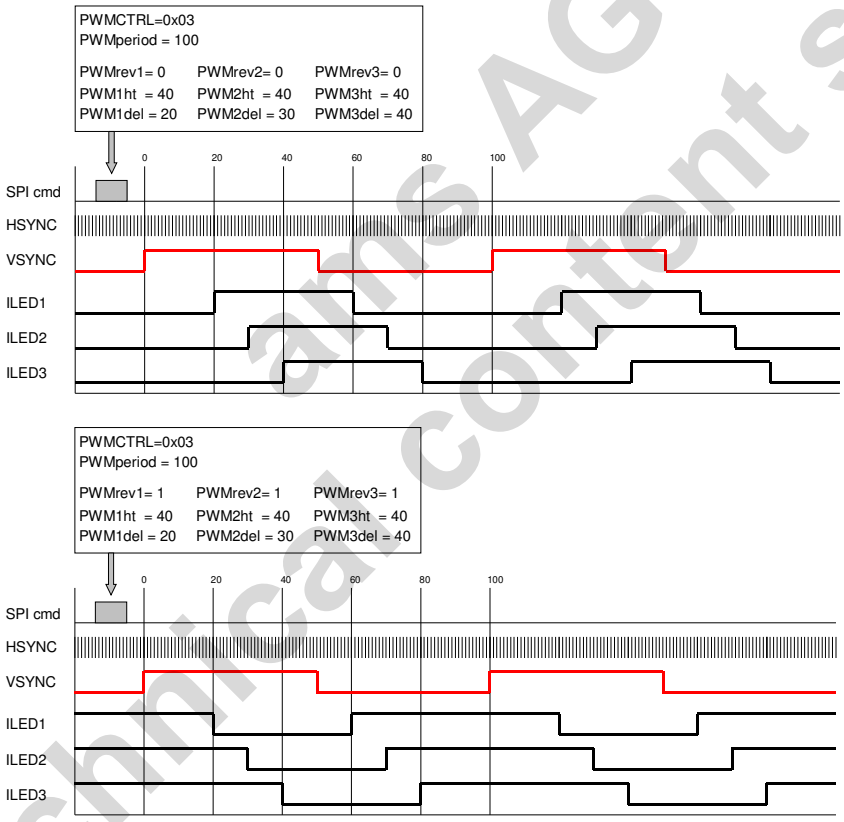
RegAddr:		PWM13hightime		
0x50	0x4F			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM13HT[11:0] sets PWM13 high time	0x00, 0x00	r/w

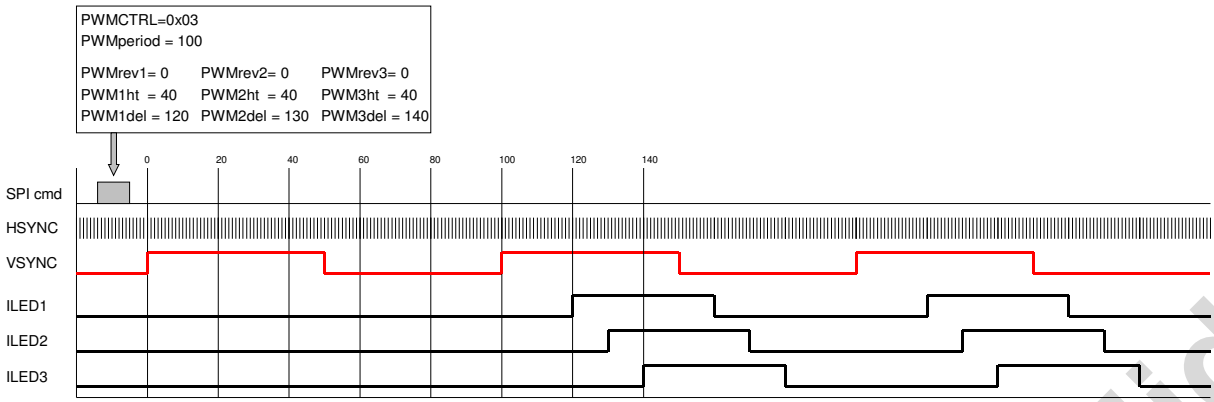
RegAddr:		PWM14hightime		
0x52	0x51			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM14HT[11:0] sets PWM14 high time	0x00, 0x00	r/w

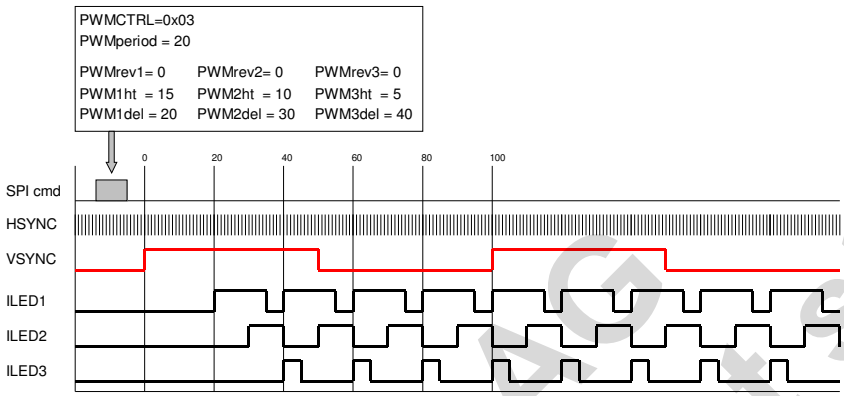
RegAddr:		PWM15hightime		
0x54	0x53			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM15HT[11:0] sets PWM15 high time	0x00, 0x00	r/w

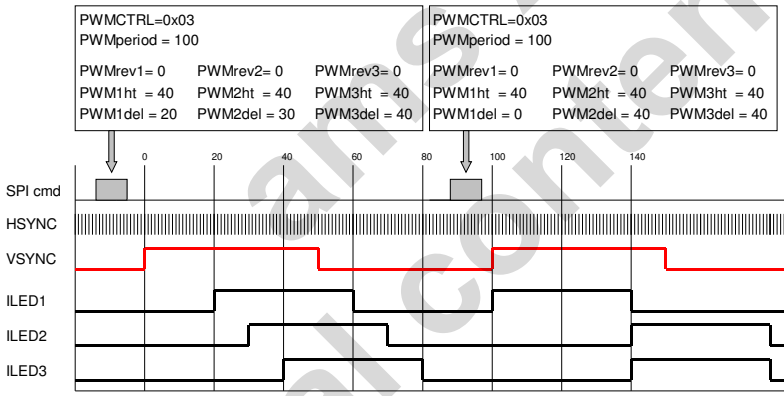
RegAddr:		PWM16hightime		
0x56	0x55			
Bit	Bit	Description	Default	Access
3:0	7:0	PWM16HT[11:0] sets PWM16 high time	0x00, 0x00	r/w

4.2.8 PWM examples









4.3 Power supply

4.4 Safety features

4.4.1 Temperature shutdown

If OTturnoff = 1 the outputs of the device are turned off when the die temperature reaches 140°C. If the die temperature goes below 130°C the outputs are turned on again.

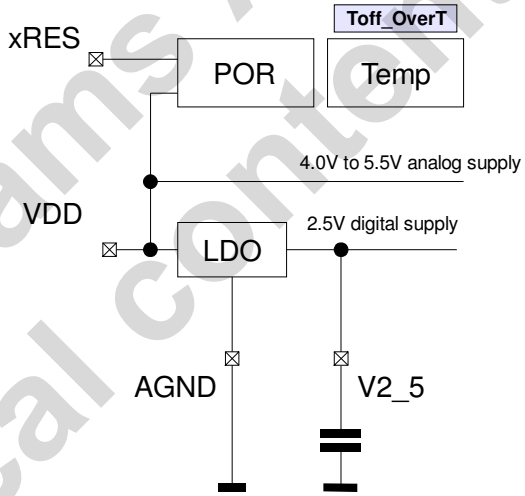
4.4.2 xRES input

In addition to the build in power on reset circuit there is an external reset input "xRES" available. This gives the possibility to keep the outputs turned off until all blocks of the LED-driver circuits are fully working (DCDC, MCU ...)

4.4.3 Register Lock/Unlock

To prevent wrong writing to registers due to noise on the serial interface a lock/unlock mechanism is implemented.
Register 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x13 belong to Group1 and can only be written if Group1 is unlocked by the "LOCKUNLOCK"-byte (Reg: 0x36)
Register 0x0D, 0x0E, 0x11, 0x12, 0x14, 0x15 belong to Group2 and can only be written if Group2 is unlocked by the "LOCKUNLOCK"-byte (Reg: 0x36)
The default value of the Groups is locked.

4.5 Reference circuit



The reference circuit generates an internal supply voltage of 2.5V for the digital logic.

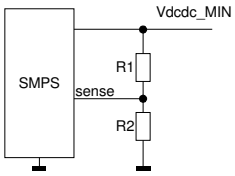
RegAddr: 0x60		STATUS		
Bit	Name	Description	Default	Access
7	STATnosync	Sync detector status 0...no sync fault 1...sync fault. VSYNC was missed for > 100ms	0	r
6	STATOT	Overtermperature status 0...no overtemperature 1...overtemperature	0	r
5	STATopen	Status open LED detection 0...no open LED detected 1...opdn LED detected	0	r
4	STATshort	Status short LED detection 0...no short LED detected 1...short LED detected	0	r
3		Not used	0	

2	STATUVLO	Status under voltage lockout detector 0...supply OK 1...supply voltage is to low	0	r
1:0	STATpower	Status of power supply monitor 00...no power supply 01...power supply is ramping up 10...power supply good 11...not used	10	r

4.6 Dynamic feedback control

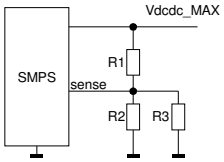
The output of pins “FB1” and “FB2” can be used to control any external power supply for best power efficiency. Every power supply senses its output voltage with a resistive voltage divider. This voltage divider can be modified to set the output voltage between a minimum output voltage VMIN and a maximum output voltage VMAX. The design of the dynamic feedback control is done in 3 steps.

Step 1: Set the resistors R1,R2 in the power supply according to the minimum output voltage



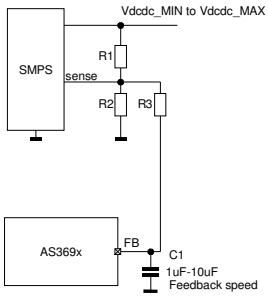
$$Vout_{MIN} = \frac{(R1+R2)}{R2} * V_{sense}$$

Step 2: Add the Resistors R3 in the power supply according to the maximum output voltage

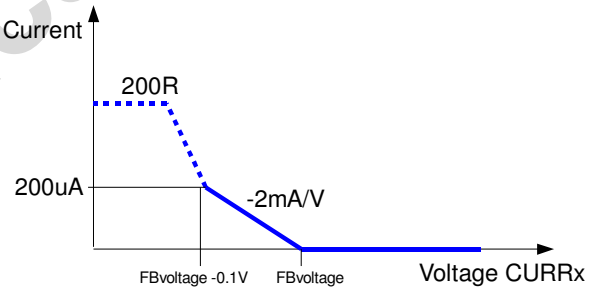


$$Vout_{MAX} = \frac{(R1+R2||R3)}{R2||R3} * V_{sense}$$

Step 3: Connect R3 to the feedback pin “FB”.
C1 should be chosen according to the speed requirements of the feedback loop.



The characteristic of the feedback function can be seen in the following diagram. The final output voltage Vdcdc is determined by the setting of “FBvoltage” and the current flowing into the FB pin.

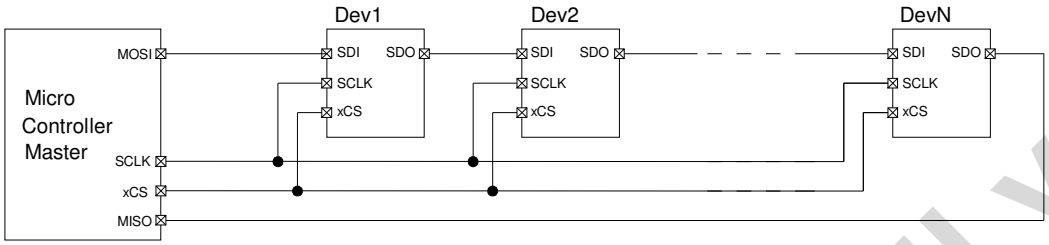


5 SPI interface

For the data transfer a serial peripheral interface (SPI) is used. The SPI is configured to work only as SPI slave. If more than one driver is connected to a SPI master, they can be connected in a "Daisy Chain"-structure or a parallel structure.

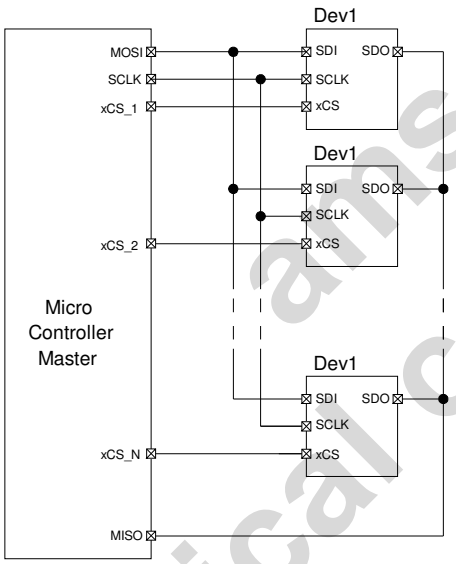
5.1 SPI daisy-chain structure

All SPI slaves share the same clock (SCLK) and chip select (xCS) signal. In that configuration all devices can be treated as one big shift register. The devices are automatically enumerated as described in the next section.



5.2 SPI parallel structure

All SPI slaves share the same input (SDI) output (SDO) and clock (SCLK) signal. Every single device can be addressed via the chip select (xCS) signal. In this configuration every device has DevAddr = 0x01.



5.3 SPI device address enumeration

The device address of each driver is automatically set by the position of the device in the chain. The first device has DevAddr = 0x01, the second device has DevAddr = 0x02 and so on. Device Addresses 0x00 and 0x3F are used for special broadcast writing commands described below.

5.4 SPI protocol

5.4.1 Data types

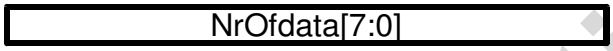
When xCS=0 all slaves will be activated. The addressing and data section is organized in byte packages. Each message can be built with the following Bytes:

Device address:

Addresses a specific driver and defines protocol information

Bit	Meaning	Value
B	Broadcast	B=1...Broadcast message to all devices B=0...Normal message to one single device
S	Singlebyte	S=0...Block data read or write S=1...Single data transmission (only one byte)
DevAddr[5:0]	Device Address	0x00 Write same data to same register of all devices (B=1) 0x01 to 0x3E. Device addresses for device 1 to 62 0x3F Write different data to same register of all devices (B=1)

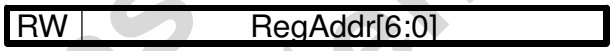
Nr_of_data:



Defines the number of data bytes in the data frame if S=0

Bit	Meaning	Value
NrOfdata[7:0]	Number of data bytes in frame	0x00 to 0xFF

Register_address:



Register address to be read or written

Bit	Meaning	Value
RW	Read/xWrite	RW=0 write to reg address RW=1 read from reg address
RegAddr[6:0]	Select register address	0x00 to 0x60

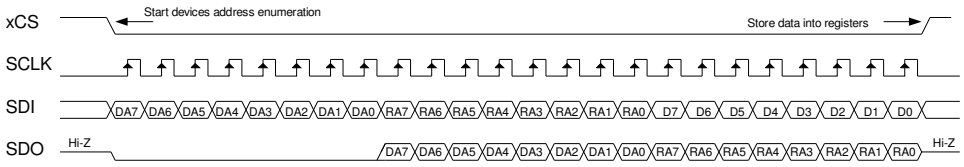
Data:

Data

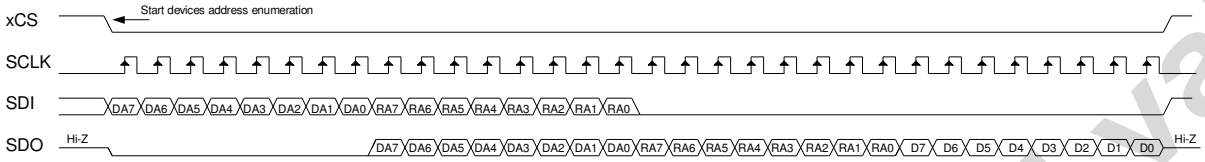
Bit	Meaning	Value
data [7:0],	Data	0x00 to 0xFF

5.4.2 Timings

Write single data into single device



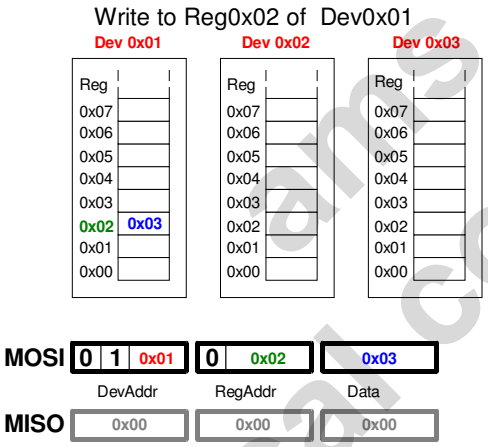
Read single data from single device

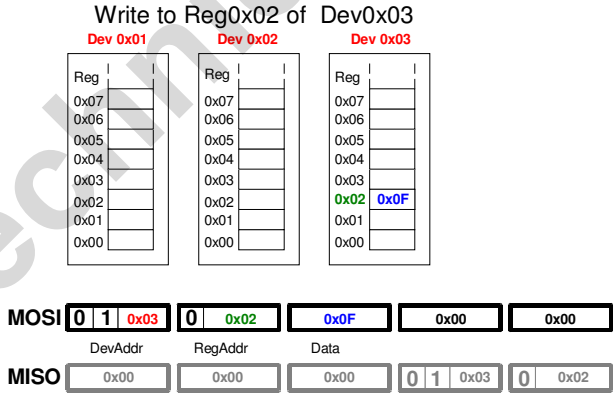


DA...DevAddr
RA...RegAddr
D.....Data

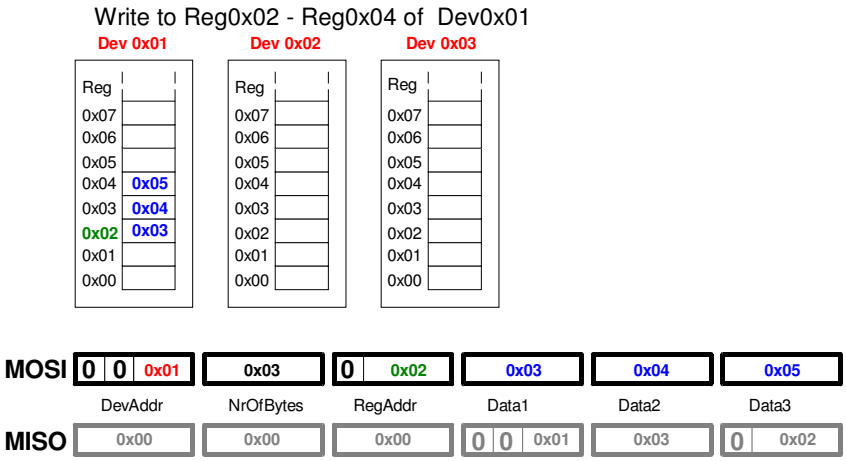
5.5 SPI protocol examples

5.5.1 Write single data



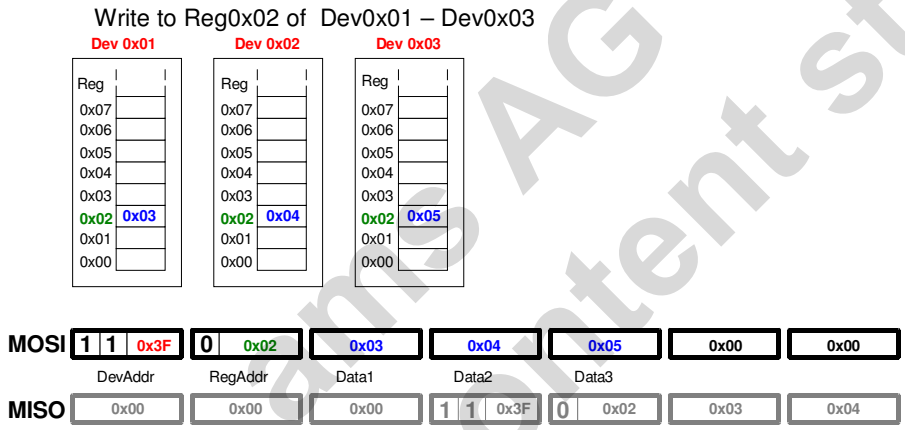


5.5.2 Write N data



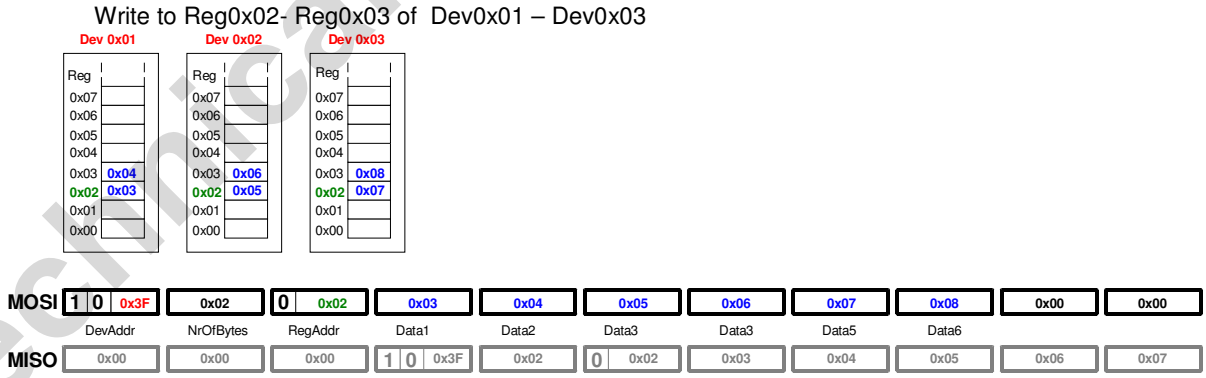
5.5.3 Write different data in same register of all devices (single byte)

Set DevAdd = 0x3F



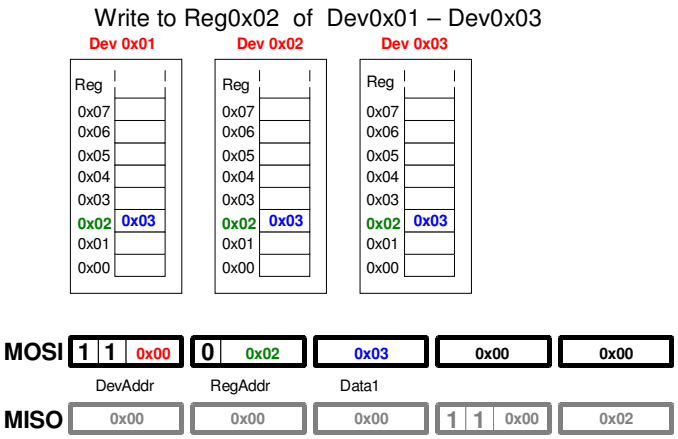
5.5.4 Write different data in same register of all devices (multiple bytes)

Set DevAdd = 0x3F



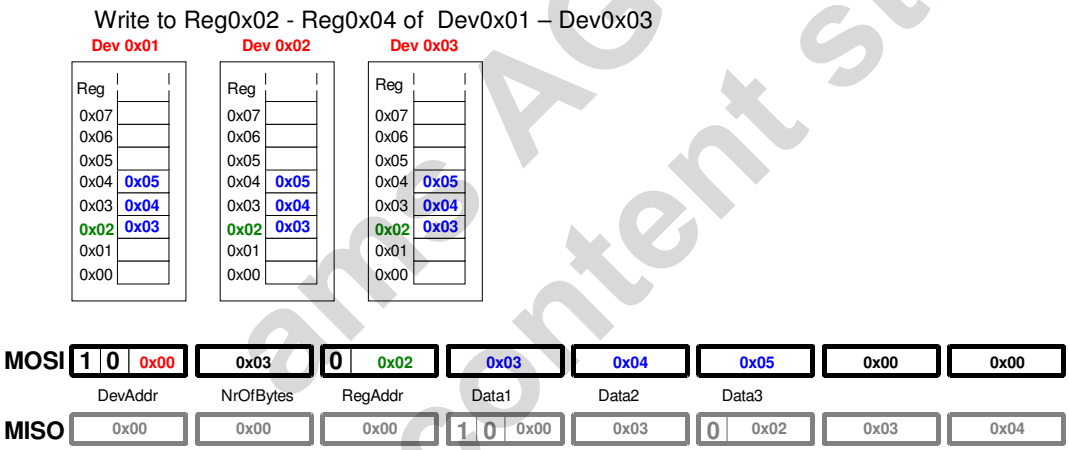
5.5.5 Write same data in same register of all devices (single byte)

Set DevAdd = 0x00

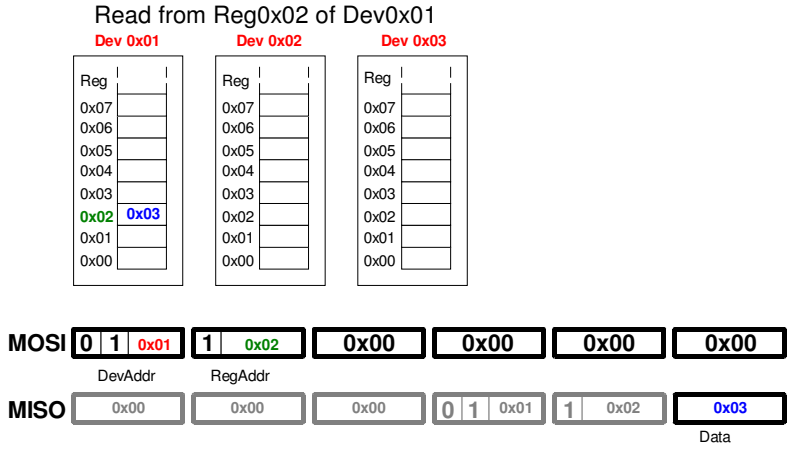


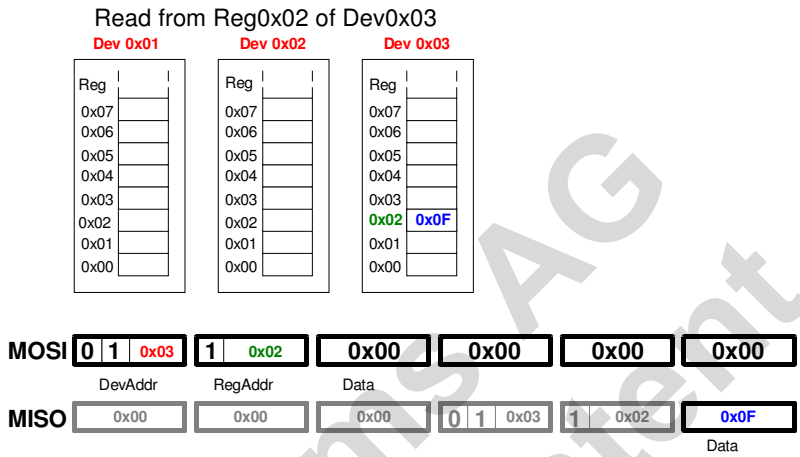
5.5.6 Write same data in same register of all devices (multiple bytes)

Set DevAdd = 0x00

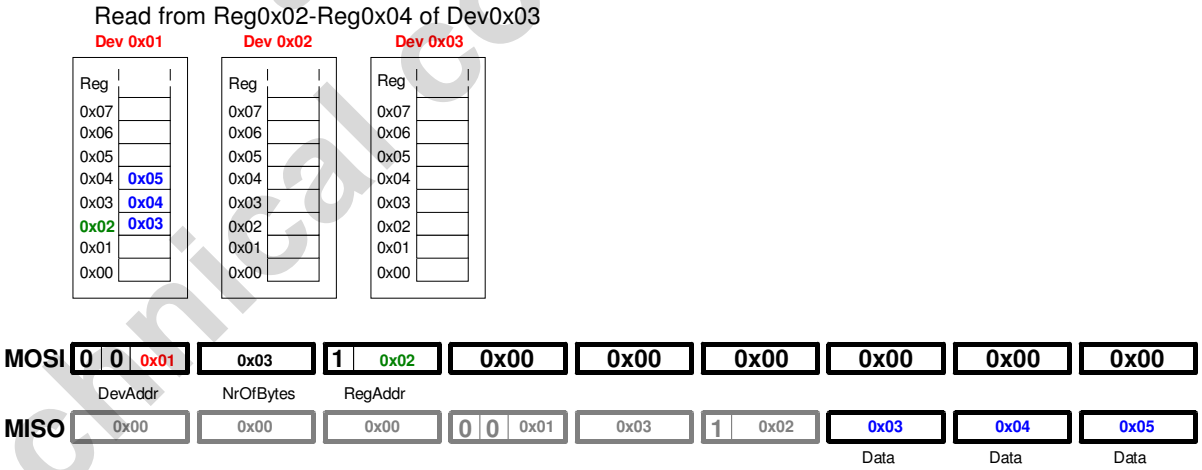


5.5.7 Read single data





5.5.8 Read N data



6 Register map

	Registers can only be written if **Group1** is UNLOCKED. **Default = LOCKED**
	Registers can only be written if **Group2** is UNLOCKED. **Default = LOCKED**

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x00		Used for block writing								
0x01	CUR_ON_1	Curr8	Curr7	Curr6	Curr5	Curr4	Curr3	Curr2	Curr1	0x00
0x02	CUR_ON_2	Curr16	Curr15	Curr14	Curr13	Curr12	Curr11	Curr10	Curr9	0x00
0x03	FAULT_1						Toff Otemp	Toff short	Toff open	0x04
0x04	FAULT_2	OPEN voltage		SHORT voltage				SHORT en	OPEN en	0x00
0x05	FEEDBACK			FB voltage		FB boost			FB enable	0x00
0x06	FB_SEL1	FBsel8	FBsel7	FBsel6	FBsel5	FBsel4	FBsel3	FBsel2	FBsel1	0x00
0x07	FB_SEL2	FBsel16	FBsel15	FBsel14	FBsel13	FBsel12	FBsel11	FBsel10	FBsel9	0x00
0x08	CURRctrl			DAC ref				Slew rate		0x00
0x09	SHORTLED1	Short8	Short7	Short6	Short5	Short4	Short3	Short2	Short1	0x00
0x0A	SHORTLED2	Short16	Short15	Short14	Short13	Short12	Shor11	Shor10	Short9	0x00
0x0B	OPENLED1	Open8	Open7	Open6	Open5	Open4	Open3	Open2	Open1	0x00
0x0C	OPENLED2	Open16	Open15	Open14	Open13	Open12	Open11	Open10	Open9	0x00
0x0D	DACLSB	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0	0x00
0x0E	DACMSB							DAC9	DAC8	0x20
0x0F										0x00
0x10										0x00
0x11	PWMREV1	PWM Rev8	PWM Rev7	PWM Rev6	PWM Rev5	PWM Rev4	PWM Rev3	PWM Rev2	PWM Rev1	0x00
0x12	PWMREV2	PWM Rev16	PWM Rev15	PWM Rev14	PWM Rev13	PWM Rev12	PWM Rev11	PWM Rev10	PWM Rev9	0x00
0x13	PWMCTRL	Fault DetDly	Delay Start		VSYNC det	VSYNC edge	PWM ext	Update Mode	Clock Src0	0x00
0x14	PWMperiodLSB	PWM Per7	PWM Per6	PWM Per5	PWM Per4	PWM Per3	PWM Per2	PWM Per1	PWM Per0	0x00
0x15	PWMperiodMSB	0	0	0	0	PWM Per11	PWM Per10	PWM Per9	PWM Per8	0x00
0x16	PWM1delLSB	PWM1 Del7	PWM1 Del6	PWM1 Del5	PWM1 Del4	PWM1 Del3	PWM1 Del2	PWM1 Del1	PWM1 Del0	0x00
0x17	PWM1delMSB	0	0	0	0	PWM1 Del11	PWM1 Del10	PWM1 Del9	PWM1 Del8	0x00
0x18	PWM2delLSB	PWM2 Del7	PWM2 Del6	PWM2 Del5	PWM2 Del4	PWM2 Del3	PWM2 Del2	PWM2 Del1	PWM2 Del0	0x00
0x19	PWM2delMSB	0	0	0	0	PWM2 Del11	PWM2 Del10	PWM2 Del9	PWM2 Del8	0x00
0x1A	PWM3delLSB	PWM3 Del7	PWM3 Del6	PWM3 Del5	PWM3 Del4	PWM3 Del3	PWM3 Del2	PWM3 Del1	PWM3 Del0	0x00
0x1B	PWM3delMSB	0	0	0	0	PWM3 Del11	PWM3 Del10	PWM3 Del9	PWM3 Del8	0x00
0x1C	PWM4delLSB	PWM4 Del7	PWM4 Del6	PWM4 Del5	PWM4 Del4	PWM4 Del3	PWM4 Del2	PWM4 Del1	PWM4 Del0	0x00
0x1D	PWM4delMSB	0	0	0	0	PWM4 Del11	PWM4 Del10	PWM4 Del9	PWM4 Del8	0x00
0x1E	PWM5delLSB	PWM5 Del7	PWM5 Del6	PWM5 Del5	PWM5 Del4	PWM5 Del3	PWM5 Del2	PWM5 Del1	PWM5 Del0	0x00
0x1F	PWM5delMSB	0	0	0	0	PWM5 Del11	PWM5 Del10	PWM5 Del9	PWM5 Del8	0x00
0x20	PWM6delLSB	PWM6 Del7	PWM6 Del6	PWM6 Del5	PWM6 Del4	PWM6 Del3	PWM6 Del2	PWM6 Del1	PWM6 Del0	0x00
0x21	PWM6delMSB	0	0	0	0	PWM6 Del11	PWM6 Del10	PWM6 Del9	PWM6 Del8	0x00
0x22	PWM7delLSB	PWM7 Del7	PWM7 Del6	PWM7 Del5	PWM7 Del4	PWM7 Del3	PWM7 Del2	PWM7 Del1	PWM7 Del0	0x00
0x23	PWM7delMSB	0	0	0	0	PWM7 Del11	PWM7 Del10	PWM7 Del9	PWM7 Del8	0x00
0x24	PWM8delLSB	PWM8 Del7	PWM8 Del6	PWM8 Del5	PWM8 Del4	PWM8 Del3	PWM8 Del2	PWM8 Del1	PWM8 Del0	0x00
0x25	PWM8delMSB	0	0	0	0	PWM8 Del11	PWM8 Del10	PWM8 Del9	PWM8 Del8	0x00
0x26	PWM9delLSB	PWM9 Del7	PWM9 Del6	PWM9 Del5	PWM9 Del4	PWM9 Del3	PWM9 Del2	PWM9 Del1	PWM9 Del0	0x00
0x27	PWM9delMSB	0	0	0	0	PWM9	PWM9	PWM9	PWM9	0x00

						Del11	Del10	Del9	Del8	
0x28	PWM10delLSB	PWM10 Del7	PWM10 Del6	PWM10 Del5	PWM10 Del4	PWM10 Del3	PWM10 Del2	PWM10 Del1	PWM10 Del0	0x00
0x29	PWM10delMSB	0	0	0	0	PWM10 Del11	PWM10 Del10	PWM10 Del9	PWM10 Del8	0x00
0x2A	PWM11delLSB	PWM11 Del7	PWM11 Del6	PWM11 Del5	PWM11 Del4	PWM11 Del3	PWM11 Del2	PWM11 Del1	PWM1 Del0	0x00
0x2B	PWM11delMSB	0	0	0	0	PWM11 Del11	PWM11 Del10	PWM11 Del9	PWM Del8	0x00
0x2C	PWM12delLSB	PWM12 Del7	PWM12 Del6	PWM12 Del5	PWM12 Del4	PWM12 Del3	PWM12 Del2	PWM12 Del1	PWM12 Del0	0x00
0x2D	PWM12delMSB	0	0	0	0	PWM12 Del11	PWM12 Del10	PWM12 Del9	PWM12 Del8	0x00
0x2E	PWM13delLSB	PWM13 Del7	PWM13 Del6	PWM13 Del5	PWM13 Del4	PWM13 Del3	PWM13 Del2	PWM13 Del1	PWM13 Del0	0x00
0x2F	PWM13delMSB	0	0	0	0	PWM13 Del11	PWM13 Del10	PWM13 Del9	PWM13 Del8	0x00
0x30	PWM14delLSB	PWM14 Del7	PWM14 Del6	PWM14 Del5	PWM14 Del4	PWM14 Del3	PWM14 Del2	PWM14 Del1	PWM14 Del0	0x00
0x31	PWM14delMSB	0	0	0	0	PWM14 Del11	PWM14 Del10	PWM14 Del9	PWM14 Del8	0x00
0x32	PWM15delLSB	PWM15 Del7	PWM15 Del6	PWM15 Del5	PWM15 Del4	PWM15 Del3	PWM15 Del2	PWM15 Del1	PWM15 Del0	0x00
0x33	PWM15delMSB	0	0	0	0	PWM15 Del11	PWM15 Del10	PWM15 Del9	PWM15 Del8	0x00
0x34	PWM16delLSB	PWM16 Del7	PWM16 Del6	PWM16 Del5	PWM16 Del4	PWM16 Del3	PWM16 Del2	PWM16 Del1	PWM16 Del0	0x00
0x35	PWM16delMSB	0	0	0	0	PWM16 Del11	PWM16 Del10	PWM16 Del9	PWM16 Del8	0x00
0x36	LOCKUNLOC	MagicByte								0x00
0x37	PWM1htLSB	PWM1 HT7	PWM1 HT6	PWM1 HT5	PWM1 HT4	PWM1 HT3	PWM1 HT2	PWM1 HT1	PWM1 HT0	0x00
0x38	PWM1htMSB	0	0	0	0	PWM1 HT11	PWM1 HT10	PWM1 HT9	PWM1 HT8	0x00
0x39	PWM2htLSB	PWM2 HT7	PWM2 HT6	PWM2 HT5	PWM2 HT4	PWM2 HT3	PWM2 HT2	PWM2 HT1	PWM2 HT0	0x00
0x3A	PWM2htMSB	0	0	0	0	PWM2 HT11	PWM2 HT10	PWM2 HT9	PWM2 HT8	0x00
0x3B	PWM3htLSB	PWM3 HT7	PWM3 HT6	PWM3 HT5	PWM3 HT4	PWM3 HT3	PWM3 HT2	PWM3 HT1	PWM3 HT0	0x00
0x3C	PWM3htMSB	0	0	0	0	PWM3 HT11	PWM3 HT10	PWM3 HT9	PWM3 HT8	0x00
0x3D	PWM4htLSB	PWM4 HT7	PWM4 HT6	PWM4 HT5	PWM4 HT4	PWM4 HT3	PWM4 HT2	PWM4 HT1	PWM4 HT0	0x00
0x3E	PWM4htMSB	0	0	0	0	PWM4 HT11	PWM4 HT10	PWM4 HT9	PWM4 HT8	0x00
0x3F	PWM5htLSB	PWM5 HT7	PWM5 HT6	PWM5 HT5	PWM5 HT4	PWM5 HT3	PWM5 HT2	PWM5 HT1	PWM5 HT0	0x00
0x40	PWM5htMSB	0	0	0	0	PWM5 HT11	PWM5 HT10	PWM5 HT9	PWM5 HT8	0x00
0x41	PWM6htLSB	PWM6 HT7	PWM6 HT6	PWM6 HT5	PWM6 HT4	PWM6 HT3	PWM6 HT2	PWM6 HT1	PWM6 HT0	0x00
0x42	PWM6htMSB	0	0	0	0	PWM6 HT11	PWM6 HT10	PWM6 HT9	PWM6 HT8	0x00
0x43	PWM7htLSB	PWM7 HT7	PWM7 HT6	PWM7 HT5	PWM7 HT4	PWM7 HT3	PWM7 HT2	PWM7 HT1	PWM7 HT0	0x00
0x44	PWM7htMSB	0	0	0	0	PWM7 HT11	PWM7 HT10	PWM7 HT9	PWM7 HT8	0x00
0x45	PWM8htLSB	PWM8 HT7	PWM8 HT6	PWM8 HT5	PWM8 HT4	PWM8 HT3	PWM8 HT2	PWM8 HT1	PWM8 HT0	0x00
0x46	PWM8htMSB	0	0	0	0	PWM8 HT11	PWM8 HT10	PWM8 HT9	PWM8 HT8	0x00
0x47	PWM9htLSB	PWM9 HT7	PWM9 HT6	PWM9 HT5	PWM9 HT4	PWM9 HT3	PWM9 HT2	PWM9 HT1	PWM9 HT0	0x00
0x48	PWM9htMSB	0	0	0	0	PWM9 HT11	PWM9 HT10	PWM9 HT9	PWM9 HT8	0x00
0x49	PWM10htLSB	PWM10 HT7	PWM10 HT6	PWM10 HT5	PWM10 HT4	PWM10 HT3	PWM10 HT2	PWM10 HT1	PWM10 HT0	0x00
0x4A	PWM10htMSB	0	0	0	0	PWM10 HT11	PWM10 HT10	PWM10 HT9	PWM10 HT8	0x00
0x4B	PWM11htLSB	PWM11 HT7	PWM11 HT6	PWM11 HT5	PWM11 HT4	PWM11 HT3	PWM11 HT2	PWM11 HT1	PWM11 HT0	0x00
0x4C	PWM11htMSB	0	0	0	0	PWM11 HT11	PWM11 HT10	PWM11 HT9	PWM11 HT8	0x00
0x4D	PWM12htLSB	PWM12 HT7	PWM12 HT6	PWM12 HT5	PWM12 HT4	PWM12 HT3	PWM12 HT2	PWM12 HT1	PWM12 HT0	0x00
0x4E	PWM12htMSB	0	0	0	0	PWM12 HT11	PWM12 HT10	PWM12 HT9	PWM12 HT8	0x00
0x4F	PWM13htLSB	PWM13 HT7	PWM13 HT6	PWM13 HT5	PWM13 HT4	PWM13 HT3	PWM13 HT2	PWM13 HT1	PWM13 HT0	0x00
0x50	PWM13htMSB	0	0	0	0	PWM13 HT11	PWM13 HT10	PWM13 HT9	PWM13 HT8	0x00
0x51	PWM14htLSB	PWM14	PWM14	PWM14	PWM14	PWM14	PWM14	PWM14	PWM14	0x00

		HT7	HT6	HT5	HT4	HT3	HT2	HT1	HT0	
0x52	PWM14htMSB	0	0	0	0	PWM14 HT11	PWM14 HT10	PWM14 HT9	PWM14 HT8	0x00
0x53	PWM15htLSB	PWM15 HT7	PWM15 HT6	PWM15 HT5	PWM15 HT4	PWM15 HT3	PWM15 HT2	PWM15 HT1	PWM15 HT0	0x00
0x54	PWM15htMSB	0	0	0	0	PWM5 HT11	PWM15 HT10	PWM15 HT9	PWM15 HT8	0x00
0x55	PWM16htLSB	PWM16 HT7	PWM16 HT6	PWM16 HT5	PWM16 HT4	PWM16 HT3	PWM16 HT2	PWM16 HT1	PWM16 HT0	0x00
0x56	PWM16htMSB	0	0	0	0	PWM16 HT11	PWM16 HT10	PWM16 HT9	PWM16 HT8	0x00
0x57	ASICIDLSB	A				Rev Nr.				0xAX
0x58	ASICIDMSB	9				5				0x95
0x59	Not used									0x00
0x60	STATUS	STAT Nosync	STAT OT	STAT Open	STAT Short	0	STAT UVLO	STAT power		

ADDRESSES ABOVE 0x60 ARE FOR FACTORY TEST ONLY. DO NOT WRITE !

7 Pinout and Packaging

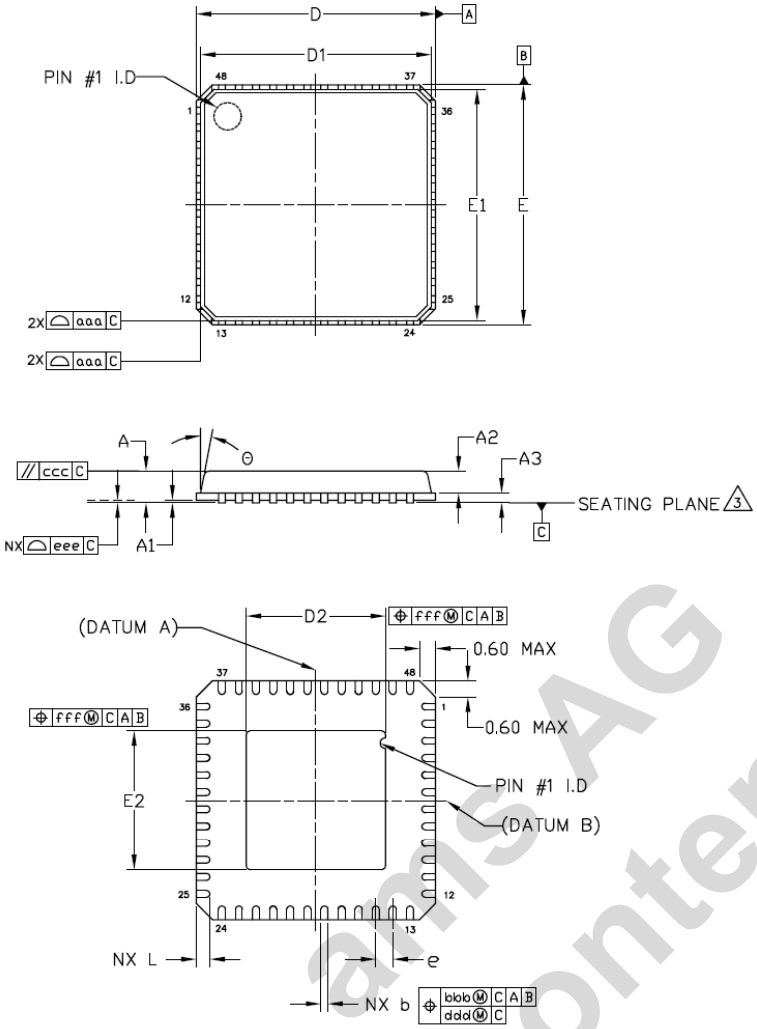
7.1 Pinout

Pin Nr	Pin Name	Pin Type	Description
1	CURR1	AIO	Current source output 1
2	RES1	AIO	Current setting resistor 1
3	V2_5	AIO	Digital supply output. Connect 2.2uF bypass capacitor to GND
4	XFAULT	DO- OD	Fault output. Open drain. Connect pullup to VDD
5	XRES	DI	Reset input active low
6	FB1	AIO	Power supply feedback output1
7	FB2	AIO	Power supply feedback output2
8	VSSA	AIO	GND
9	VDD	AIO	Power supply. Connect 4.7uF bypass capacitor to GND
10	VSS_SENSE	AIO	VSS sense input. Keep this node noise free
11	RES16	AIO	Current setting resistor 16
12	CURR16	AIO	Current source output 16
13	RES15	AIO	Current setting resistor 15
14	CURR15	AIO	Current source output 15
15	RES14	AIO	Current setting resistor 14
16	CURR14	AIO	Current source output 14
17	RES13	AIO	Current setting resistor 13
18	CURR13	AIO	Current source output 13
19	CURR12	AIO	Current source output 12
20	RES12	AIO	Current setting resistor 12
21	CURR11	AIO	Current source output 11
22	RES11	AIO	Current setting resistor 11
23	CURR10	AIO	Current source output 10
24	RES10	AIO	Current setting resistor 10
25	CURR9	AIO	Current source output 9
26	RES9	AIO	Current setting resistor 9
27	VDD	AIO	Supply
28	VSSA	AIO	GND
29	VSYNC	DI-PD	Vertical sync frequency
30	HSYNC	DI-PD	Clock input for PWM generators
31	xCS	DI-PU	SPI interface chip select
32	SDO	DO	SPI interface data output. Tristate output
33	SCL	DI-PD	SPI interface clock
34	SDI	DI-PD	SPI interface data input
35	RES8	AIO	Current setting resistor 8
36	CURR8	AIO	Current source output 8
37	RES7	AIO	Current setting resistor 7
38	CURR7	AIO	Current source output 7

39	RES6	AIO	Current setting resistor 6
40	CURR6	AIO	Current source output 6
41	RES5	AIO	Current setting resistor 5
42	CURR5	AIO	Current source output 5
43	CURR4	AIO	Current source output 4
44	RES4	AIO	Current setting resistor 4
45	CURR3	AIO	Current source output 3
46	RES3	AIO	Current setting resistor 3
47	CURR2	AIO	Current source output 2
48	RES2	AIO	Current setting resistor 2
EP	VSSA	AIO	Exposed PAD. Connect to VSSA

AIO	Analog Pin
DI	Digital input
DI-PU	Digital input with pull up resistor
DI-PD	Digital input with pull down resistor
DO	Digital output
DO-OD	Digital output open drain

7.2 Package Drawing QFN48



REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	–	0.65	1.00
A3	–	0.20 REF	–
L	0.35	0.40	0.45
θ	0°	–	14°
b	0.18	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
D2	4.00	4.10	4.20
E2	4.00	4.10	4.20
D1	–	6.75 BSC	–
E1	–	6.75 BSC	–
aaa	–	0.15	–
bbb	–	0.10	–
ccc	–	0.10	–
ddd	–	0.05	–
eee	–	0.08	–
fff	–	0.10	–
N		48	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
4. RADIUS ON TERMINAL IS OPTIONAL.
5. N IS THE TOTAL NUMBER OF TERMINALS.

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ASSEMBLY ENGINEERING

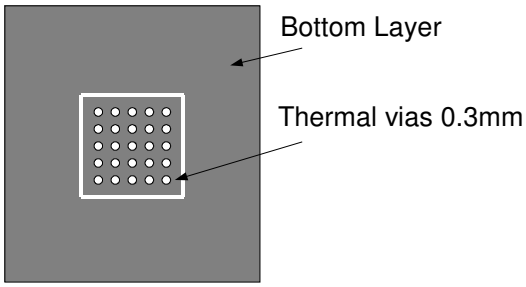
DRAWN RH8	DATE 2010.10.20	REV. N/C	TITLE PUNCHED QFN, 7x7x0.9mm 48 LEAD, 4.10mm SQ. ePAD	REFERENCE DOCUMENT JEDEC MO – 220 LATEST REVISION
CHECKED GBO	DATE 2010.10.20		DRAWING NO. QQJ	UNIT
APPROVED MKR	DATE 2010.10.20	SHEET 1 OF 1	DIMENSION AND TOLERANCE	SCALE NOT IN SCALE

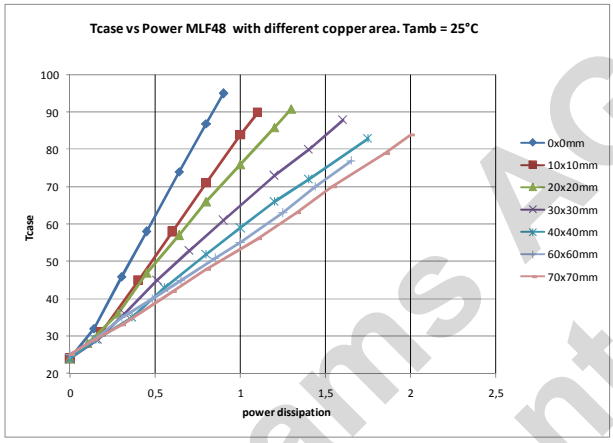
8 Thermal characteristic

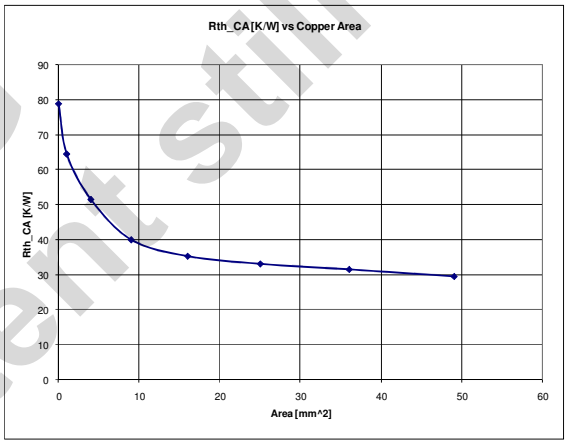
The thermal characteristics of the devices were measured at 25°C ambient temperature. The device was mounted on a double sided FR4 PCB with the bottom layer used as cooling area.

8.1 QFN48

PCB FR4, 1cm distance from ground







9 Ordering information

Part Number	Marking	Package Type	Delivery Form	Description
AS3695A-ZMFT	AS3695A	QFN48	Tape and Reel in Dry Pack	Package size = 7x7mm, Pitch = 0.5mm, Pb-free;

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