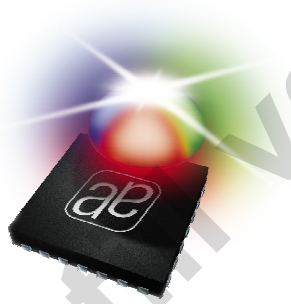
AS3693A –16 Channel high precision LED driver for LCD Backlight



1 General Description

The AS3693A is a 16 channels high precision LED driver with build in PWM generators for building backlight panels in LCD-TV-sets.
External clock and synchronizing inputs allow the synchronization of the LCD backlight with the TV picture. Local dimming and scan dimming is supported by 16 independent PWM generators with programmable delay, period and duty cycle. Three free configurable dynamic power feedback circuits make the device usable for white LED as well as RGB backlights. Build in safety features include thermal shutdown as well as open and short LED detection. All circuit parameters are programmable via I2C or SPI interface.

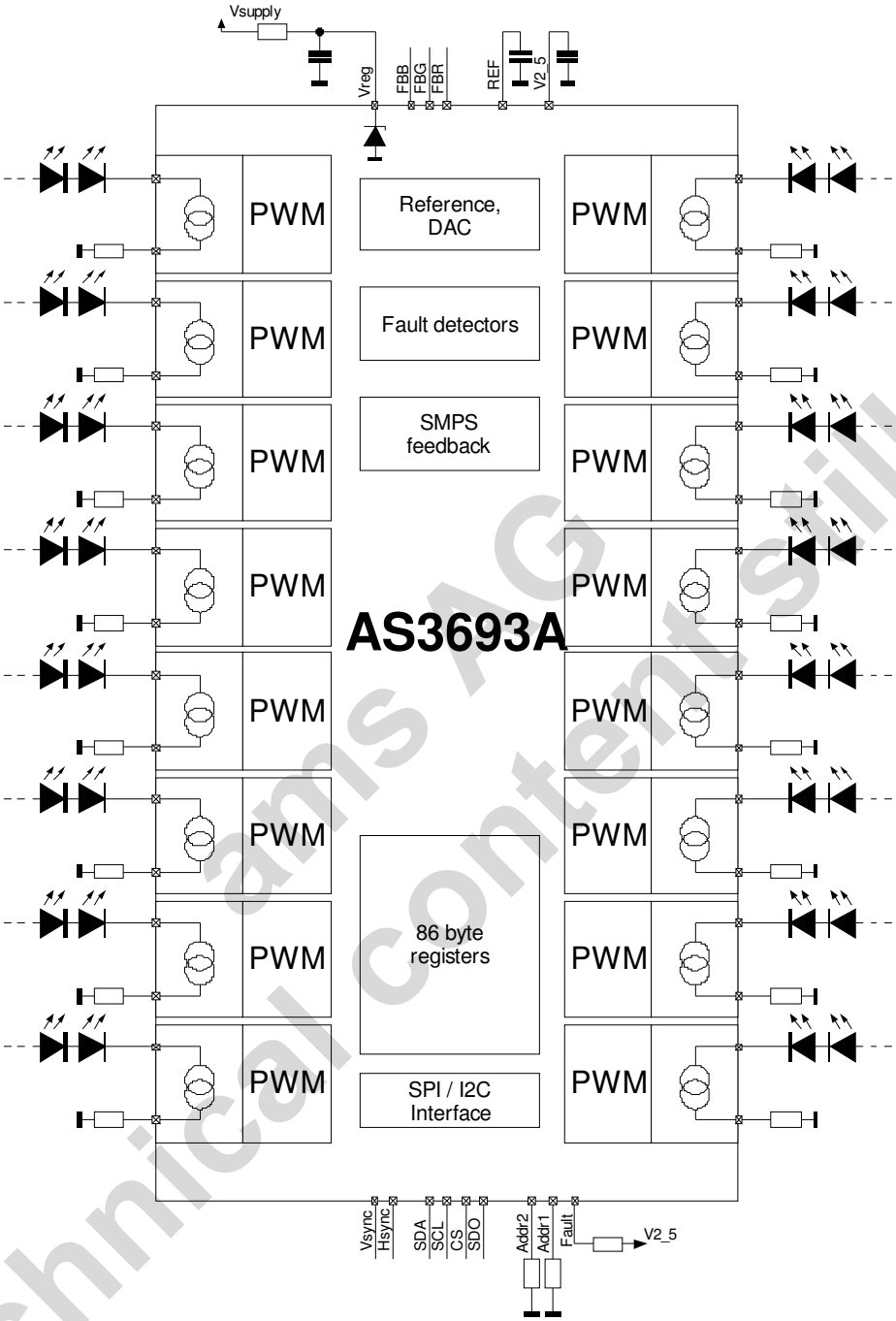
2 Key Features

- 16 Channel LED driver
- Output current 70mA (150mA) per channel
- Output voltage 0.4V to 50V
- Absolute current accuracy +/- 0.5%
- Output slew rate programmable
- Current programmable with external resistor
- Linear current control with 8 - bit DAC
- Linear current control with external analog voltage
- Digital current control with 16 independent PWM generators
- Free programmable 12 bit resolution (period, high time and delay)
- Overvoltage detection (short LED)
- Undervoltage detection (open LED)
- Temperature shutdown
- Fault interrupt output
- H-Sync, V-Sync inputs to synchronize with TV-set
- Internal or external PWM – clock
- I2C interface
- SPI interface
- 5 bit device - address (sets device address and interface mode)
- Automatic supply regulation feedback
- Each output can be assigned to red, green or blue feedback.
- Package QFN48 6x6mm, 0.4mm pitch,
  QFN48 7x7mm, 0.5mm pitch

3 Applications

- LED backlighting for LCD – TV sets and monitors

4 Block Diagram



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5 Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 1 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in Section 5 Electrical Characteristics is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1 – Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{DDMAX}	Supply for LED's	-0.3	>50	V	See notes[1]
V_{INVREG}	VREG supply voltage	-0.3	7.0	V	Applicable for pin VREG
I_{INVREG}	Maximum Vreg current		100	mA	Maximum Current flowing into Vreg
$V_{IN2.5V}$	2.5 V Pins	-0.3	V2_5+0.3V	V	Applicable for 2.5V pins[4]
V_{IN5V}	5V Pins	-0.3	VREG+ 0.3V	V	Applicable for 5V pins[2]
V_{IN50V}	50V Pins	-0.3	55	V	Applicable for CURR1, CURR2, CURR3 up to CURR16
I_{IN}	Input Pin Current	-25	+25	mA	At 25ºC, Norm: Jedec 17
T_{STRG}	Storage Temperature Range	-55	150	°C	
	Humidity	5	85	%	Non condensing
V_{ESD}	Electrostatic Discharge on Pins Curr1 – Curr16	-4000	4000	V	Norm: MIL 883 E Method 3015
V_{ESD}	Electrostatic Discharge on all Pins	-2000	2000	V	Norm: MIL 883 E Method 3015
PT	Total Power Dissipation		3.8W	W	At T At Ta = 25ºC, no airflow for QFN48 6x6mm on two layer FR4-Cu PCB[3]
P_{DERATE}	PT Derating Factor		40	mW/ °C	See notes[3]
T_{BODY}	Body Temperature during Soldering		260	°C	according to IPC/JEDEC J-STD-020C

Notes:

1, As the AS3693A is not directly connected to this supply. Only the parameters V_{INVREG}, V_{IN5V} and V_{IN50V} have to be guaranteed by the application
2, All pins except CURR1 to CURR16 and 2.5V
3, Copper area > 9 cm², thermal vias
4, 2.5V Pins are Fault, SDO, ADDR1 and ADDR2

5.2 Operating Conditions

Table 2 – Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Note
VDD	Main Supply			Not Limited	V	Supply is not directly connected to the AS3693A – see section 'Shunt Regulator'
VDDTOL	Main Supply Voltage Tolerance	-20		+20	%	Applies only for supply VREG is connected via Rvdd
VREGINT	Supply (shunt regulated by AS3693A)	5.0	5.2	5.4	V	If internally (shunt-)regulated by ZD1
VREGEXT		3.3	4.5	4.9	V	If externally supplied
TAMB	Ambient Temperature	-20	25	85	°C	
VUVL	Under voltage lockout voltage	2.6	2.8	3.0	V	If Vreg < UVUL current sources are turned off (Addr 0x01,Addr 0x02 = 0x00)
IVREG	Supply Current (Chip current consumption)			20	mA	Excluding current through shunt regulator (ZD1) – see section 'Shunt Regulator'. Note: Take care of the Power dissipation of the external Resistor.
IVREG_MAX	Maximum Supply current			30	mA	Maximum Current Into VREG – PIN (Supply current + shunt regulator current).
IVREG EXT_OFF				350	uA	Condition: externally supplied Curr_reg1-16 off (register 01h = 00h, register 02h = 00h)

5.3 Electrical Characteristics

Table 3 – Analog Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
VCURR	Current Source CURR1 to CURR16 Voltage Compliance	0.41		50.0	V	at 70mA
		0.9		50	V	at 150mA
ICURR	Current Source Range	0		150(3)	mA	ICURRx = 250mV / Rix (x=1...16)
ICURR, TOL	Current Source Tolerance	-0.5		+0.5	%	**Using 250mV reference** @25C $T_{JUNCTION}$, excluding variation of external resistors
		-1.5		+1.5	%	**Using 250mV reference** -20°C to +100°C(1) $T_{JUNCTION}$, -20°C to +85°C T_{AMB}, excluding variation of external resistors; V(CURRx) <= 4.0V
		-1.6		+1.6	%	**Using DAC reference** VDAC =250mV (Data = 0x80) @25C $T_{JUNCTION}$, excluding variation of external resistors
DAC_INL	DAC INL	-4		+4	LSB	DAC integral nonlinearity
VC	Automatic Supply Regulation trip point	0.5		1	V	See section 'Feedback Circuit (DCDC_Regulation_Trip_Point)'.

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{C,GAIN}$	Automatic Supply Regulation gain		2.0		mA/V	Voltage to current ratio; output current range typ. 0 to 200uA
T_{OVTEMP}	Over temperature Limit	130	140	150	°C	Maximum junction temperature(2)
Thyst	Over temperature hysteresis		10		°C	
CLK	Internal Clock for PWM	400	500	600	KHz	Clock for internal PWM generation

Notes:

1, Accuracy at +100°C guaranteed by design and verified by laboratory characterization

2, If the temperature exceeds the over temperature limit, the PWM will be turned off. If the temperature decreases, the PWM is activated again. The register settings are not reset.

3, To obtain higher currents use more than one current sink in parallel or use AS3693B (external transistors)

Table 4 – Digital Input pins characteristics (SDI,VSYNC,HSYNC,SCL,CS)

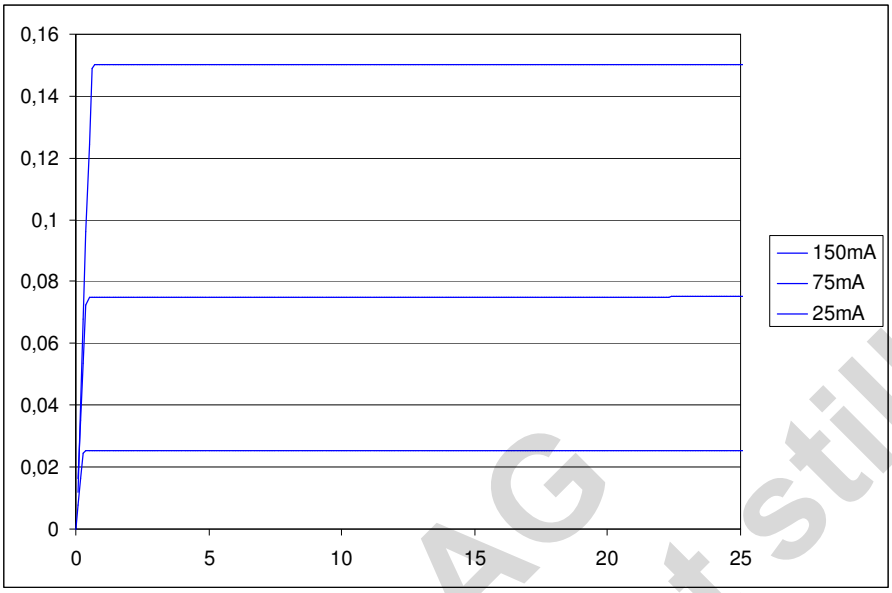
Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{IH}	High Level Input voltage	1.3		VREG	V	
V_{IL}	Low Level Input voltage	-0.3		0.4	V	
f_{SCL}	Maximum SCL Frequency			10	MHz	
f_{HSYNC}	Maximum HSYNC Frequency			10	MHz	Output driver is slew rate limited (Register: Curreg_Control 0x0D)
t_{s_VH}	Vsync setup time before rising edge of Hsync	15			ns	SYNC-mode: PWM values are updated with first rising edge of Hsync while Vsync = 1 (see 7.3.1.1)
t_{h_VH}	Vsync hold time after rising edge of Hsync	15			ns	
t_{s_SCISCL}	Setup time SDI,SCL	15			ns	SPI interface mode
t_{h_SCLSCI}	Hold time SCL,SDI	15			ns	SPI interface mode
t_{s_CSSCL}	Setup time CS,SCL	15			ns	SPI interface mode
t_{h_SCLCS}	Hold time SCL, CS	15			ns	SPI interface mode
t_{BUF}	Bus free time between Stop and Start conditions	1.3			us	I2C interface mode
$T_{setupstart}$	Setup time for repeated Start condition	100			ns	I2C interface mode
$T_{holdstart}$	Hold time for repeated Start condition	160			ns	I2C interface mode
$T_{setupstop}$	Setup time for Stop condition	160			ns	I2C interface mode

Table 5 – Digital output pins characteristics (SDO)

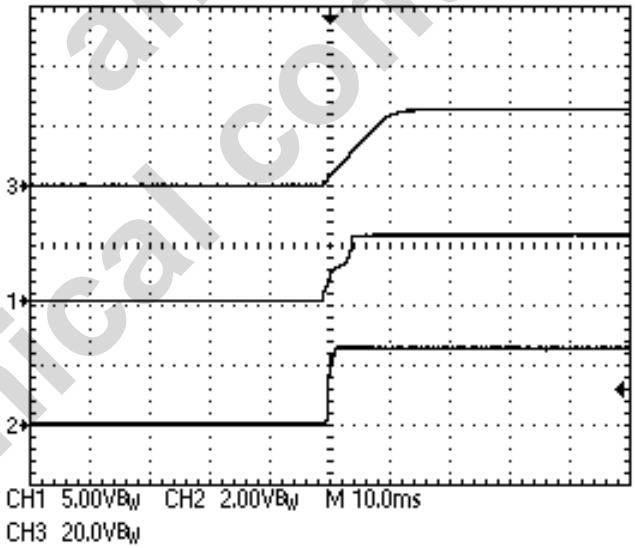
Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{OH}	High Level Output voltage	2.4		2.5	V	
V_{OL}	Low Level Output voltage	-0.3		0.4	V	

6 Typical Operation Characteristics

6.1 Output current vs Output Voltage

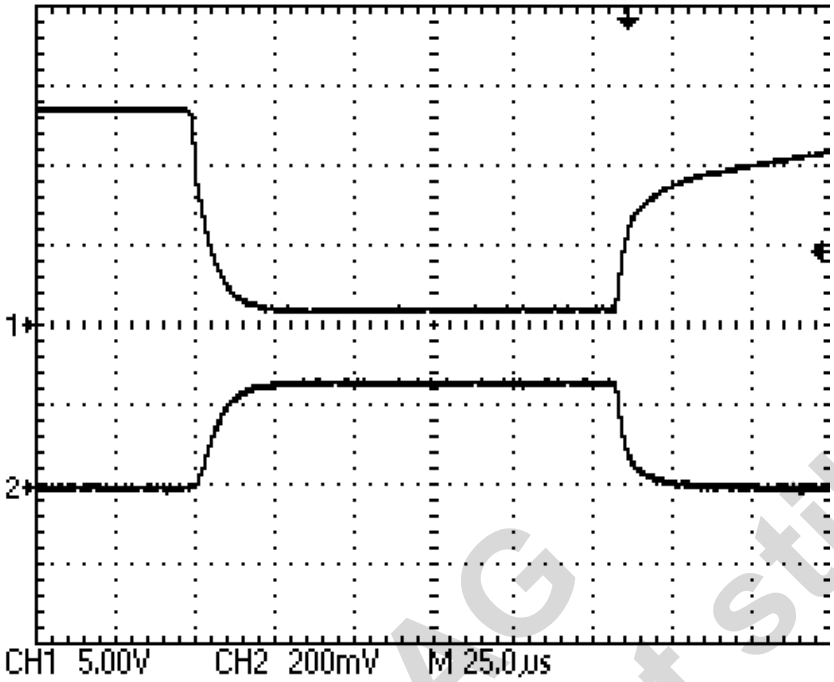


6.2 Vsupply vs VREG and V2.5 at startup



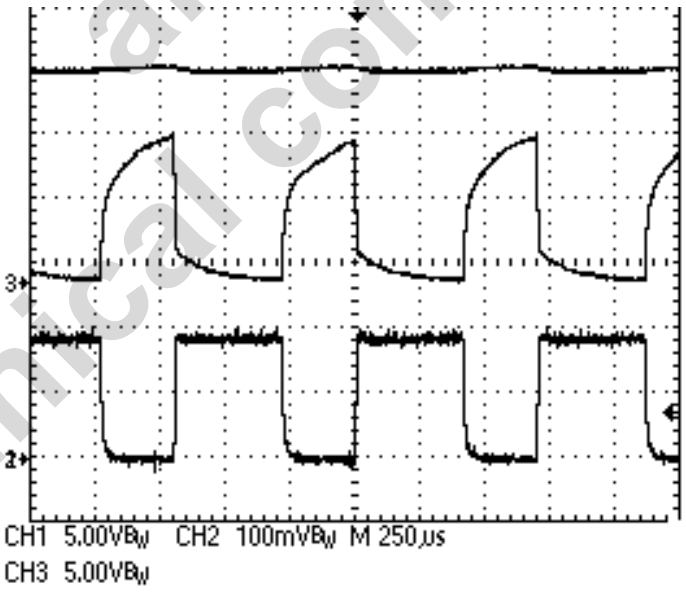
Channel 1 = VREG
Channel 2 = V2_5
Channel3 = Vsupply

6.3 9us Slew Rate



Channel 1 = Voltage on Current Source
Channel 2 + Voltage on RES Pin

6.4 Supply Regulation



Channel 1 = DCDC VOUT (30V)
Channel 2 = Voltage on RES Pin
Channel 3 = Voltage on Curr Pin

7 Block Description

7.1 Feedback Circuit

The AS3693A supports a flexible feedback selection for external DCDC – supplies. Beside the default setup for RGGB lighting, each channel can be assigned to an external DCDC feedback loop. This feedback circuit is important to reduce power dissipation of the device.

Table *6 – Feedback Control*

Addr: 04h		**Feedback control**		
		Enables and Disables the Different Feedback modes		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	Feedback on	0	R/W	1 = Feedback circuit is active 0 = The entire feedback loop is disabled
1	Feedback on PWM	0	R/W	The feedback regulator is only active, if PWM = 1
2	Open_Led_Det_on	0	R/W	Enables open led detection comparators 0 = Open Led Detection disabled 1 = Open Led Detection enabled. Level: Ucurrx = 100mV
3	Short_det_on	0	R/W	Enables short detection 0 = Short detection off 1 = Sort Detection on
4	Short Led Detect Voltage(VSL)		R/W	Short led detection trip voltage (debounced 3mS) 00 = 2V 01 = 3V
7:6	DCDC_regulation_trip Point (VC)	00	R/W	Trip point voltage of the DCDC-feedback regulation circuit. (NOTE: This value has to be adjusted if analog ref select bit is changed.) 00 = 0.5V (Note use for Currents up to 70 mA) 01 = 0.6V (Note use for Currents up to 80 mA) 10 = 0.8V (Note use for Currents up to 110 mA) 11 = 1.0V (Note use for Currents up to 150 mA)

7.1.1 Feedback Selection

In the AS3693A, each led – string feedback can be assigned to the specific led-supply, to minimize the power consumption in the system. It can be chosen in between FBR, FBG and FBB.

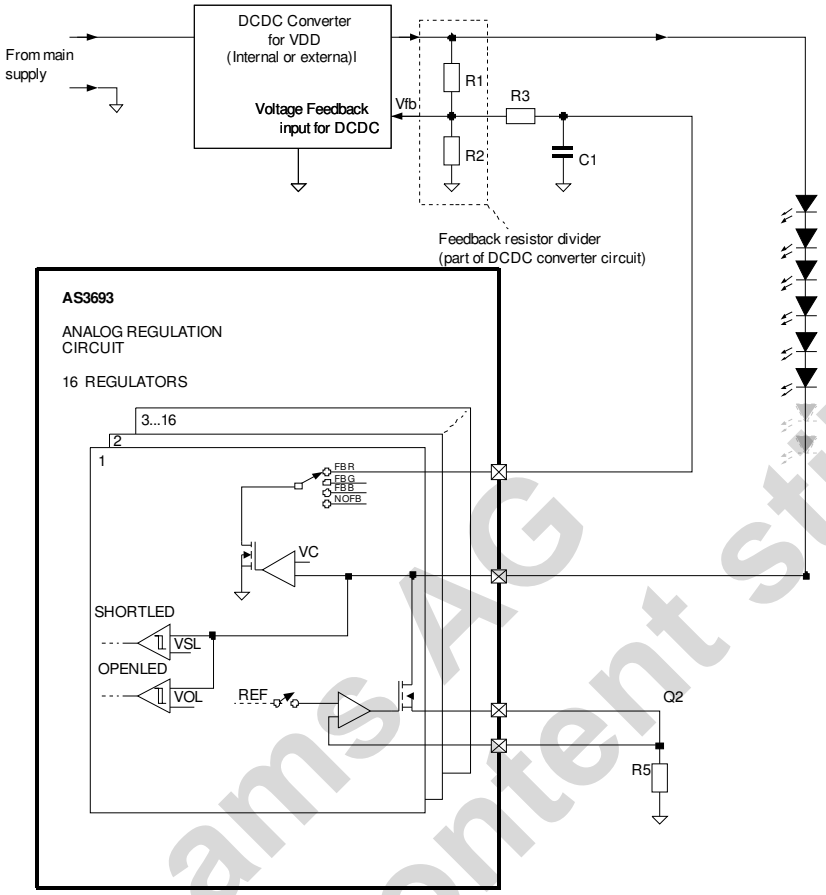


Table 7 – Feedback Selection

Addr: 05h,06h,07h,08h		Feedback Select 1-4		
		This register controls the Feedback of the Automatic feedback loop		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	FB1_Select FB5_Select FB9_Select FB13_Select	00	R/W	Selects the feedback of the voltage regulators 00= regulator on FBR 01= regulator on FBG 10= regulator on FBB 11= regulator not connected to FB
3:2	FB2_Select FB6_Select FB10_Select FB14_Select	00	R/W	Selects the feedback of the voltage regulators 00= regulator on FBR 01= regulator on FBG 10= regulator on FBB 11= regulator not connected to FB
5:4	FB3_Select FB7_Select FB11_Select FB15_Select	00	R/W	Selects the feedback of the voltage regulators 00= regulator on FBR 01= regulator on FBG 10= regulator on FBB 11= regulator not connected to FB
7:6	FB4_Select FB8_Select FB12_Select FB16_Select	00	R/W	Selects the feedback of the voltage regulators 00= regulator on FBR 01= regulator on FBG 10= regulator on FBB 11= regulator not connected to FB

7.1.2 Voltage fault registers

In this registers an open or short led fault can be detected. If an open or short led error occurs, pin fault is pulled to 0 (3 ms debounced).
Remark: At 100% PWM duty cycle, short led fault detection is not available. Please set PWM to 99% duty cycle. Open led fault detection is available at 100% PWM duty cycle.

Table 8 – Fault Registers

Addr: 09h-0ch		**Voltage Fault 1,2,3,4**		
		This register shows a fault on any led string		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	Fault_Reg 1 Fault_Reg 5 Fault_Reg 9 Fault_Reg 13	00	R	Shows a error on any led string 00 = no fault 01 = open led 10 = short led
3:2	Fault_Reg 2 Fault_Reg 6 Fault_Reg 10 Fault_Reg 14	00	R	Shows a error on any led string 00 = no fault 01 = open led 10 = short led
5:4	Fault_Reg 3 Fault_Reg 7 Fault_Reg 11 Fault_Reg 15	00	R	Shows a error on any led string 00 = no fault 01 = open led 10 = short led
7:6	Fault_Reg 4 Fault_Reg 8 Fault_Reg 12 Fault_Reg 16	00	R	Shows a error on any Led string 00 = no Fault 01 = open Led 10 = short Led

7.2 Curreg 1-16

Each current source can be turned on and off separately.

Table 9 –Reg. Control 1

Addr: 01h		Reg. Control1		
		This register enables or disables the curreg 1 - 8		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	Curreg 1-8_ON	00000000	R/W	Enables or disables the current regulators 0 = regulator off 1 = regulator on

Table 10– Reg.Control 2

Addr: 02h		Reg. Control2		
		This Register enables or disables the curreg 9-16		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	Curreg 9 -16_ON	00000000	R/W	Enables or disables the current regulators 0 = regulator off 1 = regulator on

Table 11 –CURREG_CONTROL

Addr: 0dh		Curreg Control		
		Controls Rise, Fall times and References of the Curreg.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	Analog Ref Select	00	R/W	Voltage reference for the current regulators can be chosen with these options. 00 = 250mV reference 01 = external reference 10 = DAC reference 11 = do not use
3:2	SLEW_RATE_CONTROL	00	R/W	SLEW – RATE – Control. Adjusts the rise and fall time of the current switching 00 = typ. 9us 01 = typ. 6us 10 = typ. 3us 11 = typ. 1us
5:4	PWM_LOW_LEVEL	00	R/W	Note: Test bits for internal use only
7	boost mode	0	R/W	Gives +30% current. only available in internal reference mode.

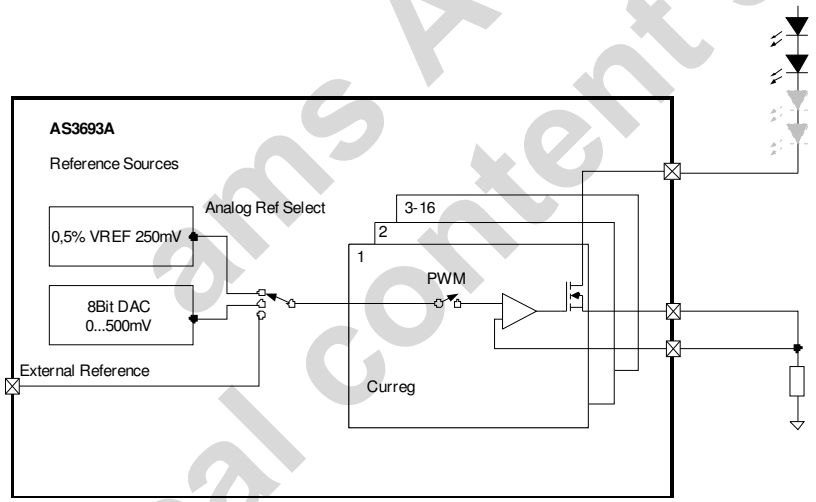


Table 12 – Ref_DAC_Voltage

Addr: 0eh		Ref_DAC_Voltage		
		The Regulation Voltage can be chosen in this register		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7…0	Ref_DAC_Voltage	00	R/W	Reference voltage for current regulators. (Note: If Analog Ref Select = 10, the regulation voltage can be adjusted here. 00000000 = 0mV 00000001 … 01111111 = 250 mV .. 11111111= 500mV

7.3 PWM – modes

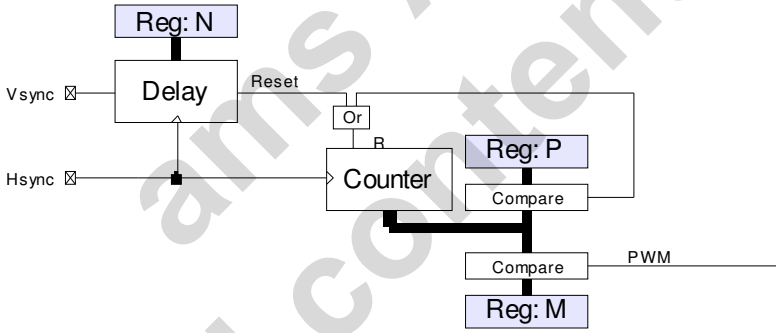
Table 14– PWM CONTROL

Addr: 0fh		PWM_CONTROL		
		Controls the different PWM modes and Internal or external PWM		
Bit	**Bit Name**	**Default**	**Access**	**Description**
1:0	PWM_MODE	01	R/W	00 Sync mode 01 Async - mode 10 Sigma – delta mode 11 not used NOTE: Sync and sigma – delta mode can only be used with PWM INT = 0.
2	PWM INT/EXT	1	R/W	0 PWM generator uses external H and Vsync clock 1 PWM generator uses internal 500kHz clock.
3	VSYNC_INVERT	0	R/W	0 VSYNC active high (PWM triggers on rising edge) 1 VSYNC active low (PWM triggers on falling edge)

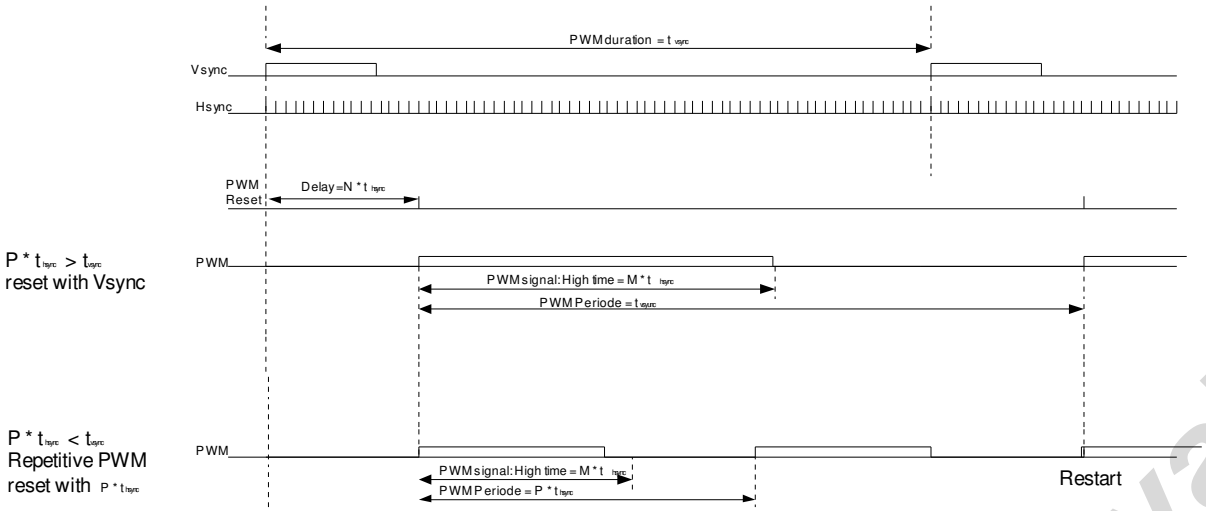
Note: If Vsync or Hsync is not used, connect it to GND.

7.3.1 SYNC mode (PWM_MODE = 00)

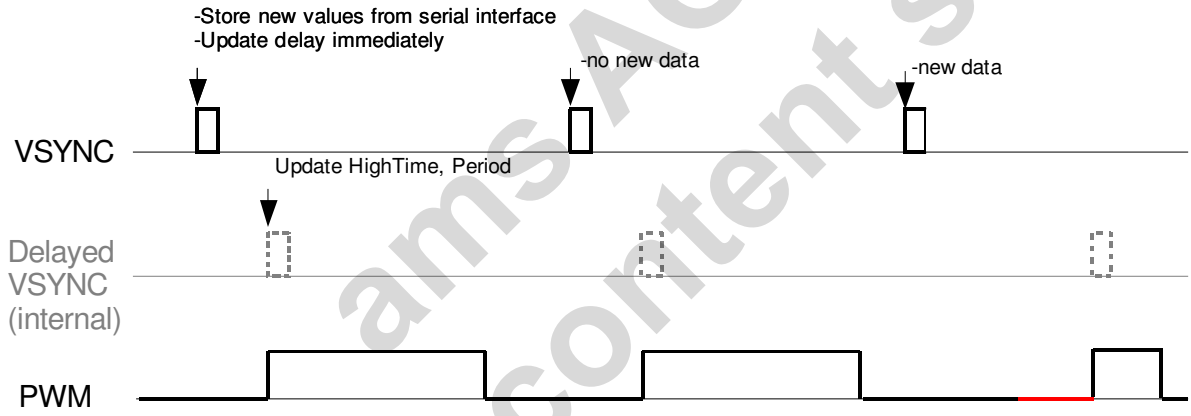
In this mode the PWM is synchronized with VSYNC and HSYNC.

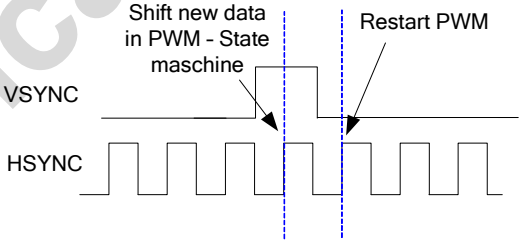


Setup options:
Delay (N) = registers 0h32 to 0h51
High Time (M) = registers 0h12 to 0h31
PWM Period (P) = register 0h10



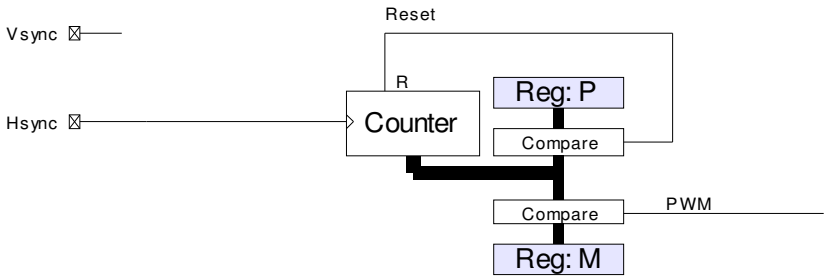
7.3.1.1 SYNC – mode PWM – generator update cycle.



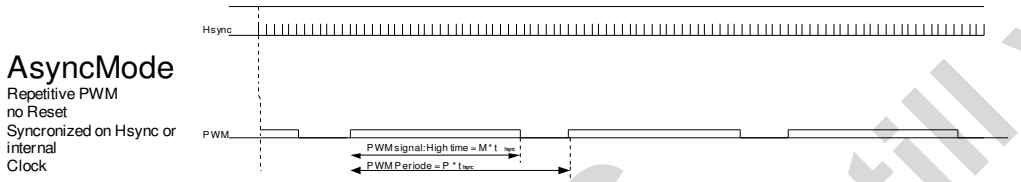


7.3.2 ASYNC – mode (PWM_MODE = 01)

This PWM is synchronized with Hsync or internal 500KHz clock. The registers are updated with each serial data.

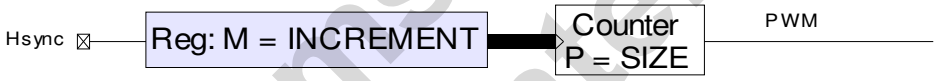


High time (M) = registers 0h12 to 0h 31
PWM period (P) = register 0h10

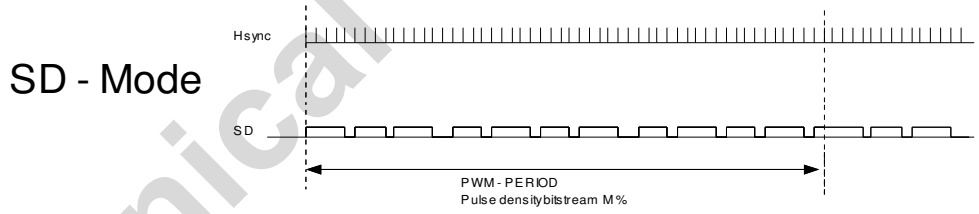


7.3.3 SIGMA DELTA – mode (PWM_MODE = 10)

This PWM is synchronized with Hsync or internal 500KHz clock



Setup options:
Increment (M) = registers 0h12 to 0h 31
Counter size (P) = register 0h10



7.4 PWM – high time, period and delay registers

Table 15 – Curreg1-16_DELAY_LSB

Addr: 32h – 50h		CURREGX_DELAY_LSB		
		Defines delay of the different PWM's		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	CurregX_DELAY_LSB	00000000	R/W	Defines the delay time of the PWM

Table 16 – Curreg1-16_DELAY_MSB

Addr: 32h-51h		CURREGX_DELAY_LSB		
		Defines delay of the different PWM's		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3:0	CurregX_DELAY_MSB	0000	R/W	Defines the delay time of the PWM

Table 17– PWM_PERIOD_LSB

Addr: 10h		PWM – Period – LSB		
		Defines PWM – Periode		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	PWM_PERIOD_LSB	11111111	R/W	Defines the period of the PWM

Table 18– PWM_PERIOD_MSB

Addr: 11h		PWM – Period – MSB		
		Defines PWM – Periode		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3:0	PWM_PERIOD_MSB	0000	R/W	Defines the period of the PWM

Table 19– Curreg1-16_HT_LSB

Addr: 12h-30h		CURREGX_HT_LSB		
		Defines High Time of PWM		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	Curreg1_HT_LSB	0	R/W	Defines PWM high time

Table 20– Curreg1-16_HT_MSB

Addr: 13h-31h		CURREGX_HT_MSB		
		Defines High Time of PWM		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3:0	Curreg1_HT_MSB	0000	R/W	Defines PWM high time

7.5 Shunt Regulator

The supply of the AS3693A is generated from the high voltage supply. To obtain a 5V regulated supply, a series resistor Rvdd is used together with an internal zener diode (ZD1). An external capacitor Cvdd is used to filter the supply on the pin VREG.

The external resistor Rvdd has to be choosen according to the following formula:

$$Rvdd = \frac{VDD_{MIN} - 5{,}4V}{20mA}$$

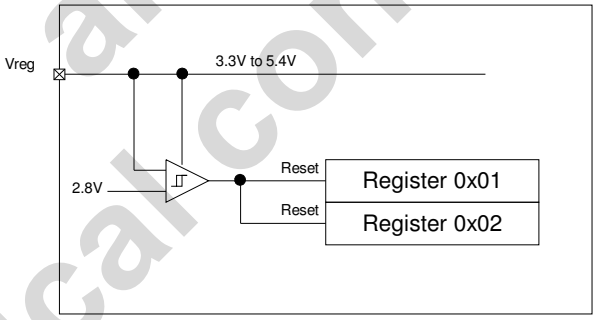
VDD_{MIN} is the minimum voltage of the supply, where Rvdd is connected

This ensures enough supply current ($IVREG_{MAX}$) for the AS3693A under minimum supply voltage VDD_{MIN}.

If a stable 5V supply within the operating conditions limits of $VREG_{EXT}$ is already existing in the system it is possible to supply the AS3693A directly. In this case remove the resistor Rvdd and connected this supply directly to VREG.

7.5.1 Undervoltage lockout

The undervoltage lockout is an additional safety feature to prevent LED-current under abnormal Vreg conditions. If the supply voltage Vreg is below 2.8V (e.g. device is supplied only by the voltage of the serial interface) the device gets a reset.



7.6 Over temperature control

Table 14– Overtemp Control

Addr:55h		Over temperature Control		
		Controls the temperature functions		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	overtemp_on	1	R/W	Enables the over temperature protection 0 = Protection off 1 = Protection on
1	ov_temp	0	R/W	Displays temperature status 0 = Normal operation 1 = Over temperature shutdown

7.7 Device address setup

The I2C and SPI – Device address can be set via PIN ADDR1 and ADDR2. The AS3693A offers 31 I2C or 32 SPI addresses, which can be set via external resistor. ADDR2 bit 2 decides if I2C or SPI interface is used.

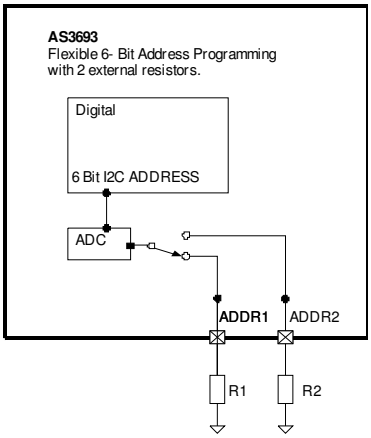


Table 13– Device Address

Device Adress Setup:		I2C ADDRESS		
		I2C ADDRESS Options		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:0	Device ADDR1	000	R	Lower 3 bits of device address 000 open Note: don't use address 00h 001 320kΩ 010 160kΩ 011 80kΩ 100 40kΩ 101 20kΩ 110 10kΩ 111 0Ω
5:3	Device ADDR2	000	R	Upper 3 bits of device address 000 open Note: activates I2C - mode 001 320kΩ Note: activates I2C - mode 010 160kΩ Note: activates I2C - mode 011 80kΩ Note: activates I2C - mode 100 40kΩ Note: activates SPI - mode 101 20kΩ Note: activates SPI - mode 110 10kΩ Note: activates SPI - mode 111 0Ω Note: activates SPI – mode

7.7.1 I2C Device Address setup

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0 (ADDR2<2>)	ADDR2<1>	ADDR2<0>	ADDR1<2>	ADDR1<1>	ADDR1<0>	R/W

7.7.2 SPI Device Address setup

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	1 (ADDR2<2>)	ADDR2<1>	ADDR2<0>	ADDR1<2>	ADDR1<1>	ADDR1<0>

7.8 Digital interface

The AS3693A can be controlled with two types of interfaces.

7.8.1 I2C interface

7.8.1.1 Feature List

- Fast-mode capability (max. SCL-frequency is 400 kHz)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

7.8.1.2 Transfer Formats

Figure *1 – I²C Byte-Write:*

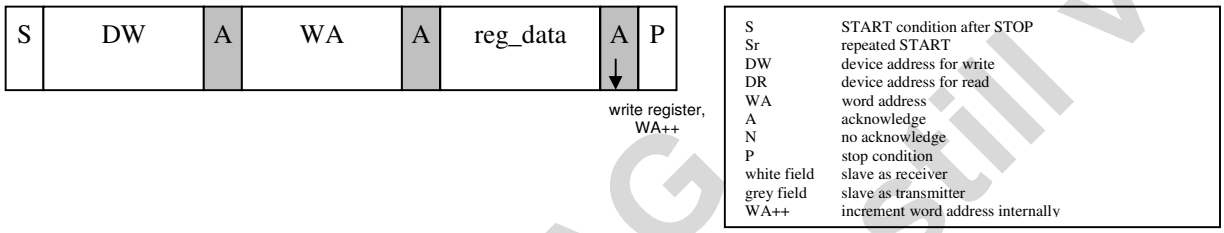
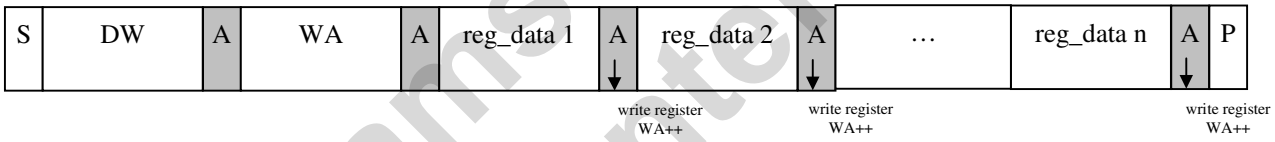


Figure *2 – I²C Page-Write:*

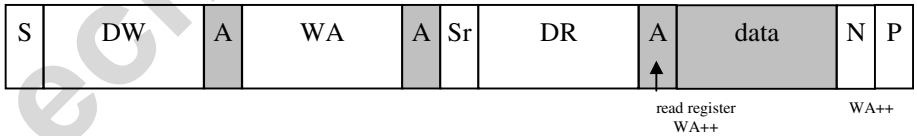


Byte-Write and Page-Write are used to write data to the slave.
The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be send to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read-Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

The diagrams below show various read formats available:

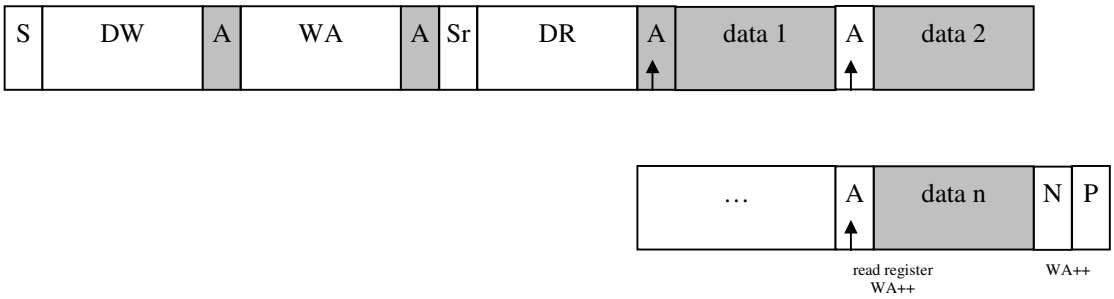
Figure *3 – I²C Random-Read:*



Random-Read and Sequential-Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.
The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes

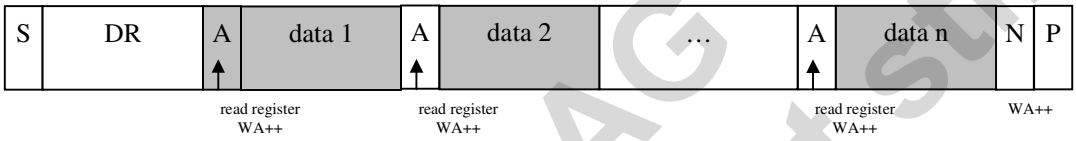
the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure *4 – I²C Sequential-Read:*



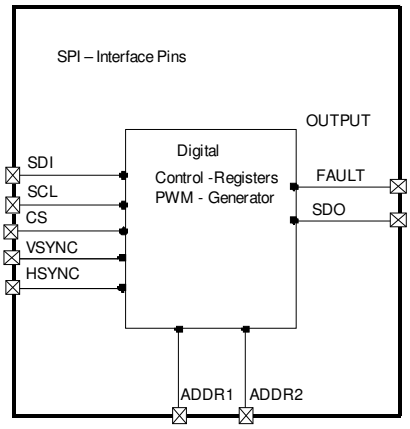
Sequential-Read is the extended form of Random-Read, as more than one register-data bytes are transferred subsequently. In difference to the Random-Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure *5 – I²C Current-Address-Read:*



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random-Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential-Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

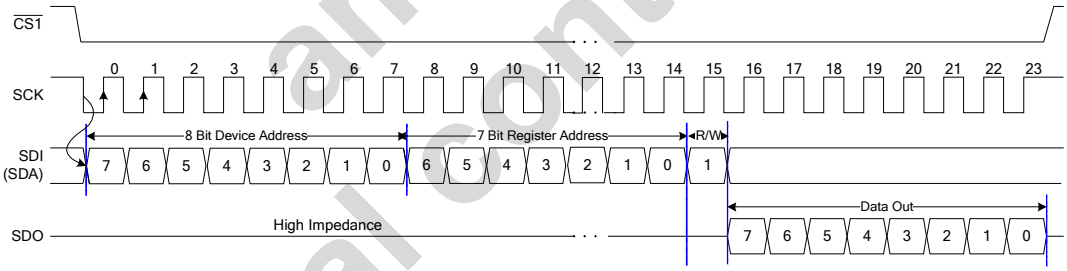
7.8.2 SPI interface



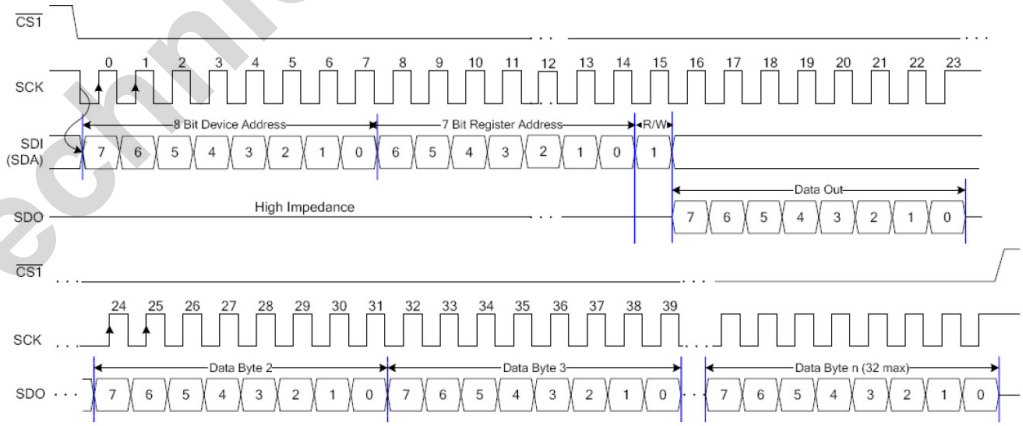
SPI Mode – Digital Interface Pins:

CS(N)	Chip Select input
SDO	Serial Data output
SDI	Serial Data input
SCL	Serial Clock input
VSYNC	Video Sync signal input
HSYNC	Video Sync signal input
ADDR1 ADDR2	Device Address pins (can be set via resistor).

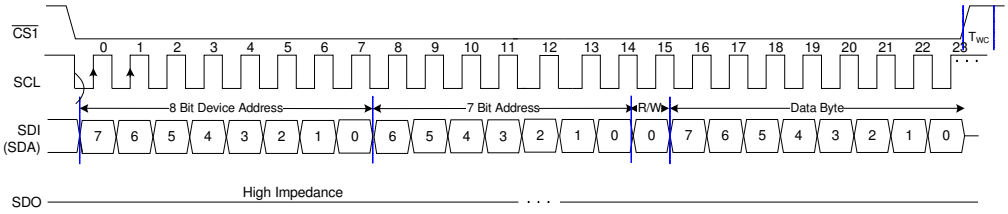
7.8.2.1 Read Sequence



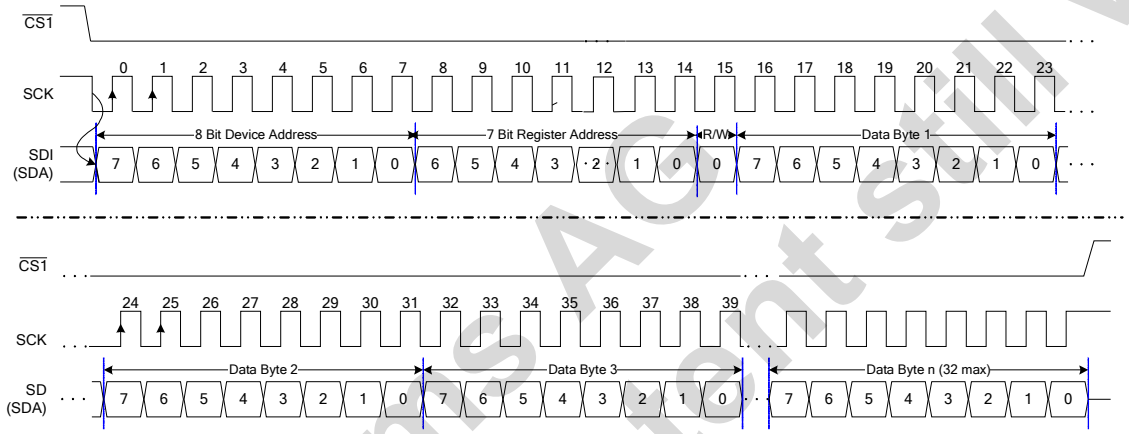
7.8.2.2 Page Read Sequence



7.8.2.3 Write Sequence



7.8.2.4 Page Write Sequence



8 Register map

Name	Addr	Default	B7	b6	b5	B4	b3	b2	b1	b0
Reg. Control1	01h	00h	Curreg 8_ON	Curreg7 _ON	Curreg6 _ON	Curreg5 _ON	Curreg4 _ON	Curreg 3_ON	Curreg 2_ON	Curreg1 _ON
Reg Control 2	02h	00h	Curreg 16_ON	Curreg1 5_ON	Curreg1 4_ON	Curreg1 3_ON	Curreg1 2_ON	Curreg 11_ON	Curreg 10_ON	Curreg9 _ON
Feedback Control	04h	00h	DCDC_REGULATION_TRIP_POINT		Short_Led Detect Voltage		SHORT _DET_ ON	OPEN_ LED _DET _ON	Feedback_on_ PWM	FEEDBACK_ON
Fedback Select 1	05h	00h	FB4_ Select		FB3_ Select		FB2_ Select		FB1_Select	
Fedback Select 2	06h	00h	FB8_ Select		FB7_ Select		FB6_ Select		FB5_ Select	
Fedback Select 3	07h	00h	FB12_ Select		FB11_ Select		FB10_ Select		FB9_ Select	
Fedback Select 4	08h	00h	FB16_ Select		FB15_ Select		FB14_ Select		FB13_ Select	
Voltage_Fault 1	09h	00h	Fault_Reg4		Fault_Reg3		Fault_Reg2		Fault_Reg1	
Voltage_Fault 2	0Ah	00h	Fault_Reg8		Fault_Reg7		Fault_Reg6		Fault_Reg5	
Voltage_Fault 3	0Bh	00h	Fault_Reg12		Fault_Reg11		Fault_Reg10		Fault_Reg9	
Voltage_Fault 4	0Ch	00h	Fault_Reg16		Fault_Reg15		Fault_Reg14		Fault_Reg13	
CURREG_CONTROL	0Dh	00h	boost mode	switch_ output_ driver	PWM_LOW_LEVEL		RC_SEL		Select Ref	
Ref_DAC_Voltage	0Eh	00h	Vref_DAC							
PWM –CONTROL	0Fh	04h					VSYNC _INVERT	PWM-INT/EXT	PWM - MODE	
PWM-PERIOD_LSB	10h	FFh	PWM –PERIOD - LSB							
PWM-PERIOD-MSB	11h	00h					PWM – period - MSB			
Curreg1_HT_LSB	12h	00h	Curreg1_HT_LSB							
Curreg1_HT_MSB	13h	00h					Curreg1_HT_MSB			
Curreg2_HT_LSB	14h	00h	Curreg2_HT_LSB							
Curreg2_HT_MSB	15h	00h					Curreg2_HT_MSB			
Curreg3_HT_LSB	16h	00h	Curreg3_HT_LSB							
Curreg3_HT_MSB	17h	00h					Curreg3_HT_ MSB			
Curreg4_HT_LSB	18h	00h	Curreg4_HT_LSB							
Curreg4_HT_MSB	19h	00h					Curreg4_HT_ MSB			
Curreg5_HT_LSB	1Ah	00h	Curreg5_HT_LSB							
Curreg5_HT_MSB	1Bh	00h					Curreg5_HT_ MSB			
Curreg6_HT_LSB	1Ch	00h	Curreg6_HT_LSB							
Curreg6_HT_MSB	1Dh	00h					Curreg6_HT_ MSB			
Curreg7_HT_LSB	1Eh	00h	Curreg7_HT_LSB							
Curreg7_HT_MSB	1Fh	00h					Curreg7_HT_ MSB			
Curreg8_HT_LSB	20h	00h	Curreg8_HT_LSB							
Curreg8_HT_MSB	21h	00h					Curreg8_HT_ MSB			

Name	Addr	Default	B7	b6	b5	B4	b3	b2	b1	b0
Curreg9_HT_LSB	22h	00h	Curreg9_HT_LSB							
Curreg9_HT_MSB	23h	00h					Curreg9_HT_ MSB			
Curreg10_HT_LSB	24h	00h	Curreg10_HT_LSB							
Curreg10_HT_MSB	25h	00h					Curreg10_HT_ MSB			
Curreg11_HT_LSB	26h	00h	Curreg11_HT_LSB							
Curreg11_HT_MSB	27h	00h					Curreg11_HT_ MSB			
Curreg12_HT_LSB	28h	00h	Curreg12_HT_LSB							
Curreg12_HT_MSB	29h	00h					Curreg12_HT_MSB			
Curreg13_HT_LSB	2Ah	00h	Curreg13_HT_LSB							
Curreg13_HT_MSB	2Bh	00h					Curreg13_HT_MSB			
Curreg14_HT_LSB	2Ch	00h	Curreg14_HT_LSB							
Curreg14_HT_MSB	2Dh	00h					Curreg14_HT_MSB			
Curreg15_HT_LSB	2Eh	00h	Curreg15_HT_LSB							
Curreg15_HT_MSB	2Fh	00h					Curreg15_HT_MSB			
Curreg16_HT_LSB	30h	00h	Curreg16_HT_LSB							
Curreg16_HT_MSB	31h	00h					Curreg16_HT_MSB			
Curreg1_DELAY_LSB	32h	00h	Curreg1_DELAY_LSB							
Curreg1_ DELAY_MSB	33h	00h					Curreg1_DELAY_MSB			
Curreg2_ DELAY_LSB	34h	00h	Curreg2_DELAY_LSB							
Curreg2_ DELAY_MSB	35h	00h					Curreg2_DELAY_MSB			
Curreg3_ DELAY_LSB	36h	00h	Curreg3_DELAY_LSB							
Curreg3_ DELAY_MSB	37h	00h					Curreg3_DELAY_ MSB			
Curreg4_ DELAY_LSB	38h	00h	Curreg4_DELAY_LSB							
Curreg4_ DELAY_MSB	39h	00h					Curreg4_DELAY_ MSB			
Curreg5_DELAY_LSB	3Ah	00h	Curreg5_DELAY_LSB							
Curreg5_DELAY_MSB	3Bh	00h					Curreg5_DELAY_ MSB			
Curreg6_DELAY_LSB	3Ch	00h	Curreg6_DELAY_LSB							
Curreg6_DELAY_MSB	3Dh	00h					Curreg6_DELAY_ MSB			
Curreg7_DELAY_LSB	3Eh	00h	Curreg7_DELAY_LSB							
Curreg7_DELAY_MSB	3Fh	00h					Curreg7_DELAY_ MSB			
Curreg8_DELAY_LSB	40h	00h	Curreg8_DELAY_LSB							
Curreg8_DELAY_MSB	41h	00h					Curreg8_DELAY_ MSB			

Name	Addr	Default	B7	b6	b5	B4	b3	b2	b1	b0
Curreg9_DELAY_LSB	42h	00h	Curreg9_DELAY_LSB							
Curreg9_DELAY_MSB	43h	00h					Curreg9_DELAY_ MSB			
Curreg10_DELAY_LSB	44h	00h	Curreg10_DELAY_LSB							
Curreg10_DELAY_MSB	45h	00h					Curreg10_DELAY_ MSB			
Curreg11_DELAY_LSB	46h	00h	Curreg11_DELAY_LSB							
Curreg11_DELAY_MSB	47h	00h					Curreg11_DELAY_ MSB			
Curreg12_DELAY_LSB	48h	00h	Curreg12_DELAY_LSB							
Curreg12_DELAY_MSB	49h	00h					Curreg12_DELAY_MSB			
Curreg13_DELAY_LSB	4Ah	00h	Curreg13_DELAY_LSB							
Curreg13_DELAY_MSB	4Bh	00h					Curreg13_DELAY_MSB			
Curreg14_DELAY_LSB	4Ch	00h	Curreg14_DELAY_LSB							
Curreg14_DELAY_MSB	4Dh	00h					Curreg14_DELAY_MSB			
Curreg15_DELAY_LSB	4Eh	00h	Curreg15_DELAY_LSB							
Curreg15_DELAY_MSB	4Fh	00h					Curreg15_DELAY_MSB			
Curreg16_DELAY_LSB	50h	00h	Curreg16_DELAY_LSB							
Curreg16_DELAY_MSB	51h	00h					Curreg16_DELAY_LSB			
Overtemp control	55h	01h							ov_temp	ov_temp_on
ASIC ID1	5Ch	CAh	1	1	0	0	1	0	1	0
ASIC ID2	5Dh	57h	0	1	0	1	REVISION			

9 Pinout and Packaging

9.1 Pinout

Table 5 – Pinlist

Pin	Name	Type	Description
1	RES1	AIO	Connect to current set resistor R1
2	CURR1	AIO	Current Source 1 output
3	FBG	AIO	Automatic supply regulation for GREEN led strings; if not used, leave open
4	FBB	AIO	Automatic supply regulation for BLUE led strings; if not used, leave open
5	REF(EXT)	AI	Reference pin for PWM = 1 voltage, if not used leave open
6	GND(SENSE)	AIO	GND supply connection (sense)
7	VREG	AIO	Shunt regulator supply; connect to Rvdd and Cvdd
8	V2_5	AIO	Digital supply, connect 1uF blocking capacitor
9	ADDR2	AIO	Connect to external resistor for serial interface address selection,
10	ADDR1	AIO	Connect to external resistor for serial interface address selection.
11	CURR2	AIO	Current Source 2 output
12	RES2	AIO	Connect to current set resistor R2
13	RES3	AIO	Connect to current set resistor R3
14	CURR3	AIO	Current Source 3 output
15	RES4	AIO	Connect to current set resistor R4
16	CURR4	AIO	Current Source 4 output
17	RES5	AIO	Connect to current set resistor R5
18	CURR5	AIO	Current Source 5 output
19	CURR6	AIO	Current Source 6 output
20	RES6	AIO	Connect to current set resistor R6
21	CURR7	AIO	Current Source 7 output
22	RES7	AIO	Connect to current set resistor R7
23	CURR8	AIO	Current Source 8 output
24	RES8	AIO	Connect to current set resistor R8
25	RES9	AIO	Connect to current set resistor R9
26	CURR9	AIO	Current Source 9 output
27	FBR	AIO	Automatic supply regulation for RED led strings; if not used, leave open
28	VSYNC	DI	Video sync signal , **NOTE: Connect to GND in ASYNC MODE**
29	HSYNC	DI	Video sync signal or external clock input in ASYNC mode
30	CS	DI	SPI : CS – function, I2C: connect to GND
31	SCL	DI	SPI/ I2C: Serial interface clock input.
32	SDA	DI	SPI/ I2C: Serial interface data I/O.
33	SDO	DO	SPI: digital data output, I2C: leave open
34	FAULT	DO	FAULT PIN, open drain output. Connect pull up resistor to V2_5

Table 5 – Pinlist

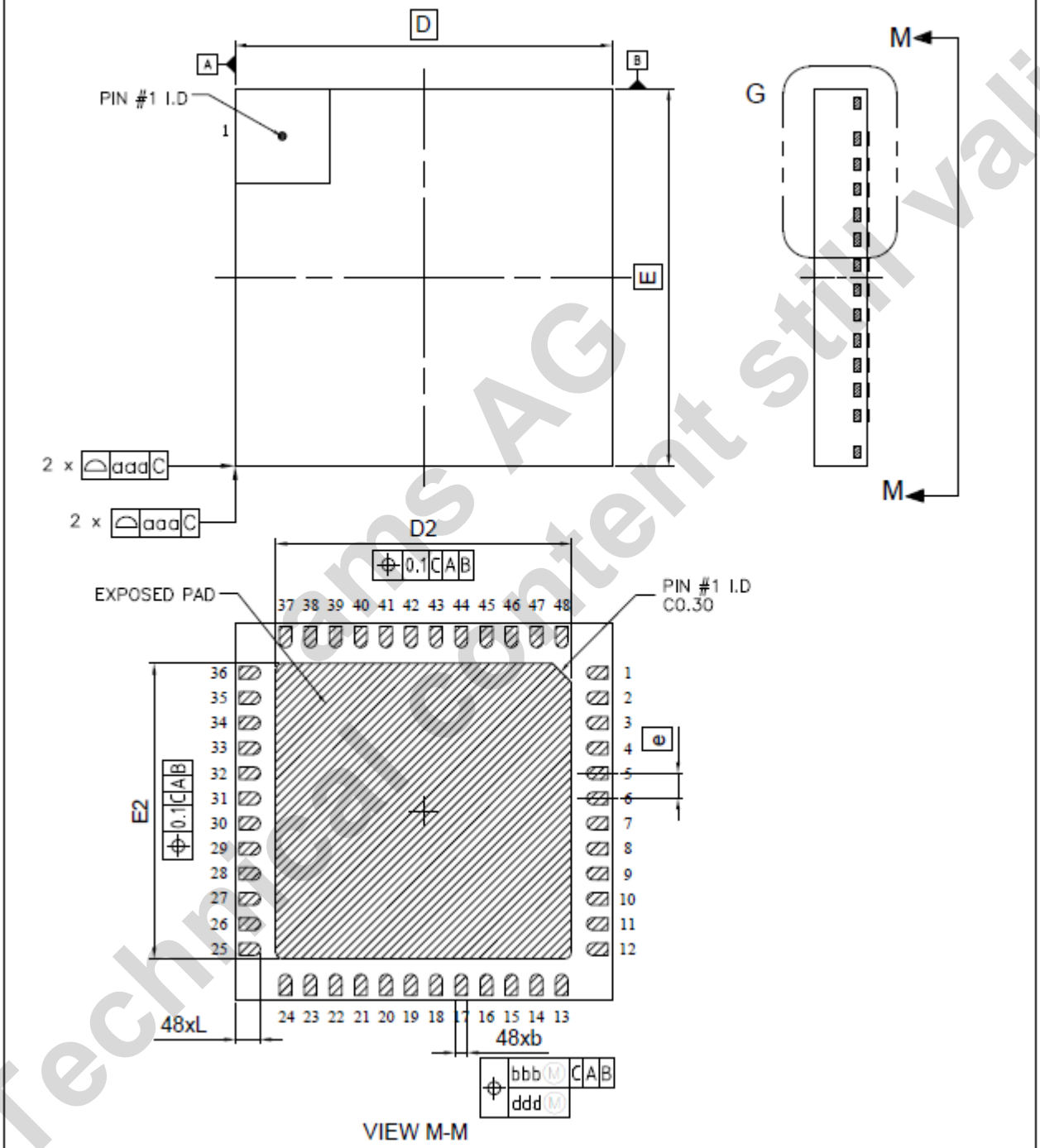
Pin	Name	Type	Description
35	CURR10	AIO	Current Source 10 output
36	RES10	AIO	Connect to current set resistor R10
37	RES11	AIO	Connect to current set resistor R11
38	CURR11	AIO	Current Source 11 output
39	RES12	AIO	Connect to current set resistor R12
40	CURR12	AIO	Current Source 12 output
41	RES13	AIO	Connect to current set resistor R13
42	CURR13	AIO	Current Source 13 output
43	CURR14	AIO	Current Source 14 output
44	RES14	AIO	Connect to current set resistor R14
45	CURR15	AIO	Current Source 15 output
46	RES15	AIO	Connect to current set resistor R15
47	CURR16	AIO	Current Source 16 output
48	RES16	AIO	Connect to current set resistor R16
49 (EP)	GND	S	VSS Supply connection; add as many vias to ground plane as possible.

AIO…Analog pin
DI…Digital input. Protected with clamp to 2.5V
DO…Digital output. Protected with clamp to 2.5V
S… VSS supply

Note: Connect any unused current output channel as follows:
- CURRx = open, Resx = GND

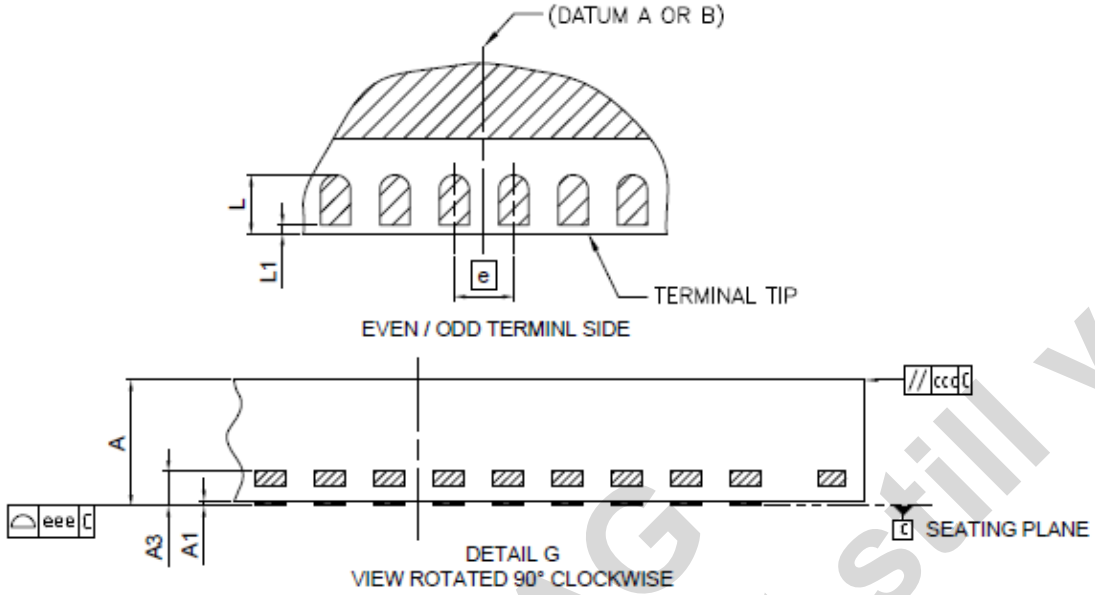
9.2 Package drawing QFN48, 6x6mm, 0.4mm pitch

ASE Advanced Semiconductor Engineering Korea, Inc.	PACKAGE OUTLINE	DWG NO.	98SPP48069A
		ISSUE	XO1
		DATE	MAR.06,2009



TITLE: QFN 6X6 48LD 4.90 X 4.90 PAD	COMPANY	ASE KOREA
	SHEET	1 OF 3

ASE Advanced Semiconductor Engineering Korea, Inc.	PACKAGE OUTLINE	DWG NO.	98SPP48069A
		ISSUE	XO1
		DATE	MAR.06,2009



DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D		6.00 BSC	
E		6.00 BSC	
D2	4.60	4.70	4.80
E2	4.60	4.70	4.80
e		0.40 BSC	
L	0.35	0.40	0.45
L1	0.00		0.10
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

TITLE: QFN 6X6 48LD 4.90 X 4.90 PAD	COMPANY	ASE KOREA
	SHEET	2 OF 3

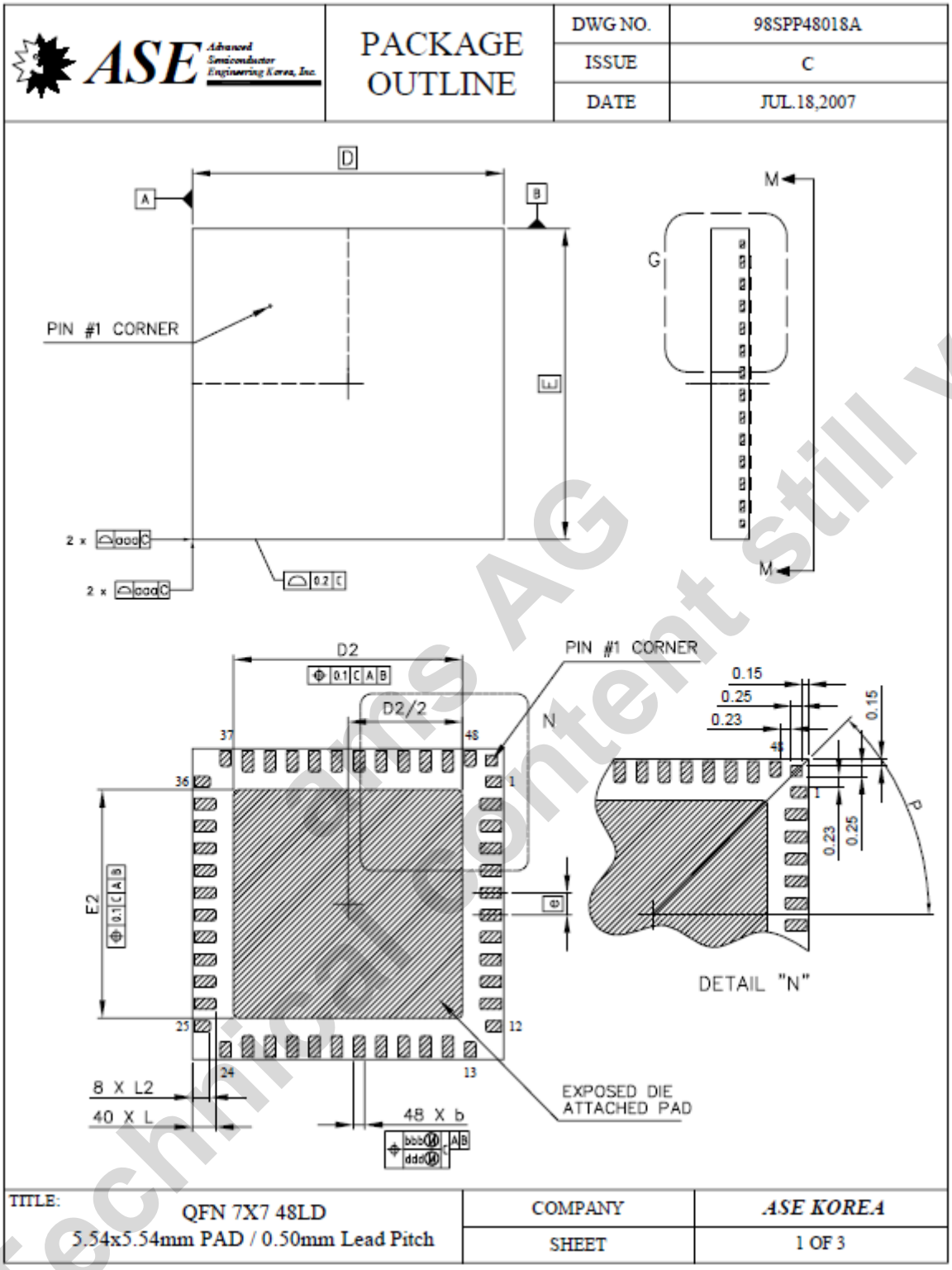
ASE Advanced Semiconductor Engineering Korea, Inc.	PACKAGE OUTLINE	DWG NO.	98SPP48069A
		ISSUE	XO1
		DATE	MAR.06,2009

REVISION HISTORY ;

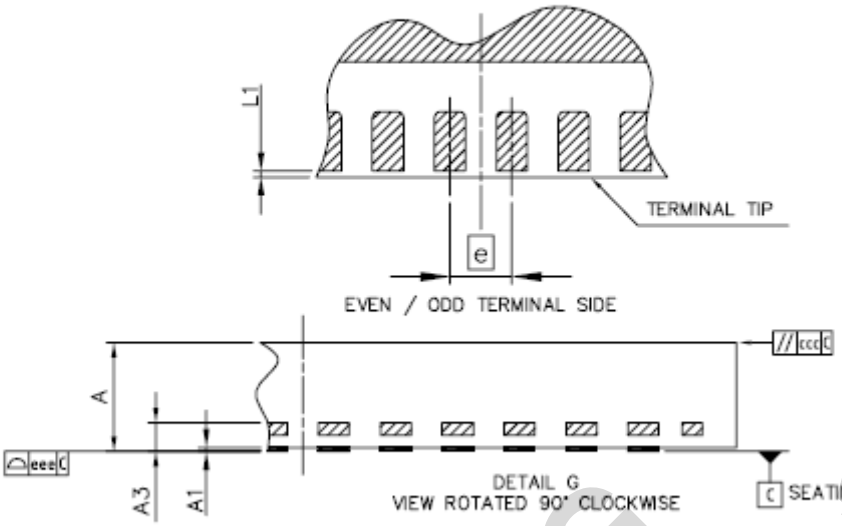
REV	DESCRIPTION	PREPARED BY	REVIEWED BY
XO1	Initial issue	J.S.Park/Mar.06,2009	S.M.Kwon/Mar.06,2009

TITLE: QFN 6X6 48LD 4.90 X 4.90 PAD	COMPANY	ASE KOREA
	SHEET	3 OF 3

9.3 Package drawing QFN48, 7x7mm, 0.5mm pitch



ASE Advanced Semiconductor Engineering Korea, Inc.	PACKAGE OUTLINE	DWG NO.	98SPP48018A
		ISSUE	C
		DATE	JUL.18,2007



DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00		0.05
A3		0.203 REF	
b	0.18	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
D2	5.04	5.14	5.24
E2	5.04	5.14	5.24
e		0.50 BSC	
L	0.48	0.53	0.58
L1	0.00		0.10
L2	0.35	0.40	0.45
P		45° BSC	
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.

4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

5.0 RADIUS ON TERMINAL IS OPTIONAL.

TITLE: QFN 7X7 48LD 5.54x5.54mm PAD / 0.50mm Lead Pitch	COMPANY	ASE KOREA
	SHEET	2 OF 3

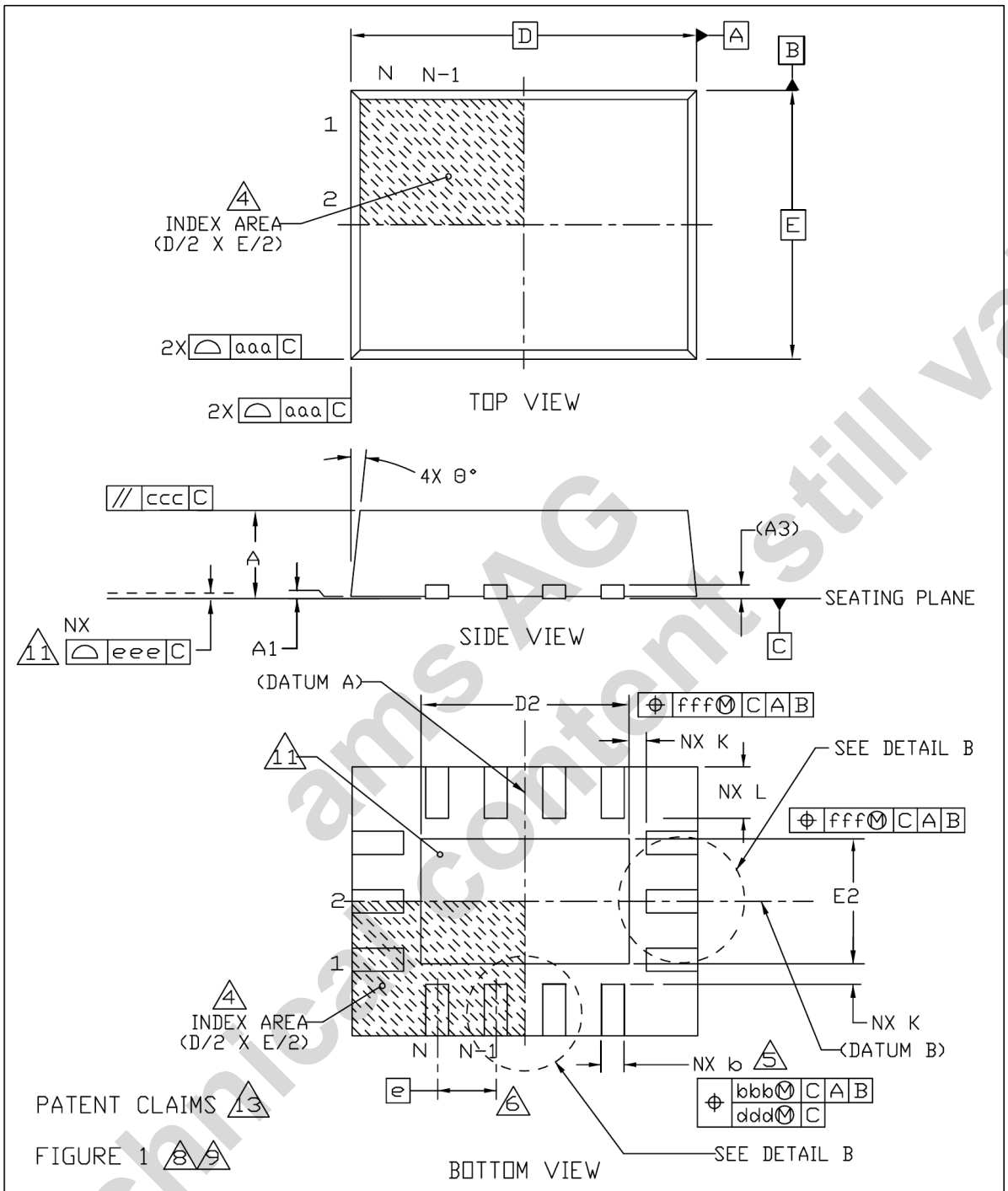
ASE Advanced Semiconductor Engineering Korea, Inc.	PACKAGE OUTLINE	DWG NO.	98SPP48018A
		ISSUE	C
		DATE	JUL.18,2007

REVISION HISTORY ;

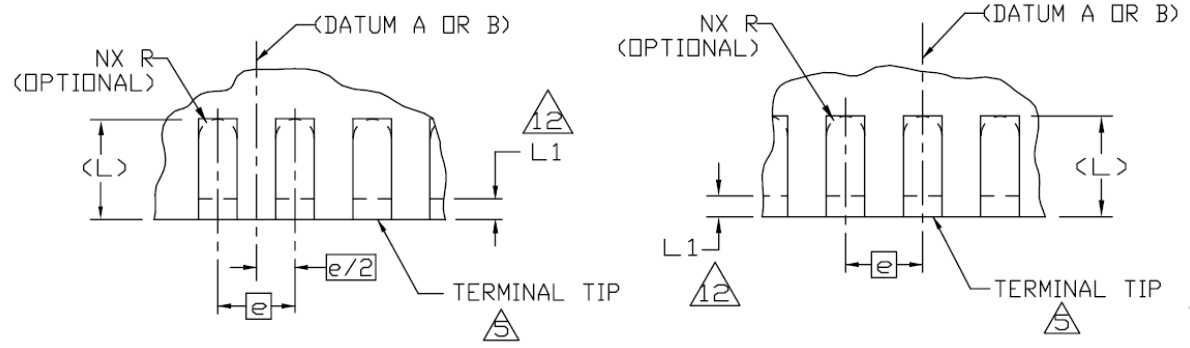
REV	DESCRIPTION	PREPARED BY	REVIEWED BY
O	INITIAL ISSUE	Feb.13,2003/ S.B.Park	Feb.13,2003/HyungJ.Park
A	Change PKG thickness from 0.90+/-0.10mm to 0.85+/-0.05mm	Jan.19,2004/ S.B.Park	Jan.19,2004/HyungJ.Park
B	1. Change Dim "A" from 0.85+0.15/-0.05mm to 0.85+/-0.05mm 2. Add Dim "A1" . 3. Change Dim "L" from 0.53+/-0.10mm to 0.53+/-0.05mm 4. Change Dim "L2" from 0.40+/-0.10mm to 0.40+/-0.05mm	Apr.15,2005/H.J.Han	Apr.15,2005/S.B.Park
C	1. Add the pin #1 i.d dimension 2. Add the dim 'bbb, ddd, eee'	Jul.18,2007/H.J.Han	Jul.18,2007/Y.J.Chong

TITLE: QFN 7X7 48LD 5.54x5.54mm PAD / 0.50mm Lead Pitch	COMPANY	ASE KOREA
	SHEET	3 OF 3

9.4 Package Drawing MLF48



JEDEC SOLID STATE PRODUCT OUTLINE	THIS REGISTERED OUTLINE HAS BEEN PREPARED BY THE JEDEC JC-II COMMITEE AND REFLECTS A PRODUCT WITH ANTICIPATED USAGE IN THE ELECTRONICS INDUSTRY; CHANGES ARE LIKELY TO OCCUR				
THERMALLY ENHANCED PLASTIC VERY THIN AND VERY VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE	JESD-30 DESIGNATOR H(V,W)F-PQFN	ISSUE K	DATE JUNE 2006	**MO- 220**	PAGE 1 OF 20



DETAIL B

MLF 7x7, 0.5mm pitch:
Package Type: VKKD-4,6,8
Body size: 7x7mm
Lead pitch: 0.5mm

MLF 6x6, 0.4mm pitch:
Package Type: VJJE/VJJE-1
Body size: 6x6mm
Lead pitch: 0.4mm

TABLE 8G

e=0.50 PITCH											
VARIATION / SYMBOL		VKKD WKKD	VKKD-1 WKKD-1	VKKD-2 WKKD-2	VKKD-3 WKKD-3	VKKD-4 WKKD-4	VKKD-5 WKKD-5	VKKD-6 WKKD-6	VKKD-7 WKKD-7	VKKD-8 WKKD-8	NOTE
D BSC		7.00	7.00	7.00	7.00	7.00	7.00	7.00	7.00	7.00	
E BSC		7.00	7.00	7.00	7.00	7.00	7.00	7.00	7.00	7.00	
D1 BSC		–	6.75	6.75	–	–	–	–	–	–	9
E1 BSC		–	6.75	6.75	–	–	–	–	–	–	9
D2	MIN	5.50	2.25	2.25	5.50	5.50	3.40	1.25	3.40	5.00	
	NOM	5.65	4.70	4.70	5.65	5.65	–	–	–	5.10	
	MAX	5.80	5.25	5.25	5.80	5.80	5.30	5.45	5.30	5.20	
E2	MIN	5.50	2.25	2.25	5.50	5.50	3.40	1.25	3.40	5.00	
	NOM	5.65	4.70	4.70	5.65	5.65	–	–	–	5.10	
	MAX	5.80	5.25	5.25	5.80	5.80	5.30	5.45	5.30	5.20	
L	MIN	0.35	0.35	0.30	0.35	0.35	0.35	0.45	0.35	0.35	
	NOM	0.40	0.55	0.40	0.40	0.40	0.55	0.50	0.55	0.55	
	MAX	0.45	0.75	0.50	0.45	0.45	0.75	0.55	0.75	0.75	
N		40	44	48	44	48	44	48	44	48	7.3
ND		10	11	12	11	12	12	12	10	11	6
NE		10	11	12	11	12	10	12	12	13	6
NOTES		1,2,10	1,2,10	1,2,10	1,2,10	1,2,10	1,2,10	1,2,10	1,2,10	1,2,10	
REF		11-640	11-534	11-534	11-640	11-640	11-684	11-648	11-684	11-684	
ISSUE		F	A	A	F	F	I	G	I	I	

TABLE 9A

e=0.40 PITCH											
VARIATION / SYMBOL		VEEE	VEEE-1	VGGE	VHHE	VHHE-1	VJJE	VJJE-1	VGHE	VGHE-1	NOTE
		WEEE	WEEE-1	WGGE	WHHE	WHHE-1	WJJE	WJJE-1	WGHE	WGHE-1	
D BSC		3.00	3.00	4.00	5.00	5.00	6.00	6.00	4.00	4.00	
E BSC		3.00	3.00	4.00	5.00	5.00	6.00	6.00	5.00	5.00	
D1 BSC		———	2.75	3.75	4.75	———	5.75	5.75	4.75	4.75	9
E1 BSC		———	2.75	3.75	4.75	———	5.75	5.75	5.75	5.75	9
D2	MIN	0.95	0.95	1.95	2.95	3.45	3.95	4.45	2.30	2.30	
	NOM	1.10	1.10	2.10	3.10	3.60	4.10	4.60	2.50	2.50	
	MAX	1.25	1.25	2.25	3.25	3.75	4.25	4.75	2.70	2.70	
E2	MIN	0.95	0.95	1.95	2.95	3.45	3.95	4.45	3.30	3.30	
	NOM	1.10	1.10	2.10	3.10	3.60	4.10	4.60	3.50	3.50	
	MAX	1.25	1.25	2.25	3.25	3.75	4.25	4.75	3.70	3.70	
L	MIN	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30	
	NOM	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	0.40	
	MAX	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	0.50	
N		20	16	28	36	40	48	48	32	34	7,3
ND		5	4	7	9	10	12	12	7	7	6
NE		5	4	7	9	10	12	12	9	10	6
NOTES		1,2,10	1,2,10	1,2,10	1,2,10	1,2,10	1,2,10	1,2,10	1,2,10	1,2,10	
REF		11-743	11-743	11-743	11-743	11-743	11-743	11-743	11-743	11-743	
ISSUE		K	K	K	K	K	K	K	K	K	

TABLE 2

COMMON DIMENSIONS							
	V: VERY THIN			W: VERY VERY THIN			
SYMBOL	*MIN*	*NOM*	*MAX*	*MIN*	*NOM*	*MAX*	
A	0.80	0.90	1.00	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	
A2	0	0.65	1.00	0	0.55	0.80	9
A3	–	0.20 REF	–	–	0.20 REF	–	
L1	0.00	–	0.15	0.00	–	0.15	12
θ	0°	–	14°	0°	–	14°	
K	0.20	–	–	0.20	–	–	
R	b MIN/2	–	–	b MIN/2	–	–	
NOTES	1,2						
REF	11-684						
ISSUE	I						

TABLE 3

LEAD WIDTH			
b			
PITCH	*MIN*	*NOM*	*MAX*
1.00	0.30	0.40	0.45
0.80	0.25	0.30	0.35
0.65	0.25	0.30	0.35
0.50	0.18	0.25	0.30
0.40	0.15	0.20	0.25
NOTES	5,14		
REF	11-534		
ISSUE	A		

TABLE 4

TOLERANCE OF FORM & POSITION		
symbol \ pitch	0.40mm	>0.40mm
aaa	0.10	0.15
bbb	0.07	0.10
ccc	0.10	0.10
ddd	0.05	0.05
eee	0.08	0.08
fff	0.10	0.10
NOTES	1,2	
REF	11-743	
ISSUE	K	

EXAMPLE: A 20-TERMINAL PQFN WHICH IS 5 mm LONG (DIMENSION D) BY 5 mm WIDE (DIMENSION E) AND 0.65 mm PITCH WILL BE VARIATION HHC.

JEDEC SOLID STATE PRODUCT OUTLINE	THERMALLY ENHANCED PLASTIC VERY THIN AND VERY VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE	ISSUE K	DATE JUNE 2006	**MO- 220**	PAGE 4 OF 20

10 Ordering Information

Table 6 – Ordering Information

Part Number	Marking	Package Type	Delivery Form	Description
AS3693A-ZQFT-6x6	AS3693A	QFN48 6x6mm 0.4mm pich	Tape & Reel	Package size = 6x6mm Pitch = 0.4mm, Pb-Free
AS3693A-ZQFT-7x7	AS3693A	QFN48 7x7mm 0.5mm pich	Tape & Reel	Package size = 7x7mm Pitch = 0.5mm, Pb-Free
AS3693A-ZMFT-6x6	AS3693A	MLF48 6x6mm 0.4mm pich	Tape & Reel	Package size = 6x6mm Pitch = 0.4mm, Pb-Free
AS3693A-ZMFT-7x7	AS3693A	MLF48 7x7mm 0.5mm pich	Tape & Reel	Package size = 7x7mm Pitch = 0.5mm, Pb-Free

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