AS3820

16 Channel White LED Controller for LCD Backlight

General Description

The AS3820 is a 16 channels precision LED controller for use in LCD-backlight panels.

Dynamic power feedback controls the external power supply to guarantee best efficiency. Built-in safety features include thermal shutdown as well as open and short LED detection. The device is programmable via serial interface.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3820, 16 Channel White LED Controller, are listed below:

Figure 1:
Added Value of Using AS3820

Benefits	Features
• All LED backlight topologies	• No limit of VLED or ILED, device is not exposed to high voltage/high current
• Optimum power savings through local dimming	• 16 fully flexible 12 bit PWM generators (period, high time, delay, revers)
• Highest brightness uniformity	• One global high accurate 10 bit DAC which sets the LED current (±0.5% accuracy)
• Full platform approach	• Dedicated device family (AS382x)(1) is available with different number of channels, all SW compatible
• Global dimming mode available	• AS3820E is pre-programed to external PWM mode. VSYNC pin is used as PWM input
• Synchronization with TV frame	• VSYNC and HSYNC inputs available as well as a digital PLL integrated (2)
• Lowest BOM	• Due to 2 pin concept of the output channel: no HV protection, no cascade FETs
• Digital enhanced DC-DC feedback	• Feedback function is compatible to every DC-DC architecture and configurable via SPI (2)
• On chip safety features	• Short/open LED detection, temperature shutdown, register lock/unlock, SPI transfer checksum

Note(s):

1. The device family AS382x includes AS3820, AS3821, AS3822, AS3823.
2. **ams** system patent

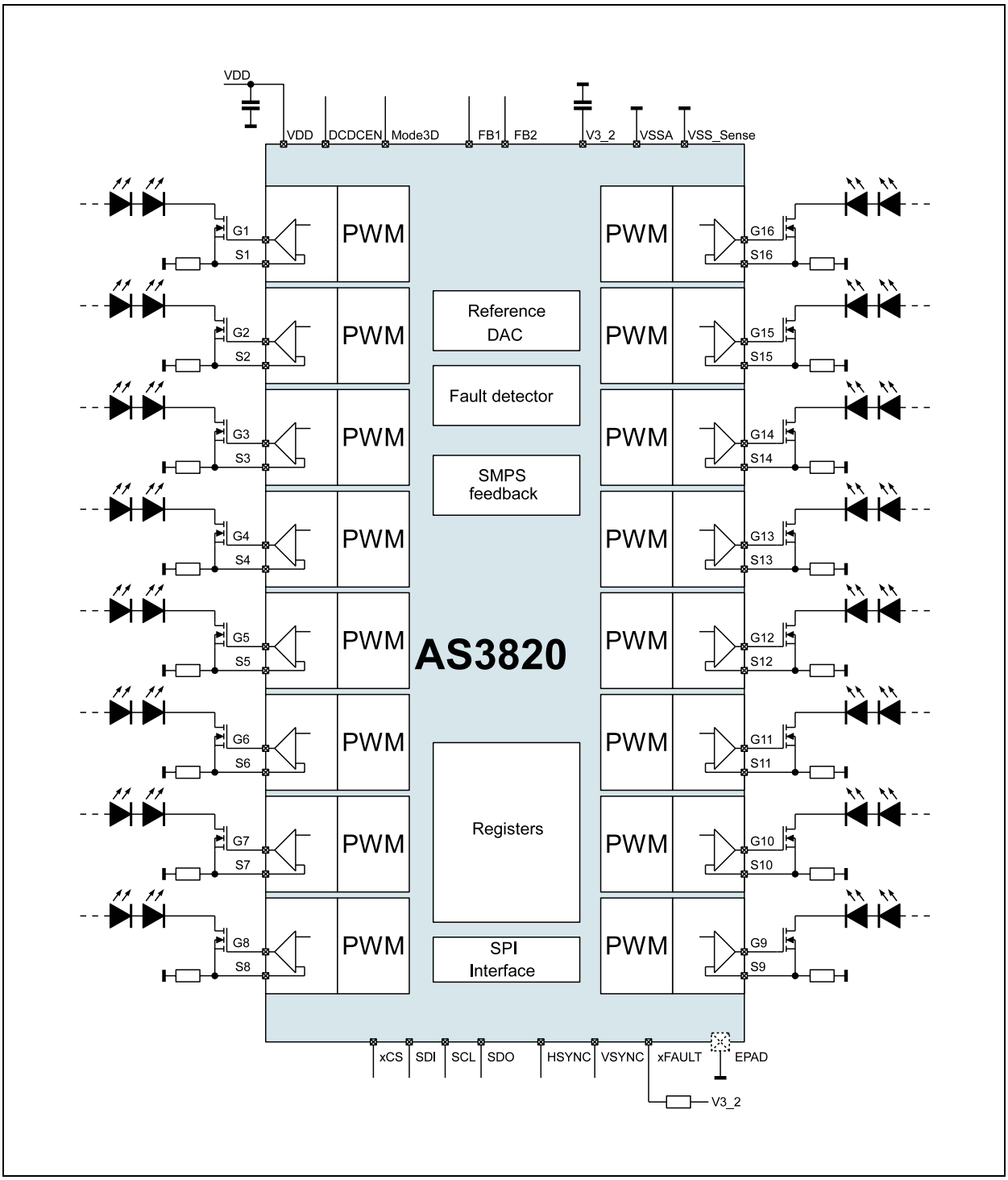
Applications

The AS3820 is suitable for LED backlighting for LCD such as TV sets and monitors.

Block Diagram

The functional blocks of this device are shown below:

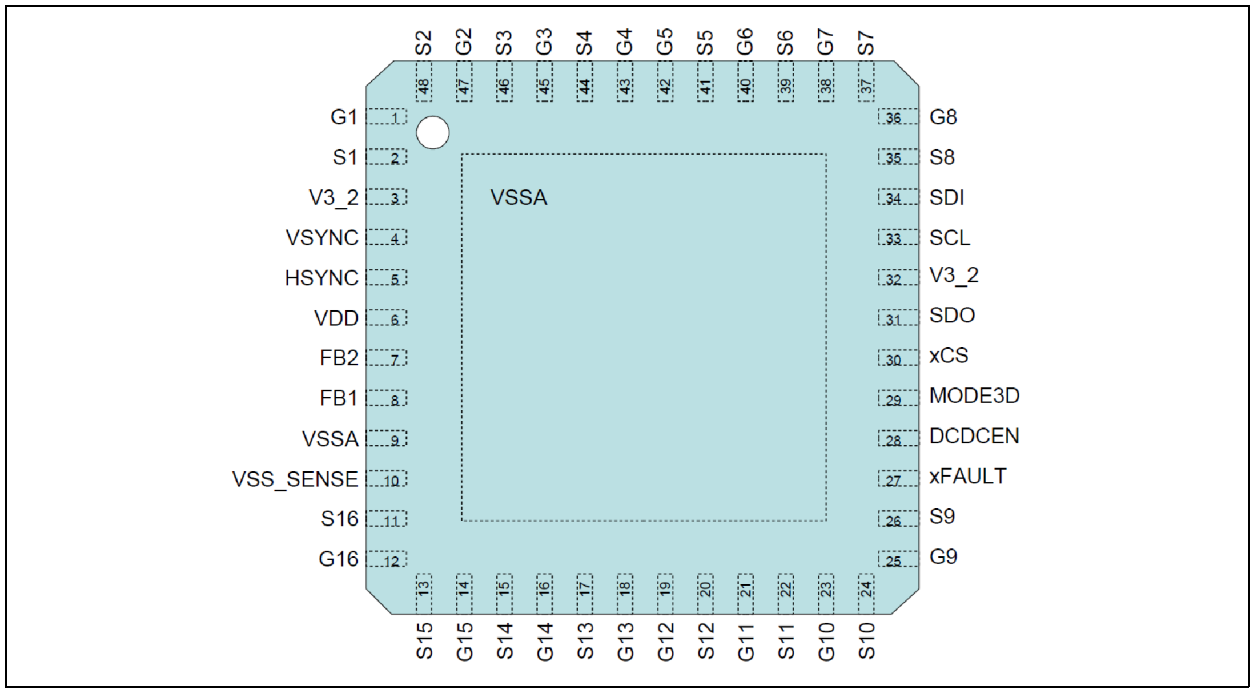
Figure 2:
AS3820 Block Diagram



Pin Assignments

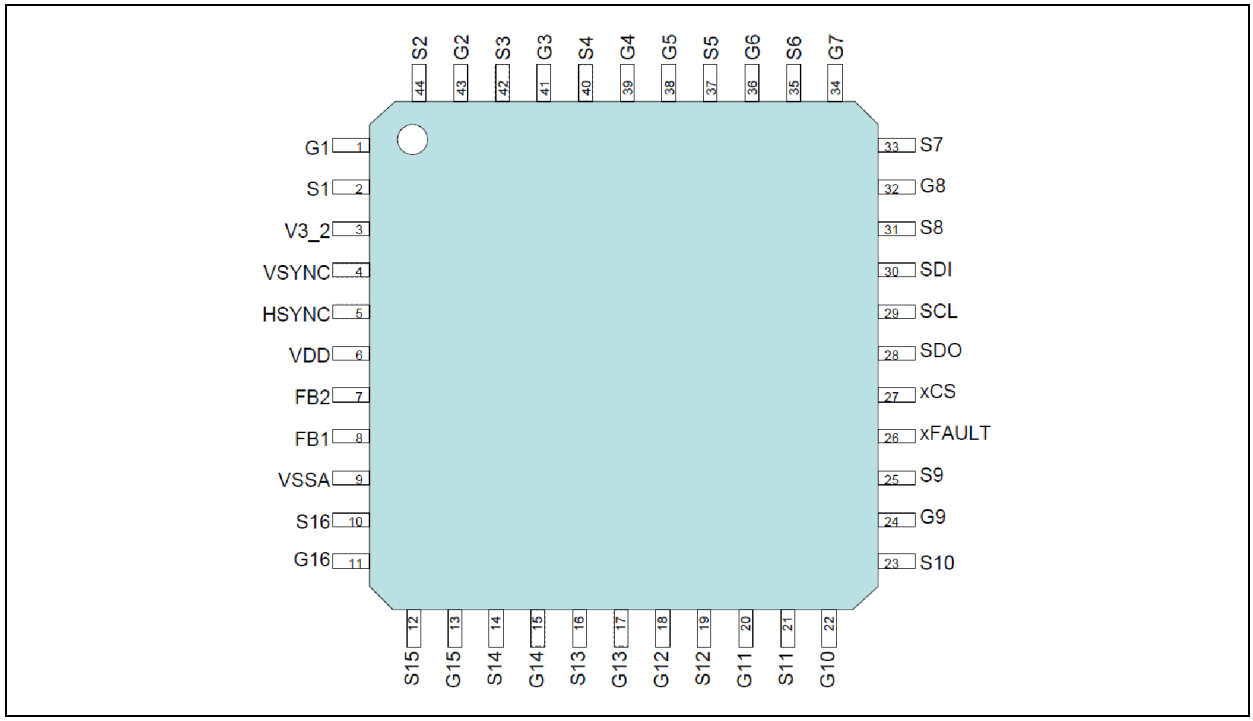
48-Pin QFN

Figure 3:
QFN-48 Pin Assignments (Top View)



44-Pin LQFP

Figure 4:
LQFP-44 Pin Assignments (Top View)



Pin Descriptions

Figure 5:
Pin Descriptions

Pin Number		Pin Name	Pin Type	Description
QFN48	LQFP44			
1	1	G1	A_I/O	Connect to gate of external transistor
2	2	S1	A_I/O	Connect to source of external transistor
3	3	V3_2	P	Digital supply output. Connect 2.2µF capacitor to GND
4	4	VSYNC	DI_PD	Vertical sync frequency
5	5	HSYNC	DI_PD	Clock input for PWM generators
6	6	V_{DD}	P	Power supply. Connect 4.7µF bypass capacitor to GND
7	7	FB2	A_I/O	Power supply feedback output2
8	8	FB1	A_I/O	Power supply feedback output1
9	9	VSSA	P	GND
10		VSS_SENSE	P	GND
11	10	S16	A_I/O	Connect to source of external transistor
12	11	G16	A_I/O	Connect to gate of external transistor
13	12	S15	A_I/O	Connect to source of external transistor
14	13	G15	A_I/O	Connect to gate of external transistor
15	14	S14	A_I/O	Connect to source of external transistor
16	15	G14	A I/O	Connect to gate of external transistor
17	16	S13	A I/O	Connect to source of external transistor
18	17	G13	A I/O	Connect to gate of external transistor
19	18	G12	A I/O	Connect to gate of external transistor
20	19	S12	A I/O	Connect to source of external transistor
21	20	G11	A I/O	Connect to gate of external transistor
22	21	S11	A I/O	Connect to source of external transistor
23	22	G10	A I/O	Connect to gate of external transistor
24	23	S10	A I/O	Connect to source of external transistor
25	24	G9	A I/O	Connect to gate of external transistor

Pin Number		Pin Name	Pin Type	Description
QFN48	LQFP44			
26	25	S9	A I/O	Connect to source of external transistor
27	26	xFAULT	DO_OD	Fault output. Open drain. Connect pullup to V3_2
28		DCDCEN	DO	GPIO output to enable DC-DC converter
29		MODE3D	DO	GPIO output to enable 3D mode
30	27	xCS	DI_PU	SPI interface chip select
31	28	SDO	DO	SPI interface data output. Tristate output
32		V3_2	P	Digital supply output.
33	29	SCL	DI_PD	SPI interface clock
34	30	SDI	DI_PD	SPI interface data input
35	31	S8	A I/O	Connect to source of external transistor
36	32	G8	A I/O	Connect to gate of external transistor
37	33	S7	A I/O	Connect to source of external transistor
38	34	G7	A I/O	Connect to gate of external transistor
39	35	S6	A I/O	Connect to source of external transistor
40	36	G6	A I/O	Connect to gate of external transistor
41	37	S5	A I/O	Connect to source of external transistor
42	38	G5	A I/O	Connect to gate of external transistor
43	39	G4	A I/O	Connect to gate of external transistor
44	40	S4	A I/O	Connect to source of external transistor
45	41	G3	A I/O	Connect to gate of external transistor
46	42	S3	A I/O	Connect to source of external transistor

Pin Number		Pin Name	Pin Type	Description
QFN48	LQFP44			
47	43	G2	A I/O	Connect to gate of external transistor
48	44	S2	A I/O	Connect to source of external transistor
EP		VSSA	P	Exposed PAD. Connect to VSSP

Note(s):

1. If an output channel X is not used, short Gx and Sx

The abbreviations used in Figure 5 are explained below:

A_I/O: Analog Input/Output

P: Power

DO: Digital Output

DO_OD: Digital Output Open Drain

DI: Digital Input

DI_PU: Digital Input with Pull-Up Resistor

DI_PD: Digital input with Pull-Down Resistor

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	
Electrical Parameters					
V_{DDMAX}	Supply voltage	-0.3	7	V	Applicable for pin V_{DD}
Vanamax	Maximum voltage analog pins	-0.3	7	V	see note (1)
Vdigmax	Maximum voltage digital pins	-0.3	5	V	see note (2)
I_{latch}	Latch-up immunity	-100	+100	mA	Norm: JEDEC 78
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge	±2000		V	Norm: MIL 883 E Method 3015 Human body model
Temperature Ranges and Storage Conditions					
T_{Jmax}	Junction temperature		150	°C	
T_{STRG}	Storage temperature range	-55	150	°C	
T_{BODY}	Package body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
RH_{NC}	Relative humidity non-condensing	5	85	%	
MSL	Moisture sensitivity level	3			Represents a maximum floor life time of 168h

Note(s):

1. Pins: FB1,FB2,G1-G16, S1-S16,VSYNC, HSYNC
2. Pins: V3_2, SDI, SDO, SCL, xCS, MODE3D, DCDCEN, xFAULT

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Operating Conditions

Figure 7:
General Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Rthca	Thermal resistance case – ambient	See Thermal Characteristics QFN48				°C/W
T_J	Junction temperature		-20		115	°C

Figure 8:
Power Supply

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		4.5		5.5	V
V3_2	Voltage regulator output	I_{LOAD} = 20mA	3.0	3.2	3.4	V
$V_{3\_2\_POR}$	Power-on reset level	Circuit stays in power down until V3_2 reaches $V_{3\_2\_POR}$	1.6		2.2	V
V_{DD_UVL}	Under voltage lockout level	Current outputs are turned OFF if V_{DD} is lower than V_{DD_UVL}. This is done by resetting the CURRx bits.	2.4		2.9	V
IDD_q	Quiescent current	V_{DD} = 5V, Default setting, PWM = 0		12		mA
IDD_r	Supply current	V_{DD} = 5V, HSYNC = 1MHz, VSYNC = 480Hz, Duty = 50%, VDAC=250mV		13		mA

Figure 9:
Current Outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{led\_500\_250}$	Trimmed current accuracy at 25°C	Trimmed during production. ILED = 100mA DACref = 500mV, VDAC = 250mV T_J = 25°C (excluding error of external Rset)	-0.5		+0.5	%
I_{ch_250}	Channel to channel accuracy at 25°C	ILED=100mA, DACref = 500mV, VDAC = 250mV, T_J = 25°C (excluding error of external Rset)	-0.2		+0.2	%
$I_{led\_500\_ALL}$	Current accuracy over VDAC	DACref = 500mV, VDAC = 200mV - 500mV T_J = 25°C (excluding error of external Rset)	-1.5		+1.5	%
$I_{led\_500\_TMP}$	Current accuracy over VDAC and Temp	DACref = 500mV, VDAC = 200mV – 500mV T_J = -20°C to 115°C (excluding error of external Rset)	-2		+2	%
$I_{led\_800\_250}$	Trimmed current accuracy at 25°C	Trimmed during production. ILED = 100mA, DACref = 800mV, VDAC = 250mV, T_J = 25°C (excluding error of external Rset)	-0.5		+0.5	%
$I_{led\_800\_ALL}$	Current accuracy over VDAC	DACref = 800mV, VDAC = 200mV - 800mV T_J = 25°C (excluding error of external Rset)	-1.5		+1.5	%
$I_{led\_800\_TMP}$	Current accuracy over VDAC and Temp	DACref = 800mV, VDAC = 200mV - 800mV T_J = -20°C to 115°C (excluding error of external Rset)	-2		+2	%
IGX	Output current pin Gx		3		4	mA
RGX	Output resistor pin Gx			1.0	1.3	kΩ
Vgx	Output voltage pin Gx	Igx = 0mA			V_{DD}	V

Figure 10:
Feedback Circuit, Fault Detectors

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IFBmax	Feedback current maximum	V_{FB_X} > 0.25V		255		µA
FB_IDAC_LSB	FB_IDAC LSB			1		µA
Tovtemp	Overtemperature limit		130	140	150	°C
Thyst	Overtemperature hysteresis			10		°C
$T_{shortmin}$	Minimum time to detect short		300			µs

Figure 11:
PWM Generators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Internal Clock for PWM		400	500	600	kHz
f_{HSYNC}	HSYNC frequency		100		2000	kHz
f_{VSYNC}	VSYNC frequency		60		480	Hz

Figure 12:
Digital Pins

Symbol	Parameter	Min	Typ	Max	Units	Note
V_{IH}	High level input voltage	1.3		V3_2 + 0.3	V	
V_{IL}	Low level input voltage	-0.3		0.8	V	
V_{OH}	High level output voltage	V3_2 - 0.3			V	I = 2mA
V_{OL}	Low level output voltage			0.3	V	I = 2mA
V_{OL_PD}	Low level output voltage open drain outputs			0.3	V	I = 2mA
R_pu	Input resistance pullup inputs		300		kΩ	
R_pd	Input resistance pulldown inputs		300		kΩ	

Timing Characteristics

Figure 13:
SPI Timings

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{SCLK}	SCLK frequency	0		10	MHz	
t1	xCS setup time	50			ns	
t2	xCS hold time	100			ns	
t3	xCS disable time	100			ns	
t4	SDI setup time	5			ns	
t5	SDI hold time	5			ns	
t6	SCLK rise time	5			ns	
t7	SCLK fall time	5			ns	
t8	SCLK low time	40			ns	
t9	SCLK high time	40			ns	
t10	Output valid from SCLK low	10			ns	
t11	SCLK falling to xCS rising edge	50			ns	

Timing Diagrams

Figure 14:
SPI Input Timing

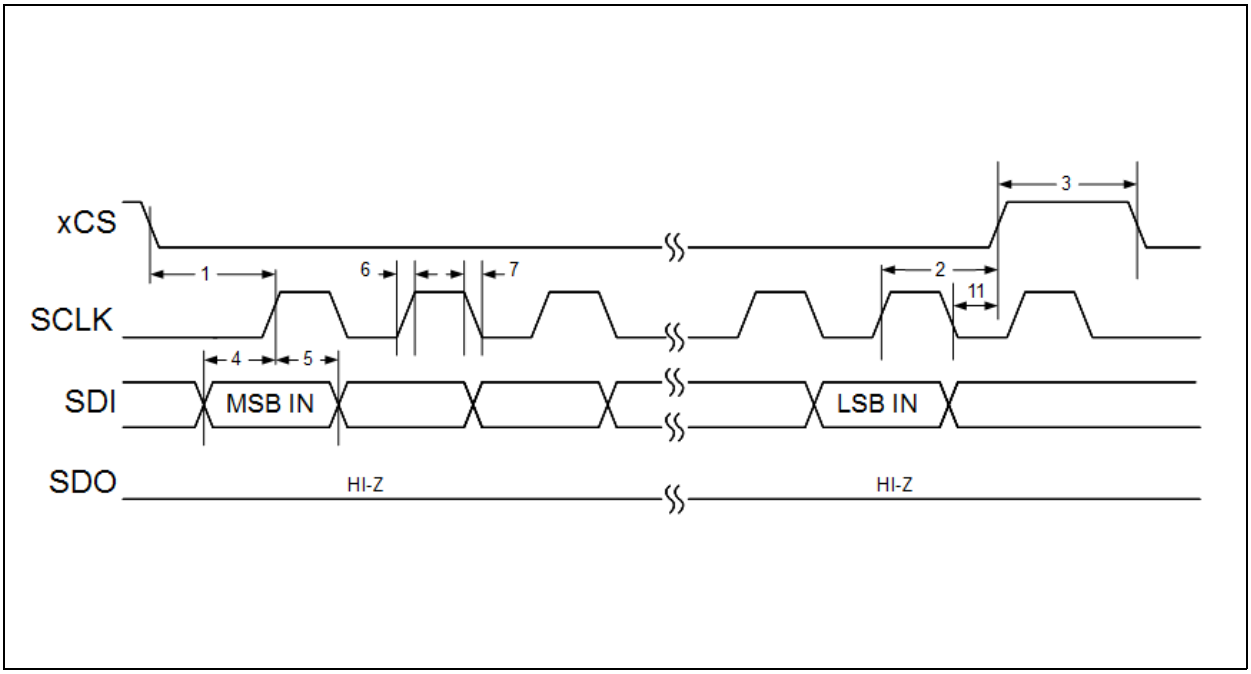
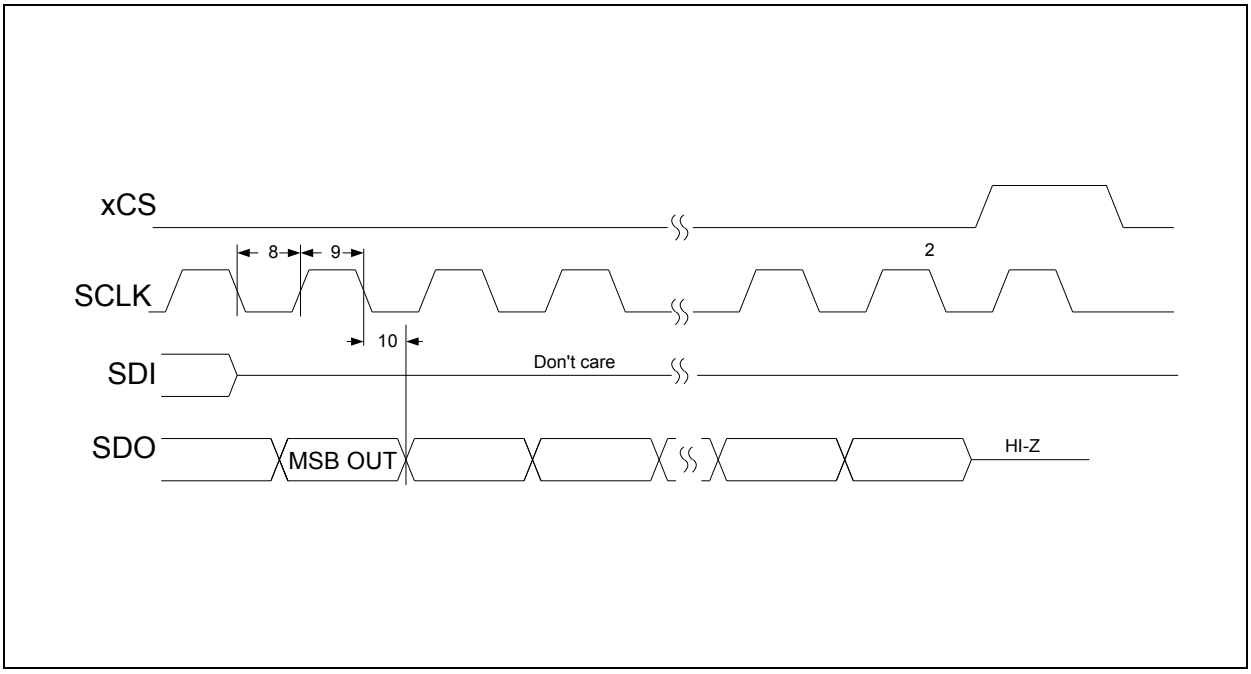
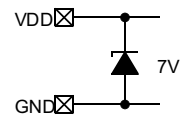
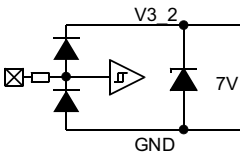
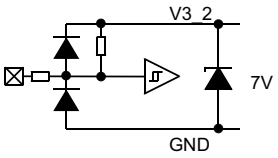
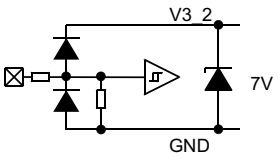
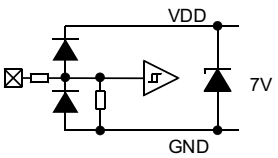
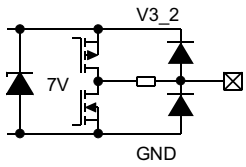
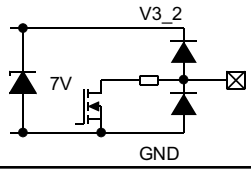
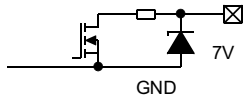
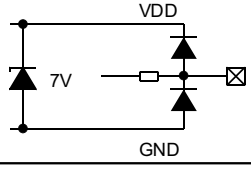


Figure 15:
SPI Output Timing



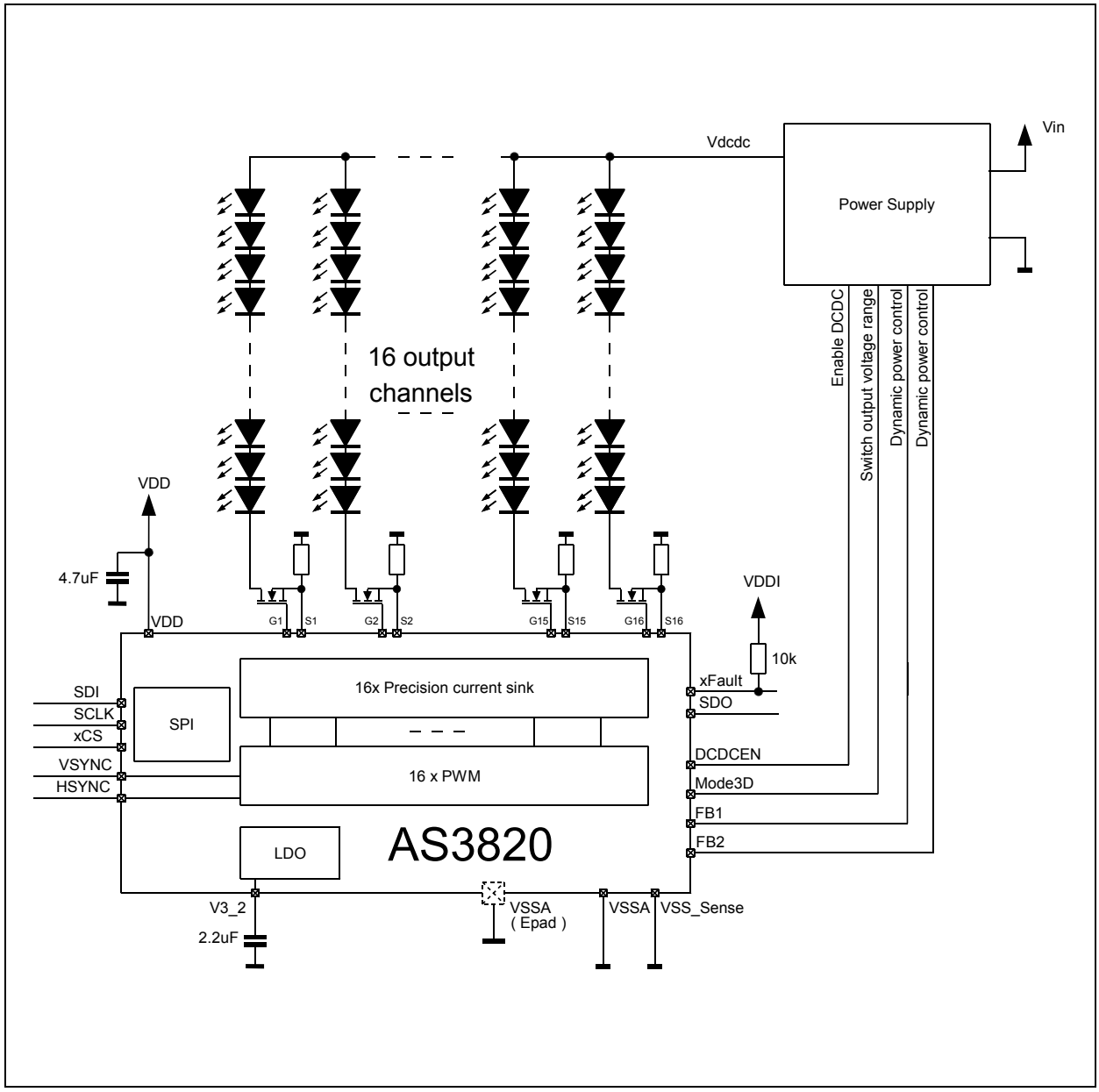
Pin Equivalent Circuits

Figure 16:
Pin Equivalent Circuits

VDD	
Digital Input	
Digital Input with PullUp	
Digital Input with PullDown	
Digital Inputs HSYNC, VSYNC	
Digital Output PushPull	
Digital Output Open Drain	
Feedback output	
Analog I/O	

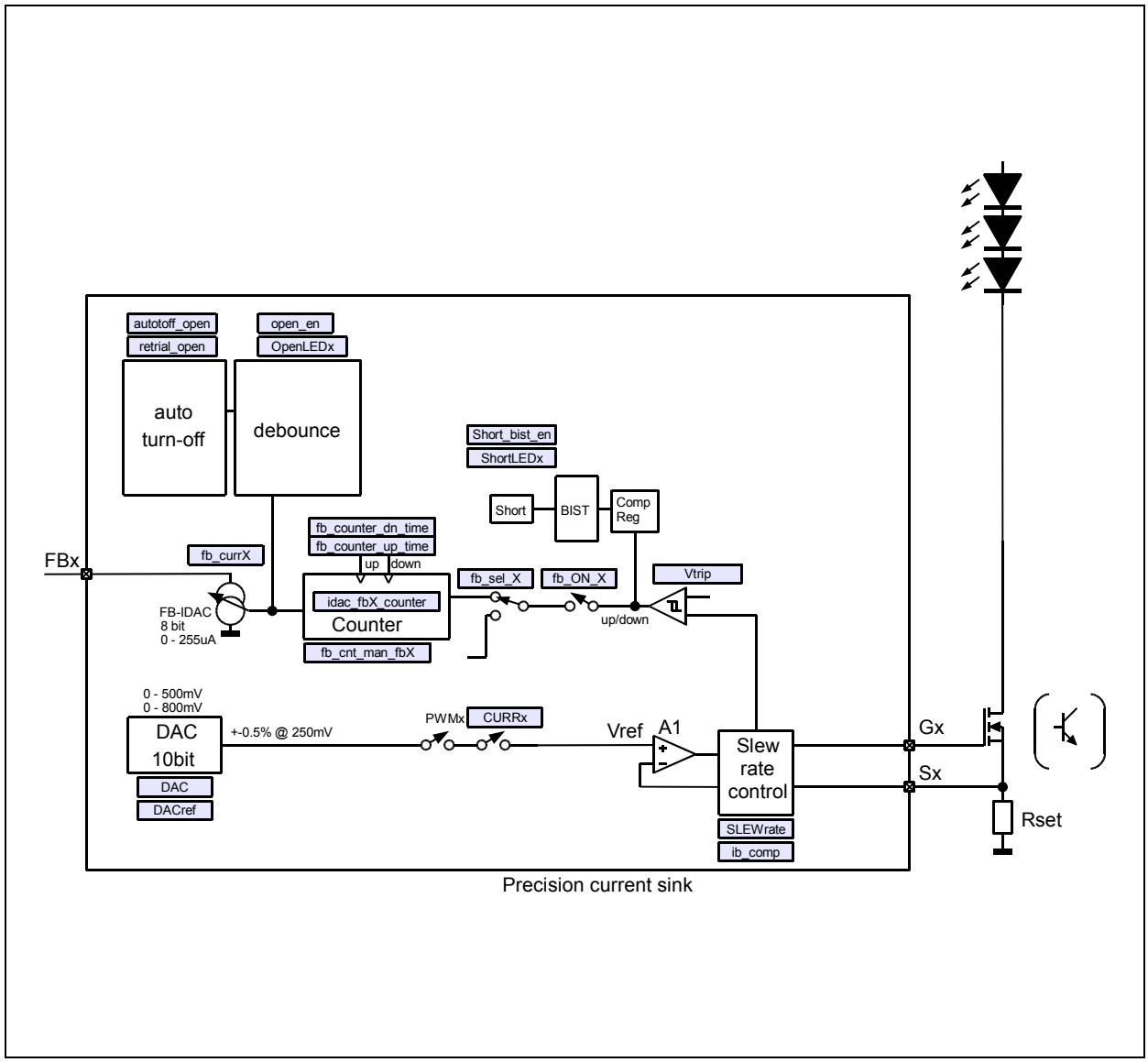
Detailed Description

Figure 17:
Typical Application Circuit



Current Outputs

Figure 18:
Precision Current Sink



Precision Current Sink

All current sinks are built with an internal error amplifier A1 and an external power transistor. The external transistor can either be a NMOS or a NPN bipolar transistor. For low EMI radiation the slew rate of the amplifier output voltage can be adjusted.

Power Supply Feedback

The gate driving voltage for the external transistor is monitored to adjust the power supply output. If this voltage gets to high a comparator enables counting up of the "*idac_fbX_counter*" with 256µs clock speed. This increases the output current of the FB-IDAC and so the output voltage of the external power supply can be increased via pin FB1 or pin FB2. The feedback function of each output can be assigned to either FB1 or FB2. The power supply feedback can be turned OFF for every current channel separately.

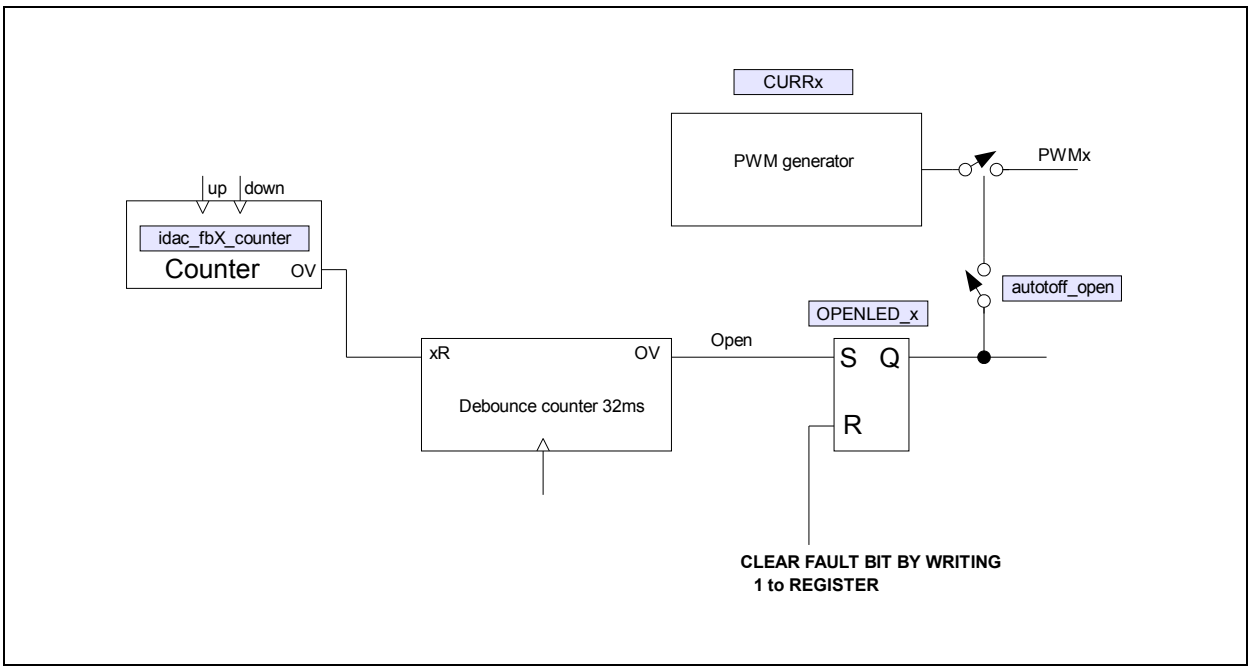
Manual Control of External Power Supply

The counter value "*idac_fbX_counter*" can also be preset by software if "*fbcounter_man_fx*" =1. This enables software control of the external power supply output voltage.

Open LED Detection

If open led detection is enabled a broken LED-string is detected during PWM=1. If a LED-string is broken and the feedback function is enabled, the *"idac_fbx_counter"* will count up in order to increase the power supply output voltage. After the *"idac_fbx_counter"* has reached its maximum value, a debounce counter is started. In order to run the debounce counter, the corresponding PWM-signal has to be high for more than 150µs. After the debounce couter has counted up for 32ms, the corresponding "*OPENLED_x*" bit is set and the output xFAULT = "0".

Figure 19:
Open LED Detection

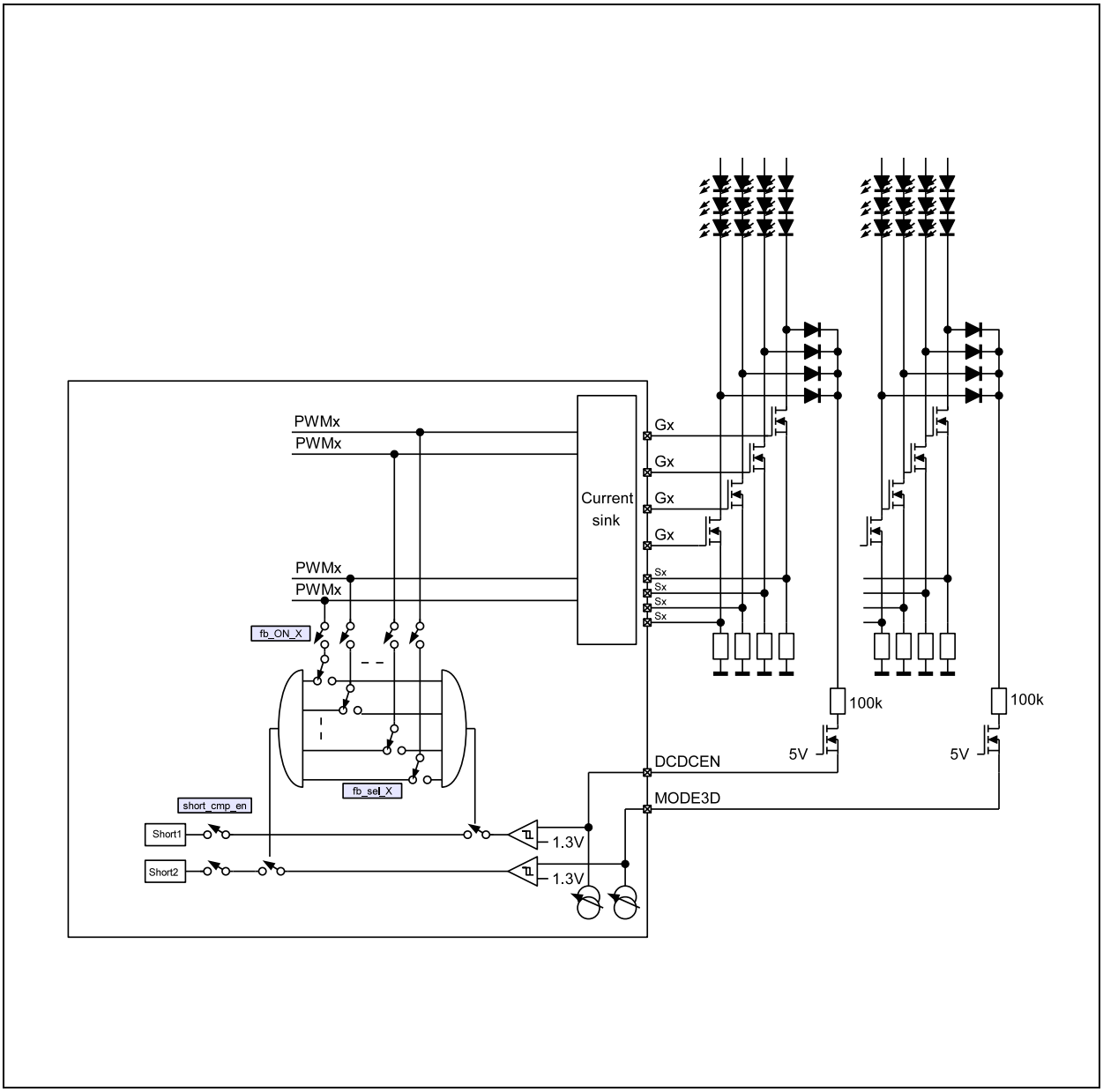


Short LED Detection

Short LED detection is implemented in two different ways:

1. With a built-in self-test (Short-BIST) circuit.
2. With two comparator inputs for monitoring external voltages (Short-COMP).

Figure 20:
Short-COMP Block Diagram

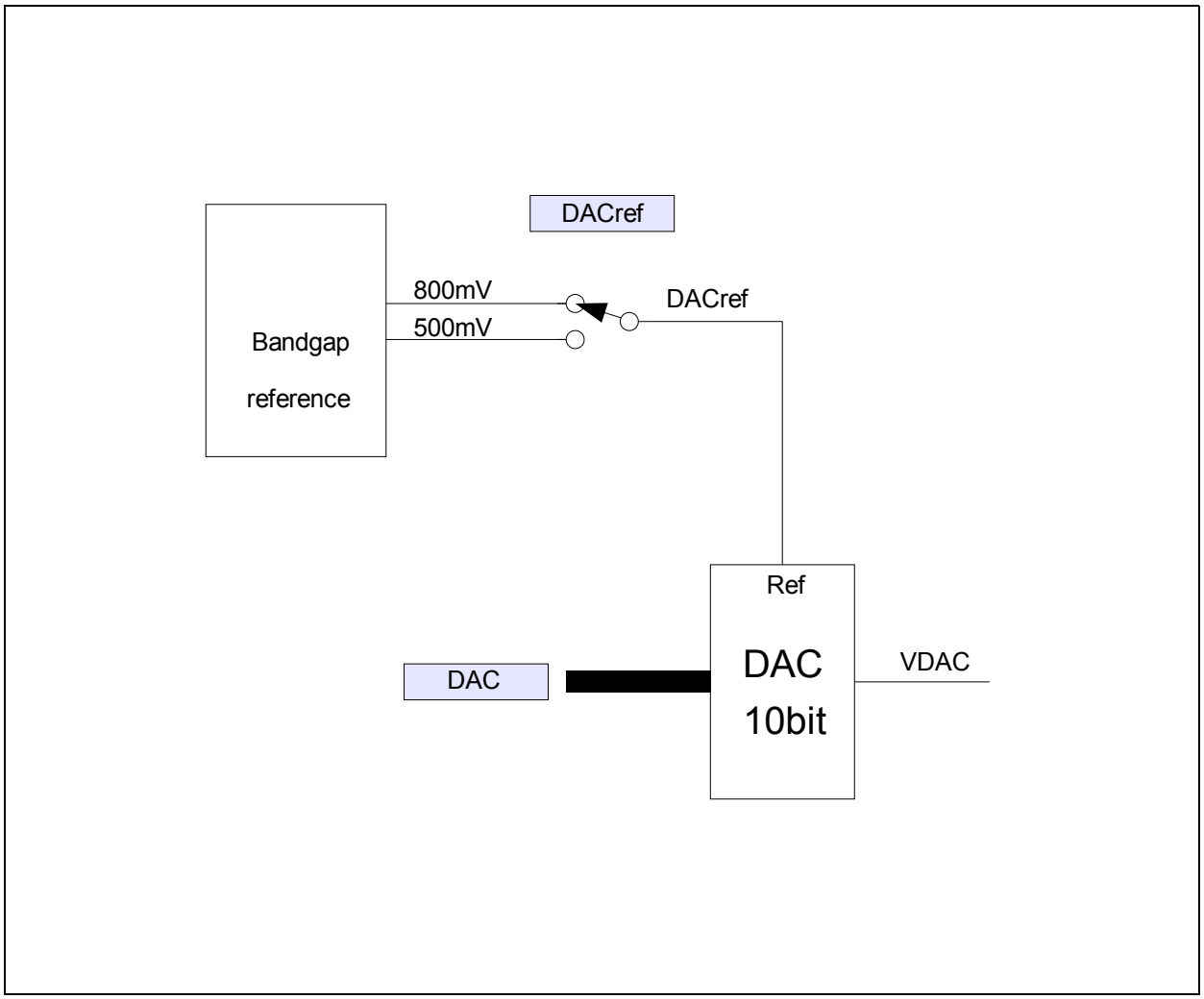


The external voltage is divided by an external resistor and an internal current source. The output of the comparators only takes effect if all selected PWM-signals are "1" for a minimum time of "*Tshortmin*" at the same time. The selection of Short1 or Short2 Group is done by "*fb_ON_x*" and "*fb_sel_X*".

DAC

The reference voltage for the output stage is generated by an internal 10-bit DAC. The DAC reference can be selected between 500mV and 800mV depending on register settings. The DAC is trimmed during production with
DACref = 800mV/VDAC = 250mV and
DAQref = 500mV/ VDAC = 250mV to guarantee an output current accuracy of ±0.5% on every current output.

Figure 21:
DAC and DAC Reference Generation



The DAC output voltage can be calculated with:

(EQ1) $$VDAC = \frac{DACref}{1024} \times DAC$$

DAC...10-bit data value

DACref...DAC reference voltage 500mV or 800mV

Registers in Current Output Stage

ACCESS: R...read, W...write, AS...async set, AC...async clear, WC...write clear

Figure 22:
CUR_ON_1

RegAddr: 0x01		CUR_ON_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CURR1 - CURR8	00000000	RW_AC	Enables or disables current outputs. 0: Output OFF 1: Output ON

Figure 23:
CUR_ON_2

RegAddr: 0x02		CUR_ON_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CURR9 – CURR16	00000000	RW_AC	Enables or disables current outputs. 0: Output OFF 1: Output ON

Figure 24:
Fault_1

RegAddr: 0x03		Fault_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Autotoff_uv	1	RW	1...Undervoltage lockout: If $V_{DD} < V_{DD\_UVL}$ channels are turned OFF by resetting CURRx-bits.
6	Short_bist_en	0	RW_AC	1...Starts built-in self-test (BIST) for short detection. Bit is cleared after BIST has finished.
5:4	Short_cmp_en	00	RW	Short detection with comparators: Not available in LQFP44 00...OFF 01...Enables short comp 1 10...Enables short comp 2 11...Enables short comp 1 and comp 2
3	Retrial_open	0	RW	1... Retrial open detection after autotoff_open was triggered
2	Autotoff_ot	1	RW	Automatic output turn OFF at overtemperature 0... Do not turn OFF current outputs on overtemperature 1... Turn OFF current outputs on overtemperature
1	Open_en	0	RW	1... Enable open LED detection for all channels
0	Autotoff_open	0	RW	Automatic feedback turn OFF on open LED detection 0... Do not turn OFF feedback on open LED detection 1... Turn OFF feedback on open LED detection

Figure 25:
GPIO_CTRL

RegAddr: 0x04		GPIO_CTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	xFAULT_config	0	RW	Output configuration pin xFAULT: 00...Open Drain 01...Push/Pull 10...Hi-Z, input only 11...No effect
5:4	Mode3D_config	0	RW	Output configuration pin Mode3D: Not available in LQFP44 00...Open Drain 01...Push/Pull 10...Hi-Z, input only, SHORT COMP 2 INPUT enabled 11...No effect
3	Mode3D	0	RW	0...Pin Mode3D = 0 Not Available in LQFP44 1...Pin Mode3D = 1
2:1	DCDCEN_config	0	RW	Output configuration pin DCDCEN: Not available in LQFP44 00...Open Drain 01...Push/Pull 10...Hi-Z, input only, SHORT COMP 1 INPUT enabled 11...No effect
0	DCDCEN	0	RW	0...Pin DCDCEN = 0 not available in LQFP44 1...Pin DCDCEN = 1

Figure 26:
FB_SEL1

RegAddr: 0x05		FB_SEL1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Fb_sel_1 – Fb_sel_8	00000000	RW	Select FB-channel for current outputs 1 to 8 0...Select FB channel FB1 and short-comparator group 1 1...Select FB channel FB2 and short-comparator group 2

Figure 27:
FB_SEL2

RegAddr: 0x06		FB_SEL2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Fb_sel_9 – Fb_sel_16	00000000	RW	Select FB-channel for current outputs 9 to 16 0...Select FB channel FB1 and short-comparator group 1 1...Select FB channel FB2 and short-comparator group 2

Figure 28:
CURR_CTRL

RegAddr: 0x07		CURR_CTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Sel_ac	00	RW	Do not change
5	Fb_ac_off	0	RW	0...AC feedback enabled 1...AC feedback disabled (external BJT) If Ib_comp=1, FB_ac_off = 1 must be set
4	Ib_comp	0	RW	0...Bias current compensation OFF 1...Bias current compensation ON (external BJT) If Ib_comp=1, FB_ac_off = 1 must be set
3	DACref_buffer	0	RW	0...DAC output is buffered 1...DAC output is unbuffered
2	DACref	0	RW	0...DACref = 500mV 1...DACref = 800mV
1:0	Slew_rate	00	RW	Select slew rate of output drivers. (Slew rate of VREF) 00...250mV/16µs 01...250mV/8µs 10...250mV/4µs 11...250mV/2µs

Figure 29:
SHORTLED_1

RegAddr: 0x08		SHORTLED_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SHORTLED_1 – SHORTLED_8	00000000	R/WC	Indicates short LED found with BIST on outputs 1 to 8 0...No short LED detected 1... Short LED detected

Figure 30:
SHORTLED_2

RegAddr: 0x09		SHORTLED_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	SHORTLED_9 – SHORTLED_16	00000000	R/WC	Indicates short LED found with BIST on outputs 9 to 16 0...No short LED detected 1... Short LED detected

Figure 31:
OPENLED_1

RegAddr: 0x0A		OPENLED_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	OPENLED_1 – OPENLED_8	00000000	AS/WC	Indicates open LED condition on outputs 1 to 8 0...No open LED detected 1... Open LED detected

Figure 32:
OPENLED_2

RegAddr: 0x0B		OPENLED_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	OPENLED_9 – OPENLED_16	00000000	AS/WC	Indicates open LED condition on outputs 9 to 16 0...No open LED detected 1... Open LED detected

Figure 33:
FB_ON_1

RegAddr: 0x0E		FB_ON_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FB_CURR_1 – FB_CURR _8	00000000	RW	Enables or disables feedback function of output channels 0...No feedback function on CURRx 1... Function on CURRx

Figure 34:
FB_ON_2

RegAddr: 0x0F		FB_ON_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	FB_CURR_9 – FB_CURR _16	00000000	RW	Enables or disables feedback function of output channels 0...No feedback function on CURRx 1... Function on CURRx

Figure 35:
VDAC_H / VDAC_L

RegAddr: 0x0C	RegAddr: 0x0D	VDAC_H / VDAC_L		
Bit	**Bit**	**Default**	**Access**	**Bit Description**
7:0	1:0	0x80, 0x00	RW	DAC input [9:0]

Figure 36:
IDAC_FB1_COUNTER

RegAddr: 0x10		IDAC_FB1_COUNTER		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	IDAC_FB1_COUNTER	00000000	RW	Feedback 1 counter value. Can be overwritten if Fb_cnt_man_fb1 = 1 0x00... FB-current 0µA 0xFF... FB-current 255µA

Figure 37:
IDAC_FB2_COUNTER

RegAddr: 0x11		IDAC_FB2_COUNTER		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	IDAC_FB2_COUNTER	00000000	RW	Feedback 2 counter value. Can be overwritten if Fb_cnt_man_fb2 = 1 0x00... FB-current 0µA 0xFF... FB-current 255µA

Figure 38:
FBLOOP_CTRL

RegAddr: 0x12		FBLOOP_CTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Vtrip	00	RW	Select gate trip voltage for feedback 00...5*(VDD/6) 01... 4*(VDD/6) 10... 3*(VDD/6) 11... 2*(VDD/6)
5	Fb_cnt_man_fb2	0	RW	0...FB2 counter runs automatically in feedback loop 1...FB2 counter is set manual
4	Fb_cnt_man_fb1	0	RW	0...FB1 counter runs automatically in feedback loop 1...FB1 counter is set manual
3:2	Fbcount_dn_time	01	RW	FB1 and FB2 counter down counting clock cycle. (1) 00...512µs 01...2048µs 10...4096µs 11...8192µs
1:0	Fbcount_up_time	01	RW	FB1 and FB2 counter up counting clock cycle 00...1024µs 01... 256µs 10... 64µs 11... 16µs

Note(s):

1. Down counting starts after 200ms delay time

Figure 39:
STATUS

RegAddr: 0x60		STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	STAT novsync	0	R	1...Indicates missing Vsync signal for longer than 100ms
6	STAT OT	0	R	1...Indicates Overtemperature fault happened
5	STAT Open	0	R	1...Indicates open detection fault happened
4	Short_bist	0	R	1...Indicates a short bist interrupt
3	Vcnt underflow	0	AS_WC	1...VSYNC signal to fast
2	Short2	0	AS_WC	1...Indicates short on channel group 2
1	Short1	0	AS_WC	1...Indicates short on channel group 1
0	Power_good	0	R	1...Power good. Indicates that VDD is greater than VDD_UVL

Figure 40:
SHORT_BIST_CTRL1

RegAddr: 0x63		SHORT_BIST_CTRL1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5		000	R	Do not change
4	BIST_retrial	0	RW	0...No BIST retrial 1...Short BIST retrial after 1 second
3	BIST_steptime	0	RW	BIST counter step down time 0...64µs/step 1...128µs/step
2	Autotoff_BIST	0	RW	1...Shorted channels found by BIST are turned OFF
1:0	BIST_wait	0	RW	Wait after max step down value of counter is reached. 00...No wait 01...Wait 1 VSYNC pulse 10...Wait 2 VSYNC pulses 11...Wait 3 VSYNC pulses see note (1)

Note(s):

1. This option is necessary for phase shifted PWM. To ensure each channel is tested.

Figure 41:
SHORT_BIST_MAXSTEP

RegAddr: 0x64		SHORT_BIST_MAXSTEP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	BISTmaxstep	11111111	RW	Maximum down-counts of IDAC counter during BIST

Figure 42:
SHORT_BIST_CTRL2

RegAddr: 0x65		SHORT_BIST_CTRL2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6		00	R	Do not change
5	COMP_retrial	0	RW	0...No COMP retrial 1...Short COMP retrial after 1 second
4	Autotoff_COMP	0	RW	1...Shorted channels found by COMP are turned OFF
3:0	COMP_LEVEL	1010	RW	Short detection voltage based on external 100k resistor 0000...2V 0001...3V 0010...4V 0011...5V 0100...6V 0101...7V 0110...8V 0111...9V 1000...10V 1001...11V 1010...12V 1011...13V 1100...13V 1101...13V 1110...13V 1111...13V

Figure 43:
COMPREG_1

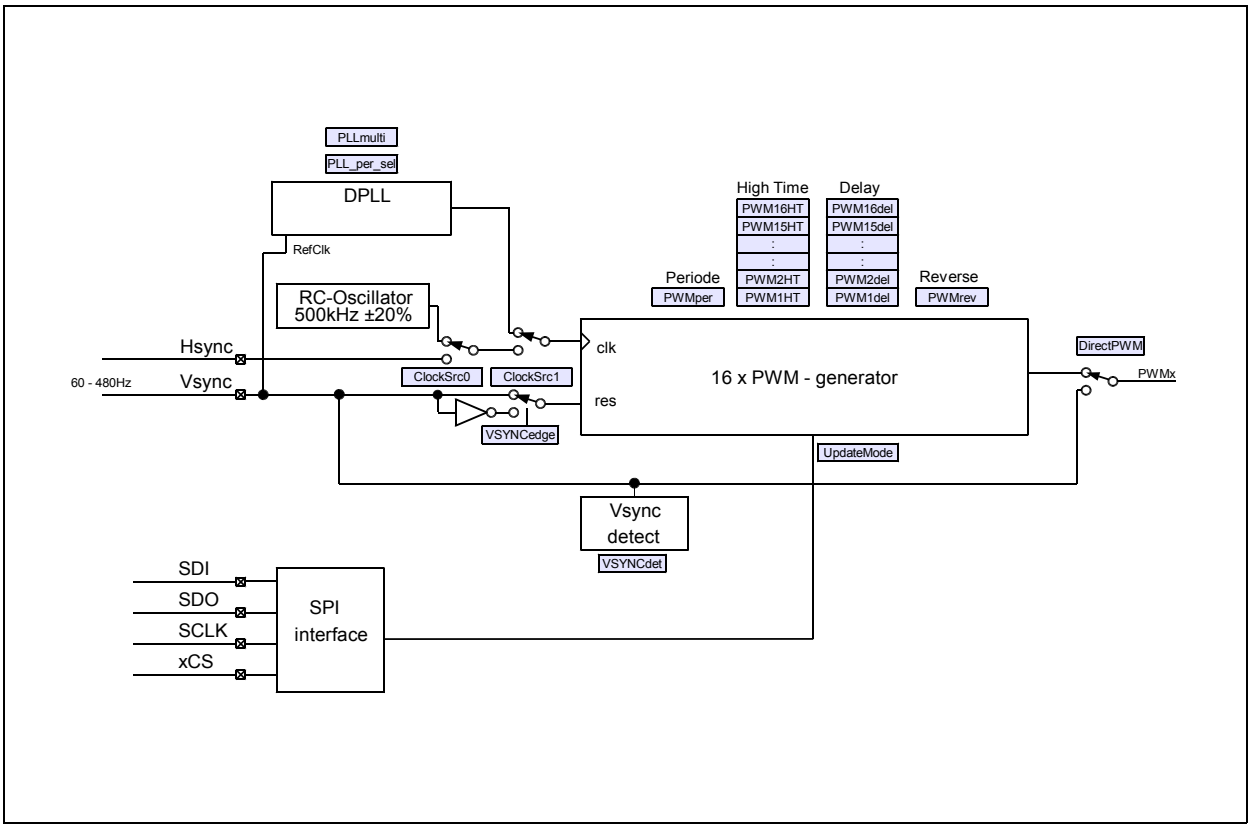
RegAddr: 0x6C		COMPREG_1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CompReg1 – CompReg8	00000000	AS/AR	Status of trip comparator

Figure 44:
COMPREG_2

RegAddr: 0x6D		COMPREG_2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CompReg9 – CompReg16	00000000	AS/AR	Status of trip comparator

PWM Generators

Figure 45:
PWM Generators



Clock and Reset

The clock for the built-in PWM generators can be one of three different sources listed below:

1. Internal RC oscillator with 500KHz
2. External clock signal. This is usually the HSYNC signal of the TV.
3. Digital PLL (DPLL) clock derived from Vsync

Digital PLL

A DPLL can be used to generate a PWM input clock with a frequency that is a multiple of the VSYNC frequency. The frequency multiplication factor can be controlled to be either “PWMperiod” or “PLLmulti” by control bit “PLL_per_sel”.

By default “PLL_per_sel”=0 to control the frequency by “PWMperiod” which also defines the period for the PWM generators.

If necessary, control bit “PLL_per_sel” can be set to control the frequency multiplication by register “PLLmulti” with 16-bit resolution and independently of PWMperiod.

PLL_per_sel = 0 (Default):

(EQ2) $$f_{DPLLout} = f_{VSYNC} \cdot PWMperiod$$

PLL_per_sel = 1:

(EQ3) $$f_{DPLLout} = f_{VSYNC} \cdot PLLmulti$$

The VSYNC frequency is determined by measuring the VSYNC period with an internal clock. Since the internal clock and the external VSYNC signal are asynchronous, the result of the measurement will jitter by one internal clock cycle. Therefore the generated DPLL-frequency jitters by one clock cycle.

In order to prevent starting of a new PWM-period at the end of the current PWM-period due to this jitter it is recommended to use the following setting:

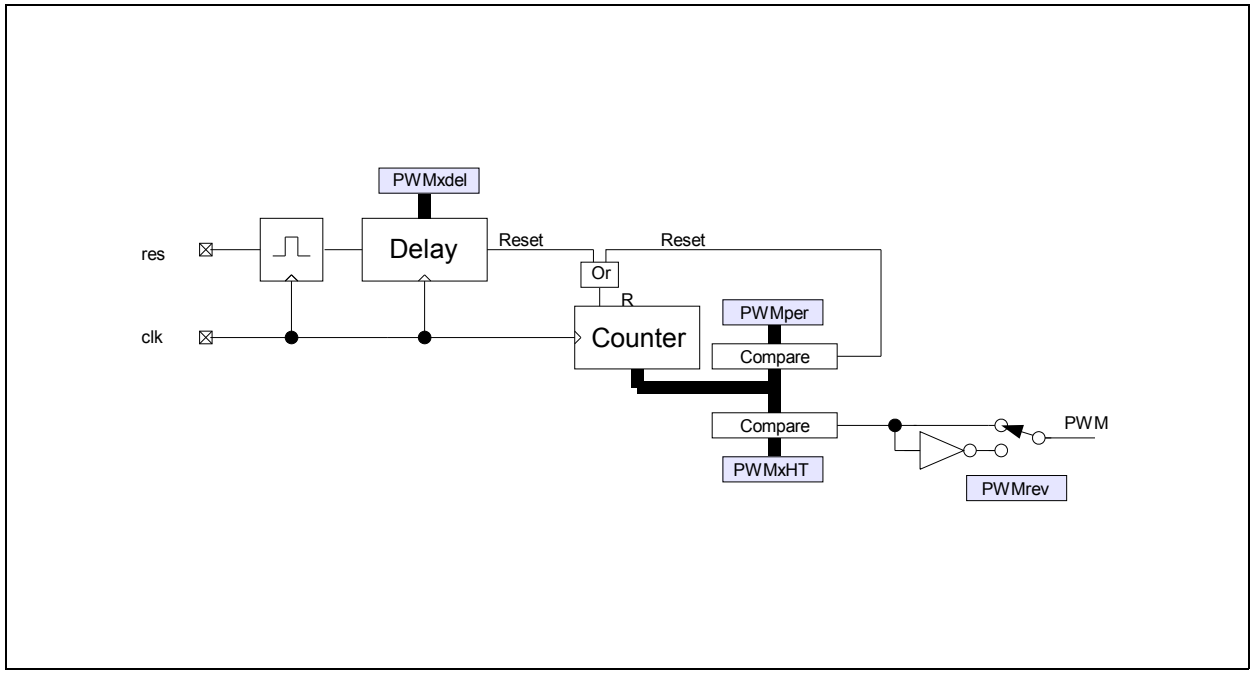
- Set PLL_per_sel = 1
- Set PLLmulti = PWMperiod - 1

By either changing the input frequency at VSYNC or by changing the divider setting the DPLL will need up to 4 VSYNC cycles to settle to the new value.

If f_{VSYNC} > 8MHz/PLLmulti, the bit V_{CNT} is set and a fault is indicated.

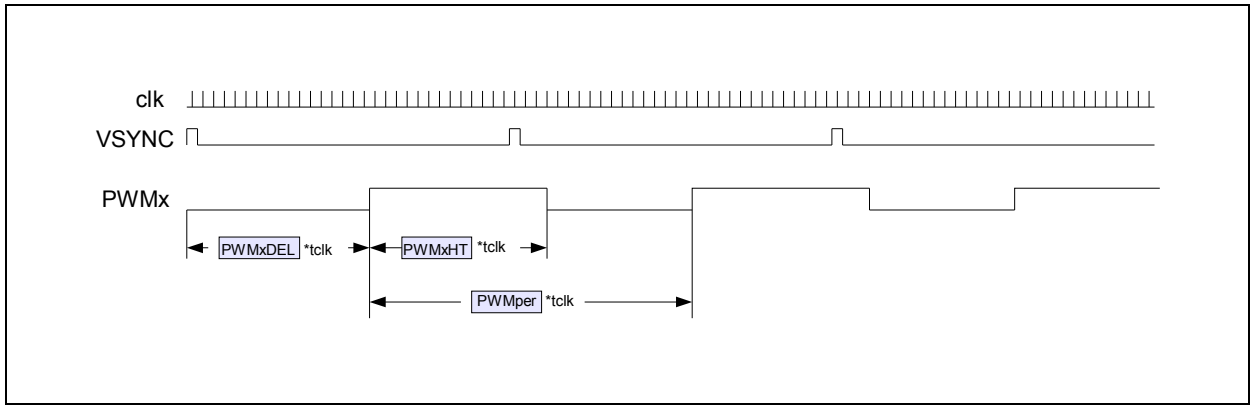
PWM Counter

Figure 46:
PWM Counter



Each PWM-generator is build with a 13bit counter and digital comparators. The counter is counting up with t_{clk} until the value stored in "PWMper" is reached. This resets the counter and starts the next period. While the counter value is below "PWMxHT" the PWM-signal is "1", the rest of the period the PWM-signal is "0". The output of each PWM-generator can also be inverted by means of the "PWMrev".

Figure 47:
PWMx, VSYNC and CLK Timing Diagram



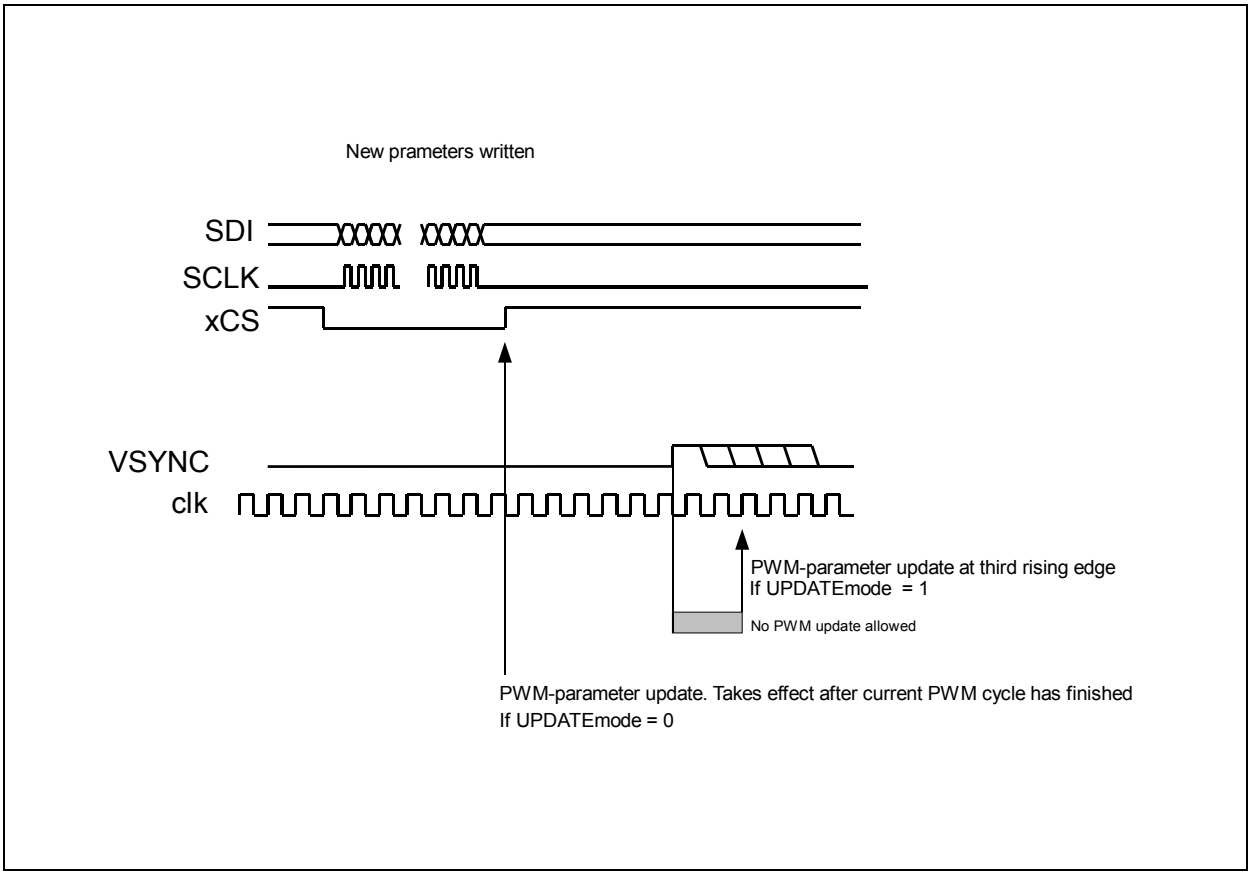
SPI Data Update, UPDATEmode Bit

The PWM-settings that are programmed via the SPI-Interface take effect depending on the status of the “UPDATEmode”-bit.

If UPDATEmode = 1 new data from the serial interface are stored at the next rising edge of VSYNC

If UPDATEmode = 0 new data from the serial interface are stored immediately after xCS goes high and will take effect after current PWM cycle is finished. In this mode the values in the PWMxdel registers are ignored. There will be no Delay on the PWM signals.

Figure 48:
UPDATEmode



The PWMxHT-values are double buffered. HighTime values for the next VSYNC can be written even when the current HighTime is not finished.

Within the first two HSYNC pulses after rising VSYNC no SPI data transfer is allowed.

Direct PWM Mode

The internal signals PWMx can also be direct applied at the VSYNC input if the bit Direct_PWM =1.

In this mode the default driver has the following configuration:

- All current outputs are ON
- All feedback controls are enabled and connected to FB1
- Open LED detection is enabled
- Open LED detection auto turn OFF function is enabled
- Open LED detection retrial function is enabled
- Short LED detection (Short-COMP) is enabled
- Short LED detection auto turn OFF function is enabled
- Undervoltage lockout and overtemperature detection are enabled

In this mode the device starts with default settings and can still be programmed via SPI.

VSYNC Detect

If the bit "VSYNCdet" is set (Register "PWM_CTRL") the VSYNC detector monitors the presence of a VSYNC signal.

If the VSYNC signal is missing for more than 100ms the following changes are done:

- In Register "STATUS" the bit "STAT novsync" ist set.
- Output xFAULT is acitivated (LOW)
- Current outputs are turned OFF. All register settings remain while the outputs are turned OFF.

If the VSYNC signal is applied again the following changes are done:

- In Register "STATUS" the bit "STAT novsync" ist reset.
- Output xFAULT is deactivated
- Current outputs are turned ON.

VSYNC Duration

Since the VSYNC input is connected to an edge detector, there is no restriction on the duration of the VSYNC pulse.

Registers in PWM Generators

Figure 49:
PWM_CTRL

RegAddr: 0x13		PWM_CTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	PLL_per_sel	0	RW	DPLL frequency generation 0...DPLL-period = Vsync*PWMperiod 1...DPLL-period = Vsync*PLLmulti
6	ClockSrc1	0	RW	Clock source for internal PWM-generators 0…Internal RC oscillator or HSYNC (depending on ClockSrc0) 1...PLL output
5	Pwm_rev	0	RW	0...Normal PWM operation 1...PWM signals are inverted
4	VSYNCdet	0	RW_AS	Enable VSYNC detection 0...VSYNC-detection OFF 1... VSYNC-detection ON. All current outputs are turned OFF if VSYNC signal is missing for 100ms
3	VSYNCedge	0	RW	Defines VSYNC trigger edge 0...VSYNC trigger on rising edge 1...VSYNC trigger on falling edge
2	Direct_PWM	0	RW_AS	Select external or internal PWM signal 0...PWM signal is generated internally 1...PWM signal is applied externally at pin VSYNC Factory trim bit is read during startup. See section Direct PWM Mode
1	Update_Mode	0	RW	Defines when internal registers are updated 0...Registers updated with rising edge of xCS 1...Registers updated with next VSYNC-edge
0	ClockSrc0	0	RW	Clock source for internal PWM-generators 0…Internal RC oscillator 1...External Pin HSYNC see note (1)

Note(s):

1. This bit only takes effect when ClockSrc1 = 0

Figure 50:
PWMperiod

RegAddr: 0x15	RegAddr: 0x14	PWMperiod		
Bit	Bit	Default	Access	Bit Description
4:0	7:0	0x00, 0x00	RW	PWMper[12:0] sets PWM period

Figure 51:
PWM1delay

RegAddr: 0x17	RegAddr: 0x16	PWM1delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM1del[11:0] sets PWM1 delay

Figure 52:
PWM2delay

RegAddr: 0x19	RegAddr: 0x18	PWM2delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM2del[11:0] sets PWM2 delay

Figure 53:
PWM3delay

RegAddr: 0x1B	RegAddr: 0x1A	PWM3delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM3del[11:0] sets PWM3 delay

Figure 54:
PWM4delay

RegAddr: 0x1D	RegAddr: 0x1C	PWM4delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM4del[11:0] sets PWM4 delay

Figure 55:
PWM5delay

RegAddr: 0x1F	RegAddr: 0x1E	PWM5delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM5del[11:0] sets PWM5 delay

Figure 56:
PWM6delay

RegAddr: 0x21	RegAddr: 0x20	PWM6delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM6del[11:0] sets PWM6 delay

Figure 57:
PWM7delay

RegAddr: 0x23	RegAddr: 0x22	PWM7delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM7del[11:0] sets PWM7 delay

Figure 58:
PWM8delay

RegAddr: 0x25	RegAddr: 0x24	PWM8delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM8del[11:0] sets PWM8 delay

Figure 59:
PWM9delay

RegAddr: 0x27	RegAddr: 0x26	PWM9delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM9del[11:0] sets PWM9 delay

Figure 60:
PWM10delay

RegAddr: 0x29	RegAddr: 0x28	PWM10delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM10del[11:0] sets PWM10 delay

Figure 61:
PWM11delay

RegAddr: 0x2B	RegAddr: 0x2A	PWM11delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM11del[11:0] sets PWM11 delay

Figure 62:
PWM12delay

RegAddr: 0x2D	RegAddr: 0x2C	PWM12delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM12del[11:0] sets PWM12 delay

Figure 63:
PWM13delay

RegAddr: 0x2F	RegAddr: 0x2E	PWM13delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM13del[11:0] sets PWM13 delay

Figure 64:
PWM14delay

RegAddr: 0x31	RegAddr: 0x30	PWM14delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM14del[11:0] sets PWM14 delay

Figure 65:
PWM15delay

RegAddr: 0x33	RegAddr: 0x32	PWM15delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM15del[11:0] sets PWM15 delay

Figure 66:
PWM16delay

RegAddr: 0x35	RegAddr: 0x34	PWM16delay		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM16del[11:0] sets PWM16 delay

Figure 67:
LOCKUNLOCK

RegAddr: 0x36		LOCKUNLOCK		
Bit	Bit Name	Default	Access	Bit Description
7:0	LOCKUNLOCK	0x00	RW	MagicByte to lock and unlock writing and reading of registers Writing into register: 0xCX...Unlock register Group1. Writing enabled 0xXA...Unlock register Group2. Writing enabled 0xCA...Unlock register Group1 and Group2. Writing enabled 0xAX...Lock register Group1. Writing disabled 0xXC...Lock register Group2. Writing disabled 0xAC...Lock register Group1 and Group2. Writing disabled X...Don't care. All other values do not change the status of LOCKUNLOCK. Reading from register: 0x00....Group1 and Group2 are locked 0x01...Group1 is unlocked 0x02...Group2 is unlocked 0x03...Group1 and Group2 are unlocked

Figure 68:
PWM1hightime

RegAddr: 0x38	RegAddr: 0x37	PWM1hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM1HT[11:0] sets PWM1 high time

Figure 69:
PWM2hightime

RegAddr: 0x3A	RegAddr: 0x39	PWM2hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM2HT[11:0] sets PWM2 high time

Figure 70:
PWM3hightime

RegAddr: 0x3C	RegAddr: 0x3B	PWM3hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM3HT[11:0] sets PWM3 high time

Figure 71:
PWM4hightime

RegAddr: 0x3E	RegAddr: 0x3D	PWM4hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM4HT[11:0] sets PWM4 high time

Figure 72:
PWM5hightime

RegAddr: 0x40	RegAddr: 0x3F	PWM5hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM5HT[11:0] sets PWM5 high time

Figure 73:
PWM6hightime

RegAddr: 0x42	RegAddr: 0x41	PWM6hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM6HT[11:0] sets PWM6 high time

Figure 74:
PWM7hightime

RegAddr: 0x44	RegAddr: 0x43	PWM7hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM7HT[11:0] sets PWM7 high time

Figure 75:
PWM8hightime

RegAddr: 0x46	RegAddr: 0x45	PWM8hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM8HT[11:0] sets PWM8 high time

Figure 76:
PWM9hightime

RegAddr: 0x48	RegAddr: 0x47	PWM9hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM9HT[11:0] sets PWM9 high time

Figure 77:
PWM10hightime

RegAddr: 0x4A	RegAddr: 0x49	PWM10hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM10HT[11:0] sets PWM10 high time

Figure 78:
PWM11hightime

RegAddr: 0x4C	RegAddr: 0x4B	PWM11hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM11HT[11:0] sets PWM11 high time

Figure 79:
PWM12hightime

RegAddr: 0x4E	RegAddr: 0x4D	PWM12hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM12HT[11:0] sets PWM12 high time

Figure 80:
PWM13hightime

RegAddr: 0x50	RegAddr: 0x4F	PWM13hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM13HT[11:0] sets PWM13 high time

Figure 81:
PWM14hightime

RegAddr: 0x52	RegAddr: 0x51	PWM14hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM14HT[11:0] sets PWM14 high time

Figure 82:
PWM15hightime

RegAddr: 0x54	RegAddr: 0x53	PWM15hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM15HT[11:0] sets PWM15 high time

Figure 83:
PWM16hightime

RegAddr: 0x56	RegAddr: 0x55	PWM16hightime		
Bit	Bit	Default	Access	Bit Description
3:0	7:0	0x00, 0x00	RW	PWM16HT[11:0] sets PWM16 high time

Figure 84:
PWM Example 1

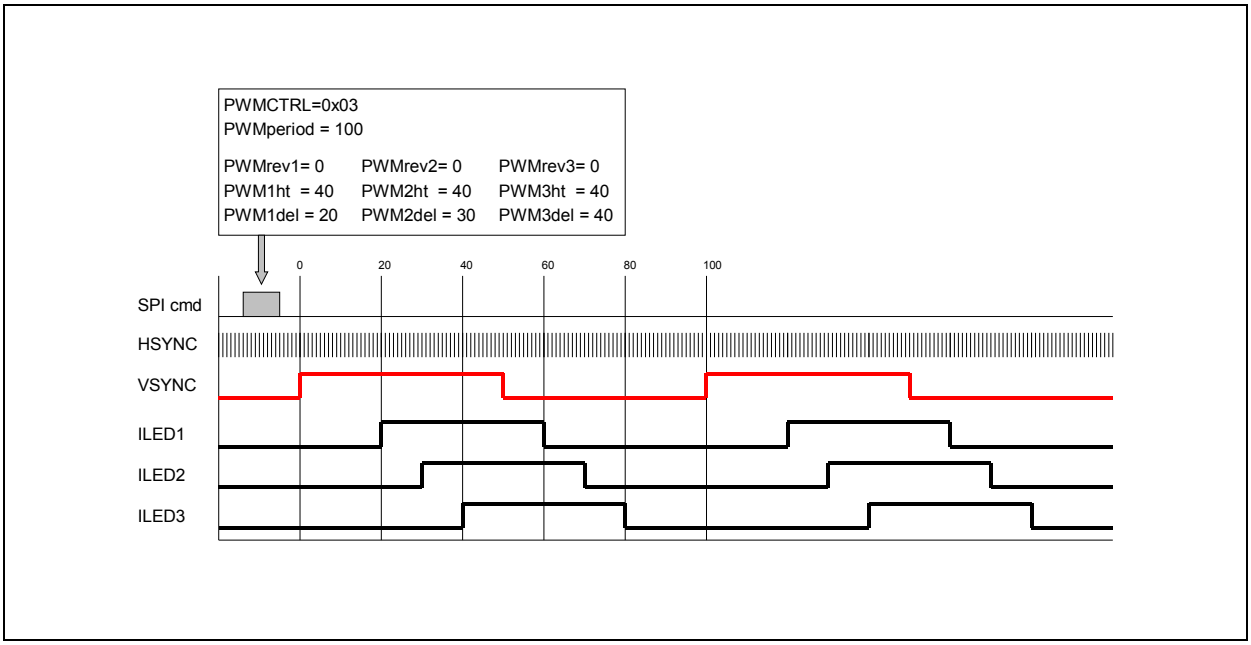


Figure 85:
PWM Example 2

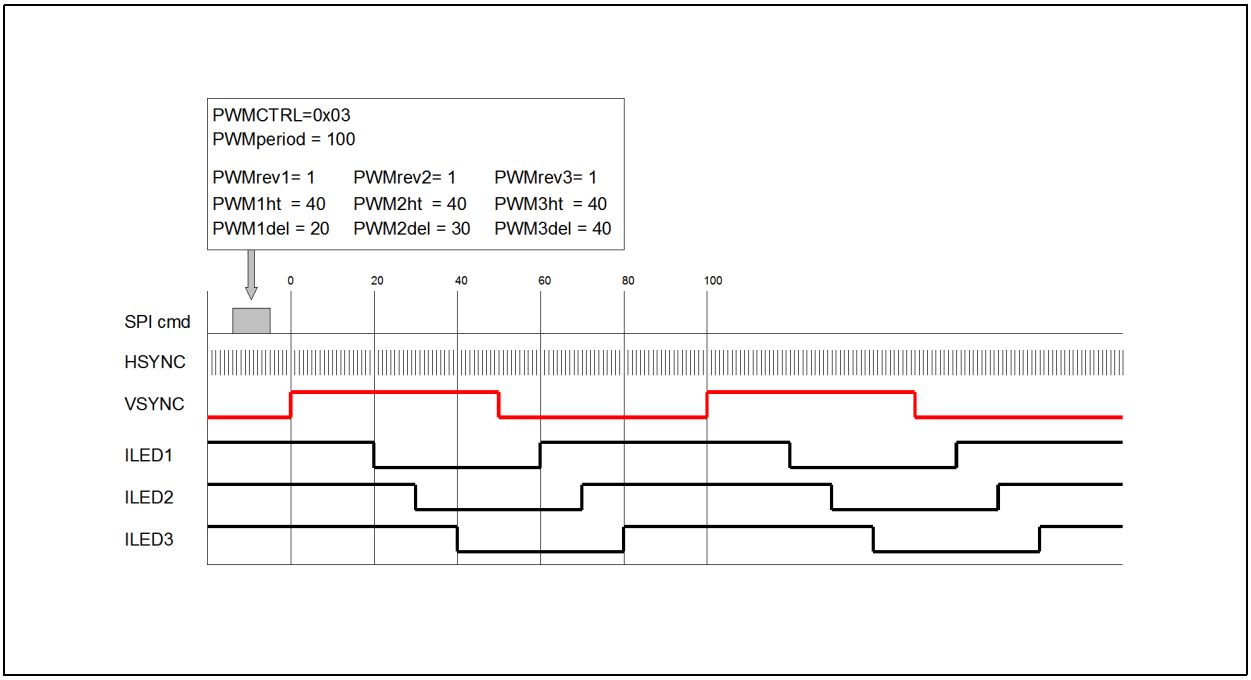


Figure 86:
PWM Example 3

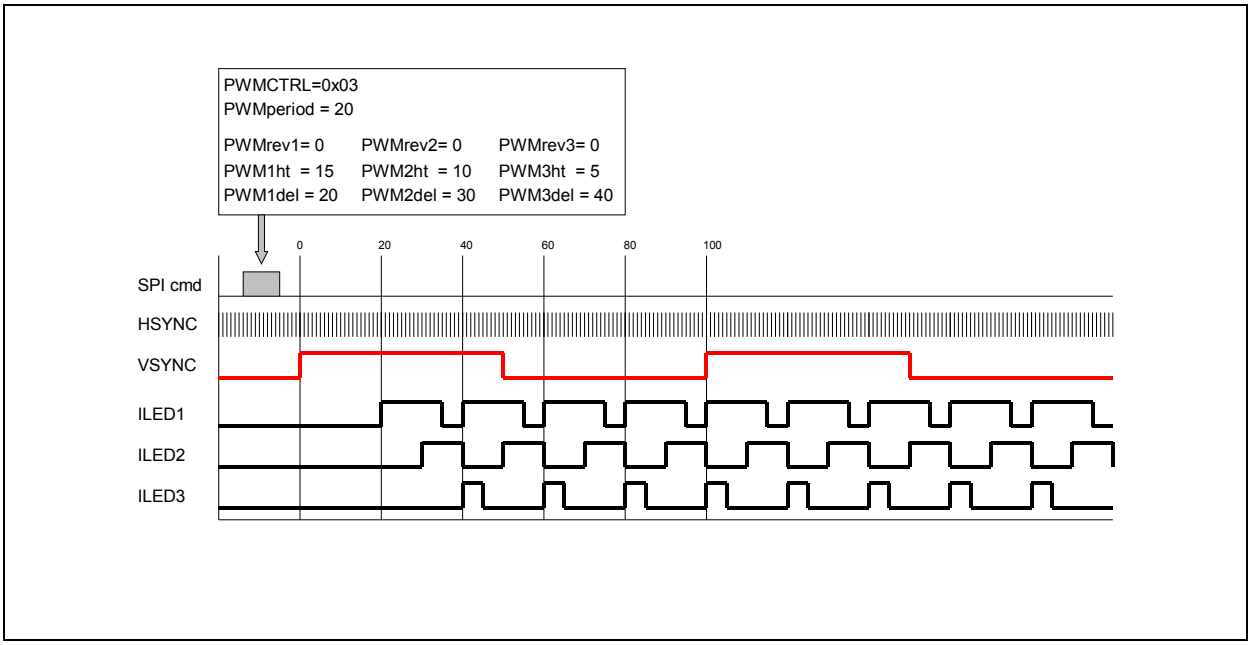
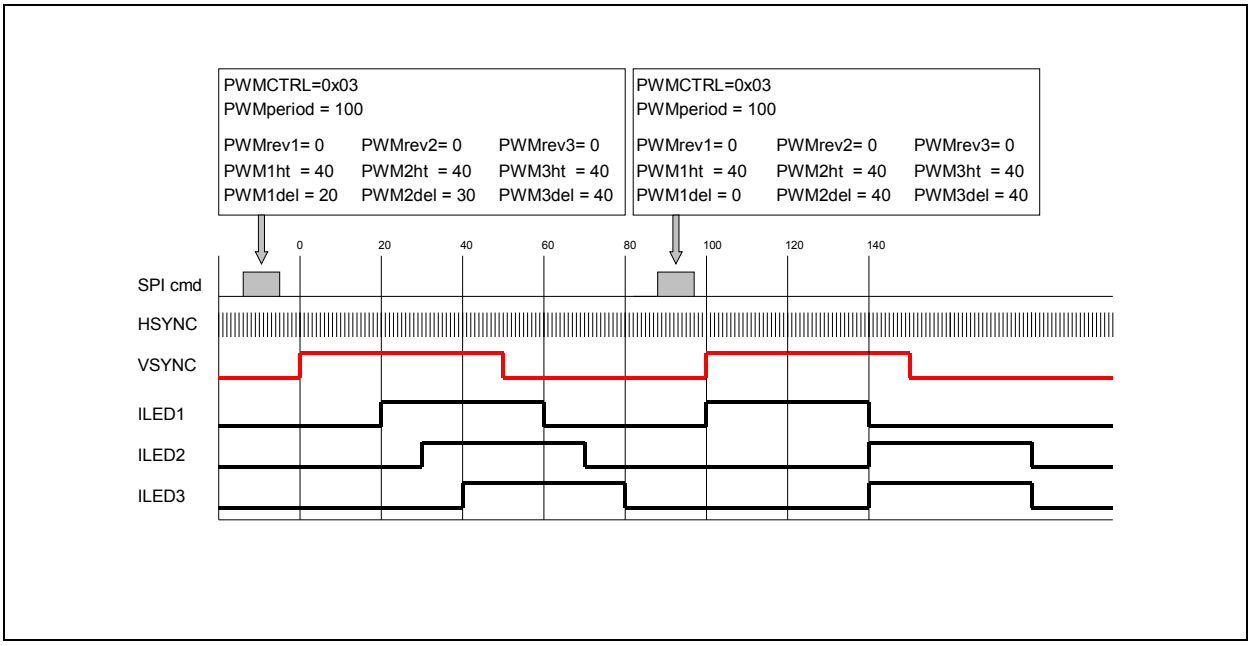


Figure 87:
PWM Example 4



Power Supply

Voltage Regulator V3_2

A build in linear voltage regulator provides 3.2V supply voltage for external devices at pin V3_2. A 2.2µF decoupling capacitor should be connected to pin V3_2.

Interface Power Supply V3_2

Pin V3_2 supplies all digital inputs/outputs.

Safety Features

Temperature Shutdown

If "autotoff_ot" = 1 the outputs of the device are turned OFF when the die temperature reaches 140°C. If the die temperature goes below 130°C the outputs are turned ON again.

Register Lock/Unlock

To prevent wrong writing to registers due to noise on the serial interface a lock/unlock mechanism is implemented.

Register 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x0E, 0x0F, 0x10, 0x11, 0x12, 0x13, 0x63, 0x64, 0x65 belong to Group1 and can only be written if Group1 is unlocked by the "LOCKUNLOCK"-byte (Reg: 0x36)

Register 0x0C, 0x0D, 0x14, 0x15, 0x61, 0x62 belong to Group2 and can only be written if Group2 is unlocked by the "LOCKUNLOCK"-byte (Reg: 0x36)

The default value of the Groups is locked.

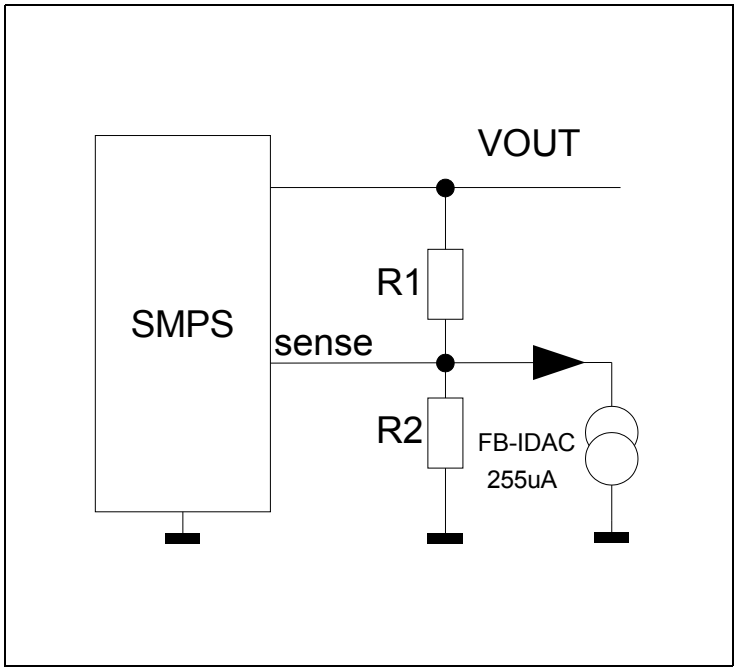
Dynamic Feedback Control

The output of pins "FB1" and "FB2" can be used to control any external power supply for best power efficiency.

Every power supply senses its output voltage with a resistive voltage divider. This voltage divider can be modified to set the output voltage between a minimum output voltage VMIN and a maximum output voltage VMAX. The design of the dynamic feedback control is done in 2 steps.

Step 1: Calculate resistors R1 in order to achieve the desired voltage range (VMAX – VMIN) with 255µA maximum current DAC output.

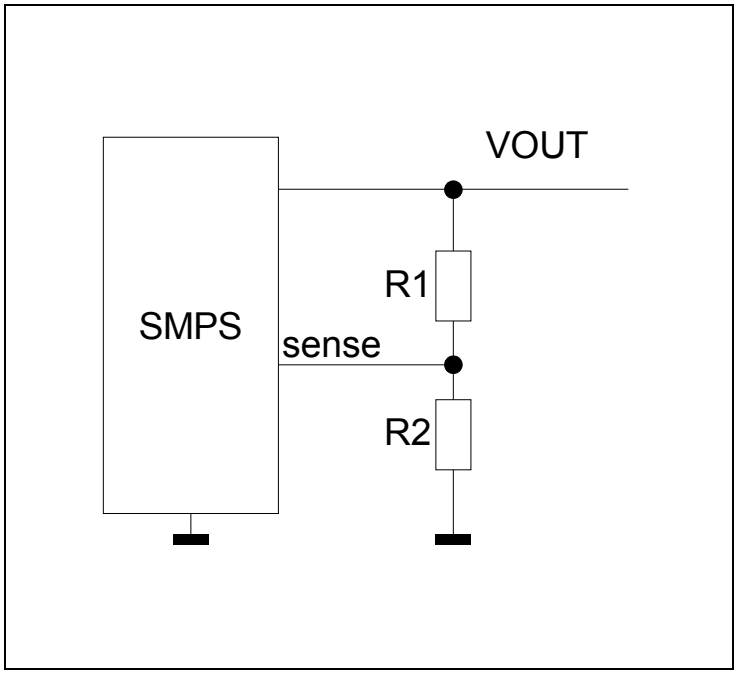
Figure 88:
Step 1



(EQ4) $$R1 = \frac{Vout_{MAX} - Vout_{MIN}}{255\mu A}$$

Step 2: Calculate resistor R2 for minimum output voltage with 0µA minimum current DAC output.

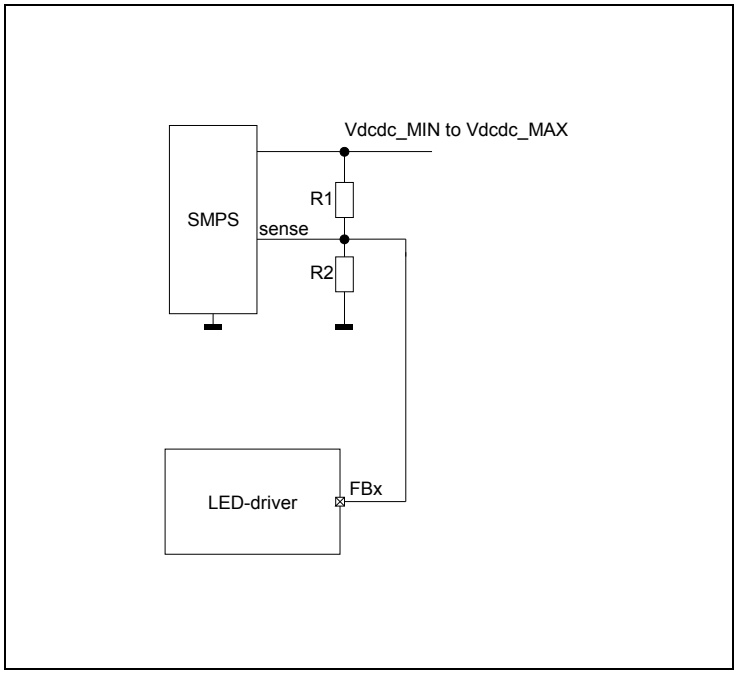
Figure 89:
Step 2



(EQ5) $$R2 = \frac{R1}{\left(\frac{Vout_{MIN}}{V_{sense}} - 1\right)}$$

The output voltage VOUT can also be adjusted manually by writing the "*idac_FBx_counter*" value ("FB_cnt_man_fbx"=1). In this case the output voltage can be calculated as follows:

Figure 90:
Step 3



(EQ6) $$VOUT = \left(1 + \frac{R1}{R2}\right) \times V_{sense} + R1 \times \text{"idac\_fbx\_counter"} \times 1\mu A$$

Example: Voutmin = 60V, Voutmax = 80V, Vsense = 1.25V

(EQ7) $$R1 = \frac{(Vout_{MAX} - Vout_{MIN})}{255\mu A} = \frac{(80V - 60V)}{255\mu A} = 78k\Omega$$

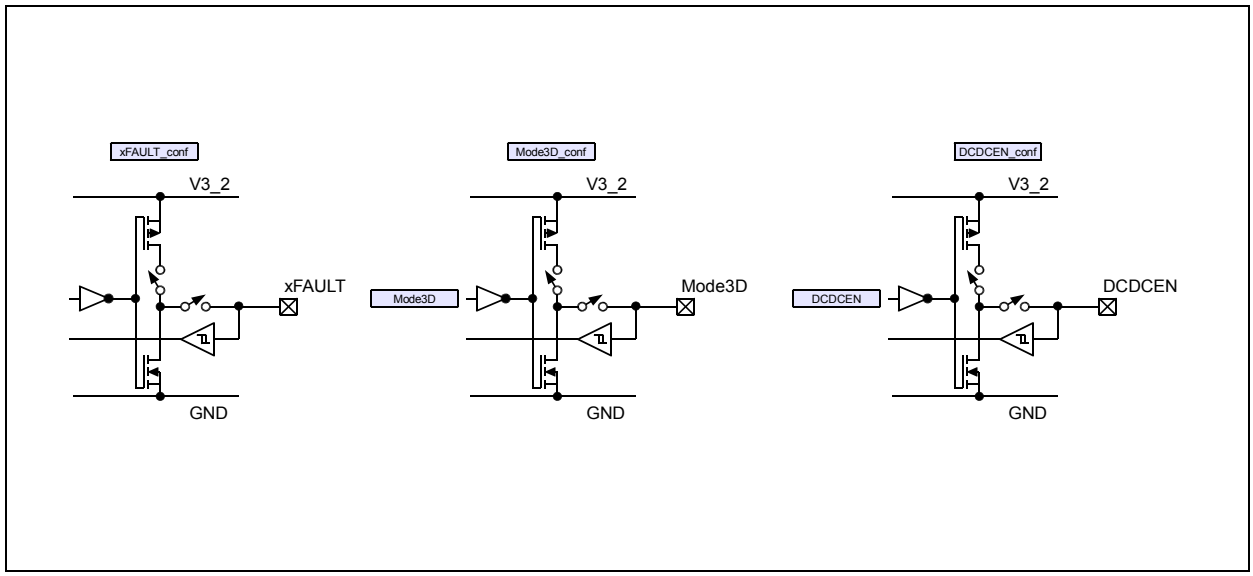
(EQ8) $$R2 = \frac{R1}{\left(\frac{Vout_{MIN}}{V_{sense}} - 1\right)} = \frac{78k\Omega}{\left(\frac{60V}{1.25V} - 1\right)} = 1.66k\Omega$$

GPIO

(NOT AVAILABLE IN LQFP44)

The two pins DCDCEN and Mode3D can be used to change the configuration of a DC-DC controller. These pins can also be used as general purpose input/output pins which can be configured as high impedance input, Push-Pull output or Open drain output. Also the output pin xFAULT can be configured.

Figure 91:
GPIO



Application Information

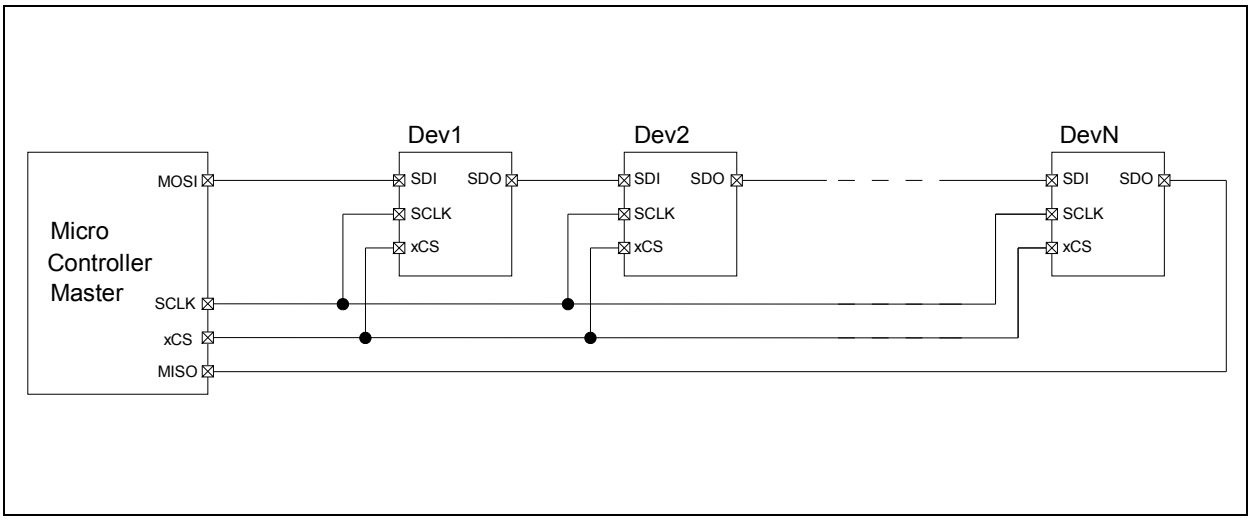
SPI Interface

For the data transfer a serial peripheral interface (SPI) is used. The SPI is configured to work only as SPI slave. If more than one driver is connected to a SPI master, they can be connected in a “Daisy Chain”-structure or a parallel structure.

SPI Daisy Chain Structure

All SPI slaves share the same clock (SCLK) and chip select (xCS) signal. In that configuration all devices can be treated as one big shift register. The devices are automatically enumerated as described in the next section.

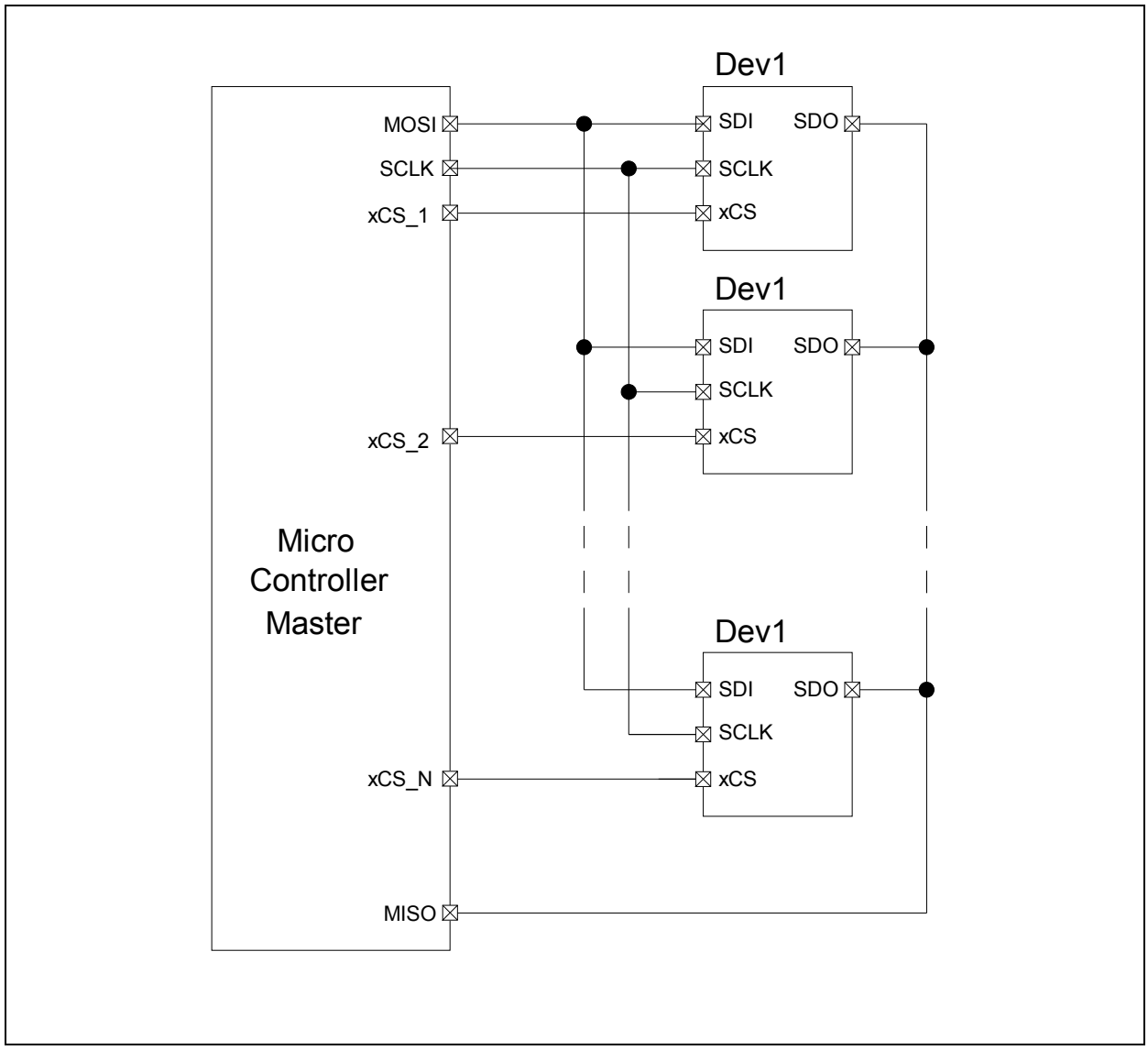
Figure 92:
SPI Daisy Chain Structure



SPI Parallel Structure

All SPI slaves share the same input (SDI) output (SDO) and clock (SCLK) signal. Every single device can be addressed via the chip select (xCS) signal. In this configuration every device has DevAddr = 0x01.

Figure 93:
SPI Parallel Structure



SPI Device Address Enumeration

The device address of each driver is automatically set by the position of the device in the chain.

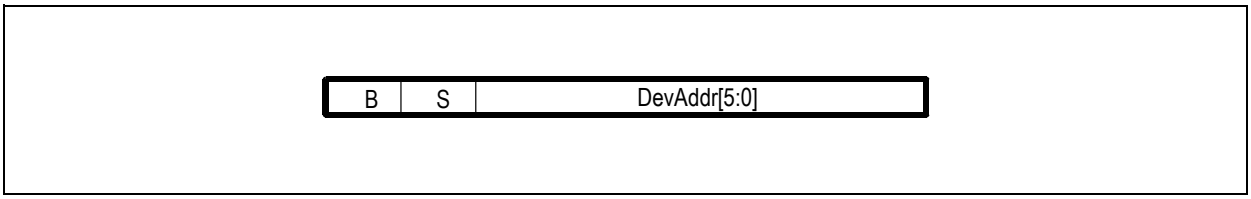
The first device has DevAddr = 0x01, the second device has DevAddr = 0x02 and so on. Device Addresses 0x00 and 0x3F are used for special broadcast writing commands described below.

SPI Protocol

Data Types

When xCS=0 all slaves will be activated. The addressing and data section is organized in byte packages. Each message can be built with the following Bytes:

Figure 94:
Device Address

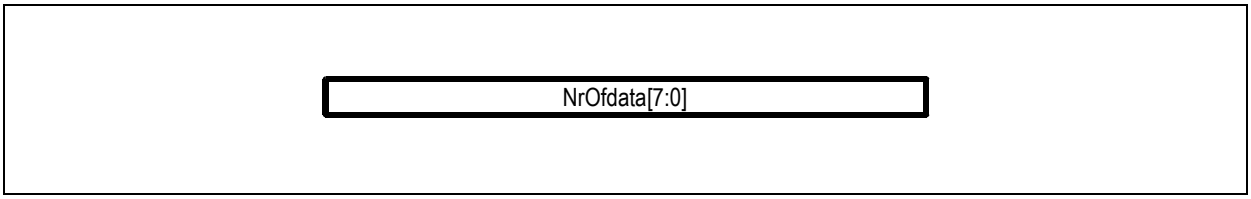


Addresses a specific driver and defines protocol information

Figure 95:
Device Address

Bit	Meaning	Value
B	Broadcast	B=1...Broadcast message to all devices B=0...Normal message to one single device
S	Singlebyte	S=0...Block data read or write S=1...Single data transmission (only one byte)
DevAddr[5:0]	Device Address	0x00 Write same data to same register of all devices (B=1) 0x01 to 0x3E. Device addresses for device 1 to 62 0x3F Write different data to same register of all devices (B=1)

Figure 96:
Nr_of_data

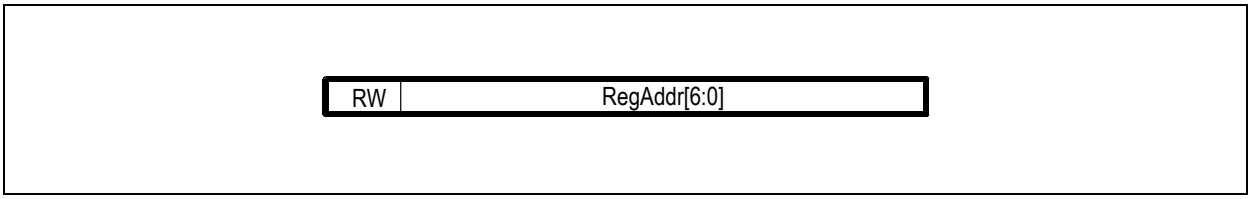


Defines the number of data bytes in the data frame if S=0

Figure 97:
Nr_of_data

Bit	Meaning	Value
NrOfdata[7:0]	Number of data bytes in frame	0x00 to 0xFF

Figure 98:
Register_address



Register address to be read or written

Figure 99:
Register Address to Be Read or Written

Bit	Meaning	Value
RW	Read/xWrite	RW = 0 write to reg address RW = 1 read from reg address
RegAddr[6:0]	Select register address	0x00 to 0x60

Figure 100:
Data

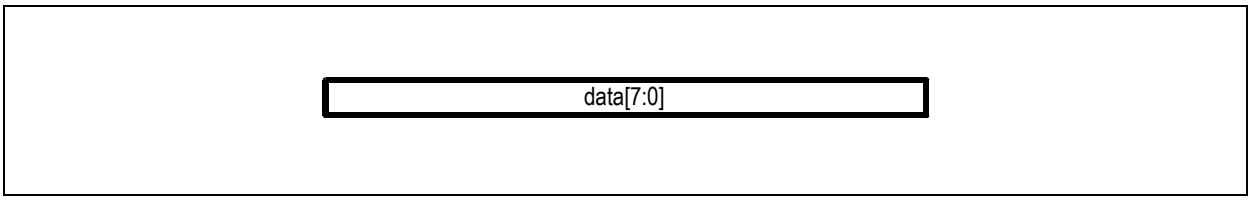


Figure 101:
Data

Bit	Meaning	Value
data[7:0]	Data	0x00 to 0xFF

Timings

Figure 102:
Write Single Data into Single Device

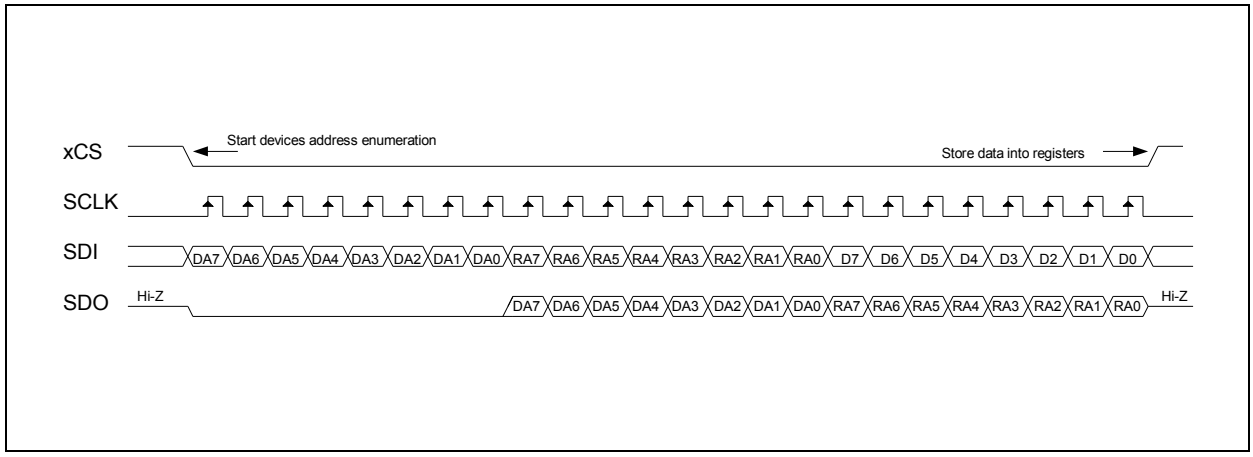
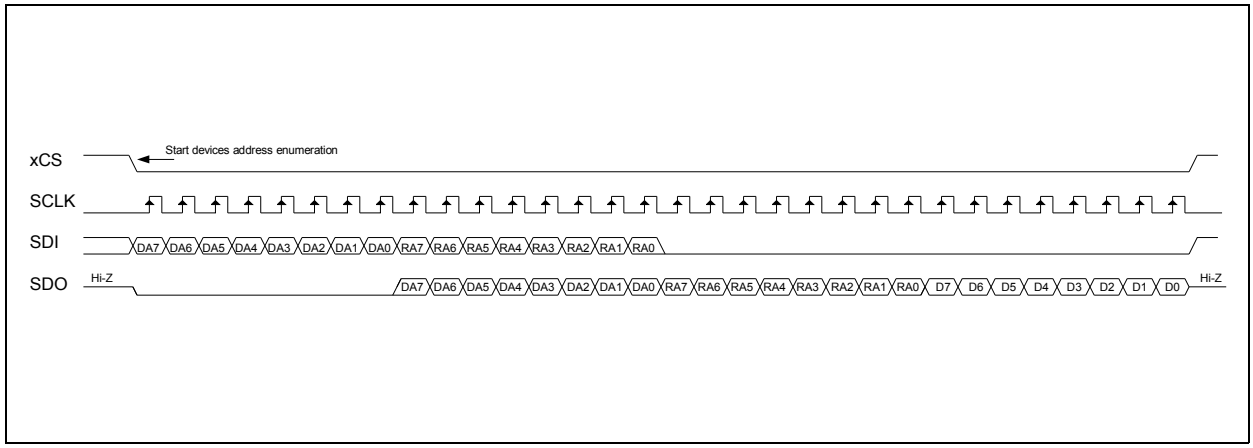


Figure 103:
Read Single Data from Single Device



DA...DevAddr

RA...RegAddr

D.....Data

SPI Protocol Examples

Write Single Data

Figure 104:
Write to Reg0x02 of Dev0x01

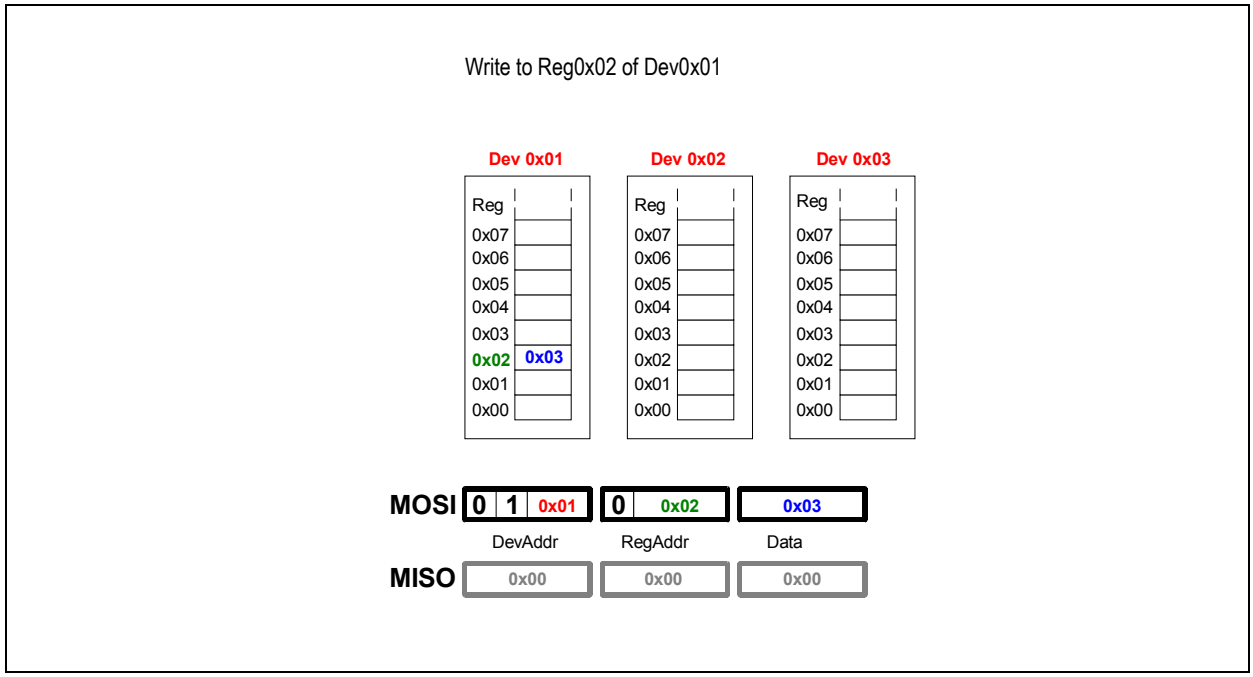
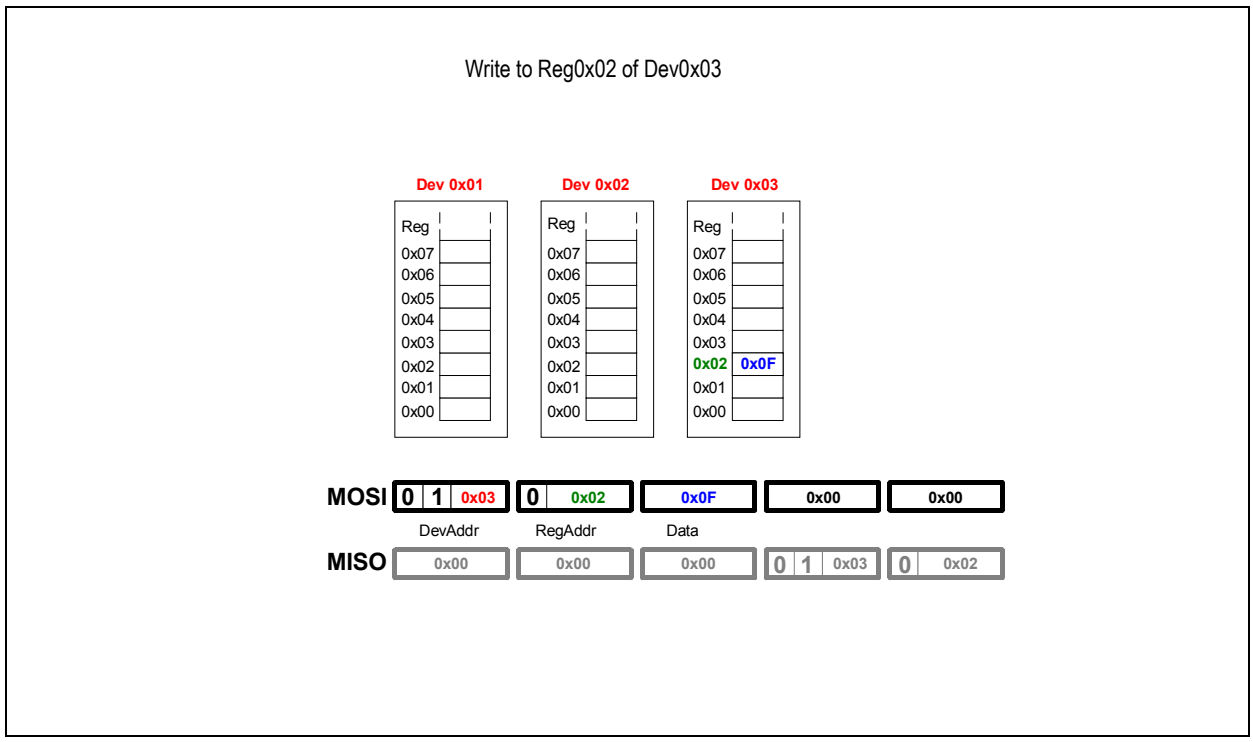
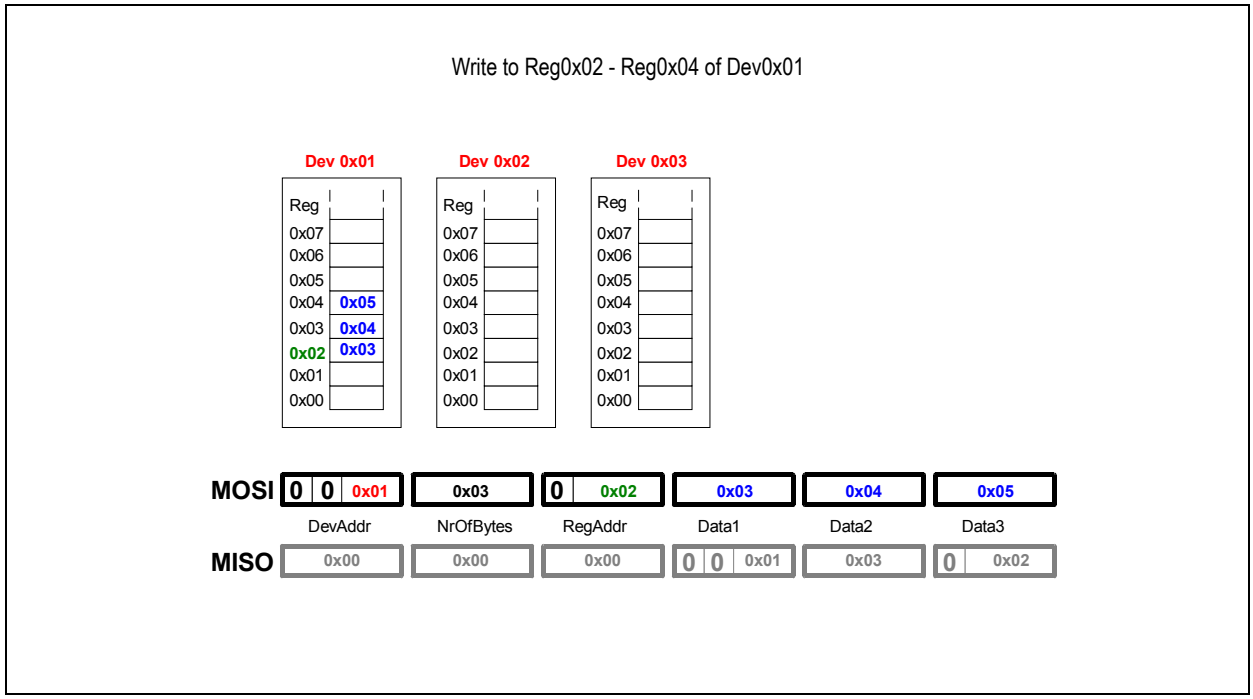


Figure 105:
Write to Reg0x02 of Dev0x03



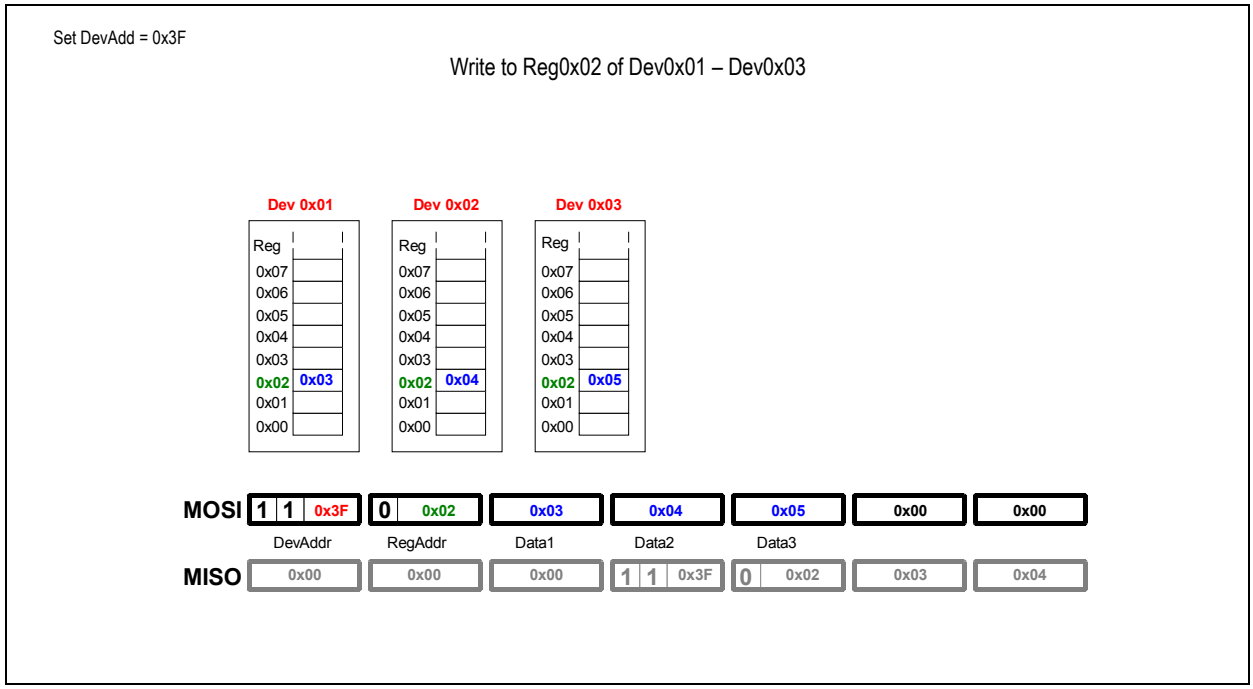
Write N Data

Figure 106:
Write to Reg0x02 - Reg0x04 of Dev0x01



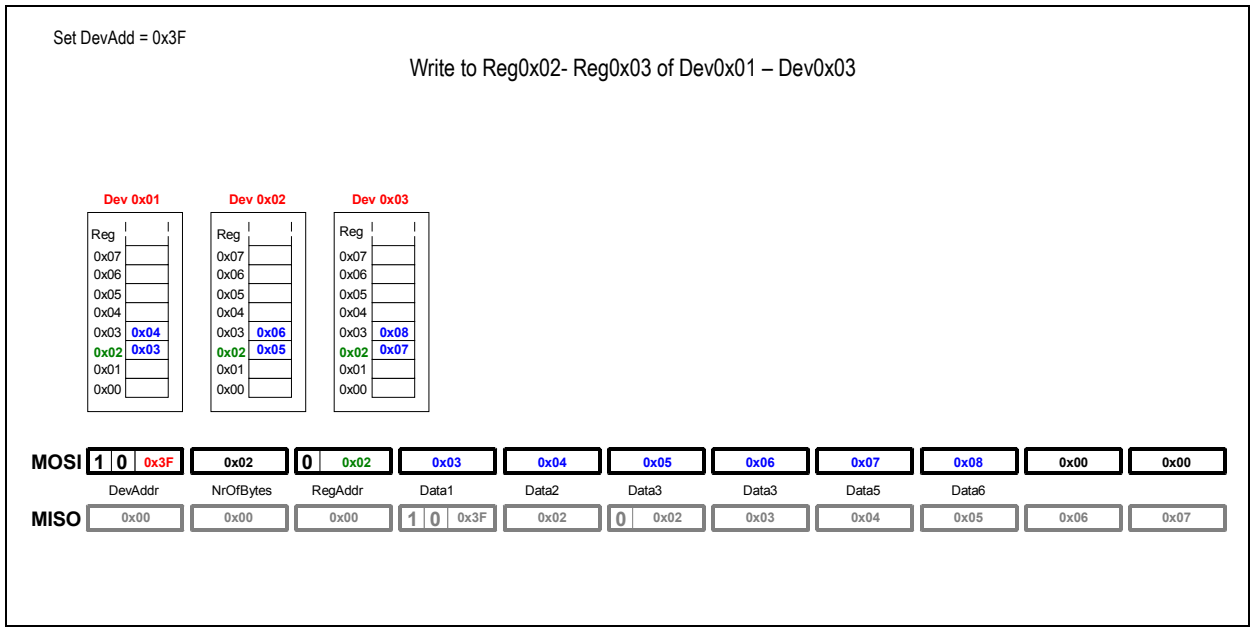
Write Different Data in Same Register of All Devices (single byte)

Figure 107:
Write to Reg0x02 of Dev0x01 – Dev0x03



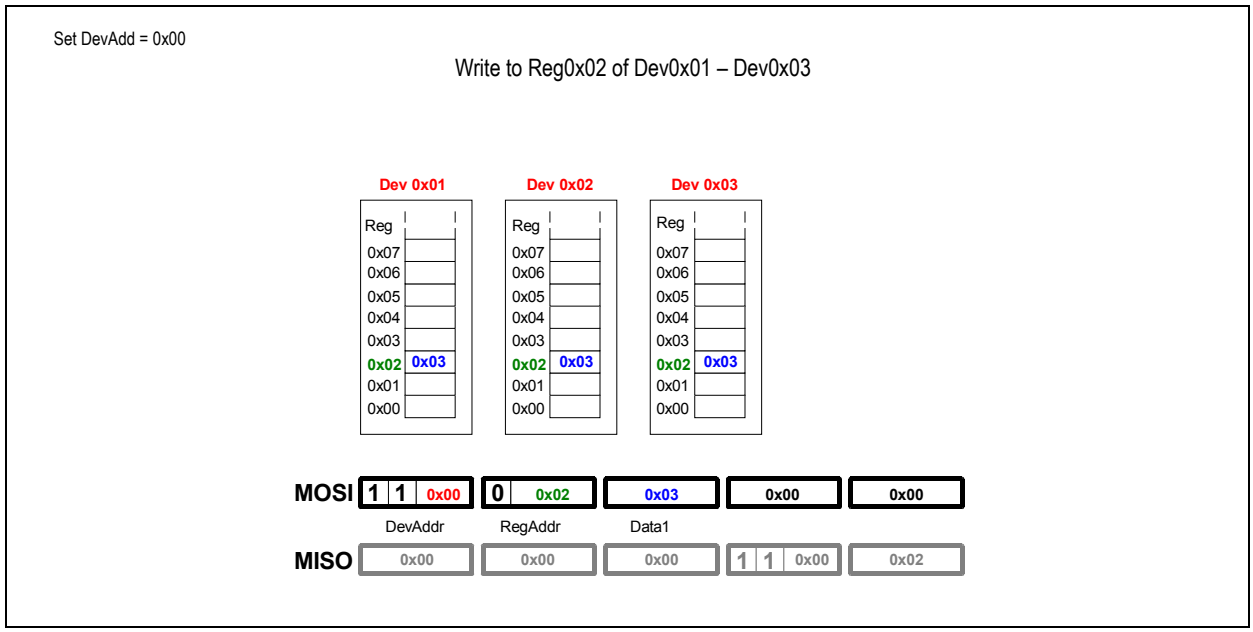
Write Different Data in Same Register of All Devices (multiple bytes)

Figure 108:
Write to Reg0x02- Reg0x03 of Dev0x01 – Dev0x03



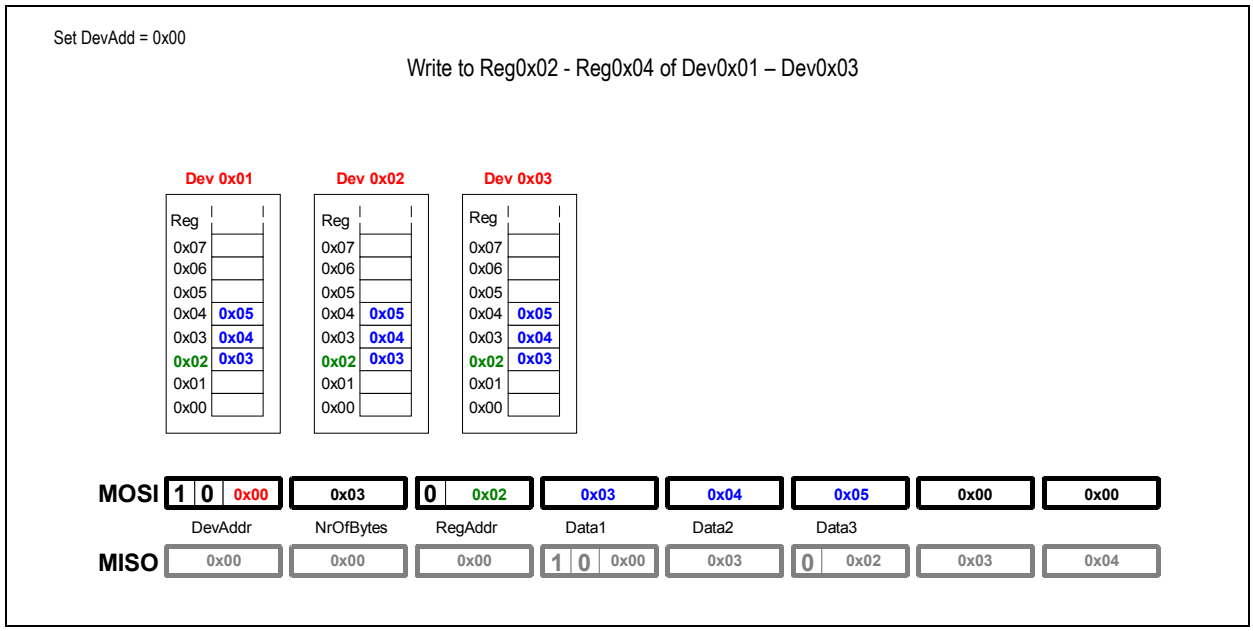
Write Same Data in Same Register of All Devices (single byte)

Figure 109:
Write to Reg0x02 of Dev0x01 – Dev0x03



Write Same Data in Same Register of All Devices (multiple bytes)

Figure 110:
Write to Reg0x02 - Reg0x04 of Dev0x01 – Dev0x03



Read Single Data

Figure 111:
Read from Reg0x02 of Dev0x01

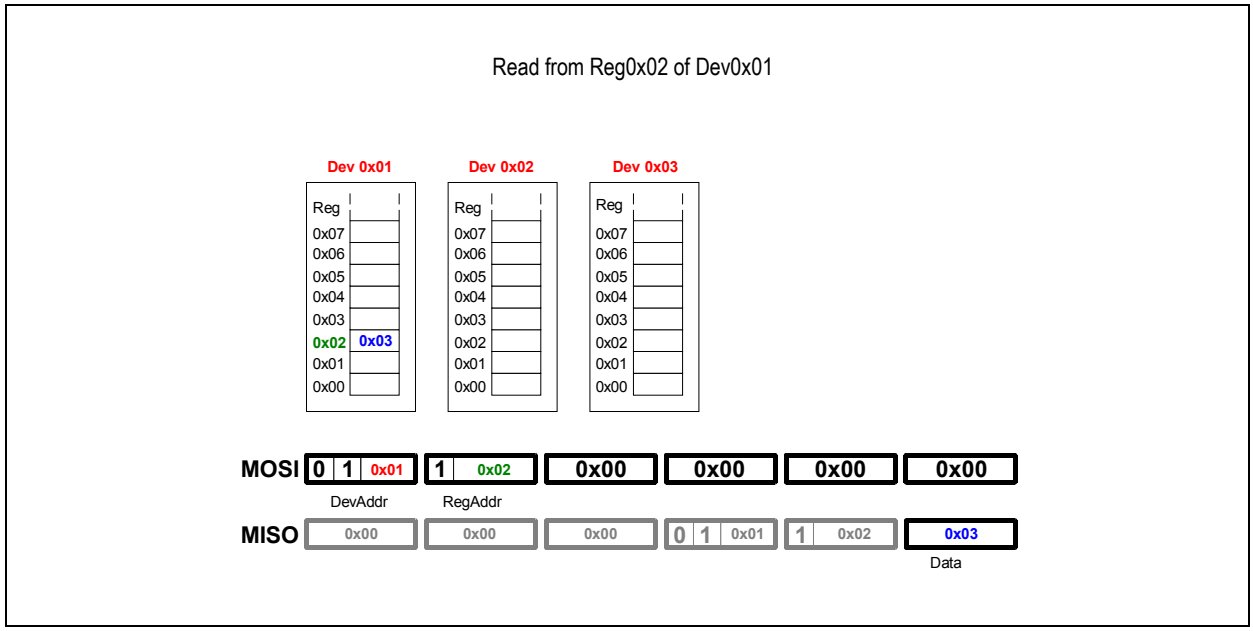
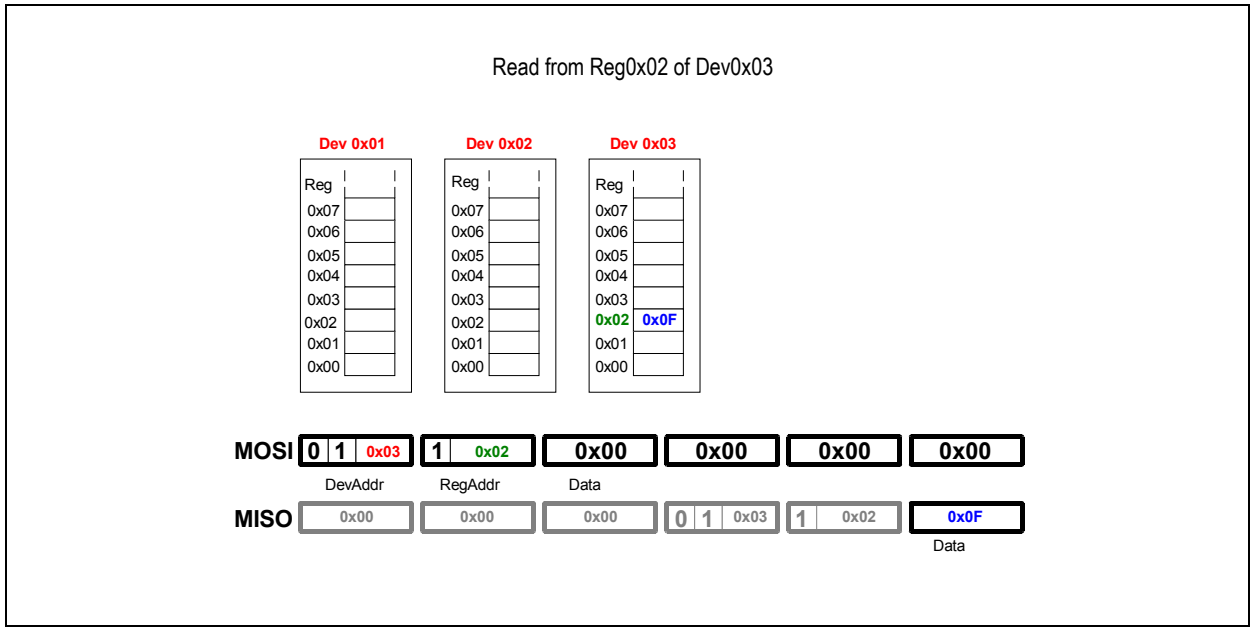
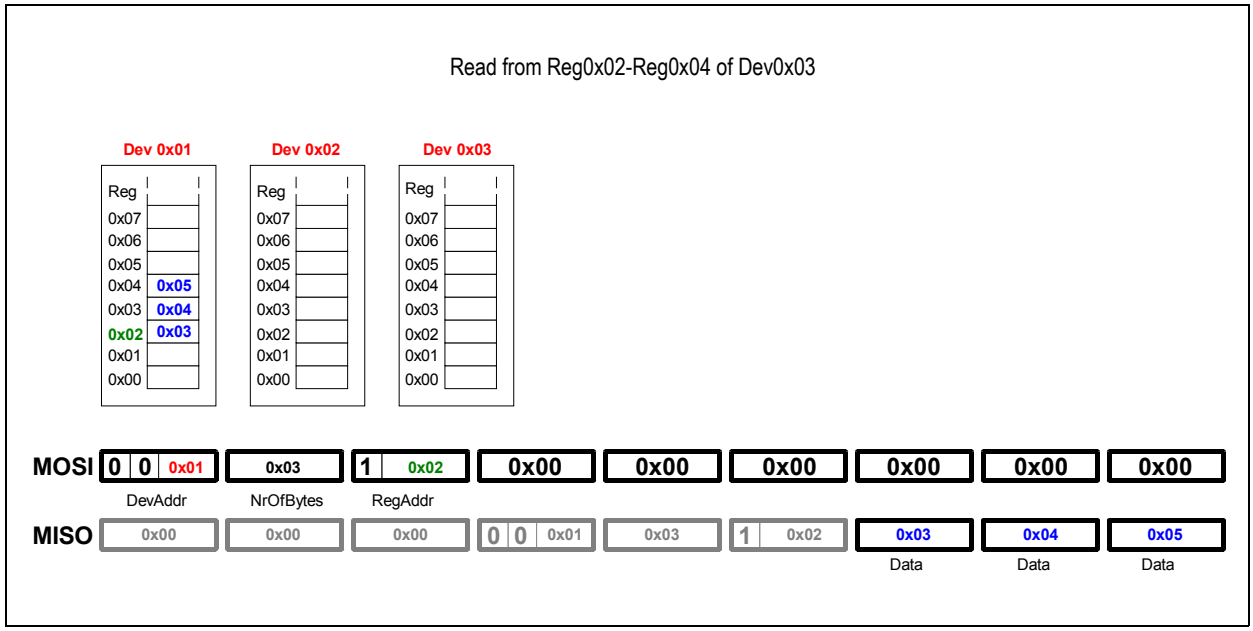


Figure 112:
Read from Reg0x02 of Dev0x03



Read N Data

Figure 113:
Read from Reg0x02-Reg0x04 of Dev0x03



Register Map

Figure 114:
Color Coding in Register Map

Registers can only be written if Group1 is UNLOCKED. Default = LOCKED
Registers can only be written if Group2 is UNLOCKED. Default = LOCKED

Figure 115:
Register Map

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x00		Used for block writing								
0x01	CUR_ON_1	Curr_8	Curr_7	Curr_6	Curr_5	Curr_4	Curr_3	Curr_2	Curr_1	0x00
0x02	CUR_ON_2	Curr_16	Curr_15	Curr_14	Curr_13	Curr_12	Curr_11	Curr_10	Curr_9	0x00
0x03	FAULT_1	Autotoff _uv	Short Bist_en	Shortcmp_en		Retrial _Open	Autotoff _ot	Open _en	Autotoff _open	0x84
0x04	GPIO_CTRL	xFAULT_config		Mode3D_config		Mode3D	DCDCEN_config		DCDCEN	0x00
0x05	FB_SEL1	FBsel_8	FBsel_7	FBsel_6	FBsel_5	FBsel_4	FBsel_3	FBsel_2	FBsel_1	0x00
0x06	FB_SEL2	FBsel_16	FBsel_15	FBsel_14	FBsel_13	FBsel_12	FBsel_11	FBsel_10	FBsel_9	0x00
0x07	CURR_CTRL	Sel_ac		Fb_ac_off	Ib_comp	DACref _buffer	DACref	Slew_rate		0x00
0x08	SHORTLED_1	Short_8	Short_7	Short_6	Short_5	Short_4	Short_3	Short_2	Short_1	0x00
0x09	SHORTLED_2	Short_16	Short_15	Short_14	Short_13	Short_12	Shor_11	Shor_10	Short_9	0x00
0x0A	OPENLED_1	Open_8	Open_7	Open_6	Open_5	Open_4	Open_3	Open_2	Open_1	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x0B	OPENLED_2	Open_16	Open_15	Open_14	Open_13	Open_12	Open_11	Open_10	Open_9	0x00
0x0C	VDAC_H	DAC9	DAC8	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	0x80
0x0D	VDAC_L							DAC1	DAC0	0x00
0x0E	FB_ON_1	FB_ Curr_8	FB_ Curr_7	FB_ Curr_6	FB_ Curr_5	FB_ Curr_4	FB_ Curr_3	FB_ Curr_2	FB_ Curr_1	0x00
0x0F	FB_ON_2	FB_ Curr_16	FB_ Curr_15	FB_ Curr_14	FB_ Curr_13	FB_ Curr_12	FB_ Curr_11	FB_ Curr_10	FB_ Curr_9	0x00
0x10	IDAC_FB1_COUNTER	IDAC_FB1_COUNTER								0x00
0x11	IDAC_FB2_COUNTER	IDAC_FB2_COUNTER								0x00
0x12	FBLOOP_CTRL	Vtrip		FB_cnt _man_fb2	FB_cnt _man_fb1	FB_count_dn_time		FB_count_up_time		0x05
0x13	PWM_CTRL	DPLL_per_s el	Clock Src1	PWM_rev	VSYNC det	VSYNC edge	Direct_ PWM	Update_ Mode	Clock Src0	0x00
0x14	PWMperiodLSB	PWM Per7	PWM Per6	PWM Per5	PWM Per4	PWM Per3	PWM Per2	PWM Per1	PWM Per0	0x00
0x15	PWMperiodMSB	0	0	0	PWM Per12	PWM Per11	PWM Per10	PWM Per9	PWM Per8	0x00
0x16	PWM1delLSB	PWM1 Del7	PWM1 Del6	PWM1 Del5	PWM1 Del4	PWM1 Del3	PWM1 Del2	PWM1 Del1	PWM1 Del0	0x00
0x17	PWM1delMSB	0	0	0	0	PWM1 Del11	PWM1 Del10	PWM1 Del9	PWM1 Del8	0x00
0x18	PWM2delLSB	PWM2 Del7	PWM2 Del6	PWM2 Del5	PWM2 Del4	PWM2 Del3	PWM2 Del2	PWM2 Del1	PWM2 Del0	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x19	PWM2delMSB	0	0	0	0	PWM2 Del11	PWM2 Del10	PWM2 Del9	PWM2 Del8	0x00
0x1A	PWM3delLSB	PWM3 Del7	PWM3 Del6	PWM3 Del5	PWM3 Del4	PWM3 Del3	PWM3 Del2	PWM3 Del1	PWM3 Del0	0x00
0x1B	PWM3delMSB	0	0	0	0	PWM3 Del11	PWM3 Del10	PWM3 Del9	PWM3 Del8	0x00
0x1C	PWM4delLSB	PWM4 Del7	PWM4 Del6	PWM4 Del5	PWM4 Del4	PWM4 Del3	PWM4 Del2	PWM4 Del1	PWM4 Del0	0x00
0x1D	PWM4delMSB	0	0	0	0	PWM4 Del11	PWM4 Del10	PWM4 Del9	PWM4 Del8	0x00
0x1E	PWM5delLSB	PWM5 Del7	PWM5 Del6	PWM5 Del5	PWM5 Del4	PWM5 Del3	PWM5 Del2	PWM5 Del1	PWM5 Del0	0x00
0x1F	PWM5delMSB	0	0	0	0	PWM5 Del11	PWM5 Del10	PWM5 Del9	PWM5 Del8	0x00
0x20	PWM6delLSB	PWM6 Del7	PWM6 Del6	PWM6 Del5	PWM6 Del4	PWM6 Del3	PWM6 Del2	PWM6 Del1	PWM6 Del0	0x00
0x21	PWM6delMSB	0	0	0	0	PWM6 Del11	PWM6 Del10	PWM6 Del9	PWM6 Del8	0x00
0x22	PWM7delLSB	PWM7 Del7	PWM7 Del6	PWM7 Del5	PWM7 Del4	PWM7 Del3	PWM7 Del2	PWM7 Del1	PWM7 Del0	0x00
0x23	PWM7delMSB	0	0	0	0	PWM7 Del11	PWM7 Del10	PWM7 Del9	PWM7 Del8	0x00
0x24	PWM8delLSB	PWM8 Del7	PWM8 Del6	PWM8 Del5	PWM8 Del4	PWM8 Del3	PWM8 Del2	PWM8 Del1	PWM8 Del0	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x25	PWM8delMSB	0	0	0	0	PWM8 Del11	PWM8 Del10	PWM8 Del9	PWM8 Del8	0x00
0x26	PWM9delLSB	PWM9 Del7	PWM9 Del6	PWM9 Del5	PWM9 Del4	PWM9 Del3	PWM9 Del2	PWM9 Del1	PWM9 Del0	0x00
0x27	PWM9delMSB	0	0	0	0	PWM9 Del11	PWM9 Del10	PWM9 Del9	PWM9 Del8	0x00
0x28	PWM10delLSB	PWM10 Del7	PWM10 Del6	PWM10 Del5	PWM10 Del4	PWM10 Del3	PWM10 Del2	PWM10 Del1	PWM10 Del0	0x00
0x29	PWM10delMSB	0	0	0	0	PWM10 Del11	PWM10 Del10	PWM10 Del9	PWM10 Del8	0x00
0x2A	PWM11delLSB	PWM11 Del7	PWM11 Del6	PWM11 Del5	PWM11 Del4	PWM11 Del3	PWM11 Del2	PWM11 Del1	PWM1 Del0	0x00
0x2B	PWM11delMSB	0	0	0	0	PWM11 Del11	PWM11 Del10	PWM11 Del9	PWM Del8	0x00
0x2C	PWM12delLSB	PWM12 Del7	PWM12 Del6	PWM12 Del5	PWM12 Del4	PWM12 Del3	PWM12 Del2	PWM12 Del1	PWM12 Del0	0x00
0x2D	PWM12delMSB	0	0	0	0	PWM12 Del11	PWM12 Del10	PWM12 Del9	PWM12 Del8	0x00
0x2E	PWM13delLSB	PWM13 Del7	PWM13 Del6	PWM13 Del5	PWM13 Del4	PWM13 Del3	PWM13 Del2	PWM13 Del1	PWM13 Del0	0x00
0x2F	PWM13delMSB	0	0	0	0	PWM13 Del11	PWM13 Del10	PWM13 Del9	PWM13 Del8	0x00
0x30	PWM14delLSB	PWM14 Del7	PWM14 Del6	PWM14 Del5	PWM14 Del4	PWM14 Del3	PWM14 Del2	PWM14 Del1	PWM14 Del0	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x31	PWM14delMSB	0	0	0	0	PWM14 Del11	PWM14 Del10	PWM14 Del9	PWM14 Del8	0x00
0x32	PWM15delLSB	PWM15 Del7	PWM15 Del6	PWM15 Del5	PWM15 Del4	PWM15 Del3	PWM15 Del2	PWM15 Del1	PWM15 Del0	0x00
0x33	PWM15delMSB	0	0	0	0	PWM15 Del11	PWM15 Del10	PWM15 Del9	PWM15 Del8	0x00
0x34	PWM16delLSB	PWM16 Del7	PWM16 Del6	PWM16 Del5	PWM16 Del4	PWM16 Del3	PWM16 Del2	PWM16 Del1	PWM16 Del0	0x00
0x35	PWM16delMSB	0	0	0	0	PWM16 Del11	PWM16 Del10	PWM16 Del9	PWM16 Del8	0x00
0x36	LOCKUNLOCK	MagicByte								0x00
0x37	PWM1htLSB	PWM1 HT7	PWM1 HT6	PWM1 HT5	PWM1 HT4	PWM1 HT3	PWM1 HT2	PWM1 HT1	PWM1 HT0	0x00
0x38	PWM1htMSB	0	0	0	0	PWM1 HT11	PWM1 HT10	PWM1 HT9	PWM1 HT8	0x00
0x39	PWM2htLSB	PWM2 HT7	PWM2 HT6	PWM2 HT5	PWM2 HT4	PWM2 HT3	PWM2 HT2	PWM2 HT1	PWM2 HT0	0x00
0x3A	PWM2htMSB	0	0	0	0	PWM2 HT11	PWM2 HT10	PWM2 HT9	PWM2 HT8	0x00
0x3B	PWM3htLSB	PWM3 HT7	PWM3 HT6	PWM3 HT5	PWM3 HT4	PWM3 HT3	PWM3 HT2	PWM3 HT1	PWM3 HT0	0x00
0x3C	PWM3htMSB	0	0	0	0	PWM3 HT11	PWM3 HT10	PWM3 HT9	PWM3 HT8	0x00
0x3D	PWM4htLSB	PWM4 HT7	PWM4 HT6	PWM4 HT5	PWM4 HT4	PWM4 HT3	PWM4 HT2	PWM4 HT1	PWM4 HT0	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x3E	PWM4htMSB	0	0	0	0	PWM4 HT11	PWM4 HT10	PWM4 HT9	PWM4 HT8	0x00
0x3F	PWM5htLSB	PWM5 HT7	PWM5 HT6	PWM5 HT5	PWM5 HT4	PWM5 HT3	PWM5 HT2	PWM5 HT1	PWM5 HT0	0x00
0x40	PWM5htMSB	0	0	0	0	PWM5 HT11	PWM5 HT10	PWM5 HT9	PWM5 HT8	0x00
0x41	PWM6htLSB	PWM6 HT7	PWM6 HT6	PWM6 HT5	PWM6 HT4	PWM6 HT3	PWM6 HT2	PWM6 HT1	PWM6 HT0	0x00
0x42	PWM6htMSB	0	0	0	0	PWM6 HT11	PWM6 HT10	PWM6 HT9	PWM6 HT8	0x00
0x43	PWM7htLSB	PWM7 HT7	PWM7 HT6	PWM7 HT5	PWM7 HT4	PWM7 HT3	PWM7 HT2	PWM7 HT1	PWM7 HT0	0x00
0x44	PWM7htMSB	0	0	0	0	PWM7 HT11	PWM7 HT10	PWM7 HT9	PWM7 HT8	0x00
0x45	PWM8htLSB	PWM8 HT7	PWM8 HT6	PWM8 HT5	PWM8 HT4	PWM8 HT3	PWM8 HT2	PWM8 HT1	PWM8 HT0	0x00
0x46	PWM8htMSB	0	0	0	0	PWM8 HT11	PWM8 HT10	PWM8 HT9	PWM8 HT8	0x00
0x47	PWM9htLSB	PWM9 HT7	PWM9 HT6	PWM9 HT5	PWM9 HT4	PWM9 HT3	PWM9 HT2	PWM9 HT1	PWM9 HT0	0x00
0x48	PWM9htMSB	0	0	0	0	PWM9 HT11	PWM9 HT10	PWM9 HT9	PWM9 HT8	0x00
0x49	PWM10htLSB	PWM10 HT7	PWM10 HT6	PWM10 HT5	PWM10 HT4	PWM10 HT3	PWM10 HT2	PWM10 HT1	PWM10 HT0	0x00

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x4A	PWM10htMSB	0	0	0	0	PWM10 HT11	PWM10 HT10	PWM10 HT9	PWM10 HT8	0x00
0x4B	PWM11htLSB	PWM11 HT7	PWM11 HT6	PWM11 HT5	PWM11 HT4	PWM11 HT3	PWM11 HT2	PWM11 HT1	PWM11 HT0	0x00
0x4C	PWM11htMSB	0	0	0	0	PWM11 HT11	PWM11 HT10	PWM11 HT9	PWM11 HT8	0x00
0x4D	PWM12htLSB	PWM12 HT7	PWM12 HT6	PWM12 HT5	PWM12 HT4	PWM12 HT3	PWM12 HT2	PWM12 HT1	PWM12 HT0	0x00
0x4E	PWM12htMSB	0	0	0	0	PWM12 HT11	PWM12 HT10	PWM12 HT9	PWM12 HT8	0x00
0x4F	PWM13htLSB	PWM13 HT7	PWM13 HT6	PWM13 HT5	PWM13 HT4	PWM13 HT3	PWM13 HT2	PWM13 HT1	PWM13 HT0	0x00
0x50	PWM13htMSB	0	0	0	0	PWM13 HT11	PWM13 HT10	PWM13 HT9	PWM13 HT8	0x00
0x51	PWM14htLSB	PWM14 HT7	PWM14 HT6	PWM14 HT5	PWM14 HT4	PWM14 HT3	PWM14 HT2	PWM14 HT1	PWM14 HT0	0x00
0x52	PWM14htMSB	0	0	0	0	PWM14 HT11	PWM14 HT10	PWM14 HT9	PWM14 HT8	0x00
0x53	PWM15htLSB	PWM15 HT7	PWM15 HT6	PWM15 HT5	PWM15 HT4	PWM15 HT3	PWM15 HT2	PWM15 HT1	PWM15 HT0	0x00
0x54	PWM15htMSB	0	0	0	0	PWM5 HT11	PWM15 HT10	PWM15 HT9	PWM15 HT8	0x00
0x55	PWM16htLSB	PWM16 HT7	PWM16 HT6	PWM16 HT5	PWM16 HT4	PWM16 HT3	PWM16 HT2	PWM16 HT1	PWM16 HT0	0x00

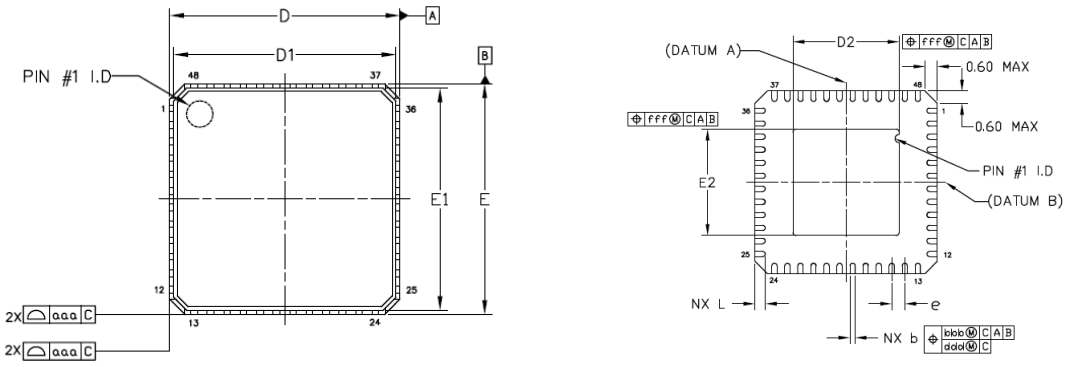
Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x56	PWM16htMSB	0	0	0	0	PWM16 HT11	PWM16 HT10	PWM16 HT9	PWM16 HT8	0x00
0x57	ASICIDLSB	Asic_ID0				Rev Nr.				0xA0
0x58	ASICIDMSB	ASIC_ID2				ASIC_ID1				0x20
0x59	Not used									0x00
0x60	STATUS	STAT Nosync	STAT OT	STAT Open	Short Bist	Vcnt underflow	Short2	Short1	Power good	0x00
0x61	PLLmultiMSB	PLL Multi15	PLL Multi14	PLL Multi13	PLL Multi12	PLL Multi11	PLL Multi10	PLL Multi9	PLL Multi8	0x00
0x62	PLLmultiLSB	PLL Multi7	PLL Multi6	PLL Multi5	PLL Multi4	PLL Multi3	PLL Multi2	PLL Multi1	PLL Multi0	0x00
0x63	SHORT_BIST_CTRL1	0	0	0	BIST _retrial	BIST _steptime	Autotoff _BIST	BIST_wait		0x02
0x64	SHORT_BIST_MAXSTEP	BIST maxstep7	BIST Maxstep6	BIST Maxstep5	BIST Maxstep4	BIST Maxstep3	BIST Maxstep2	BIST Maxstep1	BIST Maxstep0	0xFF
0x65	SHORT_BIST_CTRL2	0	0	COMP _retrial	Autotoff _COMP	COMP level				0x0A
0x6C	CompReg_1	Comp Reg8	Comp Reg7	Comp Reg6	Comp Reg5	Comp Reg4	Comp Reg3	Comp Reg2	Comp Reg1	0x00
0x6D	CompReg_2	Comp Reg16	Comp Reg15	Comp Reg14	Comp Reg13	Comp Reg12	Comp Reg11	Comp Reg10	Comp Reg9	0x00

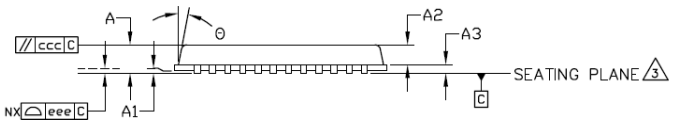
Note(s):

1. Addresses from 0x66 to 0x6b and above 0x6d are for factory test only. DO NOT WRITE!

Package Drawings & Markings

Figure 116:
48-pin QFN Package





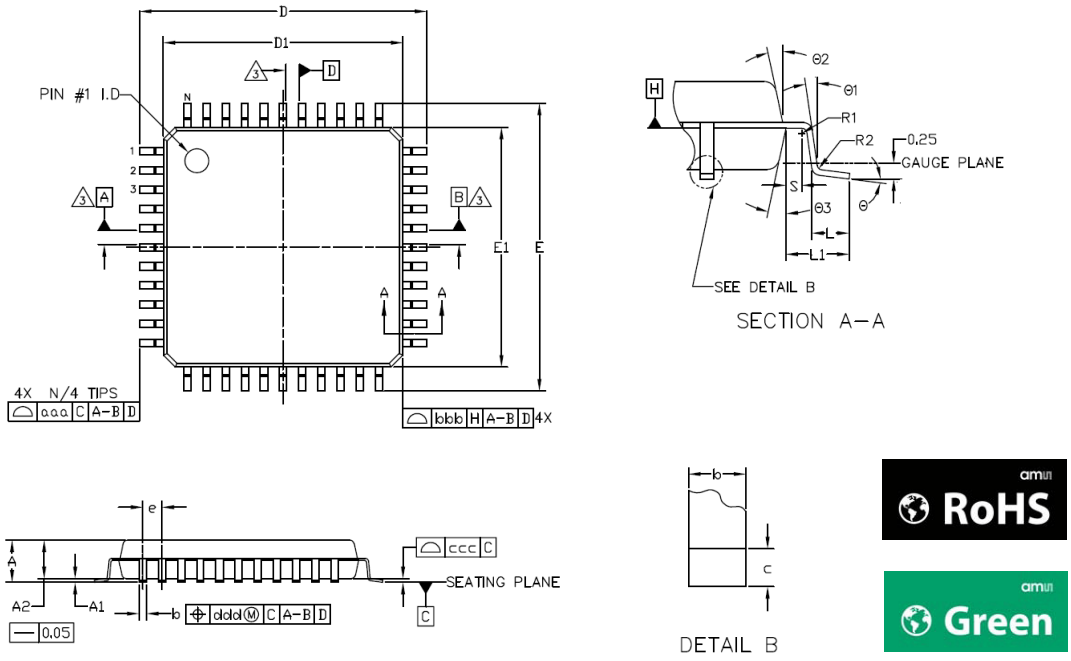
Ref	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3	-	0.20 REF	-
L	0.35	0.40	0.45
Θ	0°	-	14°
b	0.18	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
D2	4.00	4.10	4.20

Ref	Min	Nom	Max
E2	4.00	4.10	4.20
D1	-	6.75 BSC	-
E1	-	6.75 BSC	-
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N	48		

Note(s):

1. Dimensions and tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

Figure 117:
LQFP 44 Package



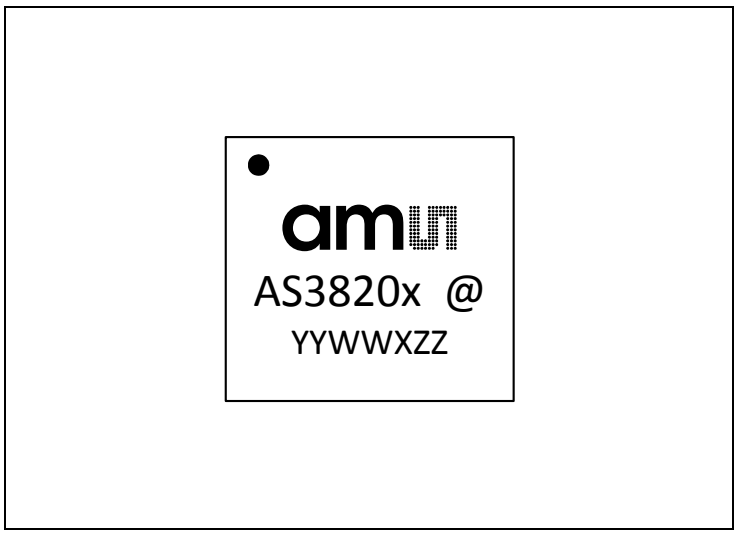
Ref	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	-	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

Ref	Min	Nom	Max
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
Θ	0°	3.5°	7°
Θ1	0°	-	-
Θ2	11°	12°	13°
Θ3	11°	12°	13°
aaa	-	0.20	-
bbb	-	0.20	-
ccc	-	0.10	-
ddd	-	0.20	-
N	44		

Note(s):

1. Dimensions and tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Datums A-B and D to be determined at datum H.

Figure 118:
48-Pin QFN Marking



Note(s):
1. AS3820**x**: '**x**' represents variant A or E

Figure 119:
44-Pin LQFP Marking

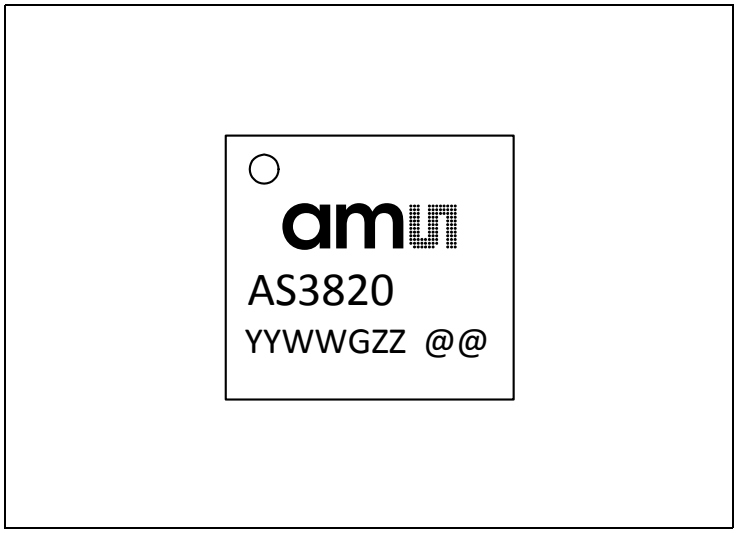


Figure 120:
Packaging Code YYWWXZZ or YYWWGZZ

YY	WW	X or G	ZZ
Last two digits of the manufacturing year	Manufacturing week	Plant identifier	Free choice/ traceability code

Thermal Characteristics QFN48

The thermal characteristics of the devices were measured at 25°C ambient temperature. The device was mounted on a double sided FR4 PCB with the bottom layer used as cooling area.

Figure 121:
PCB FR4, 1cm Distance from Ground

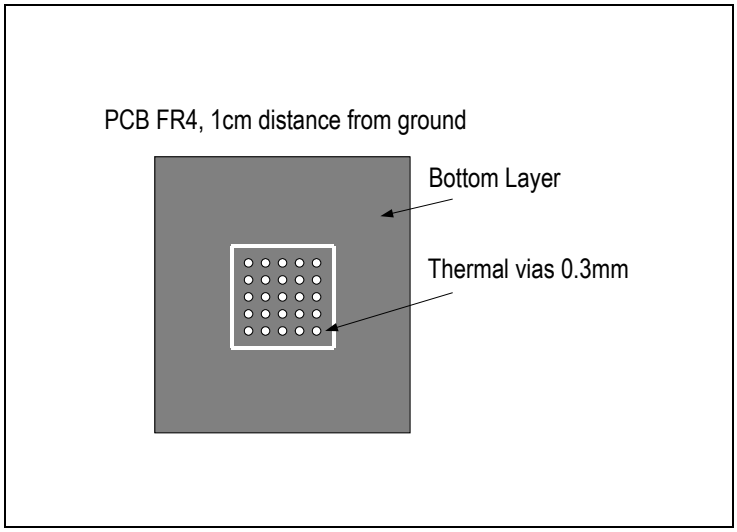


Figure 122:
Tcase vs Power QFN48 with Different Copper Area, Tamb = 25°C

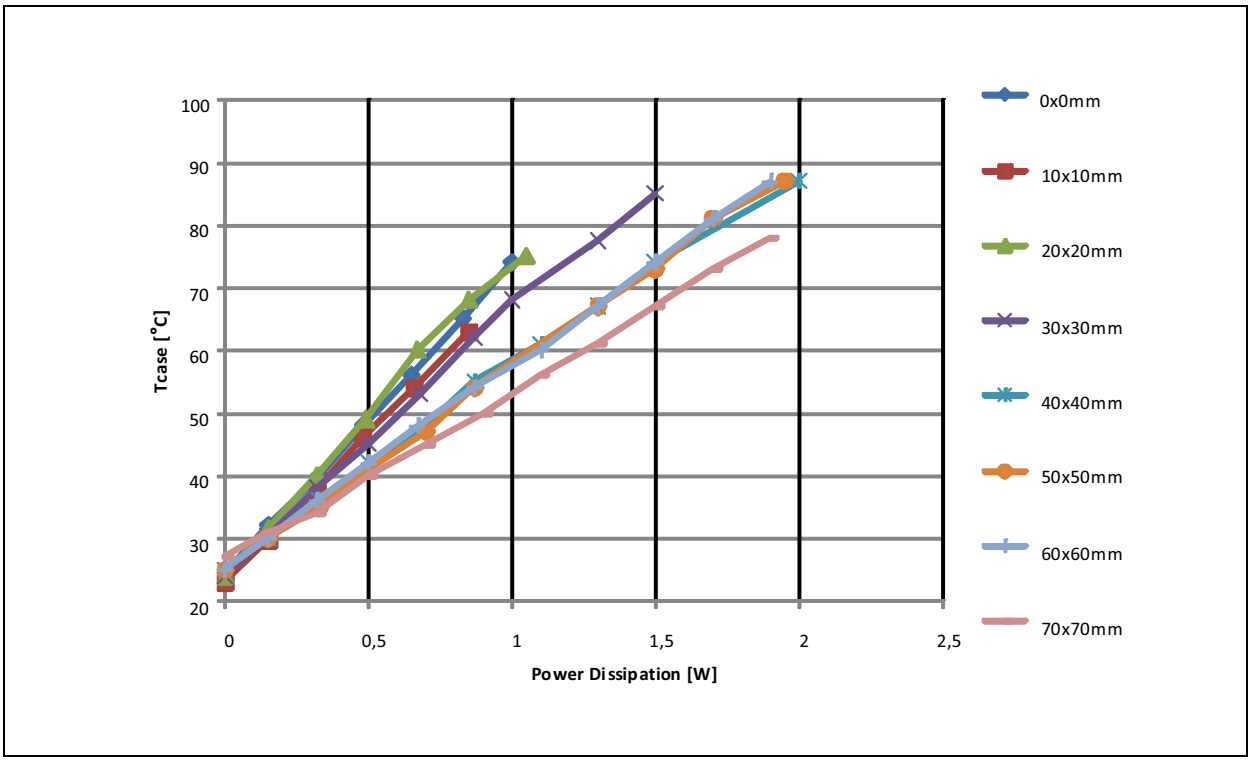
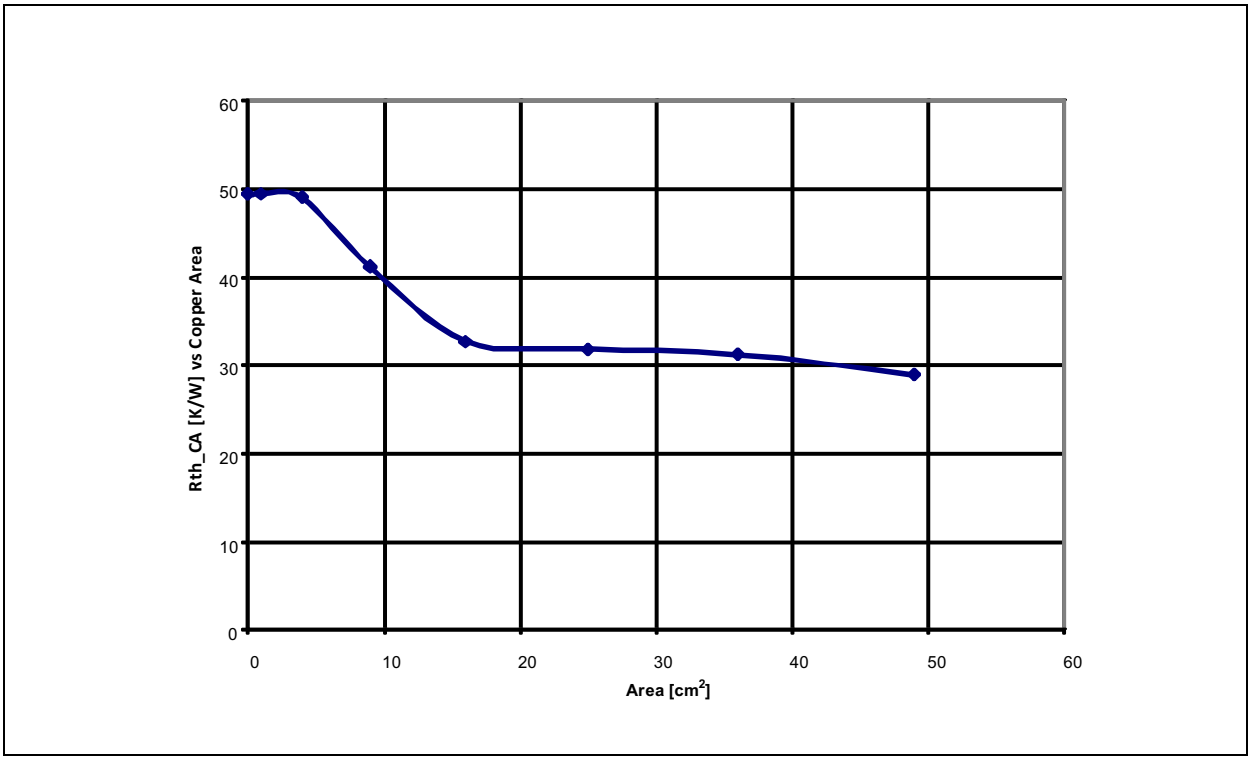


Figure 123:
Rth_CA [K/W] vs Copper Area



Ordering & Contact Information

Figure 124:
Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS3820A-ZQFT	AS3820A	16 Channel White LED Controller for LCD Backlight	Tape & Reel	48-pin QFN
AS3820E-ZQFT	AS3820E	16 Channel White LED Controller for LCD Backlight Direct PWM Mode Activated	Tape & Reel	48-pin QFN
AS3820-ZLQT	AS3820	16 Channel White LED Controller for LCD Backlight	Tape & Reel	44-pin LQFP

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Revision Information

Changes from 1.9 to current revision 2-00 (2015-Dec-23)	Page
Content of austriamicrosystems datasheet was converted to latest **ams** design	
Updated Figure 1	1
Updated Figure 13	11
Updated Figure 14	12

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide