AS3992

UHF RFID Single Chip Reader EPC Class1 Gen2 Compatible

General Description

The AS3992 UHF reader chip is an integrated analog front-end and provides protocol handling for ISO180006c/b 900MHz RFID reader systems. Equipped with multiple built-in programming options, the device is suitable for a wide range of UHF RFID applications.

The AS3992 is pin to pin and firmware compatible with the previous AS3990/91 IC's. It offers improved receive sensitivity to -86dB, programmable Rx Dense Reader Mode (DRM) filters on chip and pre-distortion. Fully scalable, the AS3992 is ideal for longer range and higher power applications.

Offering DRM filtering on chip, combined with improved sensitivity and pre-distortion allows the AS3992 to be the only true world wide shippable IC. The reader configuration is achieved through setting control registers allowing fine tuning of different reader parameters.

The AS3992 complies with EPC Class 1 Generation 2 protocol (ISO 18000-6C) and ISO 18000-6A/B (in direct mode).

Parallel or serial interface can be selected for communication between the host system (MCU) and the reader IC. When hardware coders and decoders are used for transmission and reception, data is transferred via 24 bytes FIFO register. In case of direct transmission or reception, coders and decoders are bypassed and the host system can service the analog front end in real time.

The transmitter generates 20dBm output power into 50Ω load and is capable of ASK or PR-ASK modulation. The integrated supply voltage regulators ensure supply rejection of the complete reader system.

The transmission system comprises low level data coding. Automatic generation of FrameSync, Preamble, and CRC is supported.

The receiver system allows AM and PM demodulation. The receiver also comprises automatic gain control option (patent pending) and selectable gain and signal bandwidth to cover a range of input link frequency and bit rate options. The signal strength of AM and PM modulation is measured and can be accessed in RSSI register. The receiver output is selectable between digitized sub-carrier signal and any of integrated sub-carrier decoders. Selected decoders deliver bit stream and data clock as outputs.

The receiver system also comprises framing system. This system performs the CRC check and organizes the data in bytes. Framed data is accessible to the host system through a 24 byte FIFO register.

To support external MCU and other circuitry a 3.3V regulated supply and clock outputs are available. The regulated supply has 20mA current capability.

The AS3992 is available in a 64-pin QFN (9mm × 9mm), ensuring the smallest possible footprint.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of the AS3992 UHF reader chip, are listed below:

Figure 1:
Added Value of Using AS3992

Benefits	Features
• Wide input supply range	• Supply voltage range 4.1V to 5.5V

• Integration means simpler BOM	• Filters dedicated to 250kHz and 320kHz M4 and M8 DRM operation. Available RX modes:
	  • LF40kHz, 160kHz: FM0, M2, M4, M8
	  • LF 250kHz, 320kHz, 640kHz: M4, M8

• Compliant to EPC standard	• ISO18000-6C (EPC Gen2) full protocol support
• Flexibility for variations in standards	• ISO18000-6A,B compatibility in direct mode
• Integration means simpler BOM	• Programmable Dense Reader Mode filters on chip allowing a true World Wide Shippable device
• Increased read range	• Improved receive sensitivity to -86dBm
• Integration means simpler BOM	• On chip pre-distortion meaning improved external PA efficiency • Integrated low level transmission coding, Integrated low level decoders • Integrated data framing, Integrated CRC checking
• Flexibility in interfaces	• Parallel 8-bit or serial 4-pin SPI interface to MCU using 24 bytes FIFO
• Integration reduces need for level shifter independent of the MCU supply	• Voltage range for communication to MCU between 1.8V and 5.5V
• Minimize need for external regulator	• Can be powered by USB with no need for step conversion from 4.1V to 5.5V
• Flexibility for different MCU's	• Selectable clock output for MCU

Benefits	Features
• Integration means simpler BOM	• Integrated supply voltage regulator (20mA), which can be used to supply MCU and other external circuitry • Integrated supply voltage regulator for the RF output stage, providing rejection to supply noise • Internal power amplifier (20dBm) for short range applications
• Flexibility and improved performance	• Antenna driver using ASK or PR-ASK modulation • Adjustable ASK modulation index
• Reliable tag reads	• AM & PM demodulation ensuring no “communication holes” with automatic I/Q selection
• Flexibility in design	• Selectable reception gain, Reception automatic gain control • AD converter for measuring TX power using external RF power detector • DA converter for controlling external power amplifier • Frequency hopping support
• Ease in design due to integration	• On-board VCO and PLL covering complete RFID frequency range 840MHz to 960MHz
• Lower cost xtal	• Oscillator using 20MHz crystal
• Configurability based on power needs	• Power down, standby and active mode available

Applications

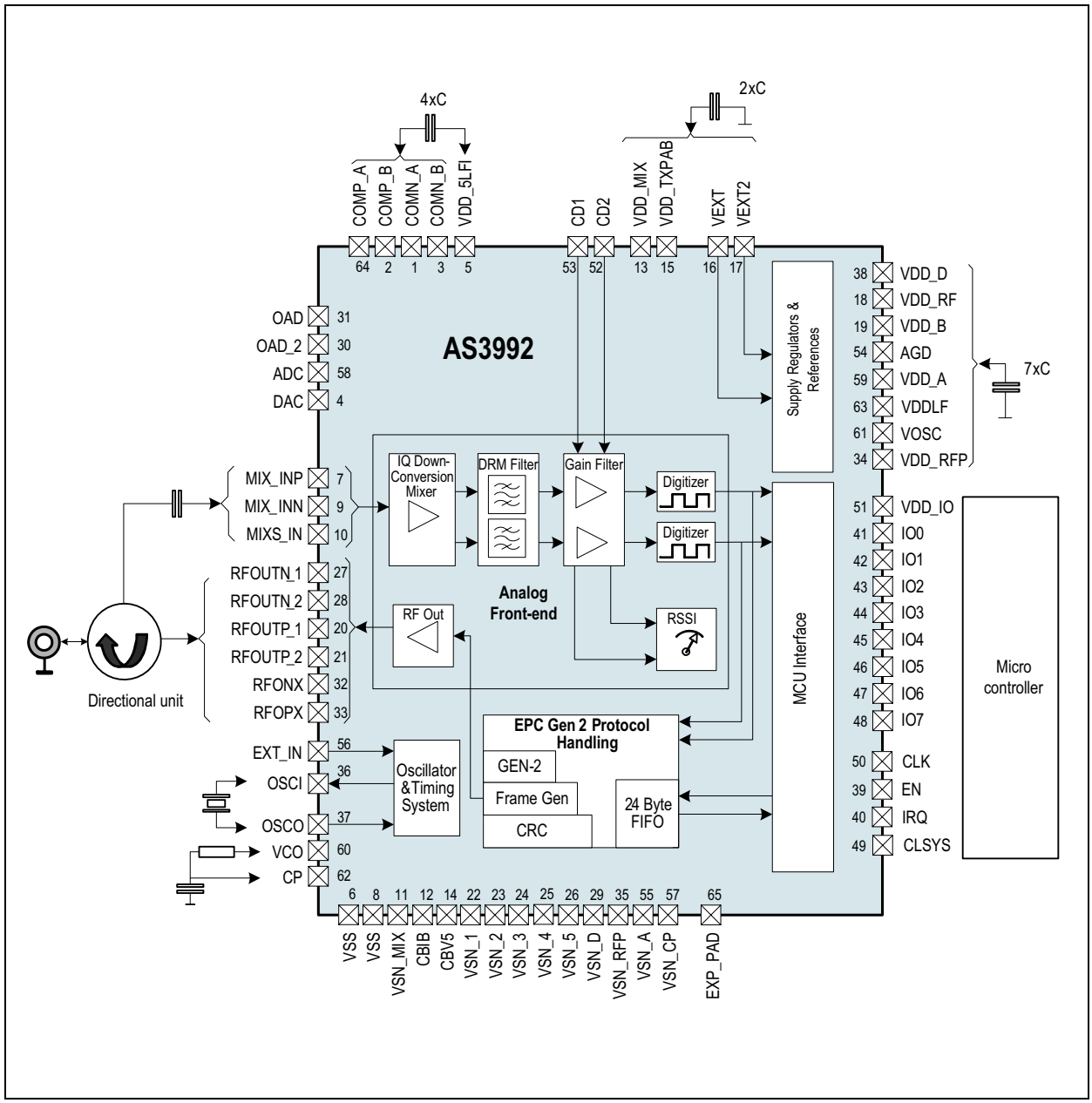
The device is an ideal solution for:

- UHF RFID reader systems
- Hand-held UHF RFID readers

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS3992 Block Diagram



Pin Assignments

The AS3992 pin assignments are described below:

Figure 3:
Pin Diagram (Top View)

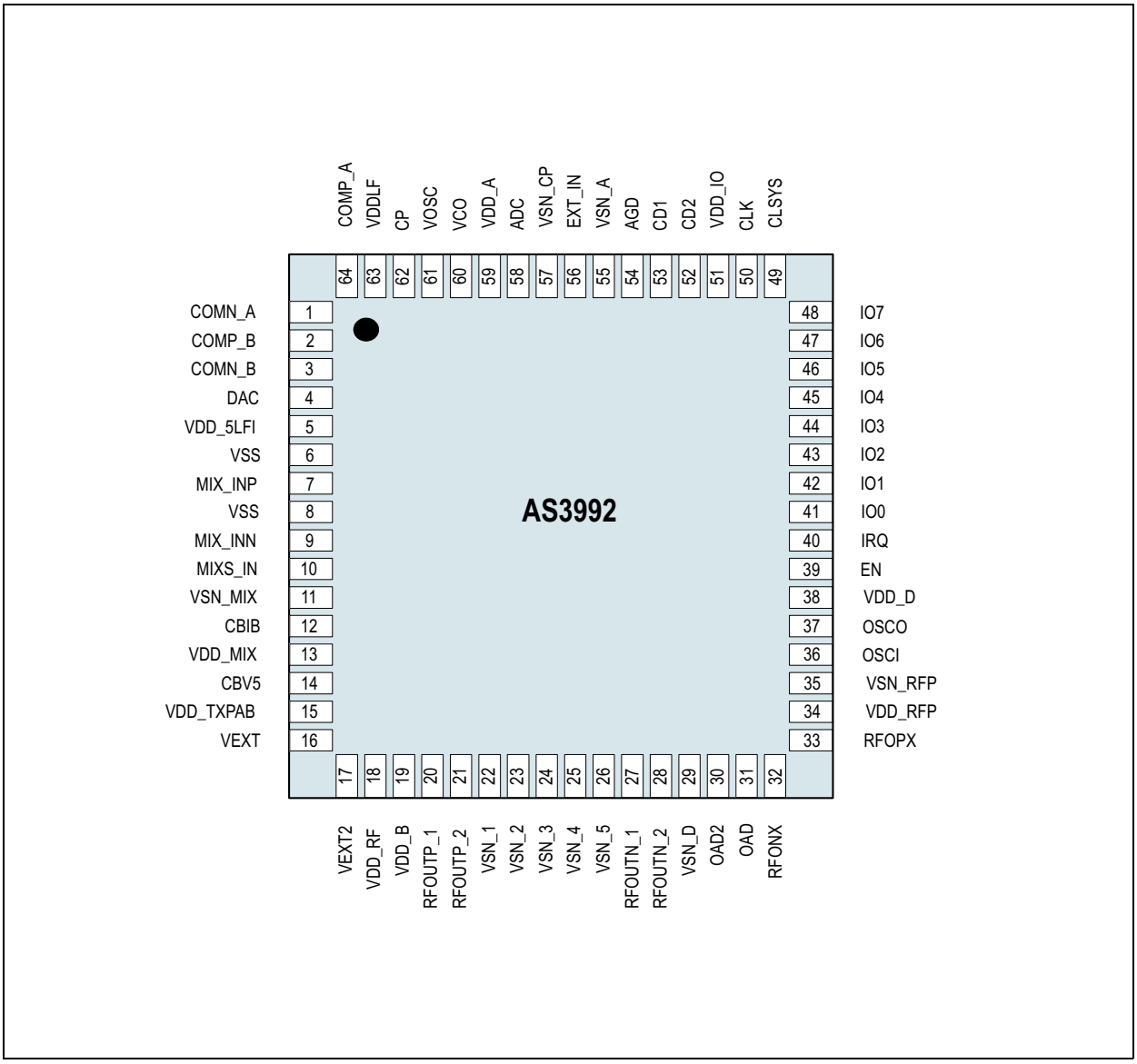


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	COMN_A	Bidirectional	Connect de-coupling capacitor to VDD_5LFI
2	COMP_B	Bidirectional	
3	COMN_B	Bidirectional	
4	DAC	Output	DAC output for external amplifier support, output resistance of DAC pin is 1kΩ
5	VDD_5LFI	Supply Input	Positive supply for LF input stage, connect to VDD_MIX
6	VSS	Supply Input	Substrate
7	MIX_INP	Input	Differential mixer positive input
8	VSS	Supply Input	Substrate
9	MIX_INN	Input	Differential mixer negative input
10	MIXS_IN	Input	Single ended mixer input
11	VSN_MIX	Supply Input	Mixer negative supply
12	CBIB	Bidirectional	Internal node de-coupling capacitor to GND
13	VDD_MIX	Supply Output	Mixer positive supply, internally regulated to 4.8V
14	CBV5	Bidirectional	Internal node de-coupling capacitor to VDD_MIX
15	VDD_TXPAB	Supply Input	Power Amplifier Bias positive supply. Connect to VDD_MIX
16	V_{EXT}	Supply Input	Main positive supply input (5V to 5.5V)
17	V_{EXT2}	Supply Input	PA positive supply regulator input (2.5V to 5.5V)
18	VDD_RF	Supply Output	PA positive supply regulator output, internally regulated to 2V - 3.5V
19	VDD_B	Supply Output	PA buffer positive supply. Internally regulated to 3.4V
20	RFOUTP_1	Output	PA positive RF output RFOUT1 and RFOUT2 must be tied together
21	RFOUTP_2	Output	
22	VSN_1	Supply Input	PA negative supply
23	VSN_2	Supply Input	
24	VSN_3	Supply Input	
25	VSN_4	Supply Input	
26	VSN_5	Supply Input	

Pin Number	Pin Name	Pin Type	Description
27	RFOUTN_1	Output	PA negative RF output or used in single ended mode. RFOUT1 and RFOUT2 must be tied together
28	RFOUTN_2	Output	
29	VSN_D	Supply Output	Digital negative supply
30	OAD2	Bidirectional	Analog or digital received signal output and MCU support mode sense input
31	OAD	Bidirectional	Analog or digital received signal output
32	RFONX	Output	Low power linear negative RF output (~0dBm)
33	RFOPX	Output	Low power linear positive RF output (~0dBm)
34	VDD_RFP	Supply Output	RF path positive supply, internally regulated to 3.4V
35	VSN_RFP	Supply Input	RF path negative supply
36	OSCI	Input	Crystal oscillator input
37	OSCO	Bidirectional	Crystal oscillator output or external 20MHz clock input
38	VDD_D	Supply Output	Digital part positive supply, internally regulated to 3.4V
39	EN	Input	Enable input
40	IRQ	Output	Interrupt output
41	IO0	Bidirectional	I/O pin for parallel communication
42	IO1	Bidirectional	
43	IO2	Bidirectional	I/O pin for parallel communication EnableRX input in case of direct mode
44	IO3	Bidirectional	I/O pin for parallel communication Modulation input in case of direct mode
45	IO4	Bidirectional	I/O pin for parallel communication Slave select in case of serial communication (SPI)
46	IO5	Bidirectional	I/O pin for parallel communication Sub-carrier output in case of direct mode
47	IO6	Bidirectional	I/O pin for parallel communication. MISO in case of serial communication (SPI) Sub-carrier output in case of direct mode
48	IO7	Bidirectional	I/O pin for parallel communication. MOSI in case of serial communication (SPI)
49	CLSYS	Output	Clock output for MCU operation
50	CLK	Input	Clock input for MCU communication (parallel and serial)
51	VDD_IO	Supply Input	Positive supply for peripheral communication, connect to host positive supply

Pin Number	Pin Name	Pin Type	Description
52	CD2	Bidirectional	Internal node de-coupling capacitor
53	CD1	Bidirectional	
54	AGD	Bidirectional	Analog reference voltage
55	VSN_A	Supply Input	Analog part negative supply
56	EXT_IN	Input	RF input in case external VCO is used
57	VSN_CP	Supply Input	Charge pump negative supply
58	ADC	Input	ADC input for external power detector support
59	VDD_A	Supply Output	Analog part positive supply, internally regulated to 3.4V
60	VCO	Input	VCO input
61	VOSC	Bidirectional	Internal node de-coupling capacitor
62	CP	Output	Charge pump output
63	VDDLF	Supply Input	Positive supply for LF processing, internally regulated to 3.4
64	COMP_A	Bidirectional	Internal node, connect de-coupling capacitor to VDD_5LFI
65	EXP_PAD	Supply Input	Exposed paddle, must be tied to GND

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{EXT}, V_{EXT2}	Supply voltage	-0.3	6	V	All voltage values are with respect to substrate ground terminal V_{SS}
	Positive Voltage		V_{EXT} + 0.3	V	For pins EN, I07..IO0, CLK, IRQ, CLSYS, VDDIO, VDD_MIX, VDD_5LFI, VDD_TXPAB, CBV5, DAC, OAD, OAD2
			4.5	V	For other pins
	Negative voltage		-0.3	V	For other pins
I_O	Latchup immunity (1)		±100	mA	According to JEDEC 78
Electrostatic Discharge					
ESD Rating, human body model (2)	Other pins	±2		kV	According to MIL 883 E method 3015
	RF pins	±1			

Symbol	Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions					
T_J	Operating junction temperature		120	°C	The maximum junction temperature for continuous operation is limited by package constraints.
T_{STRG}	Storage temperature range	-55	150	°C	
T_{BODY}	Package body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/ JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is Matte Tin (100% Sn)
RH_{NC}	Relative humidity (non condensing)	5	85	%	
MSL	Moisture sensitivity level	3			Represents a max. floor life time of 168h

Note(s):

1. The AGD (Pin 54) is excluded from Latch-up immunity test at EN (Pin 39) high. AGD is a reference voltage pin and must be kept at the reference voltage level for proper chip operation. AGD must be connected to an external stabilization capacitor.
2. This integrated circuit can be damaged by ESD. We recommend that all integrated circuits are handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet the published specifications. RF integrated circuits are also more susceptible to damage due to use of smaller protection devices on the RF pins, which are needed for low capacitive load on these pins.

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

V_{EXT} = 5.3V, typical values at 25°C, unless otherwise noted.

Note(s): The difference between the external supply and the regulated voltage is higher than 250mV.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VEXT}	Supply current without PA driver current	V_{EXT} Consumption		80		mA
I_{VEXT2}	Supply Current for internal PA	V_{EXT2} Consumption, V_{DD_RF} = 2.5V		140		mA
I_{STBY}	Standby current			3		mA
I_{PD}	Supply current in power-down mode	All system disabled including supply voltage regulators		2	10	µA
V_{AGD}	AGD voltage		1.5	1.6	1.7	V
V_{POR}	Power on reset voltage (POR)		1.4	2.0	2.5	V
V_{VDD}	Regulated supply for internal circuitry and for external MCU		3.2	3.4	3.6	V
V_{DD_RF}	Regulated supply for internal PA		1.9	2	2.1	V
$V_{VDD\ MIX1}$	Regulated supply for mixers, bit vext_low = L	The difference between the external supply and the regulated voltage is higher than 250mV	4.5	4.8	5.1	V
$V_{VDD\ MIX2}$	Regulated supply for mixers, bit vext_low = H		3.5	3.7	3.9	V
P_{PSSR}	Rejection of external supply noise on the supply regulators			26		dB
P_{RFAUX}	Auxiliary output power			0		dBm
P_{RFOUT}	Internal PA output power			20		dBm
R_{RFIN}	RFIN input resistance			100		Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{SENS-NOM}$	Input sensitivity	Nominal mixer setting, PER = 0.1%		-66		dBm
$V_{SENS-GAIN}$		Increased mixer gain, PER = 0.1%		-76		dBm
$V_{SENS-LBT}$	LBT sensitivity	Maximum LBT sensitivity		-86		dBm
$1dB_{CP}$	Input 1dB compression point	Nominal mixer setting		10		dBm
IP3	Third order intercept point			21		dBm
PN200	VCO Phase noise @ 200kHz			-118		dBc/Hz
PN400	VCO Phase noise @ 400kHz			-125		dBc/Hz
T_{REC}	Recovery time after modulation	Maximum LF selected		18		µs
Logic Input/Output						
	Maximum CLK frequency				2	MHz
V_{LOW}	Input logic low				0.2	V_{DD_IO}
V_{HIGH}	Input logic high		0.8			V_{DD_IO}
RIO	Output resistance IO0…IO7	low_io = H for V_{DD_IO} < 2.7V		400	800	Ω
$R_{CL\ SYS}$	Output resistance CL SYS			200		Ω

Figure 7:
Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{EXT}	Positive Supply Voltage		5.0	5.3	5.5	V
		Bit vext_low = 1	4.1		5.5	V
T_J	Operating virtual junction temperature range		-40		110	°C
T_{AMB}	Ambient temperature		-40		110	°C
-	Rth junction to exposed die pad	-		19		°/W

Detailed Description

The RFID reader IC comprises complete analog and digital functionality for reader operation including transmitter and receiver section with complete EPC Gen2 or ISO18000-6C digital protocol support. To integrate as many components as possible, the device also comprises an onboard PLL section with integrated VCO, supply section, DAC and ADC section, and host interface section. In order to cover a wide range of possibilities, there is also Configuration registers section that configures operation of all blocks.

For operation, the device needs to be correctly supplied via. V_{EXT} and V_{EXT2} pins and enabled via. EN pin (Refer Supply for connecting to supply and Power Modes about operation of the EN pin). At power-up, the configuration registers are preset to a default operation mode. The preset values are described in the Configuration Registers Address Space below each register description table. It is possible to access and change registers to choose other options.

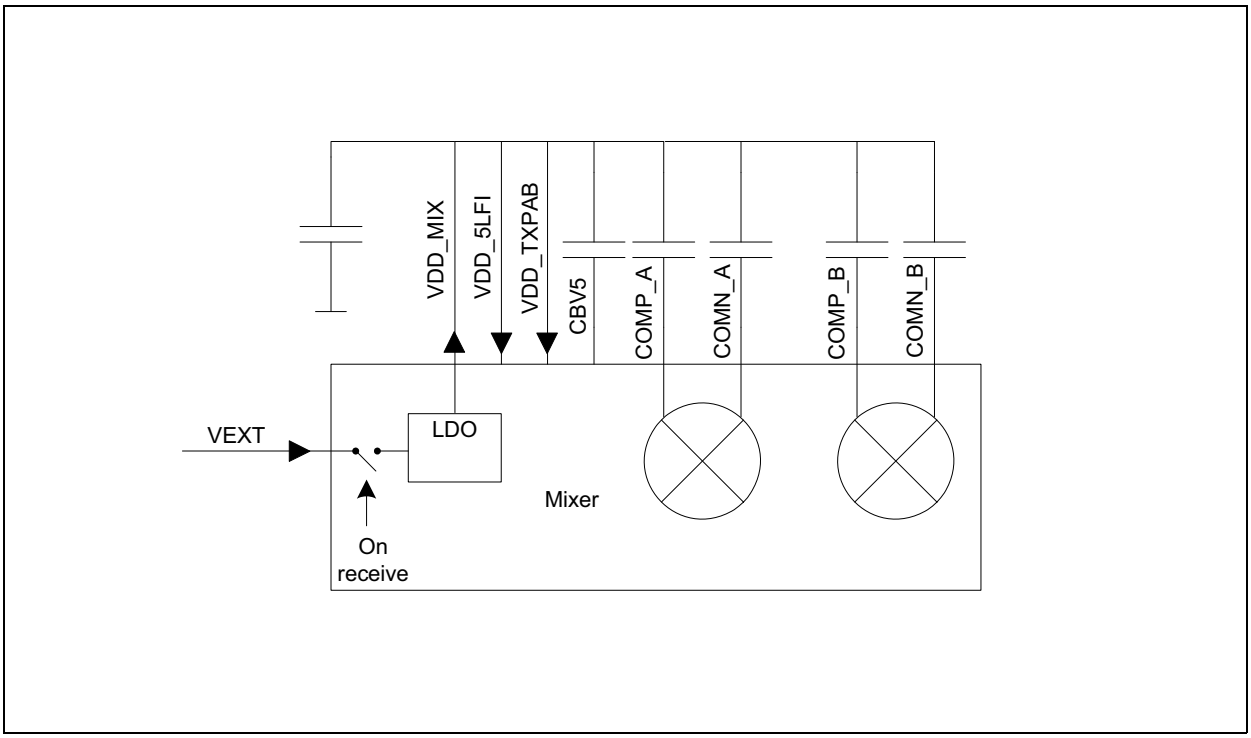
The communication between the reader and the transponder follows the reader talk first method. After power-up and configuring IC, the host system starts communication by turning on the RF field by setting option bit rf_on in the 'Chip status control register' (00) (Figure 26) and transmitting the first protocol command (Select in EPC Gen2). Transmitting and receiving is possible in the following two modes:

1. **Normal Data Mode:** In this mode, the TX and RX data is transferred through the FIFO register and all protocol data processing is done internally.
2. **Direct Data Mode:** In this mode, the data processing is done by the host system.

Supply

The effective supply system of the chip decreases the influence of the supply noise and interference and thus improves de-coupling between different building blocks. A set of 3.4V regulators is used for supplying the reference block, AD and DA converters, low frequency receiver cells, the RF part, and digital part. It is possible to use the digital part supply VDD_D for supplying the external MCU with a current consumption up to 20mA. The input pin for the regulators is V_{EXT}. The output pins for regulators are VDD_A, VDD_LF, VDD_D, VDD_RFP and VDD_B. Each of the pins require stabilizing capacitors to be connected to ground (2.2µF to 10µF and 10nF to 100nF) in parallel. Depending on quality of the capacitors, 100pF could be required.

Figure 8:
Mixer Supply



An additional 4.8V regulator is used for the input RF mixers supply. The input of this regulator is V_{EXT}, output is VDD_MIX pin. For correct operation of the 4.8V regulator, the V_{EXT} voltage needs to be between 5.3V and 5.5V. VDD_MIX needs de-coupling capacitors to VDD_MIX like other VDD pins.

In case lower V_{EXT} supply voltage is used (down to 4.1V), the vext_low option bit needs to be set to optimize the chip performance to the lower supply. The vext_low in the 'TRcal high and misc register' (05) bit decreases VDD_MIX voltage to 3.7V to maintain the regulators PSSR and the ir<1> bit in the 'RX special setting 2' (0A) adapts mixer's internal operating point to lower supply. Adaptation to low supply is implemented in differential mixer only. The consequence of the decreased supply is lower mixer's input range.

VDD_5LFI and VDD_TXPAB pins are supply input pins and should be connected to VDD_MIX. The internal 20dBm power amplifier has an internal regulator from 2…3.5V. The output voltage selection is done by reg2v1:0 option bits in the 'Regulator and IO control register' (0B) (see Figure 37).

The input pin is V_{EXT2} and output is VDD_RF. For optimum noise rejection performance, the input voltage at V_{EXT2} pin needs to be at least 0.5V above the regulated supply output. Connecting V_{EXT2} directly to V_{EXT} is possible only at the expense of increasing IC's power dissipation and decreasing the maximum operating temperature.

A separate I/O supply pin (VDD_IO) is used to supply the internal level shifters for communication interface to the host system (MCU). VDD_IO should be connected to MCU supply to ensure proper communication between the chip and MCU. In case the MCU is supplied by VDD_D from the reader IC also VDD_IO should be connected to VDD_D.

Power Modes

The chip has five power modes.

Power Down Mode

The power down mode is activated by EN pin low (EN = L). For correct operation, the OAD2 pin should not be connected.

Normal Mode

The normal mode is entered by setting EN = H. In this case all supply regulators, reference voltage and bias system, crystal oscillator, RF oscillator and PLL are enabled. After the crystal oscillator stabilizes, the CLSYS clock becomes active (default frequency is 5MHz) and the chip is ready to work with internal registers.

In case the crystal oscillator is used the time that the crystal stabilizes dependent on the crystal used. Typical time is 1.5 - 3ms. By reading the register 0E, the firmware can check the crystal status: register 0E:x1 (osc_ok = 1, pll_ok = 0, rf_ok = 0) shows that crystal oscillator is stable and that device is ready to operate. In case the continuously running TCXO is used, only the OSCO pin DC level needs to be set before the internal clock is ready. The same test with reg0E as above can be used.

The bias and reference voltages after EN = H stabilize in 12ms typically. Then the chip is ready to switch on the RF field and start data transmission.

Standby Mode

The standby mode is entered from normal mode by option bit stby = H. In the standby mode the regulators, reference voltage system, and crystal oscillator are operating in low power mode; but the PLL, transmitter output stages and receiver are switched off. All the register settings are kept while switching between standby and normal mode.

The bias and reference voltages after stby = 0 stabilize in 12ms typically. Then the chip is ready to switch on the RF field and start data transmission.

MCU Support Mode

Power down with MCU support mode intends to support the MCU if the majority of the reader IC is in power down. This mode is enabled by connecting 10kΩ resistor between OAD2 pin and ground. During EN = L period, the VDD_D regulator is enabled in low power mode and the CLSYS frequency is 60kHz typically.

Temporary Normal Mode

It is also possible to trigger temporary normal mode from power down mode (EN = L) by pulling shortly the OAD2 pin low via 10kΩ or less. After the crystal oscillator is stable and the CLSYS clock output is active, the chip waits for approximately 200µs and then changes back to the power down mode. Using this function, the superior system can wake up the reader IC and MCU that are both in the power down mode. If the MCU during 200µs period finds out that the RFID system must react, it confirms the normal mode by setting EN high.

Figure 9:
AS3992 Power Modes

Power Mode	EN	OAD2	Std By
Power down	L	-	X
Power down SYSCLK of 60kHz	L	10k to GND	X
Normal power	H	X	X
Standby		X	H
Listen mode	L	10k and falling edge	X

Host Communication

An 8-bit parallel interface (pins IO0 to IO7) with two control signals (CLK, IRQ) forms the main communication system. It can also be changed (by hardwiring some of the 8 I/O pins) to a serial interface. The data handling is done by a 24 byte FIFO register used in both directions, transmission and reception. For more details, refer Reader Communication Interface.

The signal level for communication between the host system (MCU) is defined by the supply voltage connected to VDD_IO pin. Communication is possible in wide range between 1.8V and 5.5V. In case the pull-up output resistance at VDD_IO below 2.7V is to high, it can be decreased by setting option bit vdd_io_low in the 'TRcal High and Misc register' (05). In case the MCU is supplied from the reader IC, then both the MCU supply and VDD_IO pin need to be connected to VDD_D.

CLSYS output level is defined by the VDD_IO voltage. It is also possible to configure CLSYS to open drain N-MOS output by setting the option bit open_dr in the in the 'TRcal high and misc register' (05), (see Figure 31). This function can be used to decrease amplitude and harmonic content of the CLSYS signal and decrease the cross-talk effects that could corrupt operation of other parts of the circuit.

VCO and PLL

The PLL section is composed of a voltage control oscillator (VCO), prescaler, main and reference divider, phase-frequency detector, charge pump, and loop filter. All building blocks excluding the loop filter are completely integrated. Operating range is 840MHz to 960MHz.

VCO and External RF Source

Instead of the internal PLL signal, an external RF source can be used. The external source needs to be connected to EXT_IN pin and option bit eext_in in the 'PLL A/B divider auxiliary register' (17) (see Figure 52) needs to be set high. The EXT_IN input optimum level is 0dBm with a DC level between 0V and 2V.

It is also possible to use external VCO and internal PLL circuitry. In this case, the output of the external VCO (0dBm) needs to be connected to EXT_IN, option bits eext_in and epresc in the 'PLL A/B divider auxiliary register' (17) both need to be set high. The charge pump output pin CP needs to be connected to the external loop filter input and loop filter output to the external VCO input. This configuration is useful in case the application demands better phase noise performance than the completely integrated oscillator offers.

The internal on-board VCO is completely integrated including the variable capacitor and inductor. The control input is pin VCO; input range is between 0 and 3.3V. The option bits eosc<2:0> in the 'CLSYS, analog out and CP control' (14) (Figure 49) can be used for oscillator noise and current consumption optimization. Option bit lev_vco in the 'PLL A/B divider auxiliary register' (17) (see Figure 52) is used to optimize the internal VCO output level to other RF circuitry demands. VCO and CP pin valid range is between 0.5V and 2.9V.

AS3992 has internal VCO set to a frequency range around 1800MHz, later internally divided by two for decreasing the VCO pulling effect. The tuning curve of 1800MHz VCO is divided into 16 segments to decrease VCO gain and attain lowest possible phase noise.

Configuration of the 1800MHz VCO tuning range can be manual using option bits vco_r<3:0> in the 'CL_SYS, analog out and CP control' register (14) or automatic using L-H transition on option bit auto in the same register. The device allows measurement of the VCO voltage using option bit mvco and reading out the 4 bits result of the automatic segment selection procedure, both in the 'AGL/VCO/F_CAL status' register (10).

PLL

The divide by 32/33 prescaler is controlled by the main divider. The main divider ratio is defined by the 'PLL A/B divider main register' (16). The low ten bits in the three bytes deep register define A value and the next ten bits define B value. The A and B values define the main divider division ratio to N=B*32+A*33. The reference clock is selectable by RefFreq<2:0> bits in the 'PLL R, A/B divider main register' (16) (see Figure 51). The available values are 500kHz, 250kHz, 200kHz, 100kHz, 50kHz and 25kHz.

Charge pump current is selectable between 150µA and 1200µA using option bits cp1:0 in the 'CL_SYS, analog out and CP control register' (14) (see Figure 49). The cp<3> is used to change the polarity (direction) of the charge pump output.

The frequency hopping is supported by direct commands 'Hop to main frequency' (84) and 'Hop to auxiliary frequency' (85). The hopping is controlled by host system (MCU) using two configuration registers for two frequencies. Before enabling the RF field, the host system needs to configure the PLL by writing the 'CL_SYS, analog out and PLL register' (09) and the 'PLL R, A/B divider main' (16) registers. Any time during operating at the first selected frequency, the external system can configure the three bytes deep 'PLL A/B divider auxiliary (17)' register. Hopping to the second frequency is triggered, if direct command 'Hop to auxiliary frequency' is sent. Hop to the third frequency is similar: the register 'PLL A/B divider main (16)' can be written any time the external system has free resources and actual hop is triggered by direct command 'Hop to main frequency'.

Chip Status Control

In the 'Chip status control register' (00) (see Figure 26), main functionality of the chip is defined. By setting the rf_on bit in the 'Chip control register' (00), the transmit and receive part are enabled. The initial RF field ramp-up is defined with the Tari1:0 option bits in the 'Protocol control register' (01) (see Figure 27). It is also possible to slow down the initial RF field ramp by option bits trfon1:0 in the 'Modulator control register' (15) (see Figure 50). The available values are 100µs, 200µs, and 400µs.

The host system can check whether the field ramp-up is finished via the rf_ok bit in the 'AGC and internal status register' (0E) (see Figure 40), which is set high when ramp-up is finished. By setting the rf_on bit low, the field will ramp-down similarly to the ramp-up transient. It is also possible to enable receiver operation by setting rec_on bit. The agc_on and agl_on bits enables the (Automatic Gain Control) AGC and (Automatic Gain Leveling) AGL functionality, dac_on enables DA converter, bit direct enables the direct data mode, and stby bit moves chip to the stand-by power mode.

Protocol Control

In the 'Protocol control register' (01) (see Figure 27), the main protocol parameters are selected (Tari value and RX coding for EPC Gen2 protocol). The Gen2 Protocol is configured by setting Prot<1:0> bits to low. The dir_mode<6> bit defines type of output signals in case the direct mode is used. The rx_crc_n<7> bit high defines reception in case the user does not want to check CRC internally. In this case, the CRC is not checked but is just passed to the FIFO like other data bytes. In the EPC Gen2, this function is useful in case of truncated EPC reply where the 'CRC' transponder transmits is not valid CRC calculated over actual transmitted data.

Option Registers Preset

After power up (EN low to high transition), the option registers are preset to values that allow default reader operation. Default transmission uses Tari 25µs, PW length is 0.5Tari, TX one length is 2 Tari, and RTcal is 133µs. Default reception uses FM0 coding with long preamble, link frequency 160kHz. Default operation is set to internal PLL with internal VCO, differential input mixers, low power output (RFOPX, RFONX), and DSB-ASK transmit modulation.

Transmitter

Transmitter section comprises of protocol processing digital part, shaping, modulator and amplifier circuitry. The RF carrier is modulated with the transmit data and amplified for transmission.

Normal Mode

In normal mode, all signal processing (protocol coding, adding preamble or frame-sync and CRC, signal shaping, and modulation) is done internally.

The external system (MCU) triggers the transmission and loads the transmit data into the FIFO register. The transmission is started by sending the transmit command followed by information on the number of bytes that should be transmitted and the data. The number of bytes needs to be written in the 'TX length' registers and the data to the FIFO register. Both can be done by a single continuous write. The transmission actually starts when the first data byte is written into the FIFO.

The second possibility is to start transmission with one of the direct Gen2 commands (Query, QueryRep, QueryAdjust, ACK, NAK, ReqRN). In this case, the transmission is started after receiving the command.

In case the transmission data length is longer than the size of the FIFO, the host system (MCU) should initially fill the FIFO register with up to 24 bytes. The reader chip starts transmission and sends an interrupt request when only 3 bytes are left in the FIFO. When interrupt is received, the host system needs to read

the 'IRQ status register' (0C) (seeFigure 38). By reading this register, the host system is notified by the cause of the interrupt and the same reading also clears the interrupt. In case the cause of the interrupt is low FIFO level and the host system did not put all data to the FIFO, the remaining data needs to be sent to FIFO, again according to the available FIFO size. In case all transmission data was already sent to the FIFO, the host system waits until the transmission runs out. At the end of the transmit operation, the external system is notified by another interrupt request with a flag in the IRQ register that signals the end of transmission.

The two 'TX length' registers support in-complete bytes transmission. The high two nibbles in register 1D and the nibble composed of bits B4 ~B7 in 'TX length byte 2' (1E) register (see Figure 59) store the number of complete bytes that should be transmitted. Bit B0 (in register 1E) is a flag that signals the presence of additional bits that do not form a complete byte. The number of bits are stored in bits B1~B3 of the same register (1E).

The protocol selection is done by the 'Protocol control register' (01) (see Figure 27). As defined by selected protocol, the reader automatically adds all the special signals like Preamble, Frame-Sync, and CRC bytes. The data is then coded to the modulation pulse level and sent to the modulator. This means that the external system only has to load the FIFO with data and all the micro-coding is done automatically.

The EPC Gen 2 protocol allows some adjustment in transmission parameters. The reader IC supports three Tari values (25µs, 12.5µs, 6.25µs) by changing Tari<1:0> option bits in the 'Protocol control register' (01). PW length and length of the logical one in the transmission protocol can be adjusted by TxPW<1:0> and TxOne<1:0> option bits in the 'TX options' (02) register. Session that should be used in direct commands is defined in the S1and S0 bits in the same register. The back scatter link frequency is defined by TRcal in the Query command transmission. The TRcal is defined by option bits TRcal<11:0> in the 'TRcal registers' (04, 05).

Figure 10:
Register Bits Settings

Protocol Setting	Register Bits	Individual Settings						
TARI	Protocol control<1:0>	6.25µs (00)		12.5µs (01)		25µs		
PW length control	TX option <7:6>	0.27TARI (00)	0.35TARI(01)		0.44TARI(10)		0.5TARI(11)	
Data1 Tx	TX option <5:4>	1.5TARI (00)	1.66TARI(01)		1.83TARI(10)		2TARI(11)	
Coding	Protocol control <4:3>	FMO(00)	M2(01)		M4(10)		M8(11)	
Link frequency	RX option <7:4>	40 kHz (0000)		160 kHz (0110)		256 kHz (1001)	320 kHz (1100)	640 kHz (1111)

The software designer needs to take care that actual TRcal (reg. 04, 05) and RxLF<3:0> (reg. 03) bits and DR bit in the transmission of the Query command are matched. Precise description is in the EPC Gen2 or ISO18000-6C protocol description.

The Transmit section contains a timer. The timer is used to issue a command in a specified time window after a transponder's response. The timer's time is defined in 'TX reply in slot' (06) register. The timer is enabled by using the command 'Delayed transmission without CRC' (92) or 'Delayed transmission with CRC' (93) and is actually started at the end of the reception.

Figure 11:
EPC_gen2 - Tari Combinations

Forward Link	TARI Settings Zero and One Length (RT CAL)			25µs		12.5µs		6.25µs	
				2.5	3	2.5	3	2.5	3
Backscatter Link	LF (kHz)	Division Ratio	TR cal (micro seconds)						
	40	8	200.00	3.2	2.6667				
	160	64/3	133.33	2.1333	1.7778				
	256	64/3	83.33	1.3333	1.1111	2.6667	2.2222		
	320	64/3	66.67			2.1333	1.7778		
	640	64/3	33.33					2.1333	1.7778
	40	8	200.00						
	160	8	50.00			1.6	1.3333		
	256	8	31.25					2	1.6667
	320	8	25.00					1.6	1.3333
	640	8	12.50						
	40	64/3	533.33						
	160	64/3	133.33	2.1333	1.7778				
	256	64/3	83.33	1.3333	1.1111	2.6667	2.2222		
	320	64/3	66.67			2.1333	1.7778		
	640	64/3	33.33					2.1333	1.7778

Direct Mode

Direct mode is applied if the user wants to use analog functions only and bypass the protocol handling supported in the reader IC.

Direct Mode Using Parallel Interface

The reader IC enters the direct mode when option bit 'direct' is set to high in the 'Chip status control register' (00). As the direct mode starts immediately, all the register settings that help to configure the operation of the chip needs to be done prior to entering the direct mode. The 'write' command for direct mode should not be terminated by stop condition since the stop condition terminates the direct mode. This is necessary as direct mode uses four IO pins (IO2, IO3, IO5, IO6) and normal parallel or serial communication is not possible in direct mode. To terminate the direct mode, the user needs to send the stop condition. After stop condition, normal communication via. interface and access to the registers are possible.

Direct Mode Using Serial Interface (SPI)

To enter direct mode via SPI, bit direct should be set to high in the 'Chip status control register' (00) and stop condition (IO4 L-to-H transition) has to be sent. As the direct mode starts immediately, all the register settings that help to configure the operation of the chip needs to be done prior to entering the direct mode. The direct mode persists till writing bit direct to low (IO4 H-to-L, SPI write to reg00). Since the direct mode uses four IO pins (IO2, IO3, IO5, IO6), it is not possible to read registers during the direct mode (IO6 which is MISO in SPI mode is used as direct mode data or subcarrier output). It is possible to write register 00 to terminate the direct mode. After direct mode termination, normal communication via SPI interface and access to the registers are possible.

For more information on transmit modulation input signal possibilities, refer to Modulator.

For more information on the receive output signal possibilities, refer to TX Pre-Distortion.

The digital modulation input in direct mode is IO3. RF field is set to high level if IO3 is high, and to low level if IO3 is low. IO2 is used as RX enable. For correct operation, follow the instructions given below:

1. Configuration registers should be defined, starting from reg01
2. Direct command Enable RX (97) should be sent
3. Bit direct should be written to reg00
4. IO2 should be low during data transmission via IO3
5. IO2 should be changed to high level just before the reception is expected
6. IO3 should be maintained high during reception

Modulator

For the modulation signal source, there are three possibilities:

- Normal data mode – Internally coded and internally shaped.
- Externally coded and internally shaped modulation enabled by entering direct mode. For more information on entering and terminating the direct mode, refer to Direct Mode.
- Externally coded and externally shaped modulation is enabled by setting option bit e_amod in the 'Modulator control register' (15) and entering direct mode. For more information on entering and terminating the direct mode, refer to Direct Mode. In this case, ADC and DAC pins are differential modulator input. The DC level should be 2.2V, amplitude 600mVp. It is also possible to use CD1 and CD2 pins as high and low reference for the external modulation shape circuitry.

The internal modulator is capable of DSB-ASK and PR-ASK modulation. Modulation shape is controlled with a double D/A converter. The first one defines the upper (un-modulated) signal level while the second one generates the modulation transient. The level defined by the first converter is filtered by capacitors on CD1 and CD2 pins to decrease the noise level. The two levels are used as a reference for the shaping circuitry that transforms the digital modulation signal to shaped analog modulation signal. Sinusoidal and linear shapes are available. The output of the shaping circuit is interpolated and connected to the modulator input.

The output level and modulation shape properties are controlled by the 'Modulator control register' (15). The level of the output signal is adjusted by option bits tx_lev<4:0>. Modulation depth for ASK is adjusted by mod_dep<5:0> bits. Valid values for DSB-ASK are 01 to 3F. PR-ASK modulation is selected by pr-ask bit high. In case of PR-ASK, the mod_dep<5:0> bits are used to adjust the delimiter/first zero timing. Linear modulation shape is selected by lin_mod bit. The rate of the modulation transient is automatically adjusted to selected Tari and can be adjusted by ask_rate<1:0> bits. For smoother transition of the modulation signal, an additional low pass filter can be used. The Filter will be enabled by e_lpf bit. The adjustment step is 1.6%, 3F gives 100% ASK modulation depth.

PR-ASK modulation is selected by pr-ask bit high. In case of PR-ASK the mod_dep<5:0> bits are used to adjust the delimiter/first zero timing in a range 9.6µs to 15.9µs. Linear modulation shape is selected by lin_mod bit. The rate of the modulation transient is automatically adjusted to selected Tari and can be adjusted by ask_rate<1:0> bits. For smoother transition of the modulation signal, additional low pas filter can be used by e_lpf bit.

In ASK modulation it is possible to adjust delimiter length by setting option bit ook_ask in the 'Modulator control register' (15). In this case, ook_ask defines 100% ask modulation and the mod_dep<5:0> bits are used for delimiter length setting similar to the PR-ASK mode.

Bits aux_mod and main_mod define whether the modulation signal will be connected to the auxiliary low power output or to the main PA output. In case one of the outputs are enabled by the etxp<3:0> bits and appropriate aux_mod or main_mod bit is low, the output is enabled but not modulated.

Amplifier

The following two outputs are available:

- **Low power high linear output** (~0dBm) can be used for driving an external amplifier. This output uses RFOPX and RFONX pins and it has nominal output impedance of 50Ω. It needs an external RF choke and de-coupling capacitor for operation. It is also possible to use differential output for driving balanced loads. The output is enabled by etx<1:0> bits in the 'Regulator an IO control' (0B) register (see Figure 37). With the help of these bits, it is also possible to adjust current capability of the output.
- **Higher output power output** (~20dBm) can be used for antenna driving in case of short range applications. Internal higher power amplifier is enabled by etx<3:2> bits in the 'Regulator an IO control' (0B) register (see Figure 37). For operation it needs external RF choke and correct impedance matching for operation in 50Ω system. It is also possible to use differential output by setting etx<4>. Bias current in the PA stage can be increased by a factor of two or four using option bits ai2x and ai4x in registers 16 and 17. The differential outputs are RFOUT_1 and RFOUT_2. Single ended output is RFOUT_1. UHF - power amplifiers (PAs) are generally sensitive to parasitics (layout, placement, routing, PCB material etc) and load conditions. We recommend to carefully investigate the specific system implementation on inherent parasitic and load variations to avoid instabilities over production.

TX Pre-Distortion

Transmission signal is modulated with the cosine shaped representation of the digital modulation signal. It is possible to tune the initial shape by writing the correction data in the register 13 and setting option bit use_corr in register 15. Register 13 is 252 bytes deep register accessible in continuous write mode. Bytes on positions 1 to 251 are used for pre-distortion. Byte on position 0 is not used for pre-distortion. The value on position 1 should be set to 0 and the value on position 251 should be set to 250 for smooth continuous transition. The values between positions 1 and 251 form the pre-distortion curve. In case the ramp with values 0 - 250 is written, the initial cosine shape is maintained.

The pre-distortion data can be written and read during use_corr = 0 period.

Receiver

Receiver section comprises two input mixers followed by gain and filtering stages. The two receiving signals are fed to decision circuitry, bit decoder and framer where preamble is removed and CRC is checked. The clean framed data is accessible to the host system (MCU) via. 24 byte FIFO.

Input Mixer

The two input mixer pairs are driven with 90° shifted LO signals and form IQ demodulator circuit. Using IQ architecture, the amplitude modulated input signals are demodulated in the in-phase channel (I) while the phase modulated input signals are demodulated in the quadrature phase (Q) channel. Mixed input modulation is demodulated in both receiving channels. This configuration allows reliable operation regardless the transponders. Modulation presents amplitude or phase modulation at receiver's input and suppresses communication holes that are caused by modulation alternation.

One can use differential input mixer or single ended input mixer. The differential input is formed by pins MIX_INP and MIX_INN. Input should be AC coupled. By default, differential mixers input is chosen. If the inputs are not used, then they should be unconnected.

The mixer with single ended mixers input is selected by s_mix bit in the 'Rx special setting register' (0A). The single ended mixers input is the MIXS_IN pin. Input should be AC coupled. If the input is not used, then it should be unconnected.

To optimize the receiver's noise level and dynamic input range, the mixers have adjustable input range. Depending on expected level of the reflected power the one can adapt mixer performance by internal attenuator or increasing mixer gain. Depending on the reflectivity of the environment or antenna, the receiver's input RF voltage can increase to a level that corrupts mixer operation. In such a case, the input range can be widened by internal input attenuator by setting option bit ir<0>. This is valid for both differential and single ended input mixer.

In case of low reflected power, the host system can increase the differential input mixer's conversion gain and improve the overall sensitivity of the receiver by setting option bit ir<1>. The drawback of this setting is decreased mixer's input dynamic range. The single ended input mixer does not support the gain increase feature. The ir<1:0> bits are in the 'RX special setting' (0A) register.

In case lower supply voltage is used (low_vext=1, refer to Supply), the low_vext option bit adapts mixer's operation point to decreased supply. The consequence of low supply voltage is

up to 1dB decreased performance in terms of sensitivity and input dynamic range. The ir<1:0> bits are in the 'RX special setting2 register' (0A) (see Figure 36).

DRM RX Filter

The analog filtering is composed of four filter stages:

- 4th-order elliptic low-pass with notch characteristic to suppress neighboring channel (500kHz or 600kHz). The filter can be set to have -1dB point at 360kHz and 280kHz for ETSI and FCC channel spacing in DRM operation. It allows one non-DRM setting: 800kHz upper frequency for 640kHz LF.
- 2nd-order high-pass Chebyshev filter with adjustable -1dB from 72kHz to 200kHz. The filter can also be switched off (only gain stage) for lower LF frequencies.
- 2nd-order low-pass Chebyshev filter with -1dB frequencies at 360kHz and 280kHz for European and US channel spacing in DRM operation.
  It allows three non-DRM settings:
  - 800kHz upper frequency for 640kHz LF,
  - 180kHz upper frequency for 160kHz LF and,
  - 72kHz upper frequency for 40kHz LF.
- 2nd-order high-pass Chebyshev filter with adjustable -1dB from 72kHz to 200kHz. The filter can also be reconfigured to 1st-order with -3dB frequency at 5.5kHz or 12kHz for lower LF and FM0 coding.

Filter setting is done via option bits setting in 'RX Filter register' 09. Available bit combinations are:

Figure 12:
640kHz LF– (reg09:00 to reg09:07)

Filter Setting	-3dB High-Pass Frequency	-3dB Low-Pass Frequency	Atten. at 40kHz	Atten. at 1.2MHz
reg09:00	220kHz	770kHz	-55dB	-35dB
reg09:07	80kHz	770kHz	-18dB	-35dB

Figure 13:
320kHz LF – DRM ETSI Range Filter (reg09:20 to reg09:27)

Filter Setting	-3dB High-Pass frequency	-3dB low-Pass frequency	Atten. at 40kHz	Atten. at 600kHz	Atten. at 1.2MHz
reg09:20	200kHz	380kHz	-50dB	-40dB	-54dB
reg09:27	75kHz	380kHz	-18dB	-40dB	-54dB

Figure 14:
250kHz LF – DRM FCC Range Filter (reg09:30 to reg09:37)

Filter Setting	-3dB High-Pass Frequency	-3dB Low-Pass Frequency	Atten. at 40kHz	Atten. at 600kHz	Atten. at 1.2MHz
reg09:30	200kHz	320kHz	-50dB	-45dB	-55dB
reg09:37	75kHz	320kHz	-18dB	-45dB	-55dB

Figure 15:
160kHz – (reg09:3B to reg09:3F)

Filter Setting	-3dB High-Pass Frequency	-3dB Low-Pass Frequency	Atten. at 40kHz	Atten. at 600kHz	Atten. at 1.2MHz
reg09:3B	110kHz	245kHz	NA	-52dB	-56dB
reg09:3F	56kHz	255kHz	NA	-52dB	-56dB

Figure 16:
40kHz LF – (reg09:FF)

Filter Setting	-3dB High-Pass Frequency	-3dB Low-Pass Frequency	Atten. at 40kHz	Atten. at 600kHz	Atten. at 1.2MHz
reg09:FF	7kHz	80kHz	NA	-60dB	-55dB

Following filter settings for different link frequency and RX coding are proposed:

Figure 17:
DRM Modes:

Link Frequency and RX Coding	Proposed reg09 Setting
320kHz, M4, M8	24
250kHz, M4, M8	34

Figure 18:
Other Supported Modes:

Link Frequency and RX Coding	Proposed reg09 Setting
40kHz, FM0, M2, M4, M8	FF
160kHz, FM0	BF
160kHz, M2, M4, M8	3F
640kHz, M4, M8	04

RX Filter Calibration

The calibration procedure implemented in the chip helps to compensate the resistor and capacitor process and temperature variations. Calibration procedure is triggered by 'Trigger RX filter calibration' (88) direct command. Calibration is finished in 5ms maximum. Calibration should be triggered prior to first reception after power down and from time to time, especially in cases wherein significant temperature changes are expected.

The result of calibration is seen in the 'AGL/VCO/F_CAL/PilotFreq status register' (10) in case option bits r10page<2:0> in 'Test setting' register (12) are set to 2. Typical calibration result values are 88.

The calibrated values can be changed automatically by using 'Decrease RX filter calibration data' (89) and 'Increase RX filter calibration data' (8A) direct command, together with f_cal_hp_cgh option bit in 'Test setting' register (12).

Note(s): hp_cal<3:0> affects the high pass part of the filter characteristic and lp_cal<3:0> affects the low pass part of the filter characteristic, both in 4% steps.

Fast AC Coupling

The internal (patent pending) feedback AC coupling system prior to start of transmit modulation stores the DC operating points, and after data transmission progressively adjusts the high pass time constant to allow very fast settling time prior to beginning of reception. Such a system is needed to accommodate the short TX to RX time used at the highest bit rates in the EPC Gen 2 protocol.

It is possible to additionally speed up the first AC coupling time constant by setting option bit lf4_ac_su in the 'Test register' (12).

RX Gain

Gain in the receiving chain can be adjusted to optimize the signal to noise and interference ratio. There are three ways of adjusting: manual adjustment, AGC, and AGL.

- **Manual adjustment** is gain adjustable by setting option bits gain<5:0> in the 'RX special setting 2 register' (0A) (see Figure 36) and 'TRcal high and misc register' (05) (see Figure 31). The low three bits decrease digitizer hysteresis by 3dB (7 steps), the high two bits change the amplifier gain by 3dB (3 steps). Gain<5:4> direction (increase or decrease) is defined by gd<3>.
- **AGC** is automatic gain control. It can be enabled by option bit agc_on in the 'Chip status control' register (00) (see Figure 26). AGC comprises of a system that decreases gain during the first periods of the incoming preamble. Gain is decreased equally for both channels to a level that results the stronger signal is just in the range. In this case, the ratio between I and Q channel amplitude is maintained. The resulted status of the AGC can be seen in the 'AGC and internal status' register (0E) (see Figure 40).
- **AGL** is another possibility for adjusting the gain. AGL bit needs to be set high at the moment when there is no actual transponder response at receiver input. It automatically decreases gain for each channel to the level that is just below the noise and interference level. The gain of the two channels is independent. The resulted status of the AGL for both channels can be seen in the 'AGL status 'register (10) (see Figure 42).

Difference between the AGC and AGL functionality is that AGC is done each time at beginning of the receive telegram; while AGL is done only at the moment when agl_on bit is set high, stored, and is valid till the agl_on bit is set low.

The two receiving signals are digitized and evaluated. The decision circuit selects the in-phase signal or quadrature signal for further processing, whichever presents the better received signal. Which of the signals is chosen can be seen in the in_ select bit in the 'AGC and internal status' register (0E). Bit is valid from preamble end till start of the next transmission.

Received Signal Strength Indicator (RSSI)

The receiver section includes a double RSSI meter. The RSSI meters are connected to the outputs of both receiver chains to measure in real time the peak to peak demodulated voltage of each receiving channel during the reception of each transponder response (from the end of RX wait timer till the end of reception). The peak value of each RSSI meter is stored and presented in the 'RSSI levels' (0F) register (see Figure 41). The RSSI register is valid till start of next transmission.

Reflected RF Level Indicator

The receiver also comprises the input RF level indicator. It is used for diagnostic of circuitry or environment difficulties.

The reflection of poor antenna, reflection of reflective antenna's environment, or directional device leakage (circulator) can cause that input mixers are overdriven with the transmitting signal.

Overloading of the input mixers by reflected transmitting carrier can be notified by the host system (MCU) by measuring the RF input level via internal AD converter. The reflected carrier that is seen on the two mixers input is down converted to zero frequency. The two DC levels on the mixers outputs are proportional to the input RF level and dependant on the input phase and can be used for measuring the level of the reflected carrier. They can be connected to the on-board ADC converter by setting option bits msel<2:0> in the 'Test setting and measurement selection register' (11). The appropriate settings for connecting two mixers' DC levels to AD converter are 001 and 002. Conversion is started by direct command 'Trigger ADC conversion' (87). Result in register 19 is valid 20µs after triggering.

Normal Mode

In the normal mode, the digitized output after decision circuit is connected to the input of the digital portion of the receiver. This input signal is the sub-carrier coded signal, which is a digital representation of modulation signal on the RF carrier.

The digital part of the receiver consists of two sections, which partly overlap. The first section comprises the bit decoders for the various protocols. The bit decoders convert the sub-carrier coded signal to a bit stream and the data's clock according to the protocol defined by option bits Rx-cod<1:0> in the 'Protocol control' (01) register (see Figure 27) and Rx_LF<3:0> option bits in the 'RX options' (03) register. Preamble is truncated. The decoder logic is designed for maximum error tolerance. This enables the decoders to successfully decode even partly corrupted sub-carrier signals due to noise or interference. The receiver also supports transfer of incomplete bytes. The number of valid bits in the last received byte is reported by Bb<2:0> bits in the 'TX length byte 2' (1E) register (see Figure 59).

The second section comprises the framing logic for the protocols supported by the bit decoder section. In the framing section, the serial bit stream data is formatted in bytes. The preamble, FrameSync, and CRC bytes are checked and removed. The result is 'clean' data, which is sent to the 24-byte FIFO register where it can be read out by the host system (MCU).

In the EPC Gen2 protocol, the decoder supports long RX preamble (TRext=1) for FM0, and all Miller coded signals and short RX preamble (Trext=0) for Miller4 and Miller8 coded signals. In the EPC Gen2 protocol, the timing between transponders response and the subsequent reader's command is quite short. To relieve the host system (MCU) of reading RN16 (or handle) out of the FIFO and then writing it back into the FIFO, there is a special register for storing last received RN16 during the Query, QueryRep, QueryAdjust or RegRN commands. The last stored RN16 is automatically used in ACK command.

The start of the receive operation (successfully received preamble) sets the flags in the 'IRQ and status' register. The end of the receive operation is signalled to the host system (MCU) by sending an interrupt request (pin IRQ). If the receive data packet is longer than 8 bytes, an interrupt is sent to the MCU when the 18^{th} byte is received to signal that the data should be removed from the FIFO.

In case an error in data format or in CRC is detected, the external system is made aware of the error by an interrupt request pulse. The nature of the interrupt request pulse is available in the 'IRQ and status register' (0C) (see Figure 38).

The receive part comprises two timers.

- **The RX wait time** timer setting is controlled by the value in the 'RX wait time' (08) (see Figure 34). This timer defines the time after the end of transmit operation in which the receive decoders are not active (held in reset state). This prevents any incorrect detection that could be caused as a result of transients that are caused by transmit operation or transients that are caused by noise or interference. The value of the 'RX wait time register' defines this time with increments of 6.4µs. This register is preset at every write to the 'Protocol control' register (01) according to the minimum tag response time defined by default register definition.
- **The RX no response** timer setting is controlled by the 'RX no response wait time' (07) (see Figure 33). This timer measures the time from the start of slot in the anti-collision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in 'IRQ status control' register. This enables the external controller to be aware of empty slots. The wait time is stored in the register with increments of 25.6µs. This register is automatically preset for every new protocol selection.

'RX length register' (1A, 1B) defines the number of bits that the receiver should receive. The number of bits is taken into account only in case the value is different than 0 00, otherwise receiver stops on pause at the end of reception. Since in noisy environment, the end of transponders transmission is not precisely defined using the RX length registers improves the probability for successful receiving. For direct commands 98 to 9C, the RX length is internally set to 16 to receive RN16. For direct command 9F, the RX length is internally set to 32 to receive RN16 and CRC. For other commands when the host system knows the expected RX length, it is recommended to write it in the RX length register. The only case when RX length is not known in advance is reception of the PC+EPC.

AS3992 handles the issue mentioned above by using special RX mode. The idea is that reader chip generates an additional interrupt after two bytes (PC part of the PC+EPC field) are received. MCU reads out the two bytes that define the length of the on going telegram and writes it in the RX length register.

To use IRQ after the two received bytes, the fifo_dir_irq2 bit in the reg1A should be set and non-zero length (typical PC+EPC length) should be written in the 1B register before start of reception. The fifo_dir_irq2 performs the following changes in the behavior of the logic:

- All received bytes are directly transferred to FIFO. Normally the receiving data is pipelined, causing that the two CRC bytes are not seen in the FIFO. If dir_fifo=1, then all bytes including CRC are seen in the FIFO.
- Additional interrupt is generated after two bytes are received. In the IRQ status register, the 'header/2byte' (B3) bit is set. If the reception is still in progress, IRQ status value is 48. At this moment, the MCU needs to read out the first two bytes (PC part of the PC+EPC field) and set RX length accordingly. The fifo_dir_irq2 bit should be maintained high.
- At the end of reception, another IRQ is generated. Additional IRQ status bit 'Irq_err3 – preamble/end' (B1) is set. IRQ status is 42 if the intermediate 2nd_byte interrupt was read out and cleared, or 4A if the reception was over before the intermediate interrupt was read out and cleared.

Direct Mode

The direct mode is applied in case the user wants to use analog functions only and bypass the protocol handling supported in the reader IC. (Refer to Transmitter for information on entering direct mode.)

Regarding receiving tag data in direct data mode, there are three possibilities depending on setting of option bits:

- Internally decoded bit stream and bit clock according to the protocol defined by option bits Rx-cod<1:0> in the 'Protocol control' (01) register and Rx_LF<3:0> option bits in the 'RX options' (03) register is enabled by low level of option bit dir_mode in the 'Protocol control' (01) register. Outputs are IO5 and IO6.
- Digitized sub-carrier signals of both receiving channels are enabled by high level of option bit dir_mode in the 'Protocol control' (01) register. Outputs are IO5 and IO6.
- Analog sub-carrier signals of both receiving channels are enabled by high level of option bit e_anasupc in the 'CLSYS, analog out, and CP control' (14) register. Outputs are OAD and OAD2.

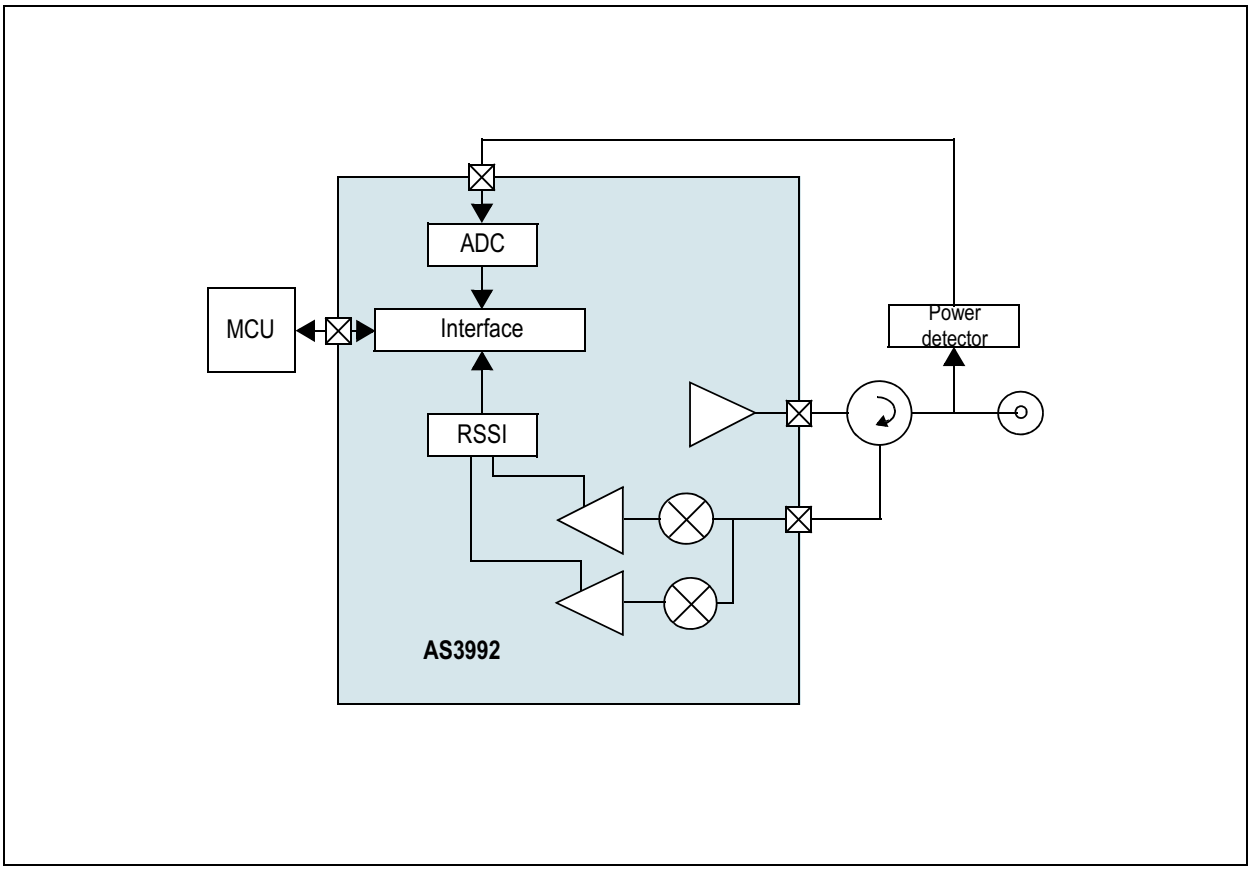
In case MCU support mode is used, the OAD2 resistor to ground (the one that is needed for entering this mode) can be removed during reception not to load the analog OAD2 output. Resistor is necessary only during EN=L, EN L-to-H transition and EN H-to-L transition. It is not necessary during reception.

Normal Mode with Mixer DC Level Output and Enable RX Output Available

One of the possibilities for achieving low reflected TX power is active tuning of the antenna or the directivity device. For correct tuning, the data on the amplitude and phase of the incoming reflected power is available in the output DC level of the two mixers. The two voltages are available on the OAD and OAD2 inputs. For correct operation, the tuning circuitry needs to know when receiver is enabled and the two mixer output DC levels are correct. This signal is available on ADC in case 'Test setting' low register (12l) is set to 1A, or on DAC pin in case 'Test setting' low register (12l) is set to 1B. Tuning can be done on CW and also during telegram reception. In the first case, the receiver is enabled by 'Enable RX' direct command. In the second case, the receiver is automatically enabled after data transmission.

ADC / DAC

Figure 19:
ADC / DAC Section



DA Converter

DA converter intends to support the TX power control function in cases that the external PA supports this function (typically named ramp input or gain control input). The output level is stored in the DAC control register (18) (see Figure 53) and the output pin is DAC. Output range is 0V to two times AGD voltage (3.2V). Input code 00 gives output level equal to AGD. The 7 LSB gives absolute output level and the MSB Bit is the sign. DA converter is enabled by dac_on bit in the 'Chip status control' register (00). Output resistance on DAC pin is 1kΩ typically. For applications that require current, a voltage follower needs to be included.

AD Converter

AD converter intends to support the external power detector placed before or after the circulator to measure actual output power. The analog voltage from the power detector is connected to the ADC pin. AD conversion is triggered by the 'Trigger AD conversion' (87) command, and the resulted value is available in the 'ADC readout register' (19) (see Figure 54). AD converter can also be used for measuring the mixers DC output levels. The source for the conversion is selected by msel<2:0> bits in the 'Test setting 1 and measurement selection' register (11) (see Figure 47). Input range is 0V to two times AGD voltage (3.2V). Input level equal to AGD gives output code 00. The 7 LSB bits give absolute output level, the MSB bit is a sign, H means positive, L means negative value. Result is valid 20µs after triggering. AD converter can be used to measure V_{EXT} voltage, and according to the result, the MCU can decide to use adaptation to low supply voltage (low_vext=1 and ir<1>=1 option bits) or inform the superior system that supply needs to be fixed or just disable transmission. The value in 'ADC readout register' (19) is calculated accordingly to the equation:

(EQ1) *ADCreg = [(VEXT-1.6)*0.8-1.6] / 0.0126*

Where:

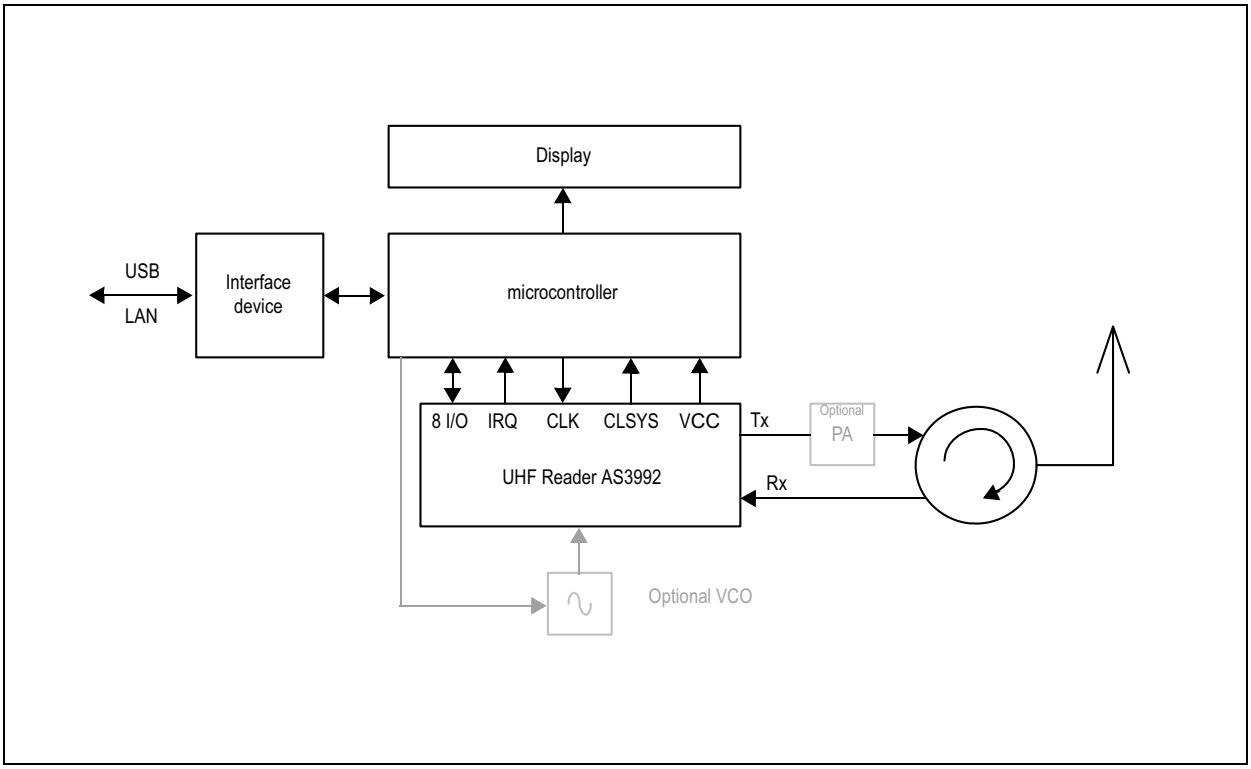
ADCreg is the value, sign should be considered as above V_{EXT} is in Volts.

Reference Oscillator

Reference frequency of 20MHz is needed for the chip. It is possible to use quartz crystal or external reference source (TCXO). In case the crystal is used it should be connected between OSCI and OSCO pin with appropriate load capacitors between each oscillating pin and ground. Load capacitance 15-20pF is proposed. Maximum series resistance in resonance is 30Ω. In case external reference source is used, it should be connected to OSCO pin. The signal should be sinusoidal shape, 1Vpp, DC level 1.6V or AC coupled.

Application Information

Figure 20:
Application Example



Configuration Registers Address Space

At power up, the configuration registers are preset to a value that allows default operation. The preset values are given after each register description table.

Figure 21:
Main Control Registers

Adr (hex)	Register		Length
00	Chip status control	R/W	1
01	Protocol control	R/W	1

Figure 22:
Protocol Sub-Setting Registers

Adr (hex)	Register		Length
02	TX options Gen2	R/W	1
03	RX options Gen2	R/W	1
04	TRcal L register Gen2	R/W	1
05	TRcal H and misc	R/W	1
06	TX reply in slot	R/W	1
07	RX no response wait	R/W	1
08	RX wait time	R/W	1
09	RX filter	R/W	1
0A	RX special setting2	R/W	1
0B	Regulator and IO control	R/W	1
13	TX pre-distortion (deep register)	R/W	
14	CL_SYS, analog out, and CP	R/W	3
15	Modulator control (3 bytes deep)	R/W	3
16	PLL main (3 bytes deep)	R/W	3
17	PLL auxiliary (3 bytes deep)	R/W	3
18	DAC register	R/W	1
19	ADC register	R	1

Figure 23:
Status Registers

Adr (hex)	Register		Length
0C	IRQ and status	R	1
0D	Interrupt mask register	R/W	1
0E	AGC and internal status register	R	1
0F	RSSI levels	R	1
10	AGL / VCO / F_CAL / PilotFreq status register	R	1

Figure 24:
Test Registers

Adr (hex)	Register		Length
11	Measurement selection	R/W	1
12	Test setting	R/W	1

Figure 25:
FIFO Registers

Adr (hex)	Register		Length
1A	RX length	R/W	1
1B	RX length	R/W	1
1C	FIFO status	R	1
1D	TX length byte1	R/W	1
1E	TX length byte2	R for RX W for TX	1
1F	FIFO I/O register	R/W	1

Main Configuration Registers

Chip Status Control (00) – Controls of the operation mode

Figure 26:
Chip Status Control (00) (1)

Bit	Signal Name	Function	Comments
B7	stby	Stand-by power mode	0: normal mode 1: stby power mode
B6	direct	Direct data mode	External modulation control for transmission and IQ or bit stream output for reception
B5	dac_on	DA converter enable	0: DAC OFF 1: DAC ON
B4			
B3	agl_on	AGL mode enable	0: AGL OFF 1: AGL ON
B2	agc_on	AGC select	0: AGL OFF 1: AGL ON
B1	rec_on	Receiver enable	Receiver is enabled
B0	rf_on	TX and RX enable	TX RF field and receiver are enabled

Note(s):
1. Reset to 00 at EN=L or POR=H

Protocol Control (01) – Controls the RFID protocol selection, operation of Tari10 bits is defined with Prot10 bits.

Figure 27:
Protocol Control (01) [1]

Bit	Signal Name	Function	Comments
B7	rx_crc_n	Receiving without CRC	0: RX CRC (generate interrupt) 1: No RX CRC (interrupt and no CRC truncation)
B6	dir_mode	Direct mode type	0: Output is bit stream and clock from the selected decoder 1: Output is sub-carrier data.
B5	Prot1	Protocol selection	00: EPC Gen2 / ISO18000-6C: Tari 6.26/12.5/25us, FM0, M2, M4, M8 01: 10: ISO18000-6A/B:, A/B FM0 decoder in direct mode
B4	Prot2		
B3	RX_cod1	RX decoding select (Gen2)	00: FM0 01: Miller 2 10: Miller 4 11: Miller 8
B2	RX_cod0		
B1	Tari1	Tari (Gen2)	00: Tari=6.25µs (Gen2, ISO-C) 01: Tari=12.5µs (Gen2, ISO-C) 10: Tari=25µs (Gen2, ISO-C)
B0	Tari0		

Note(s):

1. Preset to 06 (Gen2, Miller2, Tari = 25µs) at EN = L or POR = H

Control Registers - Low Level Configuration Registers

TX Options (02) – Gen2

Figure 28:
TX Options (02) [1]

Bit	Signal Name	Function	Comments
B7	TxPw1	PW length control	00: 0.27Tari 01: 0.35Tari 10: 0.44Tari 11: 0.50Tari
B6	TxPw0		
B5	TxOne1	TX one length control	00: 1.50Tari 01: 1.66Tari 10: 1.83Tari 11: 2.00Tari
B4	TxOne0		
B3	Tx-CRC	TX CRC type	0: CRC-16 1: CRC-5
B2	Force_TRcal	TRcal period in normal transmission	Normally TRcal is automatically transmitted when Query (98) direct command is issued, according to EPC Gen2 and ISO18000-6C. In case Force_TRcal=1 the TRcal period is transmitted also in normal data transmission (direct commands 90, 91)
B1	S1	Session bits	Used for Gen 2 direct commands
B0	S0		

Note(s):

1. Preset at POR=H or EN=L
   Gen2: F0 (TxPW=0.5 Tari, TxOne=2 Tari)

RX Options (03) - Gen 2

Figure 29:
RX Options (03) (1)

Bit	Signal Name	Function	Comments
B7	Rx_LF3	Link frequency selection	0000: 40kHz 0110: 160kHz 1001: 256kHz 1100: 320kHz 1111: 640kHz
B6	Rx_LF2		
B5	Rx_LF1		
B4	Rx_LF0		
B3	pil_meas_sh<1:0>	Shorter pilot measurement	Shorten pilot measurement interval to 1/2, 1/4, 1/8. Available intervals are 80, 40, 20, 10, 5 LF periods.
B2			
B1	TRext	RX preamble length	0: Short preamble 1: Long preamble Short preamble is supported for Miller 4 and Miller 8 coding.
B0		don't care	Set to 0

Note(s):

1. Preset at POR = H or EN = L
   Gen2: 60 (160kHz)

TRcal Low Register (04) – Gen2

Figure 30:
TRcal Low Register (04) (1)

Bit	Signal Name	Function	Comments
B7	TRcal7		Gen2: 17.2µs…225µs
B6	TRcal6		
B5	TRcal5		
B4	TRcal4		
B3	TRcal3		
B2	TRcal2		
B1	TRcal1		TRcal range 0.1µs…409µs (1…4096 steps) step size 0.1µs worst case relative resolution (0.1µs/ 17.2µs=0.6%)
B0	TRcal0		

Note(s):

1. Preset at POR = H or EN = L
   Gen2: 35 (1333 steps: 133.3µs, DR = 64/3(bit DR = 1) => LF = 160µs)

TRcal High and Miscellaneous Register (05) – Gen 2

Figure 31:
TRcal High and Miscellaneous Register (05) (1)

Bit	Signal Name	Function	Comments
B7	gain<3>	RX gain direction	0: Decrease 1: Increase gain by option bits gain<5:4> in reg0A
B6	vext_low	Decrease VDD_MIX	0: 4.8V 1: 3.7V, also differential mixer adaptation to low supply
B5	vdd_io_low	Supports low peripheral communication voltage	When high decreases output resistance of logic outputs. Should be set high when VDD_IO voltage is below 2.7V.
B4	open_dr	Open drain N-MOS outputs	Valid for CLSYS, OAD, OAD2 pins
B3	TRcal11		(see Figure 30)
B2	TRcal10		
B1	TRcal9		
B0	TRcal8		

Note(s):

1. Preset at POR = H or EN = L
   Gen2: 05

Delayed Transmission Wait Time (06)

Figure 32:
Delayed Transmission Wait Time (06) (1)

Bit	Signal Name	Function	Comments
B7	Txdel7	Delayed transmission wait time	TX reply range 6.4µs to 1632µs (1…255), Start at end of RX. 00: Delayed transmission is disabled. Gen2: T2 = 4.68µs…500µs after end of RX, Select T4>31.2…150µs after end of TX
B6	Txdel6		
B5	Txdel5		
B4	Txdel4		
B3	Txdel3		
B2	Txdel2		
B1	Txdel1		
B0	Txdel0		

Note(s):

1. Preset at POR = H or EN = L
   Gen2: 00

RX No Response Wait Time (07) – Defines the time when 'No Response' interrupt is sent.

Figure 33:
RX No Response Wait Time (07) (1)

Bit	Signal Name	Function	Comments
B7	NoResp7	No response wait time	Defines the time when 'no response' interrupt is sent. It starts from the end of TX. RX no response wait range is 25.6µs to 6528µs (1…255), Step size 25.6µs Interrupt is sent in case the time runs out before 6-10 periods of link frequency is detected. Gen2: T1max=23.6µs…262µs
B6	NoResp6		
B5	NoResp5		
B4	NoResp4		
B3	NoResp3		
B2	NoResp2		
B1	NoResp1		
B0	NoResp0		

Note(s):

1. Preset at POR = H or EN = L
   Gen2: 07 (179.2µs > 54.25µs…84.5µs + 10 periods – LF:160kHz)

RX Wait Time (08) – Defines the time after TX when the RX input is disregarded.

Figure 34:
RX Wait Time (08) (1)

Bit	Signal Name	Function	Comments
B7	Rxw7	RX wait time	Defines the time during which the RX input is ignored. It starts from the end of TX. RX wait range is 6.4µs to 1632µs (1…255), Step size 6.4µs, 00: receiver enabled immediately after TX. ISO 1800-6C(Gen2) Gen2: T1min=11.28µs…262us, ISO 1800 - 6A: 150…1150µs ISO 1800 - 6B: 85…460µs
B6	Rxw6		
B5	Rxw5		
B4	Rxw4		
B3	Rxw3		
B2	Rxw2		
B1	Rxw1		
B0	Rxw0		

Note(s):

1. Preset at POR = H or EN = L
   Gen2: 07(44.8µs < 54.25µs…84.5µs – LF:160kHz)

RX Filter (09)

Figure 35:
RX Filter (09) (1)

Bit	Signal Name	Function	Comments
B7	byp160	Bypass for 160kHz LF	See DRM RX Filter
B6	byp40	Bypass for 40kHz LF	
B5	lp3	Low pass setting	
B4	lp2		
B3	lp1		
B2	hp3	High pass setting	
B1	hp2		
B0	hp1		

Note(s):

1. Preset at POR = H or EN = L
   Gen 2:41

RX Special Setting2 (0A)

Figure 36:
RX Special Setting2 (0A) [(1)]

Bit	Signal Name	Function	Comments
B7	gain<5>	RX gain setting	Gain change, 3 steps by 3dB, Increase/decrease defined by gain<3> option bit in reg05
B6	gain<4>		
B5	gain<2>	Digitizer hysteresis setting	Hysteresis increase, 7 steps by 3dB
B4	gain<1>		
B3	gain<0>		
B2	s_mix	Mixer input selection	0: differential input mixer 1: single ended input mixer
B1	ir<1>	Differential mixer gain increase	10dB gain increase
B0	ir<0>	Mixer input attenuation	8dB attenuation using differential mixer, 5dB attenuation using single ended input mixer

Note(s):

1. Preset to 01 (Max gain, mixer range) at POR = H or EN = L

Regulator and I/O Control (0B)

Figure 37:
Regulator and I/O Control (0B) (1)

Bit	Signal Name	Function	Comments
B7	reg	for VDD_RF current source	
B6	reg2v<1>	Internal power amplifier regulator setting	00: 2V 01: 2.5V 10: 3V 11: 3.5V
B5	reg2v<0>		
B4	etx<4>	PA2 enable	0: RFOUT1 only 1: differential RFOUT1 and RFOUT2
B3	etx<3>	Enable for main PA and current for main PA pre-driver	00: disabled 01:7mA 10: 14mA 11: 22mA
B2	etx<2>		
B1	etx<1>	Enable for low power output and current for auxiliary driver low power output	00: disabled 01:7mA 10: 14mA 11: 22mA
B0	etx<0>		

Note(s):

1. Preset to 02 (Medium driver current) at POR = H or EN = L

Status Registers

IRQ and Status Register (0C) displays the cause of IRQ and TX / RX status.

Figure 38:
IRQ and Status Register (0C) (1)

Bit	Signal Name	Function	Comments
B7	Irq_tx	IRQ set due to end of TX	Signals the TX is in progress. Interrupt when TX is finished.
B6	Irg_srx	IRQ set due to RX start	Signals the RX was received and RX is in progress. Interrupt when RX is finished.
B5	Irq_fifo	Signals the FIFO is 3/4<FIFO <1/4	Signals FIFO high or low (less than 6 or more than 18)
B4	Irq_err1	CRC error	Reception CRC
B3	Irq_header / Irq_2nd_byte	Header bit / 2 bytes	Received header bit is high / Two bytes already in FIFO – in case fifo_dir_irq2=1(reg1A)
B2	Irq_err2	RX count error	Signals to MCU that reception was shorter than expected (see RX length (1A, 1B) register definition)
B1	Irq_err3 / Irq_RX_finished	Preamble detect error / RX finished	Signals to MCU that there was an error during preamble detection / Rx is finished – in case fifo_dir_ irq2=1(reg1A)
B0	Irq_noresp	No response interrupt	Signals to MCU that next slot command can be sent.

Note(s):

1. Preset to 00 at POR = H or EN = L. It is automatically reset at the end of read phase. The reset also removes the IRQ flag.

Interrupt Mask Register (0D)

Figure 39:
Interrupt Mask Register (0D) [1]

Bit	Signal Name	Function	Comments
B7		IRQ enabled by default	
B6			
B5	e_irq_fifo	When enabled, AS3992 will generate an active high Interrupt when the FIFO is getting low (6 Bytes left to send on transmit operation) or is getting full over 18 bytes on receive operation.	
B4	e_irq_err1	When enabled, AS3992 will generate an active high Interrupt when the device detects an CRC error (This option will report no crc error when receive without crc is enabled).	
B3	e_irq_header	When enabled, AS3992 will generate an active high Interrupt when the device detects an error into the header Bit of the Tag reception.	
B2	e_irq_err2	When enabled, AS3992 will generate an active high Interrupt when the length of the received Bit stream from the Tag has been shorter than expected in the RX length configuration. Such event occurs, for example, if the Tag is not powered sufficiently.	
B1	e_irq_err3	When enabled, AS3992 will generate an active high Interrupt in case the device detects an error during preamble reception.	
B0	e_irq_noresp	When enabled, AS3992 will generate an active high Interrupt in case no Tag has been answered.	

Note(s):

1. Preset to 37 at POR = H and EN = L

AGC and Internal Status Register (0E)

Figure 40:
AGC and Internal Status Register (0E)

Bit	Signal Name	Function	Comments
B7	rfu	AGC status	7 steps, 3dB per step
B6	agc<2>		
B5	agc<1>		
B4	agc<0>		
B3	in_select	Shows the source of the subcarrier signal that is used for decoding.	0: REC_A 1: REC_B Value is valid from reception start till start of next transmission
B2	rf_ok	RF level stable	
B1	pll_ok	PLL locked	
B0	osc_ok	Crystal oscillator stable	

RSSI Levels Register (0F) – Displays the signal strength on both reception channels.

Figure 41:
RSSI Levels Register (0F) (1)

Bit	Signal Name	Function	Comments
B7	rssi<7>	RSSI value of Q channel (REC_B)	(16 steps, 2dB per step)
B6	rssi<6>		
B5	rssi<5>		
B4	rssi<4>		
B3	rssi<3>	RSSI value of I channel (REC_A)	(16 steps, 2dB per step)
B2	rssi<2>		
B1	rssi<1>		
B0	rssi<0>		

Note(s):

1. The RSSI values are valid from the start of reception till start of next transmission.

AGL / VCO / F_CAL / PilotFreq Status Register (10) – in case **r10page<1:0>=00** (reg12) displays the status of the AGL.

Figure 42:
AGL / VCO / F_CAL / PilotFreq Status Register (10)

Bit	Signal Name	Function	Comments
B7			
B6			
B5	agl<5>	AGL status - REC_A	7 steps, 3dB per step
B4	agl<4>		
B3	agl<3>		
B2	agl<2>	AGL status - REC_B	7 steps, 3dB per step
B1	agl<1>		
B0	agl<0>		

AGL / VCO / F_CAL / PilotFreq Status Register (10) – in case **r10page<1:0>=01** (reg12) displays the status of the internal VCO.

Figure 43:
AGL / VCO / F_CAL / PilotFreq Status Register (10)

Bit	Signal Name	Function	Comments
B7	vco_ri<7>	VCO automatic range select result	16 steps
B6	vco_ri<6>		
B5	vco_ri<5>		
B4	vco_ri<4>		
B3	vco_ri<3>	Internal VCO type	0: 900 MHz VCO 1: 1800 MHz VCO
B2	vco_ri<2>	VCO pin voltage measurement	7 steps, step size 0.4V
B1	vco_ri<1>		
B0	vco_ri<0>		

AGL / VCO / F_CAL / PilotFreq Status Register (10) – in case **r10page<2:0>=2** (reg12) displays the result of RX filter calibration.

Figure 44:
AGL / VCO / F_CAL / PilotFreq Status Register (10)

Bit	Signal Name	Function	Comments
B7	hp_cal<3:0>	High pass calibration data	16 steps, step size 4%
B6			
B5			
B4			
B3	lp_cal<3:0>	Low pass calibration data	16 steps, step size 4%
B2			
B1			
B0			

AGL / VCO / F_CAL / PilotFreq Status Register (10) – in case **r10page<2:0>=3** (reg12) displays the result of RX filter calibration.

Figure 45:
AGL / VCO / F_CAL / PilotFreq Status Register (10)

Bit	Signal Name	Function	Comments
B7	pilot_freq<7:0>	RX pilot frequency measurement result	Typical value 160
B6			
B5			
B4			
B3			
B2			
B1			
B0			

Version Register (13)

30: AS3990

38: AS3991

51: AS3992

Test Registers

Measurement Selection (11)

Figure 46:
Measurement Selection (11) (1)

Bit	Signal Name	Function	Comments
B7			
B6			
B5			
B4			
B3	msel<3>	rfu	
B2	msel<2>	ADC measurement selection	000: None 011: ADC pin 001: Rec. A mixer DC 100: Internal RF level 111: V_{EXT} level
B1	msel<1>		
B0	msel<0>		

Note(s):

1. Default: Reset to 00 at POR = H and EN = L

Test Setting (12) – (Three bytes deep)

Sets special connections for test or direct chip use. Should be low for normal operation.

Figure 47:
Test Setting (12) (1)

Bit	Signal Name	Function	Comments
23:17		rfu	Reserved for future use; set 0 for correct device operation.
16	r10page<2>	Page reg10 selection extension	0: agl<5:0> 1: vco_r<7:0> 2: hplp_cal<7:0> 3: pilot_freq
15:14	r10page<1:0>	Page reg10 selection	00: agl 01: VCO range presented in reg10
13:0		rfu	Reserved for future use; set 0 for correct device operation.

Note(s):

1. Default: Reset to 00 at POR = H and EN = L

TX Pre-Distortion (13), Deep register

Figure 48:
TX Pre-Distortion (13) [(1)]

Bit	Signal Name	Function	Comments
251:1byte	ramdat	Pre-distortion shape	Should be written in one continuous write, including byte 0, byte1=0, byte 251=250, write at use_corr=0 (reg15).
0 byte	reg13_0	rfu	First byte in register 13.

Note(s):

1. Default: First byte preset to 30/35/37/38/50/51 at POR = H and EN = L. Others bytes not cleared.

PLL, Modulator, DAC, and ADC Registers

CL_SYS, Analog Out and CP Control (14) – (Three bytes deep)

Figure 49:
CL_SYS, Analog Out and CP Control (14) [(1)]

Bit	Signal Name	Function	Comments
23:22	xosc<1:0>	Crystal oscillator adaptation	00 – normal operation with auto power saving mode 01 – External sinus TCXO AC coupled to OSCO 10 – Disable auto power saving mode
21	rfu	rfu	
20	rfu	rfu	cp<4> – disable ½ cp out – test, should be low for normal operation
19:16	vco_r	Manual VCO range selection	Manual selection of the VCO range segment. Used in case auto = 0
15	auto	Automatic VCO range enable	L-H transition triggers the automatic selection of the VCO range segment
14	h2	Auto range selection speed-up	
13	h6	Auto range selection speed-up	
12	ozko	Auto range selection mode	
11	mvco	VCO measurement enable	7 steps, result in reg10
10:9	eosc<2:1>	Internal oscillator bias current	00: min. bias current (~1.3mA) 11: max. bias current (~5mA)

Bit	Signal Name	Function	Comments
8	clsys2	CLSYS output frequency	000: Off 001: 5MHz 010: 10MHz 011: 20MHz 100: 4MHz
7	clsys1		
6	clsys0		
5	e_anamix	Analog mixer DC output on OAD/OAD2	
4	e_anasubc	Analog sub-carrier out on OAD/OAD2	
3	cp<3>	VCO frequency dependence	0: increasing with VCO voltage 1: decreasing with VCO voltage
2:0	cp<2:0>	Charge pump current	000: 150µA 001: 300µA 010: 600µA 011: 1200µA 100: 1350µA 101: 1500µA 110: 1800µA 111: 2350µA

Note(s):

1. Preset at POR = H or EN = L
   Default setting: 00 04 40 (Medium VCO bias, CLSYS: 5MHz, min. CP current)

Modulator Control Register (15) – (Three bytes deep)

Figure 50:
Modulator Control Register (15) [(1)]

Bit	Signal Name	Function	Comments
23	e_amod	Analog modulation	0: IO3 is digital modulation input in direct mode. 1: ADC is analog mod. input in direct mode (allowed when ADC not used).
22	main_mod	Modulation connected to main TX	
21	aux_mod	Modulation connected to aux. TX	
20	tpreset	Test bit	Should be low for normal operation
19	use_corr	TX pre-distortion enable	
18	e_lpf	Enable low pass filter	
17:16	ask-rate<1:0>	ASK Modulation transient rate	00: Tari determined 01: Skip 2 10: Skip 4 11: Skip 8
15	lin_mod	Selects linear modulation transient	Default is shaped modulation transient for ASK and PR-ASK modulation.
14	pr-ask	PR-ASK enable	In case Tari is 25µs, the ook_ask bit defines delimiter transient in PRASK modulation mode: ook_ask=1 forces ASK shaped transient, ook_ask=0 forces PRASK shaped transient. In case Tari is 12.5µs or 6.25µs, the ASK delimiter transient is used regardless ook_ask bit value. ASK shaped delimiter transient offers correct and adjustable delimiter length. The TX spectrum is not affected to a visible level due to ASK delimiter transient. Other field transitions are done in PRASK mode.
13:8	mod_dep<5:0>	ASK modulation depth/ PR delimiter adjust	In case pr_ask=0 and ook_ask=0: 00…3E: ASK modulation depth, 3F: 100% in case pr_ask=1 or ook_ask=1: Adjust delimiter length, range 9.6µs to 15.9µs, step 0.1µs. 1D=12.5µs
7:6	trfon<1:0>	RF on/off transition time	00: Tari determined 01: 100µs 10: 200µs 11: 400µs

Bit	Signal Name	Function	Comments
5	ook_ask	100% ASK enable with variable delimiter length	Enforces 100% ASK modulation depth, bits <13:8> are used to adjust the delimiter length
4:3	tx_lev<4:3>	TX output level coarse adjustment	00: 0dB, nominal 10: -12dB 01: -6dB
2:0	tx_lev<2:0>	TX output level fine adjustment	0: nominal, decrease: 1…7: -1dB...-7dB, step 1dB

Note(s):

1. Preset at POR = H and EN = L
   Default: set to 20 3F 00 (aux. modulation, ASK, level nominal)

PLL R, A/B Divider Main Register (16) – (three bytes deep)

Figure 51:
PLL R, A/B Divider Main Register (16) (1)

Bit	Signal Name	Function	Comments
23	ai2x	Increase internal PA bias	Increase two times
22:20	RefFreq<2:0>	PLL reference divider	000: 500kHz 001: 250kHz 100: 200kHz 010: 125kHz 101: 100kHz 110: 50kHz 111: 25kHz
19:10	B value	PLL main divider	Prescaler 32/33, dividing ratio N=B*32+A*33, proposed A/B ratio: 1/3...3
9:0	A value		

Note(s):

1. Preset at POR = H and EN = L
   Default: set to 40 D8 4F (R: 200kHz, N: 4335: 54*32+79*33 =>867MHz)

PLL A/B Divider Auxiliary Register (17) – (Three bytes deep)

Figure 52:
PLL A/B Divider Auxiliary Register (17) (1)

Bit	Signal Name	Function	Comments
23	ai4x	Increase internal PA bias	Increase four times
22	lev_vco	VCO signal adjustment	0: normal VCO connection 1: direct VCO connection
21	eext_in	Enable external RF input EXT_IN	0: Internal VCO 1: External RF source is used.
20	epresc	Enable divider and prescaler	1: In case internal PLL drives external VCO
19:10	B value	PLL main divider	Prescaler 32/33, dividing ratio N=B*32+A*33, proposed A/B ratio: 1/3...3
9:0	A value		

Note(s):

1. Preset at POR = H and EN = L
   Default: set to 01 18 46 (R: 200kHz, N: 4550: 70*32+70*33 =>910MHz)

DAC Control Register (18)

Figure 53:
DAC Control Register (18) (1)

Bit	Signal Name	Function	Comments
B7	dac<7>	DAC control value	
B6	dac<6>		
B5	dac<5>		
B4	dac<4>		
B3	dac<3>		
B2	dac<2>		
B1	dac<1>		
B0	dac<0>		

Note(s):

1. Default: reset to 00 at POR = H and EN = L

ADC Readout Register (19)

Figure 54:
ADC Readout Register (19)

Bit	Signal Name	Function	Comments
B7	adc<7>	ADC readout	Via ADC the two mixers output DC levels can be measured showing the reflectivity of the antenna or the environment. Also DC level on ADC pin can be measured. The later case can be used for checking the RF output power via external power detector. The measurement is selected using msel<2:0> bits. The measurement is triggered by the 'Trigger ADC conversion' command (87). Result is valid 20µs after triggering.
B6	adc<6>		
B5	adc<5>		
B4	adc<4>		
B3	adc<3>		
B2	adc<2>		
B1	adc<1>		
B0	adc<0>		

RX Length Registers

RX Length 1 (1A)

Figure 55:
RX Length 1 (1A) (1)

Bit	Signal Name	Function	Comments
B7	rx_crc_n2	Receiving without CRC	Temporary receiving without CRC. Valid for a single reception.
B6	fifo_dir_irq2	Direct FIFO and 2nd byte IRQ	All bytes including CRC are transferred to FIFO, irq_header is changed to irq_2ndbyte, irq_err3 is changed to irq_RX_finished. For PC+EPC reception
B5			
B4			
B3			
B2			
B1	rxl<9>	RX length	
B0	rxl<8>		

Note(s):

1. Default: reset to 00 at POR = H, EN = L, at the end of reception.

RX Length 2 (1B)

Figure 56:
RX Length 2 (1B) (1)

Bit	Signal Name	Function	Comments
B7	rxl<7>	RX length	
B6	rxl<6>		
B5	rxl<5>		
B4	rxl<4>		
B3	rxl<3>		
B2	rxl<2>		
B1	rxl<1>		
B0	rxl<0>		

Note(s):

1. Default: reset to 00 at POR = H, EN = L, at the end of reception.

FIFO Control Registers

FIFO Status – adr 1C hex number of received bytes and FIFO flags.

Figure 57:
FIFO Status – adr 1C hex (1)

Bit	Signal Name	Function	Comments
B7	Fhil	High FIFO level	Indicates that 18 bytes are in FIFO already (for RX)
B6	Flol	Low FIFO level	Indicates that only 6 bytes are left in FIFO (for TX)
B5	Fove	FIFO overflow error	Several data is written to FIFO
B4	Fb4	FIFO bytes fb[4]	How many bytes loaded in FIFO were not read out yet
B3	Fb3	FIFO bytes fb[3]	
B2	Fb2	FIFO bytes fb[2]	
B1	Fb1	FIFO bytes fb[1]	
B0	Fb0	FIFO bytes fb[0]	

Note(s):

1. Default: reset to 00 at POR = H and EN = L

TX Length Byte1 – adr 1D hex high 2 nibbles of complete bytes, which will be transferred through FIFO.

Figure 58:
TX Length Byte1 - adr 1D hex (1)

Bit	Signal Name	Function	Comments
B7	Txl11	Number of complete byte– bn[11]	High nibble of complete bytes to be transmitted or received.
B6	Txl10	Number of complete byte– bn[10]	
B5	Txl9	Number of complete byte– bn[9]	
B4	Txl8	Number of complete byte– bn[8]	
B3	Txl7	Number of complete byte– bn[7]	Middle nibble of complete bytes to be transmitted or received.
B2	Txl6	Number of complete byte– bn[6]	
B1	Txl5	Number of complete byte– bn[5]	
B0	Txl4	Number of complete byte– bn[4]	

Note(s):

1. Default: reset to 00 at POR = H and EN = L. It is also automatically reset at TX EOF

TX Length Byte2 – adr 1E hex low nibbles of complete bytes, which will be transferred through FIFO and information if there is broken byte and how many bits from it should be transferred.

Figure 59:
TX Length Byte2 – adr 1E hex (1)

Bit	Signal Name	Function	Comments
B7	Txl3	Number of complete byte– bn[3]	Low nibble of complete bytes to be transmitted or received.
B6	Txl2	Number of complete byte– bn[2]	
B5	Txl1	Number of complete byte– bn[1]	
B4	Txl0	Number of complete byte– bn[0]	
B3	Bb2	Broken byte number of bits bb[2]	Number of bits in the last (broken) byte to be transmitted or number of bits that is valid in the last (broken) received byte. It is taken into account only when broken byte flag is set.
B2	Bb1	Broken byte number of bits bb[1]	
B1	Bb0	Broken byte number of bits bb[0]	
B0	Bbf	Broken byte flag	1: Indicates that last byte is not complete 8 bit wide.

Note(s):

1. Default: reset to 00 at pro = H and EN = L

Note(s): For transmission, the register 1E is write only. The written value is used for the transmission but can not be read out by the micro controller. For reception bits B0 to B4 are read only. The value read out is the number of valid bits in the last received byte. Bits B0 to B4 are updated at the end of the last successful reception. In case the last received byte is not complete, the valid bits are on the LSB side.

FIFO I/O Register – adr 1F hex 24 bytes FIFO register filled and read in cyclical way.

Direct Commands

Figure 60 lists out the direct commands that are supported in the UHF reader IC.

Figure 60:
Command Codes

Cmd (Hex) (1)	Command	Comments
9A	QueryAdjustUp (=TX no TX CRC, no RX CRC)	
9B	QueryAdjustNic (=TX no TX CRC, no RX CRC)	
9C	QueryAdjustDown (=TX no TX CRC, no RX CRC)	
9D	ACK (repeat) RN 16	
9E	NAK	
9F	ReqRN	

Note(s):

1. Value in this column includes the command bit (MSB) high.

Idle (80)

Command

Hop to Main Frequency (84)

This command forces the PLL to use frequency setting in 'PLL A/B divider main register' (see Figure 51). This is also the default setting.

Hop to Auxiliary Frequency (85)

This command forces the PLL to use frequency setting in 'PLL A/B divider auxiliary register' (see Figure 52).

Trigger AD Conversion (87)

This command triggers the analog to digital conversion with the internal 8-bit AD converter. Conversion result is available in the 'ADC readout register' (19) (see Figure 54). The source for the AD conversion is defined with msel<2:0> bits in the 'Test setting 1 register' (11) (see Figure 47). With this command it is possible to measure the both mixers output DC levels (msel<2:0>=001 and 010) and DC value on the pin ADC (msel<2:0>=011). The first two possibilities are used for diagnostic purposes. Reflectivity of the antenna or antenna environment, or leakage of the directional device causes reflection of the transmitted carrier towards receivers input. The mixers DC levels are defined with the amplitude and phase of the incoming carrier. The ADC pin is direct input to the AD converter. The input can be used to connect the external power detector for measuring the actual transmitted power. Other msel<2:0> combinations are used for test purposes.

Trigger RX Filter Calibration (88)

The command triggers the RX filter calibration cycle. The calibration cycle is finished after t.b.d. Result is available in reg10.

Decrease RX Filter Calibration Data (89)

After RX filter calibration (88), the host system (MCU) can decrease the automatically selected time constant by sending direct command 89 to fine adjust the filters. The option bit f_cal_hp_chg in reg12 defines whether the calibration data change triggered by command 89 will affect the lp or hp part of the filter. Sending one command 89 decreases calibration data for one step. There are 16 steps available, step size is 4%. Result is available in reg10.

Increase RX Filter Calibration Data (8A)

After RX filter calibration (8A), the host system (MCU) can increase the automatically selected time constant by sending direct command 8A to fine adjust the filters. The option bit f_cal_hp_chg in reg12 defines whether the calibration data change triggered by command 89 will affect the lp or hp part of the filter. Sending one command 8A increases calibration data for one step. There are 16 steps available, step size is 4%. Result is available in reg10.

Reset FIFO (8F)

The reset command clears the FIFO pointers and all IRQ flags. It also clears the register storing the error (collision) location.

Transmission with CRC (90)

The transmission commands are used to transmit data from the reader to the transponders. First the registers 'Tx length' (1D, 1E) need to be set with the number of bytes for transmission, including data on broken bytes. Then transmission data can be loaded to FIFO register (1F). Transmission starts when the third byte is written in the FIFO. Transmission of short messages (less than three bytes) is started when complete data is in the FIFO. When the command is received the reader starts transmitting. CRC-16 is included in the transmitted sequence. In this mode the micro controller has control on precise timing.

Optimal way to load transmission data is use of Continuous Write mode, starting from address 1D. Example 90 3D 00 30 AA BB CC operates as follows: Transmit with CRC, write 00 to 1D and 30 to 1E (three bytes are going to be transmitted), and write AA, BB, CC to address 1F (FIFO, data that will be transmitted). Continuous write command must be terminated by 'Continuous stop condition'. Transmission starts when the data is in the FIFO.

Transmission with CRC Expecting Header Bit (91)

This command functions similar to Transmission with CRC (90), but also informs RX decoding logic that header bit is expected in the response (Gen 2).

Transmission without CRC (92)

This command functions similar to Transmission with CRC (90), but CRC is excluded.

Delayed Transmission with CRC (93)

Delayed transmission is used in case the transmission needs to be started in a quite narrow time window after end of reception. The time between end of reception and start of transmission is set in register 'Delayed transmission wait time' (06) (see Figure 32). The register 06 needs to be set prior to the reception after which the delayed transmit should be done. After sending the 'Delayed transmission with CRC' the TX length bytes must be set and transmission data needs to be loaded in the FIFO. The reader transmitting is triggered by the TX timer.

Example: 93 3D 00 40 AA BB CC DD will transmit AA BB CC DD and CRC. Transmission will start after delayed defined in reg 06. The delay time will start at the end of previous reception - despite the command is sent during the delay is already running out.

Delayed Transmission without CRC (94)

This command functions similar to Delayed transmission with CRC, but CRC is excluded.

Block RX (96)

The block RF command puts the digital part of receiver (bit decoder and framer) in reset. The reset of the receiver is useful in case the system operates in an extremely noisy environment, causing a constant switching of the sub-carrier input of the digital part of the receiver. The receiver (if not in reset) would try to 'catch' a Preamble and in case the noise pattern matches the expected signal pattern, an interrupt is sent. A constant flow of interrupt requests can be a problem for the external system (MCU), so the external system can stop this by putting the receive decoders in reset mode. The reset mode can be terminated in two ways. One possibility is that the external system sends the 'Enable RX' command. The reset mode is also automatically terminated at the end of TX operation. The receiver can stay in reset also after end of TX if the 'RX wait time' registers (address 08) is set. In this case, the receiver is enabled at the end of the wait time following the transmit operation.

Enable RX (97)

This command clears the reset mode in the digital part of the receiver, if the reset mode was entered on the request by the 'Block RX' command.

EPC GEN2 Specific Commands

Query (98)

The Query command must be followed by 3F (continuous FIFO write) and two bytes of query data (00, DR, M, TRext, Sel, Session, Target, Q). Since this gives 15 applicable bits the last LSB bit is disregarded. Transmitter issues preamble, command, TX data and CRC-5. The received RN16 is stored in an internal register for further communication (ACK…). RN 16 is also achievable from the FIFO.

QueryRep (99)

The QueryRep command issues the command followed by two session bits. The session bits are taken from 'TX options' (02) register. The received RN16 is stored in an internal register for further communication (ACK). RN 16 is also achievable from the FIFO.

QueryAdjustUp (9A)

The QueryAdjustUp command issues the command QueryAdjust followed by two session bits and 'up' parameter (increase number of slots Q). The session bits are taken from 'TX options' (02) register. The received RN16 is stored in an internal register for further communication (ACK…). RN 16 is also achievable from the FIFO.

QueryAdjustNic (9B)

The QueryAdjustNic command issues the command QueryAdjust followed by two session bits and 'no change' parameter. The session bits are taken from 'TX options' (02) register. The received RN16 is stored in an internal register for further communication (ACK). RN 16 is also achievable from the FIFO.

QueryAdjustDown (9C)

The QueryAdjustUp command issues the command QueryAdjust followed by two session bits and 'down' parameter (decrease number of slots Q). The session bits are taken from 'TX options' (02) register. The received RN16 is stored in an internal register for further communication (ACK, ReqRN). RN 16 is also achievable from the FIFO.

ACK (9D)

The ACK command issues the command followed by RN16 (or handle) that was stored in the internal register. The stored RN16 was acquired in last successful Query command.

NAK (9E)

The direct NAK command issues the NAK command to tags.

ReqRN (9F)

The direct ReqRN command issues the ReqRN command to the tag. The last received RN is used as a parameter and the received new RN16 (handle) is stored in an internal register for further communication (ACK, ReqRN…). New RN 16 is also achievable from the FIFO.

Reader Communication Interface

The basic interface is a parallel 10-pin bus, which can be also configured and used as a serial peripheral interface (SPI) also. Both modes are exclusive and one can not switch between them in a single application. The parallel mode is selected if all IO pins are low during low to high transition of the EN pin (enable).

When the serial interface is selected in an application, the unused IO1 and IO0 pins should be hard wired according to Figure 61. Upon power-up (EN low to high transition), the reader looks for the status of these three pins and as given in Figure 61, it enters parallel or serial mode.

The reader will always behave as the “slave” connected to the host system (MCU), which behaves as the “master” device. The host system initiates all communications with the reader and is used for communication to the higher levels towards the host station, which can typically be a personal computer. The reader has an IRQ pin to ask for host system attention.

Figure 61:
Pin Assignment in Parallel and Serial Interface Connection and in Case of Direct Mode

Pin	Parallel Normal Mode, Direct Mode	SPI with SS (1), Direct Mode
CLK	CLK	SCLK from master
IO7	A/D[7]	MOSI (2) (data in)
IO6	A/D[6], Direct mode out (sub-carrier)	MISO (3) (data out), Direct mode out (sub-carrier)
IO5	A/D[5], Direct mode out (sub-carrier)	Direct mode out (sub-carrier)
IO4	A/D[4]	SS – Slave Select
IO3	A/D[3], Direct mode modulation input	Direct mode modulation input
IO2	A/D[2], Direct mode enable RX input	Direct mode enable RX input

Pin	Parallel Normal Mode, Direct Mode	SPI with SS (1), Direct Mode
IO1	A/D[1]	Hard wire to VDD_IO
IO0	A/D[0]	Hard wire to ground
IRQ	IRQ interrupt	IRQ interrupt

Note(s):

1. SS – Slave Select pin active low
2. MOSI – Master Output, Slave Input
3. MISO – Master Input, Slave Output

Communication is initialized by a Start condition, which should be followed by an Address or Command word. The Address and Command words are 8-bits long. Their format is shown in Figure 62. Communication is closed by an appropriate stop condition. Three different communication modes are available: Continuous address mode, non-continuous address mode, and command mode. Continuous address mode needs to be closed by StopCont condition, while the other two modes need to be terminated by StopSgl condition.

Figure 62:
Address / Command Word Bit Distribution

Bit	Description	Bit Function	Address	Command
7	Command control bit	0=Address, 1=Command	0	1
6	Read/Write	1=Read, 0=Write	R/W	Not used
5	Continuous address mode	1=Cont., 0=Non-cont mode	Cont	Not used
4	Address/Command bit 4		Adr 4	Cmd 4
3	Address/Command bit 3		Adr 3	Cmd 3
2	Address/Command bit 2		Adr 2	Cmd 2
1	Address/Command bit 1		Adr 1	Cmd 1
0	Address/Command bit 0		Adr 0	Cmd 0

The MSB (Bit 7) determines if the word is to be used as a command or address. The last two columns in Figure 62 show the function of the separate bits in the event that either address or command is written. Data is expected once the address word is sent. In the event of continuous address mode (Cont mode=1), the first data that follows the address is written (or read) to (from) the given address. For each additional data, the address is incremented by one.

This continuous mode can be used to write part of the control registers in a single stream without changing the address: for instance, set-up of the pre-defined standard control registers from the MCU's non-volatile memory to the reader.

In the case of noncontinuous address, only one data word is expected after the address. The two address modes are used to write or read the configuration registers or the FIFO. When writing or reading more than one byte the Continuous address mode should be used. The Command mode is used to enter a command resulting in reader action (initialize transmission, frequency hop…). Examples of expected communication between MCU and reader chip are shown below:

Figure 63:
Continuous Address Mode

Start	Adrc x	Data (x)	Data (x+1)	Data (x+2)	Data (x+3)	Data (x+4)	...	Data (x+n)	StopCont

Figure 64:
Non-Continuous Address Mode (Single Address Mode)

Start	Adr x	Data (x)	Adr y	Data y	...	Adr z	Data (z)	StopSgl

Figure 65:
Command Mode

Start	Cmd x	Cmd y	...	StopSgl

Where:

- Start = Start condition
- Adr = Address with Cont bit low
- Adrc = Address with the Cont bit high
- Cmd = Command byte
- Data = Data byte
- StopSgl = Stop condition for termination of the command or non-continuous address mode
- StopCont = Stop condition for termination of the continuous address mode

There are also combinations of different communication modes allowed in a single stream between the start and stop condition. Some examples of combined communication are presented below:

Figure 66:
Non-Continuous Address Mode and Command Mode

Start	Adr x	Data (x)	Adr y	Data (y)	...	Cmd z	Cmd w	StopSgl

Figure 67:
Command and Continuous Address Mode

Start	Cmd x	Cmd y	...	Adrc z	Data (z)	Data (z+1)	...	Data (z+n)	StopCont

Figure 68:
Non-Continuous, Command, and Continuous Address Mode

Start	Adr x	Data (x)	...	Cmd y	...	Adrc z	Data (z)	Data (z+1)	...	Data (z+n)	...	StopSgl

Non-Continuous address mode and command mode can be continued by any mode including the Continuous address mode. The Continuous address mode should be terminated by StopCont condition. Changing from Continuous address mode to the other two modes can be done only by StopCont condition followed by start condition.

Majority of the registers in the reader IC are 8-bit long. They can be accessed by continuous or non-continuous address mode.

Registers 12, 14, 15, 16, and 17 are three bytes deep. They can be accessed by Continuous address mode only. The least significant byte is accessed first. It is possible to access only deep register in a single communication stream, more of them, or combination of normal and deep registers. Example is presented below:

Figure 69:
Example

Start	Adrc x	Data0 (x) [1]	Data1 (x) [2]	Data2 (x) [3]	StopCont

Note(s):

1. Least significant byte
2. Middle byte
3. Most significant byte

Continuous access is possible for registers 00 to the end of the register 12. Register 13 is deep register and prevents continuous access over it to register 14. Continuous access is again possible from register 14 to the end of FIFO (address 1F).

The 24 bytes deep FIFO register can be accessed by Continuous address mode only. It is allowed to use communication stream combined of command mode and address mode.

Example is combination needed for transmission composed of Reset FIFO, Transmit, write to 1D, 1E for transmission length, and continuously to 1F for filling FIFO with transmission data.

Figure 70:
24 Bytes Deep FIFO Register

Start	ResetFIFO	Transmit	Write Cont. to 1D	Data (1D)	Data (1E)	Data FIFO (0)	Data FIFO (1)	...	StopCont
	8F	90	3D	TX length		TX data			

Parallel Interface Communication

In parallel mode, the Start condition is triggered by rising edge of the IO7 pin while the CLK pin is high and IO6-IO0 are low. This is used to reset the interface logic. Communication is terminated by StopSgl condition or StopCont condition. StopSgl condition is triggered by falling edge on IO7 pin while CLK pin is high and IO6-IO0 are low. StopCont condition is triggered by successive rising and falling edge on IO7 pin while CLK and IO6-IO0 are low. The 'StopSgl' condition is used to terminate the direct mode.

Figure 71:
Parallel Interface Communication with Single Stop Condition "StopSgl"

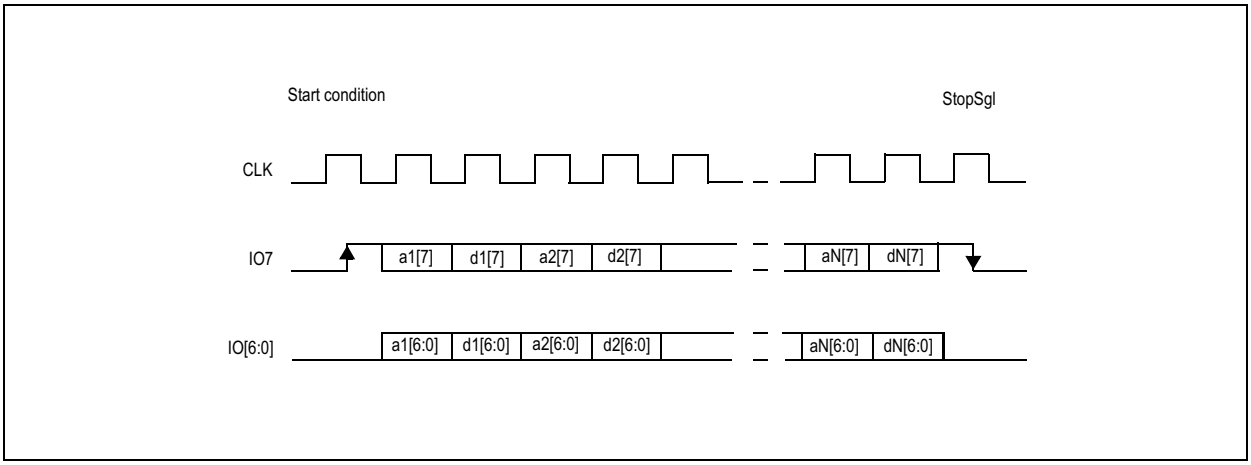


Figure 72:
Parallel Interface Communication with Continuous Stop Condition "StopCont"

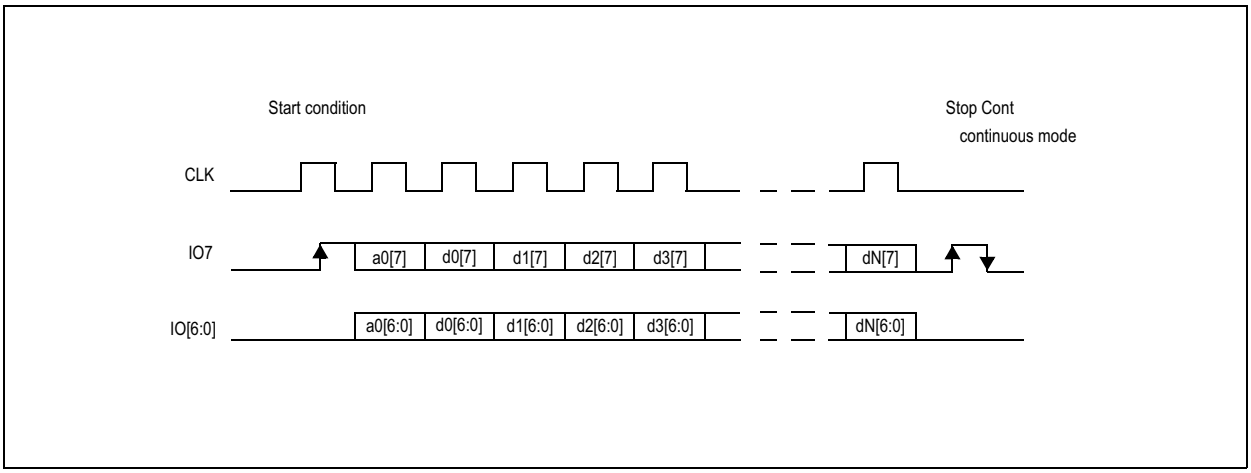
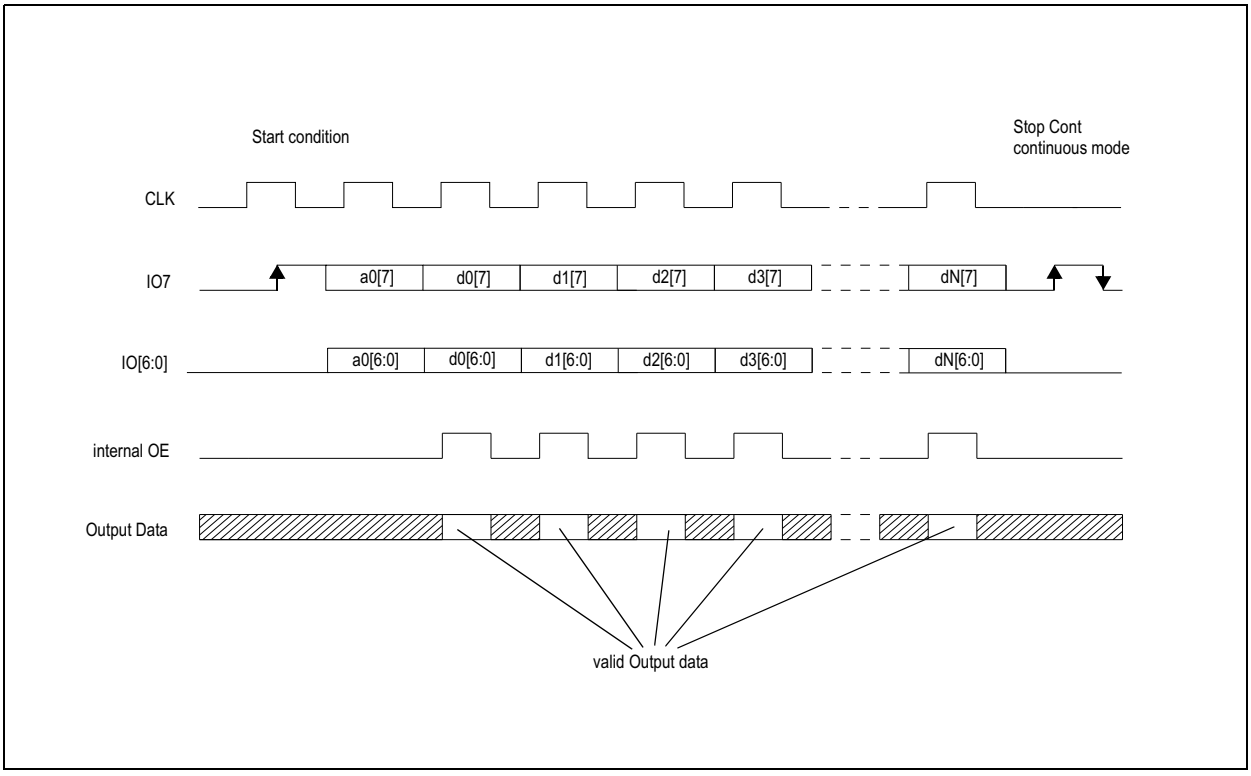


Figure 73:
Data Output Only when CLK is High



Timing Requirements for Parallel Interface. While using parallel interface, there must always be a separation between CLK transitions and IO0…IO7 transitions. Minimum time interval between transition on CLK and data lines is 100ns.

Minimum CLK high time interval is 300ns in periods when IO0…IO7 pins are used as data outputs (see Figure 73) or 100ns in periods when IO0…IO7 pins are used as inputs (address, command, or register write).

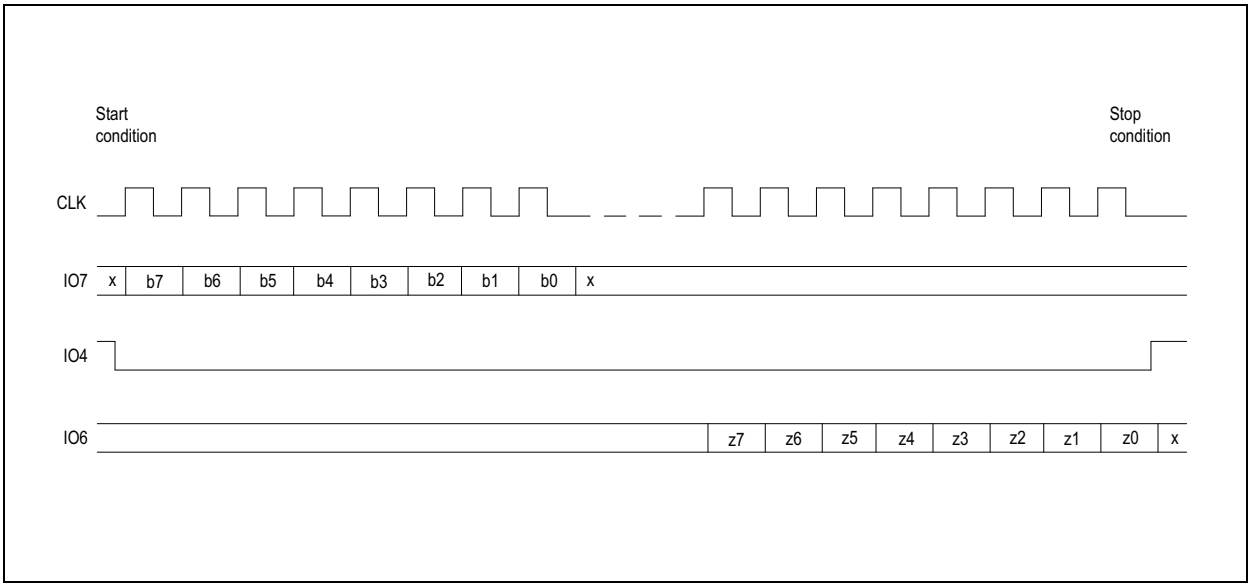
To decrease interferences between MCU communication and RF part of the chip, the output resistance of IO0…IO7 lines is 400Ω typical and 800Ω maximum. The firmware designer should be aware of the fact that in case higher capacitance are connected to these pins, then possibly longer CLK high intervals are needed to allow settling of the output level.

Serial Interface Communication

In serial interface IO4 pin enables the communication, CLK pin is serial data clock, IO7 is serial data input, and IO6 is serial data output.

The interface is in reset as long the IO4 pin is high. Communication is started by falling edge on the IO4 pin. Data coming from the host system is sampled on the falling of the CLK pin. When reading out the data from the UHF chip, the data is set on the rising edge of the CLK pin. Host system (MCU) should sample the data on the falling edge on the CLK pin. Communication is terminated by rising edge on the IO4 pin. All words are 8-bits long with the MSB transmitted first.

Figure 74:
Serial Interface Communication



In this mode the serial interface is in reset while the IO4 signal is high. CLK pin is serial data clock, IO7 is serial data in, and IO6 is serial data output. Communication is terminated when IO4 signal goes high again.

Timing Requirements for Serial Interface. Minimum time interval between IO4 falling edge and first CLK change is 100ns.

Minimum CLK high time interval is 300ns in periods IO6 pin is used as data output (like register reading – data from UHF chip to MCU) or 100ns in periods when IO7 pin is used as input (address, command, or register write – data from MCU to UHF chip). Minimum CLK low interval is 100ns.

To decrease interferences between MCU communication and RF part of the chip the output resistance of IO6 line is 400Ω typical and 800Ω maximum. The firmware designer should be aware that in case of higher capacitance is connected to this pin possibly longer CLK high interval is needed to allow settling of the output level.

Minimum hold time (time in which IO6 output data is valid after the CLK fall edge) is 130ns.

Minimum time interval between bytes is 200ns.

Minimum time interval between last CLK falling edge and IO4 rising edge is 200ns.

Minimum IO4 high time interval is 200ns.

Timing Diagrams

Figure 75:
Write Data

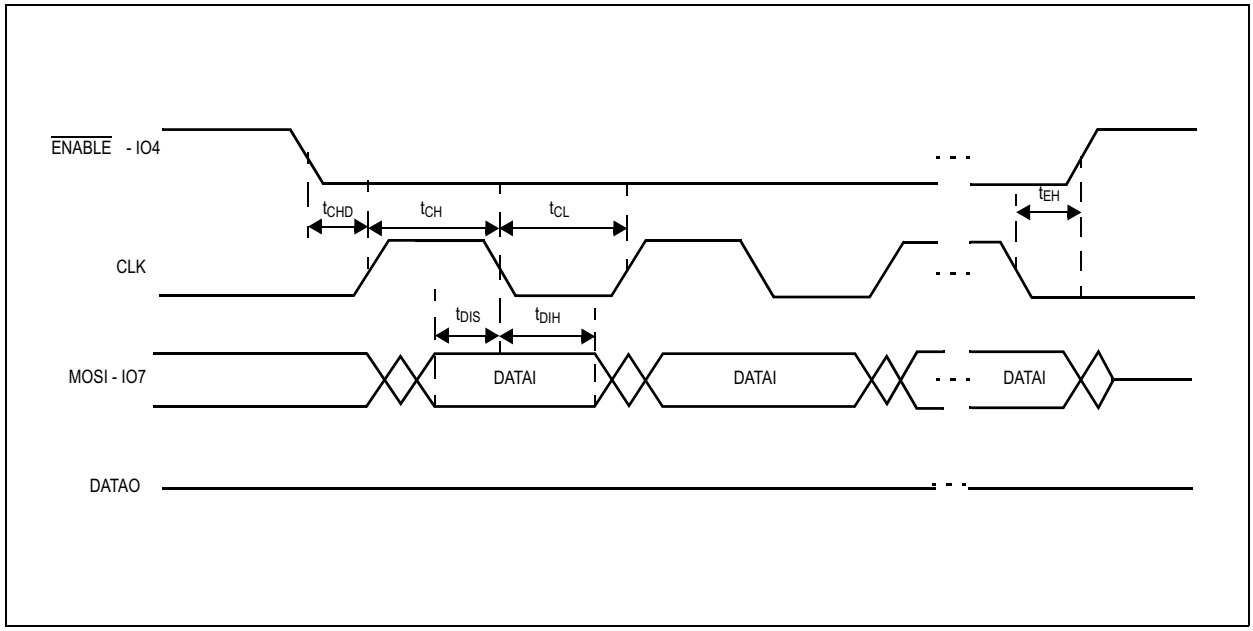
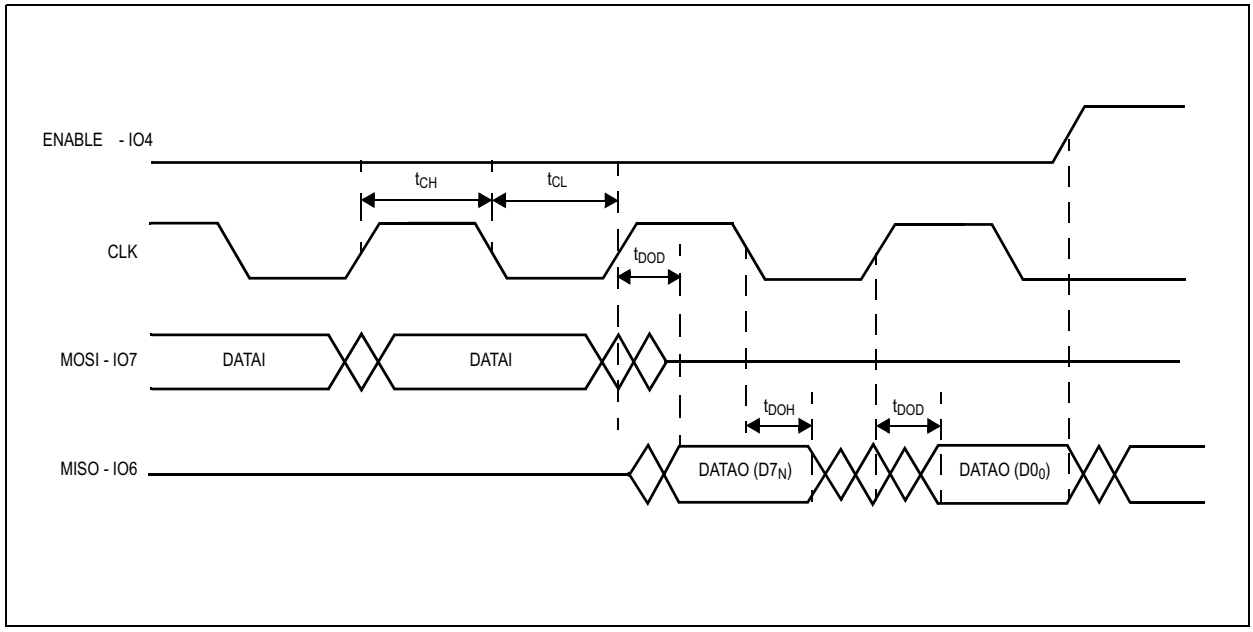


Figure 76:
Read Data



Timing Parameters

Figure 77:
Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
General						
BR_{SDI}	Bit rate				2	Mbps
t_{CH}	Clock high time		250			ns
t_{CL}	Clock low time		250			ns
Write Timing						
t_{DIS}	Data in setup time		20			ns
t_{DIH}	Data in hold time		10			ns
t_{EH}	Enable hold time		300			ns
Read Timing						
t_{DOH}	Data out hold time		150			ns
t_{DOD}	Data out delay				150	ns

FIFO

The FIFO is loaded in a cyclical manner. The FIFO and its pointers should be cleared by the Reset FIFO command (0F) prior each FIFO write for transmission. Data coming from the MCU is stored in the FIFO at address 1F hex from location 0 to 23. When the bytes are loaded in the reader, the input FIFO counter is counting the number of bytes loaded into the FIFO. When data is read from the FIFO, an output FIFO counter is incremented and it follows the status of the bytes read.

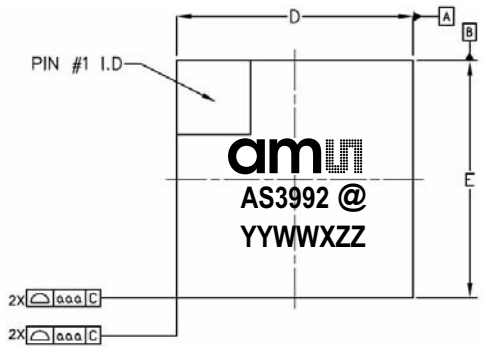
The input and output counters are 12 bits each. They are used to control the data flow in and out of the FIFO. This control sends an interrupt request if the number of bytes in the FIFO is less than 6 and if number of bytes increases to above 18 so that MCU can send new data or remove the data as necessary. It additionally checks that the number of data bytes to be sent does not surpass the value defined in 'TX length' bytes. It also signals the transmit logic when the last data to be sent was moved from FIFO to the transmit logic. The number of bytes in the FIFO is available in the FIFO status register. This register also contains three status flags:

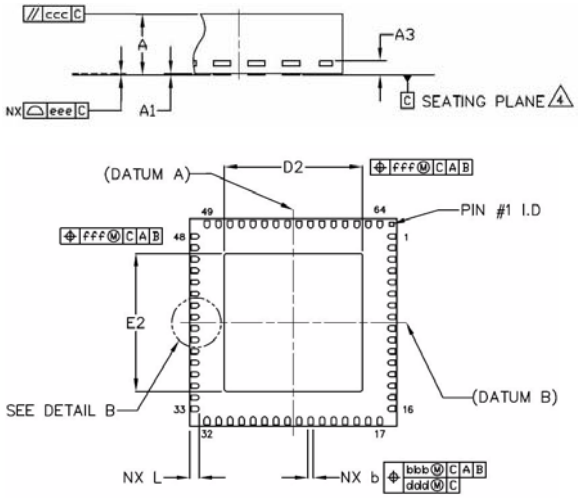
- Fove bit is set in case of FIFO overflow
- Flol bit is set in case of low FIFO level during transmission
- Fhil bit is set in case of high FIFO level during reception

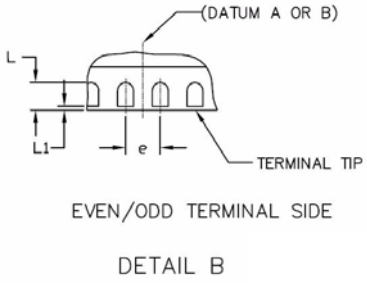
Package Drawings & Markings

The device is available in a 64-pin QFN (9mm x 9mm) package.

Figure 78:
Drawings and Dimensions







DETAIL B

Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	-	0.20 REF	-
L	0.35	0.40	0.45
L1	0	-	0.15
b	0.18	0.25	0.30
D		9.00 BSC	
E		9.00 BSC	
e		0.50 BSC	
D2	5.90	6.00	6.10
E2	5.90	6.00	6.10
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		64	

REF: Reference Dimension, usually without tolerance, for information purposes only.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Note(s):

1. Dimensions and Tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension b applies to metalized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.15mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.
6. N is the total number of terminals

Figure 79:
Marking: @YYWWXZZ

@	YY	WW	X	ZZ
Sublot Identifier	Manufacturing Year	Manufacturing Week	Assembly plant identifier	Assembly traceability code

Ordering & Contact Information

Figure 80:
Ordering Information

Ordering Code	Description	Package	Delivery Form	Delivery Quantity
AS3992-BQFM	Internal DRM compatible VCO, pre-distortion	64-pin QFN (9mm x 9mm)	Tape and Reel (1)	50 pcs/reel
AS3992-BQFT				500 pcs/reel

Note(s):

1. Dry Pack Sensitivity Level =3 according to IPC/JEDEC J-STD-033A for full reels.

Buy our products or get free samples online at:
www.ams.com/ICdirect

Technical Support is available at:
www.ams.com/Technical-Support

Provide feedback about this document at:
www.ams.com/Document-Feedback

For further information and requests, e-mail us at:
ams_sales@ams.com

For sales offices, distributors and representatives, please visit:
www.ams.com/contact

Headquarters
ams AG
Tobelbaderstrasse 30
8141 Unterpremstaetten
Austria, Europe

Tel: +43 (0) 3136 500 0

Website: www.ams.com

RoHS Compliant & ams Green Statement

RoHS: The term RoHS compliant means that ams AG products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ams Green (RoHS compliant and no Sb/Br): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

Important Information: The information provided in this statement represents ams AG knowledge and belief as of the date that it is provided. ams AG bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. ams AG has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams AG and ams AG suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

Copyrights & Disclaimer

Devices sold by ams AG are covered by the warranty and patent indemnification provisions appearing in its General Terms of Trade. ams AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein. ams AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with ams AG for current information. This product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by ams AG for each application. This product is provided by ams AG “AS IS” and any express or implied warranties, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose are disclaimed.

ams AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of ams AG rendering of technical or other services.

Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 1.10 (2010-Nov-24) to current revision 1-12 (2015-Nov-04)	Page
1.10 (2010-Nov-24) to 1-11 (2015-May-22)	
Content of austriamicrosystems datasheet was converted to latest **ams** design	
Updated Figure 80	80
Added Appendix - Errata Notes	85
1-11 (2015-May-22) to 1-12 (2015-Nov-04)	
Updated Figure 5	9
Updated Package Drawings & Markings section	79
Updated Figure 80	80

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Appendix - Errata Notes

Known Issues in AS3992 (V6)

No.	Issue Description	Comment	Workaround
Issues found in Digital Section			
P1	clsys<2:0>=000b enables 60kHz on the CLSYS output	As a consequence a -62dBc TX spur at 60kHz can be seen. This problem can be considered as non- critical. By using the proposed workaround, the spur disappears.	Set the bit **open_dr** in register 0x05 to high.
P2	In case exactly two bytes are received in the FIFO and both bytes are read out during reception, the subsequent **ReqRN** command is corrupted. The case happens when 2byte_ irq is used.	The data length information is contained in the first received byte – therefore it is sufficient to read only one byte. Any other number of bytes (1, 3, 4, …) can be read out without any problems.	Read out only the first FIFO byte which contains the EPC length information upon receiving **Irq_2nd_byte**
P5	In case BlockRX is used after receiving the RN16 the IRQstatus register (0x0C) reports 0x00 instead of 0x4x. (Select, NAK)	An alternative to the Block RX command, reg03:0A can be used as well.	Skip the direct command BlockRX. In case the issue still happen act as in case of a collision.
P6	In case BlockRX is used after receiving the RN16 the IRQstatus register (0x0C) reports 0xC0 instead of 0x4x. (Select, NAK)	An alternative to the Block RX command, reg03:0A can be used as well.	Skip the direct command BlockRX. In case the issue still happen act as in case of a collision.
P7	After corrupted reception of RN16 with IRQ status register (0x0C) = 0x40 the reception remains enabled, TX is blocked and consequently the TX IRQ is missing.	There are two possibilities to identify this condition: • Read IRQstatus just after subsequent TX command (IRQstatus=0x80 is expected) • Watch dog timer action when waiting on the missing IRQ pulse at the end of transmission.	EN H-L-H transition is needed.
P8	After EPC reception the IRQstatus register contains 0X00.	This case does not indicate that a collision has happened. There is no need to increase the number of slots in the subsequent inventory.	Continue inventory round as if a corrupted EPC was received.
P9	After any reception the IRQstatus register contains 0x41.		Continue inventory round as if a corrupted reception has happened (collision on RN, error EPC…)

No.	Issue Description	Comment	Workaround
P10	SPI: Direct command Reset FIFO (0x8F) should not be sent before the direct command ReqRN (0x9F).		Send the direct command Reset FIFO after the TX IRQ, before the receiving the HANDLE.
G5d	SPI: Reading the FIFO register 0x1F should not be done right after an IO4 H-L transition.		Read the FIFO status register in single byte mode before reading the contents of the FIFO register.
Issues found in Analog Section			
A4b	MCU support current not stable and higher than expected (400uA- 1000uA). Should be 400-500uA typ.	Issue is less critical since MCU current in operation is typically much higher than the unwanted 500uA.	
H3	The internal PA cannot be used in majority of the applications due to insufficient linearity and stability.	Use low power RF output.	

Important Notes and Hints

No.	Issue Description	Comment	Recommendation
P3	**QueryRep** and **QueryAdj** need a Reset FIFO (0x8F) direct command for correct operation.	Not critical in a normal inventory round in case an access operation (read/write) is done in the same round. The issue decreases tag inventory rate in case only the EPCs are read and no read or write operation is planned.	Use **Reset FIFO** command before **QueryRep** and **QueryAdj**.
P3A	Direct commands for transmission (0x90, 0x91, 0x92) require a Reset FIFO direct command for correct operation.		Use Reset FIFO before transmission commands.
P4	To meet a **StopSgl** condition a IO7 transition at CLK=H is needed. IO6:0 should be stable during **StopSgl**.	Previously also the stop condition met by a transition of all IO lines at CLK=H was allowed.	Use correct StopSgl.
G8	A FIFO read operation requires the continuous read mode for correct status of the pointers.		Read FIFO contents in the continuous read mode.

Content Guide