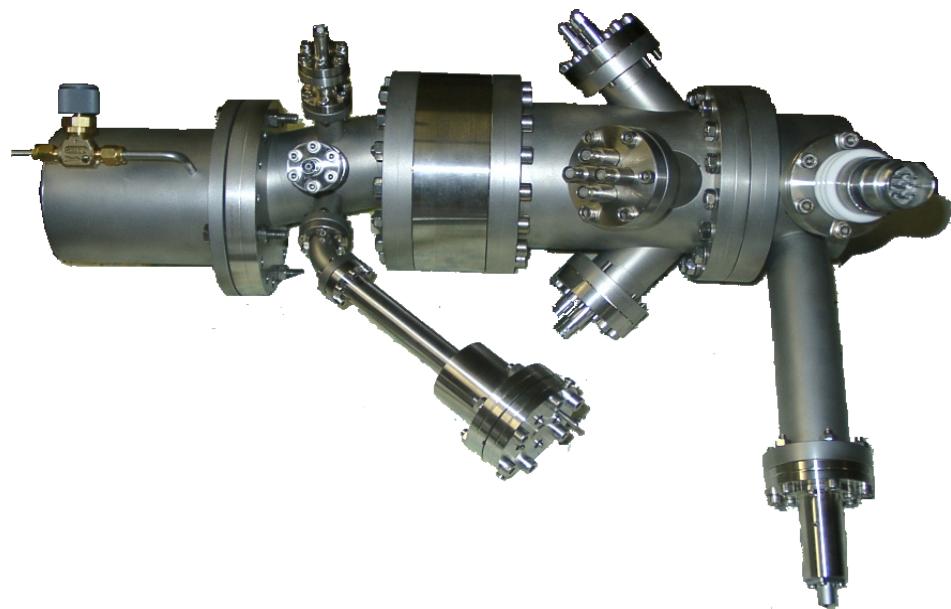


# High Voltage SPLEED Detector/ Delayline Detector Combination



# Manual



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## 2 Introduction

### 2.1 General Information

This manual provides an overview of the set-up of the HV SPLEED Detector, the naming of its internal parts and the pin-out of the feed-throughs as well as to assist users in the installation, operation and maintenance of the Delayline Detector DLD 1818 as part of the HV SPLEED Detector/ DLD Combination. It is divided into 13 chapters.

### 2.2 Safety Instructions

Please read this manual carefully before performing any electrical or electronic operations and strictly follow the safety rules given within this manual.

The following symbols appear throughout the manual:



The “note symbol” marks text passages, which contain important information/ hints about the operation of the detector. Follow these information to ensure a proper functioning of the detector.



The “caution symbol” marks warnings, which are given to prevent an accidentally damaging of the detector or the readout system. Do NOT ignore these warnings and follow them strictly. Otherwise no guarantee is given for resulting damages.



The “high voltage symbol” marks warnings, given in conjunction with the description of the operation/ use of high voltage supplies and/ or high voltage conducting parts. Hazardous voltages are present, which can cause serious or fatal injuries. Therefore only persons with the appropriate training are allowed to carry out the installation, adjustment and repair work.

## 2.3 General Overview of the System

---

The HV SPLEED detector/ DLD Combination is designed to fit to a Scienta R4000 energy analyzer and is laid out for an operation on a base voltage of up to 10 kV. It consists of three parts [named A, B, and C]. Part A is the front cover, which is installed directly into the Scienta analyzer. It holds the HV connection ports for the DLD. Part B and C are separated by a UHV valve (100 mm i.d.). The part B is housing an electrostatic lens system, for electron transfer to the actual SPLEED detector as well as the delayline detector, while part C holds the sample holder of the SPLEED detector with a tungsten analyzer crystal with integrated heater, the electron optics, 4 channeltron detectors and the electronic oxygen doser.

The delayline detector is particularly developed for the needs of 3D(x,y,t) area and time detection of electrons. It is mounted next to the entrance lens on the front side of part B. It consists of a microchannel plate stack and two layers (x, y) of meander structured delaylines. The image is sampled by the DLD readout electronics. The 3D (x, y, t) detection bases on the measurement of time differences and time sums of signals, with a high temporal resolution in one device. The count rate can reach up to 0.7 MHz in the commonly used 4-fold coincidence measurement.

# 3 Installation

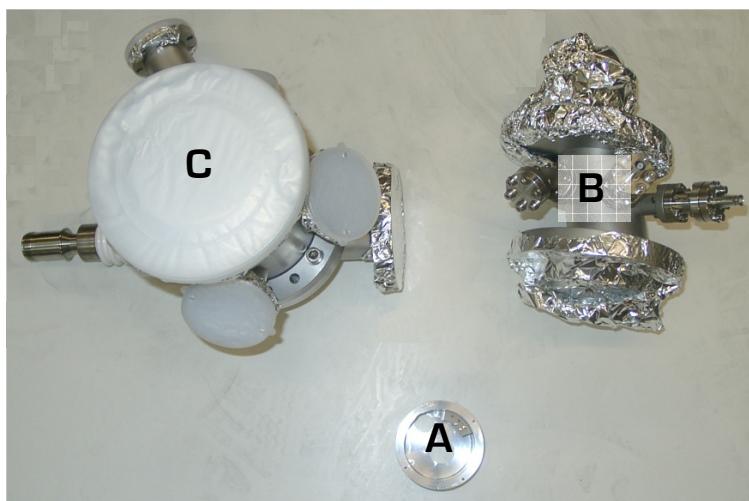
## 3.1 Initial Inspection

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Visual inspection of the system is required to ensure that no damage has occurred during shipping. Should there be any signs of damage, please contact SURFACE CONCEPT immediately. Please check the delivery according to the packing list (see Table 1) for completeness.

- a) Detector front cover (part A). It is directly installed in the exit port of the Scienta analyzer.
  - b) Detector top part (part B) is holding the first two transfer lenses as well as the DLD.
  - c) Detector bottom part (part C) is holding further lenses, the deflector, the sample holder, and mounting ports for the channeltron detector.
- 
- 1] Quad Channel USB2.0-TDC with power cable.
  - 2] Specification Sheet and CD (Software + Documentation)
  - 3] ACU 4.3.2
  - 4] DLD Readout cable
  - 5] USB2.0 cable

**Table 1: Packing list for the HV SPLEED/ DLD Combination**



**Figure 1: Contents of delivery package**

## 3.2 Installation

### 3.2.1 Mounting the HV SPLEED/ DLD Combination to a Scimenta R4000 Analyzer

The HV SPLEED/ DLD Combination is transported under vacuum. Vent the transport container carefully. Release the M8 screws of the vacuum container and take it off carefully.



Figure 2: HV SPLEED/ DLD with transport container.

The detector front is covered with an aluminum foil (see Figure 3). Remove this foil carefully. Take care, that no parts are falling into the detector.

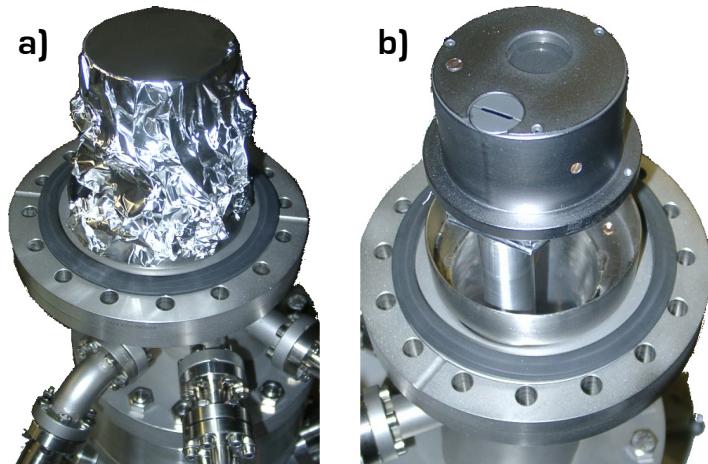


Figure 3: HV SPLEED/ DLD Front, (a) covered with aluminum foil for transportation  
(b) without aluminum foil.

The detector front cover (Part A) is fastened to Part B with a drilled wire for transportation. Open this wire carefully and remove Part A from Part B.  
Check the front side of the MCP stack of the DLD for particles.



The microchannel plates in front of the detector should be protected from exposure to particle contamination. Particles that stick to the plate can be removed by carefully using a single-hair brush carefully and/or with dry nitrogen. Reading the instructions "microchannel plates" in chapter 10 is strongly recommended.

Keep the vacuum container in case that the detector must be sent back for repair. It can also be used to store the detector when not installed in a vacuum chamber.



**Note** The detector should be kept under vacuum all the time.

The HV SPLEED/ DLD Combination is installed to the same CF100 flange as the standard Scienta MCP detector. Therefore the Scienta MCP detector must be removed before the HV SPLEED/ DLD Combination can be installed.



Strictly follow the description for dismounting the Scienta MCP detector within the Scienta analyzer and/ or the Scienta MCP detector manual.

The high voltage supply of the Scienta MCP detector is provided by three HV cables, which are installed within the analyzer. Disconnect these three cables, before removing the MCP detector.



**Note** Two of the three HV cables for supplying the MCP detector are used to supply the DLD.

#### **Mounting Part A**

The detector cover (Part A) must be installed first. It is installed directly to the Herzog Plate within the Scienta analyzer. The correct orientation for Part A can be found in Figure 4. The hole for the entrance lens is moved 24mm out of the center of part A. This hole must be orientated to the bottom of the CF 100 mounting flange on the analyzer. Use the three special M3 screws (see Figure 5) to fasten the detector cover to the analyzer.

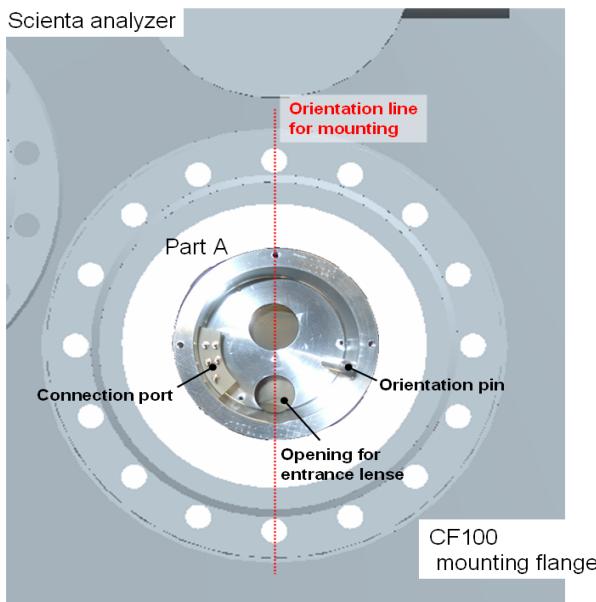


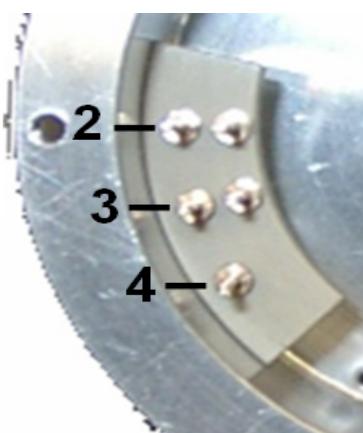
Figure 4: Mounting of detector cover (Part A).



Figure 5: Copper screws for mounting the detector cover (Part A) to the analyzer.

The detector cover holds a connection port for the high voltage supply of the DLD. It holds two rows of 3 and 2 pins (5 pins in total). The outer row with three pins is meant for the connection of the three HV cables from the analyzer, which are originally used for connecting the Scienta MCP detector. The two inner pins are contacting the DLD automatically, when placing part B into the analyzer correctly.

The three HV cables within the Scienta analyzer are marked by kapton foil with punched holes (2, 3, and 4). See chapter 5 for further details.



Correspondence of Pin no. and Scienta HV Supply:

- 2 – MCP Front
- 3 – MCP Back
- 4 – Screen

Figure 6: Pin out of connection port in Part A.



**Do not forget to connect the three HV cables to the connecting port of Part A before mounting Part B.**  
**Check for the correct connection.**

### **Mounting Part B**

In a second step, part B is installed to the analyzer. Be really careful when entering the front part of the electrostatic lens system with the delayline detector into the analyzer. Check for the correct orientation. It is defined by the orientation pin of Part A and the corresponding hole in the PEEK isolation plate of Part B, as well as by the connection port of Part A and the corresponding plugs on Part B and by the opening for the entrance lens (see Figure 7 for details). Also note the red orientation line in Figure 8 for the correct flange orientation.

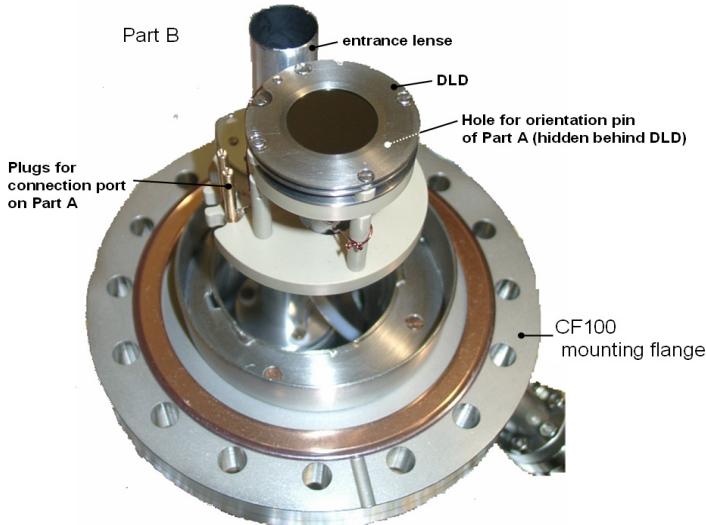


Figure 7: Parts of Part B, which can be used for correct orientation during installation.

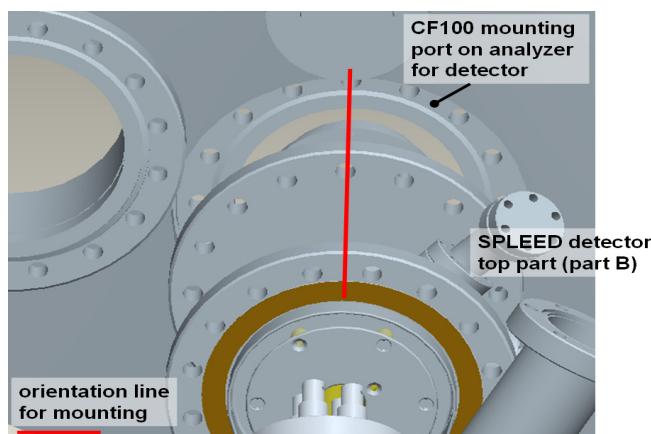


Figure 8: Flange orientation for Part B.



Be very careful when mounting Part B of the HV SPLEED/ DLD Combination to the analyzer. It is crucial to check for the correct orientation right at the beginning of entering the front lens with the DLD into the analyzer.

In case of a wrong orientation, do **NOT** try to rotate Part B within the analyzer. This can lead to fatal damage of the electrostatic lens system and/or the delayline detector. Withdraw Part B completely before correcting the orientation.

#### **Mounting Part C**

The SPLEED Detector has been designed to allow the installation of a valve between Part B and Part C. Install this valve to Part B before mounting Part C. There are electrostatic elements of Part A and B, which are extending above the CF100 mounting flanges by up to 18mm and more [see Figure 9 for details]. Therefore it is extremely important that only valves are installed, which still allow a proper opening and closing with material extending such deep into the valve.

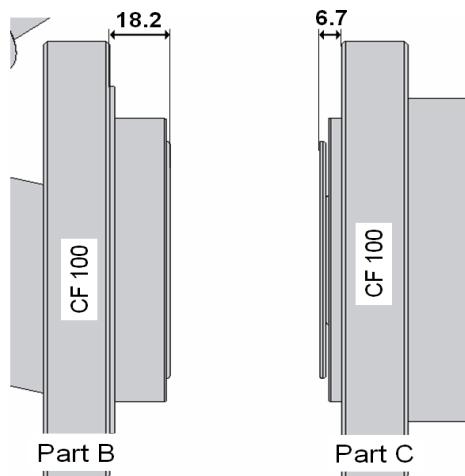


Figure 9: Part A and Part B with extending electrostatic elements (schematic).



Do only install valves, which still allow a proper opening and closing with material extending up to 18mm into the valve. Otherwise the closing of the valve will damage the electrostatic elements.

In case that no valve should or can be installed, an adequate adapter flange CF100 – CF100 of at least 30mm length but of not more than 70mm must be installed between Part B and C.



Do not mount Part C of the SPLEED Detector directly to Part B. Always use a valve or an adapter flange. The length of the adapter flange should be at least 30mm but not more than 70mm.

The correct flange orientation for mounting Part C is indicated in Figure 10 by the red orientation line.

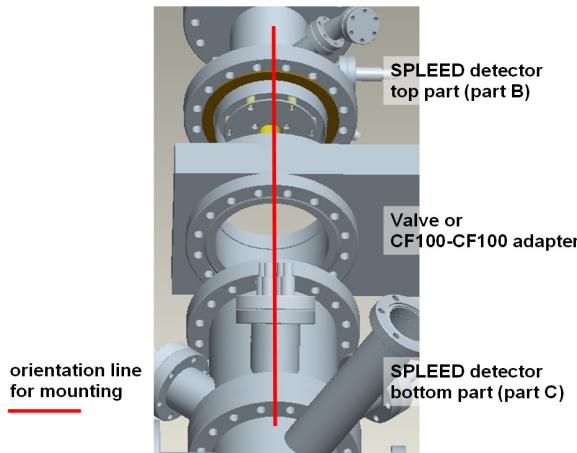


Figure 10: Flange orientation for mounting Part C to Part B (schematic).

### 3.2.2 Cabling and High Voltage

The general connection scheme of the SPLEED detector is shown in Figure 11 and the connection scheme of the DLD readout electronics is shown in Figure 12.

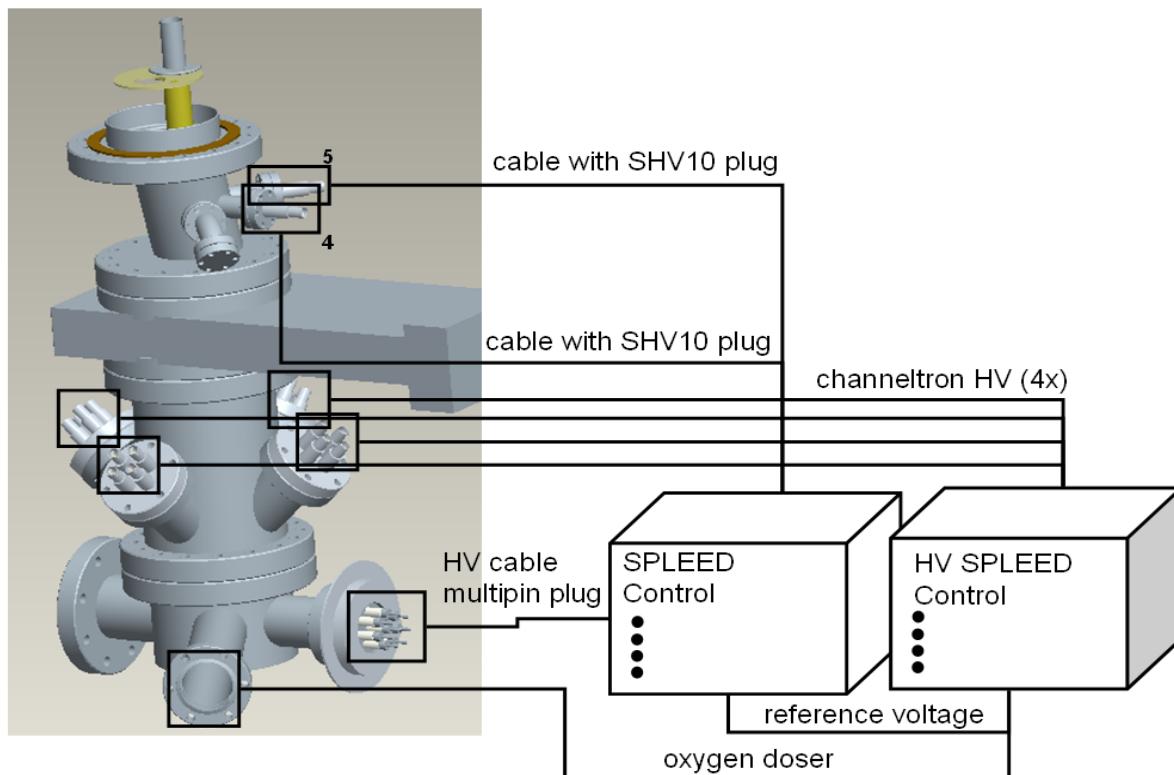


Figure 11: Connection scheme of HV SPLEED detector.

- Connect the high voltage multipin plug to the 10fold high voltage feed-through on part C of the SPLEED
- Connect the two single cables with SHV10 plugs to the corresponding SHV10 ports (4 & 5) on

part B of the SPLEED detector.

- Connect the cable for the oxygen doser between HV SPLEED Control and the oxygen doser
- Connect the corresponding high voltage to the 4 channeltrons.



**Be sure that all voltages are settled to zero before connecting the high voltage cables to the detector, otherwise serious damage to the detector can occur due to high voltage sparks.**

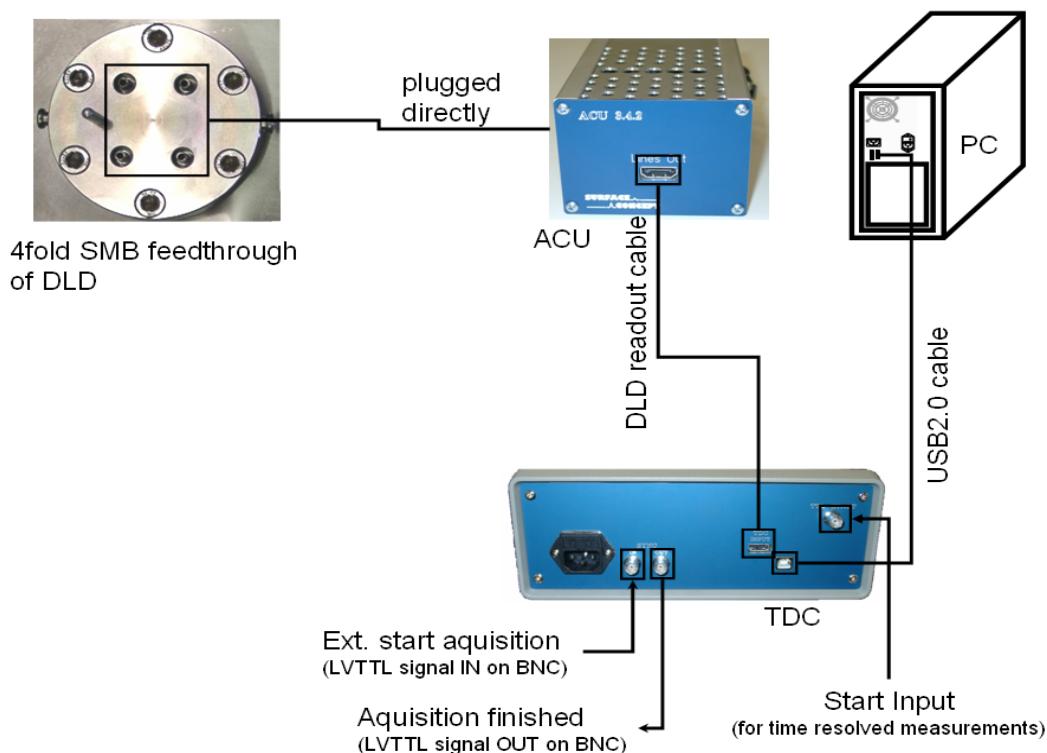


Figure 12: Connection scheme of DLD Readout Electronics.

- The pulse processing unit ACU can be connected directly to the DLD 4-fold SMB feed-through. The metal pin gives the orientation. Fix the ACU with the two clips on the housing to the fastening bolts on the feed-through.
- Use the DLD readout cable to connect the "Lines Out" socket on the front of the ACU with the "TDC Input" socket at the rear panel of the USB2.0-TDC. To perform time measurements with respect to an external clock, provide start pulses to the start input of the TDC. Use the BNC socket named "TTL Start" to apply standard TTL signals.
- Use the USB 2.0 cable to connect the USB2.0-TDC to the PC and follow the instructions for installing the device driver if connected for the first time. If the device driver is already installed, the USB connection is established automatically. Do not use PC front panel USB connectors; they are often restricted in performance. For further details on driver installation please see chapter Fehler! Verweisquelle konnte nicht gefunden werden..
- Connect the power cable to the main connector and plug the USB cable into the PC. Switch on the TDC

and follow the instructions for installing the device driver being connected for the first time. If the device driver is already installed, the USB connection is established automatically.

- The high voltage is supplied via the three cables from the MCP detector within the Scienta analyzer. Connect these cables as already described above.



**Finish the complete cabling before the TDC is turned on and the software is started.**  
Also, close the software and turn off the TDC before performing any changes to the cabling. This applies especially to the connection and disconnection of the start input of the TDC. The start input of the TDC cannot handle pulses which are arriving in a time interval of smaller than 150 ns, as they are produced by e.g. connecting to and disconnecting from the start input respectively.

**Don't start the detector operation before you are familiar with the detailed descriptions of chapter 8 within this manual.**

## 4 USB 2.0 Driver Installation

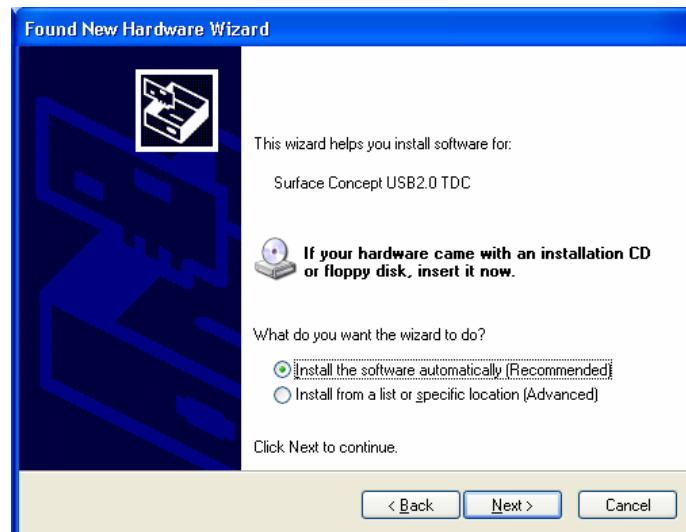
Read-out of the USB2.0-TDC is done with a standard PC via USB2.0. For the PC the following system requirements are highly recommended:

- Processor: 1.6 Ghz
- RAM: 1GB
- Windows XP / Windows 2000
- USB 2.0 [no front panel connector]
- Monitor resolution: in Y min. 864 pixel [most critical], in X min. 1024 pixel

**Note** ! The use of USB2.0 for the readout of the TDC is highly recommended. In principle the readout of the TDC is compatible to USB1.0, but the required data transfer rates are not reached. Do not use PC front panel USB connectors; they are often restricted in performance.

Before the detector can be used, the USB driver for the TDC must be installed. The installation procedure is described below:

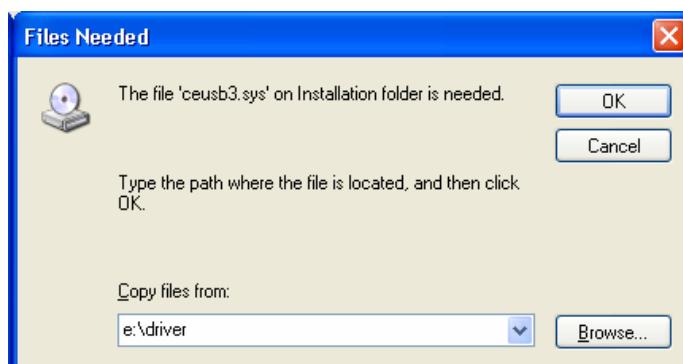
- First, log on as Administrator. Close all applications on your PC. If you are using any anti-virus or firewall software, close them (or disable them). Connect the USB cable to your Windows System with USB2.0 enabled. Windows will find the new hardware, and the "Found New Hardware Wizard" will launch. To continue, select "No, not this time" (not looking for windows updates) and "click "Next>".



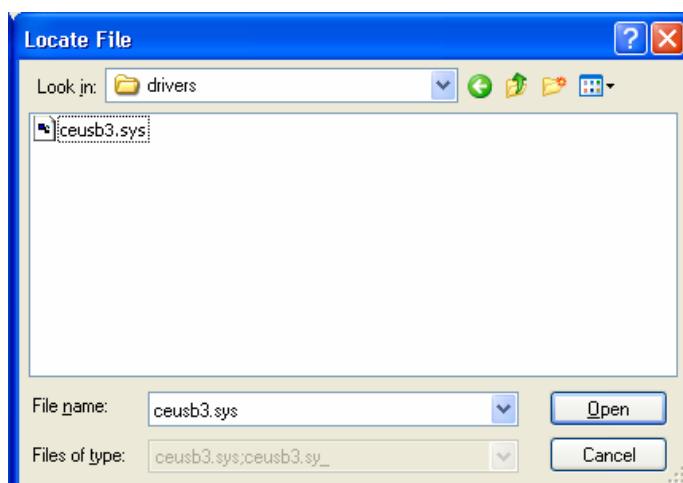
- Continue Installation although the Windows XP capability test failed.



- Enter the path where the driver is located (or Browse to it)



- The internal name of the USB2.0 TDC driver is "ceusb3.sys", select it and press "Open".



- To continue, click "OK". The driver for the Surface Concept USB2.0 TDC will be installed.

- After a few seconds, a finishing dialog should appear as below. To finish, click "Finish".



**Note** After finishing the installation routine for the first time, it will start again. Go through the routine again a second time completely. The driver installation will be complete only after the second installation.

The driver also has to be installed again, when the USB cable is connected to a different USB port on the PC than at the last installation. In this case the driver installation should start automatically.

## 5 HV SPLEED/ DLD Layout

### 5.1 HV SPLEED Detector – Schematic Cut

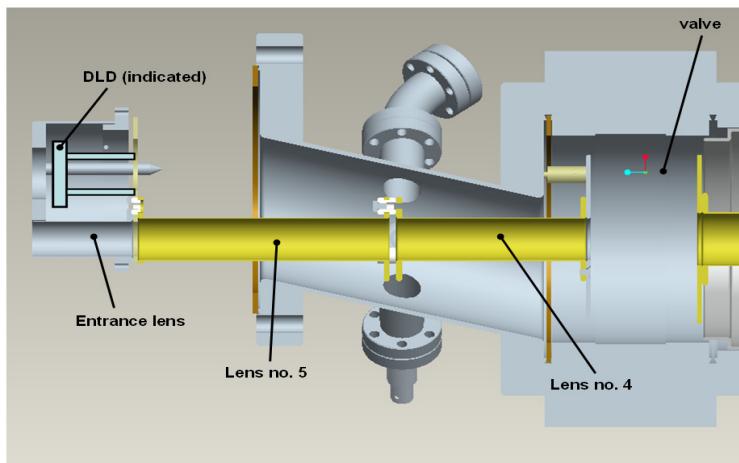
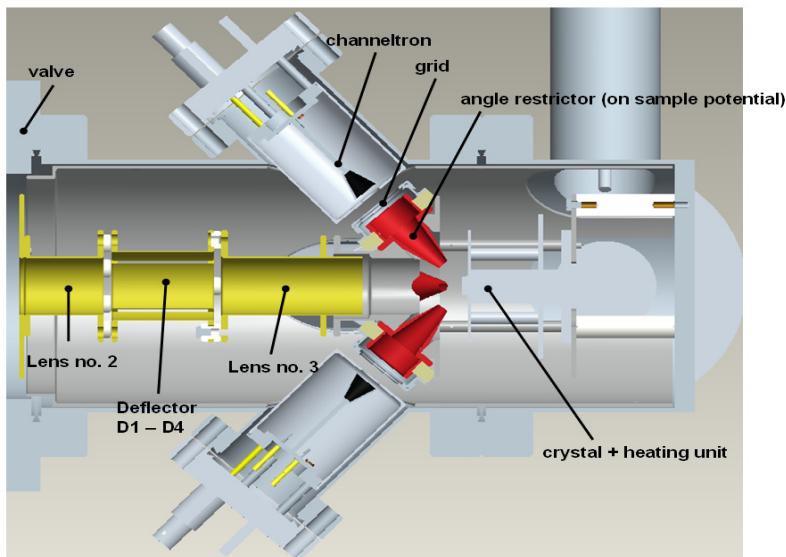


Figure 13: Cross section of HV SPLEED detector and transfer optics (DLD is only indicated)

## 5.2 HV SPLEED Detector – Internal Set-up

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The HV SPLEED/ DLD combination consists of three parts [A, B, and C]. Part A is the detector front pot [see Figure 14]. It is installed directly into the Scienta analyzer. It holds a connection port with 5 pins, sorted in two rows of 3 and 2 pins. The outer row with 3 pins is used for the high voltage connection from the Scienta power supply. Connect the three HV cables, which are originally used to supply the Scienta MCP detector to the 3 pins in the outer row of the connection port in the corresponding order 2, 3, and 4 (see Figure 14). The HV cables are labeled with the same numbering [marking is made with 2, 3, and 4 holes in a kapton foil around the cables]. The correspondence of the numbering to the Scienta power supplies is as follows:

- No. 2 – MCP Front
- No. 3 – MCP Back
- No. 4 – Screen

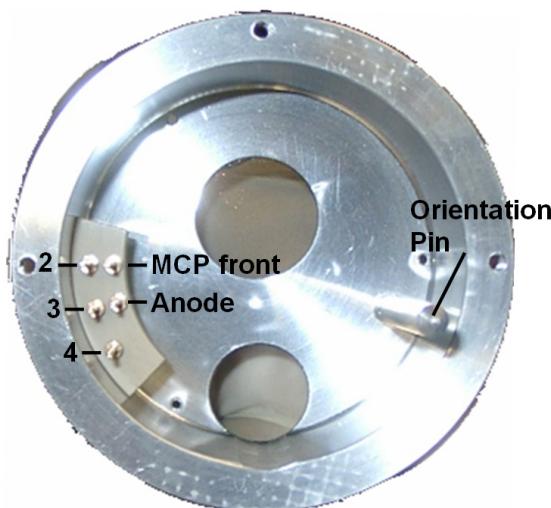
The MCP front and the MCP back voltage are used to supply the delayline detector. The Screen voltage is not used. The corresponding pin no. 4 on the connection port is just used to hold the third HV cable in a defined and isolated position.

The pin no. 2 and no. 3 in the outer row are directly connected their neighbor pin in the inner row. The correspondence is as follows:

- Outer pin no. 2 is connected to inner pin named “MCP Front”
- Outer pin no. 3 is connected to inner pin named “Anode”
- Outer pin no. 4 has no connection to the DLD

The two pins in the inner row are used to connect the delayline detector, which is mounted on part B. For this the DLD carries two sockets fitting to the two pins [see Figure 14]. The connection is established automatically, if part B is mounted carefully in the correct orientation.

## Part A



## Part B

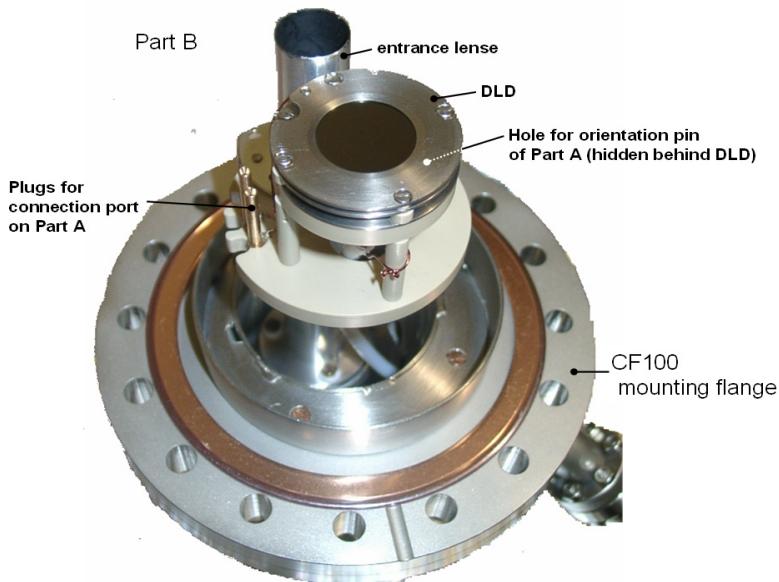
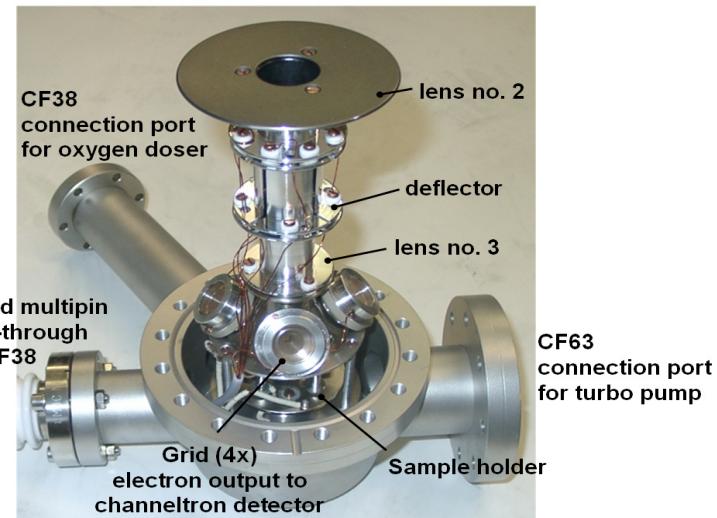


Figure 14: Part A and B of HV SPLEED/ DLD Combination

Part B carries the delayline detector as well as the entrance lens [EL], lens no. 4 and lens no. 5 of the electrostatic lens system. The high voltage connection of lens no. 4 and 5 is done via two 10kV SHV feed-throughs on the side of part B. The corresponding naming (4 or 5) is written directly onto the feed-through, for a correct identification. The entrance lens [EL] is connected internally directly to the herzog potential of the analyzer.

Part C is the bottom part of the SPLEED detector. It holds the lenses no. 2 and 3, the deflector as well as the sample holder with an integrated heating system and the mounting ports for the channeltron detectors. All parts are connected to a 10fold high voltage multipin feed-through. The pin-out is given in the following chapter. Figure 15 give the naming, the position and the orientation of different internal parts of Part C.

## Part C (image)



## Part C (schematic)

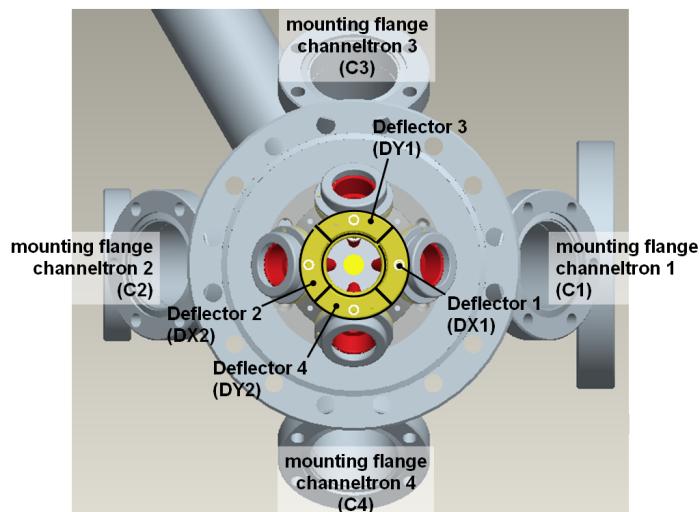


Figure 15: Part C of HV SPLEED/ DLD Combination; side view and top view [schematic].

### 5.3 HV SPLEED Detector – Connection Ports

The HV SPLEED detector carries two 10 kV SHV feed-throughs on part B for lens elements L4 and L5, as well as a high voltage multipin feed-through on part C for power supply of lens elements L2 and L3, the deflector elements DX1 – DY2, the filament/ Wehnelt, the sample potential and the grid potential [retarding grids in front of the channeltrons]. The pin out of the feed-throughs is given in Figure 16.



pin no./ part/ Marking SPLEED Controller Output

4	lens 4	[L4] [4: marking feed-through]
5	lens 5	[L5] [5: marking feed-through]



pin no./ part/ Marking SPLEED Controller Output

1	lens 3	[L3]
2	deflector 1	[DX1]
3	deflector 2	[DX2]
4	grid	[GRID]
5	sample	[CRY.S.]
6	deflector 4	[DY2]
7	deflector 3	[DY1]
8	lens 2	[L2]
9	filament	[FIL]
10	filament + Wehnelt	[FIL+]

Figure 16: Connection ports for SPLEED detector a) 10kV SHV feed-throughs in part B and b) multipin feed-through in part C.



Do not disconnect single high voltage cables from the SPLEED detector as long as high voltage is applied. This will lead to sparks which can damage the detector.

## 5.4 Channeltron – Connection Ports on Feed-Through

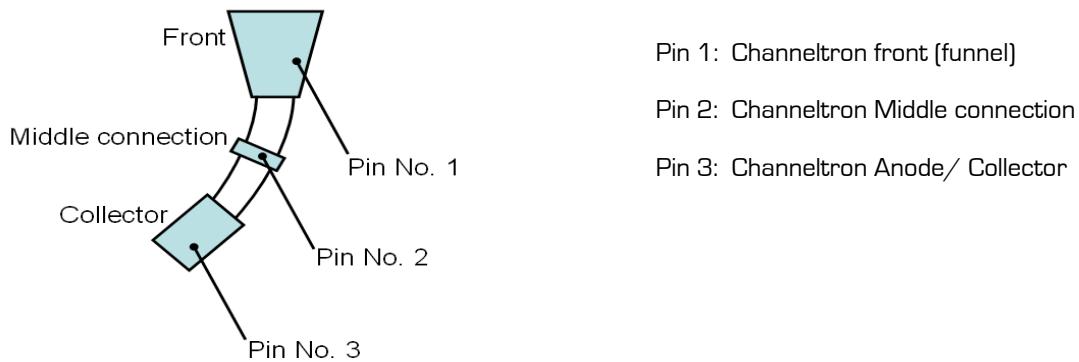


Figure 17: Relation between connecting point of channeltron and numbering of SHV feed-through.

In the HAXPES mode of operation the channeltron front is grounded by a termination/ grounding plug.

## 5.5 Delayline Detector - Vacuum Wiring

The delayline detector consists of a detection area, defined by the detector cover, the MCP holders and the detector anode. The detector anode consists of two meander structured delaylines [named x and y], which are placed above each other [electrically isolated] and are oriented perpendicular to each other. The delayline in the top layer is referred to as the x meander and the delayline in the buried layer as the y meander. The y meander is orientated in the way to be sensitive along the dispersive direction of the analyzer. Figure 18 give a schematic orientation of the x and y meanders. The meander structured delaylines are close to ground potential (in respect to the high voltage of the MCPs). A pulse coupling layer is used to isolate the meander from the high voltage of the MCP stack as well as to couple pulses from the electron cloud into the meander. The MCP front (input) is electrically isolated from the housing.

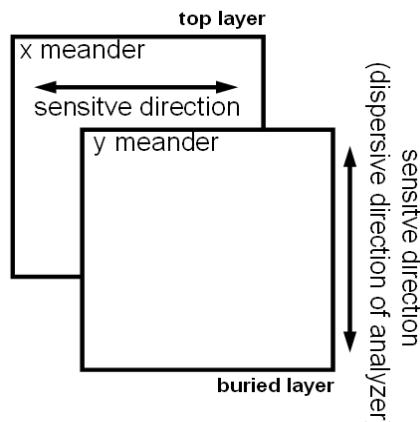


Figure 18: Schematic orientation and naming of the two-meander structured delaylines.

Signal readout is done via two readout lines (named 1 and 2) per meander structured. There are 4 readout lines in total for the complete detector. The naming of the single readout lines is put together of the individual naming 1 or 2 and the naming of the meander structured delaylines x or y.

## 5.6 Delayline Detector – Connection Ports

The HV SPLEED/ DLD Combination carries a CF 40 flange, which holds 4 SMB feed-throughs for signal transfer of the meander. It also carries an orientation pin for correct orientation of the ACU. The allocation of the four signal channels X1, X2, Y1 and Y2 on the “SMB flange” can be taken from Figure 19. The internal connection of the high voltage supply to the DLD is given schematically in Figure 20.



**Do not disconnect single high voltage cables from the delayline detector as long as high voltage is applied. This will lead to high voltage sparks which can damage the very sensitive detector, the MCPs and/or the analogue readout electronics seriously.**

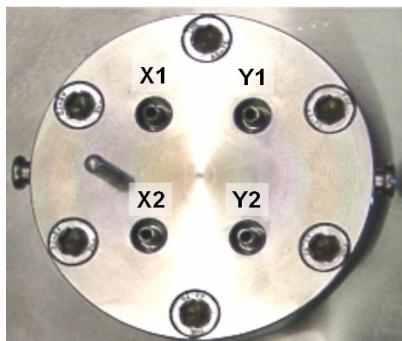


Figure 19: CF 40 “SMB” flange for signal transfer of delayline detector.

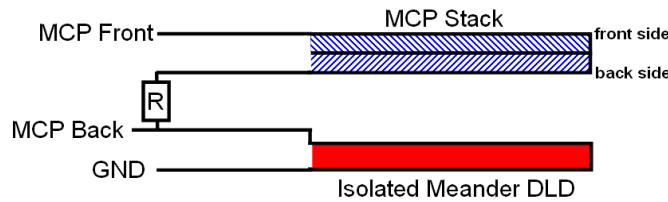


Figure 20: Internal connection of high voltage potentials (schematic).



**Note** The resistance between MCP Front and MCP Back [resistance of MCP stack incl. internal resistor] should be in the range of 130 – 250 MΩ [the exact value is given in the specification sheet of your detector].

The MCP Back voltage is always given and measured in respect to the MCP Front voltage.



**CAUTION** Check the manual for the Scienta R4000 analyzer for information about the stacking order of the high voltage power supplies for the MCP Front and MCP Back voltage. It is very important to know the reference potential of these power supplies in order do apply the correct voltage differences to the DLD.

# 6 Pulse Processing Electronics

## 6.1 Pulse Processing Electronics ACU

The pulse processing electronics ACU [Amplifier-CFD-Unit] and AU [Amplifier-Unit] hold all devices like the amplifiers, pulse shapers, and constant fraction discriminators to turn the analogue pulses from the detector into digital pulses suitable for the Time-to-Digital Converter. Pulse decoupling is either performed within the pulse processing electronics or directly in-vacuum, depending on detector type and layout. Some pulse processing electronics also contain an integrated high voltage power supply for the complete detector. This also depends on the layout of the detector as well as the pulse processing electronics.

The ACU 3.4.2 contains the amplifiers, pulse shapers and constant fraction discriminators for signal processing.



Figure 21: Layout of ACU 3.4.2

The ACU can be plugged directly onto the 4-fold SMB feed-throughs. Fasten the two clips of the ACU to the fastening bolts of the CF 40 flange to fix it to the detector. Figure 21 shows the layout of the ACU 3.4.2b.

### 6.1.1 Positions of the Discriminator Threshold Regulators

Discriminator threshold regulators of the 4 DLD channels as well as potentiometers for an additional adjustment can be found on the corresponding boards inside the ACU 3.4.2. They can be reached through the holes on the top side of the ACU housing (see Figure 22).

The adjustment of the readout electronics goes hand in hand with the detector voltage. In fact there is only a small "window" for an optimum setting of the readout electronics for a given operation voltage. Changes of the detector voltage, other than to compensate loss in the amplification of the MCP stack due to wearing out effects, will directly lead to a loss in performance of the readout electronics [artifacts within the image, increased dark count rate etc.]. The readout electronics is adjusted to its best performance to the operation voltage of the detector when delivered. A new adjustment should not be needed. The operation voltage is given in the specification sheet.

The sensitivity of the CFD is increased (threshold decreased) by turning the screw of the potentiometer clockwise and vice versa for decreasing the sensitivity of the CFD. This is only to be used under some circumstances where adjusting becomes necessary at all.



**CAUTION** The readout electronics is adjusted to its best performance to the operation voltage of the detector when delivered. Do not change the adjustment, without contacting Surface Concept before.

Changing the adjustment can easily end up with a status, where a readjustment must be made by Surface Concept.

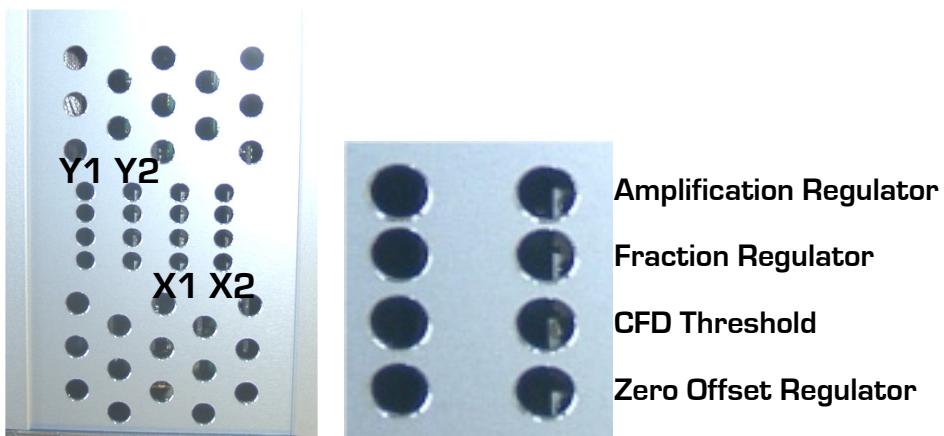


Figure 22: Labeling of discriminator threshold and amplification regulators.

## 7

# Time-to-Digital-Converter (TDC)

## 7.1 Schematic Description of the USB2.0-TDC

The USB2.0-TDC series combines the excellent performance of the GPX TDC chip [ACAM GmbH] with a high speed USB interface, either in the design with a single GPX chip (USB2.0-TDC) or with two GPX chips (Double USB2.0-TDC) operated in I-mode or with a single GPX chip (Dual Channel USB2.0-TDC) or with two GPX chips (High Resolution USB2.0-TDC/ Quad Channel USB2.0-TDC) operated in R-mode.

A field programmable gate array (FPGA) enables comfortable setups and a variable data stream handling from the TDC via USB 2.0.

The main delayline detector and segment readout (optional device) functionality is permanently programmed. A complex FIFO design makes data losses almost impossible. The user DLL controls the data handling and streaming for the user. In this light, the following brief description about the internal structure of the measurement unit is only informative:

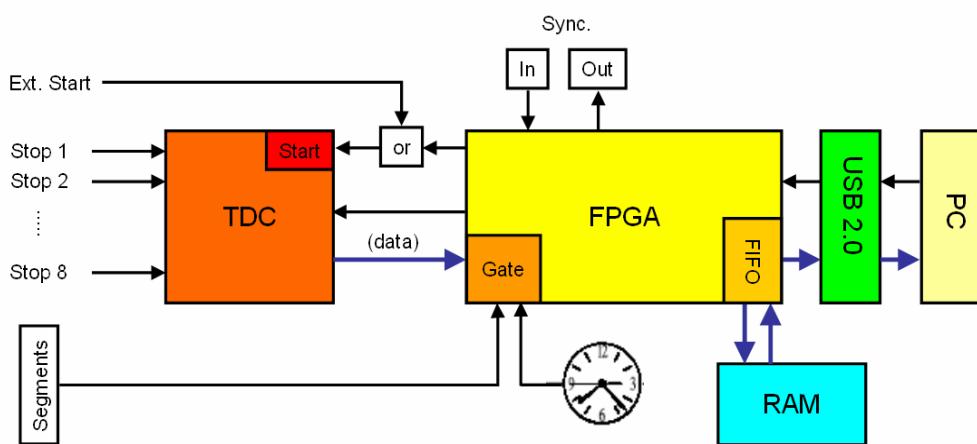


Figure 23: Schematic sketch of TDC functioning

Arrival times of pulses on the stop inputs are measured by the TDC with respect to either an internal reference start signal, provided by the FPGA, or an external start signal. Data from the segments are read out directly by the FPGA. The measurement dwell times for data from the TDC as well as from the segments are settled within the FPGA by a quartz stabilized time gate in an interval from 1 ms to 1193 h. The synchronization pulses for the external acquisition start (Sync. In) is fed directly into the FPGA, controlling the acquisition process. The FPGA also sends out the synchronization pulse for marking the end of an acquisition (Sync. Out). The TDC data streaming can be performed as measured (RawData mode) or including a DLD

specific data pre-conditioning (Pair mode). This concerns a channel pairing and a pair result arithmetic, a modulo arithmetic and many more. Communication to and from the PC is achieved via a USB 2.0 interface. Data streaming via the USB 2.0 interface is provided without losses using a large memory buffer within the device.

## 7.2 Basic operation modes of the GPX TDC chip

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### 7.2.1 I-Mode (USB2.0-TDC/ Double USB2.0-TDC )

- 8 stop channels with typically 81 ps digital time bin resolution
- 1 start channel
- Input level: TTL or LVTTL
- Start retrigger rate [max.]: 7 MHz
- Measurement range: 0 ns – 10.6 µs in start-stop operation
- Dynamic range:  $2^{17}$
- 32-fold multi-hit capability
- Trigger to rising or falling edge
- Endless measurement range by internal retrigger of START
- 10 MHz continuous rate per channel
- 40 MHz continuous rate per chip

### 7.2.2 R-Mode (Dual Channel/ Quad Channel USB2.0-TDC)

- 2 stop channels with typically 27 ps digital time bin resolution
- 1 start channel
- Input level: differential LVPECL
- Start retrigger rate [max.]: 7 MHz
- Measurement range: 0 ns – 40 µs in start-stop operation
- Dynamic range:  $2^{19}$
- 32-fold multi-hit capability
- Trigger to rising or falling edge
- 40 MHz continuous rate per channel
- 40 MHz continuous rate per chip

## 7.3 Layout of the Quad Channel USB2.0-TDC



Figure 24: Layout of the Quad Channel USB2.0-TDC

### 7.3.1 TDC Inputs (Stop + Start)

The USB2.0-TDC provides a HDMI socket for the signal input (stop inputs) from the ACU. The TDC inputs are laid out for PECL levels (R-mode operation mode).

An external start signal must be provided to the TDC for time resolved measurements. Apply standard TTL signals to the "TTL Start" input (BNC socket).



**Note** The USB2.0-TDCs do not work with start signals of frequencies larger than 7 MHz. Therefore larger start pulse frequencies must be divided down with an appropriate frequency divider (e.g. divider with factor of 16 for 80 MHz start pulse frequency).

The temporal resolution is influenced mainly by the quality of the start signal while the TDC measures the time in a leading edge determination. Therefore, if the start signal is varying in time, one needs to process it by means of a constant-fraction-discriminator or similar external electronics components.

### 7.3.2 Trigger Synchronization IN/OUT

Image acquisition of the DLD can be synchronized to an external trigger signal. To do so, the trigger signal must be applied as TTL signal to the "SYNC IN" BNC socket of the USB2.0-TDC. Additionally the corresponding software switch "ext\_trigger" must be set to "1" in the delayline.dll (see your corresponding software manual for further details). Otherwise the TDC ignores external trigger signals. The TDC provides a TTL signal on the "SYNC OUT" BNC socket after each acquisition. This function is always activated. No software switch must be set.

### 7.3.3 Line Input

Electrical Input (LINE): 85 V – 260 V, 50/60 Hz  
Power: 65 Watt (max.)  
Fuse: 1x T 1.6 A

## 7.4 Interface (PC) and Software

---

All operation functions of the USB2.0-TDCs for data readout of the detector package are encapsulated in the dynamic linked library "delayline.dll". Data processing and presentation on the PC is realized by an end-user software (e.g. GUI). See the corresponding software manuals for detailed information on the software package and the DLL interface.

## 8 DLD - Principle of Operation

### 8.1 Basics of Delayline Detection

A delayline detector (DLD) consists of a microchannel plate array for pulse amplification and an in-vacuum readout unit consisting of a meander structured delayline (DLD anode). Each hit position is encoded by a fast data acquisition unit, which also may detect the hit time referenced to an external clock in repetitive (stroboscopic) experiments.

#### Principle of the 2-D(x,t) delayline operation

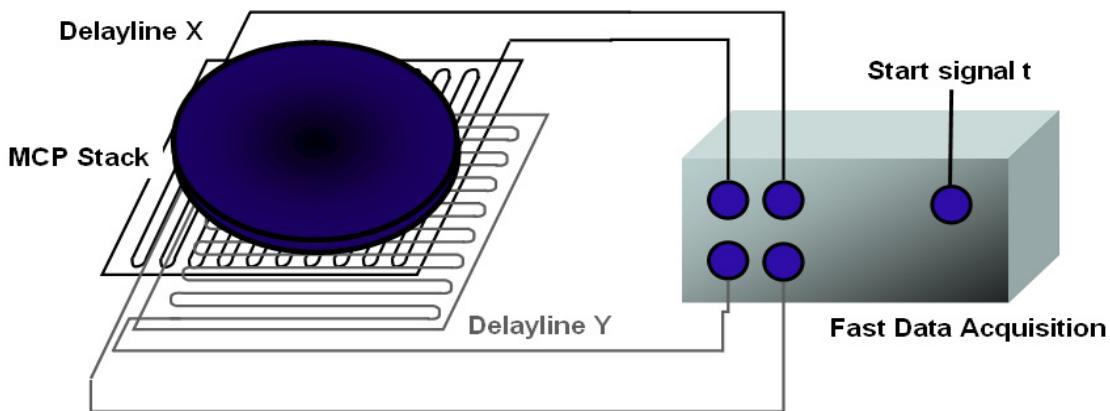


Figure 25: Schematic drawing of the basic assembly of a delayline detector

The DLD anode consists basically of two meander structured delaylines, the one rotated by 90° with respect to the other and both isolated from each other. The delaylines are positioned behind a Chevron microchannel plate stack, which is required to amplify incoming electrons by at least 10<sup>7</sup>. The electron cloud from the MCP stack output is drawn to the DLD meander (positive potential difference between anode and back side of MCP stack) where it induces electrical pulses in the delayline by capacitive coupling. The pulses are traveling to the both ends of the meander within a time determined by the hitting position. The average time at both ends of the meander relative to an external repetitive clock generates the time coordinate if required.

Delayline detectors are single counting devices; therefore the complete device works linearly even at extremely low numbers of incoming electrons.

The detection principle limits the maximum detectable count rates at least due to the maximum delay of the meanders. Currently, the main limitation is given by the appearance of multi-hit events, which can only be resolved up to a certain degree. The maximum count rate in the fourfold coincidence measurement can be up to  $3.0 \times 10^6$  counts per second.

## 8.2 Basic Operational Modes of the Delayline Detector

### 8.2.1 2D(x, y) Area Detection

The area detection mode is the normal operation mode of the delayline detector. The arrival times of pulses per event at the ends of the detector meanders are subtracted in order to determine a position in x and y [x: tx1-tx2; y: ty1-ty2]. The 4 TDC stop signals are grouped internally in pairs to form x and y. All DLD software adjustments are done by the end-user software according to the user's chosen parameters.

### 8.2.2 3D(x, y, t) Time Resolved Imaging

The delayline detector may measure all events in temporal reference to an external clock. For this mode, the user needs to start the USB2.0-TDC by an external clock, providing a low jitter LVTTL (or TTL) signal to the start input of the TDC.

Time measurements are performed by summing up the arrival times of pulses at the end of the meanders, i.e. the same results which are used to determine positions for each event are summed. It is possible to sum only tx1 and tx2 [tsumx] or ty1 and ty2 [tsumy]. Because both sums should carry the same temporal information of a time related experiment, the total sum t[DLD] of all four time measurements [tx1, tx2, ty1, ty2] may be a good choice as well. The results of all these time sums correspond to  $t[\text{sum}] = t[\text{offset}] + n * [t[\text{hit}] - t[\text{reference}]]$ , where  $[t[\text{hit}] - t[\text{reference}]]$  is the interesting time (e.g. ToF) in a given experiment, n is the number of summed time results (2 or 4 results), and  $t[\text{offset}]$  is a device related constant, which depends on cable lengths, electronics propagation times, experiments setup etc.. Therefore, it is possible to completely determine position and time of each event from only 4 precise time measurements.

The software may group all measured time sums in plain 1D time histograms, which are valid for the chosen region of interest (ROI). The time bin size for each readout channel x1, x2, y1 and y2 is 82ps in the I-mode. The channel width in the 1D histogram is 41ps for the tsumx and tsumy histograms as well as 20.5ps for the total t[DLD] histogram.

The time bin size for the readout channels in the R-mode is 27ps and the channel width in the 1D histogram is 13.5ps for the tsumx and tsumy histograms and 6.75ps for the total t[DLD] histogram. Due to the calculation of the tsums and t[DLD], the time axis is expanded virtually (simplified expression). The t[DLD] signature can be used in order to setup the regions of interest in time for measurements of time resolved images, the software is able to sample 3D histograms as image stacks in time, where each image corresponds to one time bin of the total time histogram.

## 8.3 Data Acquisition

In the delayline detector, each end of each meander is connected to a fast amplifier followed by a constant fraction discriminator (CFD) for pulse shaping. They are encapsulated inside the pulse processing electronics (ACU = Amplifier-CFD-Unit or AU = Amplifier-Unit). The main function of the CFD is digital pulse discrimination, ideally without any time-walk even at varying pulse heights. A time-to-digital converter (TDC) behind these

chains serves as stop-watch for arrival time measurements. The measurement results, in terms of differences and sums are fed into the PC via a USB 2.0 interface and are completed to 2D images (with or without time stamps) by the histogram module of the data acquisition DLL. Data processing and presentation on the PC is achieved with the GUI software. See the corresponding software manuals for detailed information on the software package.

## 8.4 Working with the DLD – Important details

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The DLD is a counting system that works in a laterally resolving sense by detecting four pulses from the four ends of the delayline meanders in fourfold coincidence. It only works correctly within a certain range of the supply voltage. The MCP voltage has to exceed an operation threshold for the detector otherwise the pulse detection is not possible. This is due to the induced pulses on the delayline which have to reach a certain amplitude to be detected by the electronics, independent on the intensity of the electron source [e.g. mercury lamp]. On the other hand, if the MCP voltage and/or the intensity of the electron source are too high, the detector overloads and again pulse detection is not possible. Saturation effects of the MCPs limit the amount of electrons provided by single pulses. An intensity increase of the electron source leads to an increased number of hits on the MCP. The current per bunch and therefore the amplitude of the pulses decreases. There are two kinds of overloads: local and global. A local overload (locally high intensity on the MCP) leads to no count rate within this local area and to an absolute "black spot" in the images. An intensity too high and homogeneously distributed over the whole MCP first leads to diffuse images and with further increasing intensity to randomly distributed artificial structures up to no count rate at all (global overload). The explanation for the effects for a local overload is a pulse amplitude that is too low to be detected by the electronics. The explanation for the global overload effects is mainly the loss of the fourfold coincidence condition of an incoming event and a fitting fourfold coincidence of random pulses, respectively. High intensity on the MCPs always leads to a significant pressure increase. Therefore an observed pressure increase can always be taken as an indicator for an overload of the detector, when problems with the functionality of the DLD occur.

 **Note** It is easy to mistake an overload for no signal at all. To distinguish between these two, check the pressure. A pressure increase indicates an overload.

The DLD has been calibrated for an optimized MCP voltage and it is strongly advised to use this optimized voltage value for operation. It is given in the specification sheet and also in the commissioning sheet, provided with your shipment from SPECS. A change of the MCP voltage can lead to artifacts within the images. The MCP voltage should only be increased to compensate a decrease in amplification of the MCP stack due to wearing-out.

## 9

# HV SPLEED/DLD Operation

### 9.1 Bake Out Procedure

**CAUTION**

The maximum allowed temperature for the detector is 150°C. Do not exceed this temperature.

- Windows and feed-throughs should be wrapped with aluminum foil, to protect them from rapid temperature changes.
- The use of heating tapes and jackets is not recommended, due to danger of local overheating.
- Do not remove the bake out hood or blankets until the entire system has thoroughly cooled off.
- Do not operate the detector before the temperature has returned to ambient conditions.

**CAUTION**

After a bake out, the detector needs at least one day (24 hours and more) to cool down. Even if the detector housing feels just warm, any internal parts seated on insulators (e.g. the lenses or channeltrons) may still be too hot for safe operation. It is imperative that all users be informed of this issue and take the necessary precaution to ensure proper device operation.

### 9.2 Getting Started

Be sure, that the vacuum pressure at the detector is remarkably below  $10^{-8}$  mbar. Finish the complete cabling as described in section 3 before the high voltage is turned on. Turn off the high voltage before performing any changes of the cabling.

## 9.3 Turning on the High Voltage



High voltage sparks may seriously damage the detector. Observe the chamber pressure carefully every time the high voltage is turned on. Switch off the high voltage immediately in case of a significant pressure rise.

### 9.3.1 "Run-In" Procedure for base voltage (analyzer and HV SPLEED/DLD Combination)



Read the following section very carefully and respect all warnings given there. Do also read the manual of the Scienta analyzer and about the procedure of applying the high voltage.

To reach stable conditions during measurements at high voltages, it is important to go through the Run-In procedure for the base voltage of the analyzer and the HV SPLEED/DLD combination (e.g. the Herzog potential), before starting the actual measurements. The Run-In procedure has to be done after each new installation of the detector and after each venting of the system.

The first time the detector is used or after the system has been vented, the detector and analyzer base voltage must be ramped very slowly above the final operation value (e.g. 10 kV if operation will take place at 8 kV).

Before starting the Run-In procedure make sure that the ACU 3.4.2 has been removed and that the shortcut plug (see Figure 26) has been connected to the 4-fold SMB feed-through.



Do not start the Run-In procedure without replacing the ACU by the shortcut plug. Operating the Run-In procedure with connected ACU can easily damage the preamplifiers and CFDs.



Operating the Run-In procedure without any termination/grounding of the SMB plugs on the 4-fold SMB feed-through will lead to high voltage potential on the inner pins of the SMBs and to sparking within the feed-through as well as to fatal high voltage sparks, when touching the SMB plugs.

**DO NOT APPLY ANY VOLTAGE TO THE DLD WITHOUT THE ACU OR THE GROUNDING PLUG CONNECTED TO THE 4-fold SMB FEED-THROUGH.**

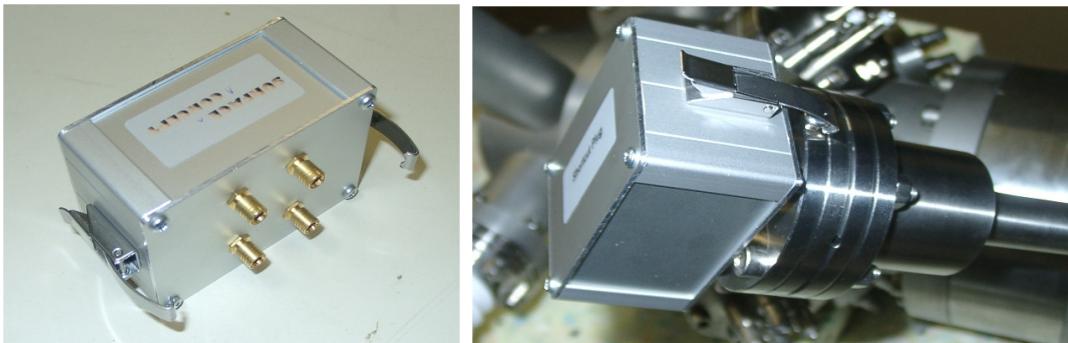


Figure 26: Shortcut Plug for 4-fold SMB feed-through.

Increase the analyzer's base voltage slowly and stepwise with around 4 kV per hour. The final voltage should be approx. 2 kV higher than the voltage you want to use for later measurements (e.g. 10 kV when measurements should be performed at 8 kV later on). All other voltages, which are applied in respect to the base voltage (e.g. MCP Front and MCP Back voltage of the DLD) are not being turned up.



- Do only increase the base voltage and voltages, which are not applied in respect to the base voltage. Check if this applies for the electrostatic lens system.**
- Do not increase additional voltages, which are applied in respect to the base voltage (this could be for example the MCP Front and Back voltage – check this).**
- Do not exceed a base voltage of 10 kV.**

Keep the final base voltage **for a couple of hours** before turning down the voltage again.

During the complete time of the procedure sparking can and most likely will occur. Up to a certain degree sparking is part of the Run-In procedure and does not state any malfunction of the detector.

Watch the vacuum pressure during this procedure. A sudden pressure increase is a very good indicator for sparking.



- Sparking should only occur random and with a larger time distance between single sparks and it must stop after some time (a couple of hours). If sparking occurs regular and/ or too often (once every few minutes) and/ or does not stop after some time, there might be a problem within the detector. Turn down the high voltage immediately and contact SURFACE CONCEPT.**

Do not finish the Run-In procedure as long as sparking occurs.

After finishing the Run-In procedure, turn off the complete system (detector and analyzer). Wait approx. 5 – 10 minutes before removing the grounding plug. Connect the ACU to the detector.

Now the measurement can be started with the standard start procedure, as described below.

### 9.3.2 Standard Start Procedure

The following procedure is used for all later operation starts, when the "Run-In" procedure has finished successfully and/ or the detector has already been operated in vacuum under high voltage and has not been vented in between.

Turn on the analyzers base voltages slowly. Turn stepwise within a few minutes to the operation voltage. Watch the vacuum pressure during this procedure. Turn back the voltages immediately, if an unusual

increase is observed in the pressure.

After reaching the final base voltage under stable conditions, increase the additional voltages for the electrostatic lens system and or the MCP Front and MCP Back voltage of the DLD.

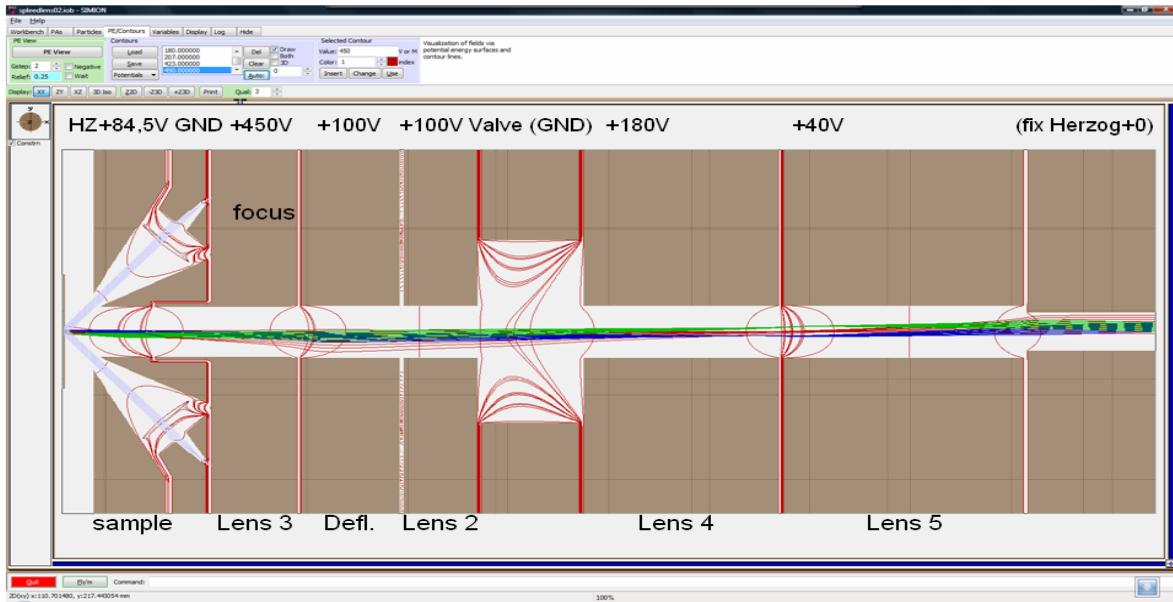
Both voltages, MCP Front and MCP Back, must be ramped parallel to their individual operation values (see the specification sheet for the exact operation voltage).

The base potential of the analyzer and HV SPLEED/ DLD combination must also be applied to the electrostatic lens system. After ramping the base potential to its operation value, one can also turn up the voltages for the electrostatic lens system. The voltages of the electrostatic lens system should also be ramped parallel until reaching their operation voltages. Operation voltages for the different elements of the electrostatic lens system are given in Figure 27 for pass energies of 20 eV and 100 eV.



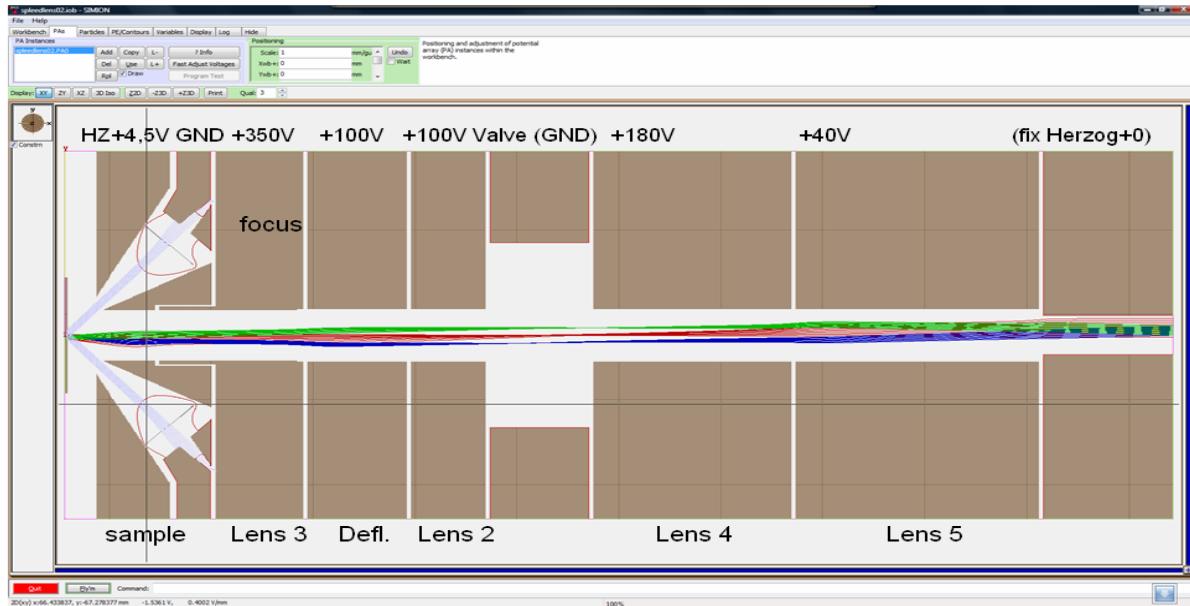
**CAUTION** The voltages given in Figure 27 are in respect to the Herzog potential.

## pass energy: 20eV



Set grid potential to + 20 V to compress 24,5 eV secondary electrons.

## pass energy: 100eV



Set grid potential to + 20 V to compress 24,5 eV secondary electrons.

Figure 27: Operation voltages for the electrostatic lens elements for pass energies of 20 eV and 100 eV.  
Note: The operation voltages are given in respect to the Herzog potential.

# 10 Microchannel Plate (MCP)



**Contact SURFACE CONCEPT before performing a replacement.**

**Note**

Take care to note the orientation of the MCPs. The channels in the MCPs include a certain angle against the surface normal to the plate and the MCPs must be mounted in a chevron or z-stack configuration (depending on no. of MCPs). All parts of the detector, especially the MCPs should be handled with great care. The MCP surfaces are very sensitive and should never be touched or scratched.

## 10.1 Storage

Because of their structure and the nature of the materials used in manufacture, care must be taken when handling or operating MCPs. The following precautions are strongly recommended:

- The most effective long-term storage environment for an MCP is an oil-free vacuum.

## 10.2 Handling

- Shipping containers should be opened only under class 100 Laminar flow cleanroom conditions.
- Personnel should always wear clean, talc-free, class 100 clean-room compatible, vinyl gloves when handling MCPs. No physical object should come into contact with the active area of the wafer. The MCP should be handled by its rims, there is no solid glass border! Use clean degassed tools fabricated from stainless steel, Teflon™ or other ultra-high vacuum-compatible materials. Handling MCPs should be limited to trained, experienced personnel.
- MCPs without solid glass border should be handled very carefully with great care taken to contact the outer edges of the plate only.
- The MCP should be protected from exposure to particle contamination. Particles which become affixed to the plate can be removed by using a very pure and low pressure air flow such as from a clean rubber bellows.
- The MCP should be mounted only in fixtures designed for this purpose. Careful note should be taken of electrical potentials involved.



**Voltages must not be applied to the device while at atmospheric pressure. The pressure should be  $1 \times 10^{-6}$  mbar or lower at the microchannel plate before applying voltage. Otherwise, damaging ion feedback or electrical breakdown will occur.**

## 10.3 Operation

- A dry-pumped or well-trapped/diffusion-pumped operating environment is desirable. A poor vacuum environment will most likely shorten MCP life or change MCP operating characteristics.
- A pressure of  $1 \times 10^{-6}$  mbar or better is preferred. Higher pressure can result in high background noise due to ion feedback.
- When a satisfactory vacuum has been achieved, voltages may be applied. It is recommended that this is done slowly and carefully. If fluctuations do appear, damage or contamination should be suspected and the voltage should be turned off. The assembly should then be inspected before proceeding.
- Voltage across single MCPs should not exceed the max. voltage given in Table 2 and in the specification sheet of the detector. Higher potentials may result in irreversible damage.
- MCPs can be degraded by exposure to various types of hydrocarbon materials which raise the work function of the surface, causing gain degradation.
- Operation at higher temperatures ( $> 50^{\circ}\text{C}$ ) will cause gain degradation.

Thickness	1.0 mm
Outer diameter	24.7 mm
Active diameter	18 mm
L/D [channel length / channel diameter]	40 : 1
Resistance [single MCP]	15 – 125 MΩms
Max. voltage [single MCP]	1000 V
Max. Gain @ 1000 V	$\geq 1 \cdot 10^5$ minimum
Pore size [diameter]	25 µm
Center – to – Center Spacing	32 µm
Bias angle of channels	$12^{\circ} \pm 1^{\circ}$
Quality level	detection quality, extended dynamic range
Open area ratio	55 % minimum
Operating pressure	$< 1 \cdot 10^{-6}$ mbar

Table 2: MCP Specifications

# 11 Technical Data

**HV SPLEED/ DLD Combination General:**

HV capability:	Up to 10 kV
Max. bake-out temperature:	150°C
Pressure range for operation:	< 10 <sup>-8</sup> mbar
Max. voltage for each channeltron detector:	3000 V

**Delayline detector DLD1818:**

Active area of the DLD 1818:	Ø 22 mm round
Operation voltage at detector:	see specification sheet
Max. voltage difference between MCP back and anode:	internally connected, not adjustable from outside

**Amplifier – CFD – Unit ACU 3.4.2:**

No. of Amplifier-CFD channels:	4
Bandwidth of DLD amplifiers:	1.6 GHz
CFD working frequency:	200 MHz
CFD jitter (max.):	20ps
CFD walk (typ.):	< 50 ps (while ambient temperature varies less than 5 K)

**Quad Channel USB2.0-TDC (Two GPX chips – R mode):**

- Differential PECL (LVPECL) inputs, common start input usable as reset of the internal clock resolution adjust mode: quartz-accurate, adjustable resolution, insensitive to temperature variations, adjustable via software (no calibration necessary)
- 4 stop channels with 27.4 ps digital time bin resolution
- 1 start channel
- Start retrigger rate (max): 9 MHz
- Measurement range 0 ns – 40 µs in start-stop operation
- Dynamic range: 2<sup>19</sup>
- Trigger to rising or falling edge
- All channels provide precisely an equal resolution
- No minimum time limit for hits at different channels
- 5.5 ns pulse-pair resolution on one channel and 0 ns between two channels
- 32-fold multi-hit capability = 182 MHz peak rate
- 80 MHz internal data acquisition rate
- Counter line frequency limit of 35 MHz per channel

**Channeltron Specification:**

<b>Channeltron on Flange 1</b>	
Operating Voltage	ca. 1900 V [new channeltron] – ca. 3000 V [very old channeltron]
Gain @ Voltage	$1.10 \cdot 10^8$ minimum @ 2440 V
Operating pressure	$< 1 \cdot 10^{-6}$ mbar
<b>Channeltron on Flange 2</b>	
Operating Voltage	ca. 1900 V [new channeltron] – ca. 3000 V [very old channeltron]
Gain @ Voltage	$1.10 \cdot 10^8$ minimum @ 2200 V
Operating pressure	$< 1 \cdot 10^{-6}$ mbar
<b>Channeltron on Flange 3</b>	
Operating Voltage	ca. 1900 V [new channeltron] – ca. 3000 V [very old channeltron]
Gain	$1.10 \cdot 10^8$ minimum @ 2270 V
Operating pressure	$< 1 \cdot 10^{-6}$ mbar
<b>Channeltron on Flange 4</b>	
Operating Voltage	ca. 1900 V [new channeltron] – ca. 3000 V [very old channeltron]
Gain	$1.10 \cdot 10^8$ minimum @ 2360 V
Operating pressure	$< 1 \cdot 10^{-6}$ mbar

## 12 Information for Replacement

### Replacement of Channeltrons:

The replacement of the channeltrons is fairly easy:

- Dismount the complete CF40 flange holding the channeltron to be replaced.
- Open the screws on the bottom side (feed-through side) of the channeltron cover.
- Remove the channeltron cover **carefully**.
- The channeltron is fasten to a mounting plate by 3 screws. Open these three screws.
- Pull up the channeltron carefully and just little bit.
- Disconnect the 3 gold plugs from the pins of the channeltron.
- Remove the old channeltron and place in a new one.
- **CAUTION! Check the new channeltron for a fixed grounding connection of the front part. Remove it, in case there is such a fixed grounding connection. Compare the new channeltron with the old one.**
- Place in the new channeltron and connect the three gold pins. **CAUTION! Check for the correct connection of pins. Compare with Figure 17.**
- Fasten the channeltron to the mounting plate and mount the channeltron cover.
- Take care that the channeltron is positioned centered in respect to the hole in the channeltron cover.
- Mount the CF40 flange with the new channeltron back to the SPLEED chamber.

### Replacement of Crystal Heater Filament

The actual description for the replacement of the filament of the crystal heater must be taken from the Focus manual. Follow you find some important notes for uninstalling the sample holder with integrated heater from the HV SPLEED/ DLD Combination.

- Dismount Part C form the HV SPLEED/DLD Combination.
- Remove all four channeltrons. Otherwise they will be damaged when removing the inner part of Part C .
- Open the bottom CF 100 flange of Part C and take off the upper part **carefully**. This can be a bit difficult due to the  $\mu$ -metal which is quiet close to the inner wall of the housing.
- Open the flange of the 10 pin HV Feed-through **carefully** and disconnect **only** the pins no. 9 + 10, if possible.
- Unscrew the big mounting plate from its aluminum standoffs. It is positioned above the sample holder and carries the ring with the grids as well as the complete setup of the lower part of the electrostatic lens system. Put the complete part to the side **carefully**.
- Remove the aluminum standoffs as well as the screw, which are holding the sample holder/crystal heater unit.
- Now the sample holder can be removed **carefully**.
- Check the Focus manual on how to replace the filament of the heater.

- Mount back the sample holder, after the replacement has been finished.

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## EU Declaration of Conformity

Manufacturer **Surface Concept GmbH**  
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Product details Delayline Detector DLD 1D, 2D, 3D, Quadrant in all variations and sizes to be operated with ACU and USB2.0-TDC in all versions and subversions.

The above named products comply with the following European directive:

89/336/EEC Electromagnetic Compatibility Directive, amended by 91/263/ EEC and 92/31/ EEC and 93/68/EEC  
73/23/EEC Low Voltage Equipment Directive, amended by 93/68/EEC

The compliance of the above named product to which this declaration relates are in conformity with the following standards or other normative documents where relevant:

EN 50081-1 (3/94) Electromagnetic Compatibility Generic Emission Standard-Part 1:  
EN50082-1 (3/94) Electromagnetic Compatibility  
EN 61010-1 (2001) Safety Requirements for Electrical Equipment for Measurement,  
Control and Laboratory Use

For and on behalf of **Surface Concept GmbH**

Mainz, 15.09.2009..... Legal signature.....

**SURFACE**  
**CONCEPT**  
Surface Concept GmbH,  
Staudingerweg 7, 55128 Mainz  
(Pasqual Bernhard, product manager)

This declaration does not represent a commitment to features or capabilities of the instrument. The safety notes and regulations given in the product related documentation must be observed at all times.