AS3993

UHF RFID Single Chip Reader EPC Class1 Gen2 Compatible

General Description

The AS3993 is an EPC Class 1 Gen 2 RFID reader IC which implements all the relevant protocols, including ISO 18000-6C, the ISO 29143 air-interface protocol for mobile RFID interrogators, and ISO 18000-6A/B (for operation in direct mode). Highly integrated – it includes an on-chip VCO and a power amplifier – it offers a complete set of RFID features including Dense Reader Mode functionality and support for frequency-hopping, low-level transmission coding, low-level decode, data framing and CRC checking.

The AS3993 operates at very low power, which means that this advanced RFID reader IC is suitable for use in portable and battery-powered equipment such as mobile phones.

Packaged in a 7x7 mm QFN outline, the IC benefits from fabrication process technology unique to **ams** to deliver very high sensitivity and providing high immunity to the effects of antenna reflections and self-jamming. This is critical in mobile and embedded applications, in which antenna design is often compromised by cost or size constraints. High sensitivity enables end-product designs to achieve their required read range while using a simpler and cheaper antenna, thus reducing system bill-of-materials cost.

AS3993 requires only an external simple 8-bit microcontroller to create a complete RFID reader system. AS3993 is highly integrated and implements the RFID functions on chip thus eliminating a need for a complex RFID co-processor.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3993, UHF RFID Single Chip Reader EPC Class1 Gen2 Compatible are listed below:

Figure 1:
Added Value of Using AS3993

Benefits	Features

• Optimized for battery operation	• Supply voltage range 3.0V to 3.6V
	  • Limited operation possible down to 2.7V
	  • Maximum PA supply voltage 4.3V
	  • Peripheral I/O supply range 1.65V to 5.5V

• ISO 18000-6C and ISO 29143 implemented in HW	• Protocol support for:
	  • ISO 18000-6C (EPC Class1 Gen2)
	  • ISO 29143 (Air interface for mobile RFID)
	  • ISO 18000-6A/B through direct mode

• Direct mode for customized commands and future protocol extensions	
• Low coding effort and MCU requirements	
• High sensitivity	• DRM: 250 kHz and 320 kHz filters for M4 and M8
• High PSRR	• Integrated supply regulators
• World-wide shippable product	• Frequency hopping support
• Flexible modulation method	• ASK or PR-ASK modulation
• Avoidance of communication holes	• Automatic I/Q selection
• Tag movement detection support	• Phase bit for tag tracking with 8-bit linear RSSI
• Small package footprint – saving PCB area	• 48-pin QFN (7x7x0.9 mm) package
• Wide temperature range	• -40°C to 85°C

Applications

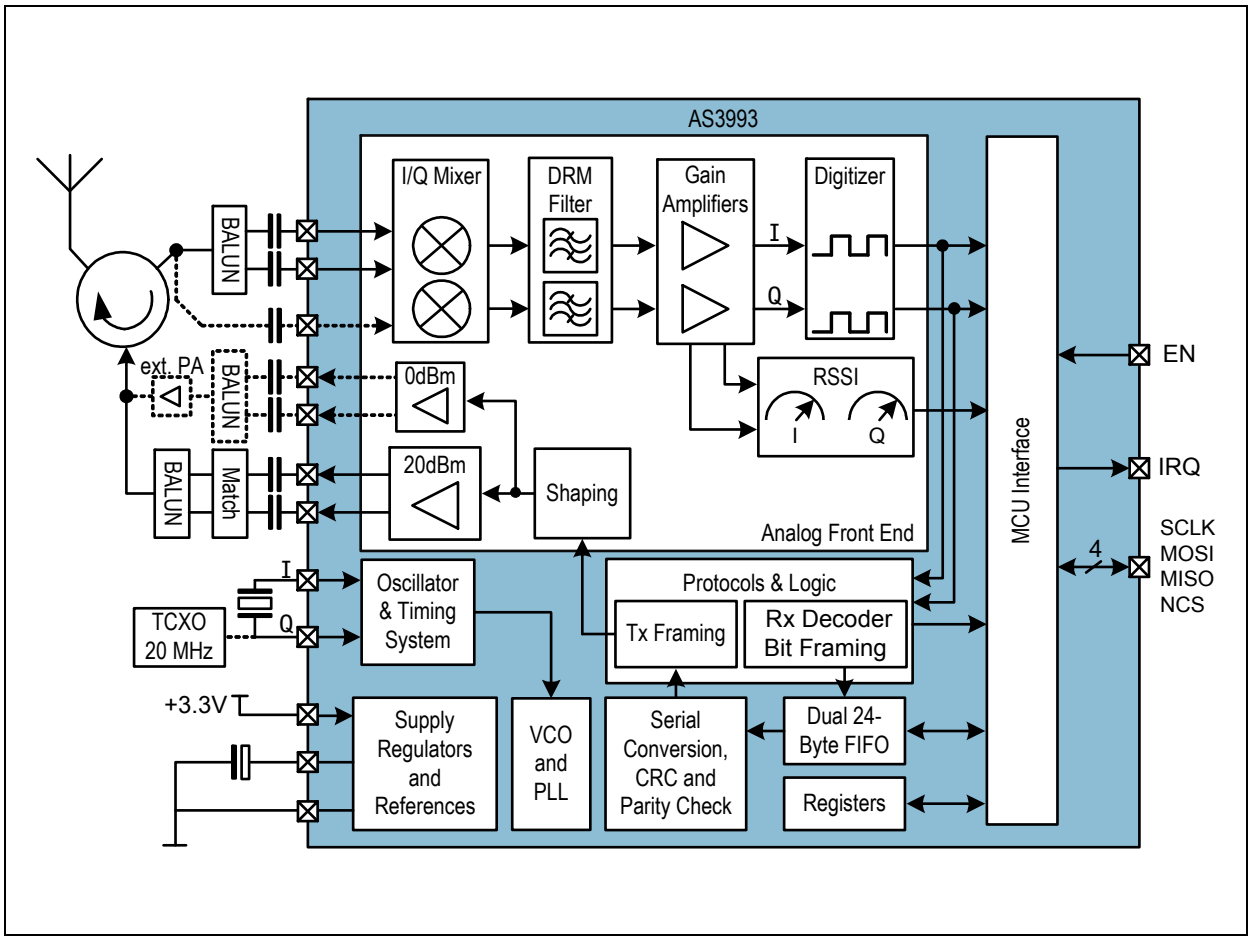
The AS3993 device is ideally suited for:

- Embedded consumer/industrial applications with cost constraints such as beverage dispensing
- Hand-held readers
- Mobile UHF RFID readers
- Battery-powered stationary readers

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS3993 Block Diagram



AS3993 Block Diagram: Basic block diagram of AS3993 reader device

Pin Assignments

The AS3993 pin assignments are described below.

Figure 3:
Pin Diagram

AS3993 Pin Assignment: This figure shows the pin assignment and location viewed from top.

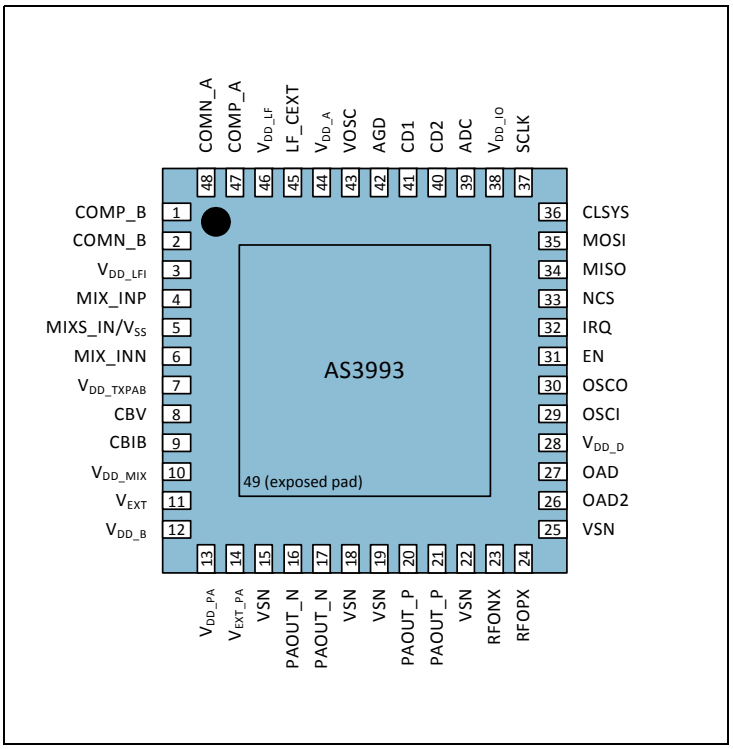


Figure 4:
Pin Description

Pin Number 48-Pin QFN	Pin Name	Pin Type	Description
1	COMP_B	Analog I/O	Internal node, connect de-coupling capacitor to V_{DD_LFI}
2	COMN_B	Analog I/O	Internal node, connect de-coupling capacitor to V_{DD_LFI}
3	V_{DD_LFI}	Supply pad	Positive supply for LF input stage, connect to V_{DD_MIX}
4	MIX_INP	Analog input	Positive differential mixer input
5	MIXS_IN/V_{SS}	Analog input	Single ended mixer input
6	MIX_INN	Analog input	Negative differential mixer input
7	V_{DD_TXPAB}	Supply pad	Bias positive supply. Connect to V_{DD_MIX}
8	CBV	Analog I/O	Internal node, connect de-coupling capacitor to V_{DD_MIX}
9	CBIB	Analog I/O	Internal node, connect de-coupling capacitor to ground
10	V_{DD_MIX}	Analog I/O	Mixer positive supply, internally regulated

Pin Number 48-Pin QFN	Pin Name	Pin Type	Description
11	V_{EXT}	Supply pad	Main positive supply input, input to regulators
12	V_{DD_B}	Analog I/O	Buffer positive supply, internally regulated
13	V_{DD_PA}	Analog I/O	PA positive supply, internally regulated
14	V_{EXT_PA}	Supply pad	PA positive supply regulator input
15	VSN	Supply pad	Negative supply
16	PAOUT_N	Analog output	Negative PA RF output
17	PAOUT_N	Analog output	Negative PA RF output
18	VSN	Supply pad	Negative supply
19	VSN	Supply pad	Negative supply
20	PAOUT_P	Analog output	Positive PA RF output
21	PAOUT_P	Analog output	Positive PA RF output
22	VSN	Supply pad	Negative supply
23	RFONX	Analog output	Low power linear negative RF output (~0dBm)
24	RFOPX	Analog output	Low power linear positive RF output (~0dBm)
25	VSN	Supply pad	Negative supply
26	OAD2	Analog I/O	Analog or digital received signal output
27	OAD	Analog I/O	Analog or digital received signal output
28	V_{DD_D}	Analog I/O	Positive supply for logic, internally regulated
29	OSCI	Analog input	Crystal oscillator input or short to ground in case external TCXO is used
30	OSCO	Analog I/O	Crystal oscillator output or external 20MHz clock input
31	EN	Digital input	Enable input
32	IRQ	Digital output	Interrupt request output
33	NCS	Digital input	Serial Peripheral Interface enable (active low)
34	MISO	Digital output / tri-state	Serial Peripheral Interface DATA output

Pin Number 48-Pin QFN	Pin Name	Pin Type	Description
35	MOSI	Digital input	Serial Peripheral Interface DATA input
36	CLSYS	Digital output	Clock Output for MCU
37	SCLK	Digital input	Serial Peripheral Interface clock
38	V_{DD_IO}	Supply pad	Positive supply for peripheral communication, connect to host positive supply.
39	ADC	Analog input	ADC input for external power detector support
40	CD2	Analog I/O	Internal node de-coupling capacitor
41	CD1	Analog I/O	Internal node de-coupling capacitor
42	AGD	Analog I/O	Analog reference voltage
43	VOSC	Analog I/O	Internal node de-coupling capacitor
44	V_{DD_A}	Analog I/O	Analog part positive supply, internally regulated
45	LF_CEXT	Analog output	PLL Loop filter
46	V_{DD_LF}	Analog I/O	Positive supply for LF processing, internally regulated
47	COMP_A	Analog I/O	Internal node, connect de-coupling capacitor to V_{DD_LFI}
48	COMN_A	Analog I/O	Internal node, connect de-coupling capacitor to V_{DD_LFI}
49	Exposed Pad	Supply pad	Exposed pad of the package

Pin Description: This table shows a detailed pin description of the AS3993.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD_IO}	Supply voltage V_{DD_IO}	-0.3	6.0	V	
V_{EXT}	Supply voltage V_{EXT}	-0.3	4	V	
V_{EXT_PA}	Supply voltage V_{EXT_PA}	-0.3	5	V	
V_{INH}	Input pin voltage host interface	-0.3	V_{DD_IO} + 0.5	V	Valid for inputs EN, IRQ, MOSI, SCLK, NCS
V_{INO}	Input pin voltage, other pins	-0.3	V_{EXT} + 0.5	V	
I_scr	Input current (latch-up immunity)	-100	100	mA	JEDEC 78, AGD excluded from latch-up immunity test when EN is high. AGD is a reference voltage pin and must be kept at the reference voltage.
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge for RF pins 4, 5, 6, 16, 17, 20, 21, 23, 24	±1		kV	JESD22-A114E
	Electrostatic discharge for other pins	±2		kV	
Continuous Power Dissipation					
P_T	Total power dissipation (all supplies and outputs)		1.6	W	

Symbol	Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions					
T_J	Maximum operating virtual junction temperature		120	°C	
T_{strg}	Storage temperature	-55	150	°C	
T_{body}	Package body temperature		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn)
RH_{NC}	Relative humidity (non condensing)	5	85	%	
MSL	Moisture sensitivity level	3			Represents a max. floor life time of 168h

Absolute Maximum Ratings: This figure shows the absolute maximum ratings of the AS3993.

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

V_{EXT} = 3.3 V, V_{EXT_PA} = 3.3 V, V_{DD_IO} = 3.3 V, T_{AMB} = 25 °C unless otherwise noted.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{EXT}	Supply current without V_{DD_PA} current	V_{EXT} consumption	65 (2)	75		mA
I_{EXT_PA}	Supply current for internal PA	V_{DD_PA} = 3 V **pa_bias<1:0>** = 00_b **TX_lev<4:0>** = 0 dB **eTX<3:2>** = 00_b		120		mA
		V_{DD_PA} = 3 V **pa_bias<1:0>** = 01_b **TX_lev<4:0>** = 0 dB **eTX<3:2>** = 00_b		180		
I_{STBY}	Supply current in standby mode			3		mA
I_{PD}	Supply current in power-down mode	All system disabled including supply voltage regulators		1	10	µA
V_{AGD}	AGD voltage		1.45	1.55	1.65	V
V_{POR}	Power-on reset voltage (POR)		1	1.8	2.0	V
V_{RD}	Regulator drop	See note (3)		300		mV
V_{DD_PA}	Regulated supply for internal PA			3		V
P_{PSSR}	Rejection of external supply noise on the supply regulator	See note (4)		26		dB
P_{RFAUX}	Auxiliary RF output power	V_{DD_B} =3V		0		dBm

Symbol	Parameter	Conditions	Min	Typ	Max	Units
P_{PAOUT}	Internal PA output power	V_{DD_PA} = 3 V **pa_bias<1:0>** = 00_b **TX_lev<4:0>** = 0 dB **eTX<3:2>** = 00_b		17		dBm
		V_{DD_PA} = 3 V **pa_bias<1:0>** = 01_b **TX_lev<4:0>** = 0 dB **eTX<3:2>** = 00_b		20		
Differential Mixer						
R_{RFIN_DIFF}	Diff. mixer input impedance			100		Ω
$V_{SENS\_NOM\_DIFF}$	Nominal diff. mixer input sensitivity	Nominal diff. mixer setting, PER=0.1%		-67		dBm
$V_{SENS\_GAIN\_DIFF}$	Increased diff. mixer input sensitivity	Increased diff. mixer gain, PER=0.1%		-77		dBm
$V_{SENS\_LBT\_DIFF}$	Diff. mixer LBT sensitivity	Maximum diff. mixer LBT sensitivity		-89		dBm
$IP3_{DIFF}$	Diff. mixer third order intercept point	Nominal diff. mixer setting VEXT = 3V		20		dBm
$1dBcp_{DIFF}$	Diff. mixer input 1dB compression point	Nominal diff. mixer setting VEXT = 3V		9		dBm
T_{REC_DIFF}	Recovery time after modulation	Maximum LF selected		18		µs
Single-Ended Mixer						
R_{RFIN_SE}	Single ended mixer input impedance			50		Ω
$V_{SENS\_NOM\_SE}$	Nominal SE input sensitivity	Nominal SE mixer setting, PER=0.1%		-67		dBm
$V_{SENS\_GAIN\_SE}$	Increased SE input sensitivity	Increased SE mixer gain, PER=0.1%		-77		dBm
$V_{SENS\_LBT\_SE}$	SE mixer LBT sensitivity	Maximum SE mixer LBT sensitivity		-89		dBm
$IP3_{SE}$	SE mixer third order intercept point	Nominal SE mixer setting (5) VEXT = 3V		17		dBm

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1dBcp_{SE}$	SE mixer input 1dB compression point	Nominal SE mixer setting (5) VEXT = 3V		7		dBm
T_{REC_SE}	Recovery time after modulation	Maximum LF selected		18		µs
CMOS Input (valid for all CMOS inputs)(1)						
V_{IH}	High level input voltage	See note (6)	0.8 * V_{DD_IO}			V
V_{IL}	Low level input voltage	See note (7)			0.2 * V_{DD_IO}	V
I_{LEAK}	Input leakage current				1	µA
CMOS Output (valid for all CMOS outputs)						
f_{SCLK}	SCLK frequency	**hs_output** = 1 (8), $V_{DD\_IO} \geq 3$ V, C_{LOAD} = 50 pF			5	MHz
		hs_output = 1, $V_{DD\_IO} \geq 1.65$ V, C_{LOAD} = 50 pF			3	MHz
		hs_output = 0, $V_{DD\_IO} \geq 3$ V, C_{LOAD} = 50 pF			2	MHz
R_{NMOS}	Output NMOS resistance on digital pins	**hs_output** = 1		120		Ω
R_{PMOS}	Output PMOS resistance on digital pins	**hs_output** = 1, $V_{DD\_IO} > 3$ V		150		Ω
		hs_output = 1, $V_{DD\_IO} > 1.65$ V		300		Ω

Electrical Characteristics: Figure 6 show the electrical characteristics of the AS3993 device like supply voltages, current consumptions and RF parameters.

Note(s):

1. On all outputs, it is recommended to use loads with the smallest required current driving capability in order to prevent current/spikes.
2. Using **ic_bia_m<1:0>** option bits, the consumption can be decreased up to 9%. The drawback of decreased power consumption can be higher noise, lower output power, and declining sensitivity.
3. After execution of direct command: *Automatic Power Supply Level Setting ($A2_h$)*.
4. The difference between the external supply and the regulated voltage is higher than 300mV.
5. Register settings for nominal mixer settings: $0A:01_h$, $0D:84_h$, $22:13_h$.
6. At supply voltage ≤1.8V, the minimum VIH is defined as $0.9*V_{DD\_IO}$.
7. At supply voltage ≤1.8V, the maximum VIL is defined as $0.1*V_{DD\_IO}$.
8. Option bit 7 of Miscellaneous Register 1.

Typical Operating Characteristics

All defined tolerances for external components in this specification need to be assured over the whole operation condition range and also over lifetime.

Figure 7:
Typical Operating Characteristics

Symbol	Parameter	Min	Max	Units	Comments
V_{DD_IO}	Positive supply voltage V_{DD_IO}	1.65	5.5	V	
V_{EXT}	Positive supply voltage V_{EXT}	2.7	3.6	V	For optimal power supply rejection and performance a supply voltage of at least 3.3 V is required. A supply voltage above 3.0 V allows operation with reduced power supply rejection. Operation down to 2.7 V is possible with reduced performance.
V_{EXT_PA}	Positive supply voltage V_{EXTRF}	2.7	4.3	V	
V_{SS}	Negative supply voltage	0	0	V	Valid for all V_{SS} and VSN pins
T_{AMB}	Ambient temperature	-40	85	°C	

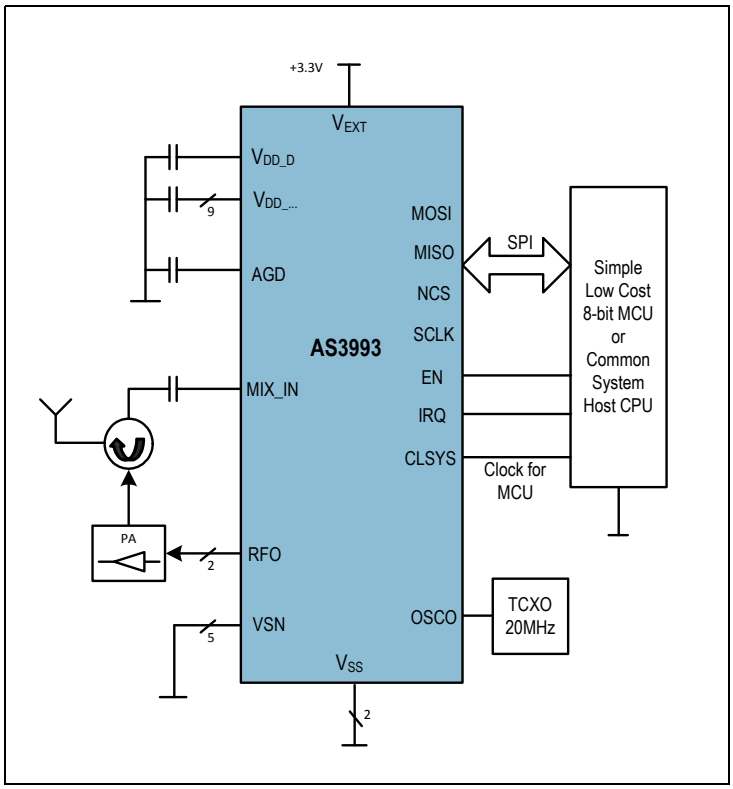
Typical Operating Characteristics: This figure shows the typical operating characteristics of the AS3993.

Detailed Description

The AS3993 UHF reader device is an integrated analog front end and protocol handling system for UHF RFID readers. The chip works on 3.3V supply voltage and is therefore perfectly suited for low voltage, low power applications. It supports operation on DRM link frequencies used in ETSI and FCC regions (see Rx Filter section for supported link modes). It complies with EPC Class1 Gen2 protocol (ISO 18000-6C) in normal mode and ISO 18000-6A/B in direct mode.

Figure 8:
Basic UHF Reader System

Basic UHF RFID System: This figure shows a very basic UHF RFID system using the AS3993 device.



The RFID reader device comprises of a complete analog and digital functionality for the reader operation, including transmitter and receiver section with complete EPC Class1 Gen2 (ISO18000-6C) digital protocol support.

The reader is enabled by setting the EN pin of the device to a positive logic level. A four-wire serial peripheral interface (SPI) is used for communication between the host system (MCU) and the reader device. The MCU is notified to service an IRQ by a logic high level on the IRQ pin. The device configuration and fine tuning of the reader performance is achieved through direct access to all control registers. The baseband data is transferred via a dual 24-byte FIFO buffer register to and from the reader device. The transmission system comprises of a parallel/serial data conversion, low-level data encoding and automatic generation of FrameSync, Preamble, and cyclic redundancy check (CRC).

Two transmitter output ports are available. A differential low power, high linearity 0 dBm output which drives its power into a single ended 50 Ω load or a differential high power output which is amplified by the internal PA. The high power output delivers up to 20 dBm and requires also a single ended 50 Ω load. Both outputs are capable of amplitude shift keying (ASK) or phase reversal amplitude shift keying (PR-ASK) shaped modulation. The integrated supply voltage regulators ensure supply ripple rejection of the complete reader system.

The receiver system allows AM and PM demodulation and comprises of a proprietary automatic gain control system. Selectable gain stages and signal bandwidth cover a wide range of input link frequencies and bit rate options. The signal strength of AM and PM modulation is measured and can be accessed through the RSSI Display Register ($2B_h$). The receiver output is selectable between digitized sub-carrier signals and internal sub-carrier decoder output. The internal decoder output delivers a bit stream and a data clock.

The receiver system comprises of a framing system for the baseband data. It performs a CRC check and organizes the data in bytes which is then accessible to the host system through a 24-byte FIFO register.

To minimize the BOM as much as possible, it also comprises of an on-board PLL section with an integrated voltage controlled oscillator (VCO), partially integrated loop filter, supply section, ADC section and host interface section. To cover a wide range of applications the reader device has numerous configuration possibilities. The register section configures operation and the behavior of all blocks.

The device needs to be supplied via V_{EXT} and V_{EXT_PA} pins. The power supply connection is described in the power supply section. At device power-up, the configuration registers are preset with their default values. The default values are described in the configuration register tables along with all option bits. The communication between the reader device and the transponder(s) follows the reader-talk-first method. After device power-up and configuring the reader device registers, the host system (MCU) can start a communication with the transponder by turning the RF field ON and transmitting the first protocol command. Transmission and reception is possible in two modes:

- Normal mode
- Direct mode

In normal mode the base band data is transferred through the double FIFO buffer and all protocol data processing is done internally. In the direct mode the encoders and decoders are bypassed for transmission and reception and the data processing must be done by the MCU. In the direct mode the MCU can service the analog front-end in real time.

Power Supply

The device has its own power supply system to minimize the influence of external power supply noise and interferences and improves decoupling between different internal building blocks.

The positive supply pins are V_{EXT} and V_{EXT_PA}. The negative supply pins are all VSN and VSS pins, including the exposed die pad. For optimal power supply rejection and device performance the supply voltage should be at least 3.3 V. A power supply voltage above 3.0 V allows operation with reduced power supply rejection. For an operation down to 2.7 V reduced device performance should be expected.

Main Regulators

A set of adjustable regulators is used to supply the different internal building blocks of the device. The common input pin for most regulators is V_{EXT}. The regulator output pins are the V_{DD_A}, V_{DD_LF}, V_{DD_D}, V_{DD_MIX} and V_{DD_B} pins. Each regulator output requires shunt capacitors to ground. Typical values are 2.2 µF and 100 pF. Recommended are ceramic capacitors of at least X5R class. V_{DD_LFI} and V_{DD_TXPAB} pins are supply input pins and should be connected to V_{DD_MIX}.

The regulated output voltage can be set in the range from 2.7V up to 3.4 V in 0.1 V steps using option bits **rvs<2:0>** in the Regulator and PA Bias Register ($0B_h$). It is also possible to adjust the regulated output voltage automatically to approximately 300mV below the supply voltage V_{EXT} using the direct command *Automatic Power Supply Level Setting ($A2_h$)*.

Internal PA Supply Regulator

The internal power amplifier has a dedicated voltage regulator. The input pin is V_{EXT_PA} and output is V_{DD_PA}. The regulator has an internal compensation circuit which requires a small external capacitance on V_{DD_PA} (typical 1 nF). Operation of this voltage regulator is allowed only in a loaded condition.

The regulated output voltage can be set in the range from 2.7 V up to 3.4 V in 0.1 V steps using option bits **rvs_rf<2:0>** in the Regulator and PA Bias Register ($0B_h$). It is also possible to adjust the regulated output voltage automatically to approximately 300 mV bellow the supply voltage V_{EXT} using the direct command *Automatic Power Supply Level Setting ($A2_h$)*.

As the **rvs_rf<2:0>** settings and the automatic power supply level adjustment generally can have different values, the system is designed to automatically select the lowest voltage level for the V_{DD_PA}.

Periphery Communication Supply

The logic levels used for communication with the host system (MCU) can vary within a wide voltage range. The V_{DD_IO} input pin is used to define these logic levels between 1.65V and 5.5V. It is recommended to connect V_{DD_IO} to the host system power supply in order to avoid any voltage mismatch.

Automatic Power Supply Level Setting

The power supply section comprises of a system that automatically adjusts the regulators to approximately 300 mV below the V_{EXT} supply voltage which is required to achieve good power supply rejection in the regulators.

The direct command *Automatic Power Supply Level Setting ($A2_h$)* activates the system. To switch back to manual power supply level adjustment, the direct command *Manual Power Supply Level Setting ($A3_h$)* should be sent.

Before the direct command *($A2_h$)* is issued it is necessary to set and lock the PLL to an allowed target frequency (840 MHz – 960MHz).

At the beginning of the automatic adjustment, the device sets the regulators to 3.4 V and enables the RF field to simulate a normal power supply load. During the procedure the device decreases the regulated voltage in 100 mV steps each 300 µs long. The lowest voltage the regulator can set is 2.7 V.

The procedure stops when the difference between the V_{EXT} and the regulated voltages is at least 300 mV or it reaches the last step. The device then disables the RF field and sends an IRQ request with **Irq_cmd** bit (register 36_h) set to high.

Power Modes

The device has three main power modes:

- Power Down mode
- Standby mode
- Normal mode– RF OFF
- Normal mode – RF ON

Power Down Mode

By driving the EN pin to a logic low level the device enters the power-down mode. In this mode, the circuit is disabled.

Normal Mode - RF OFF

Setting the EN pin to a logic high level activates the normal mode. In this mode the following internal blocks are enabled:

- All supply regulators
- Reference voltage and bias system
- Crystal oscillator
- RF oscillator and PLL

When the EN pin is set to a logic high level the bias and reference voltages stabilizes typically after 12 ms. From then onwards the device is ready to allow interaction with the internal registers After the reference frequency source stabilizes and the CLSYS clock becomes active, the device is ready to operate the way it is configured by the internal registers. In case the crystal oscillator is used, the time the crystal stabilizes depends on the crystal type used. A typical time is 1.5 ms to 3 ms. By reading the AGC and Internal Status Display Register ($2A_h$), the MCU can check the crystal status. The status bit **osc_ok** = 1 in this register indicates that the crystal oscillation is stable and that the device is ready to operate.

In case a continuously running TCXO is used the settling of the internal clock is faster as only the OSCO pin DC level needs to be set. The same test with the **osc_ok** status bit as described above can be used.

Normal Mode - RF ON

By setting the **rf_on** option bit in the Device Status Control Register(00_h) the device immediately starts with the field ramp-up. The ramp-up time and shape are defined by **trfon<1:0>** and **lin_mod** option bits in the Modulator Control Register 3 (15_h). When the RF field ramp-up is finished the **rf_ok** status bit (register $2A_h$) is set to high. In addition an IRQ is generated which is indicated by **Irq_ana** status bit set to high (register 38_h).

Setting the option bit **rf_on** to low starts the field ramp-down. The RF field is decreased according to **trfon<1:0>** and **lin_mod** bits (register 15_h). When finished, the **rf_ok** status bit in AGC and Internal Status Display Register ($2A_h$) is set to low, and an IRQ is sent with the **Irq_ana** status bit high.

Standby Mode

The standby mode is entered from normal mode by setting the option bit **stby** high (register 00_h). In the standby mode the voltage regulators, the reference voltage system and the crystal oscillator are operating in a low power mode. The PLL, transmitter output stages and the receivers are switched off. All register settings are maintained while switching between standby and normal mode. The bias and reference voltages after **stby** = 0 typically stabilize within 12 ms. By then the device is ready to switch on the RF field and start data transmission.

Figure 9:
Power Modes Overview

Mode	EN Pin	Stby Option Bit	rf_on Option Bit	Current Consumption	Time to Enter the Mode	Time from Mode to Active RF Field
Power down	L	X	X	1 µA	Immediately from normal mode	12-17ms (Crystal or TCXO start + bias start)
Standby	H	H	L	3 mA	Immediately from normal mode	12 - 17 ms (Crystal or TCXO start + bias start)
Normal	H	L	L	24 mA	12 - 17 ms (Crystal or TCXO start + bias start)	12.5 µs (Field ramp-up)
Normal with RF field on	H	L	H	75 mA	12.5 µs (Field ramp-up)	NA

Power Modes Overview: This figure presents the available power modes and the transitions times between them.

Host Communication

A standard 4-wire serial interface (SPI) together with an interrupt request line (IRQ pin) is used to communicate with the device. An additional line (CLSYS) can be used as a system clock source for the MCU.

Figure 10:
Serial Data Interface (SPI Interface) Signal Lines

Name	Signal	Signal Level	Description
NCS	Digital Input	CMOS	SPI Enable (active low)
SCLK	Digital Input	CMOS	Serial Clock
MOSI	Digital Input	CMOS	Serial Data input
MISO	Digital Output with tri-state	CMOS	Serial Data output
IRQ	Digital Output	CMOS	Interrupt request output
CLSYS	Digital Output	CMOS	MCU clock output

SPI Interface: This figure shows the SPI signals and describes their function.

By setting the NCS pin to low the SPI interface is enabled. While NCS is high the SPI interface is deactivated. It is recommended to keep signal NCS high whenever the SPI interface is not used. MOSI is sampled at the falling edge of SCLK. The SPI

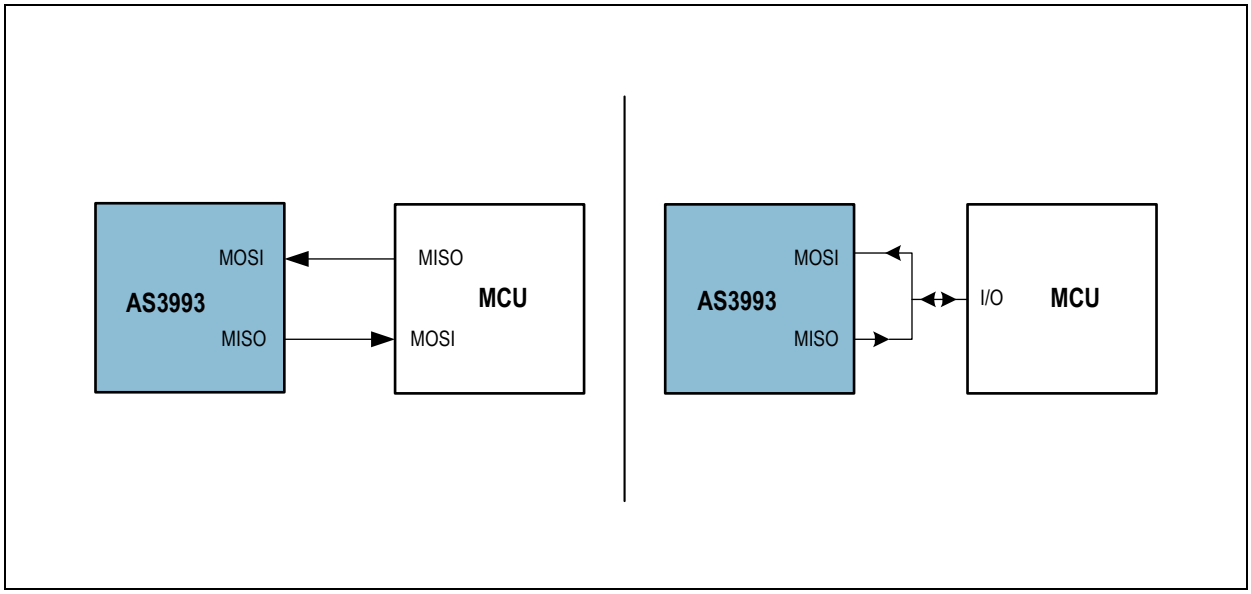
communication is done in bytes. The first two bits of the first byte on the MOSI line (after NCS high-to-low) define the SPI operation mode. MSB bit is always transmitted first (valid for address and data).

The read and write modes support address auto incrementing for multi byte transfers. Only the first address needs to be sent and internally the address is incremented for consecutive reads or writes.

The MISO output is usually in tri-state and it is only driven when output data is available. This allows short-circuiting the MOSI and the MISO line externally to create a bi-directional signal (see Figure 11).

During the time the MISO output is in high impedance it is possible to activate a 50 kΩ pull-down resistor by setting option bits **miso_pd1** and **miso_pd2** in Miscellaneous Register 1 ($0D_h$).

Figure 11:
Possible SPI Configurations



SPI Configuration Options: These figures depict two possible SPI interconnection options.

Figure 12:
SPI Operation Modes

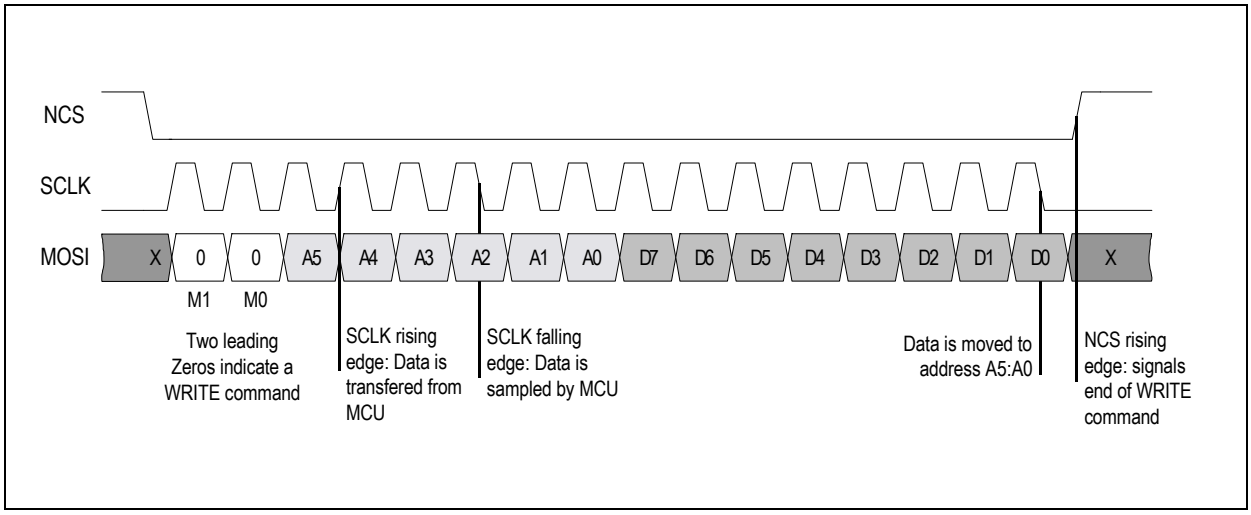
Command Type	Mode Pattern (MSB to LSB)								Mode Related Data
	Mode		Register Address / Command ID						
	M1	M0	X5	X4	X3	X2	X1	X0	
WRITE	0	0	A5	A4	A3	A2	A1	A0	Data byte (or more bytes in case of auto incrementing)
READ	0	1	A5	A4	A3	A2	A1	A0	Data byte (or more bytes in case of auto incrementing)
Direct Command	1	0	C5	C4	C3	C2	C1	C0	
RFU	1	1	x	x	x	x	x	x	

SPI Operations Modes: This figure shows the SPI operation modes and describes their function.

Writing to Registers

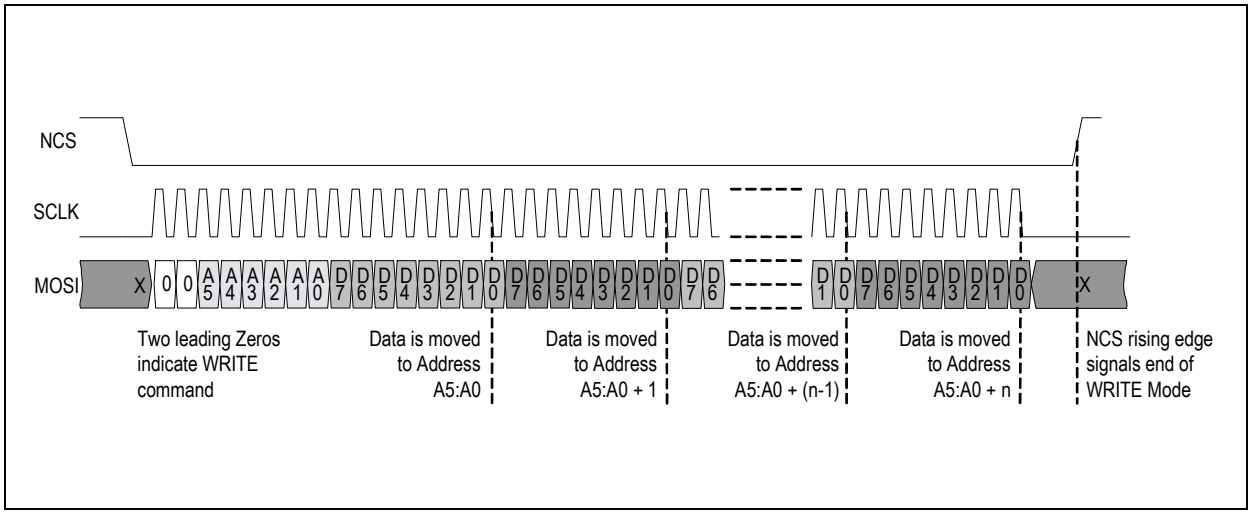
The figures below show typical SPI WRITE communication examples for a single byte and for multiple bytes using address auto-incrementing. Following the SPI operation mode bits (M1 and M2) the address bits (A5:A1) of the target register are sent. Then one or more data bytes are sent depending on using auto-incrementing or not. The communication is terminated by putting NCS back to high. In case this happens before a packet of 8 bits, composing one byte, is sent, writing to this register is not performed. In case the register at the defined address does not exist or is a read only register the write command does not succeed either.

Figure 13:
Writing of a Single Byte



SPI Single Byte Write Command: This figure shows an example of a SPI write command signaling for a single byte.

Figure 14:
Writing of Registers Using Address Auto-Incrementing



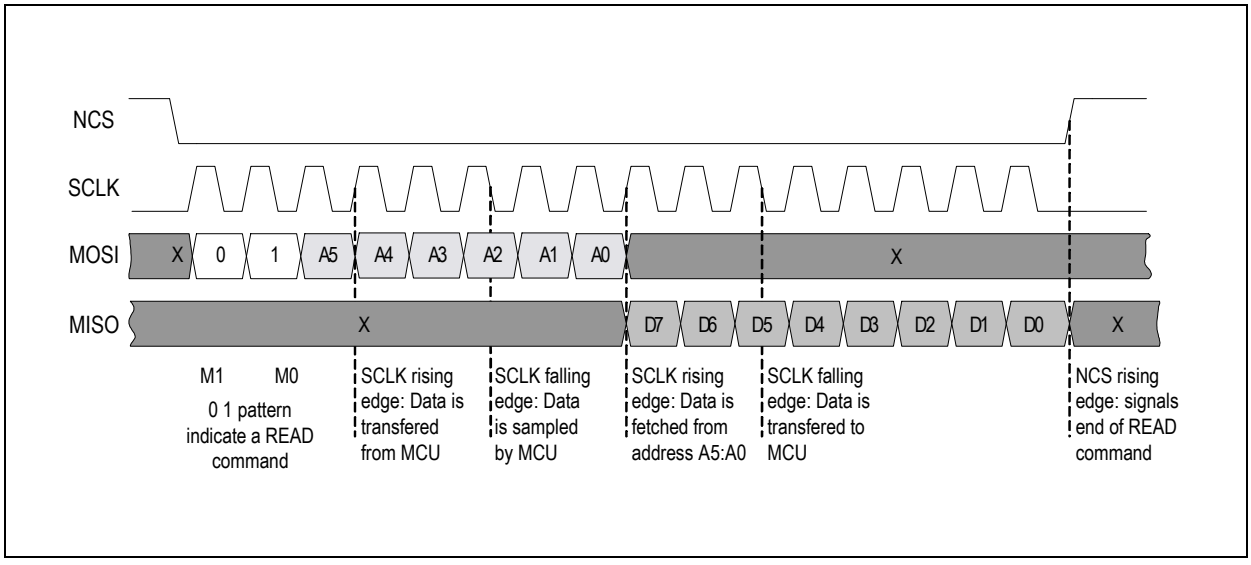
SPI Multiple Bytes Write Command: This figure shows an example of a SPI write command signaling for multiple bytes.

Reading from Registers

After the SPI operation mode bits (M1 and M0) the target address is sent. Then one or more data bytes are transferred to the MISO output. MOSI is sampled at the falling edge of SCLK. Data to be read from the internal registers is transferred to the MISO pin on rising edge of SCLK and should be sampled by the MCU at the falling edge of SCLK. In case the register address does not exist all 0 data is sent to MISO.

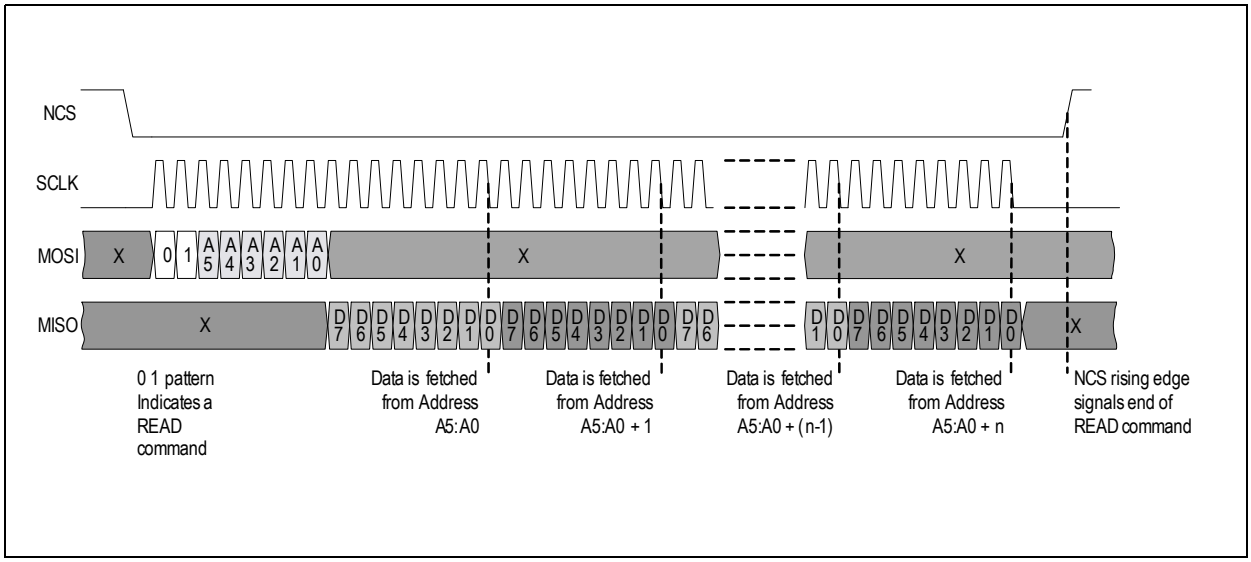
The figure below shows an example for a typical SPI READ command for a single byte.

Figure 15:
Reading of a Single Byte



SPI Single Byte Read Command: This figure shows an example of a SPI read command signaling for a single byte.

Figure 16:
Reading from Registers Using Address Auto-Incrementing



SPI Multiple Bytes Read Command: This figure shows an example of a SPI read command signaling for multiple bytes.

Direct Commands

Direct commands have no parameters so only a single byte needs to be sent. The only exception is the Query command which requires two parameter bytes (stored in FIFO) following the command byte. SPI operation mode bits M1 = 1 and M0 = 0 define a direct command. The following six bits define the direct command ID. The direct command is executed at the last falling edge of SCLK. Some direct commands are executed immediately while others start a process with certain duration (calibration, measurements…).

Important: During execution of such commands it is not recommended to start another activity on the SPI interface.

After the execution of a direct command an IRQ request with **Irq_cmd** bit high (register 38_h) is sent.

Figure 17:
List of Direct Commands

Code (HEX)	Command	Direct Execution
80_h	Idle	Yes
81_h	Direct Mode	Yes
83_h	Soft Init	Yes
84_h	Hop to Main Frequency	Yes
85_h	Hop to Auxiliary Frequency	Yes

Code (HEX)	Command	Direct Execution
87_h	Trigger AD Conversion	No
88_h	Trigger Rx Filter Calibration	No
89_h	Decrease Rx Filter Calibration Data	Yes
$8A_h$	Increase Rx Filter Calibration Data	Yes
90_h	Transmission with CRC	Yes
91_h	Transmission with CRC Expecting Header Bit	Yes
92_h	Transmission without CRC	Yes
96_h	Block Rx	Yes
97_h	Enable Rx	Yes
98_h	Query	Yes
99_h	QueryRep	Yes
$9A_h$	QueryAdjustUp	Yes
$9B_h$	QueryAdjustNic	Yes
$9C_h$	QueryAdjustDown	Yes
$9D_h$	ACK	Yes
$9F_h$	ReqRN	Yes
$A2_h$	Automatic Power Supply Level Setting	No
$A3_h$	Manual Power Supply Level Setting	Yes
$A4_h$	Automatic VCO Range Selection	No
$A5_h$	Manual VCO Range Selection	Yes
$A6_h$	AGL On	Yes
$A7_h$	AGL Off	Yes
$A8_h$	Store RSSI	Yes
$A9_h$	Clear RSSI	Yes
AA_h	Interrogator Anti-collision Support Enable	Yes
AB_h	Interrogator Anti-collision Support Disable	Yes

Direct Commands: This figure lists all available direct commands for the AS3993 device.

Direct Command Description

The following section describes the direct commands that are supported by the AS3993 reader device in more detail. The values in parenthesis show the related command byte.

Direct Mode (81_h):

Device enters the direct mode.

Soft Init (83_h):

This command resets the configuration registers to their default values and terminates all functions that were triggered before.

Hop to Main Frequency (84_h):

This command forces the PLL to use the frequency defined in the PLL Main Registers 1 - 3. The PLL main registers are used per default.

Hop to Auxiliary Frequency (85_h):

This command forces the PLL to use the frequency setting defined in the PLL Auxiliary Registers 1 – 3.

Trigger A/D Conversion (87_h):

This command triggers the analog to digital conversion using the internal 8-bit A/D converter. For further information, please refer to the A/D Converter description.

Trigger Rx Filter Calibration (88_h):

This command triggers the Rx filter calibration procedure. For further information, please refer to the Rx Filter Calibration description.

Decrease Rx Filter Calibration Data (89_h), Increase Rx Filter Calibration Data ($8A_h$):

These commands adjust the automatically acquired Rx filter calibration data. For further information, please refer to the Rx Filter Calibration description.

Transmission with CRC (90_h):

Transmission commands are used to transmit data from the reader to transponders. First, the Tx length registers ($3D_h$, $3E_h$) need to be set with the number of complete bytes for transmission, including the number of bits for the incomplete byte. Then transmission data can be loaded to the FIFO register ($3F_h$). Transmission starts when the first byte is loaded. CRC-16 is included in the transmitted sequence.

The optimal way to load all transmission data is to use the Continuous Write mode, starting with the address $3D_h$.

Example Using Address Auto-Incrementing:

SPI data (MOSI): 90_h - $3D_h$ - 00_h - 30_h - AA_h - BB_h - CC_h operates as follows:

- 90_h:Transmission with CRC
- Write 00_h to $3D_h$
- Write 30_h to $3E_h$ (three bytes are going to be transmitted)
- Write AA_h, BB_h, CC_h to address $3F_h$ (FIFO data which will be transmitted).

Transmission with CRC Expecting Header Bit (91_h):

Same as above, but also informs Rx decoding logic that header bit is expected in the response.

Transmission without CRC (92_h):

Same as direct command 'Transmission with CRC', but the CRC part is omitted.

Block Rx (96_h):

The *Block Rx* command deactivates the digital part of receiver (bit decoder and framer). Turning OFF of the receiver is useful in case the system operates in a noisy environment, causing a constant switching of the sub-carrier input of the Rx digital part. The active receiver would try to detect a Preamble and in case the noise pattern matches the expected signal pattern, an interrupt is generated. A constant flow of interrupt requests can be a problem for the MCU which may prevent this condition by putting deactivating the receive decoders. The receiver is automatically activated again at the end of any data transmission after the Rx wait time elapses. To set the Rx wait time please refer to the Rx Wait Timer section. A second possibility to stop *Block Rx is to send the Enable Rx (97_h)* command.

Enable Rx (97_h):

This command prepares analog and digital part of the receiver for reception. This command should be sent to trigger the reception manually. This command should not be sent in case reception is automatically triggered by a data transmission command.

Query (98_h):

The *Query* command issues the EPC Query, which starts the inventory round. The *Query* command requires additional 2 data bytes which should be written to the FIFO ($3F_h$):

The two bytes in the FIFO should contain:

00, DR, M, TRext, Sel, Session, Target, Q

Since this adds-up to 15 applicable bits, the LSB bit is disregarded.

The transmitter finally sends:

- Preamble
- Command ID
- Tx data (two bytes from FIFO)
- CRC-5.

The received RN16 is stored in the internal RN16 register for further communication steps (ACK, ReqRN). RN16 is also stored in the FIFO.

QueryRep (99_h):

The *QueryRep* command issues the EPC Gen2 QueryRep command followed by two session bits. The session bits are taken from Tx Setting Register ($3C_h$). The received RN16 is stored in the internal RN16 register for further communication (ACK, ReqRN). RN16 is also accessible in the FIFO.

QueryAdjustUp ($9A_h$):

The *QueryAdjustUp* direct command issues the EPC Gen2 QueryAdjust command followed by two session bits and 'up' parameter (increasing the number of available slots). The session bits are taken from Tx Setting Register ($3C_h$). The received RN16 is stored in the internal RN16 register for further communication (ACK, ReqRN). RN16 is also accessible in the FIFO.

QueryAdjustNic ($9B_h$):

The *QueryAdjustNic* command issues the EPC Gen2 QueryAdjust command followed by two session bits and 'no change' parameter. The session bits are taken from Tx Setting Register ($3C_h$). The received RN16 is stored in the internal RN16 register for further communication (ACK, ReqRN). RN16 is also accessible in the FIFO.

QueryAdjustDown ($9C_h$):

The *QueryAdjustUp* command issues the EPC Gen2 QueryAdjust followed by two session bits and 'down' parameter (decreasing the number of available slots). The session bits are taken from Tx Setting Register ($3C_h$). The received RN16 is stored in the internal RN16 register for further communication (ACK, ReqRN). RN16 is also accessible in the FIFO.

ACK ($9D_h$):

The *ACK* command issues the EPC ACK followed by RN16 that was stored in the internal RN16 register. The stored RN16 was acquired during last successful Query command.

NAK ($9E_h$):

The *NAK* command issues the EPC Gen2 NAK command to tags.

ReqRN ($9F_h$):

The *ReqRN* command issues the EPC Request RN to the tag. The last received RN is used as a parameter and the received new RN16 (handle) is stored in the internal RN16 register for further communication (ACK, ReqRN). New RN 16 is also stored in the FIFO.

Automatic Power Supply Level Setting ($A2_h$), Manual Power Supply Level Setting ($A3_h$):

These commands trigger the automatic adjustment of the on-board voltage regulators and switches back to the manual selection. See Periphery Communication Supply description for more details.

Automatic VCO Range Selection ($A4_h$), Manual VCO Range Selection ($A5_h$):

These commands trigger the automatic VCO range selection and switches back to manual VCO range selection. See PLL and VCO description for more details.

AGL On ($A6_h$), AGL Off ($A7_h$):

These commands trigger and disable the AGL action. See AGL description for more details.

Store RSSI ($A8_h$), Clear RSSI ($A9_h$):

These commands store and clear the received signal strength indicator (RSSI) data that can be used for IQ decision circuitry. See IQ Selection description for more details.

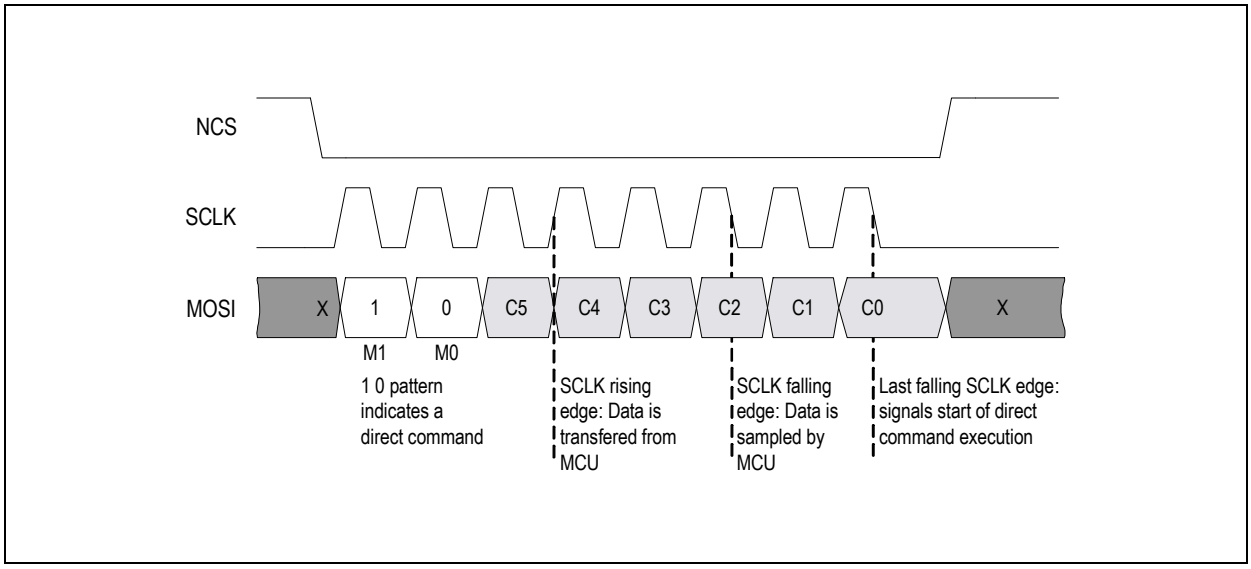
Interrogator Anti-Collision Support Enable (AA_h), Interrogator Anti-Collision Support Disable (AB_h):

These commands enable or disable the interrogator anti-collision support defined in ISO 29143.

Direct Command Chaining

Direct commands with immediate execution can be followed by another SPI commands like READ or WRITE without deactivating the NCS signal in between.

Figure 18:
Sending Direct Commands



Sending Direct Commands: This figure shows the signaling for sending a direct command.

SPI Interface Timing

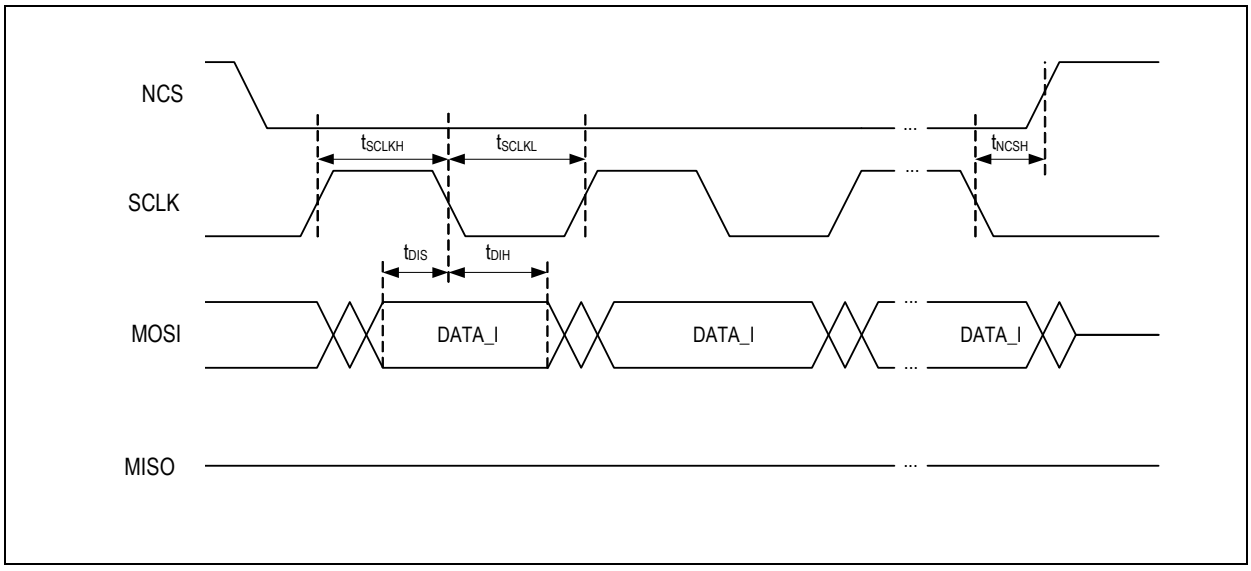
Figure 19:
SPI Timing Parameters

Symbol	Parameter	Note/ Condition	Min	Typ	Max	Units
General (V_{DD_IO} > 3 V, CLOAD < 50 pF, hs_output = 1)						
BR_{SPI}	Bit rate				5	Mbps
t_{SCLKH}	Clock high time		70			ns
t_{SCLKL}	Clock low time		70			ns
t_{NCSL}	NCS setup time	Time between NCS high-low transition to first SCLK high transition	10			ns
t_{DIS}	Data-in setup time		10			ns
t_{DIH}	Data-in hold time		10			ns
t_{NCSH}	NCS hold time READ / WRITE	Time between last SCLK falling edge and NCS low-high transition after a READ or WRITE	10			ns

Symbol	Parameter	Note/ Condition	Min	Typ	Max	Units
t_{NCSH}	NCS hold time direct command	Time between last SCLK falling edge and NCS low-high transition after a direct command	70			ns
Read Timing						
t_{DOD}	Data out delay	$V_{DD\_IO} \geq 3$ V, $C_{LOAD} = 50$ pF, **hs_output** = 1		30		ns
t_{DOD}	Data out delay	$V_{DD\_IO} \geq 1.65$ V, $C_{LOAD} = 50$ pF, **hs_output** = 1		60		ns
t_{DOD}	Data out delay	$V_{DD\_IO} \geq 3$ V, $C_{LOAD} = 50$ pF, **hs_output** = 0		90		ns
t_{DOHZ}	Data out to high impedance delay	Time for the SPI to release the MISO line		40		ns

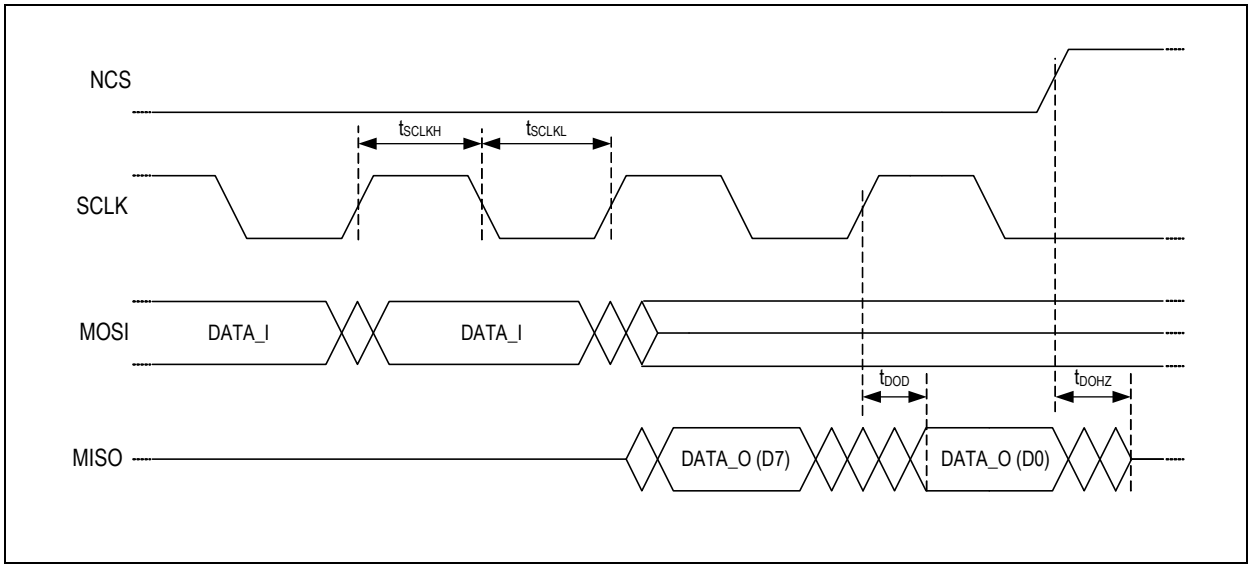
SPI Timing Parameters: This figure shows relevant SPI timing parameters for the AS3993 device.

Figure 20:
SPI WRITE Timing



SPI Write Timing: This figure shows the corresponding timing waveforms and parameters for the SPI write command.

Figure 21:
SPI READ Timing



SPI Read Timing: This figure shows the corresponding timing waveforms and parameters for the SPI read command.

CLSYS Output

The CLSYS output is intended to be used as a MCU clock source. Available frequencies are:

- 4MHz
- 5MHz
- 10MHz
- 20MHz

The CLSYS frequency is defined by **clsys<2:0>** option bits in the Miscellaneous Register 2 ($0E_h$).

IO Signal Level and Output Characteristics

The logic high level for the host communication and CLSYS is defined by the supply voltage connected to V_{DD_IO} pin. The logic high level can be in the range between 1.65V and 5.5V. V_{DD_IO} should be connected to the host system periphery supply voltage to ensure matching communication levels.

The digital outputs are by default configured for high-speed operation. A 5 MHz SPI clock is possible with a 50 pF capacitive load on the MISO and IRQ outputs and a minimum V_{DD_IO} supply voltage of 3 V. A 3 MHz SPI clock is possible with a 50 pF load and a minimum V_{DD_IO} supply voltage of 1.65V.

To decrease the harmonic content of the digital output signals, it is possible to configure the device outputs to provide weak, sloped output signals by setting the **hs_output** option bit in the Miscellaneous Register 1 ($0D_h$) to low. This way the possibility of interferences by the host system communication with other internal building blocks of the device is mitigated as well.

Using this option a 2 MHz SPI clock is possible with maximum 50 pF capacitive load on MISO and IRQ and at least a V_{DD_IO} supply voltage of 3 V.

It is also possible to define open drain N-MOS outputs by setting the option bit **open_dr** to high (register $0D_h$). This option allows reducing the harmonic content on the MISO, IRQ, and CLSYS signals further. It also decreases cross-coupling effects that could interfere with operation of other parts of the device.

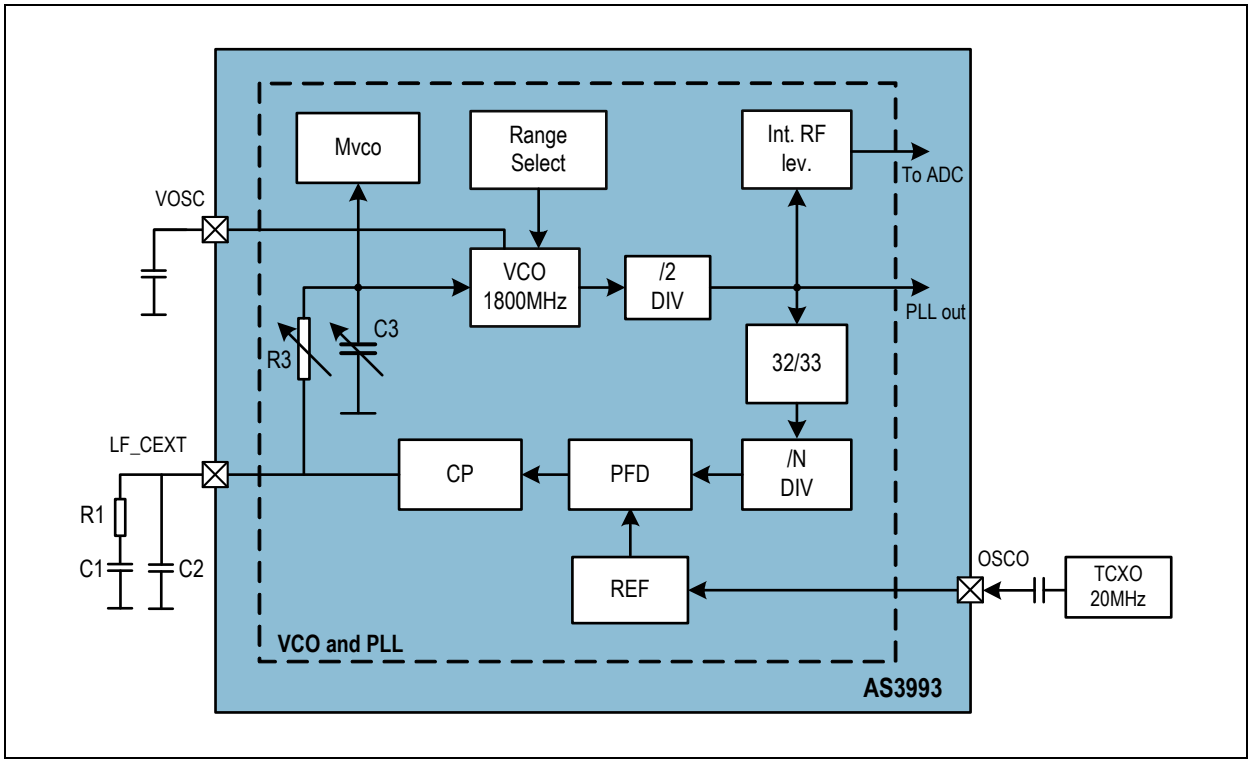
OAD, OAD2 Outputs

The OAD and OAD2 outputs are analog and digital test outputs. When used as analog outputs, the received sub-carrier signals or mixer analog DC output levels are multiplexed at these pins. The signal is centered to AGD level. When used as digital output, the levels are configured with V_{DD_IO}. The OAD pins can be configured as high speed outputs by setting the option bit **hs_oad** in the Miscellaneous Register 1 ($0D_h$). During normal operation it is not recommended to use **hs_oad**, as higher harmonic content can increase the crosstalk to sensitive pins of the device.

PLL and VCO Section

The PLL section comprises of a voltage controlled oscillator, a pre-scaler, main and reference dividers, a phase-frequency detector, a charge pump and a loop filter.

Figure 22:
PLL and VCO Section



Block Diagram PLL and VCO Section: This figure shows a detailed block diagram of the PLL and VCO section of the AS3993 device.

All building blocks except a part of the loop filter are all integrated in the AS3993.The allowed frequency operation range is 840 MHz to 960 MHz.

Voltage Controlled Oscillator

The VCO is entirely integrated including the variable capacitor and inductor. The frequency control input pin is LF_CEXT. The valid voltage range is between 0.5 V and V_{DD_A} - 0.5 V. The option bits **eosc<2:0>** in the VCO Control Register (11_h) are used for oscillator noise and current consumption optimization. Power supply decoupling is done via VOSC pin. The internal VCO frequency is set in the range of 1800 MHz which is internally divided by two for decreased VCO pulling effect. The tuning curve of the 1800 MHz VCO is divided into 16 segments (ranges) to decrease the VCO gain and to attain lowest possible phase noise.

VCO Tuning Range Selection

The selection of the VCO tuning range can be done manually by setting the option bits **vco_r<3:0>** in the VCO Control Register (11_h). An automatic selection can be started by using the direct command *Automatic VCO Range Selection ($A4_h$)*. Reverting back to manual selection is possible by sending the direct command *Manual VCO Range Selection ($A5_h$)*. The *Automatic VCO Range Selection ($A4_h$)* command starts a search algorithm which finds the appropriate VCO segment. When the algorithm is finished it sends an IRQ request with **Irq_cmd** and **autovco_done** status bit in the Command Status Display Register ($2E_h$) set to high.

Readout of VCO Tuning Range Status

The result of the automatic segment search algorithm is represented by **vco_ri<7:4>** which can be read out from the device via the AGL / VCO / F_CAL / PilotFreq Status Register ($2C_h$) when the option bits **r2Cpage<1:0>** = 01_b (register 29_h).

VCO Control Voltage Measurement

The device allows a measurement of the VCO control voltage by setting option bit **mvco** in VCO Control Register (11_h) to high. The 3 bits result **vco_ri<2:0>** can be read out from the AGL / VCO / F_CAL / PilotFreq Status Register ($2C_h$) using **r2Cpage<1:0>** = 01_b (register 29_h). During normal operation, the **mvco** option bit in register 11_h should remain low. Details on using the 1800 MHz VCO are described in a dedicated application note.

PLL Prescaler and Main Divider

The divide-by-32/33 prescaler is controlled by the N-divider. The divider ratio is defined by the PLL Main Registers 1 - 3 (17_h-19_h) or PLL Auxiliary Registers 1-3 ($1A_h$-$1C_h$). The lower ten

bits of the three main (aux.) registers define the A value and the next upper ten bits define the B value. The A and B values define the main divider dividing ratio to:

$$N = B * 32 + A * 33$$

The two register sets PLL Main Registers 1 - 3 and PLL Auxiliary Registers 1-3 are intended to support frequency hopping using the direct commands *Hop to Main Frequency (84_h)* and *Hop to Auxiliary Frequency (85_h)*.

PLL Reference Frequency

The reference frequency is selected by the **RefFreq<2:0>** bits in the PLL Main Register 1 (17_h). Available values are:

- 125 kHz
- 100 kHz
- 50 kHz
- 25 kHz

Reference Frequency Source

For the reference frequency a frequency source of 20 MHz is required. It is possible to use an external oscillator (TCXO) or quartz crystal. In case a TCXO is used, it should be connected to the OSCO pin while the OSCI pin should be shorted to ground. The signal shape of the TCXO should be of a sinusoidal type and AC coupled. The level should be in the range between 0.8 V_{pp} and 3 V_{pp}. A low OSCO level is recommended to minimize the spectral signal components spaced by ±20 MHz around the Tx carrier frequency. The OSCO input impedance in this mode is typically 9 kΩ and 9 pF in parallel. A crystal should be connected between the OSCI and OSCO pins with appropriate load capacitors in shunt configuration to ground. Load capacitances in the range from 15 pF to 20 pF are recommended. The maximum series resistance in resonance should be 30 Ω. The crystal oscillator is started-up in fast mode in order to speed-up a stable crystal oscillation. The device then switches back to the power saving mode. The device operation typically uses the power saving mode. Option bits **xosc<1:0>** in the Miscellaneous Register 2 ($0E_h$) are available to manually control the crystal operation modes.

Phase-Frequency Detector and Charge Pump

The reference frequency and the divided RF frequency are compared in the phase-frequency detector which drives the charge pump connected to the LF_CEXT pin. The charge pump current is selectable between 150 µA and 2350 µA using option

bits **cp<2:0>** in the CP Control Register (12_h).

Loop Filter

The loop filter is composed of an external and an internal part. The first stage (series capacitor, series resistor and shunt capacitor) is external and is connected to the pin LF_CEXT. The second stage (R3/C3 filter) is internally connected between the LF_CEXT pin and the VCO control input.

The values for the internal part of the loop filter (R3 and C3) can be selected by option bits **LF_R3<7:6>** and **LF_C3<5:3>** both in the CP Control Register (12_h). R3 can be set in a range 30 kΩ–100 kΩ and C3 can be set in a range 20 pF–200 pF.

Frequency Hopping Commands

Frequency hopping is possible by issuing the direct commands *Hop to Main Frequency (84_h)* and *Hop to Auxiliary Frequency (85_h)* which sets the main divider ratio either to the main or the auxiliary PLL register. The host system (MCU) is responsible to perform correct frequency hopping according to local regulations.

PLL Start-Up and Frequency Hopping

Before enabling the RF field, the host system needs to configure the PLL through the CP Control Register (12_h) and the PLL Main Registers 1-3 (17_h, 18_h, 19_h). The PLL should be locked using one of the above defined possibilities. Any time during operating at one frequency, the host system can fill the auxiliary PLL Main Registers. When the frequency hop needs to be done only the appropriate frequency hopping direct command needs to be sent to the device.

Device Status Control

In the Device Status Control Register (00_h), the main functionality of the device is controlled. By setting the option bit **rf_on**, the internal transmitter and receiver blocks are enabled. The initial RF field ramp-up is defined by the **Tari<2:0>** option bits in the Tx Options Register (02_h) and by option bits **trfon<1:0>** in the Modulator Control Register 3(15_h).

The available values are:

- 100 µs
- 200 µs
- 400 µs
- TARI determined

When finished, the **rf_ok** bit in the AGC and Internal Status Display Register ($2A_h$) is set and an IRQ with **Irq_ana** bit is sent. By setting the **rf_on** bit low, the RF field is ramped-down similar to the ramp-up transient and an IRQ with **Irq_ana** bit set is sent. The **rec_on** bit enables the receiver only. The **agc_on** bit enables the AGC functionality. The **stby** bit puts the device into the standby mode.

Protocol Control

In the Protocol Selection Register (01_h), the main protocol parameters are selected. The **prot<2:0>** option bits should be set to 000_b for EPC Class1 Gen2 operation and to 001_b for ISO18000-6A/B FM0 decoder operation. The **AutoACK<1:0>** bits enables the automatic inventory round sequencing and define its depth. There are three possible modes:

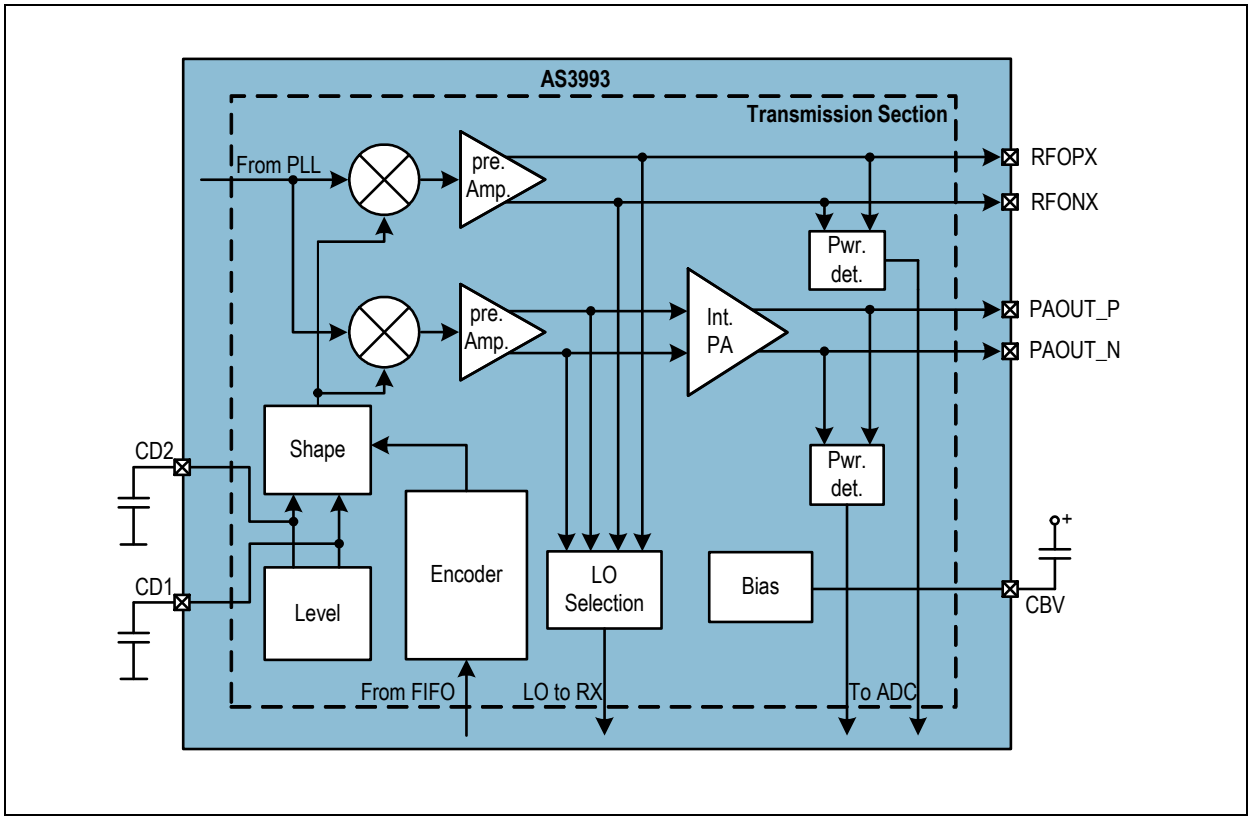
- No automatic
- Automatic ACK
- Automatic ACK + ReqRN

The option bit **RX_crc_n** = 1 defines reception with no internal CRC check. The CRC is then just passed on to the FIFO like any other data bytes. In the EPC Gen 2 protocol this is a useful feature in case of a truncated EPC reply where the stored CRC that a transponder transmits is not calculated over the actual transmitted data and is therefore an invalid CRC. The **dir_mode** bit defines the type of output signals while operating in the direct mode. It also disables any decoding and signal sensing automatics during the reception. It is advised to set this bit to high when continuous analog measurements are performed.

Transmission Section

The transmitter section comprises of a data handling, an encoding part, a shaping circuitry, a modulator and amplifier circuitry.

Figure 23:
Transmission Section



Block Diagram Transmission Section: This figure shows a detailed block diagram of the transmission section of the AS3993 device.

The RF carrier is modulated with a shaped representation of the transmit data and (pre-) amplified for transmission.

Tx Data Handling and Coding

The data handling part takes the baseband data from the FIFO and encodes it according to the Gen2 protocol (PIE). It adds a preamble or a frame-sync and calculates the CRC. The digital modulation signals are fed to the shape circuitry.

Tx Shape Circuitry

The modulation shape is controlled by a double D/A converter. The first 5-bit logarithmic converter forms two voltages, which define minimum and maximum (V_{pp}) modulation signal level.

The two voltages are filtered by two external capacitors connected to the CD1 and CD2 pins to minimize the noise level and are used as a reference for the shaping circuitry. The second 9-bit linear converter transforms the digital modulation signal

into a sinusoidal or linear shaped analog modulation signal. The output of the shaping circuit is interpolated and connected to the modulator input.

Local Oscillator (LO) Path

To improve the phase noise rejection, the local oscillator signal is derived from the output of the pre-amplifier stages. For optimal operation, the pre-amplifier levels should be close to nominal (set by **TX_lev<4:0>** in register 15_h). In case lower levels are used, the LO signal can be increased by approximately 6 dB using option bit **eTX<7>**. The drawback is increased received noise.

Modulator

The modulator modulates the RF carrier with the shaped representation of the digital modulation signal. The internal modulator is capable of ASK and PR-ASK modulation.

Tx Level and Shape Adjustments

The output level and modulation shape properties are controlled by the Modulator Control Registers 1 - 4 (13_h-16_h). The level of the output signal is adjusted by option bits **TX_lev<4:0>** in Modulator Control Register 3 (15_h). For good performance, it is advised to design the exterior circuit of the reader device as such that the reader output power is set close to the AS3993 nominal output power. In case temporarily operation at decreased power is need the **TX_lev<4:0>** option bits should be used. Sinusoidal or linear shape is defined by the option bit **lin_mod** in register *(15_h)*. PR-ASK modulation is selected by setting the **pr_ask** option bit to high. In case PR-ASK is selected, the **del_len<5:0>** option bits are used to adjust the delimiter length in the range from 9.6 µs to 15.9 µs. For Tari = 25 µs PR-ASK and ASK delimiter shapes are available. The ASK transient which gives more accurate timing can be selected by the **ook_ask** option bit in register 15_h. For Tari = 12.5 µs and 6.25 µs only the ASK delimiter shape is available. ASK modulation is selected by setting the **pr_ask** option bit to low. In ASK modulation it is possible to adjust the delimiter length by setting the option bit **ook_ask**. In this case, **ook_ask** defines 100% ASK modulation and the **del_len<5:0>** bits are used for delimiter length setting as in the PR-ASK mode described above. The rate of the modulation transient is automatically adjusted to the selected Tari setting and can be re-adjusted by the **ask_rate<1:0>** option bits (register 13_h). For smoother transitions of the modulation signal an optional low pas filter can be activated by the **e_lpf** option bit in the Modulator Control Register 1 (13_h). Bits **aux_mod** and **main_mod** define whether the modulation signal will be connected to the low power output or to the internal PA output path. In case one of the outputs is enabled by the **eTX<3:0>** bits in RF Output and LO Control Register ($0C_h$) and corresponding **aux_mod** or

main_mod bit is low, the output is enabled but not modulated. With other words the device would output only a continuous wave signal.

Tx Outputs

Two Tx differential output ports are available:

- Differential low power, high linear output (nom. 0 dBm)
- Differential high power output (nom. 20 dBm)

The low power output can be used to drive an external PA to generate a high power RF signal. The internal high power output can be used to directly drive an antenna suitable for applications with low to medium read range requirements.

Low Power Output

The differential low power, high linear RF outputs (~0dBm) are intended to be used for driving an external amplifier. The RF outputs composed of RFOPX and RFONX pins need external RF chokes connected to V_{DD_B}, decoupling capacitors and a Balun with 2:1 impedance ratio for optimal operation in a 50 Ω system. The output is enabled by **eTX<1:0>** bits in the RF Output and LO Control Register ($0C_h$). By using these bits, it is possible to adjust current capability of the RF output pins.

High Power Output

The differential high power output pins are the outputs of the internal power amplifier outputs PAOUT_P and PAOUT_N. They require external RF chokes, connected to V_{DD_PA} and an impedance matching circuit for operation in a 50 Ω system. The amplifier is enabled by the **eTX<4>** and **eTX<3:2>** option bits in register $0C_h$. The bit **eTX<3:2>** also define the bias of the internal pre-amplifier stage. The PA supply regulator is automatically enabled when the internal PA is enabled. The bias current for the internal PA is defined by the option bits **pa_bias<1:0>** in the Regulator and PA Bias Register ($0B_h$).

Tx Operation Modes

TX Normal Mode

The baseband data is transferred to the 24 byte FIFO and all signal processing (protocol encoding, adding preamble or frame-sync, CRC, signal shaping, and modulation) is done internally. The data is then coded to the modulation pulse level and sent to the modulator. This means that the MCU has only to load the FIFO with data.

Transmission Start

There are three possibilities to start data transmission in the normal mode. One is data transmission can be triggered by sending related direct commands:

- Transmission with CRC (90_h)
- Transmission with CRC Expecting Header Bit (91_h)
- Transmission without CRC (92_h)

followed by information about the number of bytes that should be transmitted and the baseband data. The number of bytes needs to be written to the Tx Length Registers 1 - 2 ($3D_h$, $3E_h$) and the data itself should be put into the FIFO I/O Register ($3F_h$). Both can be done by one continuous WRITE operation. The transmission is started when the first data byte is completely written to the FIFO.

The second possibility is to trigger the transmission is with one of the direct commands related to the EPC Class1 Gen2 protocol:

- Inventory Commands:
  - Query (98_h)
  - QueryRep (99_h)
  - QueryAdjustUp ($9A_h$)
  - QueryAdjustNic ($9B_h$)
  - QueryAdjustDown ($9C_h$)
- ACK ($9D_h$)
- ReqRN ($9F_h$)

In this case, the transmission is started upon receiving the command.

The third possibility for data transmission is using one of the AutoACK modes. In this case the ACK or ReqRn is sent automatically in case previous reception was successful.

During data transmission, the **TX_status** bit in the FIFO Status Register (39_h) is set. When the data transmission is finished, the reader device signals an IRQ request with **Irq_TX** bit set high.

Protocol Adjustments

The EPC Class1 Gen 2 protocol allows adjustment of transmission parameters. The three supported Tari values are selected by changing the **Tari<1:0>** option bits in the Tx Options Register (02_h). The length of the high period of the (PIE encoded) logical one is selected by **TXOne<1:0>** option bits in the Tx Options Register (02_h). The session parameters for the direct command *Query (98_h)* is defined by the **S1** and **S0** option bits in the Tx Setting Register ($3C_h$). TRcal, which defines the

backscatter link frequency, is incorporated in the Query command transmission. TRcal is defined by option bits **TRcal<11:0>** in the TRcal Registers (04_h, 05_h).

Important: The software designer needs to take care that the bits **TRcal<11:0>, RX_LF<3:0>** and the **DR** bit in the transmission of the Query command are according to the Gen2 protocol. A precise description can be found in the EPC Class1 Gen2 or ISO18000-6C protocol description. In case TRcal data is required in normal transmission, it can be set by **Force_TRcal** option bit in the Tx Setting Register ($3C_h$). The cyclic redundancy check can be changed to CRC-5 instead of CRC-16. This is done in normal transmission by setting **TXCRC_5** option bit in the Tx Setting Register ($3C_h$) to high.

Transmission FIFO

The reader device supports two fully separate 24-byte FIFO buffer registers, one for transmission and one for reception. They share the same address. By writing to FIFO address $3F_h$ the data will be passed to transmission FIFO, while reading from the register address $3F_h$ will fetch the values from the reception FIFO. This approach allows starting a new transmission before the previously received data is read out by the MCU.

In case the data bytes to transmit exceed the size of the FIFO buffer, the MCU should initially fill the FIFO register with 24 bytes. The reader device starts the transmission and sends an interrupt request, signaled by **irq_fifo** in the Interrupt Register 1 (37_h), when only 6 bytes are left in the FIFO. When the interrupt is received, the MCU needs to read from register 37_h. By reading this register, the host system will know the cause for the interrupt and at the same time clears the interrupt bit. After this the MCU puts the remaining transmission data bytes to the FIFO considering the available FIFO size. In case all transmission data bytes were already sent to the FIFO, the host system waits until the last data byte has been sent. The end of the transmission is signaled to the MCU by the IRQ request **irq_TX** in register 37_h. The two Tx length registers ($3D_h$, $3E_h$) support incomplete byte transmission. The MCU needs to define the number of complete bytes and the number of the remaining bits that should be transmitted.

TX Direct Mode

Direct mode is used in case one wants to use only analog functions, bypassing all the protocol handling support of the reader device.

Entering and Terminating the Direct Mode

To enter the direct mode the direct command *Direct Mode (81_h)* should be sent followed by a NCS low-to-high transition. The direct mode remains active as long as NCS is kept high. To terminate the direct mode the direct command *Block Rx (96_h)* needs to be sent immediately after the NCS H-to-L transition. During the same or consecutive NCS low periods normal communication via the SPI interface is possible again.

Direct Mode Signals

The table below shows the re-assignments of the I/O pins during the direct mode. The different reception outputs options are related to the **dir_mode** option bit in the Protocol Selection Register (01_h).

Figure 24:
I/O Pin Reassignment in Direct Mode

Pin Name	Bit Stream and Bit Clock Output	Pin Name
MOSI	Tx data input	Tx data input
SCLK	Enable Rx input	Enable Rx input
MISO	Rx data output	I-Channel subcarrier output
IRQ	Rx bit clock output	Q-Channel subcarrier output

I/O Pin Reassignment: This figure shows I/O Pin Reassignment while operating in the direct mode.

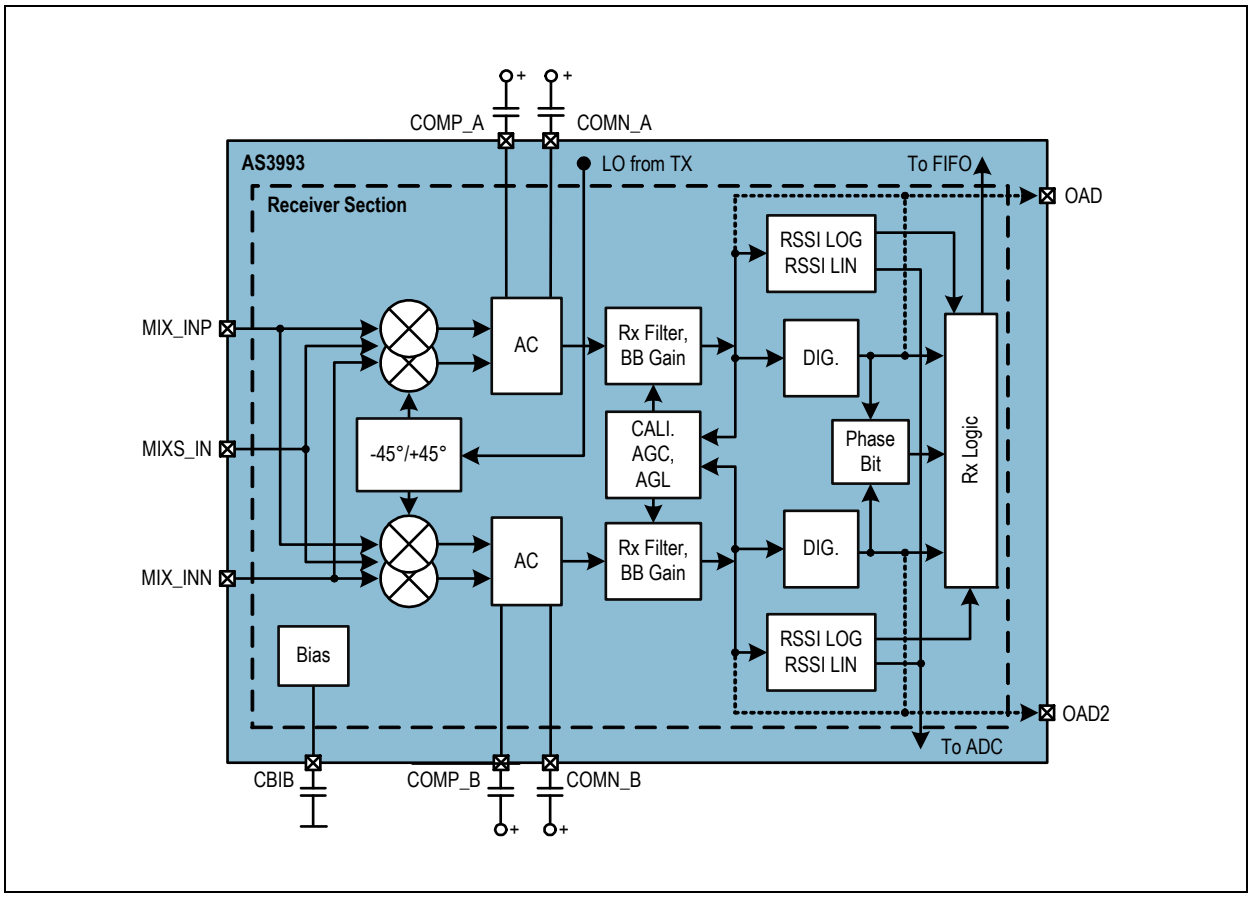
In the direct mode the MCU must directly control the transmission modulation input pin MOSI (Tx data input). The RF field is set to a high level in case MOSI is high and to low in case MOSI is low. The circuitry shapes the field according to the settings in the Modulator Control Registers 1 – 3 (13_h-15_h) and transmits the signal.

Receiver

The receiver section comprises of two input mixers followed by a fast AC coupling, gain and filtering stages, and a digitizer. The two received signals are fed then to the decision circuitry, the bit-decoder and the framer, where the preamble is removed and CRC is checked. The clean, framed baseband data is accessible for the MCU via the 24-byte FIFO I/O Register ($3F_h$).

The receiver section is activated by the option bits **rec_on** or **rf_on** from the Device Status Control Register (00_h). The typical bias settling time is 3 ms in case the reader device was previously in the normal mode (EN=H and **stby**=0). In case the **rec_on** bit is set together with the EN pin or a **stby** high-low change, the normal mode power-up timing prevails.

Figure 25:
Receiver Section



Block Diagram Receiver Section: This figure shows a detailed block diagram of the receiver section of the AS3993 device.

Input Mixers

The two input mixers are driven with 90° shifted LO signals and form an IQ demodulation circuit. By using an IQ demodulator architecture the AM-input signals are demodulated in the in-phase channel (I) while the PM-input signals are demodulated in the quadrature phase (Q) channel. The mixture of AM and PM-input signals is demodulated in both receiving channels. This configuration allows reliable operation regardless whether the transponder presents amplitude or phase modulation at receiver's input. With other words it suppresses communication holes caused by alternating modulation types. A differential input mixer and a single ended input mixer is available.

Differential Input Mixer

The pins MIX_INP and MIX_INN are the inputs for the differential Rx mixer. The inputs should be AC coupled to the external circuitry. At power-up the device automatically chooses the differential Rx mixer. In case the differential Rx mixer is not used the input pins should be shorted to ground. To optimize the receiver's noise and input range properties, the differential Rx mixer features settings to adjust the input range. Depending on the reflectivity of the environment and the antenna properties, the receiver's input RF voltage may increase to a level at which the differential Rx mixer operation gets corrupted. In such a case the input range can be extended by activating the internal input attenuator by setting the option bit **mix_ir<0>** in the Rx Mixer and Gain Register ($0A_h$) to high.

In case of low unwanted reflected power (self-jammer), the host system can increase the mixer conversion gain improving the overall sensitivity of the receiver by setting the option bit **mix_ir<1>**. The drawback of this setting is a reduced dynamic input range.

Additional settings in Emitter-Coupled Mixer Options Register (22_h):

- **emix_vr<0>:** (i2x) Increase differential Rx mixer range in mixer gain mode (~3dB)
- **emix_vr<1>**: (vsp_low) Adapts differential Rx mixer bias points to low supply
- **iadd_sink<2:0>**: Select differential Rx mixer load stage

Single Ended Input Mixers

The single ended input mixer has emitter-coupled input topology. The input MIXS_IN pin should have a DC path to GND and should be AC coupled for the RF input signal. The single ended input mixer needs to be activated by **s_mix** bit in the Miscellaneous Register 1 ($0D_h$).

Following options are available to optimize mixer operation for different mixer input ranges, sensitivity and current consumption requirements:

- **mix_ir<1:0>**: Select internal mixer impedance and gain in the Rx Mixer and Gain Register($0A_h$)
- **emix_vr<2:0>**: Select mixer input voltage range in the Emitter-Coupled Mixer Options Register (22_h)
- **id2x**, **id1x5**, **iadd_sink<2:0>**: Select mixer load stage current in the TRcal High Register (04_h) and the Emitter-Coupled Mixer Options Register (22_h)

Local Oscillator Path

To improve the phase noise rejection, the local oscillator signal can be derived from RFOPX, RFONX or the internal pre-amplifier stage of the internal PA. From which source the LO signal is tapped is selected by the **eTX<6>** option bit in the RF Output and LO Control Register ($0C_h$). In case one uses lower RF output levels than nominal, the LO signal can be increased by ~6 dB by setting the option bit **eTX<7>** to high. The drawback of this setting is an increase of received noise.

Fast AC Coupling

The internal patent pending feedback AC coupling system stores the DC operating points prior the start of the transmit modulation. After data transmission the system progressively adjusts the high pass time constant allowing a very fast settling time before reception. Such a system is required to accommodate the short Tx-to-Rx time needed for the highest bit rates in the EPC Class1 Gen 2 protocol.

Rx Filter

Filter Topology

The Rx filter is composed of four filter stages:

- 4th-order elliptic low-pass with notch characteristic to suppress neighboring channels at 500 kHz or 600 kHz. The filter can be configured to have its 1dB-compression point at 360 kHz for ETSI and at 280 kHz for FCC channel spacing in DRM operation. This filter stage allows one non-DRM setting:
  - 800 kHz low-pass corner frequency for BLF = 640 kHz.
- 2nd-order high-pass Chebyshev filter with an adjustable 1dB-compression point from 72 kHz to 200 kHz. This filter stage can be switched off (its gain stage only) for lower LF frequencies.
- 2nd-order low-pass Chebyshev filter with its 1dB-compression point at 360 kHz for ETSI and 280 kHz for FCC channel spacing in DRM operation. This filter stage allows three non-DRM settings:
  - 800 kHz low-pass corner frequency for BLF = 640 kHz
  - 180 kHz low-pass corner frequency for BLF = 160 kHz
  - 72 kHz low-pass corner frequency for BLF = 40 kHz

- 2nd-order high-pass Chebyshev filter with an adjustable 1dB-compression point from 72 kHz to 200 kHz. This filter stage can be reconfigured to 1st order high-pass with -3 dB frequency at 5.5 kHz or 12 kHz for the lower BLFs and FM0 coding.

Rx Filter Characteristics

Rx Filter characteristics are defined via the option bits in the Rx Filter Setting Register (09_h). The **hp<3:1>** option bits define the high-pass corner frequency and **lp<3:1>** define the low pass corner frequency. The bits **byp1** and **byp2** bypasses some stages allowing operation at lower back-scatter link frequencies. Since the settings of the different filter stages partially influence each other many different overall filter characteristics can be accomplished. Available register settings and their typical Rx filter characteristics are shown in the table below:

Figure 26:
Rx Filter Characteristics (Register 09_h)

Filter Setting	-3 dB HP Frequency	-3dB LP Frequency	Attenuation at 40 kHz	Attenuation at 600 kHz	Attenuation at 1.2 MHz
BLF = 640kHz					
reg09_h:00	220 kHz	770 kHz	-55 dB	-	-35 dB
reg09_h:07	80 kHz	770 kHz	-18 dB	-	-35 dB
BLF = 320kHz (ETSI DRM)					
reg09_h:20	200 kHz	380 kHz	-50 dB	-40 dB	-54 dB
reg09_h:27	75 kHz	380 kHz	-18 dB	-40 dB	-54 dB
BLF = 250kHz (FCC DRM)					
reg09_h:30	200 kHz	320 kHz	-50 dB	-45 dB	-55 dB
reg09_h:37	75 kHz	320 kHz	-18 dB	-45 dB	-55 dB
BLF = 160kHz					
reg09_h:3B	110 kHz	245 kHz	-	-52 dB	-56 dB
reg09_h:3F	55 kHz	245 kHz	-	-52 dB	-56 dB
BLF = 40 kHz					
reg09_h:FF	7 kHz	80 kHz	-	-60 dB	-55 dB

AS3993 Rx Filter Parameter: This figure shows relevant register settings for the AS3993 Rx filter characteristic.

Proposed Filter Settings

Not all filter settings might prove useful during operation. The table below shows proposed registers settings which provide optimal overall Rx filter characteristics for the supported link frequencies and Rx coding.

Figure 27:
Proposed Rx Filter Settings for Supported Link Modes

Link Frequency	Rx Coding	Register 09_h Settings
DRM Modes		
320 kHz	M4	24_h
	M8	
250 kHz	M4	34_h
	M8	
Other Supported Modes		
40 kHz	FM0	FF_h
	M2	
	M4	
	M8	
160 kHz	FM0	BF_h
	M2	$3F_h$
	M4	
	M8	
640 kHz	M4	04_h
	M8	

Proposed Rx Filter Settings: This figure shows Proposed Rx Filter Settings for the supported BFLs and Rx coding.

Rx Filter Calibration

To compensate process and temperature variations of the internal resistor and capacitor values, a filter calibration procedure is available. The calibration procedure is triggered by the direct command *Trigger Rx Filter Calibration (88_h)*. The calibration is finished after 5 ms (max.) and should be triggered after power-up, prior the first reception and later from time to time especially in case a significant temperature change has occurred. The result of this calibration is represented by the **lp_cal<3:0>** and **hp_cal<3:0>** status bits in the AGL / VCO / F_CAL

/ PilotFreq Status Register ($2C_h$) using **r2Cpage<1:0>** = 10_b. Typical calibration result values are 88_h. The automatically calibrated values can be adjusted by the direct commands *Decrease Rx Filter Calibration Data (89_h)* and *Increase Rx Filter Calibration Data ($8A_h$),* if the enabling option bit **f_cal_hp_chg** in the Miscellaneous Register 2 ($0E_h$) was set to high before. Note that **hp_cal<3:0>** affects the high pass part of the filter characteristic while **lp_cal<3:0>** affects the low pass part of the filter characteristic, both in 4% steps. Range is ±30%.

Rx Gain and Digitizer Hysteresis

The Rx gain in the receiving chain and digitizer hysteresis can be adjusted to optimize the signal to noise and interference ratio. There are three ways for adjustment:

1. Manual
2. AGC
3. AGL

Manual Adjustment

This adjustment method is done by setting option bits in the Rx Mixer and Gain Register ($0A_h$). The bits **gain<2:0>** increase the digitizer hysteresis by 3 dB per step (7 steps) and the bits **gain<5:4>** change the baseband amplifier gain by 3 dB per step (3 steps). The sign of the change (increase or decrease) is defined by the option bit **gain_sign**.

AGC

The built-in AGC comprises of a patent pending system that acts during the first periods of the incoming preamble. It partly changes the digitizer hysteresis (steps 1 - 4) and partly the baseband gain (steps 5 - 7). The hysteresis and baseband gain are changed equally for both channels maintaining the ratio between the I and Q channel so that the stronger signal is correctly digitized. The AGC can be enabled by setting the option bit **agc_on** in the Device Status Control Register (00_h) to high. The status of the AGC can be seen by the **agc<2:0>** status bits in the AGC and Internal Status Display Register ($2A_h$). The register value represents the number of 3 dB steps.

AGL

This adjustment is another possibility to decrease the sensitivity in case of bad reception conditions due to environmental noise and interferences. The AGL can be triggered by the direct command *AGL On ($A6_h$)*, during **rf_ok** = 1 after the direct command *Enable Rx (97_h)* has been sent and during a period when there is no actual transponder response pending. This means that the RF ramp-up must be finished and the receiver is ready to receive the interference signals. This automatic feature increases the digitizer hysteresis for each channel independently to the level that is just above

the noise and interference level. The maximum time required for the AGL action is 1 ms. The AGL result status for each channel can be seen by reading the **agl<5:0>** status bits in the AGL / VCO / F_CAL / PilotFreq Status Display Register ($2C_h$) using **r2Cpage<1:0>** = 00_b. The register values represent the number of 3 dB steps. There are 4 active steps available while steps 5 - 7 are inactive (0 dB). The AGL is disabled by *AGL Off ($A7_h$)* direct command. The result is stored and remains valid until the direct command *AGL Off ($A7_h$)* was sent.

The difference between AGC and AGL is that AGC is done each time at the beginning of the data packet reception, while AGL is done only at the moment when the direct command *AGL On ($A6_h$)* was sent. Both AGC and AGL operate on the **gain<2:0>** bits in the Rx Mixer and Gain Register ($0A_h$) and should be used exclusively. The manual setting has lower priority. In general, the system gain should be set to a level, that in good (normal) conditions only a small number of transitions occur on the digitizer output when no tag is transmitting. In such a case, also no AGL change would be seen.

IQ Selection

The two receiving signals are digitized and evaluated. The decision circuit selects the in-phase signal or quadrature signal channel, whichever presents the better received signal, for further processing. Which signal channel has been chosen can be seen by reading the **in_select** status bit in the AGC and Internal Status Display Register ($2A_h$). This Bit is valid from the end of the preamble until the start of the next transmission. For FM0 Rx encoding the selection is based on the evaluation of the digital representation of the received sub-carriers at the beginning of the data packet. For Miller Rx encoding the selection is supported by the logarithmic RSSI measurement. RSSI will be taken into account in case at least one RSSI reading (I or Q) is higher than defined by the **IQsel_Th<3:0>** option bits in the Interrogator Collision Detection and IQ Selection Settings Register ($1D_h$). Further improvements can be achieved by taking noise RSSI into account. To enable this mode - an active RF field and all mixer and gain settings as used for the subsequent reception, are required - send the direct commands *Enable Rx (97_h)* and *Store RSSI ($A8_h$)*. As a result only the difference between actual pilot RSSI and the stored noise RSSI will contribute to the IQ decision.

Bit Decoder

The bit decoder converts the sub-carrier coded signals to a bit stream data according to the protocol defined by the option bits **RX_cod<2:0>** and **RX_LF<3:0>** in the Rx Options Register (03_h). The system extracts the data clock and serial data bits, and removes the preamble. The decoder logic is designed for maximum error tolerance which allows successful decoding of partly corrupted sub-carrier signals due to noise or interference. In the EPC Class1 Gen2 protocol, the decoder supports long Rx preamble (TRext = 1) for FM0, and all Miller encoded signals. Short Rx preamble (TRext = 0) is supported for Miller4 and Miller8 encoded signals.

Data Framer

In the data framer, the serial bit stream is formatted into bytes. The CRC bytes are checked and removed leaving pure baseband data, which is sent to the 24-byte FIFO register from where it can be read out by the MCU. The receiver also supports transfer of incomplete bytes.

Data Reception Modes

The device can operate in the normal mode or in direct mode.

Rx Normal Mode

In the normal mode the received data is stored in FIFO.

Reception Start

The reception is triggered automatically at the end of the data transmission.

The second option to start the reception is done manually by sending the direct command *Enable Rx (97_h)*. For correct operation, the **dir_mode** bit in the Protocol Selection Register (01_h) should be set to 0.

Third possibility to start reception is using one of the AutoACK modes, which automatically triggers the reception to acquire PC+EPC and Handle.

Rx Wait Timer

The Rx wait timer defines a wait time between the end of data transmission and start of data reception. During this period, the decoder is not active. This prevents any incorrect detection that could occur due to transients that are caused by transmit operation, by noise or interference. The Rx wait time setting is done by the **RXw<7:0>** option bits in the Rx Wait Time Register (08_h). The step size for the Rx wait time is 6.4 µs.

Rx No Response Timer

The Rx no response timer starts with the reception slot of the anti-collision algorithm until a tag response arrives. In case no tag response is received during the defined time, the reception terminates and an IRQ is triggered with the **Irq_noresp** bit set. In case the **e_irq_noresp** option bit in the Enable Interrupt Register 1 (35_h) is set, the reception is not terminated by the Rx No Response Timer. Therefore the reception needs to be terminated manually by sending the direct command *Block Rx (96_h)*. This mode is aimed for commands where the response time can be long or not defined. The Rx no response timer is controlled by the Rx No Response Time Register (07_h). This time is defined in 25.6 µs steps. In case the timer is set to FF_h the Rx no response time is fixed to 26.2 ms.

Decoder Operation

During data reception the **Rx_status** bit in the FIFO Status Register (39_h) is set to high and when the data transmission is finished, the reader device issues an IRQ request with the **Irq_RX** bit set. In the Rx FIFO buffer 24 bytes can be stored. In case the number of received data bytes is more than 18, an IRQ request with the **Irq_fifo** bit set to high (register 37_h) signals the MCU that data should be removed from the FIFO. If an error in the data format or in the CRC is detected, the MCU is alerted by an IRQ request with the **Irq_err** bit set to high. Information about the cause for the error can be read from the Interrupt Register 2 (38_h). In case of a reception error, the system still receives the expected number of bits, to maintain a similar time flow for the reader and the tags.

Rx Length Register

Typically the expected reception length should be defined before the reception start. If this is not the case the reception length is updated during the reception when the actual length becomes available. When the reception is triggered at the end of normal data transmission (direct commands *90_h, 91_h, 92_h*), the reception length needs to be defined by the **RXl<11:0>** option bits in the Rx Length Registers 1 – 2 ($3A_h$, $3B_h$).

For the direct Query commands (*98_h, 99_h, $9A_h$, $9B_h$, $9C_h$*), the Rx length is predefined to 16 bits for the awaited RN16. For the direct command *ReqRN ($9F_h$)* the Rx length is internally set to 32 bits in order to receive handle and CRC. Only during the reception of the PC + EPC the reception length is not known in advance. To cover this case, the internal protocol logic checks the first received byte and adjusts the Rx length according to the value found in the first PC byte. In case reception is triggered manually by the direct command *Enable Rx (97_h)*, the Rx length needs to be set by the **RXl<11:0>** option bits in the Rx Length Registers 1 – 2 ($3A_h$, $3B_h$). If one of the AutoACK procedures is used, the Rx length is automatically set for all tag responses received during the automatic inventory command sequence.

In case the automatically set Rx length does not fit the actual tag data length, possibly due to future protocol extensions or custom tag functionality, the MCU can change the expected Rx length during reception. In case of automatically set PC+EPC length, the length change is possible after the second received byte. The MCU can request an additional interrupt after receiving two bytes (PC part of the PC+EPC field). The MCU can read out the two bytes that define the length of the on-going reception and update the Rx length register. The IRQ request after the 2nd byte is enabled by the **fifo_dir_irq2** option bit in the Rx Length Register 1 *($3A_h$)*. The side effect of this mode is that CRC bytes become available in the FIFO as well. That the second byte actually has been received is signaled by the **Irq_2nd_byte** IRQ bit set to high in the Interrupt Register 1 (37_h). If the actual Rx length becomes available even later, it is possible to prolong the 2nd byte interrupt functionality to trigger additional IRQ requests after the 4th, 6th … received byte by setting the **rep_irq2** option bit in the Rx Length Register 1 *($3A_h$)*. When the interrupt after the targeted number of received bytes is received, clearing the **rep_irq2** option bit prevents extra interrupts for the rest of the reception.

For some Gen2 commands the tag can reply with a normal response or an error code. The two types of responses are different in length. For further MCU relieve the **auto_errcode_RXI** option bit was prepared. When this option bit is set, the protocol logic checks the received header bit and adjusts its expected reception length to 41 bits (Gen2 error response length) in case it detects an error code reception.

RN16 Register

In the EPC Class1 Gen2 protocol, the timing between a tag response and the subsequent reader command in the inventory round is relatively short. To relieve the MCU of reading the RN16 (or handle) from the FIFO and then writing it back to the FIFO, a special register for storing the last received RN16 was built into the device. The RN16 is stored after the last successful reception upon one of the direct Query commands. The last stored RN16 is automatically used in the ACK command.

AutoACK Mode

The AutoACK modes automatically perform the inventory command sequence for one transponder. The aim is relieve the MCU of time critical tasks by minimizing the number of interactions between the MCU and the reader device. The AutoACK modes are enabled by setting the **AutoACK<1:0>** option bits in the Protocol Selection Register (01_h). Following modes are available:

- **AutoACK<1:0>** = 00_b: Query only
- **AutoACK<1:0>** = 01_b: Each query command is followed by an ACK
- **AutoACK<1:0>** = 10_b: Each query command is followed by an ACK and ReqRN

The automatic inventory command sequence is triggered by the direct Query commands *(98_h, 99_h, $9A_h$, $9B_h$, $9C_h$)*. After successful RN16 reception, it automatically prepares and triggers the acknowledge command ACK and subsequent receptions. After successful reception of the PC+EPC, it automatically prepares and triggers the request for a handle (ReqRN) It also prepares the appropriate Rx length settings and provides the received data (PC+EPC, Handle) in the FIFO. The MCU reads out the baseband data and triggers next Query command to continue the inventory round or another tag command that can be used in tag open state.

The number of interrupts that needs to be serviced by the host system (MCU) is minimized:

- **Irq_noresp** is signaled in case nothing is received.
- **Irq_fifo** is signaled in case EPC is longer than 18 bytes. It informs that data should be read out from the FIFO.
- **Irq_RX** is signaled at the end of the EPC and Handle reception. This also tells that one AutoACK step has been finished. Available data should be read out from the FIFO buffer in case of no error.
- **Irq_AutoACK** is signaled at the end of the AutoACK procedure, meaning that a RN16 was received and that at least the ACK command was issued during the sequence.
- **Irq_err** is signaled in case an error occurred during the procedure.

To successfully control the inventory round, the host system needs to distinguish between empty anti-collision slots and collided slots:

- **Irq_noresp** without **Irq_AutoACK** means that there was no response to a Query command. This presents a real empty slot in the inventory procedure.
- **Irq_noresp** with **Irq_AutoACK** or **Irq_err** with **Irq_AutoACK** means that RN16 was received, and that the empty slot or reception error happened later in the procedure. Probably some unidentified transponders are present in the field. But it could also mean that for particular settings and conditions, the filtered received noise level is above the digitizing hysteresis threshold and that the system recognizes it as tag signal.

The AutoACK function uses the Rx No Response Time Register (07_h) and Rx Wait Time Register (08_h) as they are used in other normal mode reception cases. An additional timer is used to define the T_2 time according to the EPC Class1 Gen2 protocol. This time is defined in the AutoACK Wait Time Register (06_h). The timer is started at the end of the reception period and defines when the subsequent data transmission is triggered.

Normal Mode with Test Outputs

Following possibilities in the Measurement Control Register (10_h) are available to observe operation in normal mode and during board debugging:

- Digitized sub-carrier signals of both receiving channels (I and Q) are enabled by setting the option bits **Tcomb<1:0>** = 01_b. Outputs are OAD and OAD2.
- The Tx modulation output and the selected digitized sub-carrier signal channel are enabled by setting the option bits **Tcomb<1:0>** = 10_b. Outputs are OAD (TX) and OAD2 (Rx).
- Analog sub-carrier signals of both receiving channels (I and Q) are enabled by setting the option bits **e_anaout<1:0>** = 01_b. Outputs are OAD and OAD2. Analog output has lower priority than the digital output.

Rx Direct Mode

Reception in the direct mode is triggered by setting the pin SCLK (Enable Rx input) to high. When receiving data from a tag in direct mode, there are three possibilities depending on option bits setting:

- Internally decoded bit stream and bit clock according to the protocol is enabled by **dir_mode = 0** and defined by the option bits **prot<2:0>** in the Protocol Selection Register (01_h), **RX_cod<2:0>** and **RX_LF<3:0>** option bits in the Rx Options Register (03_h). The outputs are the pins MISO and IRQ.
- Digitized sub-carrier signals of both receiving channels (I and Q) are enabled by setting the option bit **dir_mode** in the Protocol Selection Register (01_h) to high. The outputs are the pins MISO and IRQ.
- Analog sub-carrier signals of both receiving channels (I and Q) are enabled by setting the option bits **e_ anaout<1:0>** in the Measurement Control Register (10_h) to 01_b. The outputs are the pins OAD and OAD2.

For details on how to enter the direct mode and the re-assignments of the I/O pins in this mode please refer to the TX Direct Mode section.

Modes Supporting Tuning of Antenna or Directivity Device

A good possibility to achieve low reflected Tx power is to actively tune the antenna or the directivity device. To allow for correct tuning the amplitude and the phase information of the incoming reflected power is available through the output DC levels of the two mixers. The analog representation of the two mixer DC level outputs are available on the OAD and OAD2 outputs by setting **e_anaout<1:0> = 10_b** in the Measurement Control Register (10_h). In case one does the tuning during reception, the Enable_RX signal is required to know when the receiver is enabled. This information is available on ADC pin in case **Tcomb<1:0>** = 11_b in the Measurement Control Register (10_h). Another approach to acquire the tuning data is to read the digital representation of the reflected power level as described in the A/D Converter section.

Logarithmic RSSI

The receiver section comprises of two logarithmic RSSI (Received Signal Strength Indicator) blocks. They are connected to the outputs of both signal channels (I and Q). The value of each RSSI reading is stored during the data reception at the second received byte in the RSSI Display Register ($2B_h$) using **r2Bpage<3:0>** = 0110_b. The RSSI result is valid until the start of the next transmission.

A/D Converter

An 8-bit on board A/D converter supports an external power detector and allows to be connected to the internal diagnostic circuitry. The input range is ±1V, centered at the AGD voltage (1.6 V). The 7 LSB bits give information about the absolute output level, while the MSB bit act as a sign bit. The sign bit set to high indicates positive values while a low means negative values. The source for A/D conversion is selected through the **msel<3:0>** option bits in the Measurement Control Register (10_h). The conversion is triggered by the direct command *Trigger AD conversion (87_h)* and the result is available through the ADC Readout / Regulator Setting Display Register ($2D_h$) using **r2Dpage<1:0>** = 00_b (register 29_h). The A/D conversion is finished after 20 µs and an IRQ request is sent with the **Irq_cmd** option bit set (register 38_h).

External RF Power Detector

An external RF power detector can be placed after the PA or at the input coupled port of a directional coupler. This allows to measure actual RF output power. The resulting analog voltage from the power detector can be connected to the ADC pin of the reader device. The digital representation of this voltage level can be acquired with the on board A/D converter using **msel<3:0>** = 0011_b (register 10_h).

Reflected RF Power Indicator

The receiver comprises of an input RF level indicator. This is used for diagnostic purposes of the circuitry or for detecting environmental difficulties around the antenna. Reflections from poor antennas (S_{11}), the reflective antenna's environment and directional device leakage increase the carrier level (self-jammer level) at the mixer input. Since a higher carrier level causes an increase of demodulated noise, it is mandatory to keep the unwanted carrier level at the mixer input at a minimum. The reflected carrier that is seen on the two mixers inputs is down-converted to zero frequency. The two DC levels on the mixers outputs are proportional to the input RF level and can be used as a measure for the RF input level. The mixer DC levels are also dependent on the carrier input phase. The two mixer DC output levels can be connected to the on-board A/D converter by setting the option bits **msel<3:0>** = 0001_b and 0010_b. The **id2x** and **id1x5** option bits adapt the gain of the reflected RF power level indicator.

Supply Voltage Measurement

The A/D converter can be also used to measure the supply voltages V_{EXT}, V_{EXT_PA}, V_{DD_B}, and V_{DD_PA}. Depending on the conversion results the MCU can decide on the voltage regulator setting strategy. The selected voltage is connected to A/D converter input (V_{INPUT}) by setting the option bit to **msel<3:0>:**

- V_{EXT} : 0111_b
- V_{DD_B} : 1000_b
- V_{EXT_PA} : 1001_b
- V_{DD_PA} : 1010_b

The conversion is started by the direct command *Trigger AD conversion (87_h)* and the result is available in the ADC Readout / Regulator Setting Display Register ($2D_h$) using **r2Dpage<1:0>** = 00_b (register 29_h).

The conversion result follows the equation:

$$\text{ADCRegisterValue} = \frac{[(V_{INPUT} - 1.6) \cdot 0.8 - 1.6]}{0.0079}$$

Where the ADC Register Value is the value in register $2D_h$ and V_{INPUT} is the analog voltage present at the A/D converter input in volts.

Linear RSSI with Sub-Carrier Phase Bit

The demodulated peak-to-peak voltages of both signal channels (I and Q) are connected to a double sample and hold circuit and are sampled at the end of the tag-preamble (pilot tone). They can be A/D converted during or after the reception. The MCU can convert and read out the two voltages using the internal linear A/D converter by setting the option bits **msel<3:0>** = 1011_b and **msel<3:0>** = 1100_b (register 10_h) and triggering the conversion by the direct command *Trigger AD conversion (87_h)*. The results are available in the ADC Readout / Regulator Setting Display Register ($2D_h$) using **r2Dpage<1:0>** = 00_b (register 29_h). For the linear RSSI, the sampled voltages are shifted to use the whole ADC range. The minimum sample value gives -127 as ADC result and the maximum sample value gives +127 as ADC result. The status bit **subc_phase** in the AGC and Internal Status Display Register ($2A_h$) shows whether the two sampled peak-to-peak voltages (I and Q) were in phase or in anti-phase at the moment of sampling. The phase bit is valid from the end of pilot tone till the end of reception and should be read out before the end of reception. Using the linear (absolute) I and Q RSSI values and the phase bit information the systems allows detecting the RSSI phase information within.

Internal Signal Level Detectors

An internal signal level detector is placed at the output of the internal VCO and therefore allows measuring the internal RF carrier level. The selected source is connected to A/D converter input through the option bits **msel<3:0>** = 0100_b. For a description of the conversion procedure please refer to the A/D converter description. The internal signal level detector is meant for diagnostic purposes only and should not be used for measurement of the output power.

Interrogator Anti-Collision Support

To enable the ISO 29143 functionality, a RSSI based interrogator anti-collision support is prepared. The feature is enabled by the direct command Interrogator Anti-collision Support Enable (AA_h). According to the ISO 29143 proposal, the system monitors the RSSI envelope of the received sub-carrier signals and informs the MCU in case at least in a part of the received data packet the RSSI level exceeded the predefined threshold. Besides it stores RSSI and timing data of the data packet at relevant points.

Following RSSI values are stored:

- RSSI at pilot tone
- RSSI at data
- Maximum RSSI value in the telegram

Following timing data is stored:

- First time at which the predefined threshold was exceed
- Threshold exceedance duration
- Time of first protocol violation

Time is related to the received bits.

The predefined collision detection threshold is in the **ICD_Th<3:0>** bits in the Interrogator Collision Detection and IQ Selection Settings Register ($1D_h$). To enable the functionality the direct command *Interrogator Anti-collision Support Enable (AA_h)* needs to be sent. To disable it the *Interrogator Anti-collision Support Disable (AB_h)* direct command should be used. To clear the peak RSSI value and timing data again use the *Interrogator Anti-collision Support Disable (AB_h)* direct command.

Register Description

Register Overview

The 6-bit long register addresses are shown in the hexadecimal notation. There are two types of registers implemented in the reader device. Read/Write registers and read-only display registers. They can be accessed via the serial interface.

Figure 28:
Register Overview

Register Address (hex)	Register Name	Register Type
Main Control Registers		
00_h	Device Status Control Register	RW
01_h	Protocol Selection Register	RW
Configuration Registers		
02_h	Tx Options Register	RW
03_h	Rx Options Register	RW
04_h	TRcal High Register	RW
05_h	TRcal Low Register	RW
06_h	AutoACK Wait Time Register	RW
07_h	Rx No Response Time Register	RW
08_h	Rx Wait Time Register	RW
09_h	Rx Filter Setting Register	RW
$0A_h$	Rx Mixer and Gain Register	RW
$0B_h$	Regulator and PA Bias Register	RW
$0C_h$	RF Output and LO Control Register	RW
$0D_h$	Miscellaneous Register 1	RW
$0E_h$	Miscellaneous Register 2	RW
10_h	Measurement Control Register	RW
11_h	VCO Control Register	RW
12_h	CP Control Register	RW
13_h	Modulator Control Register 1	RW
14_h	Modulator Control Register 2	RW

Register Address (hex)	Register Name	Register Type
15_h	Modulator Control Register 3	RW
16_h	Modulator Control Register 4	RW
17_h	PLL Main Register 1	RW
18_h	PLL Main Register 2	RW
19_h	PLL Main Register 3	RW
$1A_h$	PLL Auxiliary Register 1	RW
$1B_h$	PLL Auxiliary Register 2	RW
$1C_h$	PLL Auxiliary Register 3	RW
$1D_h$	Interrogator Collision Detection and IQ Selection Settings Register	RW
22_h	Emitter-Coupled Mixer Options Register	RW
Status Registers		
29_h	Status Readout Page Setting Register	RW
$2A_h$	AGC and Internal Status Display Register	R
$2B_h$	RSSI Display Register	R
$2C_h$	AGL / VCO / F_CAL / PilotFreq Status Display Register	R
$2D_h$	ADC Readout / Regulator Setting Display Register	R
$2E_h$	Command Status Display Register	R
33_h	Version Register	R
Interrupt Registers		
35_h	Enable Interrupt Register 1	RW
36_h	Enable Interrupt Register 2	RW
37_h	Interrupt Register 1	R
38_h	Interrupt Register 2	R
Communication Registers		
39_h	FIFO Status Register	R
$3A_h$	Rx Length Register 1	RW
$3B_h$	Rx Length Register 2	RW
$3C_h$	Tx Setting Register	RW

Register Address (hex)	Register Name	Register Type
$3D_h$	Tx Length Register 1	RW
$3E_h$	Tx Length Register 2	RW
$3F_h$	FIFO I/O Register (deep)	Tx: W Rx: R

Register Overview: This figure lists all available register for the AS3993 device including their addresses and register types.

Main Control Registers

In the Register Description tables the bit names along with their default value after device power-up (EN=L). A short function description and comment are given.

Figure 29:
Device Status Control Register

Address #00_h, Device Status Control Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	stby	0	Stand-by mode	**0:** Normal mode **1:** Standby mode
6	RFU	0	Not used	RFU, do not set
5	RFU	0	Not used	RFU, do not set
4	RFU	0	Not used	RFU, do not set
3	RFU	0	Not used	RFU, do not set
2	agc_on	0	AGC enable	**0:** AGC OFF **1:** AGC ON
1	rec_on	0	Receiver enable	**0**: The receiver is disabled **1**: The receiver is enabled
0	rf_on	0	Transmitter and receiver enable	**0**: Tx RF field and receiver are disabled **1**: Tx RF field and receiver are enabled

Device Status Control Register: This figure describes the option bits of register 00_h.

Figure 30:
Protocol Selection Register

Address #01_h, Protocol Selection Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	RX_crc_n	0	Receiving without CRC	**0:** Rx with CRC **1:** Rx without CRC
6	dir_mode	0	Decoder mode type	**0:** Normal operation **1:** Disables any decoding and signal sensing automatics in the receiver. It is advised to set this bit high when continuous analog measurements are performed.
5	AutoACK<1>	0	AutoAck mode	**00_b:** No Auto ACK **01_b:** AutoACK **10_b:** AutoACK+ReqRN **11_b:** RFU, do not set
4	AutoACK<0>	0		
3	RFU	0	Not used	RFU, do not set
2	prot<2>	0	Protocol selection	**000_b**: EPC Class1 Gen2/ISO18000-6C **001_b**: ISO18000-6 Type A/B direct mode decoder enable **Others**: RFU, do not set
1	prot<1>	0		
0	prot<0>	0		

Protocol Selection Register: This figure describes the option bits of register 01_h.

Configuration Registers

Figure 31:
Tx Options Register

Address #02$_h$, Tx Options Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	RFU	0	Not used	RFU, do not set
6	RFU	0	Not used	RFU, do not set
5	TXOne<1>	1	Tx one length control	**00$_b$:** 1.50 * Tari **01$_b$:** 1.66 * Tari **10$_b$:** 1.83 * Tari **11$_b$:** 2.00 * Tari
4	TXOne<0>	1		
3	RFU	0	Not used	RFU, do not set
2	Tari<2>	0	Tari definition	**000$_b$:** Tari = 6.25 µs **001$_b$:** Tari =12.5 µs **010$_b$:** Tari =25 µs **Others:** RFU, do not set
1	Tari<1>	1		
0	Tari<0>	0		

Tx Options Register: This figure describes the option bits of register 02$_h$.

Figure 32:
Rx Options Register

Address #03$_h$, Rx Options Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	RX_LF<3>	1	Link frequency	**0000$_b$**: 40 kHz **0110$_b$**: 160 kHz **1001$_b$**: 250 kHz **1100$_b$**: 320 kHz **1111$_b$**: 640 kHz **Other**: RFU, do not set
6	RX_LF<2>	1		
5	RX_LF<1>	0		
4	RX_LF<0>	0		
3	TRext	1	Rx preamble length	**0:** Short preamble **1:** Long preamble Short preamble is supported for Miller 4 and Miller 8 coding.
2	RX_cod<2>	0	Rx coding	**000$_b$:** FM0 **001$_b$:** M2 **010$_b$:** M4 **011$_b$:** M8 **Others:** RFU, do not set
1	RX_cod<1>	1		
0	RX_cod<0>	0		

Rx Options Register: This figure describes the option bits of register 03$_h$.

Figure 33:
TRcal High Register

Address #04$_h$, TRcal High Register (TRcal definition for Gen2 / Miscellaneous)				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	low_vsp_lo	0	low_vsp_lo	**1:** Adaptation to low supply for the LO phase shifter
6	id2x	0	id2x	Adapt gain 2x of the reflected RF power level (mixer DC level) indicator
5	id1x5	0	id1x5	Adapt gain 1.5x of the reflected RF power level (mixer DC level) indicator
4	RFU		Not used	RFU, do not set
3	TRcal<11>	0	**TRcal<11:0>** bits define TRcal time	Description in register 05$_h$
2	TRcal<10>	0		
1	TRcal<9>	1		
0	TRcal<8>	0		

TRcal High Register: This figure describes the option bits of register 04$_h$.

Figure 34:
TRcal Low Register

Address #05$_h$, TRcal Low Register (TRcal definition for Gen2)				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	TRcal<7>	1	**TRcal<11:0>** bits define TRcal time	Range: **0.1 µs** - **409 µs** Steps: **4096** Step size: **0.1 µs** Worst case relative resolution in Gen 2 range: $\frac{0.1\mu s}{17.2\mu s} \approx 0.6\,\%$ Gen2 defines a range from **17.2 µs** to **225 µs**
6	TRcal<6>	0		
5	TRcal<5>	0		
4	TRcal<4>	1		
3	TRcal<3>	1		
2	TRcal<2>	0		
1	TRcal<1>	1		
0	TRcal<0>	1		

TRcal Low Register: This figure describes the option bits of register 05$_h$.

Figure 35:
AutoACK Wait Time Register

Address #06_h, AutoACK Wait Time Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	Auto_T2<7>	0	EPC protocol time T_2 according to EPC C1 Gen2	Time used in the AutoACK procedure. Range: **0 – 816 µs** Step size: **3.2 µs.**
6	Auto_T2<6>	0		
5	Auto_T2<5>	0		
4	Auto_T2<4>	0		
3	Auto_T2<3>	0		
2	Auto_T2<2>	1		
1	Auto_T2<1>	0		
0	Auto_T2<0>	0		

AutoACK Wait Time Register: This figure describes the option bits of register 06_h.

Figure 36:
Rx No Response Time Register

Address #07_h: Rx No Response Time Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	NoResp<7>	0	Defines the timeout after which the no response interrupt is sent. It starts at the end of Tx.	Step size: **25.6 µs** Range: **25.6 µs** – **6502 µs** (**1 - 254**). **255**: No response time: **26.2 ms.** Interrupt is sent in case the time runs out before 6 - 10 periods of link frequency (tag preamble) are detected. T_1 = 25.6 µs - 262 µs. Default = 15 * 25.6 µs = 384 µs. Gen2 WRITE command: 20 ms max.
6	NoResp<6>	0		
5	NoResp<5>	0		
4	NoResp<4>	0		
3	NoResp<3>	1		
2	NoResp<2>	1		
1	NoResp<1>	1		
0	NoResp<0>	1		

Rx No Response Time Register: This figure describes the option bits of register 07_h.

Figure 37:
Rx Wait Time Register

Address #08_h: Rx Wait Time Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	RXw<7>	0	Rx wait time. Defines the time during which the Rx input is ignored. It starts from the end of Tx.	Step size: **6.4 µs** Range: **6.4 µs** – **1632 µs** (1 - 255), **00_h:** The receiver is enabled immediately after Tx Gen2: T_{1min} = 11.28 µs - 262 µs. ISO1800-6A: 150 µs - 1150µs ISO1800-6B: 85 µs - 460µs Default = 7 * 6.4 µs = 44.8 µs.
6	RXw<6>	0		
5	RXw<5>	0		
4	RXw<4>	0		
3	RXw<3>	0		
2	RXw<2>	1		
1	RXw<1>	1		
0	RXw<0>	1		

Rx Wait Time Register: Defines the time after Tx when the Rx input is disregarded.

Figure 38:
Rx Filter Setting Register

Address #09_h: Rx Filter Setting Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	byp2	0	Bypass 2	For details refer to Rx Filter section
6	byp1	0	Bypass 1	
5	lp<3>	1	Low pass setting	
4	lp<2>	0		
3	lp<1>	0		
2	hp<3>	1	High pass setting	
1	hp<2>	0		
0	hp<1>	0		

Rx Filter Setting Register: This figure describes the option bits of register 09_h.

Figure 39:
Rx Mixer and Gain Register

Address #0A$_h$: Rx Mixer and Gain Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	gain<5>	0	Baseband gain change	Steps: 4 Step Size:3 dB **00$_b$**: 0 dB **11$_b$**: 9 dB Increase/decrease defined by **gain_sign** option bit
6	gain<4>	0		
5	gain_sign	0	Sign bit for BB gain settings (**gain<5:4>**)	**0:** Decrease baseband gain **1:** Increase baseband gain
4	gain<2>	0	Digitizer hysteresis increase	Steps: 5 Step Size: 3 dB **000$_b$:** 0 dB **100b:** 12 dB **Other:** RFU, do not set
3	gain<1>	0		
2	gain<0>	0		
1	mix_ir<1>	0	Mixer gain and input range selection	Differential Rx mixer: • **00$_b$**: Nominal gain • **01$_b$**: 8 dB attenuation • **10$_b$**: 10 dB gain increase Single ended Rx mixer: • **00$_b$**: 6 dB mixer gain decrease • **01$_b$**: Nominal gain • **11$_b$**: 6 dB mixer gain increase
0	mix_ir<0>	1		

Rx Mixer and Gain Register: This figure describes the option bits of register 0A$_h$.

Figure 40:
Regulator and PA Bias Register

Address #0B$_h$: Regulator and PA Bias Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	pa_bias<1>	0	Increase internal PA bias	**1:** Increase bias four times
6	pa_bias<0>	0	Increase internal PA bias	**1:** Increase bias two times
5	rvs_rf<2>	0	V_{DD_PA} regulator voltage settings	Manual settings: Steps equal to **rvs<2:0>** For correct operation the regulator voltage drop should be 300 mV or more. **Min: 000$_b$:** 2.7 V **Max: 111$_b$:** 3.4 V Steps: 8 Step size: 0.1 V Automatic setting: Output voltage results from the target voltage drop defined by **rvs<2:0>** or by manual settings **rvs_rf<2:0>**, whichever yields lower output voltage Automatic mode is triggered by the direct command (A2$_h$).
4	rvs_rf<1>	1		
3	rvs_rf<0>	1		
2	rvs<2>	0	Other regulators voltage setting	Manual setting: For correct operation the regulator voltage drop should be 300 mV or more. **Min: 000$_b$:** 2.7 V **Max: 111$_b$:** 3.4 V Steps: 8 Step size: 0.1 V Automatic setting: **001$_b$:** Target voltage drop >250 mV, **011$_b$:** Target voltage drop >300 mV, **111$_b$:** Target voltage drop >350 mV. Automatic mode is triggered by the direct command (A2$_h$).
1	rvs<1>	1		
0	rvs<0>	1		

Voltage Regulator Register: This figure describes the option bits of register 0B$_h$.

Figure 41:
RF Output and LO Control Register

Address #0C$_h$: RF Output and LO Control Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	eTX<7>	0	LO (local oscillator) gain	**0:** Nominal **1:** 6 dB gain in LO path
6	eTX<6>	0	LO source selection	**0:** LO source is RFOPX, RFONX **1:** LO source is pre-driver for the internal PA
5	eTX<5>	0	Enable internal V_{DD_PA} voltage regulator	V_{DD_PA} regulator is automatically enabled in case the internal PA is enabled via **eTX<3:2>**
4	RFU	0	Not used	RFU, do not set
3	eTX<3>	0	Main PA enable and bias current for main PA pre-driver	**00_b:** Disable **01_b:** 7 mA **10_b:** 14 mA **11_b:** 22 mA
2	eTX<2>	0		
1	eTX<1>	1	Enable RF low power output and bias current for RF output stage.	**00_b:** Disable **01_b:** 7 mA **10_b:** 14 mA (default) **11_b:** 22 mA
0	eTX<0>	0		

RF Output and LO Control Register: This figure describes the option bits of register 0C$_h$.

Figure 42:
Miscellaneous Register 1

Address #0D$_h$: Miscellaneous Register 1				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	hs_output	1	Strong, fast communication output drivers	Valid for MISO, IRQ, CLSYS
6	hs_oad	0	Strong, fast test output drivers	Valid for OAD, OAD2, ADC
5	miso_pd2	0	Pull down resistor: NCS = 0	**1:** Enable a pull down resistor on MISO, when NCS is low and MISO is not driven by the AS3993
4	miso_pd1	0	Pull down resistor: NCS = 1	**1:** Enable a pull down resistor on MISO when NCS is high
3	open_dr	0	Open drain N-MOS outputs	Valid for MISO, IRQ, CLSYS
2	s_mix	0	Single-ended mixer input enable	**0:** Differential input **1:** Single ended input
1	RFU	0	Not used	RFU, do not set
0	RFU	0	Not used	RFU, do not set

Miscellaneous Register 1: This figure describes the option bits of register 0D$_h$.

Figure 43:
Miscellaneous Register 2

Address #0E$_h$: Miscellaneous Register 2				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	xosc<1>	0	Reference frequency oscillator mode selection	**00_b:** Normal operation with auto power saving mode **01_b:** External sinus TCXO AC coupled to OSCO **10_b:** Disable auto power saving mode **11_b:** RFU, do not set
6	xosc<0>	0		
5	RFU	0	Not used	RFU, do not set
4	RFU	0	Not used	RFU, do not set
3	f_cal_hp_chg	0	Change the Rx filter calibration	**1:** Enables changing the hp calibration **0:** Enables changing the lp calibration Use direct commands: • *Decrease Rx Filter Calibration Data (89_h)* • *Increase Rx Filter Calibration Data ($8A_h$).*
2	clsys<2>	1	CLSYS output frequency	**000_b:** Off **100_b:** 4 MHz **001_b:** 5 MHz **010_b:** 10 MHz **011_b:** 20 MHz **Others:** RFU, do not set
1	clsys<1>	0		
0	clsys<0>	0		

Miscellaneous Register 2: This figure describes the option bits of register $0E_h$.

Figure 44:
Measurement Control Register

Address #10_h: Measurement Control Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	Tcomb<1>	0	Digital test output modes	**00_b:** Disable **01_b:** Digitized Rx sub-carriers outputs on OAD, OAD2 **10_b:** Tx modulation and selected Rx sub-carrier outputs on OAD, OAD2 **11_b:** Enable Rx output on ADC
6	Tcomb<0>	0		
5	e_anaout<1>	0	Analog test output modes	**00_b:** Disable **01_b:** Analog sub-carrier out on OAD, OAD2 **10_b:** Analog mixer DC output on OAD, OAD2 **11_b:** RFU, do not set
4	e_anaout<0>	0		
3	msel<3>	0	ADC measurement selection	**0001_b:** Mixer DC level I-channel **0010_b:** Mixer DC level Q-channel **0011_b:** ADC pin **0100_b:** Internal RF level **0111_b:** V_{EXT} level **1000_b:** V_{DD_B} level **1001_b:** V_{EXT_PA} level **1010_b:** V_{DD_PA} level **1011_b:** RSSI I level **1100_b:** RSSI Q level **1111_b:** RFOPX, RFONX power level **0000_b:** NC
2	msel<2>	0		
1	msel<1>	0		
0	msel<0>	0		

Measurement Control Register: This figure describes the option bits of register 10_h.

Figure 45:
VCO Control Register

Address #11_h: VCO Control Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	mvco	0	VCO measurement enable	Steps: 7 Result in register $2C_h$ **r2Cpage<1:0> = 01_b**
6	eosc<2>	1	Internal oscillator bias current	8 steps, **Step size:** 0.52 mA **000_b:** Minimum bias current (~1.3 mA) **111_b:** Maximum bias current (~5 mA)
5	eosc<1>	0		
4	eosc<0>	0		
3	vco_r<3>	0	Manual VCO range selection	Manual selection of the VCO range segment
2	vco_r<2>	0		
1	vco_r<1>	0		
0	vco_r<0>	0		

VCO Control Register: This figure describes the option bits of register 11_h.

Figure 46:
CP Control Register

Address #12_h: CP Control Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	LF_R3<7>	0	Loop filter R3-selection	**00_b:** 30 kΩ (default) **01_b:** 50 kΩ **10_b:** 70 kΩ **11_b:** 100 kΩ
6	LF_R3<6>	0		
5	LF_C3<5>	0	Loop filter C3-selection	**000_b:** 20 pF (default) **001_b:** 40 pF **010_b:** 60 pF **011_b:** 80 pF **100_b:** 100 pF **101_b:** 130 pF **110_b:** 160 pF **111_b:** 200 pF
4	LF_C3<4>	0		
3	LF_C3<3>	0		
2	cp<2>	1	Charge pump current	**000_b:** 150 µA **001_b:** 300 µA **010_b:** 600 µA **011_b:** 1200 µA **100_b:** 1350 µA (default) **101_b:** 1500 µA **110_b:** 1800 µA **111_b:** 2350 µA
1	cp<1>	0		
0	cp<0>	0		

CP Control Register: This figure describes the option bits of register 12_h.

Figure 47:
Modulator Control Register 1

Address #13_h: Modulator Control Register 1				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	RFU	0	Not used	RFU, do not set
6	main_mod	0	Modulation connected to high power output	Enables the modulation of the high power outputs.
5	aux_mod	1	Modulation connected to low power output	Enables the modulation of the low power outputs.
4	RFU	0	Not used	RFU, do not set
3	RFU	0	Not used	RFU, do not set
2	e_lpf	0	Enable low pass filter for the modulation signal	To further smooth the modulation signal
1	ask_rate<1>	0	ASK modulation transient rate change.	**00_b:** Tari determined **01_b:** Use every 2nd modulator value. **10_b:** Use every 4th modulator value. **11_b:** Use every 8th modulator value.
0	ask_rate<0>	0		

Modulator Control Register 1: This figure describes the option bits of register 13_h.

Figure 48:
Modulator Control Register 2

Address #14$_h$: Modulator Control Register 2				RW
Bit	**Name**	**Default**	**Function**	**Comments**

7	ook_ask	1	100% ASK enable with variable delimiter length and delimiter shape selection	Delimiter shape if **pr_ask** = 1:
				• Tari = 25 µs:
				  • **0**: PR-ASK shaped delimiter transient
				  • **1**: ASK shaped delimiter transient
				• Tari = 6.25 µs or 12.5 µs:
				  • ASK shaped delimiter transient (regardless of this bit setting)(1).
				Delimiter shape if **pr_ask** = 0:
				ook_ask should be set to 1,
				100% ASK shaped delimiter transient

6	pr_ask	0	PR-ASK enable	Enables PR-ASK Tx modulation. If this bit is set to low ASK modulation is used.
5	del_len<5>	0	ASK / PR-ASK delimiter length adjustment	Adjust delimiter length. Range: 9.6 µs to 15.9 µs. Step size: 0.1 µs. Default 1D$_h$ = 12.5 µs.
4	del_len<4>	1		
3	del_len<3>	1		
2	del_len<2>	1		
1	del_len<1>	0		
0	del_len<0>	1		

Modulator Control Register 2: This figure describes the option bits of register 14$_h$.

Note(s):

1. The Tx spectrum is not affected to a visible level due to ASK delimiter transient.

Figure 49:
Modulator Control Register 3

Address #15$_h$: Modulator Control Register 3				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	trfon<1>	0	RF ON/OFF transition time	**00$_b$:** Tari determined **01$_b$:** 100 µs **10$_b$:** 200 µs **11$_b$:** 400 µs
6	trfon<0>	0		
5	lin_mod	0	Selects linear modulation transient	**1**: Linear modulation transient **0**: Sinusoidal shaped modulation transient
4	TX_lev<4>	0	Tx output level coarse adjustment. For low and high power outputs	**00$_b$:** 0 dB, nominal **01$_b$:** -8 dB **10$_b$:** -12 dB **11$_b$:** RFU, do not set
3	TX_lev<3>	0		
2	TX_lev<2>	0	Tx output level fine adjustment. For low and high power outputs	**000$_b$:** Nominal **001$_b$:** -1 dB **111$_b$:** -7 dB Step size: -1 dB
1	TX_lev<1>	0		
0	TX_lev<0>	0		

Modulator Control Register 3: This figure describes the option bits of register 15_h.

Figure 50:
Modulator Control Register 4

Address #16$_h$: Modulator Control Register 4				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	1stTari<7>	0	1st Tari high period length	Adjust 1st Tari high period following the delimiter Range: 5F$_h$ - 9D$_h$, Step size: 50ns (Tari = 6.25 µs) 100ns (Tari = 12.5 µs) 200ns (Tari = 25 µs)
6	1stTari<6>	1		
5	1stTari<5>	1		
4	1stTari<4>	1		
3	1stTari<3>	1		
2	1stTari<2>	1		
1	1stTari<1>	1		
0	1stTari<0>	0		

Modulator Control Register 4: This figure describes the option bits of register 16_h.

Figure 51:
PLL Main Register 1

Address #17$_h$: PLL Main Register 1				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	RFU	0	Not used	RFU, do not set
6	RefFreq <2>	1	PLL reference divider	**100_b:** 125 kHz **101_b:** 100 kHz **110_b:** 50 kHz **111_b:** 25 kHz **Others:** RFU, do not set
5	RefFreq <1>	1		
4	RefFreq <0>	0		
3	mB_val<9>	0	PLL main divider, value B, MSB part	See register 18_h
2	mB_val<8>	1		
1	mB_val<7>	0		
0	mB_val<6>	0		

PLL Main Register 1: This figure describes the option bits of register 17_h.

Figure 52:
PLL Main Register 2

Address #18$_h$: PLL Main Register 2				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	mB_val<5>	0	PLL main divider, value B, LSB part	A and B values for the 32/33 Prescaler Dividing ratio: $N = B*32 + A*33$ Proposed A/B ratio: $\frac{1}{3}$ … 3 Example: A value: 282_d ($11A_h$) B value: 252_d ($0FC_h$) N = 17340 PLL reference divider = 50 kHz Carrier frequency = 867 MHz
6	mB_val<4>	1		
5	mB_val<3>	1		
4	mB_val<2>	0		
3	mB_val<1>	1		
2	mB_val<0>	0		
1	mA_val<9>	0	PLL main divider value A, MSB part	
0	mA_val<8>	0		

PLL Main Register 2: This figure describes the option bits of register 18_h.

Figure 53:
PLL Main Register 3

Address #19$_h$: PLL Main Register 3				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	mA_val<7>	1	PLL main divider, value A, LSB part	See register 18$_h$
6	mA_val<6>	1		
5	mA_val<5>	1		
4	mA_val<4>	1		
3	mA_val<3>	1		
2	mA_val<2>	1		
1	mA_val<1>	0		
0	mA_val<0>	0		

PLL Main Register 3: This figure describes the option bits of register 19$_h$.

Figure 54:
PLL Auxiliary Register 1

Address #1A$_h$: PLL Auxiliary Register 1				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	RFU	0	Not used	RFU, do not set
6	RFU	0		
5	RFU	0		
4	RFU	0		
3	xB_val<9>	0	PLL auxiliary divider, value B, MSB part	See register 1B$_h$
2	xB_val<8>	1		
1	xB_val<7>	0		
0	xB_val<6>	0		

PLL Auxiliary Register 1: This figure describes the option bits of register 1A$_h$.

Figure 55:
PLL Auxiliary Register 2

Address #1B$_h$: PLL Auxiliary Register 2				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	xB_val<5>	0	PLL auxiliary divider, value B, LSB part	A and B values for the 32/33 Prescaler Dividing ratio: $N = B*32 + A*33$ Proposed A/B ratio: $\frac{1}{3}$ … 3 Example: A value: 282_d ($11A_h$) B value: 252_d ($0FC_h$) N = 17340 PLL reference divider = 50 kHz Carrier frequency = 867 MHz
6	xB_val<4>	1		
5	xB_val<3>	1		
4	xB_val<2>	0		
3	xB_val<1>	0		
2	xB_val<0>	0		
1	xA_val<9>	0	PLL auxiliary divider value A, MSB part	
0	xA_val<8>	1		

PLL Auxiliary Register 2: This figure describes the option bits of register 1B$_h$.

Figure 56:
PLL Auxiliary Register 3

Address #1C$_h$: PLL Auxiliary Register 3				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	xA_val<7>	0	PLL auxiliary divider, value A, LSB part	See register 1B$_h$
6	xA_val<6>	0		
5	xA_val<5>	0		
4	xA_val<4>	1		
3	xA_val<3>	1		
2	xA_val<2>	0		
1	xA_val<1>	0		
0	xA_val<0>	0		

PLL Auxiliary Register 3: This figure describes the option bits of register 1C$_h$.

Figure 57:
Interrogator Collision Detection and IQ Selection Settings Register

Address #1D$_h$: Interrogator Collision Detection and IQ Selection Settings Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	IQsel_Th<3>	0	Threshold for IQ selection	Supports signal channel selection by the logarithmic RSSI measurement. RSSI will be taken into account in case at least one RSSI reading (I or Q) is higher than defined by this threshold setting.
6	IQsel_Th<2>	0		
5	IQsel_Th<1>	0		
4	IQsel_Th<0>	0		
3	ICD_Th<3>	0	Threshold for ICD detection	Sets the collision detection RSSI threshold for the ISO 29143 protocol.
2	ICD_Th<2>	0		
1	ICD_Th<1>	0		
0	ICD_Th<0>	0		

Interrogator Collision Detection and IQ Selection Settings Register: This figure describes the option bits of register 1D$_h$.

Figure 58:
Emitter-Coupled Mixer Options Register

Address #22$_h$: Emitter-Coupled Mixer Options Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	ic_bia_m<1>	0	Decrease device bias	**00_b:** Nominal **01_b:** bias –3 % **10_b:** bias –6 % **11_b:** bias –9 %
6	ic_bia_m<0>	0		
5	iadd_sink<2>	0	Mixer sink current adjustment	Select mixer load stage current
4	iadd_sink<1>	0		
3	iadd_sink<0>	0		
2	emix_vr<2>	0	sr2	Single ended Rx mixer: **sr2, sr1, sr0**: Select mixer input voltage range Differential Rx mixer: **sr2:** RFU **sr1: vsp_low** (adapts mixer bias points to low supply). **sr0: i2x** (increases the mixer range in mixer gain mode by ~3dB).
1	emix_vr<1>	0	sr1	
0	emix_vr<0>	0	sr0	

Emitter-Coupled Mixer Options Register: This figure describes the option bits of register 22$_h$.

Status Registers

Figure 59:
Status Readout Page Setting Register

Address #29$_h$: Status Readout Page Setting Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	r2Dpage<1>	0	Register page selection for register 2D$_h$	Defines actual display of *ADC Readout/Regulator Setting Display Register (2D$_h$)*
6	r2Dpage<0>	0		
5	r2Cpage<1>	0	Register page selection for register 2C$_h$	Defines actual display of *AGL/VCO/F_CAL/PilotFreq Status Register (2C$_h$)*
4	r2Cpage<0>	0		
3	r2Bpage<3>	0	*Register page selection for register 2B$_h$* – For more details, please refer to AN13.	**0000$_b$:** Real time RSSI I,Q **0010$_b$:** RSSI-0-quiet (noise RSSI), I,Q Quiet level- Acquired by direct command *Store RSSI (A8$_h$)* **0100$_b$:** RSSI-1-pilot, I,Q Level at pilot **0110$_b$:** RSSI-2-data, I,Q Level at 2nd byte **1000$_b$:** RSSI-3-peak, I, Q Peak Level **1100$_b$:** IDC-Time - Time at exceeding threshold. **1101$_b$:** IDC-Length - Threshold exceeding duration. **1110$_b$:** Err-Time - Time at first protocol violation. Time is in terms of received bits. **Others:** not used
2	r2Bpage<2>	0		
1	r2Bpage<1>	0		
0	r2Bpage<0>	0		

Status Readout Page Setting Register: This figure describes the option bits of register 29$_h$.

Figure 60:
AGC and Internal Status Display Register

Address #2A$_h$: AGC and Internal Status Display Register			R
Bit	**Name**	**Function**	**Comments**
7	subc_phase	Sub-carrier phase	**0:** Sub-carriers are in anti-phase **1:** Sub-carriers are in phase
6	agc<2>	AGC status	Steps: 7 Step size: 3 dB
5	agc<1>		
4	agc<0>		
3	in_select	Shows the source of the sub-carrier signal that is used for decoding	**0:** I-Channel **1:** Q-Channel Value is valid from reception start until the start of the next transmission.
2	rf_ok	RF level stable	Indicates that the RF carrier is stable.
1	pll_ok	PLL locked	Indicates that the PLL is locked to the RF carrier frequency.
0	osc_ok	Crystal oscillator stable	Indicates that the reference oscillator frequency is stable.

AGC and Internal Status Display Register: This figure describes the status bits of register 2A$_h$.

Figure 61:
RSSI Display Register

Address #2B$_h$: RSSI Display Register			R
Bit	**Name**	**Function**	**Comments**
7	rssi<7>	RSSI value of Q channel – The RSSI type defined in *Status Readout Page Setting Register (29$_h$)*, bits **r2Bpage<3:0>**.	Displays the signal strength of the Q signal channel Steps: 16 Step size: 2 dB
6	rssi<6>		
5	rssi<5>		
4	rssi<4>		
3	rssi<3>	RSSI value of I channel – The RSSItype defined in *Status Readout Page Setting Register (29$_h$)*, bits **r2Bpage<3:0>**.	Displays the signal strength of the I signal channel Steps: 16 Step size: 2 dB
2	rssi<2>		
1	rssi<1>		
0	rssi<0>		

RSSI Display Register: This figure describes the status bits of register 2B$_h$.

Figure 62:
AGL / VCO / F_CAL / PilotFreq Status Display Register

Address #2C$_h$: r2Cpage<1:0> = 00$_b$ (register 29$_h$), AGL / VCO / F_CAL / PilotFreq Status Display Register			R
Bit	**Name**	**Function**	**Comments**
7	RFU	Not used	Status bit, read as 0
6	RFU	Not used	Status bit, read as 0
5	agl<5>	AGL status of Q channel	Available steps are 0, 1, 2, 3, 4 Step size: 3 dB Range: 0 dB – 12 dB Steps 5, 6, 7 have no action
4	agl<4>		
3	agl<3>		
2	agl<2>	AGL status of I channel	Available steps are 0, 1, 2, 3, 4 Step size: 3 dB Range: 0 dB – 12 dB Steps 5, 6, 7 have no action
1	agl<1>		
0	agl<0>		

AGL/ VCO/ F_CAL/ PilotFreq Status Display Register: This figure describes the status bits of register 2C$_h$ page 0.

Figure 63:
AGL / VCO / F_CAL / PilotFreq Status Register

Address #2C$_h$: r2Cpage<1:0> = 01$_b$ (register 29$_h$), AGL / VCO / F_CAL / PilotFreq Status			R
Bit	**Name**	**Function**	**Comments**
7	vco_ri<7>	VCO automatic range select result	Displays the result of the internal VCO automatic range selection procedure. Steps: 16
6	vco_ri<6>		
5	vco_ri<5>		
4	vco_ri<4>		
3	vco_ri<3>	Set to logic 1	RFU, read as 1
2	vco_ri<2>	VCO pin voltage measurement result	Displays the result of the internal VCO measurement. Steps: 7 Range: 0 V to V_{DD_A}
1	vco_ri<1>		
0	vco_ri<0>		

AGL / VCO / F_CAL / PilotFreq Status: This figure describes the status bits of register 2C$_h$ page 1.

Figure 64:
AGL / VCO / F_CAL / PilotFreq Status Register

Address #2C$_h$: r2Cpage<1:0> = 10$_b$ (register 29$_h$), AGL / VCO / F_CAL / PilotFreq Status			R
Bit	**Name**	**Function**	**Comments**
7	hp_cal<3>	High pass calibration data	Steps: 16 Step size: 4 %
6	hp_cal<2>		
5	hp_cal<1>		
4	hp_cal<0>		
3	lp_cal<3>	Low pass calibration data	Steps: 16 Step size: 4 %
2	lp_cal<2>		
1	lp_cal<1>		
0	lp_cal<0>		

AGL / VCO / F_CAL / PilotFreq Status: This figure describes the status bits of register 2C$_h$ page 2.

Figure 65:
ADC Readout / Regulator Setting Display Register

Address #2D$_h$: r2Dpage<1:0> = 00b (register 29$_h$), ADC Readout / Regulator Setting Display Register			R
Bit	**Name**	**Function**	**Comments**
7	adc<7>	ADC readout. AD converter input is selected using **msel<3:0>** bits. The conversion is triggered by the direct command *Trigger AD conversion (87$_h$)*. The result is valid 20 µs later.	Via ADC the two mixers output DC levels can be measured showing the reflectivity of the antenna or the environment. Also a DC level on the ADC pin can be measured. The latter case can be used to monitor the RF output power via an external power detector.
6	adc<6>		
5	adc<5>		
4	adc<4>		
3	adc<3>		
2	adc<2>		
1	adc<1>		
0	adc<0>		

ADC Readout / Regulator Setting Display Register: This figure describes the status bits of register 2D$_h$ page 0.

Figure 66:
ADC Readout / Regulator Setting Display Register

Address #2D$_h$: r2Dpage<1:0> = 01b (register 29$_h$), ADC Readout / Regulator Setting Display Register			R
Bit	**Name**	**Function**	**Comments**
7	tcxo	Reference oscillator detection	**0:** OSCI AC coupled: Crystal mode detected **1:** OSCI shorted to ground: TCXO mode detected
6	RFU	Not used	Status bits, each default set to 0
5	RFU		
4	RFU		
3	RFU		
2	vs<2>	Voltage setting used by the circuitry	**000$_b$:** 2.7 V **111$_b$:** 3.4 V Steps: 8 Step size: 0.1 V
1	vs<1>		
0	vs<0>		

ADC Readout / Regulator Setting Display Register: This figure describes the status bits of register 2D$_h$ page 1.

Figure 67:
Command Status Display Register

Address #2E$_h$: Command Status Display Register			R
Bit	**Name**	**Function**	**Comments**
7	storeRSSI_done	Storing the RSSI value completed	Signals the completion of the direct commands *Store RSSI (A8$_h$)* and *Clear RSSI (A9$_h$)*. Triggers IRQ.
6	autovco_done	VCO range selection finished	Signals the completion of the direct commands *Automatic VCO Range Selection (A4$_h$)* and *Manual VCO Range Selection (A5$_h$)*. Triggers IRQ.
5	autosupp_done	Automatic supply selection finished	Signals the completion of the direct commands *Automatic Power Supply Level Setting (A2$_h$)* and *Manual Power Supply Level Setting (A3$_h$)*. Triggers IRQ.
4	f_cal_done	Rx filter calibration finished	Signals the completion of the direct command *Trigger Rx Filter Calibration (88$_h$)*. Triggers IRQ.
3	ad_conv_done	A/D conversion finished	Signals the completion of the direct command *Trigger AD conversion (87$_h$)*. Triggers IRQ.
2	intrgAC_supp	Anti-Collision Support	Interrogator anti-collision support enabled
1	AGL_on	AGL enabled	Signals the completion of the direct command *AGL On (A6$_h$)* and *AGL Off (A7$_h$)*
0	aux_PLL_ sel	Auxiliary PLL setting selected	Signals the completion of the direct commands *Hop to Main Frequency (84$_h$)* and *Hop to Auxiliary Frequency (85$_h$)*

Command Status Display Register: This figure describes the status bits of register 2E$_h$.

Figure 68:
Version Register

Address #33$_h$: Version Register			R
Bit	**Name**	**Function**	**Comments**
7	Version<7>		Device version number, preset to 61$_h$
6	Version<6>		
5	Version<5>		
4	Version<4>		
3	Version<3>		
2	Version<2>		
1	Version<1>		
0	Version<0>		

Version Register: This figure shows the bits of the version register 33$_h$.

Interrupt Registers

Figure 69:
Enable Interrupt Register 1

Address #35$_h$: Enable Interrupt Register 1				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	e_irq_TX	1	Enables corresponding interrupts of the *Interrupt Register 1 (37_h)*	When enabled the IRQ pin is set to 1 in case the corresponding IRQ occurs.The IRQ bits of registers 37_h and 38_h are always set.
6	e_irq_Rx	1		
5	e_irq_fifo	1		
4	e_irq_err	1		
3	e_irq_header	0		
2	RFU	1		
1	e_irq_AutoACK	1		
0	e_irq_noresp	1		In case **irq_noresp** interrupt is disabled, the receive operation is never interrupted by the No Response Timer.

Enable Interrupt Register 1: This figure describes the option bits of register 35_h.

Figure 70:
Enable Interrupt Register 2

Address #36$_h$: Enable Interrupt Register 2				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	e_irq_ana	0	Enables corresponding interrupts of *Interrupt Register 2 (38_h)*	When enabled the IRQ pin is set to 1 in case the corresponding IRQ occurs. The IRQ bits of registers 37_h and 38_h are always set.
6	e_irq_cmd	1		
5	RFU	0	Not used	RFU, do not set
4	RFU	0		
3	RFU	0		
2	e_irq_err1	0	interrupts of *Interrupt Register 2 (38_h)*	When enabled the IRQ pin is set to 1 in case the corresponding IRQ occurs. The IRQ bits of registers 37_h and 38_h are always set.
1	e_irq_err2	0		
0	e_irq_err3	0		

Enable Interrupt Register 2: This figure describes the option bits of register 36_h.

Figure 71:
Interrupt Register 1

Address #37$_h$: Interrupt Register 1			R
Bit	**Name**	**Function**	**Comments**
7	Irq_TX	IRQ due to the end of Tx	An interrupt is generated when Tx is finished.
6	Irq_Rx	IRQ due to the end of Rx	An interrupt is generated when Rx is finished.
5	Irq_fifo	FIFO fill level	Less than 6 bytes in FIFO during Tx or more than 18 bytes in FIFO during Rx
4	Irq_err	IRQ set due to an error	Signaling a reception or transmission error
3	Irq_header / Irq_2nd_byte	Header bit / 2nd byte	Received header bit is high / Two bytes already in the FIFO – in case fifo_dir_irq2 = 1 (Register 1A$_h$)
2	RFU	Not Used	
1	Irq_AutoACK	Auto ACK finished	AutoACK is finished. Bit is set to 1 in the following cases: The AutoACK procedure was successfully finished. In the AutoACK procedure the ACK command was sent and the procedure was terminated due to a No Response IRQ. In the AutoACK procedure the ACK command was sent and procedure was terminated due to a reception error.
0	Irq_noresp	No response interrupt	Signals the MCU that the No Response Timer expired, it also interrupts receive operation

Interrupt Register 1: This figure describes the status bits of register 37$_h$.

Note(s):

1. The content of this register is set to 0 at power up and when EN = low. It is automatically reset at the end of a read phase. A reset also removes the IRQ flag.

Figure 72:
Interrupt Register 2

Address #38$_h$: Interrupt Register 2			R
Bit	**Name**	**Function**	**Comments**
7	Irq_ana	IRQ due to an change of the oscillator, PLL, or RF field status	To present a change of the status of **osc_ok**, **pll_ok**, **rf_ok**. The interrupt is triggered on both edges.
6	Irq_cmd	IRQ due to end of direct command execution	
5	RFU	Not used	
4	RFU		
3	RFU		
2	Irq_err1	CRC error	CRC error
1	Irq_err2	Rx data length. error / protocol violation	Signals the MCU that the reception was shorter than expected (see Rx length register definition ($3A_h$, $3B_h$) or an error caused by a disabled command or protocol violation was observed during reception.
0	Irq_err3	Preamble detect error / FIFO overflow error	Signals to MCU that there was an error during preamble detection or FIFO overflow happened during reception or transmission.

Interrupt Register 2: This figure describes the status bits of register 38_h.

Note(s):

1. The content of this register is set to 0 at power up and when EN=L. It is automatically reset at the end of read phase. The reset also clears the IRQ flags.
2. The IRQ pin stays high as long as at least one of the enabled IRQ bits is set in any of the two IRQ registers. Typically the MCU knows where it can expect the IRQ, and can read that register first.
3. The main error bit Irq_err (37_h) is a separate IRQ bit which is triggered by any of the error interrupt sources. The same sources are also connected to the error sub-bits Irq_err1, Irq_err2, Irq_err3 (38_h).
4. Optimal usage in the inventory round is having main Irq_err enabled (e_irq_err=1) and error sub-bits disabled (e_irq_err1=e_irq_err2=e_irq_err3=0). In this case it is sufficient to read only (37_h) to clear the IRQ line to continue the inventory round. In case one is interested on the type of the error, the error sub-bits can be checked afterwards.

Communication Registers

Figure 73:
FIFO Status Register

Address #39_h: FIFO Status Register			R
Bit	**Name**	**Function**	**Comments**
7	TX_status	Tx status	**1:** Shows that a data transmission is in progress.
6	Rx_status	Rx status	**1:** Shows that a data reception is in progress.
5	Fovfl	FIFO overflow	**1:** More than 24 bytes were loaded to one of the FIFOs
4	Fb<4>	FIFO bytes	Number of bytes loaded in FIFO that has not been read out yet. In case an empty FIFO is read out the value $1F_h$ is displayed in the **Fb<4:0>** bits.
3	Fb<3>		
2	Fb<2>		
1	Fb<1>		
0	Fb<0>		

FIFO Status Register: This figure describes the status bits of register 39_h.

Figure 74:
Rx Length Register 1

Address #3A$_h$: Rx Length Register 1				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	Rx_crc_n2	0	Receiving without CRC	Temporary receiving without CRC.
6	fifo_dir_irq2	0	Direct FIFO and 2nd byte IRQ	All bytes including CRC are transferred to FIFO, **irq_header** is changed to irq_ 2ndbyte. For PC+EPC manual reception length setting.
5	rep_irq2	0	Repeat 2nd byte IRQ	Enables IRQ after 4th, 6th… received byte. Bit can be set to 0 during reception when additional IRQs are not required. The aim is to support XPC words.
4	auto_errcode_Rxl	0	Automatic tag error code Rx length preset	In case received header bit is set to 1, the Rx length is automatically changed to the tag error code length (41bits). Used to change the previously expected Rx length information when a tag transmits the error code instead of a normal response.
3	Rxl<11>	0	Rx length MSB part	
2	Rxl<10>	0		
1	Rxl<9>	0		
0	Rxl<8>	0		

Rx Length Register 1: This figure describes the option bits of register 3A$_h$.

Figure 75:
Rx Length Register 2

Address #3B$_h$: Rx Length Register 2				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	RxI<7>	0	Rx length LSB part, number of bits	In case short direct commands are used the register is automatically preset to correct expected reception length. 16 bits are expected for commands 98$_h$, 99$_h$, 9A$_h$, 9B$_h$, 9C$_h$; 32 bits are expected for the direct command 9F$_h$. In other cases the host system should set the expected length.
6	RxI<6>	0		
5	RxI<5>	0		
4	RxI<4>	0		
3	RxI<3>	0		
2	RxI<2>	0		
1	RxI<1>	0		
0	RxI<0>	0		

Rx Length Register 2: This figure describes the option bits of register 3B$_h$.

Figure 76:
Tx Setting Register

Address #3C$_h$: Tx Setting Register				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	RFU	0	Not used	RFU, do not set
6	RFU	0		
5	RFU	0		
4	RFU	0		
3	TXCRC_5	0	Tx CRC type	**0:** CRC-16 **1:** CRC-5
2	Force_TRcal	0	TRcal period in normal transmission	Normally TRcal is automatically transmitted when the direct command *Query* (98_h), according to EPC Gen2 and ISO18000-6C, is issued. In case Force_TRcal = 1 the TRcal period is transmitted also in normal data transmission (direct commands 90_h, 91_h)
1	S1	0	Session bits	Used for Gen 2 direct commands Query (98_h).
0	S0	0		

Tx Setting Register: This figure describes the option bits of register $3C_h$.

Figure 77:
Tx Length Register 1

Address #3D$_h$: Tx Length Register 1				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	TXl<11>	0	Tx length high nibble	High and mid nibbles of complete bytes being transmitted through the FIFO
6	TXl<10>	0		
5	TXl<9>	0		
4	TXl<8>	0		
3	TXl<7>	0	Tx length mid nibble	
2	TXl<6>	0		
1	TXl<5>	0		
0	TXl<4>	0		

Tx Length Register 1: This figure describes the bits of register 3D$_h$.

Figure 78:
Tx Length Register 2

Address #3E$_h$: Tx Length Register 2				RW
Bit	**Name**	**Default**	**Function**	**Comments**
7	TXl<3>	0	Tx length low nibble	Low nibbles of complete bytes to be transmitted through FIFO
6	TXl<2>	0		
5	TXl<1>	0		
4	TXl<0>	0		
3	Bb<2>	0	Number of bits in broken byte	Number of bits in the last (broken) byte to be transmitted
2	Bb<1>	0		
1	Bb<0>	0		
0	RFU	0	Not used	RFU, do not set

Tx Length Register 2: This figure describes the bits of register 3E$_h$.

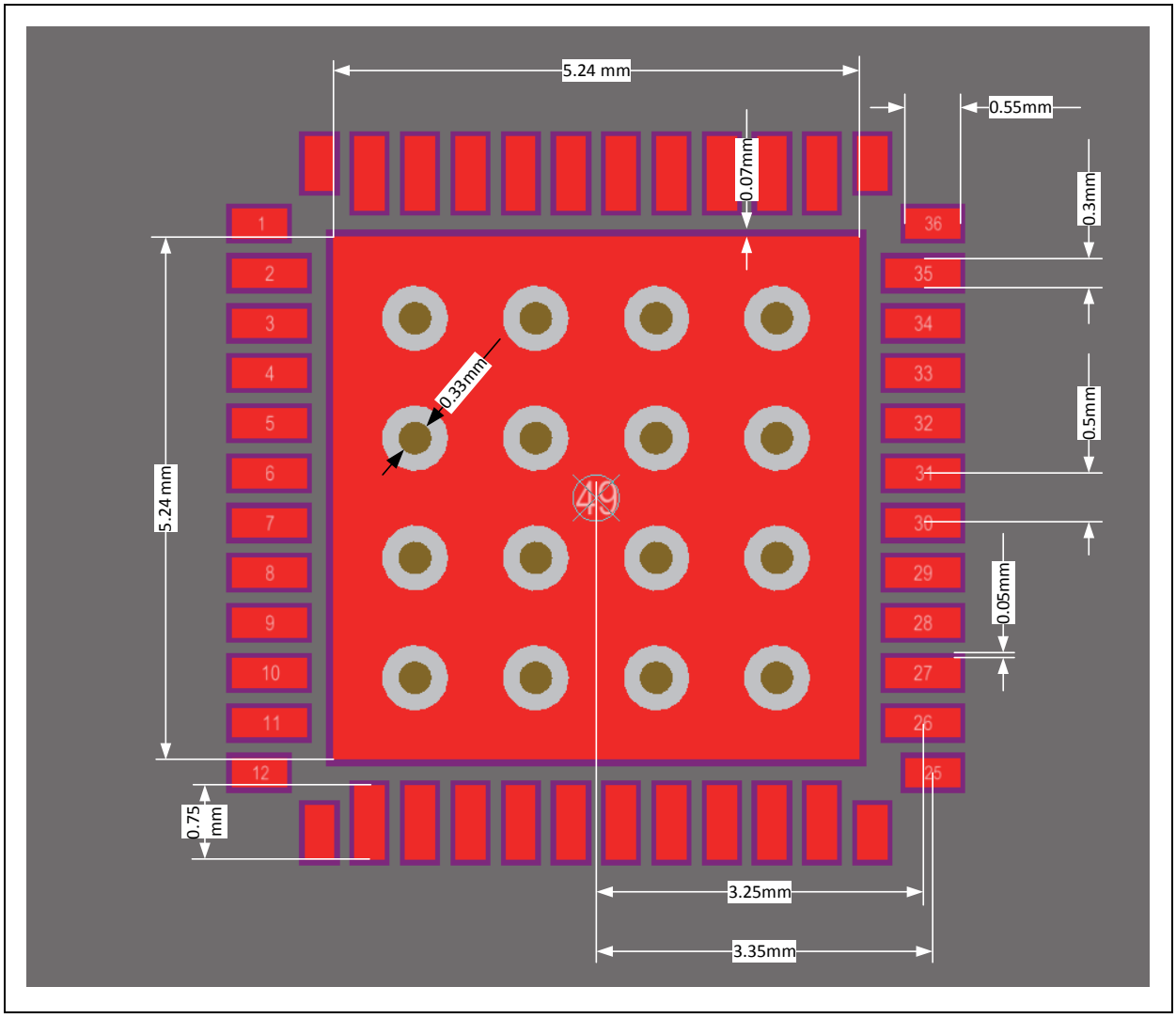
Figure 79:
FIFO I/O Register

Address #3F$_h$: FIFO I/O Register			RW
Bit	**Name**	**Function**	**Comments**
	FIFO	2 x 24 bytes FIFO register filled and read in cyclic way	

FIFO I/O Register: This figure describes the bits of register 3F$_h$.

PCB Pad Layout

Figure 80:
Recommended PCB Pad Layout



AS3993 PCB Pad Layout : This figure shows the recommended PCB land pattern of the AS3993 device.

Soldering Information

Stencil Design and Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.
2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.
3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN thermal pad area as shown in Figure 81.
4. The aperture opening for the signal pads should be between 50-80% of the QFN pad area as shown in Figure 82.
5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.
7. No-clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water-soluble flux is used.

Figure 81:
Solder Paste Application on Paddle

Solder Paste Paddle Pattern: Solder paste should be applied through an array of squares (or circles) which totals 50 % of the total area of the paddle.

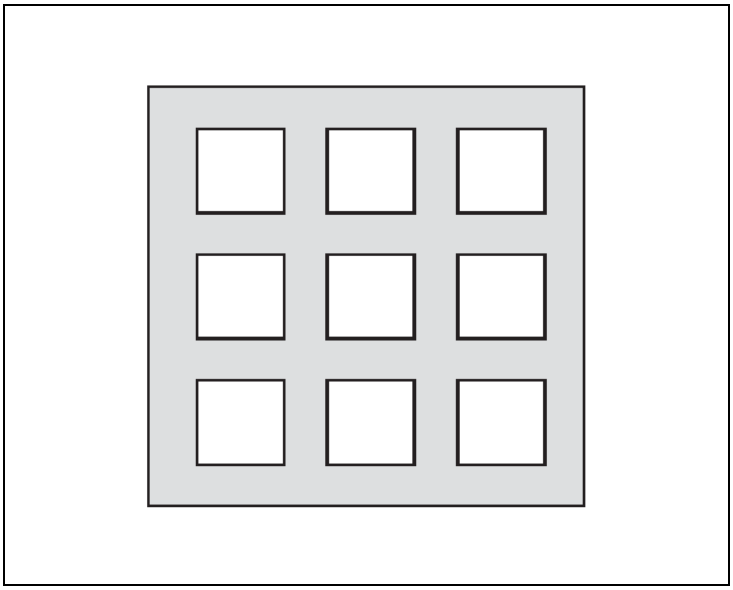
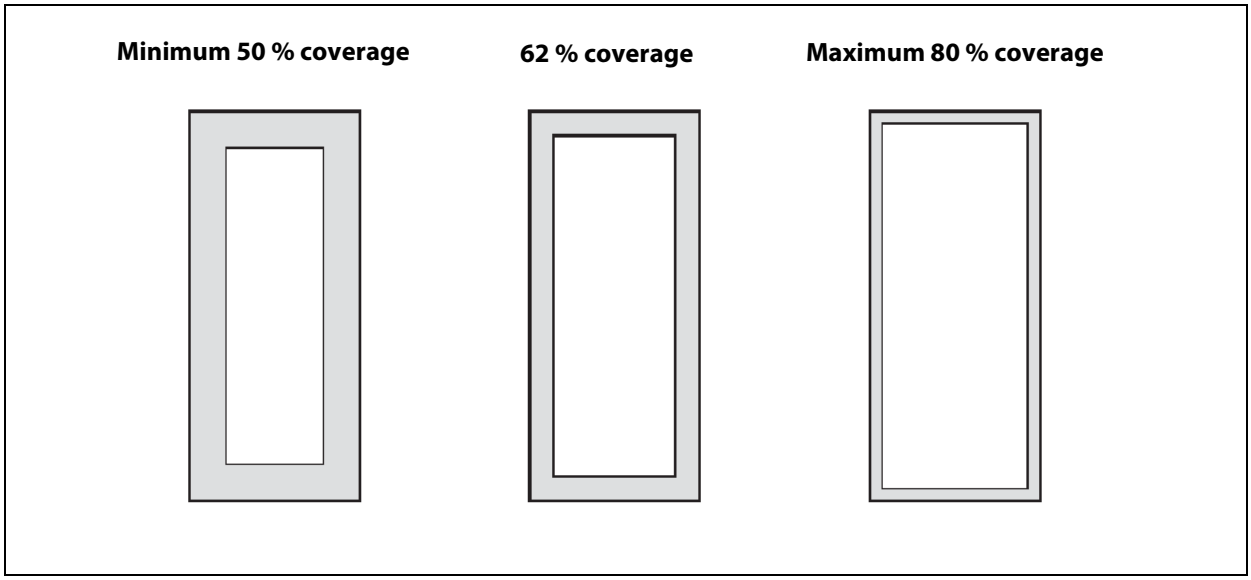


Figure 82:
Solder Paste Application on Pads



Solder Paste on Pads: The aperture opening for the signal pads should be between 50-80% of the QFN pad area.

Soldering Options and Package Placement

1. Hand soldering of these devices is not recommended even for prototypes.
2. Infrared or Convection mass reflow soldering is the preferred method of QFN attachment.
3. Manual placement and/or manual repositioning of QFN packages is not recommended.

Solder Reflow Profile

The PCB assembly should be instrumented and the reflow oven's process parameters established to ensure the solder paste manufacturer's reflow profile specification is met during the assembly process. See Figure 84.

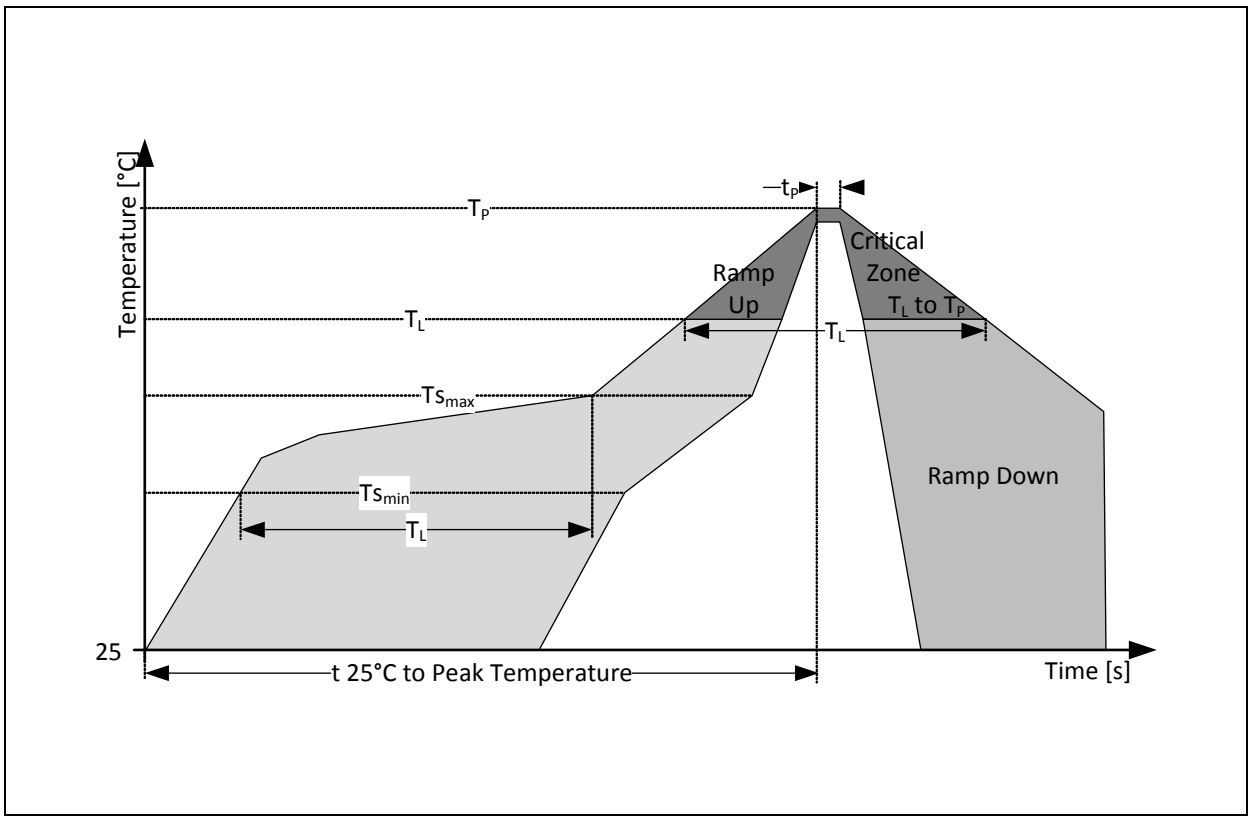
The maximum PCB temperature recommended by the supplier must not be exceeded.

Figure 83:
Solder Reflow Profile

Profile Feature	Lead-free Assembly
Average ramp-up rate (Ts_{max} to T_P)	3 °C/second max.
Preheat • Temperature Min (Ts_{min}) • Temperature Max (Ts_{max}) • Time (t_L)	150 °C 200 °C 60 – 120 seconds
Time maintained above: • Temperature (T_L) • Time (t_L)	217 °C 60 – 150 seconds
Peak/classification temperature (T_P)	260 °C
Time within 5 °C of actual peak temperature (T_P)	30 seconds
Ramp-down rate	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

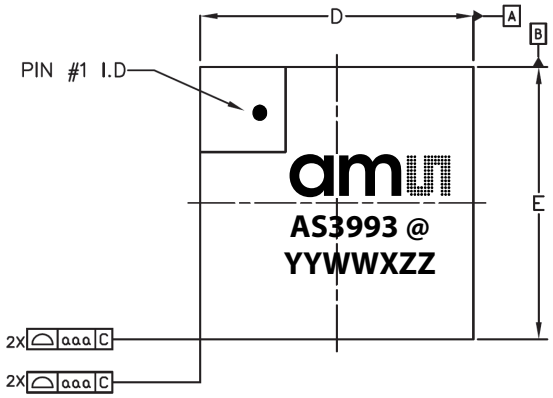
JEDEC Standard Lead-Free Reflow Profile: According to J-STD-020D.

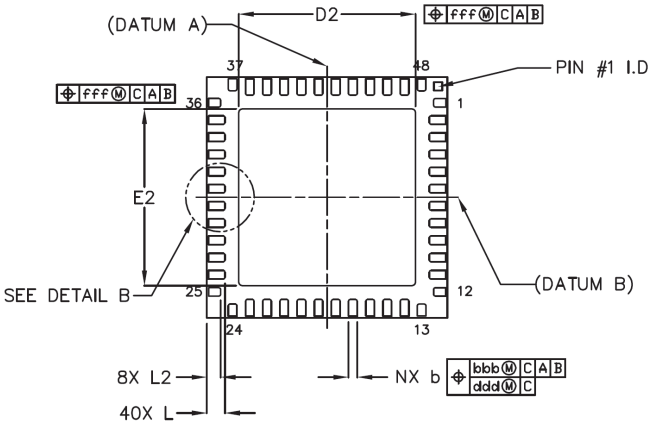
Figure 84:
Recommended Reflow Soldering Profile



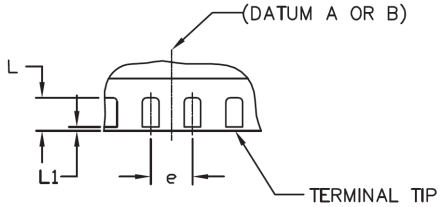
Package Drawings & Markings

Figure 85:
Package Drawings



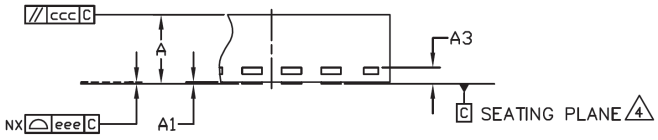


Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	-	0.20 REF	-
L	0.48	0.53	0.58
L1	0	-	0.15
L2	0.35	0.40	0.45
b	0.18	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
D2	5.04	5.14	5.24
E2	5.04	5.14	5.24
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		48	



EVEN/ODD TERMINAL SIDE

DETAIL B



AS3993 Package Drawings: This figure shows the package laser marking and package drawings of the AS3993 device. 'YYWWXZZ' is the Date Code information.

Note(s):

1. Dimensioning and tolerances conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.15mm is acceptable.
4. Co-planarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.
6. N is the total number of terminals.
7. This drawing is subject to change without notice.

Figure 86:
Packaging Code @YYWWXZZ

@	YY	WW	X	ZZ
Sublot Identifier	Year	Working week assembly / packaging	Plant Identifier	Free choice / traceability code

Packaging Code @YYWWXZZ: This figure explains the laser marked date code on the package.

Ordering & Contact Information

Figure 87:
Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS3993-BQFM	48-pin QFN (7x7x0.9 mm)	AS3993	Tape & Reel	50 pcs/reel
AS3993-BQFT				500 pcs/reel

Ordering Information: This figure shows ordering information for the AS3993 device.

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 2-04 (2015-Apr-10) to current revision 2-05 (2015-Nov-04)	Page
Updated Figure 5	7
Added Appendix-Errata Notes section	109

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Appendix - Errata Notes

Known Deviations in the Analog Section of AS3993

Deviation A1

AGD Voltage Is Below 1.6V

Description: AGD voltage is in the range of 1.52V to 1.55V instead of 1.6V. As a consequence all regulated voltages are ~100mV lower than nominal.

Workaround: Send direct command Automatic power supply level setting (A2h) to optimally adjust the regulated voltages (~300mV below VEXT voltage).

The command A2h temporarily activates RF field, to simulate the associated voltage drop during operation. After power up, set all the register related to PLL and RF output signal and then trigger the A2h.

Deviation A2

Increased Power Down Current IVEXT

Description: In case external TCXO continuously drives OSCO, the IVEXT power down current is ~70uA.

Workaround: For low I_{PD} the OSCO should not be driven in power down mode.

Deviation A4

Crystal Oscillator Power Mode Switch-Back

Description: Crystal oscillator switches to low power mode too soon, resumes to high power mode and stays there.

Workaround: Not very critical for normal application. In case oscillator mode is important, one can control it via xosc<1:0> option bits (reg0Eh).

Deviation A9

Linear RSSI Phase Bit Persistence

Description: Linear RSSI phase bit is valid only from the end of the pilot till end of reception.

Workaround: Read the phase bit after the 2nd byte IRQ, or similarly during the data reception phase.

Deviation A12

Corrupted TCXO Mode Operation

Description: When operating in the TCXO mode (OSCI = 0V) and in the presence of high RF ground currents (e.g. the AS3993 is on the same PCB as ceramic chip antenna), the induced current s on the OSCI connection can corrupt the TCXO mode operation. The problem manifests by increased OSCO voltage during RF power transmission and missing internal clock (CLSYS).

Workaround: Do not connect the OSCI pin, and writing xosc<1:0> = 10_b. Avoid an unnecessary trace on the OSCI line to decrease coupling.

Known Deviations in the Digital Section of AS3993

Deviation D4A

Re-Triggering Rx Wait Time

Description: Rx wait time is longer than set in reg08h in case a SPI read or write is done during the RX wait period (from end of data transmission to start of data reception). An SPI activity during the wait time period reloads the counter and prolongs the RX wait time.

Workaround: Typically during this period the IRQ status register (end of TX) is read. There are two possibilities:

- Read the IRQ status register immediately after TX IRQ is asserted, or
- Read the IRQ status register after the RX wait time period.

In case there are any other AS3993 related SPI activities needed after the end of TX, they should be performed after the RX wait period has ended. SPI activities to other SPI slave devices on the same bus (while AS3993's NCS pin = 1) does not prolong RX-wait time.

Deviation D6

IRQ at Start-Up

Description: IRQ at start-up. After EN = 1 the AS3993 wakes up and sends an IRQ request, before the crystal clock is settled. Until osc_ok switches to 1 the IRQ line remains high and the IRQ status contains 00h. After osc_ok = 1 the system operates correctly.

Workaround: Set EN = 1 and poll the device version register and the osc_ok status bit periodically. When both show the expected data, read the IRQ status in registers 37h and 38h and continue with the operation.

Content Guide