

AS1376

1A, Low Input Voltage, Low Quiescent Current LDO

General Description

The AS1376 is a Dual Supply Rail Linear Regulator designed to deliver 1A of load current while consuming only 67 μ A (typ) of ground current. In the typical post regulation application VBIAS is directly connected to the main input supply, (range 2.5V ... 5.5V) and VIN is supplied by the output voltage of a host DC-DC Converter (range 0.7V ... 4.5V).

The device offers excellent dropout (120mV @ 1A) and transient performance.

In shutdown (Enable pin pulled low), the device turns off and reduces quiescent current consumption to 10nA (typ) at both VBIAS and VIN terminals.

In shutdown, a 100 Ω (typ) discharge path is connected between output and ground to provide rapid discharge of the overall load capacitance connected to the AS1376 output terminal. Auto-discharge minimizes the possibility that VOUT > VIN during shutdown. When VOUT > VIN, reverse current flows through the inherent body diode of the N-channel series pass transistor.

The AS1376 also features internal protection against over-temperature, over-current and under-voltage conditions.

The AS1376 is available in an 8-pin 2x2 TDFN package and AS1376B is available in a 6-balls WL-CSP. Both package options are qualified for operation over the -40°C to 85°C temperature range.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of this device are listed below:

Figure 1:
Added Value of Using AS1376

| Benefits | Features |
|---|---|
| <ul style="list-style-type: none"> Less internal voltage losses and minimized self-heating | <ul style="list-style-type: none"> Ultra-Low Dropout Voltage: <120mV @ 1A load |
| <ul style="list-style-type: none"> Supports a variety of low voltage end applications | <ul style="list-style-type: none"> Output Voltage from 0.5V to 3.3V |
| <ul style="list-style-type: none"> Ideal as follower of a buck converter | <ul style="list-style-type: none"> Input Voltage from 0.7V to 3.6V |
| <ul style="list-style-type: none"> Independent bias supply ensures more robustness due to heavy load changes | <ul style="list-style-type: none"> Bias Supply Voltage from 2.5V to 5.5V |
| <ul style="list-style-type: none"> Supports a variety of high load applications | <ul style="list-style-type: none"> Maximum Output Current up to 1A |
| <ul style="list-style-type: none"> Cost effective, small package | <ul style="list-style-type: none"> 8-pin TDFN 2x2mm package 6-balls WL-CSP with 0.4mm pitch |

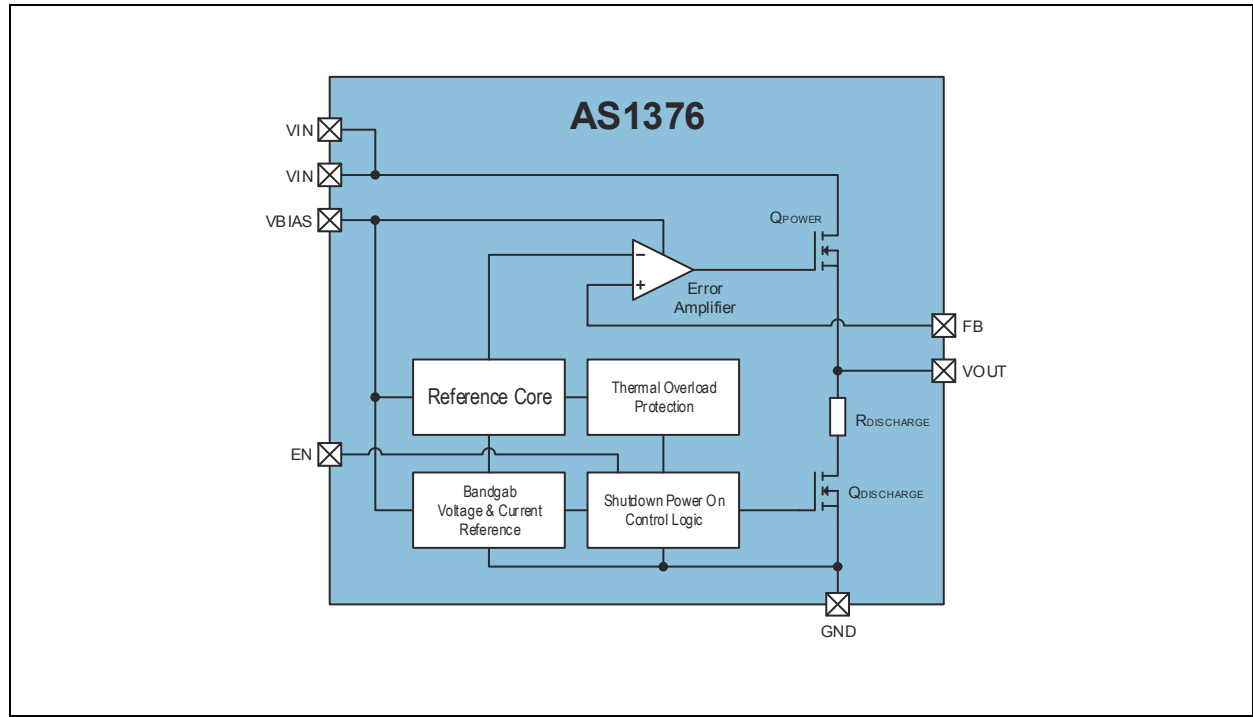
Applications

The devices are ideal for powering cordless and mobile phones, MP3 players, CD and DVD players, PDAs, hand-held computers, digital cameras and any other hand-held and/or battery-powered device.

Block Diagram

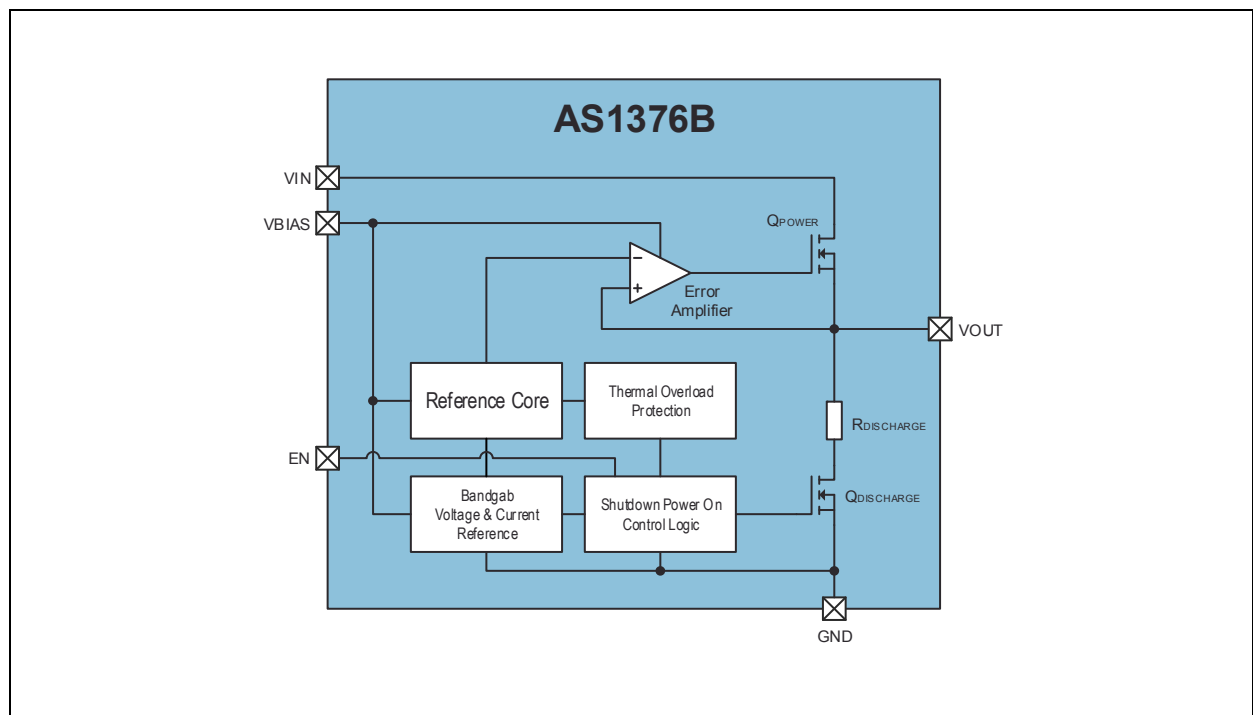
The functional blocks of this device for reference are shown below:

Figure 2:
Functional Blocks of AS1376



Block Diagram: This figure shows the block diagram of AS1376

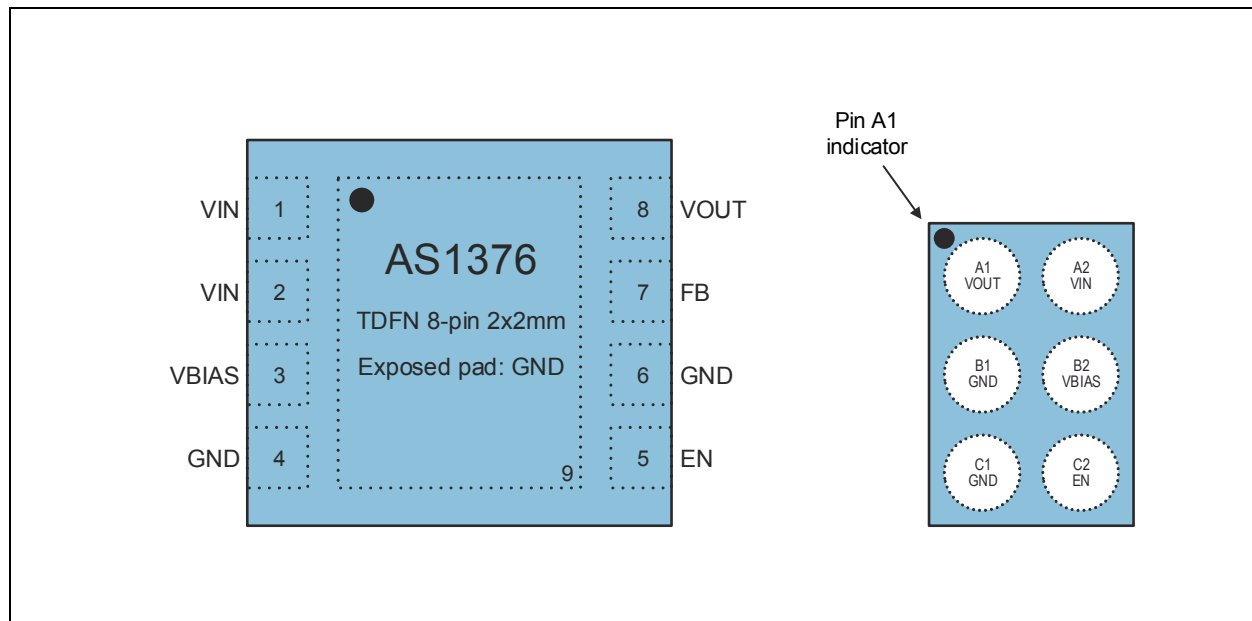
Figure 3:
Functional Blocks of AS1376B



Block Diagram: This figure shows the block diagram of AS1376B

Pin Assignments

Figure 4:
Pin Diagram of AS1376 and AS1376B



Pin Assignment: These figures show the top view pin assignment of AS1376 in 8-pin TDFN package and AS1376B in 6-balls WL-CSP.

Figure 5:
Pin Description of AS1376 and AS1376B

| Pin Number | | Pin Name | Description |
|---------------------|------------------------|----------|---|
| 8-Pin TDFN (AS1376) | 6-Pin WL-CSP (AS1376B) | | |
| 1,2 | A2 | VIN | Unregulated Input Voltage. 0.6V to 3.6V. Bypass this pin with a capacitor to GND |
| 3 | B2 | VBIAS | Bias Input Voltage. 2.5V to 5.5V. Bypass this pin with a capacitor to GND |
| 4,6 | B1,C1 | GND | Ground. |
| 5 | C2 | EN | Enable. Pull this pin low to disable the device. |
| 7 | - | FB | Feedback Pin. Connect to VOUT to select the factory preset output voltage. For the adjustable version connect to an external resistor divider to set the output voltage. |
| 8 | A1 | VOUT | Regulated Output Voltage. 0.5V to 3.3V. Bypass this pin with a capacitor to GND |
| 9 | - | | Exposed Pad. This pad is not connected internally. Ensure a good connection to the PCB to achieve optimal thermal performance. |

Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings of AS1376

| Symbol | Parameter | Min | Max | Units | Comments |
|--|--|--------|------------|-------|--------------------------------|
| Electrical Parameters | | | | | |
| | VIN to GND | -0.3 | 5.0 | V | Applicable for pin: VIN |
| | VBIAS, EN to GND | -0.3 | 6.5 | V | Applicable for pins: VBIAS, EN |
| | VOUT to GND | -0.3 | VIN + 0.3 | V | Applicable for pin: VOUT |
| | Output Short-Circuit Duration | | Indefinite | | |
| I _{SCR} | Input Current (latch-up immunity) | ± 100 | | mA | Norm: JEDEC JESD78D Nov 2011 |
| Continuous Power Dissipation (T _A = 70°C) | | | | | |
| P _T ⁽¹⁾ | Continuous power dissipation | | 0.6 | W | WL-CSP |
| | | | 1.5 | W | TDFN |
| Electrostatic Discharge | | | | | |
| ESD _{HBM} | Electrostatic Discharge HBM | ± 1000 | | V | Norm: JS-001-2014 |
| Temperature Ranges and Storage Conditions | | | | | |
| T _A | Operating Ambient Temperature | -40 | 85 | °C | |
| R _{THJA} ⁽¹⁾ | Junction to Ambient Thermal Resistance | 95 | | °C/W | WL-CSP |
| | | 36 | | °C/W | TDFN |
| T _J | Operating Junction Temperature | | 125 | °C | |
| T _{STRG} | Storage Temperature Range | -55 | 125 | °C | WL-CSP |
| | | -55 | 150 | °C | TDFN |

| Symbol | Parameter | Min | Max | Units | Comments | |
|-------------------|------------------------------------|-----|-----|-------|----------|--|
| T _{BODY} | Package Body Temperature | | 260 | °C | WL-CSP | Norm: IPC/JEDEC J-STD-020 ⁽²⁾ |
| | | | 260 | °C | TDFN | Norm: IPC/JEDEC J-STD-020 ⁽²⁾ The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn) |
| RH _{NC} | Relative Humidity (non-condensing) | 5 | 85 | % | | |
| MSL | Moisture Sensitivity Level | 1 | | | WL-CSP | Represents an unlimited floor time |
| | | 1 | | | TDFN | Represents an unlimited floor time |

Note(s) and/or Footnote(s):

1. Depending on actual PCB layout and PCB used
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non hermetic Solid State Surface Mount Devices"

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 7:
Electrical Characteristics of AS1376

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------------|-----------------------------------|--|------|--------|------|---------------|
| V_{IN} | Input Voltage | | 0.7 | | 3.6 | V |
| V_{BIAS} | Bias Supply Voltage | | 2.5 | | 5.5 | V |
| V_{OUT} | Output Voltage | Available in 100mV steps | 0.5 | | 3.3 | V |
| $V_{OUT_nom} - V_{OUT}$ | Output Voltage Accuracy | $I_{OUT} = 100\mu A$ | -1.5 | | +1.5 | % |
| | | $I_{OUT} = 0A$ to 1A | -2 | | +2 | |
| V_{FB} | Feedback Voltage ⁽¹⁾ | $I_{OUT} = 100\mu A$ | 492 | 500 | 508 | mV |
| | | $I_{OUT} = 0A$ to 1A | 490 | 500 | 510 | mV |
| $\Delta V_{OUT} / \Delta V_{IN}$ | Line Regulation V_{IN} | $I_{OUT} = 100\mu A$ | | 40 | | $\mu V/V$ |
| $\Delta V_{OUT} / \Delta V_{BIAS}$ | Line Regulation V_{BIAS} | $I_{OUT} = 100\mu A$ | | 135 | | $\mu V/V$ |
| $\Delta V_{OUT} / \Delta I_{OUT}$ | Load Regulation | $I_{OUT} = 1mA$ to 1A | | 0.0002 | | %/mA |
| I_{OUT} | Output Current ⁽²⁾ | | 1 | | | A |
| I_{LIM} | Current Limit | V_{OUT} forced to 90% of nominal V_{OUT} | | 1.35 | | A |
| V_{DROP_VIN} | Output Voltage Dropout V_{IN} | $V_{BIAS} = V_{OUT} + 1.5V, I_{OUT} = 1A$ | | 120 | | mV |
| | | $V_{BIAS} = V_{OUT} + 1.8V, I_{OUT} = 1A$ | | 115 | | |
| | | $V_{BIAS} = V_{OUT} + 2.1V, I_{OUT} = 1A$ | | 110 | | |
| | | $V_{BIAS} = 5.5V, I_{OUT} = 1A$ | | 105 | | |
| V_{DROP_VBIAS} | Output Voltage Dropout V_{BIAS} | $I_{OUT} = 500mA$ | | 0.85 | | V |
| | | $I_{OUT} = 1A$ | | 1.1 | | |
| e_N | Output Voltage Noise | $f = 10Hz$ to 100kHz, $I_{OUT} = 1mA$ | | 65 | | μV_{RMS} |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------|---|-------------------------------------|-----|-------|-----|------|
| PSRR_VIN | Power Supply Rejection Ratio Sine modulated VIN | f = 100Hz, I _{OUT} = 10mA | | 78 | | dB |
| | | f = 1kHz, I _{OUT} = 10mA | | 61 | | |
| | | f = 10kHz, I _{OUT} = 10mA | | 54 | | |
| | | f = 100kHz, I _{OUT} = 10mA | | 60 | | |
| PSRR_VBIAS | Power Supply Rejection Ratio Sine modulated VBIAS | f = 100Hz, I _{OUT} = 10mA | | 69 | | dB |
| | | f = 1kHz, I _{OUT} = 10mA | | 51 | | |
| | | f = 10kHz, I _{OUT} = 10mA | | 45 | | |
| | | f = 100kHz, I _{OUT} = 10mA | | 45 | | |
| I _{Q_VBIAS} | Quiescent Current into VBIAS | | | 60 | 120 | uA |
| I _{Q_VIN} | Quiescent Current into VIN | I _{OUT} = 0mA | | 6.5 | 8 | |
| I _{SHDN_VBIAS} | Shutdown Current into VBIAS | EN = 0V | | 0.02 | | uA |
| I _{SHDN_VIN} | Shutdown Current into VIN | EN = 0V | | 0.02 | | uA |
| I _{EN} | Enable Input Bias Current | | | 0.001 | 1 | uA |
| V _{IH} | Enable Input Threshold | V _{IN} = 0.7 to 3.6V | 1 | | | V |
| V _{IL} | | | | | 0.4 | |
| T _{SHDN} | Thermal Shutdown Temperature | | | 155 | | °C |
| ΔT _{SHDN} | Thermal Shutdown Hysteresis | | | 30 | | °C |
| ΔV _{OUT} | Dynamic Load Transient Response VBIAS | | | ±35 | | mV |
| t _{ON} | Exit Delay from Shutdown | Settling to 95%, no Load | | 72 | | us |
| C _{OUT} | Output Capacitor | Load Capacitor Range | 1 | | 10 | uF |
| | | Maximum ESR Load | | | 500 | mΩ |

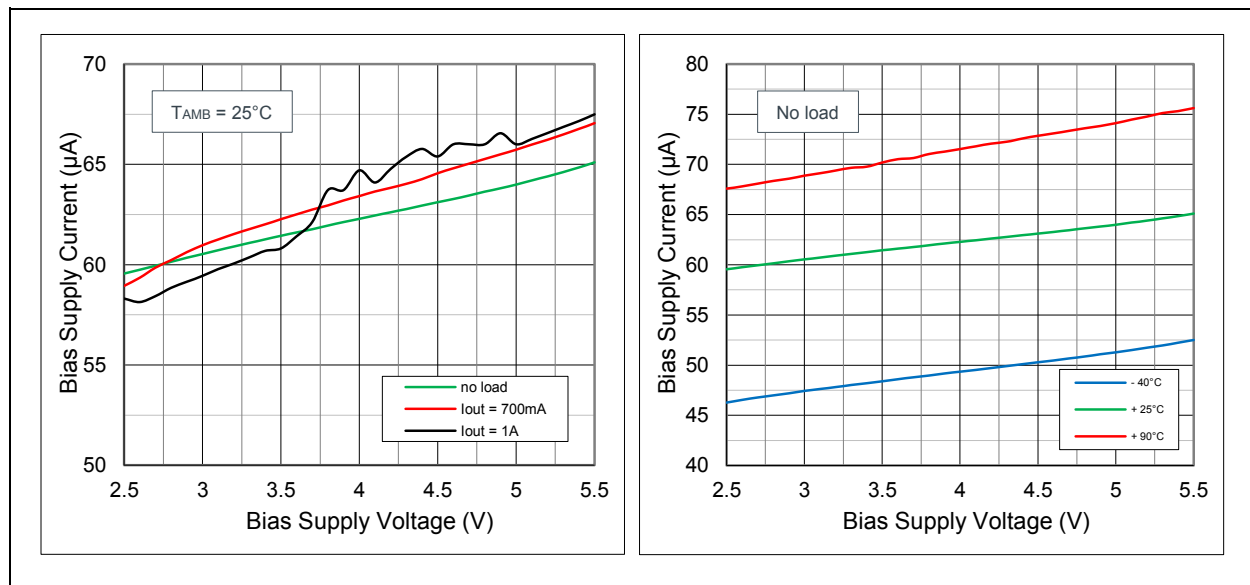
Electrical Characteristics: V_{IN} = V_{OUT} + 0.2V, V_{BIAS} = V_{OUT} + 1.5V (or 2.5V whichever is larger), EN = V_{BIAS}, C_{IN} = C_{OUT} = 1uF, C_{BIAS} = 4.7uF, T_{AMB} = -40°C to 85°C. Typical values are at T_{AMB} = 25°C (unless otherwise specified)

Note(s) and/or Footnote(s):

1. Valid only for AS1376-BTDT-AD (adjustable output versions)
2. Limit guaranteed by design and characterization

Typical Operating Characteristics

Figure 8:
Bias Supply Current vs. Bias Supply Voltage



Bias Supply Current vs. Bias Supply Voltage: $V_{\text{IN}} = 1.2\text{V}$, $\text{EN} = V_{\text{BIAS}}$, $V_{\text{OUT}} = 1.0\text{V}$, $C_{\text{IN}} = C_{\text{OUT}} = 1\mu\text{F}$, $C_{\text{BIAS}} = 4.7\mu\text{F}$

Figure 9:
GND Current vs. Bias Supply Voltage

GND Current vs. Bias Supply Voltage:

$V_{\text{IN}} = 1.2\text{V}$, $\text{EN} = V_{\text{BIAS}}$, $V_{\text{OUT}} = 1.0\text{V}$,
 $C_{\text{IN}} = C_{\text{OUT}} = 1\mu\text{F}$, $C_{\text{BIAS}} = 4.7\mu\text{F}$

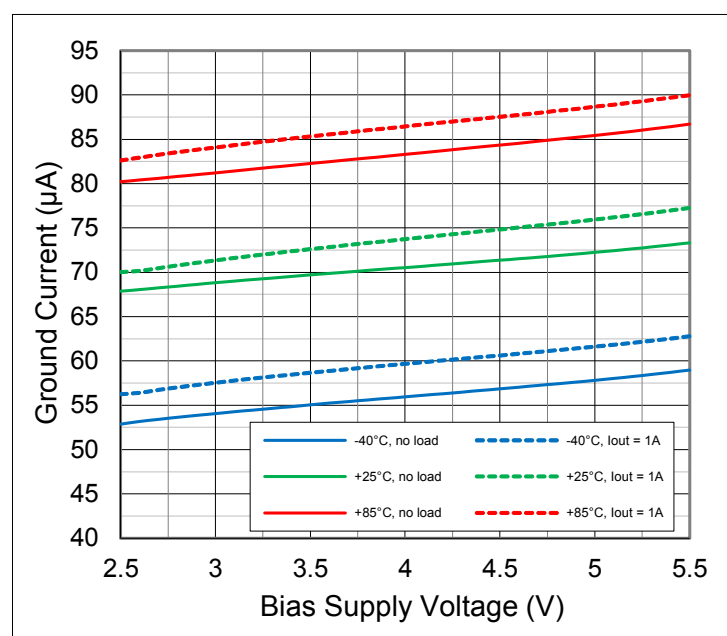


Figure 10:
GND Current vs. Load Current

GND Current vs. Load Current:

VIN = 1.2V, EN = VBIAS, VOUT = 1.0V,
CIN = COUT = 1 μ F, CBIAS = 4.7 μ F

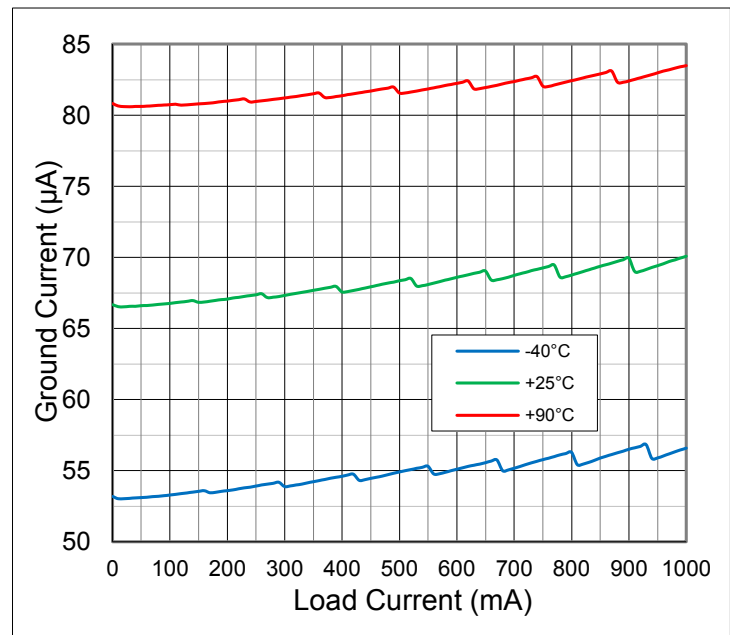


Figure 11:
PSRR vs. Frequency

PSRR vs. Frequency: PSRRVIN

(EN = VBIAS = 2.5V, VOUT = 1.0V, no CIN,
COUT = CBIAS = 1 μ F, RLOAD = 100 Ω);
PSRRVBIAS (EN = VIN = 1.2V, VOUT =
1.0V, CIN = COUT = 1 μ F, no CBIAS,
RLOAD = 100 Ω)

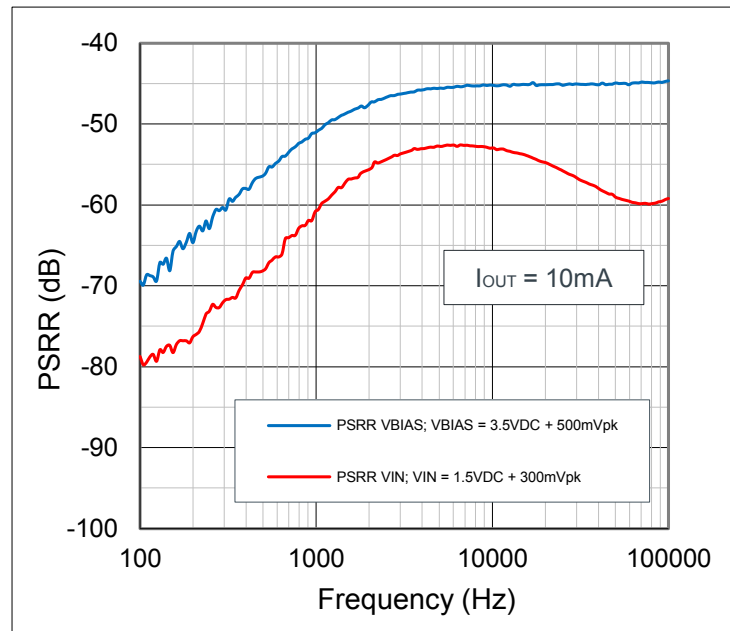
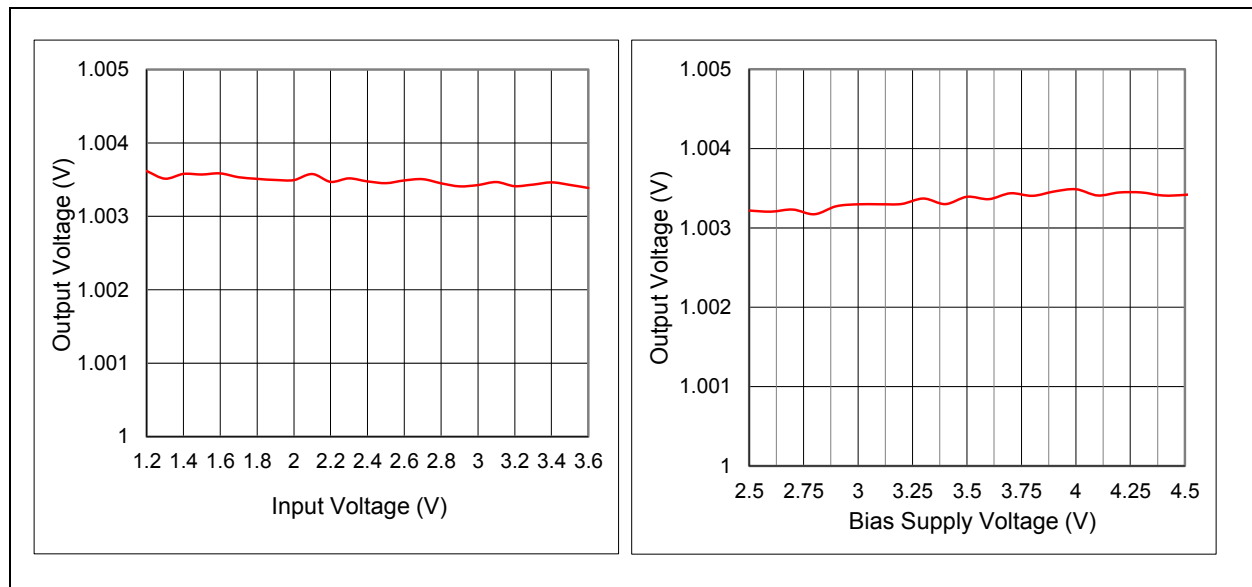


Figure 12:
Line Regulation



Line Regulation: LNRVIN (EN = VBIAS = 2.5V, VOUT = 1.0V, CIN = COUT = 1 μ F, CBIAS = 4.7 μ F, IOUT = 100 μ A);
LNRVBIAS (EN = VBIAS, VIN = 1.2V, VOUT = 1.0V, CIN = COUT = 1 μ F, CBIAS = 4.7 μ F, IOUT = 100 μ A)

Figure 13:
Load Regulation

Load Regulation: EN = VBIAS = 2.5V,
VIN = 1.2V, VOUT = 1.0V,
CIN = COUT = 1 μ F, CBIAS = 4.7 μ F

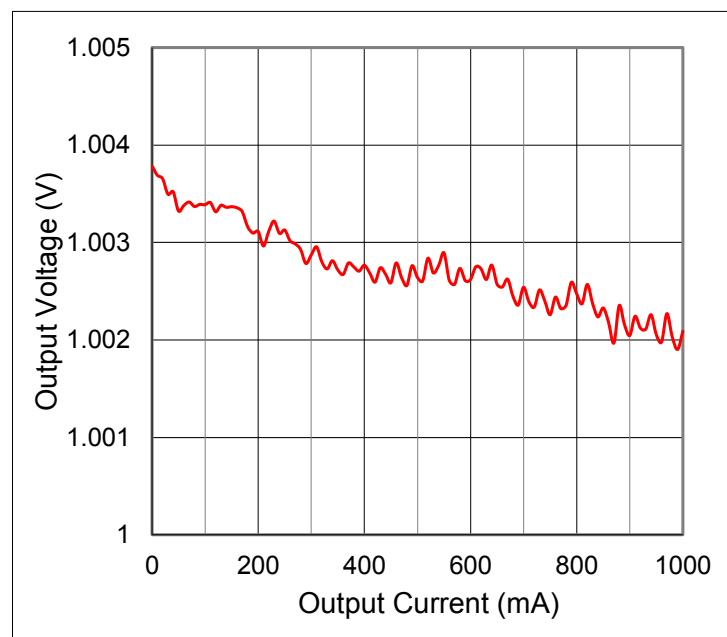


Figure 14:
Output Voltage vs. Temperature

Output Voltage vs. Temperature:

EN = VBIAS = 2.5V, VIN = 1.2V,
VOUT = 1.0V, CIN = COUT = 1 μ F,
CBIAS = 4.7 μ F, IOUT = 1mA

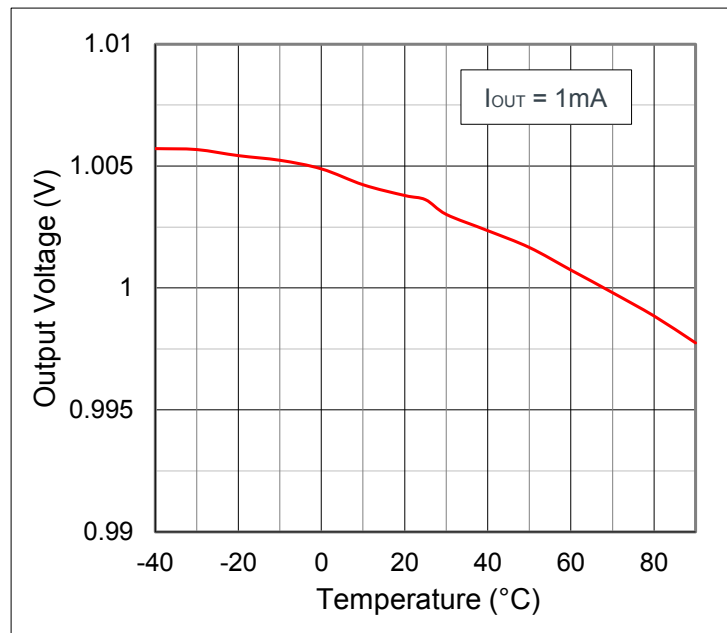


Figure 15:
Dropout VIN vs. Temperature

Dropout VIN vs. Temperature:

EN = VBIAS = 2.5V, VIN = 1.2V,
VOUT = 1.0V, CIN = COUT = 1 μ F,
CBIAS = 4.7 μ F, IOUT = 1A

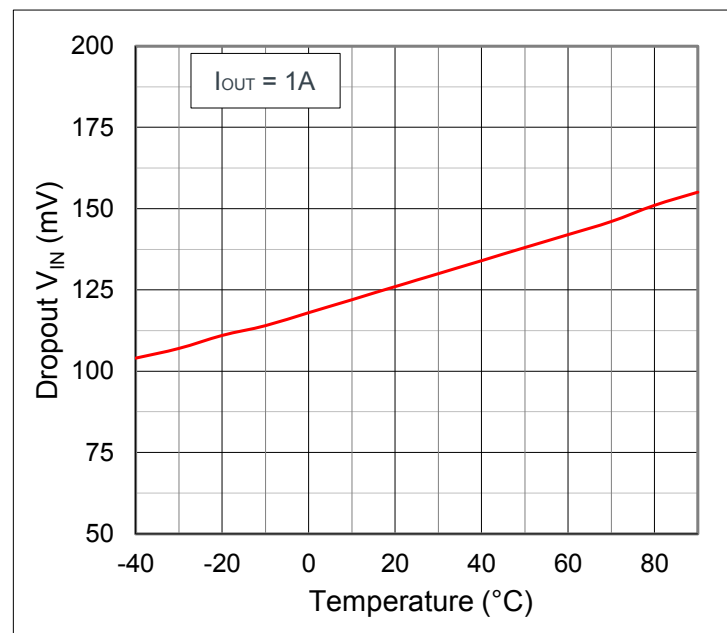
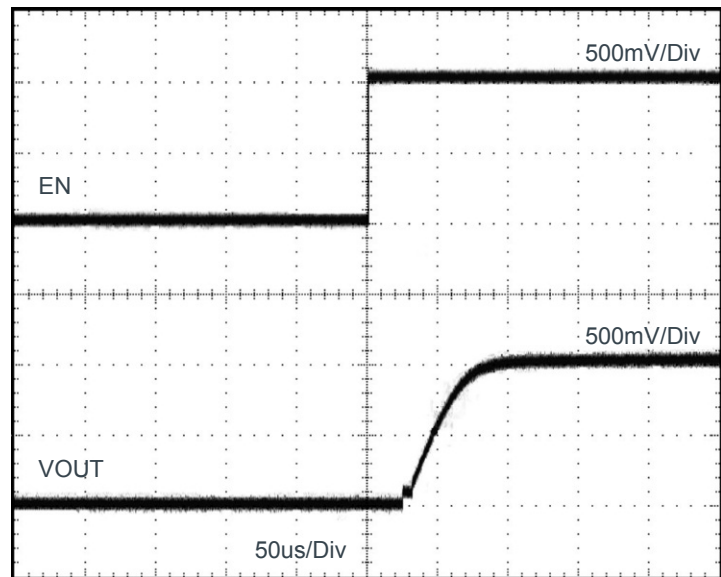


Figure 16:
Enable Start-Up

Enable Start-Up: EN = VBIAS = 2.5V,
VIN = 1.2V, settling to 95% of VOUT
(950mV), CIN = COUT = 1uF,
CBIAS = 4.7uF, no load



Detailed Description

The AS1376 is a low-dropout, low-quiescent-current linear regulator intended for LDO regulator applications where output current load requirements range from no load to 1A. All devices come with fixed output voltage from 0.5V to 3.3V.

Shutdown current for the whole regulator is typically 20nA. The device has integrated short-circuit and over current protection. Under-Voltage lockout prevents erratic operation when the input voltage is slowly decaying (e.g. in a battery powered application). Thermal Protection shuts down the device when die temperature reaches 150°C. This is a useful protection when the device is under sustained short circuit conditions.

As illustrated in the block diagram on page 3, the devices comprise voltage reference, error amplifier, N-channel MOSFET pass transistor, internal voltage divider, current limiter, thermal sensor and shutdown logic.

The bandgap reference is connected to the inverting input of the error amplifier. The error amplifier compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the N-channel MOSFET gate is pulled higher, allowing more current to pass to the output, and increases the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled down, allowing less current to pass to the output.

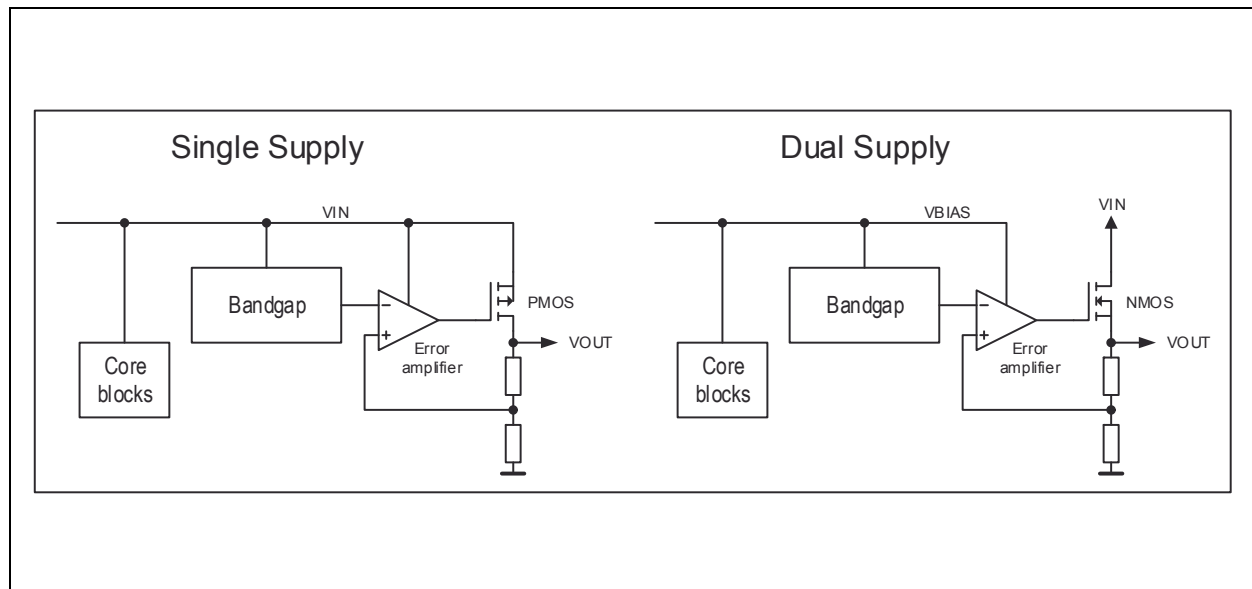
When the adjustable output variant is selected, an external resistor voltage divider is connected to FB pin and a sample of the output is compared to the 500mV reference.

When a fixed output variant is chosen, FB must be connected to the Output pin. Depending upon the variant chosen, the internal reference is trimmed to the final output voltage.

Advantage of Dual Supply Architecture vs. Traditional Single Supply Approach

Compared to the traditional single supply approach, employing a P-channel series pass MOSFET, the dual rail architecture ensures improved performances in a LDO when operating at very low input voltages below the threshold of the internal series power N-channel MOSFET. The extra supply voltage at pin VBIAS ($V_{BIAS} > V_{IN}$) ensures that the N-channel MOSFET always operates above its threshold voltage.

Figure 17:
Single vs. Dual Supply



Single vs. Dual Supply: This figure shows simplified block diagrams of single supply P-channel LDO and dual rail N-channel series pass architectures.

The P-channel LDO uses a PMOS output transistor connected in a common source configuration. During regulation, the PMOS

gate-source voltage moves between VIN and GND as the load demands. The dual supply approach is based on a NMOS output transistor in common drain configuration where the source is connected to the regulated output. During regulation, the NMOS gate source voltage increases from VOUT to VBIAS as the load demands. As the drain voltage is not shared with the remaining blocks of the circuit, its value can be chosen independently. The NMOS source follower design allows improved efficiency and dropout at low input voltages and provides faster load transient response.

Dropout Voltage

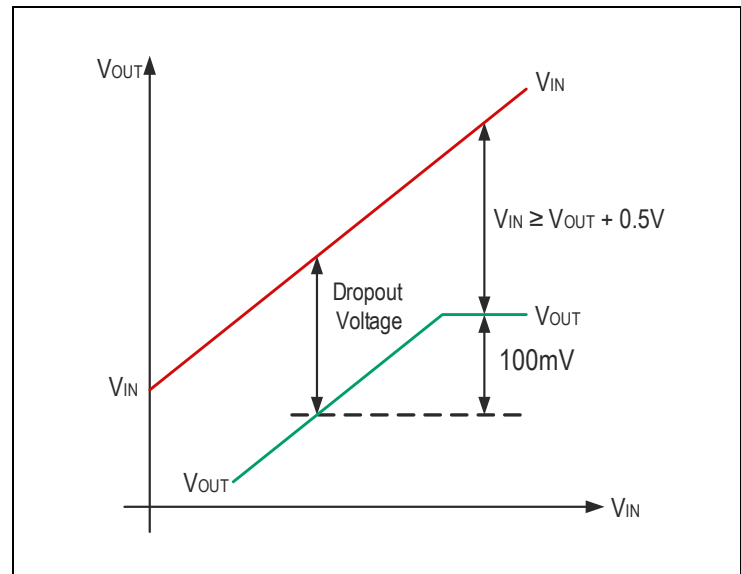
Dropout is the input to output voltage difference, below which the linear regulator ceases to regulate. At this point, the output voltage change follows the input voltage change. Dropout voltage may be measured at different currents and, in particular at the regulator maximum one. From this is obtained the MOSFET maximum series resistance over temperature.

$$(EQ1) \quad V_{DROPOUT} = I_{LOAD} * R_{SERIES}$$

Dropout is probably the most important specification when the regulator is used in a battery application. The dropout performance of the regulator defines the useful “end of life” of the battery before replacement or re-charge is required.

Figure 18:
Graphical Representation of Dropout Voltage

Dropout Voltage: This figure shows the variation of V_{OUT} as V_{IN} is varied for a certain load current. The practical value of dropout is the differential voltage ($V_{OUT} - V_{IN}$) measured at the point where the LDO output voltage has fallen by 100mV below the nominal, fully regulated output value. The nominal regulated output voltage of the LDO is that obtained when there is 500mV (or greater) input-output voltage differential.



Auto-Discharge

AS1376 features an auto-discharge function that discharges the load capacitance through a 100Ω (typ) path to ground when the device is placed in shutdown. This helps to minimize the possibility that $V_{OUT} > V_{IN}$ during shutdown caused by differing capacitance discharge rates at V_{IN} and V_{OUT} terminals. When $V_{OUT} > V_{IN}$, reverse current flows through the inherent body diode of the NMOS series pass transistor. This current should be limited to 50mA or less. If this is not possible, then an external Schottky diode should be connected between V_{OUT} (anode) and V_{IN} (cathode) to bypass the discharge current around the AS1376.

Efficiency

Low quiescent current and low input-output voltage differential are important in battery applications amongst others, as the regulator efficiency is directly related to quiescent current and dropout voltage.

$$(EQ2) \quad \text{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{V_{IN} \cdot (I_Q + I_{LOAD})} \times 100\%$$

I_Q ... Quiescent current of LDO measured at V_{BIAS}

Power Dissipation

Maximum power dissipation (PD) of the LDO is the sum of the power dissipated by the internal series MOSFET and the quiescent current required to bias the internal voltage reference and the internal error amplifier.

$$(EQ3) \quad PD_{(MAX)}(\text{Seriespass}) = I_{LOAD(MAX)} * (V_{IN(MAX)} - V_{OUT(MIN)})$$

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

$$(EQ4) \quad PD_{(MAX)}(\text{Bias}) = V_{IN(MAX)} * I_Q$$

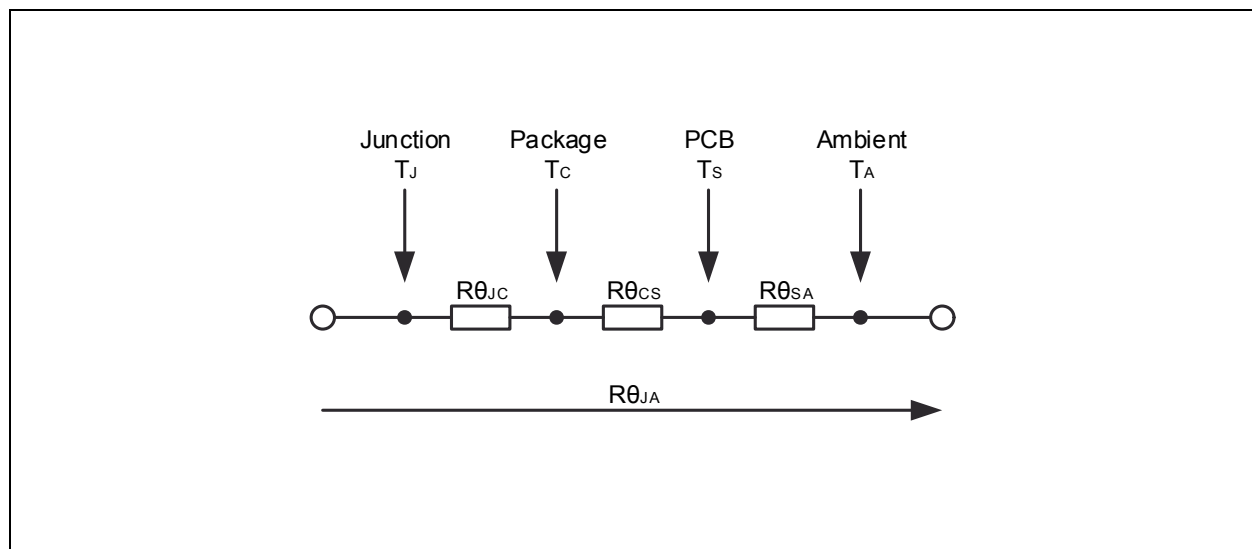
Total LDO power dissipation is calculated as:

$$(EQ5) \quad PD_{(MAX)}(\text{TOTAL}) = PD_{(MAX)}(\text{Seriespass}) + PD_{(MAX)}(\text{Bias})$$

Junction Temperature

Under all operating conditions, the maximum junction temperature should not exceed 125°C (unless the data sheet specifically allows). Limiting the maximum junction temperature requires knowledge of the heat path from junction to case ($\theta_{JC}^{\circ}\text{C/W}$ fixed by the IC manufacturer), and adjustment of the case to ambient heat path ($\theta_{CA}^{\circ}\text{C/W}$) by manipulation of the PCB copper area adjacent to the IC position.

Figure 19:
Steady State Heat Flow Equivalent Circuit

**Total Thermal Path Resistance**

$$(EQ6) \quad R_{\theta_{JA}} = R_{\theta_{JC}} + R_{\theta_{CS}} + R_{\theta_{SA}}$$

Junction Temperature ($T_J^{\circ}\text{C}$) is determined by:

$$(EQ7) \quad T_J = (PD_{(MAX)} * R_{\theta_{JA}}) + T_{AMB}$$

Explanation of Steady State Specifications

Line Regulation

Line regulation is defined as the change in output voltage when the input voltage is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the input voltage changes. Line regulation is a measure of the DC open loop gain of the error amplifier.

$$(EQ8) \quad LNR = \frac{\Delta V_{OUT}}{\Delta V_{IN}}$$

In practice, line regulation is referred to the regulator output voltage in terms of %/V_{OUT}. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$(EQ9) \quad LNR = \frac{\Delta V_{OUT}}{\Delta V_{IN}} * \frac{100}{V_{OUT}} \%$$

Load Regulation

Load regulation is defined as the change of the output voltage when the load current is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the load changes. Load regulation is a measure of the DC closed loop output resistance of the regulator.

$$(EQ10) \quad LDR = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

In practice, load regulation is referred to the regulator output voltage in terms of %/mA. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$(EQ11) \quad LDR = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} * \frac{100}{V_{OUT}} \%$$

Output Voltage Setting

For the adjustable Output Voltage version the final output voltage can be calculated by the ratio of R_{UP} and R_{DN}, the internal reference voltage (= FB voltage) and the input offset voltage of the error amplifier.

$$(EQ12) \quad V_{OUT} = (V_{FB}) * \left(1 + \frac{R_{UP}}{R_{DN}}\right) - R_{UP} * 0.45 \mu A$$

Total Accuracy

Away from dropout, total steady state accuracy is the sum of setting accuracy, load regulation and line regulation.

$$(EQ13) \quad Accuracy_{Total} = Accuracy_{Setting} + LDR + LNR$$

Explanation of Dynamic Specifications

Power Supply Rejection Ratio (PSRR)

Known also as Ripple Rejection, this specification measures the ability of the regulator to reject noise and ripple beyond DC. PSRR is a summation of the individual rejections of the error amplifier, reference and AC leakage through the series pass transistor. The specification, in the form of a typical attenuation plot with respect to frequency, shows up the gain bandwidth compromises forced upon the designer in low quiescent current conditions.

$$(EQ14) \quad PSRR = 20 \log \frac{\delta V_{OUT}}{\delta V_{IN}}$$

Power supply rejection ratio is fixed by the internal design of the regulator. Additional rejection must be provided externally.

Output Capacitor ESR

The series regulator is a negative feedback amplifier, and as such is conditionally stable. The ESR of the output capacitor is usually used to cancel one of the open loop poles of the error amplifier in order to produce a single pole response. Excessive ESR values may actually cause instability by excessive changes to the closed loop unity gain frequency crossover point. The range of ESR values for stability is usually shown either by a plot of stable ESR versus load current, or a limit statement in the datasheet.

Some ceramic capacitors exhibit large capacitance and ESR variations with temperature and DC bias. Z5U and Y5V capacitors may be required to ensure stability at temperatures below $T_{AMB} = -10^{\circ}\text{C}$. With X7R or X5R capacitors, a $1\mu\text{F}$ capacitor should be sufficient at all operating temperatures.

Larger output capacitor values ($10\mu\text{F}$ max) help to reduce noise and improve load transient-response, stability and power-supply rejection.

Input Capacitor

If the AS1376 is used stand alone, an input capacitor at VIN is required for stability. It is recommended to connect a $1\mu\text{F}$ capacitor between the AS1376 power supply input pin VIN and GND (capacitance value may be increased without limit).

This capacitor must be located as close as possible to the VIN pin and returned to a clean analog ground. A X5R or X7R type or better may be used at the input.

A capacitor at VBIAS is not required if the distance to the supply does not exceed 5cm.

Noise

The regulator output is a DC voltage with noise superimposed on the output. The noise comes from three sources; the reference, the error amplifier input stage, and the output voltage setting resistors. Noise is a random fluctuation and if not minimized in some applications, will produce system problems.

Transient Response

The series regulator is a negative feedback system, and therefore any change at the output will take a finite time to be corrected by the error loop. This “propagation time” is related to the bandwidth of the error loop. The initial response to an output transient comes from the output capacitance, and during this time, ESR is the dominant mechanism causing voltage transients at the output.

$$(EQ15) \quad \delta V_{\text{TRANSIENT}} = \delta I_{\text{OUTPUT}} \times R_{\text{ESR}}$$

Thus an initial +50mA change of output current will produce a -12mV transient when the ESR=240mΩ. Remember to keep the ESR within stability recommendations when reducing ESR by adding multiple parallel output capacitors.

After the initial ESR transient, there follows a voltage droop during the time that the LDO feedback loop takes to respond to the output change. This drift is approx. linear in time and sums with the ESR contribution to make a total transient variation at the output.

$$(EQ16) \quad \delta V_{\text{TRANSIENT}} = \delta I_{\text{OUTPUT}} \times \left(R_{\text{ESR}} + \frac{T}{C_{\text{LOAD}}} \right)$$

CLOAD... Output Capacitor

T ... Propagation Delay of the LDO

This shows why it is convenient to increase the output capacitor value for a better support for fast load changes. Of course the formula holds for $t < \text{“propagation time”}$, so that a faster LDO needs a smaller cap at the load to achieve a similar transient response. For instance 50mA load current step produces 50mV output drop if the LDO response is 1usec and the load cap is 1μF.

There is also a steady state error caused by the finite output impedance of the regulator. This is derived from the load regulation specification discussed above.

Exit from Shutdown Delay

This specification defines the time taken for the LDO to awake from shutdown. The time is measured from the release of the enable pin to the time that the output voltage is within 5% of the final value. It assumes that the voltage at VIN is stable and within the regulator min and max limits. Shutdown reduces the quiescent current to very low, mostly leakage values (<1μA).

Thermal Protection

To prevent operation under extreme fault conditions, such as a permanent short circuit at the output, thermal protection is built into the device. Die temperature is measured, and when a 150°C threshold is reached, the device enters shutdown. When the die cools sufficiently, the device will restart (assuming input voltage exists and the device is enabled). Hysteresis of 25°C prevents low frequency oscillation between start-up and shutdown around the temperature threshold.

Power Supply Sequencing

The AS1376 requires two different supply voltages active at the same time for correct operation.

- V_{IN} : Input Supply Voltage
- V_{BIAS} : Bias Supply Voltage

It's important that V_{IN} does not exceed V_{BIAS} at any time. If the device is used in the typical post regulation application as shown in Figure 20, the sequencing of the two power supplies is not an issue as V_{BIAS} supplies both, the DC-DC regulator and the AS1376. The output voltage of the DC-DC regulator will take some time to rise up and supply V_{IN} of AS1376. In this application V_{IN} will always ramp up more slowly than V_{BIAS} . In case V_{IN} is shorted to V_{BIAS} , the voltages at the two supply pins will ramp up simultaneously causing no problem. Only in applications with two independent supplies connected to the AS1376 special care must be taken to guarantee that V_{IN} is always $\leq V_{BIAS}$.

Auto Discharge

When the AS1376 is placed in shutdown, a 100Ω path to ground is connected at the output. This path speeds up the discharge of the capacitor(s) connected to the regulator output. Assuming that V_{IN} remains constant and always $>V_{OUT}$, output discharge time is calculated as follows:

$$(EQ17) \quad V(t) = V_{REG} \times e^{-\frac{t}{RC}}$$

t ... specified time after regulator shutdown (sec)

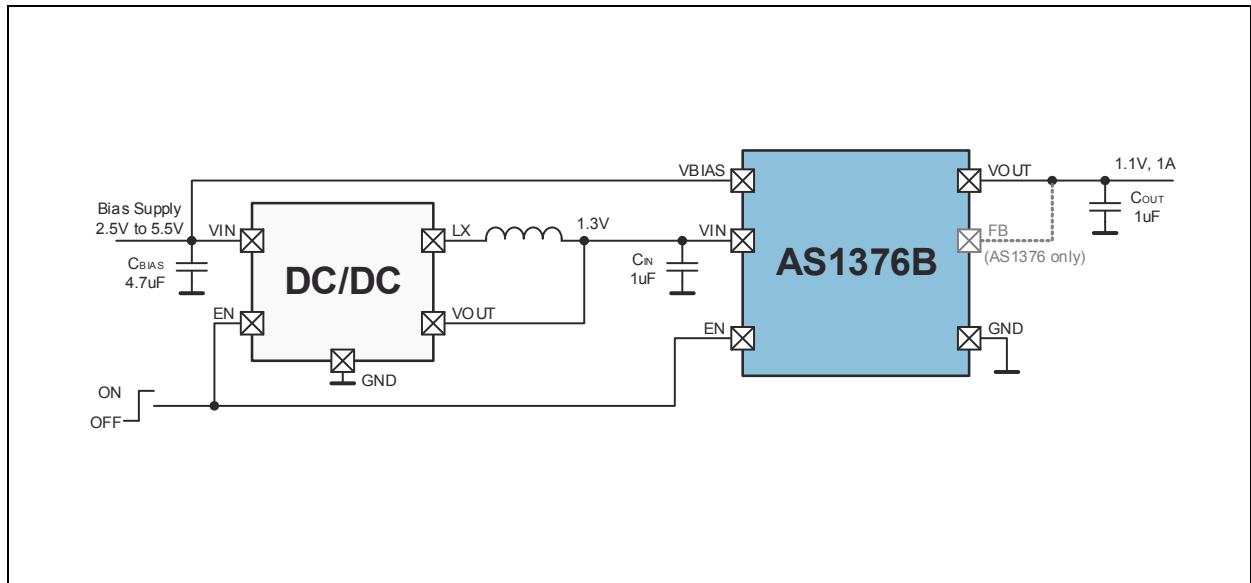
V_{REG} ... Regulated Output Voltage (initial condition)

R ... 100Ω(typ) discharge resistor

C ... Output Capacitor (F)

Application Information

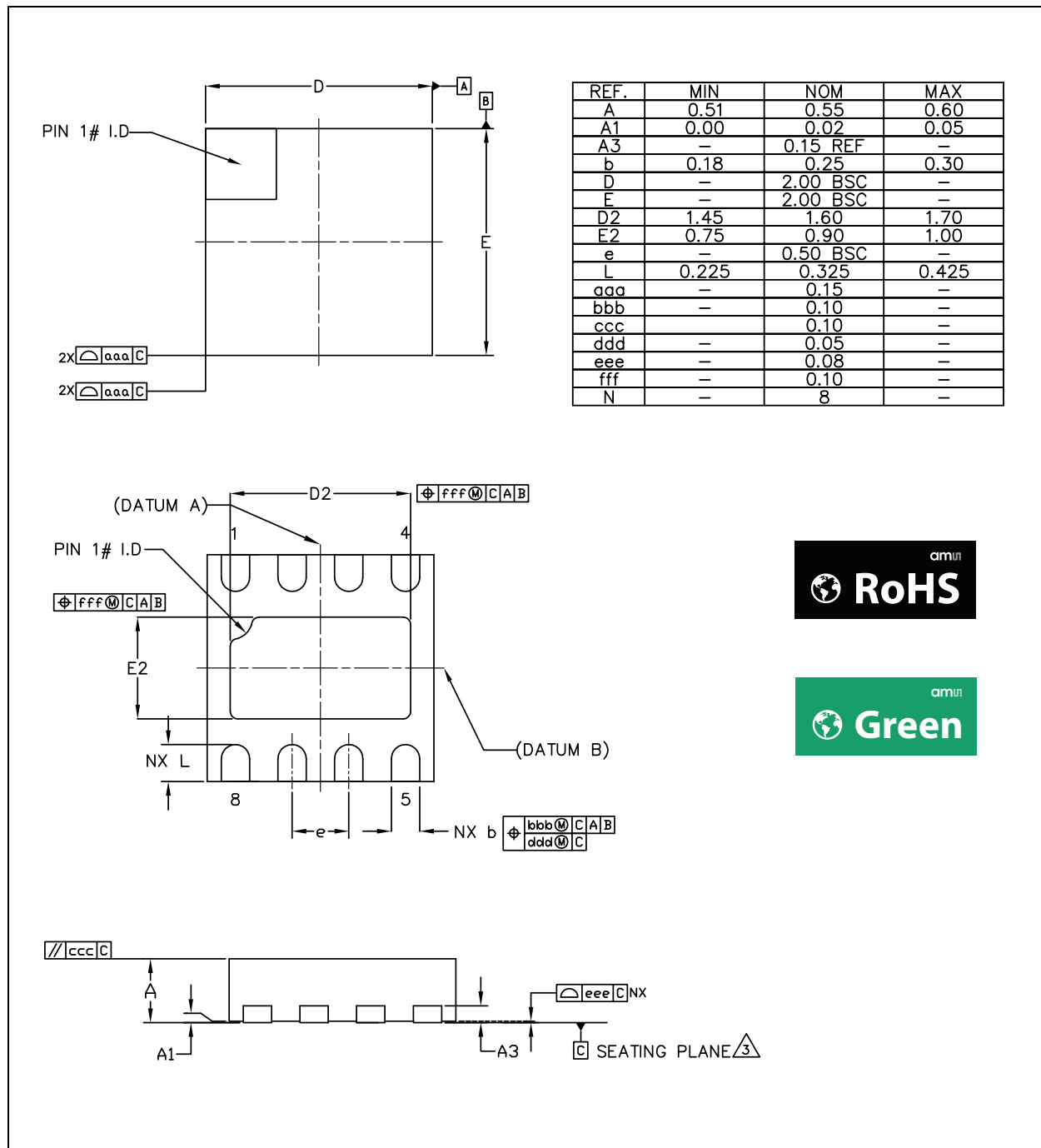
Figure 20:
Typical Application Diagram



Typical Application: This figure shows the typical application of the AS1376B for the 6-pin WL-CSP. The FB pin and the dotted line would be valid only for the AS1376 TDFN version

Package Drawings & Markings

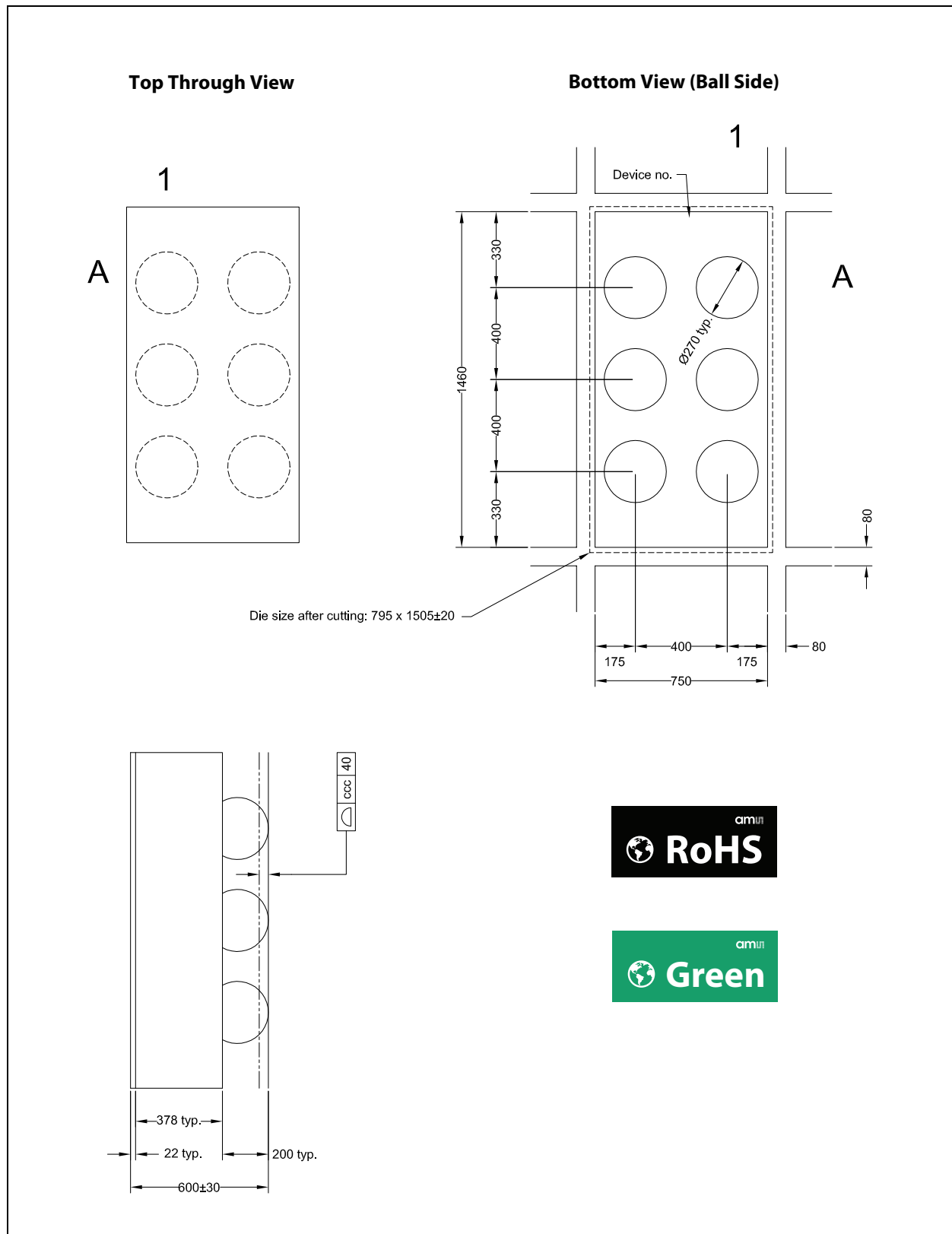
Figure 21:
MLPD-8 2x2 0.5mm Pitch Package Drawing



Note(s) and/or Footnote(s):

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

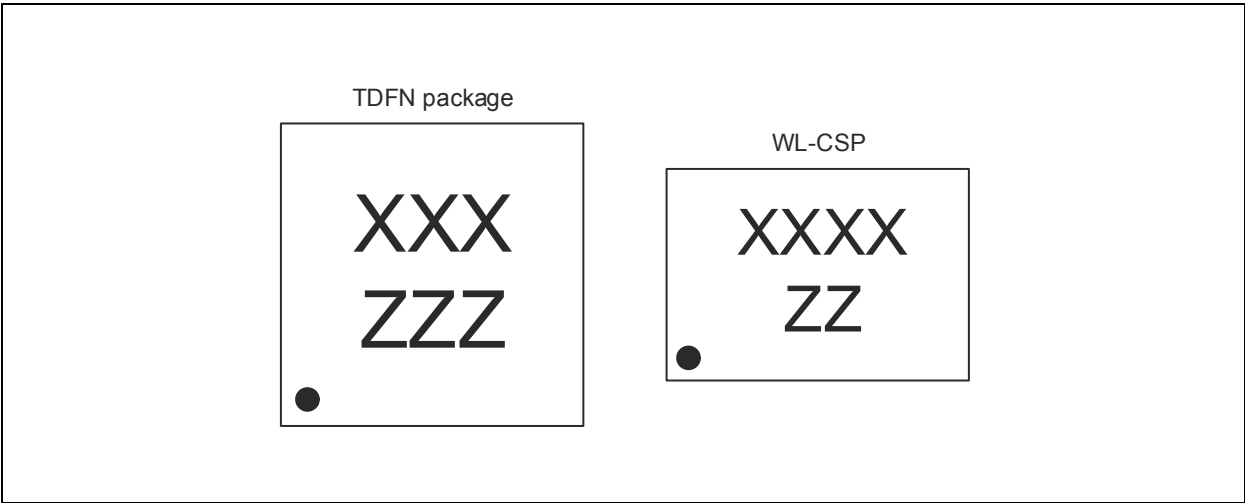
Figure 22:
WL-CSP-6 0.4mm Pitch Package Drawing



Note(s) and/or Footnote(s):

1. Pin 1 = A1
2. ccc Coplanarity
3. All dimensions are in μm .

Figure 23:
TDFN and WL-CSP Marking



AS1376 Marking: Shows the package marking of the TDFN and the WL-CSP product version

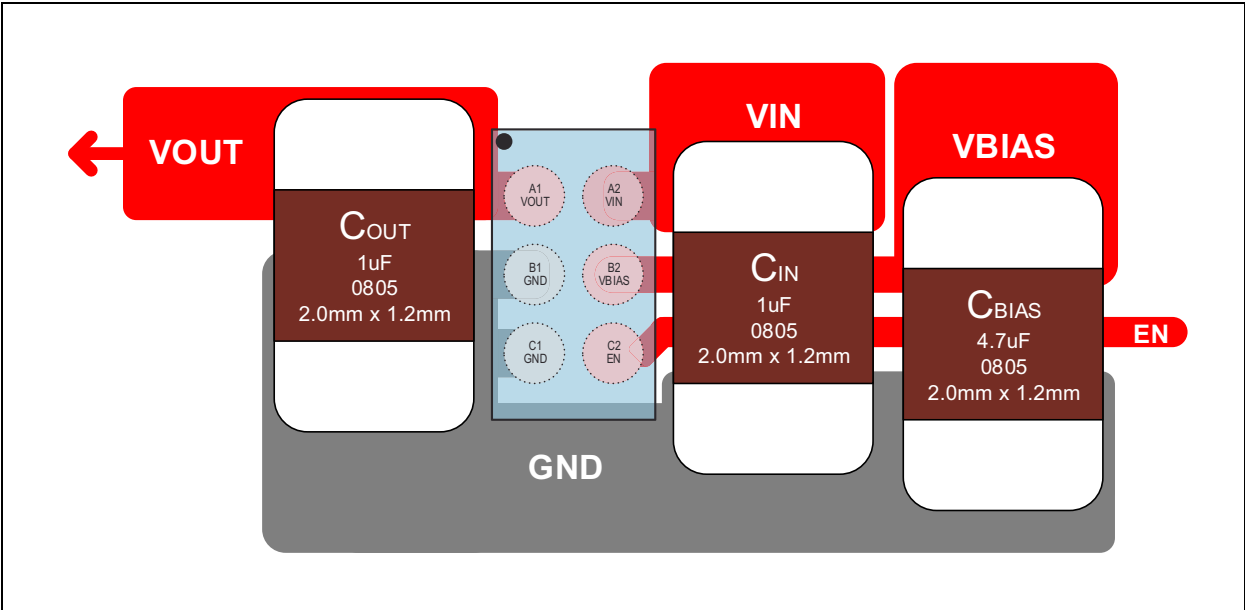
Figure 24:
Package Code

| XXX | ZZZ | XXXX | ZZ |
|--------------------|-----------------------|----------------------|-------------------------|
| Tracecode for TDFN | Marking Code for TDFN | Tracecode for WL-CSP | Marking Code for WL-CSP |

Package Codes: Shows the package codes of the TDFN and the WL-CSP product version

PCB Pad Layout

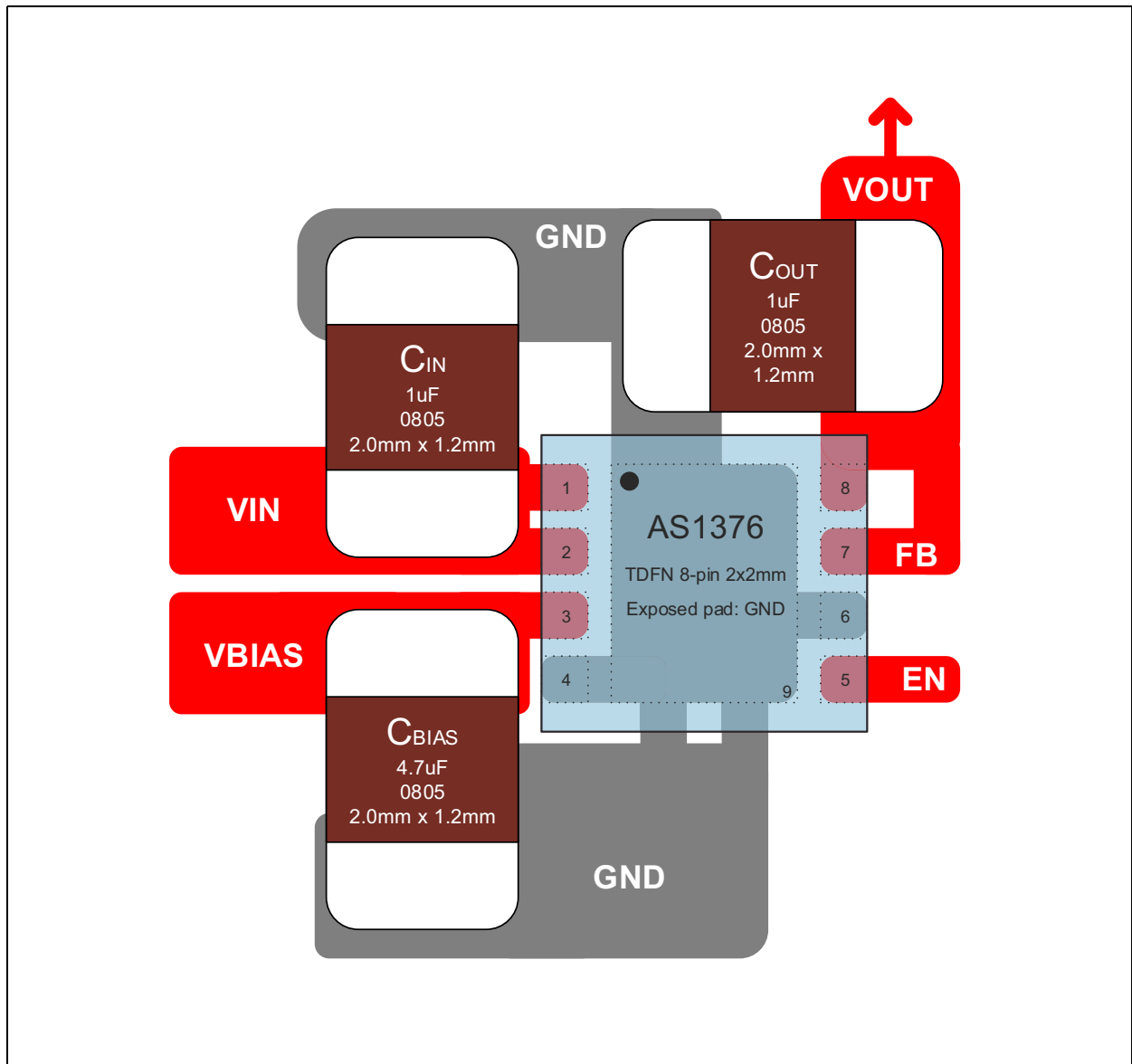
Figure 25:
PCB Layout Recommendation for the 6-Balls WL-CSP Option



WL-CSP Layout Guidelines: This figure shows the recommended layout and placement of the external components for the AS1376B version. Red lines are connections on TOP layer. Grey lines are GND connections on

TOP layer.

Figure 26:
PCB Layout Recommendation for the 8-Pins TDFN Package Option



TDFN Layout Guidelines: This figure shows the recommended layout and placement of the external components for the AS1376 version for fixed trimmed output voltages. Red lines are connections on TOP layer. Grey lines are GND connections on TOP layer.

Ordering & Contact Information

Figure 27:
Ordering Information

| Ordering Code | Package | Marking | Output | Delivery Form | Delivery Quantity |
|-------------------------------|------------------|---------|--------|---------------|-------------------|
| AS1376-BTDT-AD ⁽¹⁾ | 8-pin 2x2mm TDFN | ABL | Adj. | T&R | 1000 pcs/reel |
| AS1376-BTDT-12 | 8-pin 2x2mm TDFN | ABT | 1.2V | T&R | 1000 pcs/reel |
| AS1376B-BWLT-11 | 6-balls WL-CSP | D3 | 1.1V | T&R | 12000 pcs/reel |
| AS1376B-BWLM-11 | 6-balls WL-CSP | D3 | 1.1V | T&R | 1000 pcs/reel |

Ordering Information: Specifies the available variants of AS1376

Note(s) and/or Footnote(s):

1. Available on request

Buy our products or get free samples online at:

www.ams.com/ICdirect

Technical Support is available at:

www.ams.com/Technical-Support

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Document Status

| Document Status | Product Status | Definition |
|--------------------------|-----------------|--|
| Product Preview | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice |
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| 1.3 (2011-Oct) to 1.4 (2011-Dec) | |
| Updated Power Dissipation | 12 |
| 1.4 (2011-Dec) to 2-00 (2014-Nov) | |
| Update to new datasheet design | |
| New package option inserted | |
| 2-00 (2014-Nov) to 2-01 (2014-Nov) | |
| Updated Ordering Information | 27 |
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Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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