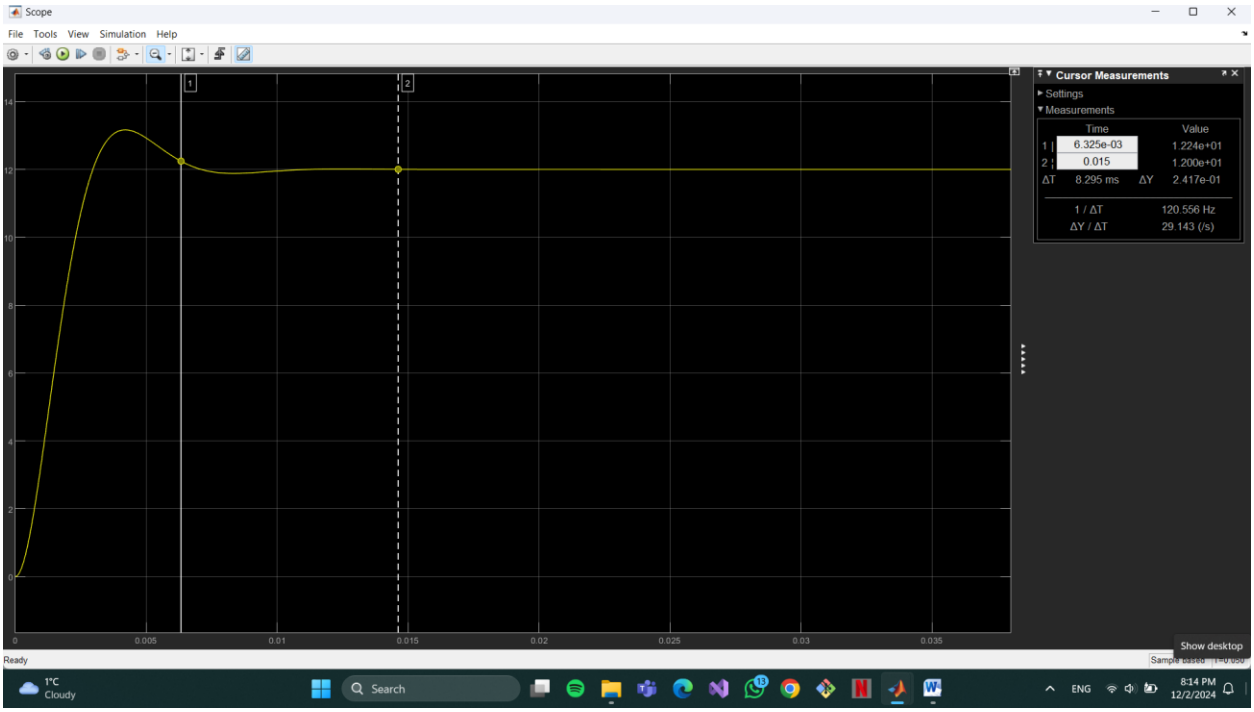
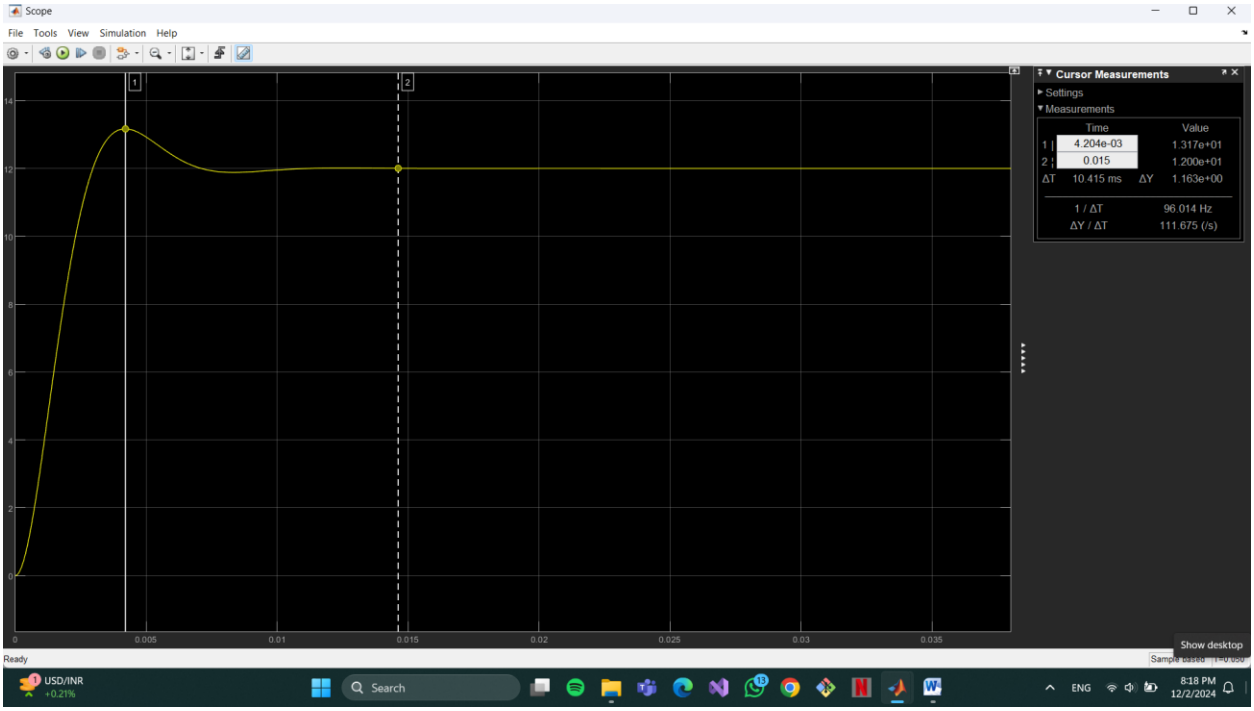
Power electronics project part 3

for the calculated output voltage from part 2 => settling time = 0.00841 s & overshoot = 0

for when the “Zero-Order Hold” = (PWM period)/10 & tr = 0.007 & sigma = 0.09

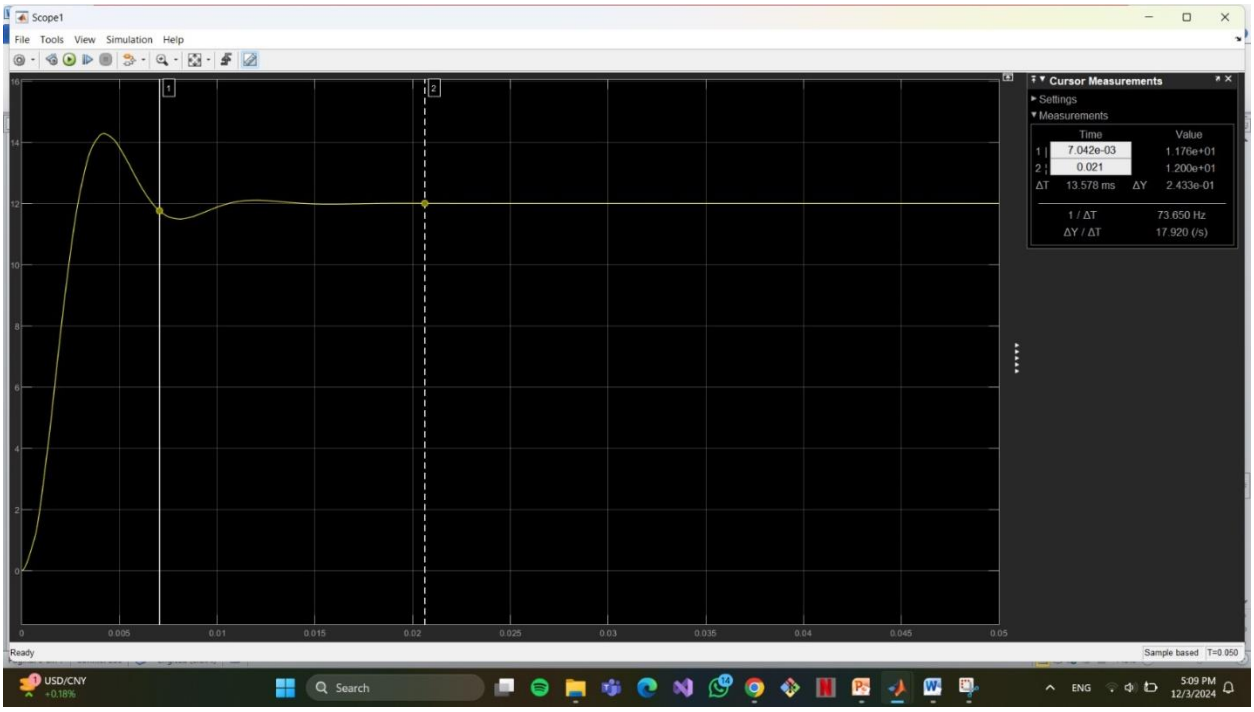
=> settling time = 0.006325 s & overshoot = 0.0975

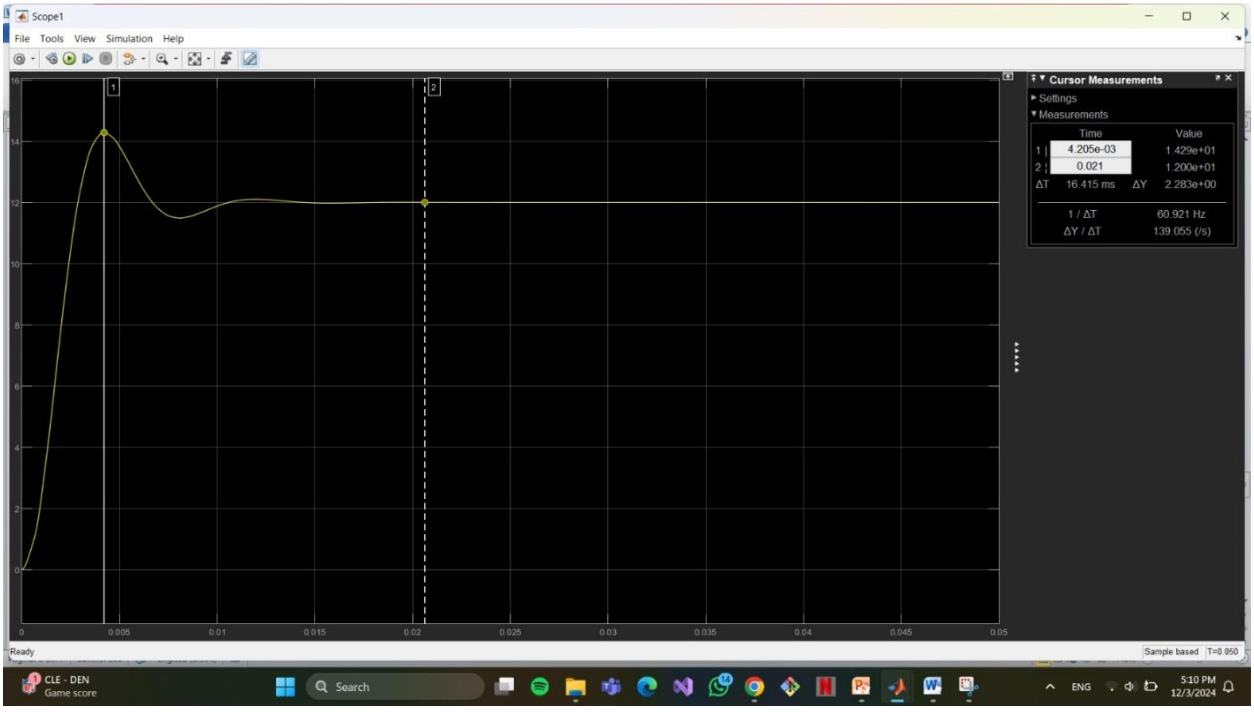




for when the “Zero-Order Hold” = PWM period & tr = 0.007 & sigma = 0.09

=> settling time = 0.007042 s & overshoot = 0.19



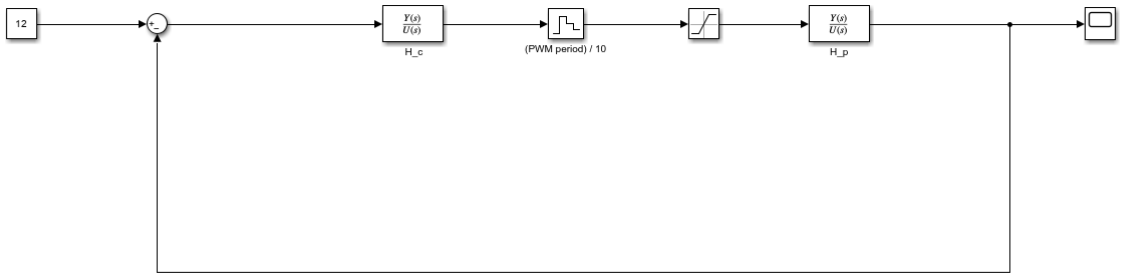


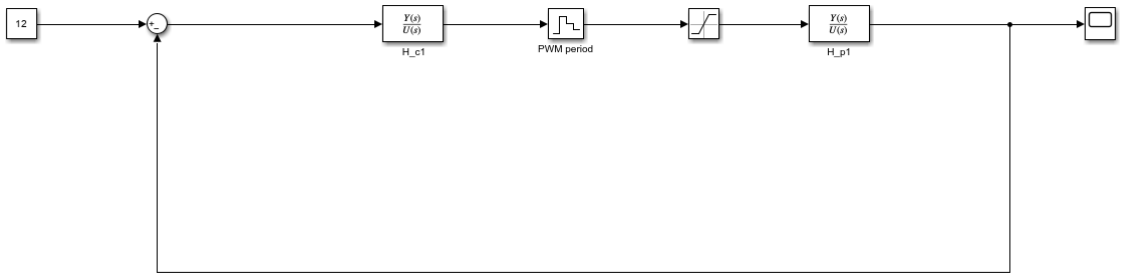
Settling Time: In comparison to the PWM/10 case (0.006325 seconds), the settling time increases to 0.007042 seconds when the period of the Zero-Order Hold block equals the PWM period which shows a slower response.

Overshoot: A less damped response is indicated by an increase in overshoot to 0.19 in the case when the Zero-Order Hold block equals the PWM period.

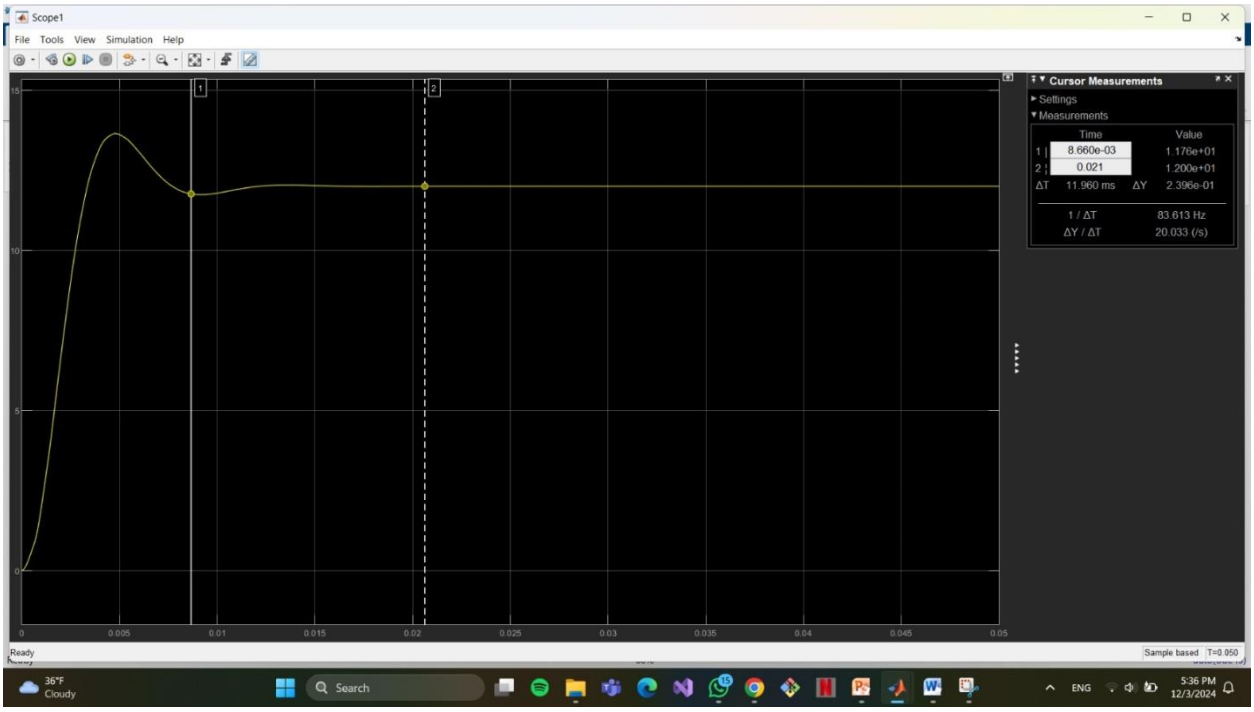
Code & Simulink:

```
clc
clear

miu = 0.25;
R = 2.4;
L = 0.006;
C = 0.000104;
Id =3.75;
It_max =5.5;
U_in = 48;
U_out = 12;
frequency = 1500;

sigma = 0.09;
t_r = 0.007;
zeta = (abs(log(sigma)))/sqrt(log(sigma)^2 + pi^2);

w_n = 4/(t_r* zeta);

A = [0 -1/L; 1/C -1/(R*C)];
B = [U_in/L; 0];
C = [0 1];
D = 0;

[nump, denp] = ss2tf(A, B, C, D);
H_p = tf(nump, denp);

H_o = tf([0, w_n^2], [1, 2*zeta*w_n, w_n^2]);
H_c = 1/H_p * H_o/(1-H_o);
% H_c = 1/H_p * feedback(H_o, 1);
[numc, denc] = tfdata(H_c);
```





for when the “Zero-Order Hold” = PWM period & tr = 0.007 & we change sigma to be 0.06
=> settling time = 0.008660 s & overshoot = 0.1375



Decreasing sigma to 6% reduces the overshoot to 0.1375, adjustment that improves the output signal stability by compensating for the sampling error.