A Modified Class D Resonance Inverter for Operating in Load Independent Condition

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***Abstract*—This paper presents a new topology to reduce the largest limitation on resonant inverters due to the resonance frequency dependency to load change. Load power variation under different conditions causes the resonant circuits become inductive or capacitive and consequently current flowing through switches will be lagging or leading in which in both cases eliminates the soft switching properties of the resonant circuits. By proposing new structure zero-current switching (ZCS) will be fulfilled and the current of the switches becomes load independent. The proposed topology reduces fabrication costs and overall losses and also the size of the converter will be reduced. The modeling and analysis has been supported with detailed simulation to verify the proposed topology.**

Keywords—inverter; resonant circuits; soft switching; zero-current switching (ZCS); class D inverter.

I. Introduction

Today, one of the most important issues in the field of designing power electronic converters especially power inverters is the loss level and especially the switching losses. In the power electronic converters increasing losses will result in increase of operating temperature of the switch and thus reduce its useful life span and consequently the overall efficiency of the converter will decrease. Higher useful life is one of the factors that increases reliability in different applications of inverters. The best solution to reduce switching losses is to use resonance techniques implemented by resonant circuits. One of the main features of resonant circuits is their low switching losses that makes them suitable for megahertz switching inverter applications [1]. In the meantime, the resonant circuits are subdivided into different classes. These circuits use the natural frequency generated by the quadrature circuits to make the switch current to zero before 'off' state transition of the switch, and then after 'on' state transition of the switch its current increases to reach its maximum value. On the other hand the voltage of the switch terminals could reach to zero before the switch transitioning 'on' state and the switching losses reduced to a very small amount before the increasing of the current.

Resonant circuits are generally divided into three main classes: class D, class E and class ϕ. In addition to the three general categories mentioned there are other circuits that have been proposed in which they are combination of main classes or quasi-resonant circuits, which are: Class DE which is usually used in DC-DC converters, Class EF which is related to amplifiers and quasi-resonant circuits which LCL circuits fall into this category. Class E inverters are well documented in the literature [2-6] and have been widely used in wireless power transfer (WPT) applications [7-9]. Class E and Class EF inverters are sensitive to load variation compared to Class D inverters and therefore when the load is not in optimum value the efficiency will be decreased. At first the load-independence Class E inverters concept was proposed in 1990 by zulinski [10]. In [11-13] the load-dependency of Class EF inverters was further investigated. In [14] a load independent Class EF inverter is proposed that achieves zero current switching (ZCS) and produces a constant output current, rather than a constant output voltage, regardless of the load resistance. The proposed method just regards the load current and does not have capability of regulating output voltage. There are several approaches to enable ZCS operation of Class E and Class EF inverters. One of the solutions to ZCS operation of mentioned classes is tune the inverter actively by the load change and one of the ways of tuning the class E inverter is saturable reactors and varactors [8]. The main drawback of these methods is the control loop and tuning elements that these elements can limit the handling capability and efficiency [15].

Class D inverters are divided in two categories: voltage switching and current switching. The advantage of the current switching type over the voltage switching is that the shoot-through does not occur to the source, but the disadvantage of this type is the increased voltage stress on the switches. In the voltage switching type, the voltage on the switches is equal to the input voltage. To reduce the voltage on the switches in the current switching type the snubber networks could be used [16]. Class D voltage-switching inverters have many attractive characteristics such as high efficiency, small size, light weight, fast dynamic response, and low noise levels. Another principal advantage of a Class D voltage switching inverter is low voltage across the switches which is equal to the input voltage [17]. For variable output power applications the Class D inverters are studied in the literature. Class-D half-bridge converter is used in the high output power range, whereas class-DE half-bridge converter [18,19] is used in the low to medium output power range. The combination of these operation modes achieves high

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efficiency levels in a wider range of output power levels. In [20] the use of half-bridge Class D inverter is investigated.

In this paper, a new resonance circuit is introduced to overcome greatest limitation of current inverters, which is the load dependence of the resonant frequency. The proposed topology reduces costs and losses and reduces the size of the converter.

II. System Structure and Control Design

A. Electrical Configuration

Complete electrical circuit of the proposed model has been presented is shown in fig.1. The class D inverter is combined with auxiliary circuit circuit to help the main switch to turn off in the load change situations. As it is clear, the boost circuit has been designed to control the input voltage of class D inverter.

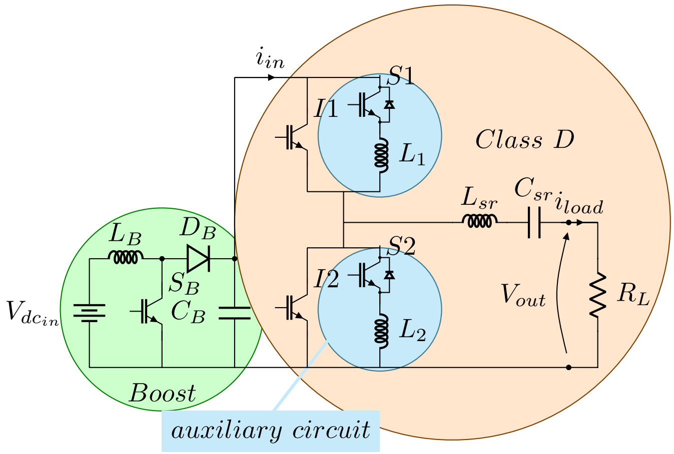

Fig. 1. Proposed Electrical Configuration

B. Proposed Model Design

The parts which are connected in parallel with I_1 and I_2 are considered as auxiliary circuit part. Also, the C_{sr}, L_{sr} and the load which are connected in series are considered as series resonance part. Knowing the minimum output power of the load is necessary for series resonance design. To understanding the circuit performance it is important to following equations of the proposed inverter. In the first half cycle only the S_1 switch is "On" and in the second half cycle only the S_2 switch is "On". The state space of the circuit for these two half cycles has been written as follows,

$$\begin{cases} A = \begin{bmatrix} \frac{-(r_{s_{on}}+r_{L_{sr}}+R_{load})}{L_{sr}} & \frac{-1}{L_{sr}} \\ -\frac{1}{C_{sr}} & 0 \end{bmatrix} \\ B = \begin{bmatrix} \frac{D}{L_{sr}} & -\frac{1}{L_{sr}} & -\frac{R_{load}}{L_{sr}} \\ 0 & 0 & 0 \end{bmatrix} \\ \begin{bmatrix} \dot{i}_{L_{sr}} \\ \dot{v}_{C_{sr}} \end{bmatrix} = A \begin{bmatrix} i_{L_{sr}} \\ v_{C_{sr}} \end{bmatrix} + B \begin{bmatrix} V_{in} \\ V_{S_{on}} \\ I_Z \end{bmatrix} \end{cases} \tag{1}$$

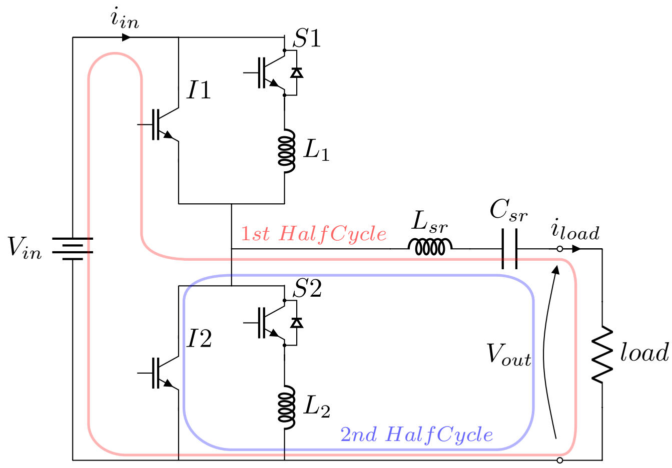

Fig. 2. Current Flow Path in Minimum Load Condition

$$y = \begin{bmatrix} R_{load} & 0 \end{bmatrix} \begin{bmatrix} i_{L_{sr}} \\ v_{C_{sr}} \end{bmatrix} + \begin{bmatrix} 0 & 0 & -R_{load} \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{S_{on}} \\ I_Z \end{bmatrix} \tag{2}$$

As it is clear, $V_{out} = R_{load} i_{load}$, $i_{load} = {}^{V_{in}}/_{Z}$ and $Z = z_{Csr} + z_{Lsr} + z_{load}$ the relationship between V_{in} and V_{out} in time domain can be described as (3),

$$\begin{cases} \omega = \sqrt{\frac{1}{L_{sr}C_{sr}} - \frac{R_{load}^2}{4L_{sr}^2}} \\ \frac{V_{out}}{V_{in}} = \frac{R_{load}}{L_{sr}} e^{\frac{-R_{load}}{2L_{sr}}} [\cos(\omega t) - \frac{R_{load}}{2L_{sr}} \frac{1}{\omega} \sin(\omega t)] \end{cases} \tag{3}$$

From the above, angular frequency of the circuit is equal to $\sqrt{\frac{1}{L_{sr}C_{sr}} - \frac{R^2}{4_{sr}L^2}}$ and it means that R_{load} and ω are inversely related and if the load decreases the i_{load} tends to lag phase respect to voltage which it demonstrates the capacitance manner of series resonance. Now in the following parts the system behavior in Minimum and Excessive Load conditions will be analyzed, and in the last part of this section, the design of series and auxiliary circuits will be described.

1) Minimum Load

Since the IGBTs (I_1 and I_2) have no inductance against auxiliary circuit parts, the IGBT side have a extremely low impedance against MOSFET side, therefore, the current flows through IGBT sides and it has been shown in Fig.2. Also, as it mentioned above, the series resonance circuit is designed based on minimum output power, hence, in this situation the C_{sr} and L_{sr} behave like a short circuit and therefore the voltage and current of output are in the same phase. It means that at the first and last moment of each half cycle, the current is zero and each half cycle has a complete half sine wave.

2) Excessive Load

In the excessive load condition, the angular frequency of the circuit rises and therefore the current tends to lead phase

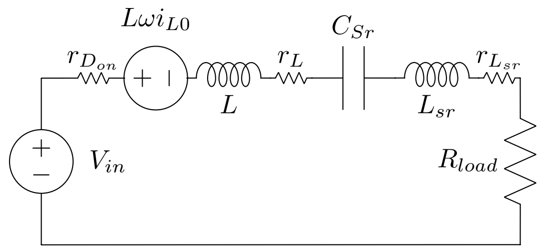

Fig. 3. Equivalent Circuit of Auxiliary Circuit

and it causes the negative current before changing the switching cycles. In the first half cycle, the negative current flows through MOSFET back diode of upper leg.

After the upper leg switches are turned off and the 1st half cycle is ended, the next half cycle is started with the lower leg IGBT turning ”On”. As we know, the current is in lead phase and it does not start from zero in the 2nd half cycle. At the beginning of the second half cycle, current flows through upper leg diode and the lower leg IGBT does not endure extra current at the turning ”On” moment.

Because of the lead current, at the end of the second half cycle, current still is not zero and this time has a positive value. As well as the first half cycle, the lower leg diode passes the remained positive current and the upper leg IGBT does not endure extra current at the turning ”On” moment.

3) Series Resonance

To design the series resonance parameters, the switching frequency, Q factor and the load resistor are required. The series resonance parameters are calculated by the following equations.

$$\begin{cases} \omega_0 = 2\pi F \\ \alpha = \frac{\omega_0}{2Q} \\ L_{sr} = \frac{R_{load}}{4\alpha} \\ C_{sr} = \frac{4L_{sr}}{R_{load}^2(1+Q^2)} \end{cases} \tag{4}$$

There are two major limitations to select the series inductance and capacitance. As we are aware, more Q factor indicates that the waveform is more closer to sinusoid, therefore the lower Q decreases the power quality. According to the above equation, the higher Q factor causes the lower capacitance and based on $q = CV$ relationship, higher capacitor leads to more voltage on capacitor which it is not desirable. Therefore, the series parameters should be selected to Q factor and capacitor voltage have acceptable values.

4) Auxiliary Circuit

Without using auxiliary circuit, at the switching time of IGBT current becomes zero in each leg in an instance which is meant switches work in the hard switching zone. To solving this problem it is necessary to implement auxiliary circuit with specific inductance to decreases $\frac{di}{dt}$ value greatly.

TABLE I. Simulation Parameters

Parameter	**Values**
Load	$R_{load} = 357\Omega$
Series Resonance Capacitance	$C_{sr} = 0.9nF$
Series Resonance Inductance	$L_{sr} = 2.8mH$
Auxiliary Circuit Inductance	$L = L_1 = L_2 = 7\mu H$
Input Voltage	$V_{dc_{in}} = 10v$

According to the equivalent circuit shown in Fig.3, the auxiliary inductance calculated from the following equation. As it is clear the ω also equals to $\frac{2\pi}{T}$ which T is the discharge time of auxiliary inductance.

$$\begin{cases} \omega = \sqrt{\frac{4(L+L_{sr})-C_{sr}(R_{load}+r_L+r_{D_{on}})^2}{4(L+L_{sr})^2 C_{sr}}} \\ L = \frac{1}{\omega^2 C_{sr}}\sqrt{\frac{1}{4\omega^4 C_{sr}^2} - \frac{(R_{load}+r_L+r_{D_{on}})^2}{4\omega^2}} \end{cases} \tag{5}$$

III. Simulation Results

In order to evaluate the proposed system, simulation studies are carried out in MATLAB/Simulink environment with 10MHz and 100kHz sampling and switching frequencies, respectively. The designed system parameters are provided in the Table 1.

1) Minimum Load Case in Modified Topology

The minimum resistance load considered as 357Ω and the switching and resonance frequencies are equal. As shown in Fig. 4, since the series resonance is a 2nd degree circuit, it causes almost pure sine wave for load voltage and current. Also, it can be realized that the upper leg switch current is almost zero and upper leg current flows completely through IGBT side and proves what has described in section II. It should be noted that current of the lower leg flows through IGBT side same as the upper leg.

Also, Fig. 4 shows the IGBT voltage and current. From the Fig. 4, the IGBT current is zero at switching times which it demonstrates the soft switching feature that happens automatically in the minimum load condition.

The total harmonic distortion of load current is 2.69% and its harmonic spectrum is shown in Fig. 5. The output voltage of boost circuit is shown in Fig. 6 and it can be seen that the $10v$ input voltage transform to the $45v$ output voltage less than 0.01 second.

2) Excessive Load Case in Modified Topology

In this case, the load value has been increased about 30 times higher than minimum load and its voltage and current waveform can be seen in Fig. 7. As it mentioned in section II, since the current has lag phase respect to voltage in this case, current flows over the IGBT and MOSFET. Because of inductance element in MOSFET path, the current flows more through the IGBT side.

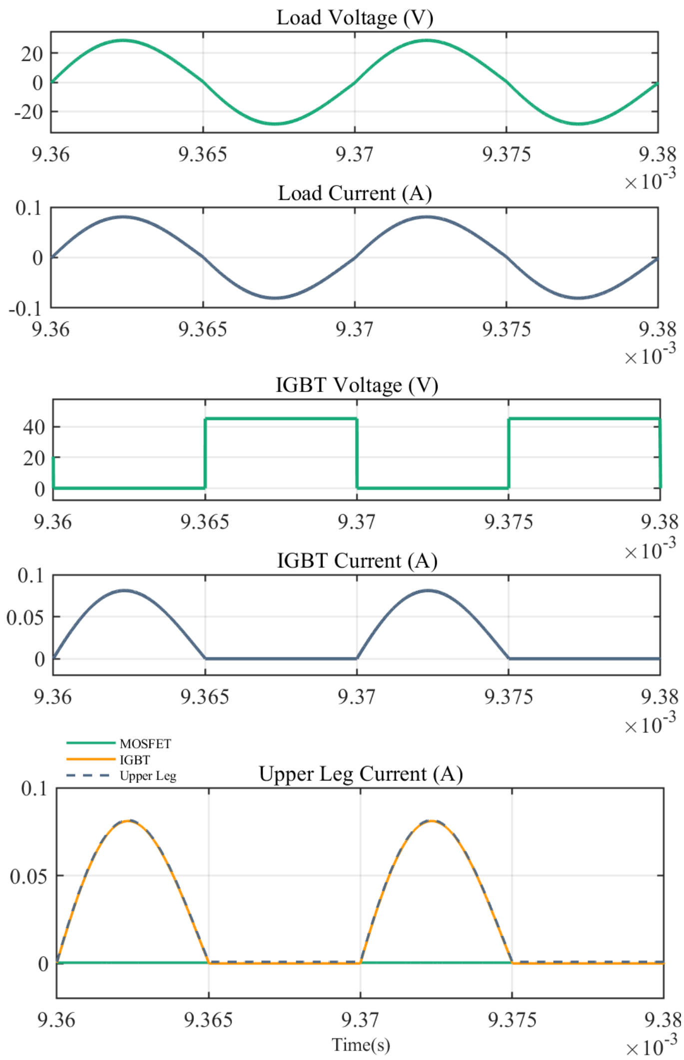

Fig. 4. Load and IGBT Voltages, and IGBT and Upper Leg Currents in Minimum Load

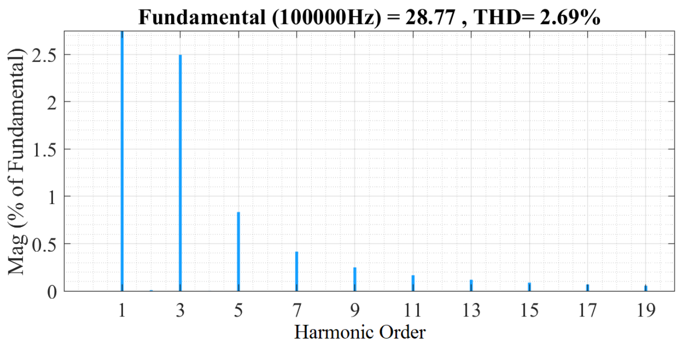

Fig. 5. Harmonic Spectrum of Load Current in Minimum Load

As shown in Fig. 7, current is not zero at the switching time of IGBT and it has a negative value when the IGBT is "ON" in upper leg. At this case, despite of the minimum load case, the negative current flows through diode of MOSFET. At the switching time of IGBT current becomes zero in $18e^{-8}s$.

From Fig. 8, in this case the total harmonic distortion of

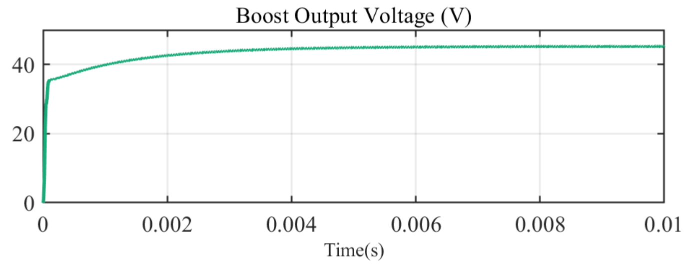

Fig. 6. Boost Dynamic Performance in Minimum Load

load current waveform is about 0.2% which is more than 10 times less than minimum load case. Also, because of using auxiliary side elements in current flow path, the output voltage of boost circuit is higher than previous case and approximately is equal to $76v$ and dynamic performance of boost circuit is shown in Fig. 9.

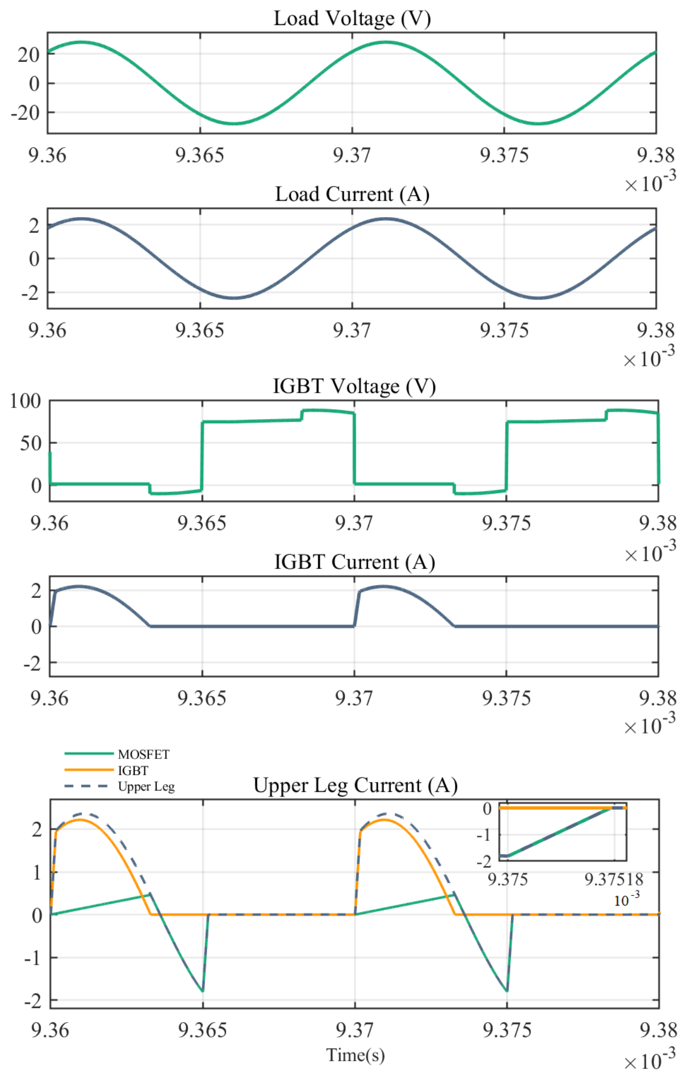

Fig. 7. Load and IGBT Voltages, and IGBT and Upper Leg Currents in Excessive Load

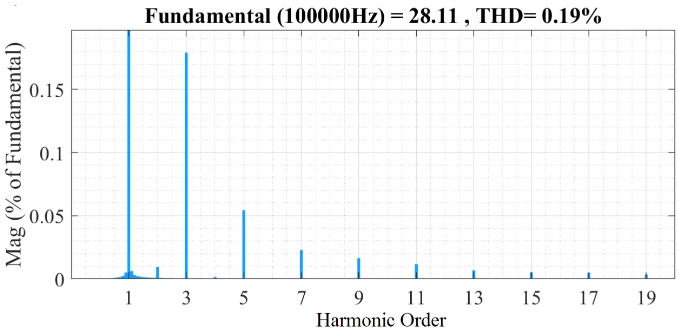

Fig. 8. Harmonic Spectrum of Load Current in Excessive Load

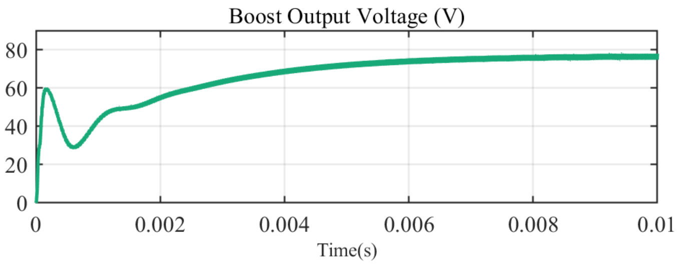

Fig. 9. Boost Dynamic Performance in Excessive Load

3) Excessive Load Case in Conventional Topology

In conventional method, instead of using parallel IGBT and MOSFET, only MOSFET is used in each leg. As seen in Fig. 10, at the switching time of IGBT current becomes zero in $1e^{-9}s$ and since the current changing time equals to sampling time which means if the sampling time becomes lower than current value, the current changing time value will be decreased as well and it show in conventional method current at IGBT switching time current becomes zero in an instant.

As it mentioned before, in conventional method the value of $\frac{di}{dt}$ is extremely high and it makes switches work in hard switching zone.

IV. Conclusion

In this paper a new Class D inverter topology has been proposed for the resonant circuits field. The class D resonance power stage voltage source which used in this design has high energy density and efficiency and also low voltage stress on the switches. On the other hand, the proposed auxiliary circuit eliminates the greatest limitation of resonant circuits and ZCS capability maintains at a wide range of load variation. The simulation results illustrate that proposed topology extremely decreased $\frac{di}{dt}$ from infinity value to $10e^6 A/s$ at the IGBT switching time and proves that the topology makes switches to work in soft switching zone. Also, the simulation results shown the topology have a great performance in minimum load and in very high load conditions and finally it demonstrates us the proposed system can work in load independent condition excellently.

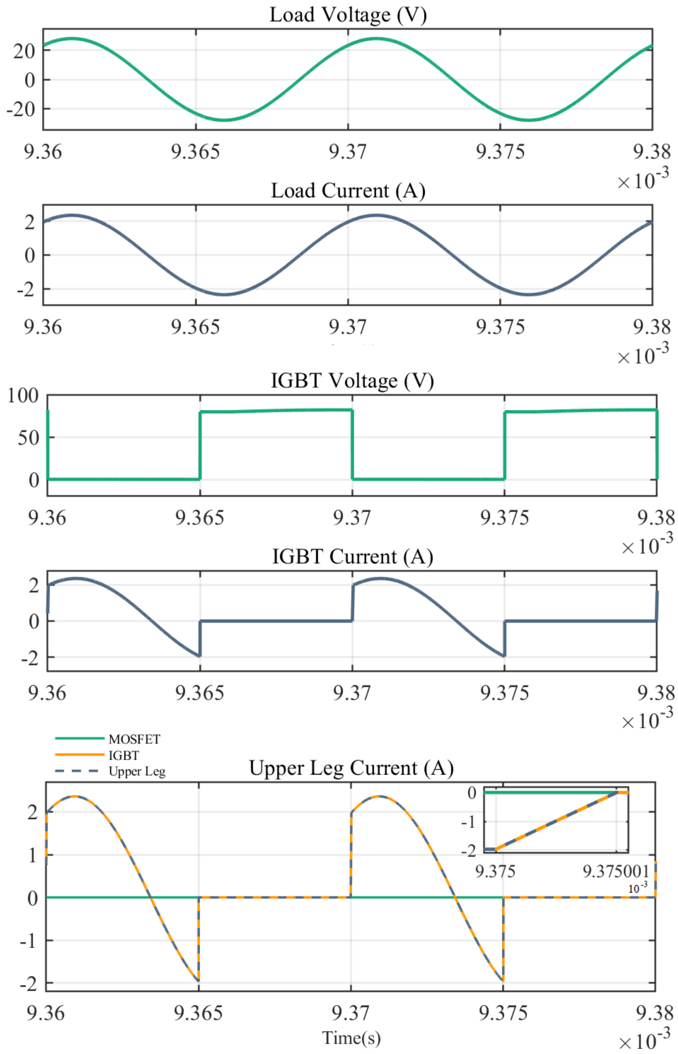

Fig. 10. Load and IGBT Voltages, and IGBT and Upper Leg Currents in Excessive Load (Only MOSFET in Upper Leg)

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