Initials: Manit Gandhi

1. Caching Benefits [20 points]

(a) What is the benefit of caching?

Speeds up loading data
Uses less resources
Reduces retrieval data time.

For the following questions, assume that there are three level of caches. The L1 cache has 1 cycle access latency, L2 cache has 5 cycles access latency, L2 cache has 10 cycles access latency and the main memory has 50 cycles access latency.

Assume that the program you are running has 80% L1 cache hit rate, 80% L2 cache hit rate, and 80% L3 cache hit rate.

(b) How many cycles is required to process 1000 memory requests? (**Hint:** Please remember that accessing a higher lever cache require the processor to know that an access to an earlier level is a cache hit or a cache miss)

1000 requests → L1 (1000 cycles)
80% hitrates = 800 hits
200 requests → L2 (5×200 = 1000 cycles)
80% hitrates = 160
40 requests → L3 (10×40) = 400
80% hitrates = 32
8 requests → main mem (8×50) = 400

1000 + 1000 + 400 + 400 = 2800 cycles

(c) Is it possible for a program to have a 100% cache hit rate assuming that this is the first time the program is ever launched and there is no prefetching?

No

Why? Explain your answer.

Since its the first time, all requests are new which makes it a miss.

(d) What is the purpose of a tag store?

A tag store represents address and tells us if the data being looked up is in the cache or not.

2. Caching Basic [20 points]

(a) Assume a 32-bit byte-addressable process with a single level of cache. The cache is a 16-way set associavative cache with 16 cache sets. Each cache block is 32 bytes. What is the total cache size?

16 x 16 = 256
256 x 32 = 8192 bytes

(b) Please feel free to explain your answer for all the questions below.

Given the 32-bit address and the same assumption, what is the **set ID** (set ID starts from 0) for each of the following addresses (in hexadecimal number)?

0xABADBEEF

offset: $\log_2(8) = 13$ bits
set id: $\log_2 16 = 4$

D B
1101 1011
set id: 0xD

0xBEEEEEEF

E E
1110 1110
set id: 0x7

(c) What are the value of the **tag bits** for the following addresses (in hexadecimal number)?

0xFFFF0000

0x5678EFEF