

CMOS OR Gates

High-Voltage Types (20-Volt Rating)

CD4071B Quad 2-Input OR Gate

CD4072B Dual 4-Input OR Gate

CD4075B Triple 3-Input OR Gate

CD4071B, CD4072B, and CD4075B OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of CMOS gates.

The CD4071B, CD4072B, and CD4075B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

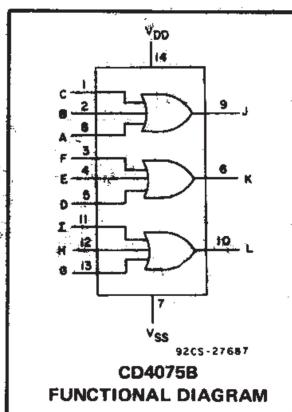
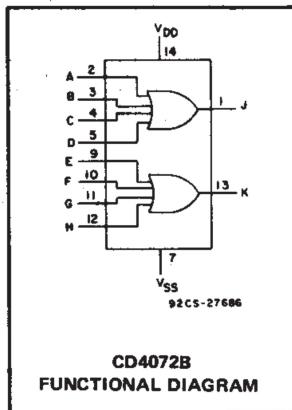
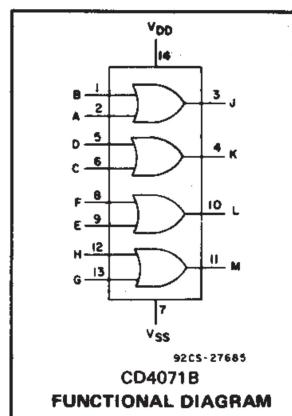
STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V_O (V)	V_{IN} (V)	V_{DD} (V)	+25				Min.	Typ.	Max.		
				-55	-40	+85	+125					
Quiescent Device Current, I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA	
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5		
	–	0,15	15	1	1	30	30	–	0.01	1		
	–	0,20	20	5	5	150	150	–	0.02	5		
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–		
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	mA	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–		
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–		
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V	
	–	0,10	10	0.05				–	0	0.05		
	–	0,15	15	0.05				–	0	0.05		
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V	
	–	0,10	10	9.95				9.95	10	–		
	–	0,15	15	14.95				14.95	15	–		
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V	
	1,9	–	10	3				–	–	3		
	1.5, 13.5	–	15	4				–	–	4		
Input High Voltage, V_{IH} Min.	4.5	–	5	3.5				3.5	–	–	V	
	9	–	10	7				7	–	–		
	13.5	–	15	11				11	–	–		
Input Current I_{IN} Max.		0,18	18	± 0.1	± 0.1	± 1	± 1	–	$\pm 10^{-5}$	± 0.1	μA	

CD4071B, CD4072B, CD4075B Types

Features:

- Medium-Speed Operation- t_{PLH} , $t_{PHL} = 60$ ns (typ.) at $V_{DD} = 10$ V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Standardized, symmetrical output characteristics
- Noise margin (over full package temperature range)
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4071B, CD4072B, CD4075B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT $\pm 10\text{mA}$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at $12\text{mW}/^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{STG}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch ($1.58 \pm 0.79\text{mm}$) from case for 10s max $+265^\circ\text{C}$

At distance $1/16 \pm 1/32$ inch ($1.58 \pm 0.79\text{mm}$) from case for 10s max $+265^\circ\text{C}$

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,
and $C_L = 50\text{ pF}, R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS		UNITS
		V_{DD} VOLTS	TYP.	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	125	250
		10	60	120
		15	45	90
Transition Time, t_{THL}, t_{TLH}		5	100	200
		10	50	100
		15	40	80
Input Capacitance, C_{IN}	Any Input	—	5	7.5
				pF

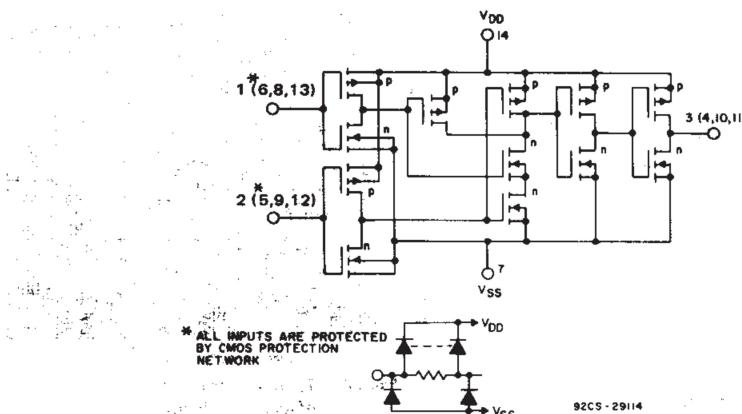


Fig. 3 — Schematic diagram for CD4071B (1 of 4 identical gates).

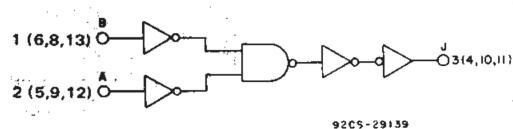


Fig. 5 — Logic diagram for CD4071B (1 of 4 identical gates).

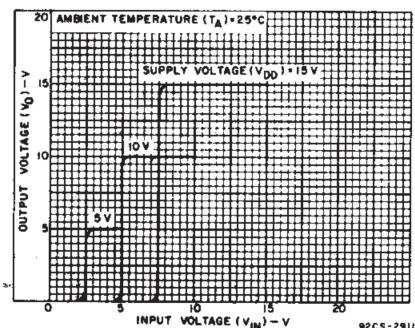


Fig. 1 — Typical voltage transfer characteristics.

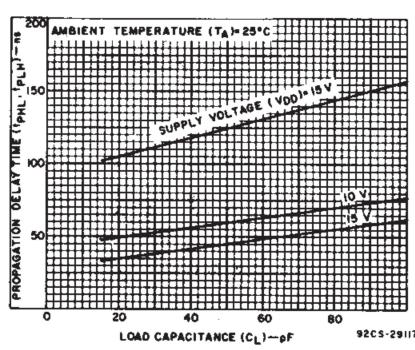


Fig. 2 — Typical propagation delay time as a function of load capacitance.

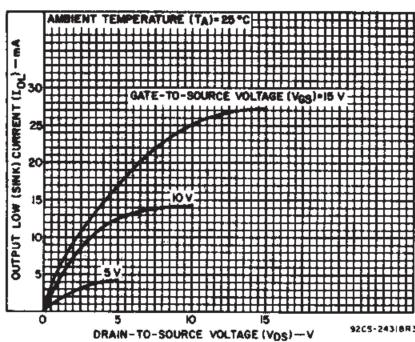


Fig. 4 — Typical output low (sink) current characteristics.

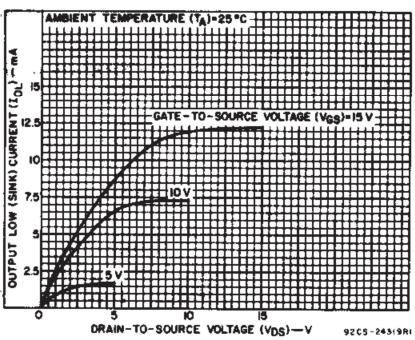


Fig. 6 — Minimum output low (sink) current characteristics.

CD4071B, CD4072B, CD4075B Types

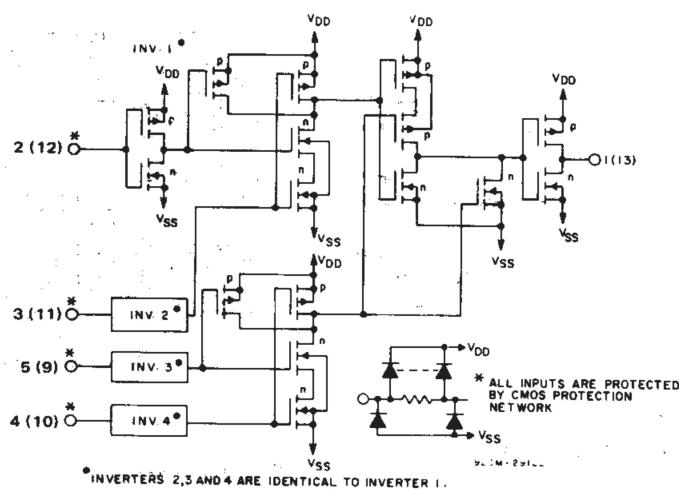


Fig. 7 – Schematic diagram for CD4072B (1 of 2 identical gates).

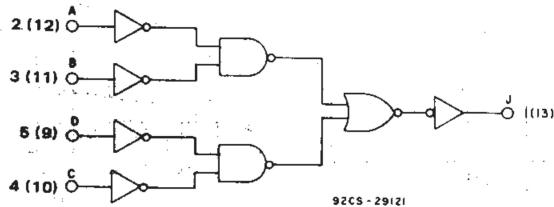


Fig. 9 – Logic diagram for CD4072B (1 of 2 identical gates).

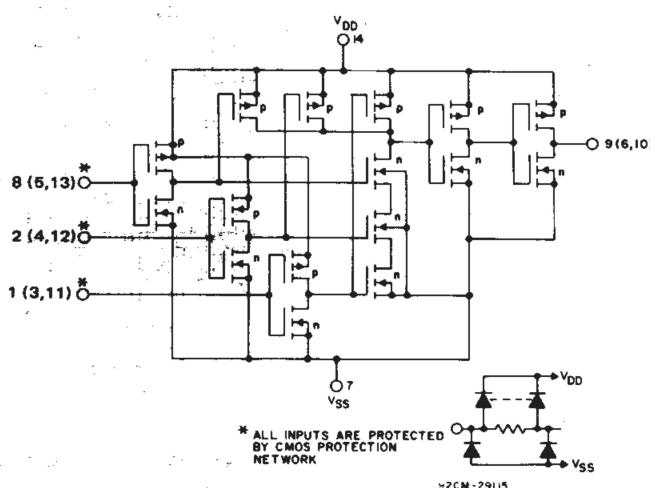


Fig. 11 – Schematic diagram for CD4075B (1 of 3 identical gates).

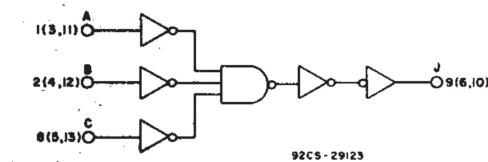


Fig. 13 – Logic diagram for CD4075B (1 of 3 identical gates).

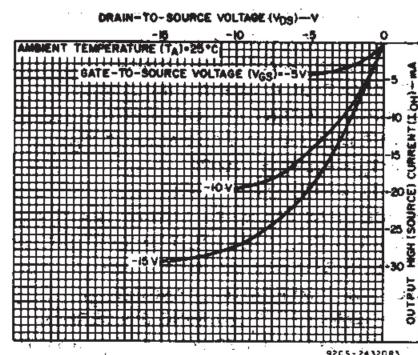


Fig. 8 – Typical output high (source) current characteristics.

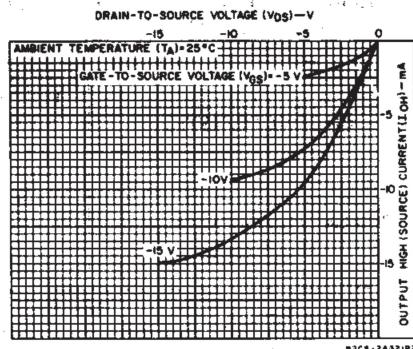


Fig. 10 – Minimum output high (source) current characteristics.

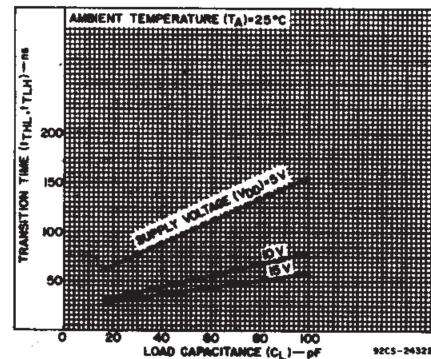


Fig. 12 – Typical transition time as a function of load capacitance.

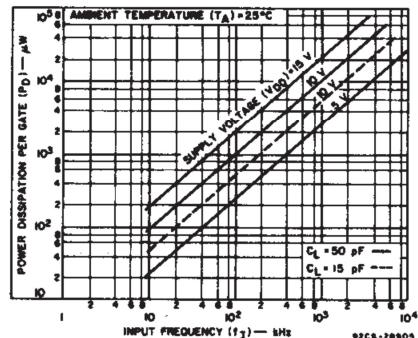


Fig. 14 – Typical dynamic power dissipation as a function of frequency.

CD4071B, CD4072B, CD4075B Types

TERMINAL ASSIGNMENTS (TOP VIEW)

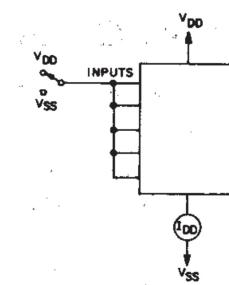
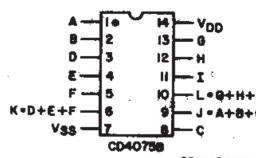
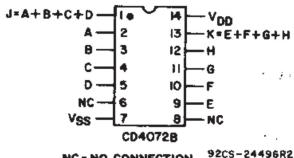
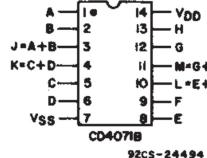


Fig. 15 — Quiescent device current test circuit.

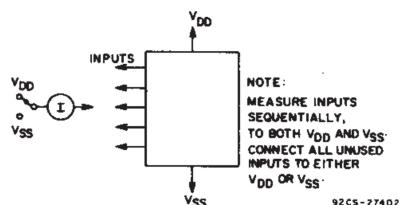


Fig. 16 — Input current test circuit.

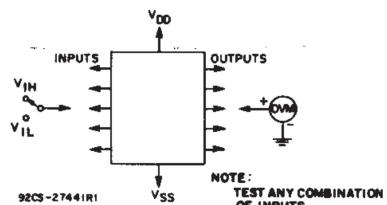
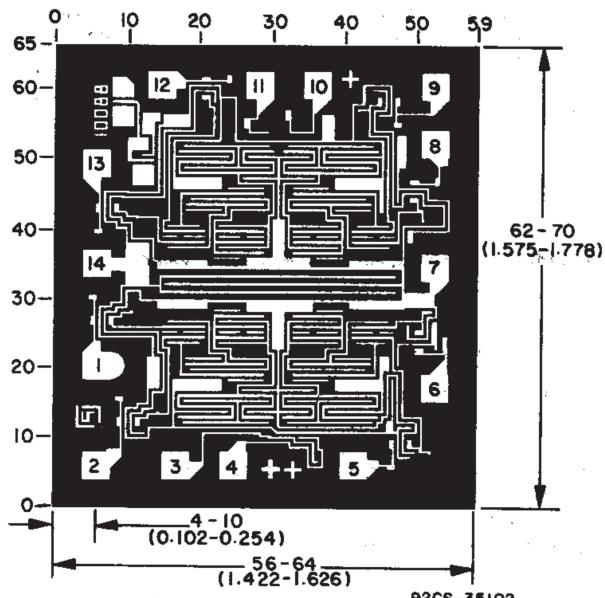
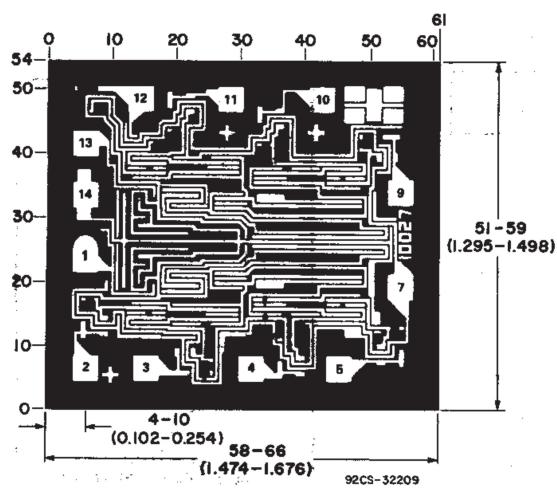


Fig. 17 — Input-voltage test circuit.

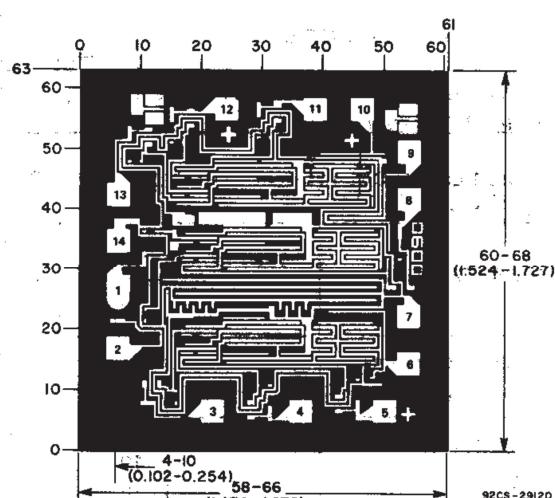
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



Chip dimensions and pad layout for CD4071B.



Chip dimensions and pad layout for CD4072B.



Chip dimensions and pad layout for CD4075B.