

# CD4060B Types

## CMOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

### High-Voltage Types (20-Volt Rating)

■ CD4060B consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of  $\phi_1$  (and  $\phi_0$ ). All inputs and outputs are fully buffered. Schmitt trigger action on the input-pulse line permits unlimited input-pulse rise and fall times.

The CD4060B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

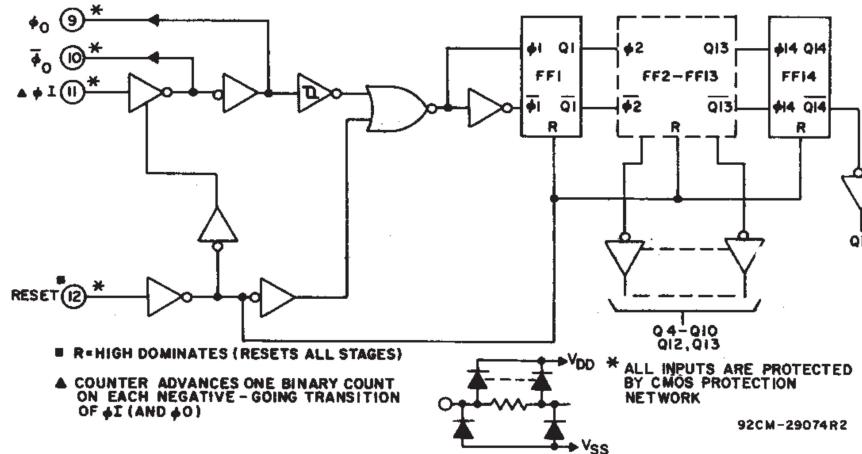


Fig. 1 – Logic diagram.

### MAXIMUM RATINGS; Absolute-Maximum Values:

#### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to  $V_{DD}$  +0.5V

DC INPUT CURRENT, ANY ONE INPUT .....  $\pm 10\text{mA}$

#### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearity at 12mW/ $^\circ\text{C}$  to 200mW

#### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  ..... 100mW

OPERATING-TEMPERATURE RANGE ( $T_A$ ) ..... -55 $^\circ\text{C}$  to +125 $^\circ\text{C}$

STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) ..... -65 $^\circ\text{C}$  to +150 $^\circ\text{C}$

#### LEAD TEMPERATURE (DURING SOLDERING):

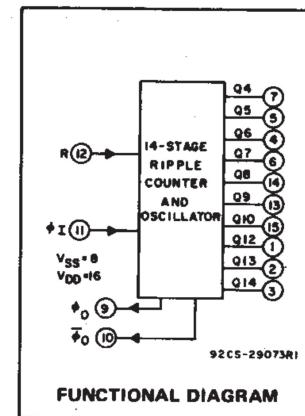
At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79\text{mm}$ ) from case for 10s max ..... +265 $^\circ\text{C}$

### Features:

- 12 MHz clock rate at 15 V
- Common reset
- Fully static operation
- Buffered inputs and outputs
- Schmitt trigger input-pulse line
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for description of "B" Series CMOS Devices"

### Oscillator Features:

- All active components on chip
- RC or crystal oscillator configuration
- RC oscillator frequency of 690 kHz min. at 15 V



### Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

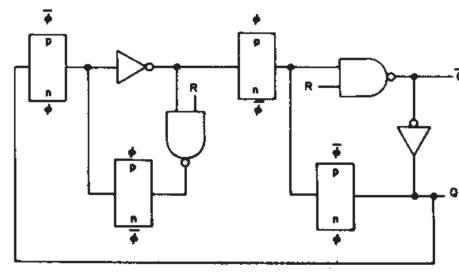


Fig. 2 – Detail of typical flip-flop stage.

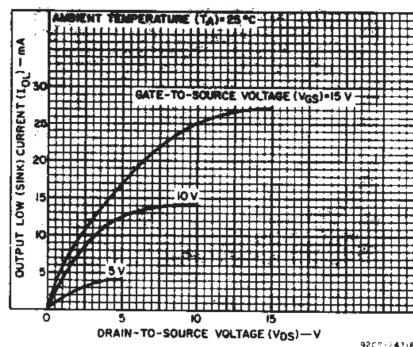


Fig. 3 – Typical n-channel output low (sink) current characteristics.

## STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS		
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	-55	-40	+85	+125	+25				
				Min.	Typ.	Max.						
Quiescent Device Current, $I_{DD}$ Max.	-	0,5	5	5	5	150	150	-	0,04	5	μA	
	-	0,10	10	10	10	300	300	-	0,04	10		
	-	0,15	15	20	20	600	600	-	0,04	20		
	-	0,20	20	100	100	3000	3000	-	0,08	100		
Output Low (Sink) Current*, $I_{OL}$ Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA	
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-		
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-		
Output High (Source) Current*, $I_{OH}$ Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA	
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-		
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-		
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-		
Output Voltage: Low-Level, $V_{OL}$ Max.	-	0,5	5	0,05			-	0	0,05	-	V	
	-	0,10	10	0,05			-	0	0,05	-		
	-	0,15	15	0,05			-	0	0,05	-		
Output Voltage: High-Level, $V_{OH}$ Min.	-	0,5	5	4,95			4,95	5	-	-	V	
	-	0,10	10	9,95			9,95	10	-	-		
	-	0,15	15	14,95			14,95	15	-	-		
Input Low Voltage $V_{IL}$ Max.	0,5,4,5	-	5	1,5			-	-	1,5	-	V	
	1,9	-	10	3			-	-	3	-		
	1,5,13,5	-	15	4			-	-	4	-		
Input High Voltage, $V_{IH}$ Min.	0,5,4,5	-	5	3,5			3,5	-	-	-	V	
	1,9	-	10	7			7	-	-	-		
	1,5,13,5	-	15	11			11	-	-	-		
Input Current $I_{IN}$ Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 <sup>-5</sup>	±0,1	μA	

\* Data not applicable to terminal 9 or 10.

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	$V_{DD}$	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For $T_A = 25^\circ C$ )	-	3	18	V
Input-Pulse Width, $t_W$ ( $f = 100$ kHz)	5	100	-	ns
	10	40	-	
	15	30	-	
Input-Pulse Rise Time and Fall Time, $t_{r\phi}, t_{f\phi}$	5	10	Unlimited	
	10	-		
	15	-		
Input-Pulse Frequency, $f_{\phi}$ (External pulse source)	5	-	3,5	MHz
	10	-	8	
	15	-	12	
Reset Pulse Width, $t_W$	5	120	-	ns
	10	60	-	
	15	40	-	

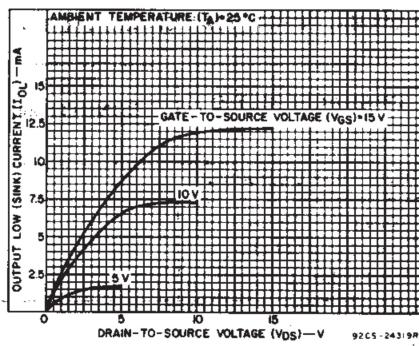


Fig. 4 – Minimum n-channel output low (sink) current characteristics.

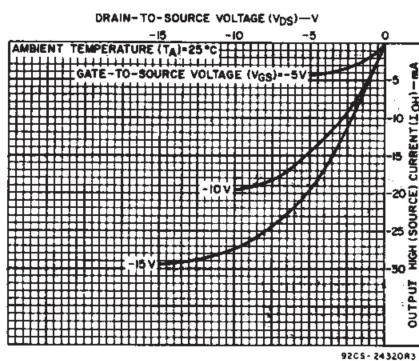


Fig. 5 – Typical p-channel output high (source) current characteristics.

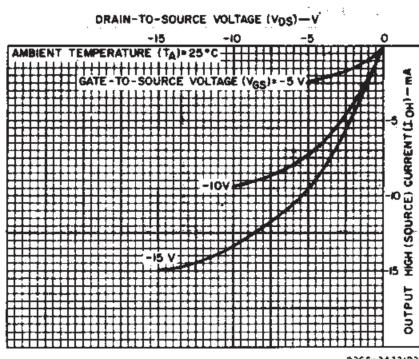
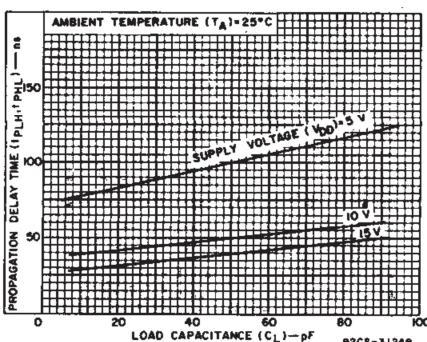


Fig. 6 – Minimum p-channel output high (source) current characteristics.

Fig. 7 – Typical propagation delay time ( $t_{PHL}$  to  $t_{PHL'}$ ) as a function of load capacitance.

## CD4060B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20 \text{ ns}$ ,  
 $C_L = 50 \text{ pF}$ ,  $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V <sub>DD</sub> (V)	MIN.	TYP.	
<b>Input-Pulse Operation</b>					
Propagation Delay Time, $\phi_I$ to Q4 Out; $t_{PHL}, t_{PLH}$		5	—	370	740
		10	—	150	300
		15	—	100	200
Propagation Delay Time, Q <sub>n</sub> to Q <sub>n+1</sub> ; $t_{PHL}, t_{PLH}$		5	—	100	200
		10	—	50	100
		15	—	40	80
Transition Time, $t_{THL}, t_{TLH}$		5	—	100	200
		10	—	50	100
		15	—	40	80
Min. Input-Pulse Width, $t_W$	f = 100 kHz	5	—	50	100
		10	—	20	40
		15	—	15	30
Input-Pulse Rise & Fall Time, $t_{r\phi}, t_{f\phi}$		5	Unlimited		
		10	Unlimited		
		15	Unlimited		
Max. Input-Pulse Frequency, $f_{\phi I}$ (External pulse source)		5	3.5	7	—
		10	8	16	—
		15	12	24	—
Input Capacitance, $C_1$	Any Input	—	5	7.5	pF
<b>Reset Operation</b>					
Propagation Delay Time, $t_{PHL}$		5	—	180	360
		10	—	80	160
		15	—	50	100
Minimum Reset Pulse Width, $t_W$		5	—	60	120
		10	—	30	60
		15	—	20	40

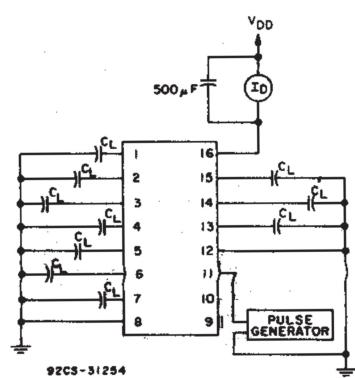
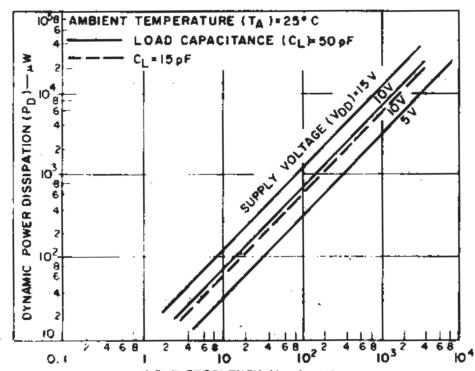
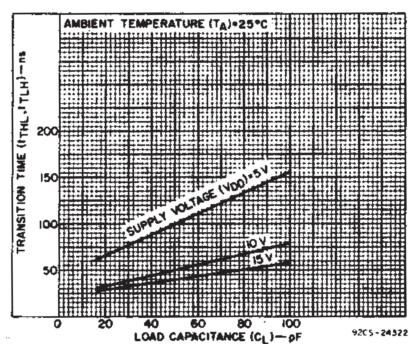
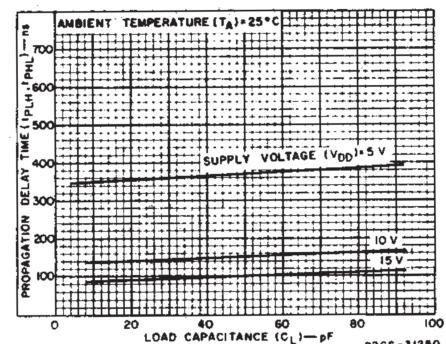


Fig. 11 – Dynamic power dissipation test circuit.

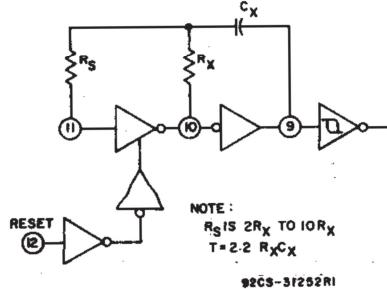


Fig. 12 – Typical RC circuit.

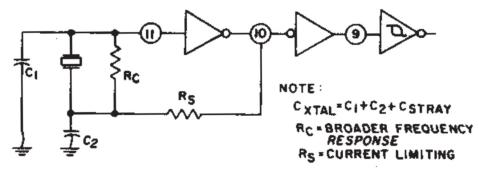


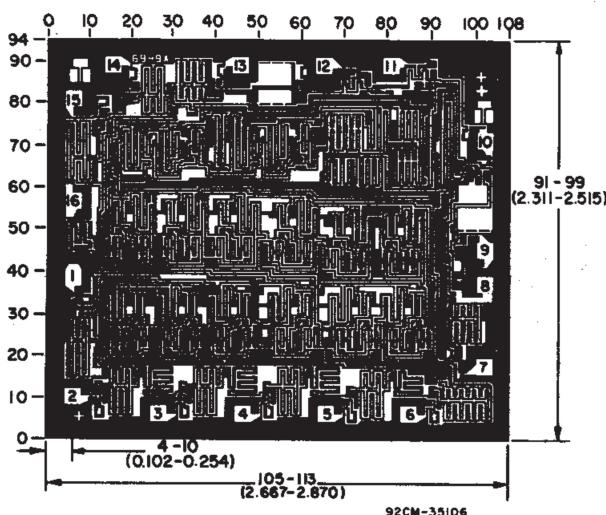
Fig. 13 – Typical crystal circuit.

## CD4060B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20 \text{ ns}$ ,  
 $C_L = 50 \text{ pF}, R_L = 200 \text{ k}\Omega$  [cont'd]**

CHARACTERISTIC	TEST CONDITIONS	$V_{DD}$ (V)	LIMITS			UNITS
			Min.	Typ.	Max.	
<b>RC Operation</b>						
Variation of Frequency (Unit-to-Unit)	$C_X = 200 \text{ pF}$ , $R_S = 560 \text{ k}\Omega$ , $R_X = 50 \text{ k}\Omega$	5	—	$23 \pm 10\%$	—	kHz
		10	—	$24 \pm 10\%$	—	
		15	—	$25 \pm 10\%$	—	
Variation of Frequency with voltage change (Same Unit)	$C_X = 200 \text{ pF}$ , $R_S = 560 \text{ k}\Omega$ , $R_X = 50 \text{ k}\Omega$	5V to 10 V 10V to 15V	—	1.5 0.5	—	
$R_X$ max.	$C_X = 10 \mu\text{F}$	5	—	—	20	$\text{M}\Omega$
	= 50 $\mu\text{F}$	10	—	—	20	
	= 10 $\mu\text{F}$	15	—	—	10	
$C_X$ max.	$R_X = 500 \text{ k}\Omega$	5	—	—	1000	$\mu\text{F}$
	= 300 $\text{k}\Omega$	10	—	—	50	
	= 300 $\text{k}\Omega$	15	—	—	50	
Maximum Oscillator Frequency*	$R_X = 5 \text{ k}\Omega$ $R_S = 30 \text{ k}\Omega$ $C_X = 15 \text{ pF}$	10	530	650	810	kHz
		15	690	800	940	
Drive Current at Pin 9 (For Oscillator Design)	$I_{OL}$	$V_O = 0.4 \text{ V}$	5	0.16	0.36	mA
		= 0.5 V	10	0.42	0.8	
		= 1.5 V	15	1	2	
	$I_{OH}$	$V_O = 4.6 \text{ V}$	5	-0.16	-0.35	mA
		= 9.5 V	10	-0.42	-0.8	
		= 13.5 V	15	-1	-2	

\*RC oscillator applications are not recommended at supply voltages below 7 V for  $R_X < 50 \text{ k}\Omega$ .



Chip dimensions and pad layout for CD4060B

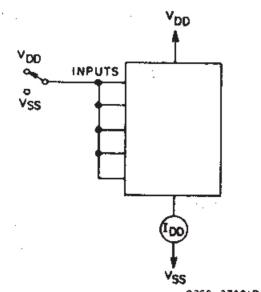


Fig. 14 – Quiescent device current.

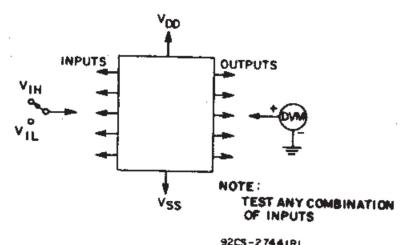


Fig. 15 – Input voltage.

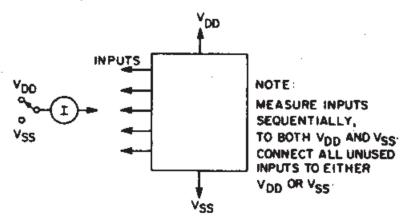
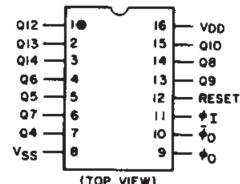


Fig. 16 – Input current.

### TERMINAL DIAGRAM



92CS-23761R2

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).