

# CD4073B, CD4081B, CD4082B Types

## CMOS AND Gates

### High-Voltage Types (20-Volt Rating)

**CD4073B Triple 3-Input AND Gate**

**CD4081B Quad 2-Input AND Gate**

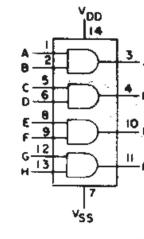
**CD4082B Dual 4-Input AND Gate**

■ CD4073B, CD4081B and CD4082B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates.

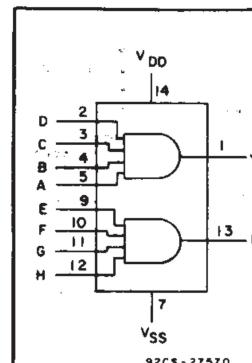
The CD4073B, CD4081B, and CD4082B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

- Medium-Speed Operation —  $t_{PLH}$ ,  $t_{PHL} = 60$  ns (typ.) at  $V_{DD} = 10$  V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



**CD4081B  
FUNCTIONAL DIAGRAM**



**CD4082B  
FUNCTIONAL DIAGRAM**

### MAXIMUM RATINGS, Absolute-Maximum Values:

#### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal ..... -0.5V to +20V

#### INPUT VOLTAGE RANGE, ALL INPUTS

-0.5V to  $V_{DD}$  +0.5V

#### DC INPUT CURRENT, ANY ONE INPUT

±10mA

#### POWER DISSIPATION PER PACKAGE (PD):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearity at 12mW/ $^\circ\text{C}$  to 200mW

#### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$  (All Package Types) ..... 100mW

#### OPERATING-TEMPERATURE RANGE ( $T_A$ )

-55°C to  $+125^\circ\text{C}$

#### STORAGE TEMPERATURE RANGE ( $T_{stg}$ )

-65°C to  $+150^\circ\text{C}$

#### LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch (1.59 ± 0.79mm) from case for 10s max .....  $+265^\circ\text{C}$

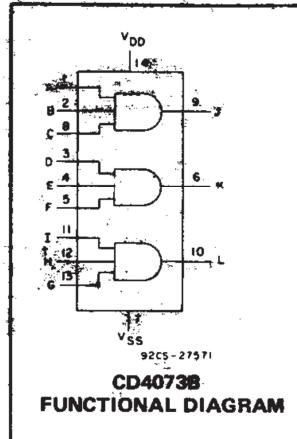
### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A = \text{Full Package Temperature Range}$ )	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20$  ns, and  $C_L = 50$  pF,  $R_L = 200$  k $\Omega$

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS			UNITS
		$V_{DD}$ Volts	TYP.	MAX.	
Propagation Delay Time, $t_{PHL}, t_{PLH}$		5	125	250	ns
		10	60	120	
		15	45	90	
Transition Time, $t_{THL}, t_{TLH}$		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, $C_{IN}$	Any Input	—	5	7.5	pF



**CD4073B  
FUNCTIONAL DIAGRAM**

# CD4073B, CD4081B, CD4082B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS	
	VO (V)	VIN (V)	VDD (V)	+25							
				-55	-40	+85	+125	Min.	Typ.		
Quiescent Device Current, I <sub>DD</sub> Max.	-	0,5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	
	-	0,10	10	0.5	0.5	15	15	-	0.01	0.5	
	-	0,15	15	1	1	30	30	-	0.01	1	
	-	0,20	20	5	5	150	150	-	0.02	5	
Output Low (Sink) Current I <sub>OL</sub> Min.	0,4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	
	0,5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1,5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current I <sub>OH</sub> Min.	4,6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2,5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9,5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13,5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, VOL Max.	-	0,5	5	0.05			-	0	0.05	-	
	-	0,10	10	0.05			-	0	0.05	-	
	-	0,15	15	0.05			-	0	0.05	-	
Output Voltage: High-Level, VOH Min.	-	0,5	5	4.95			4.95	5	-	-	
	-	0,10	10	9.95			9.95	10	-	-	
	-	0,15	15	14.95			14.95	15	-	-	
Input Low Voltage, VI <sub>L</sub> Max.	0,5	-	5	1.5			-	-	1.5	-	
	1	-	10	3			-	-	3	-	
	1,5	-	15	4			-	-	4	-	
Input High Voltage, VI <sub>H</sub> Min.	0,5,4,5	-	5	3.5			3.5	-	-	-	
	1,9	-	10	7			7	-	-	-	
	1,5,13,5	-	15	11			11	-	-	-	
Input Current I <sub>IN</sub> Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 <sup>-5</sup>	±0,1	
										μA	

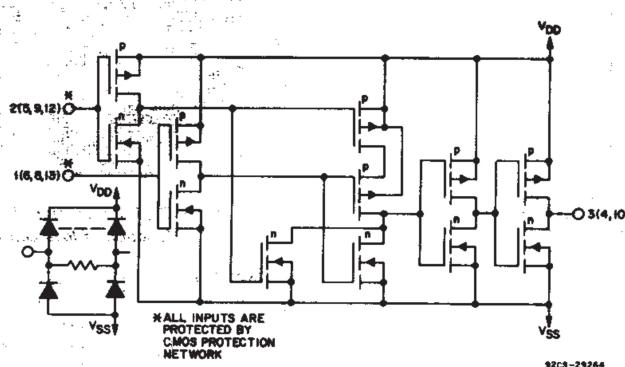


Fig. 1 – Schematic diagram for CD4081B (1 of 4 identical gates).

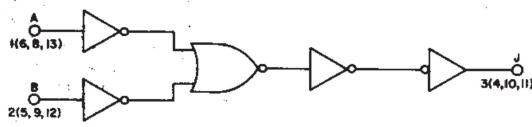


Fig. 2 – Logic diagram for CD4081B (1 of 4 identical gates).

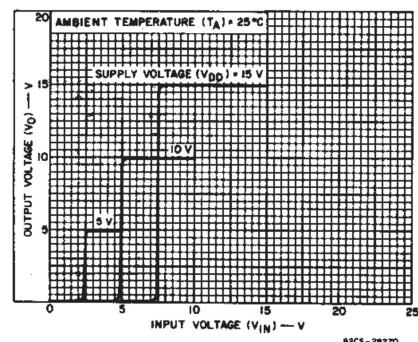


Fig. 3 – Typical voltage transfer characteristics.

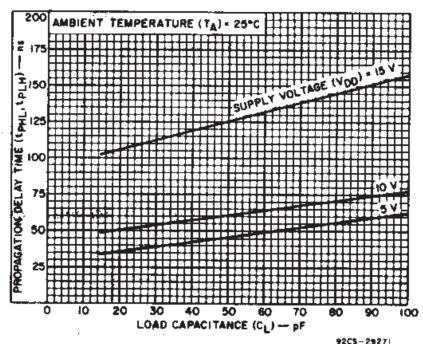


Fig. 4 – Typical propagation delay time as a function of load capacitance.

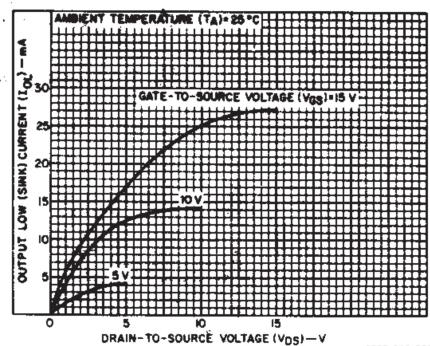


Fig. 5 – Typical output low (sink) current characteristics.

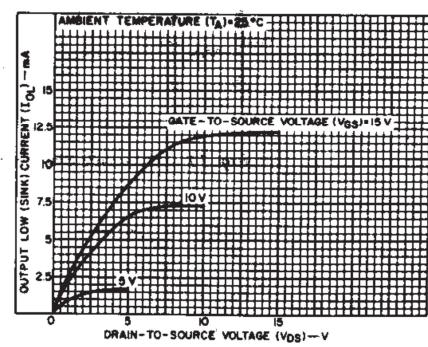


Fig. 6 – Minimum output low (sink) current characteristics.

## CD4073B, CD4081B, CD4082B Types

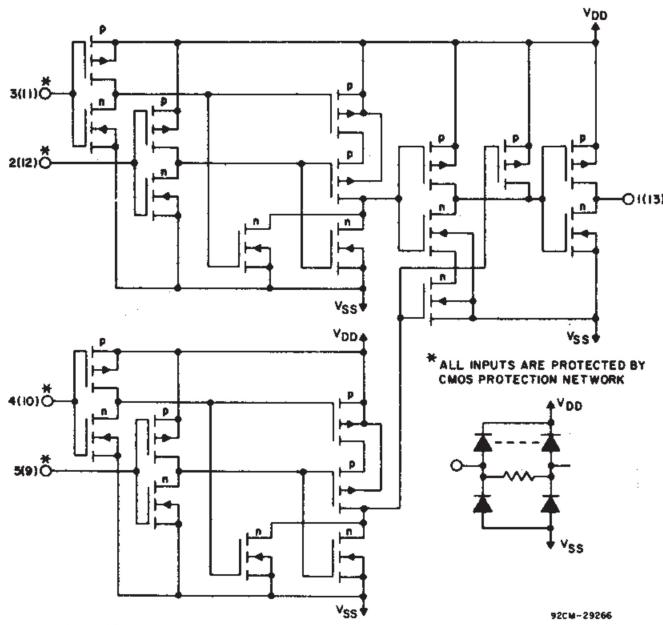


Fig. 7 — Schematic diagram for CD4082B (1 of 2 identical gates).

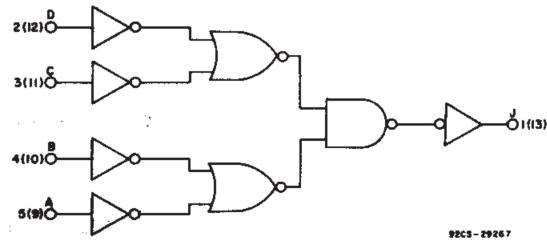


Fig. 9 — Logic diagram for CD4082B (1 of 2 identical gates).

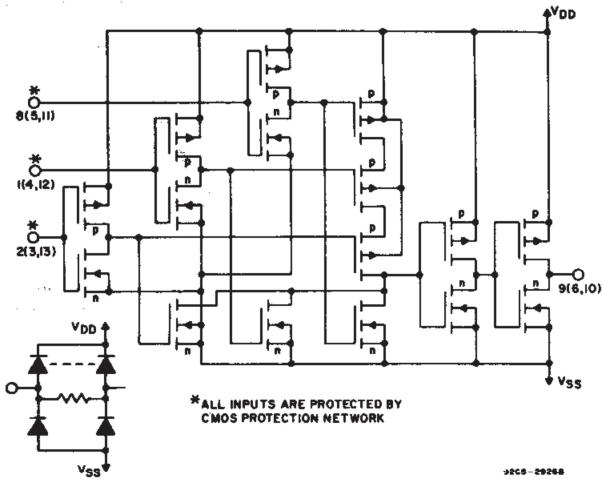


Fig. 11 — Schematic diagram for CD4073B (1 of 3 identical gates).

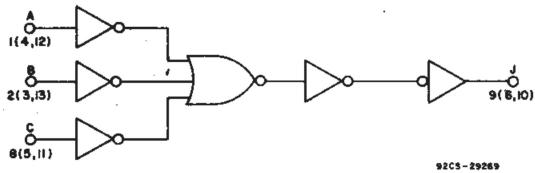


Fig. 13 — Logic diagram for CD4073B (1 of 3 identical gates).

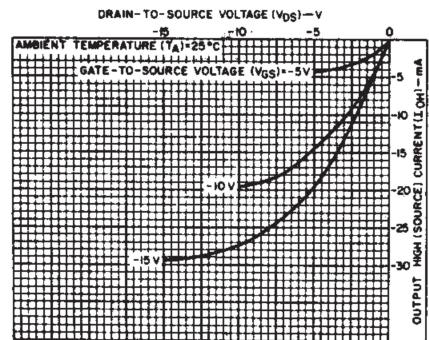


Fig. 8 — Typical output high (source) current characteristics.

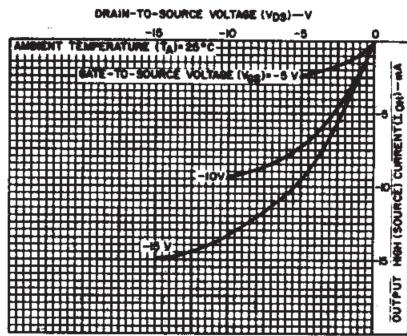


Fig. 10 — Minimum output high (source) current characteristics.

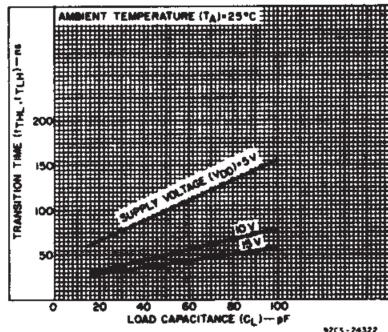


Fig. 12 — Typical transition time as a function of load capacitance.

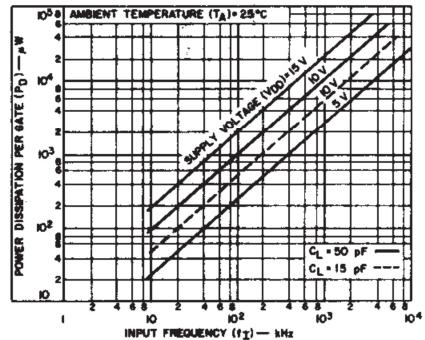


Fig. 14 — Typical dynamic power dissipation per gate as a function of frequency.

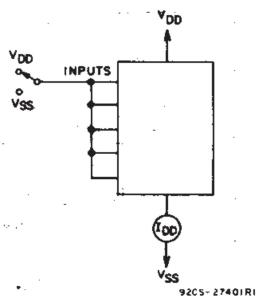
**CD4073B, CD4081B, CD4082B Types**

Fig. 15 — Quiescent device current test circuit.

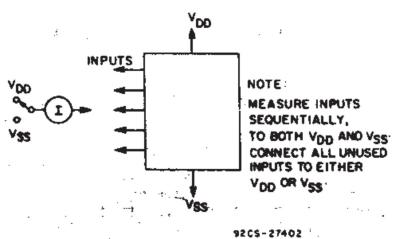


Fig. 16 — Input current test circuit.

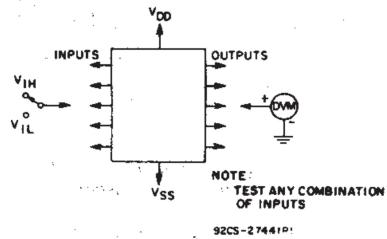


Fig. 17 — Input-voltage test circuit.

**TERMINAL ASSIGNMENTS**

A	1 e	14	V <sub>DD</sub>
B	2	13	H
J=A-B	3	12	G
K=C-D	4	11	M-G-H
C	5	10	L-E-F
D	6	9	F
V <sub>SS</sub>	7	8	E

TOP VIEW

92CS-24536

**CD4081B**

J=A-B-C-D	1 e	14	V <sub>DD</sub>
D	2	13	K=E-F-G-H
C	3	12	H
B	4	11	G
A	5	10	F
NC	6	9	E
V <sub>SS</sub>	7	8	NC

TOP VIEW

NC=NO CONNECTION

92CS-24537Z

**CD4082B**

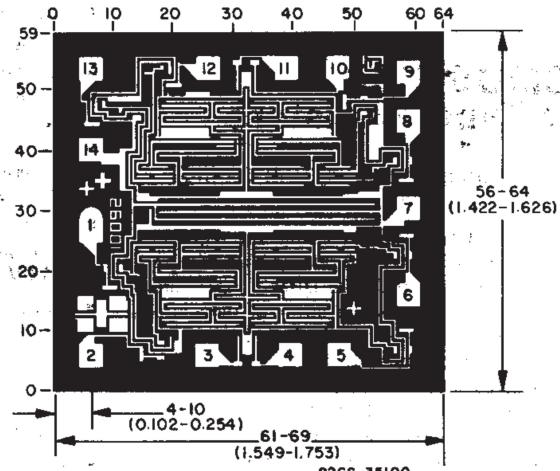
A	1 e	14	V <sub>DD</sub>
B	2	13	G
D	3	12	H
E	4	11	I
F	5	10	L=G-H-I
K=D-E-F	6	9	J=A-B-C
V <sub>SS</sub>	7	8	C

TOP VIEW

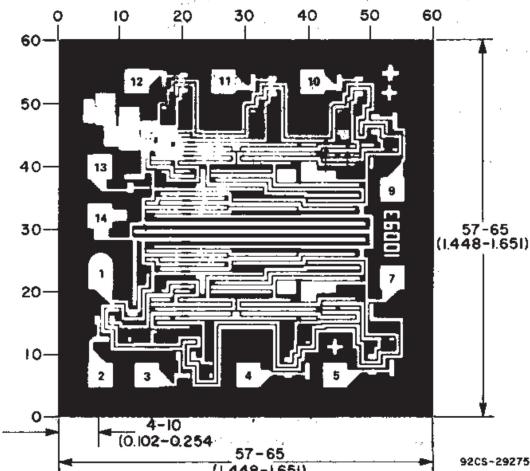
92CS-24538

**CD4073B**

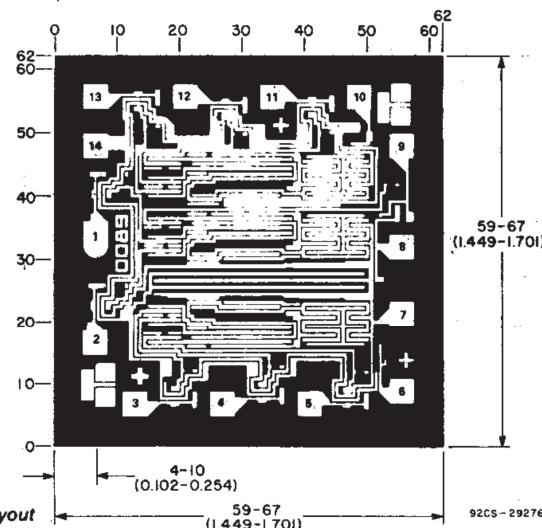
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).



Chip dimensions and pad layout for CD4081B.



Chip dimensions and pad layout for CD4082B.



Chip dimensions and pad layout for CD4073B.