

**SN54121, SN74121
MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS**

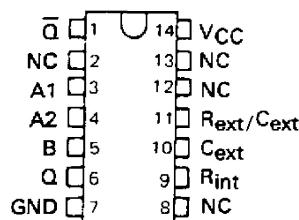
SDLS042A - MAY 1983 - REVISED MAY 2005

- Programmable Output Pulse Width
With $R_{int} \dots 35 \text{ ns Typ}$
With $R_{ext}/C_{ext} \dots 40 \text{ ns to } 28 \text{ Seconds}$
- Internal Compensation for Virtual Temperature Independence
- Jitter-Free Operation up to 90% Duty Cycle
- Inhibit Capability

SN54121 . . . J OR W PACKAGE

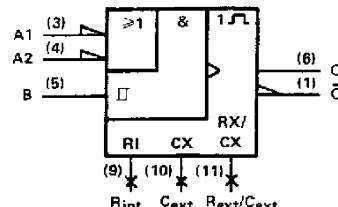
SN74121 . . . N PACKAGE

(TOP VIEW)



NC - No internal connection.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

For explanation of function table symbols, see page

† These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been setup long enough to complete any pulse started before the setup.

description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μ F) and more than one decade of timing resistance (2 k Ω to 30 k Ω for the SN54121 and 2 k Ω to 40 k Ω for the SN74121). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_{ext}R_{T}In2 = 0.7 C_{ext}R_{T}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μ F and timing resistance as low as 1.4 k Ω may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

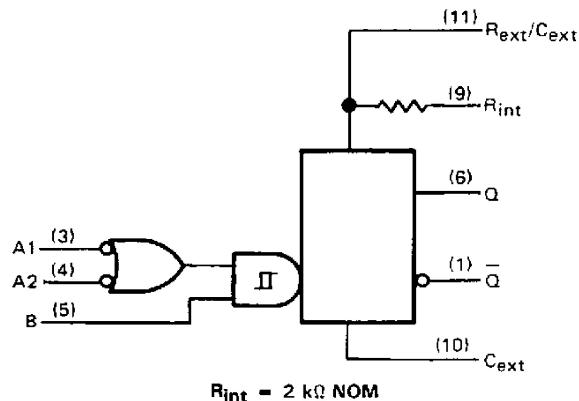
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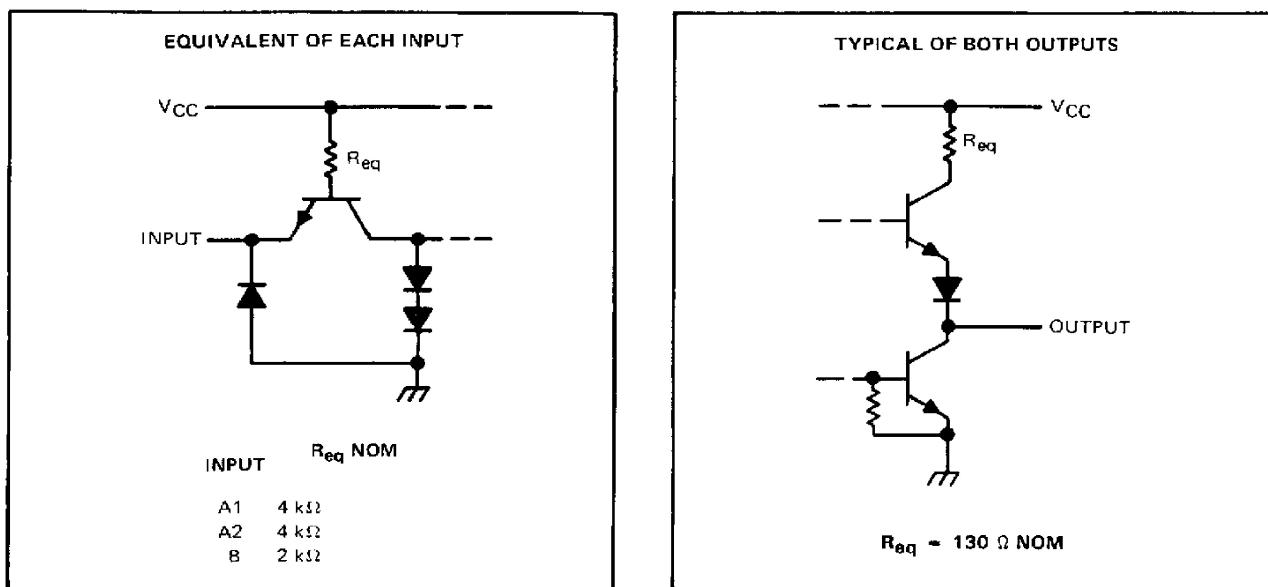
logic diagram (positive logic)



Pin numbers shown on logic notation are for J or N packages.

- NOTES: 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext} .
 2. To use the internal timing resistor, connect R_{int} to V_{CC} . For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 3: Voltage values are with respect to network ground terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		54 Family	4.5	5	5.5
			74 Family	4.75	5	5.25
I _{OH}	High-level output current				-0.4	mA
I _{OL}	Low-level output current				16	mA
dv/dt	Rate of rise or fall of input pulse	Schmitt input, B		1		V/s
		Logic inputs, A1, A2		1		V/ μ s
t _{w(in)}	Input pulse width			50		ns
R _{ext}	External timing capacitance		54 Family	1.4	30	k Ω
			74 Family	1.4	40	
C _{ext}	External timing capacitance			0	1000	μ F
Duty cycle		R _T = 2 k Ω			67	%
		R _T = MAX R _{ext}			90	
T _A	Operating free-air temperature		54 Family	-55	125	°C
			74 Family	0	70	

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH} High-level input voltage at A input	$V_{CC} = \text{MIN}$	2			V
V_{IL} Low-level input voltage at A input	$V_{CC} = \text{MIN}$			0.8	V
V_{T+} Positive-going threshold voltage at B input	$V_{CC} = \text{MIN}$		1.55	2	V
V_{T-} Negative-going threshold voltage at B input	$V_{CC} = \text{MIN}$	0.8	1.35		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
I_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = \text{MAX}$	0.2	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$		1		mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$	A1 or A2 B	40 80		μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	A1 or A2 B		-1.6 -3.2	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	54 Family 74 Family	-20 -18	-55 -55	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$	Quiescent Triggered	13 23	25 40	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[§]Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} Propagation delay time, low-to-high-level Q output from either A input		45	70		ns	
t_{PLH} Propagation delay time, low-to-high-level Q output from B input		35	55		ns	
t_{PHL} Propagation delay time, high-to-low-level \bar{Q} output from either A input		50	80		ns	
t_{PHL} Propagation delay time, high-to-low-level \bar{Q} output from B input		40	65		ns	
$t_{w(out)}$ Pulse width obtained using internal timing resistor	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Note 4	$C_{ext} = 80 \text{ pF}$, $R_{int} \text{ to } V_{CC}$	70	110	150	ns
$t_{w(out)}$ Pulse width obtained with zero timing capacitance		$C_{ext} = 0$, $R_{int} \text{ to } V_{CC}$		30	50	ns
$t_{w(out)}$ Pulse width obtained using external timing resistor		$C_{ext} = 100 \text{ pF}$, $R_T = 10 \text{ k}\Omega$	600	700	800	ns
		$C_{ext} = 1 \mu\text{F}$, $R_T = 10 \text{ k}\Omega$	6	7	8	ms

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.


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TYPICAL CHARACTERISTICS†

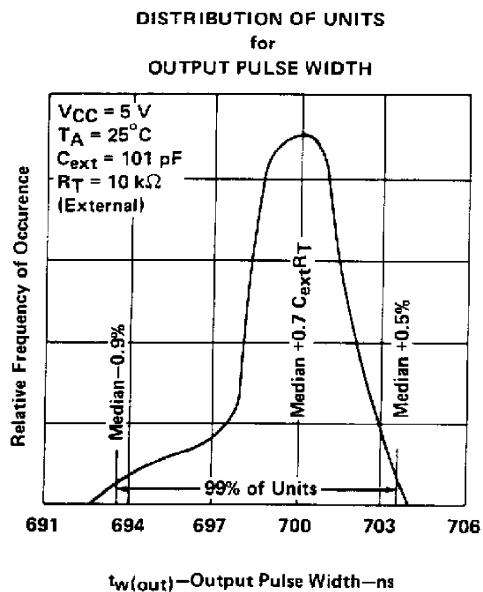


FIGURE 1

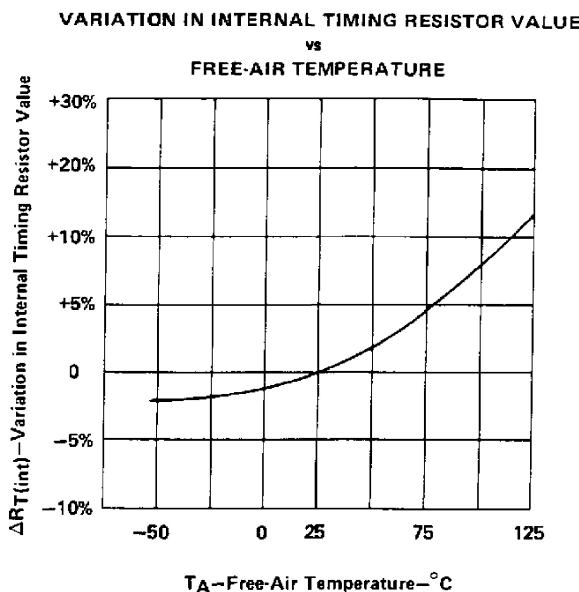


FIGURE 2

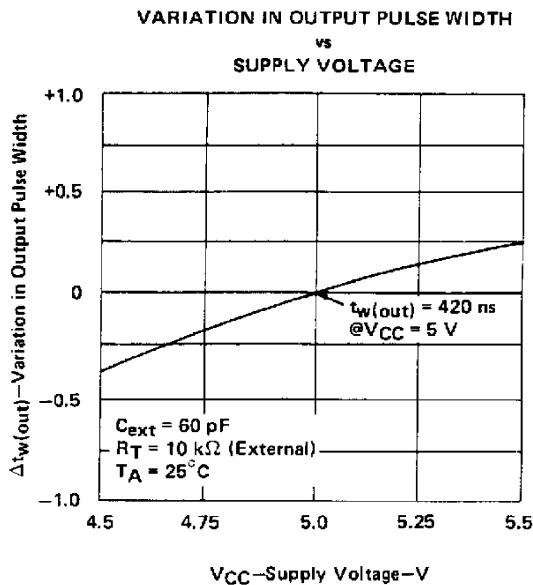


FIGURE 3

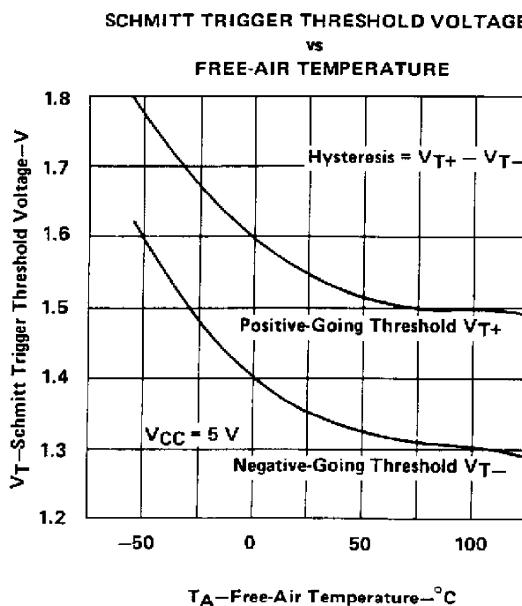


FIGURE 4

†Data for temperatures below 0°C and above 70°C are applicable for SN54121.

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TYPICAL CHARACTERISTICS[†] (continued)

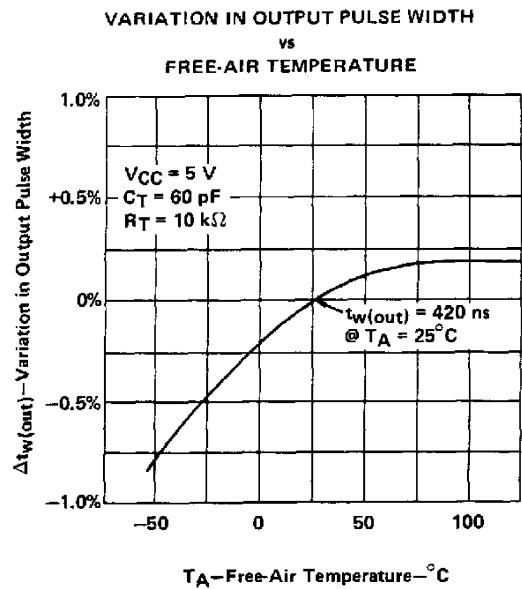


FIGURE 5

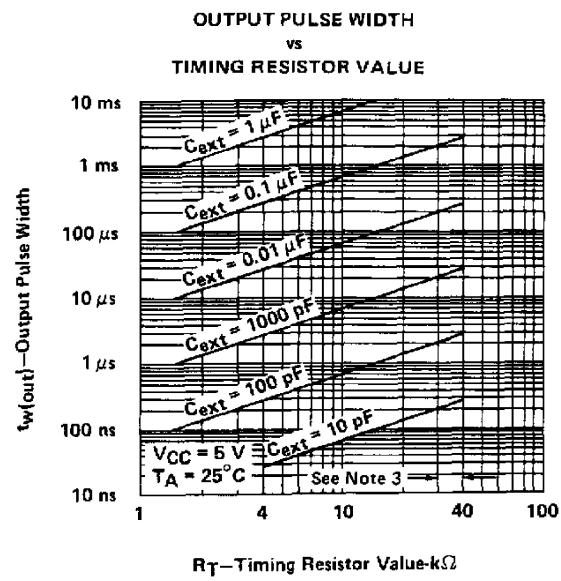


FIGURE 6

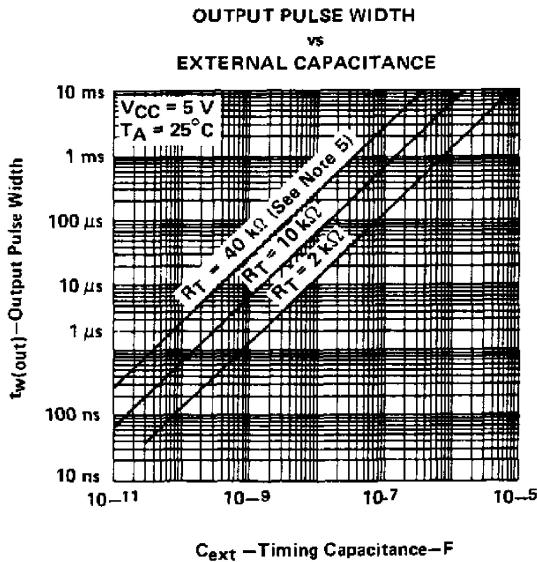


FIGURE 7

NOTE 5: These values of resistance exceed the maximum recommended use over the full temperature range of the SN54121.
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