

# DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

The SN54/74LS155 and SN54/74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS155 and LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all Motorola TTL families.

- · Schottky Process for High Speed
- · Multifunction Capability
- Common Address Inputs
- True or Complement Data Demultiplexing
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

#### **CONNECTION DIAGRAM DIP (TOP VIEW)** $\mathsf{E}_\mathsf{b}$ $O_{3b}$ $O_{2b}$ $O_{1b}$ **VCC** 16 15 14 13 11 10 9 12 NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package. 2 6 1 3 8 $o_{3a}$ $o_{2a}$ 0<sub>1a</sub> $0_{0a}$

#### **PIN NAMES** LOADING (Note a) HIGH LOW <u>A</u><sub>0</sub>, <u>A</u><sub>1</sub> Address Inputs 0.5 U.L. 0.25 U.L. Enable (Active LOW) Inputs Ea, Eb 0.5 U.L. 0.25 U.L. <u>E</u>a \_ Enable (Active HIGH) Input 0.5 U.L. 0.25 U.L. $O_0 - O_3$ Active LOW Outputs (Note b) 10 U.L. 5 (2.5) U.L.

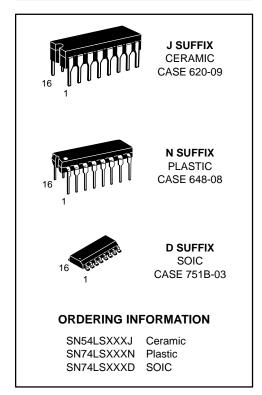
### NOTES:

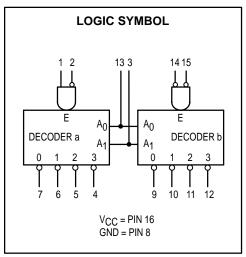
- a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.
- b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The HIGH level drive for the LS156 must be established by an external resistor.

# SN54/74LS155 SN54/74LS156

# DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

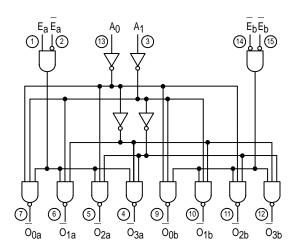
LS156-OPEN-COLLECTOR LOW POWER SCHOTTKY





# SN54/74LS155 • SN54/74LS156

#### **LOGIC DIAGRAM**



V<sub>CC</sub> = PIN 16 GND = PIN 8 = PIN NUMBERS

### **FUNCTIONAL DESCRIPTION**

The LS155 and LS156 are Dual 1-of-4 Decoder/Demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs ( $A_0$ . $A_1$ ) and provides four mutually exclusive active LOW outputs ( $O_0$ - $O_3$ ). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ( $E_a \bullet E_a$ ). In demultiplexing applications, Decoder "a" can accept either true or complemented data by using the  $E_a$  or  $E_a$  inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ( $E_b \bullet E_b$ ). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying  $E_a$  to  $E_b$  and relabeling the common connection as (A2). The other  $E_b$  and  $E_a$  are connected together to form the common enable.

The LS155 and LS156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in Fig. a. The LS156 has the further advantage of being able to

AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E_+ + A_0 + A_1) \cdot (E + A_0 + A_1)$$
 where  $E = E_a + E_a$ ;  $E = E_b + E_b$ 

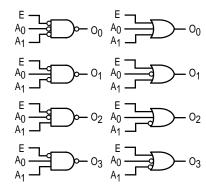


Figure a

#### **TRUTH TABLE**

ADDF	ADDRESS ENABLE "a"			OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A <sub>0</sub>	A <sub>1</sub>	Ea	Ea	00	01	02	03	E <sub>b</sub>	E <sub>b</sub>	00	01	02	03
Х	Х	L	Х	Н	Н	Н	Н	Н	Х	Н	Н	Н	Н
Х	Х	Х	Н	Н	Н	Н	Н	Х	Н	Н	Н	Н	Н
L	L	Н	L	L	Н	Н	Н	L	L	L	Н	Н	Н
Н	L	Н	L	Н	L	Н	Н	L	L	Н	L	Н	Н
L	Н	Н	L	Н	Н	L	Н	L	L	Н	Н	L	Н
Н	Н	Н	L	Н	Н	Н	L	L	L	Н	Н	Н	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

# SN54/74LS155

# **GUARANTEED OPERATING RANGES**

Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

# DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

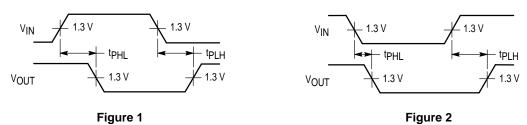
				Limits					
Symbol	Symbol Parameter		Min Typ Max			Unit	Test Conditions		
VIH	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs			
\/	Input LOW Voltage	54			0.7	V	Guaranteed Inpu	LOW Voltage for	
VIL	input LOW Voltage	74			0.8	V	All Inputs		
VIK	Input Clamp Diode Voltage	nput Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = MIN, I_{IN} = -18 \text{ mA}$		
Vou	Output HIGH Voltage	54	2.5	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub>		
VOH	Output HIGH voltage	74	2.7	3.5		V	or V <sub>IL</sub> per Truth Table		
Vo	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA	$V_{CC} = V_{CC} MIN,$ $V_{IN} = V_{II} \text{ or } V_{IH}$	
VOL	Output LOW Voltage	74		0.35	0.5	V	I <sub>OL</sub> = 8.0 mA	per Truth Table	
l					20	μΑ	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V		
¹ıн	Input HIGH Current				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V		
IIL	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V			
los	Short Circuit Current (Note 1	-20		-100	mA	V <sub>CC</sub> = MAX			
ICC	Power Supply Current				10	mA	V <sub>CC</sub> = MAX		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# AC CHARACTERISTICS $(T_A = 25^{\circ}C)$

			Limits				
Symbol	Symbol Parameter		Тур	Max	Unit	Test	Conditions
tPLH tPHL	Propagati <u>o</u> n De <u>lay</u> Address, E <sub>a</sub> or E <sub>b</sub> to Output		10 19	15 30	ns	Figure 1	
<sup>t</sup> PLH <sup>t</sup> PHL	Propagation Delay Address to Output		17 19	26 30	ns	Figure 2	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
<sup>t</sup> PLH <sup>t</sup> PHL	Propagation Delay Ea to Output		18 18	27 27	ns	Figure 1	

# **AC WAVEFORMS**



# SN54/74LS156

# **GUARANTEED OPERATING RANGES**

Symbol	Parameter		Min	Тур	Max	Unit
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
Vон	Output Voltage — High	54, 74			5.5	V
lOL	Output Current — Low	54 74			4.0 8.0	mA

# DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

				Limits					
Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs		
\/	Input I OW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for		
VIL	Input LOW Voltage	74			0.8	] <sup>v</sup>	All Inputs		
VIK	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = MIN$ , $I_{IN} = -18 \text{ mA}$		
loh	Output HIGH Current	54, 74			100	μΑ	V <sub>CC</sub> = MIN, V <sub>OH</sub> = MAX		
V	Output LOW Voltage	54, 74		0.25	0.4	٧	I <sub>OL</sub> = 4.0 mA	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>II</sub> or V <sub>IH</sub>	
VOL		74		0.35	0.5	٧	I <sub>OL</sub> = 8.0 mA	per Truth Table	
I <sub>IH</sub> Input HIGH Current					20	μΑ	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V		
					0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V		
Ι <sub>Ι</sub> L	Input LOW Current				-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V		
ICC	Power Supply Current			10	mA	V <sub>CC</sub> = MAX			

# AC CHARACTERISTICS ( $T_A = 25^{\circ}C$ )

			Limits					
Symbol	mbol Parameter		Min Typ Max		Unit	Test Conditions		
tPLH tPHL	Propagati <u>o</u> n De <u>lay</u> Address, E <sub>a</sub> or E <sub>b</sub> to Output		25 34	40 51	ns	Figure 1		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Address to Output		31 34	46 51	ns	Figure 2	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$ $R_L = 2.0 \text{ k}\Omega$	
<sup>t</sup> PLH <sup>t</sup> PHL	Propagation Delay E <sub>a</sub> to Output		32 32	48 48	ns	Figure 1		

# **AC WAVEFORMS**

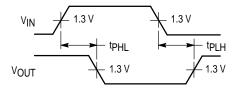


Figure 1

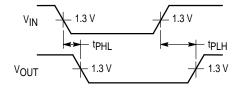


Figure 2