

CMOS Quad AND/OR Select Gate

High-Voltage Types (20-Volt Rating)

■ CD4019B types consist of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b . In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical $A + B$ function.

The CD4019B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

..... -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT

..... $\pm 10\text{mA}$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at $12\text{mW}/^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

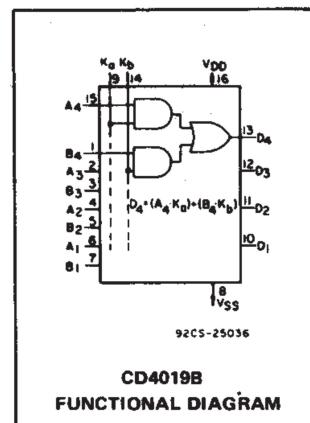
LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79\text{mm}$) from case for 10s max +265°C

Features:

- Medium-speed operation
- ... $t_{PHL} = t_{PLH} = 60\text{ ns}$ (typ.) at $C_L = 50\text{ pF}$, $V_{DD} = 10\text{ V}$
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of $1\text{ }\mu\text{A}$ at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at $V_{DD} = 5\text{ V}$
 2 V at $V_{DD} = 10\text{ V}$
 2.5 V at $V_{DD} = 15\text{ V}$

CD4019B Types

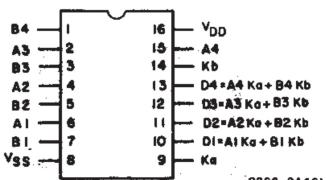


Applications:

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/Exclusive-OR selection

TERMINAL DIAGRAM

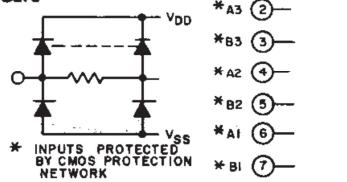
Top View



TRUTH TABLE

K_a	K_b	A_n	B_n	D_n
1	0	1	X	1
1	0	0	X	0
0	1	X	1	1
0	1	X	0	0
0	0	X	X	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

X = Don't Care



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Fig. 1—Logic diagram.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	Min.	Max.	Units
Supply-Voltage Range (For $T_A = \text{Full Package Temperature Range}$)	-	3	18	V

CD4019B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						U N I T S		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25				
				Min.	Typ.	Max.	Min.	Typ.	Max.			
Quiescent Device Current, I_{DD} Max.	-	0.5	5	1	1	30	30	-	0.02	1	μA	
	-	0.10	10	2	2	60	60	-	0.02	2		
	-	0.15	15	4	4	120	120	-	0.02	4		
	-	0.20	20	20	20	600	600	-	0.04	20		
Output Low (Sink) Current I_{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA	
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-		
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-		
Output High (Source) Current, I_{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA	
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-		
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-		
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-		
Output Voltage: Low-Level, V_{OL} Max.	-	0.5	5	0.05			-	0	0.05	-	V	
	-	0.10	10	0.05			-	-	0.05	-		
	-	0.15	15	0.05			-	0	0.05	-		
Output Voltage: High-Level, V_{OH} Min.	-	0.5	5	4.95			4.95	5	-	-	V	
	-	0.10	10	9.95			9.95	10	-	-		
	-	0.15	15	14.95			14.95	15	-	-		
Input Low Voltage, V_{IL} Max.	0.5,4.5	-	5	1.5			-	-	1.5	-	V	
	1.9	-	10	3			-	-	3	-		
	1.5,13.5	-	15	4			-	-	4	-		
Input High Voltage, V_{IH} Min.	0.5,4.5	--	5	3.5			3.5	-	-	-	V	
	1.9	-	10	7			7	-	-	-		
	1.5,13.5	-	15	11			11	-	-	-		
Input Current I_{IN} Max.	-	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1	μA	

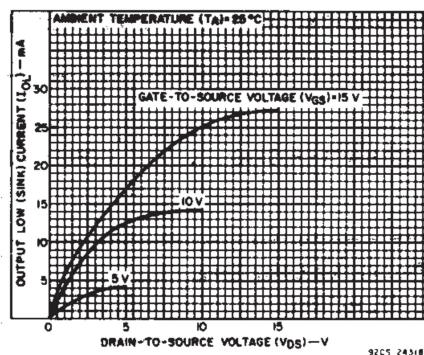


Fig. 2 – Typical output low (sink) current characteristics.

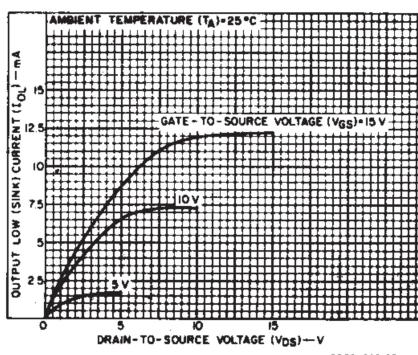


Fig. 3 – Minimum output low (sink) current characteristics.

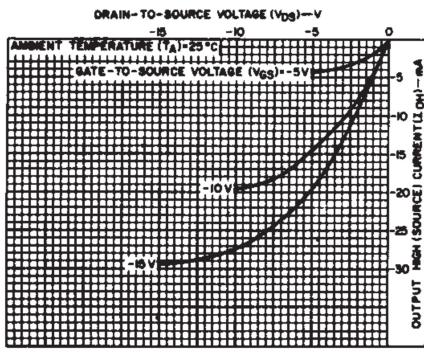


Fig. 4 – Typical output high (source) current characteristics.

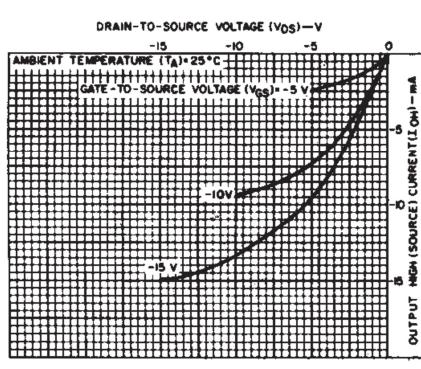


Fig. 5 – Minimum output high (source) current characteristics.

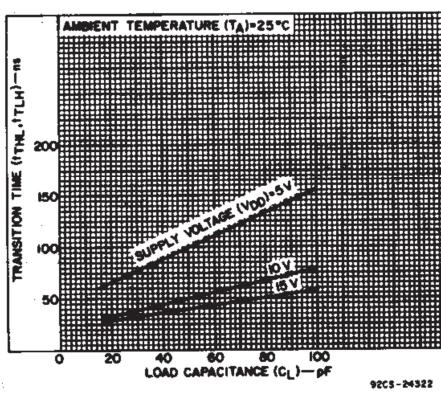


Fig. 6 – Typical transition time as a function of load capacitance.

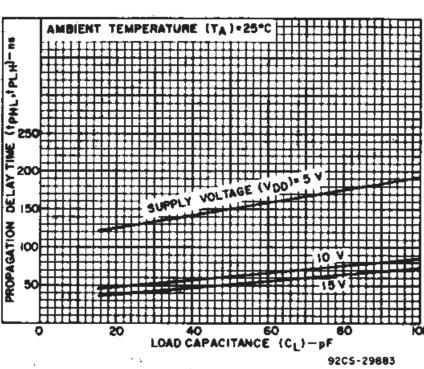


Fig. 7 – Propagation delay time as a function of load capacitance.

CD4019B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		Min.	Typ.	Max.		
Propagation Delay Time; t_{PLH}, t_{PHL}	$V_{DD} = 5, 10, 15 \text{ V}$	5	—	150	300	ns
		10	—	60	120	
		15	—	50	100	
Transition Time; t_{THL}, t_{TLH}	$V_{DD} = 5, 10, 15 \text{ V}$	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Input Capacitance, C_{IN}	All A and B Inputs	—	5	7.5	pF	
	K _a and K _b Inputs	—	10	15	pF	

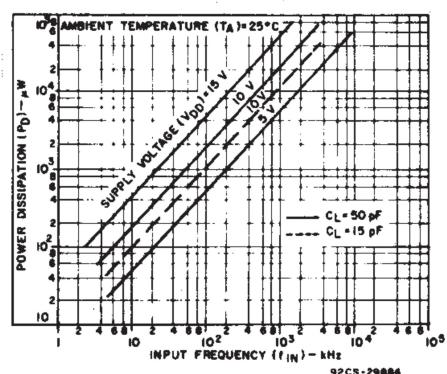


Fig. 8 – Typical dynamic power dissipation as a function of input frequency.

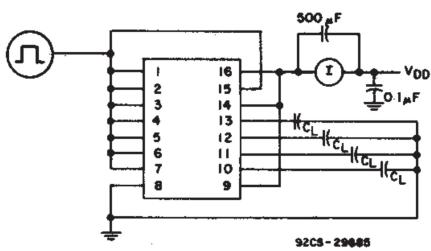


Fig. 9 – Dynamic power dissipation test circuit.

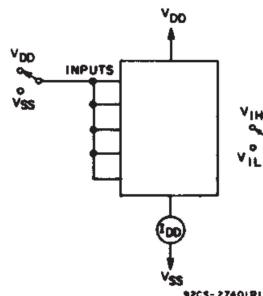


Fig. 10 – Quiescent device current test circuit.

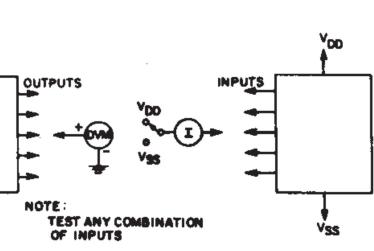


Fig. 11 – Input voltage test circuit.

NOTE:
MEASURE INPUTS
SEQUENTIALLY.
TO BOTH VDD AND VSS;
CONNECT ALL UNUSED
INPUTS TO EITHER
VDD OR VSS.

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TYPICAL APPLICATIONS

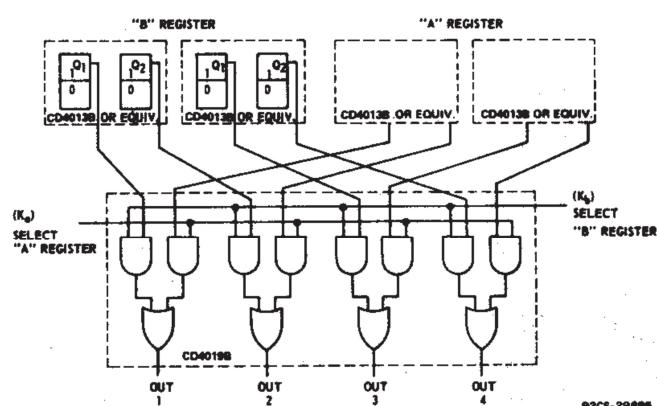


Fig. 13 – AND/OR select gating.

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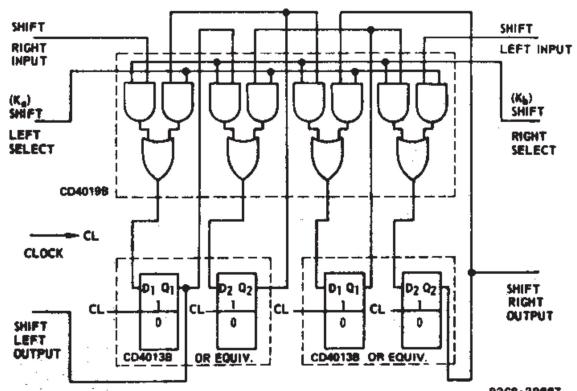


Fig. 14 – "Shift left/shift right" register.

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CD4019B Types

TYPICAL APPLICATIONS (CONT'D)

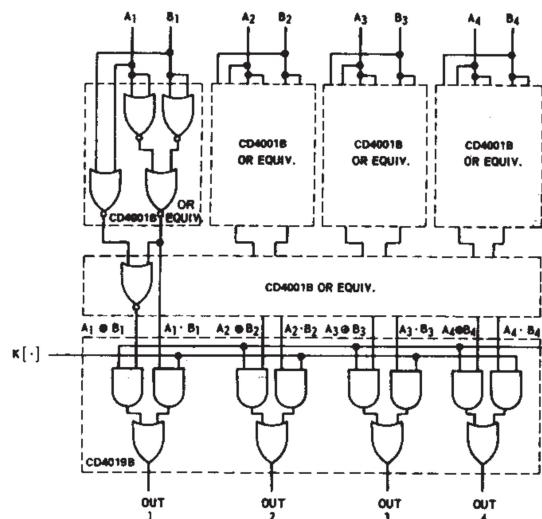


Fig. 15 – AND/OR Exclusive-OR selector.

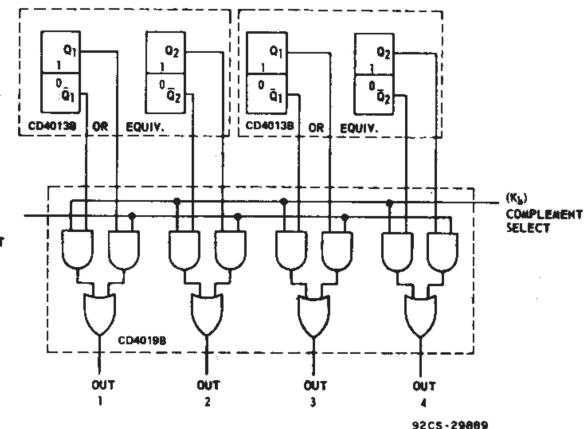
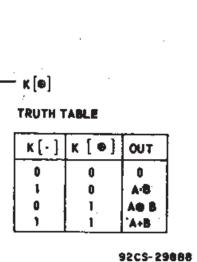
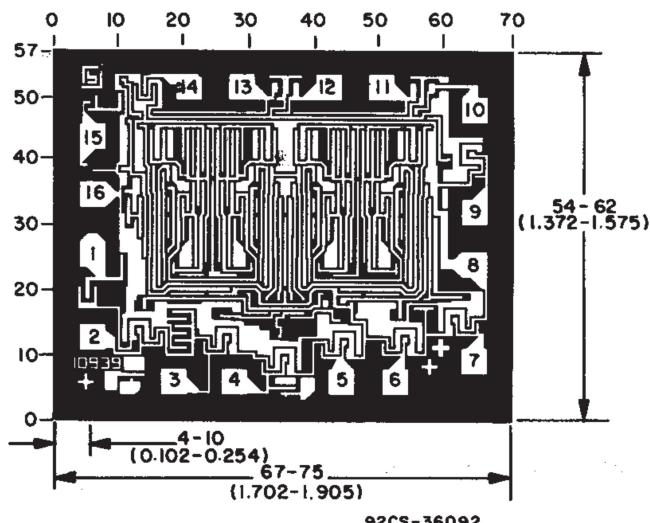


Fig. 16 – "True complement" selector.



Dimensions and pad layout for CD4019BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).