

## CMOS

### 8-Bit Addressable Latch

#### High-Voltage Types (20-Volt Rating)

■ CD4099B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

The CD4099B types are supplied in 16-lead hermetic ceramic dual-in-line packages (F3A suffix), 16-lead plastic dual-in-line packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

#### Features:

- Serial data input
- Active parallel output
- Storage register capability
- Master clear
- Can function as demultiplexer
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1  $\mu$ A at 18 V (full package-temperature range), 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at  $V_{DD} = 5$  V, 2 V at  $V_{DD} = 10$  V, 2.5 V at  $V_{DD} = 15$  V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

#### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	.....	-0.5V to +20V
Voltages referenced to $V_{SS}$ Terminal)	.....	-0.5V to $V_{DD}$ +0.5V
INPUT VOLTAGE RANGE, ALL INPUTS	.....	$\pm 10$ mA
DC INPUT CURRENT, ANY ONE INPUT	.....	±10mA
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -55^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	.....	500mW
For $T_A = +100^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	.....	Derate Linearity at 12mW/ $^{\circ}\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	.....	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	.....	-55°C to +125°C
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	.....	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) from case for 10s max	.....	+265°C

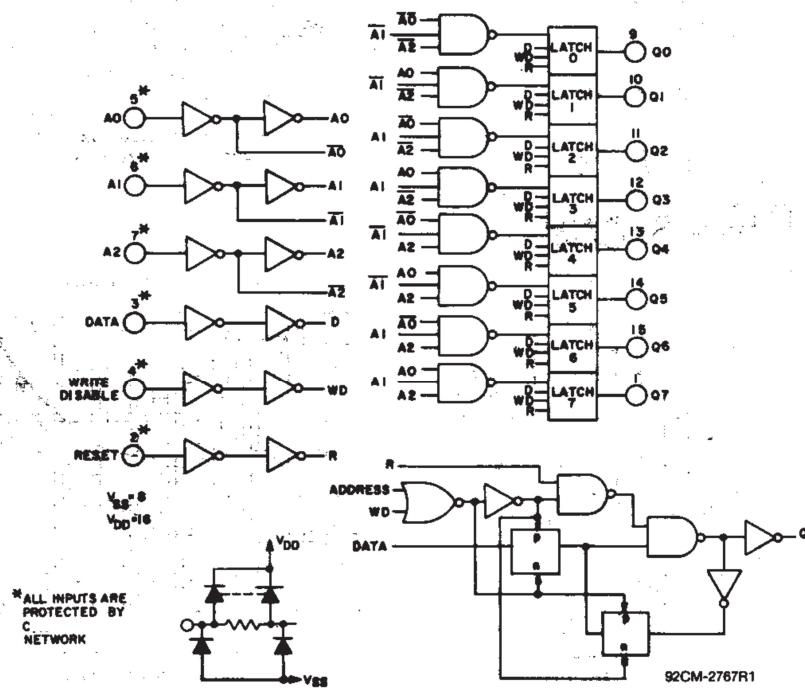
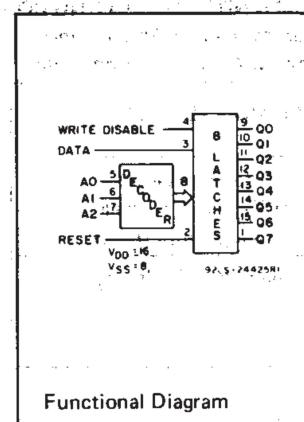


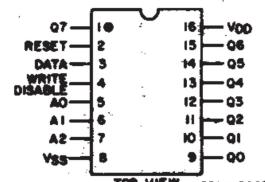
Fig. 1 — Logic diagram of CD4099B and detail of 1 of 8 latches.



Functional Diagram

#### Applications:

- Multi-line decoders
- A/D converters



TOP VIEW 92CM-24425  
TERMINAL ASSIGNMENT

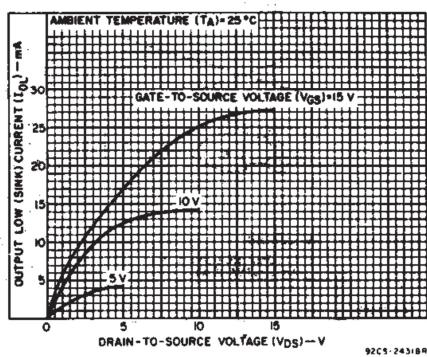


Fig. 2 — Typical output low (sink) current characteristics.

## CD4099B Types

**RECOMMENDED OPERATING CONDITIONS** at  $T_A = 25^\circ C$  (Unless otherwise specified)  
 For maximum reliability, nominal operating conditions should be selected so that operation  
 is always within the following ranges.

CHARACTERISTIC	SEE FIG. 15*	V <sub>DD</sub> (V)	LIMITS		UNITS
			MIN.	MAX.	
Supply Voltage Range: (At $T_A = 25^\circ C$ )			3	18	V
Minimum Pulse Width, $t_W$ Data	4	5	200	—	ns
		10	100	—	
		15	80	—	
Address	8	5	400	—	ns
		10	200	—	
		15	125	—	
Reset	5	5	150	—	ns
		10	75	—	
		15	50	—	
Setup Time, $t_S$ Data to WRITE DISABLE	6	5	100	—	ns
		10	50	—	
		15	35	—	
Hold Time, $t_H$ Data to WRITE DISABLE	7	5	150	—	ns
		10	75	—	
		15	50	—	

\* Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A<sub>0</sub>, A<sub>1</sub>, and A<sub>2</sub> are settling to a stable level, to prevent a wrong cell from being addressed (see Fig. 3).

MODE SELECTION			
WD	R	ADDRESSED LATCH	UNADDRESSED LATCH
0	0	Follows Data	Holds Previous State
0	1	Follows Data	Reset to "0" (Active High 8-Channel Demultiplexer)
1	0	Holds Previous State	
1	1	Reset to "0"	Reset to "0"

WD = WRITE DISABLE

R = RESET

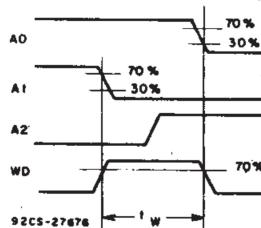


Fig. 3 – Definition of WRITE DISABLE ON time.

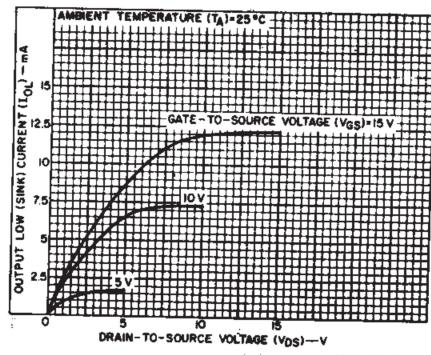


Fig. 4 – Minimum output low (sink) current characteristics.

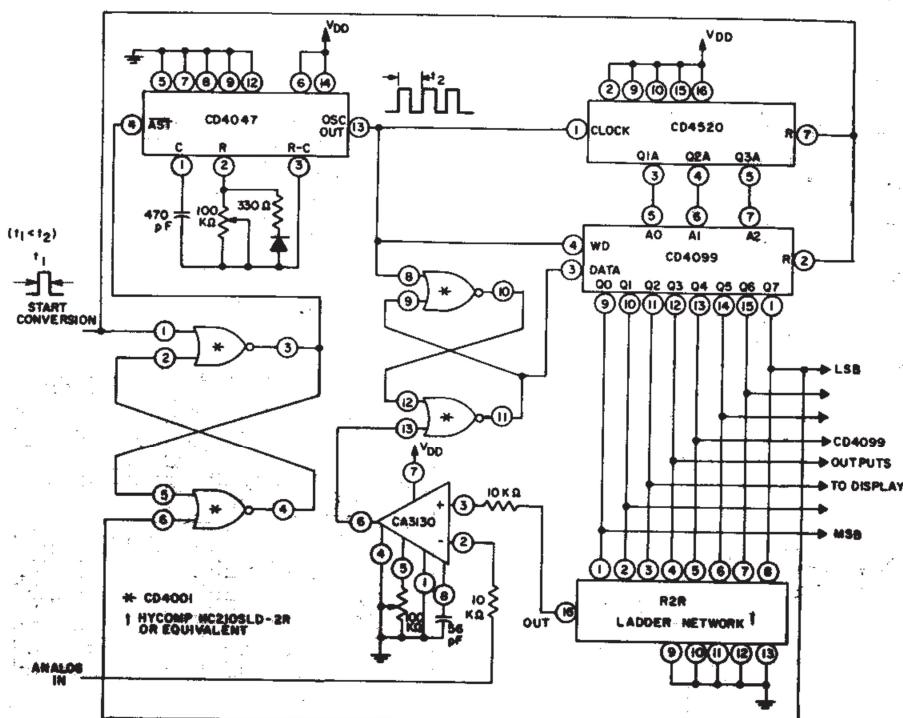


Fig. 5 – A/D converter

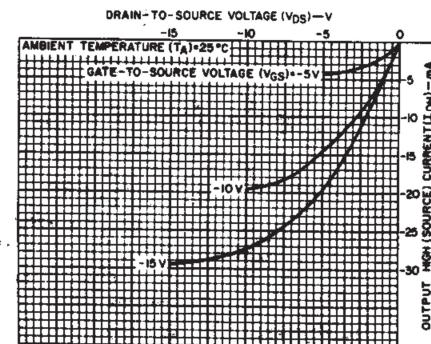
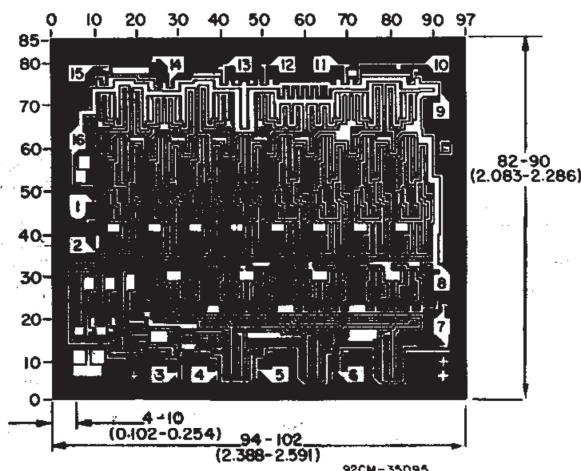


Fig. 6 – Typical output high (source) current characteristics.

# CD4099B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS	
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	+25			Min.	Typ.	Max.		
				-55	-40	+85	+125				
Quiescent Device Current, $I_{DD}$ Max.	-	0,5	5	5	5	150	150	-	0,04	5	
	-	0,10	10	10	10	300	300	-	0,04	10	
	-	0,15	15	20	20	600	600	-	0,04	20	
	-	0,20	20	100	100	3000	3000	-	0,08	100	
Output Low (Sink) Current $I_{OL}$ Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, $I_{OH}$ Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, $V_{OL}$ Max.	-	0,5	5	0,05			-	0	0,05	-	
	-	0,10	10	0,05			-	0	0,05	-	
	-	0,15	15	0,05			-	0	0,05	-	
Output Voltage: High-Level, $V_{OH}$ Min.	-	0,5	5	4,95			4,95	5	-	-	
	-	0,10	10	9,95			9,95	10	-	-	
	-	0,15	15	14,95			14,95	15	-	-	
Input Low Voltage, $V_{IL}$ Max.	0,5, 4,5	-	5	1,5			-	-	1,5	-	
	1,9	-	10	3			-	-	3	-	
	1,5, 13,5	-	15	4			-	-	4	-	
Input High Voltage, $V_{IH}$ Min.	0,5, 4,5	-	5	3,5			3,5	-	-	-	
	1,9	-	10	7			7	-	-	-	
	1,5, 13,5	-	15	11			11	-	-	-	
Input Current $I_{IN}$ Max.	-	0,18	18	$\pm 0,1$	$\pm 0,1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0,1$	$\mu A$



**CD4099BH**  
DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

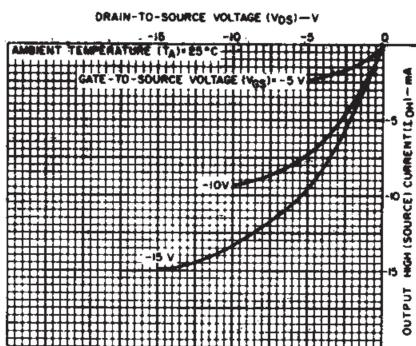


Fig. 7 – Minimum output high (source) current characteristics.

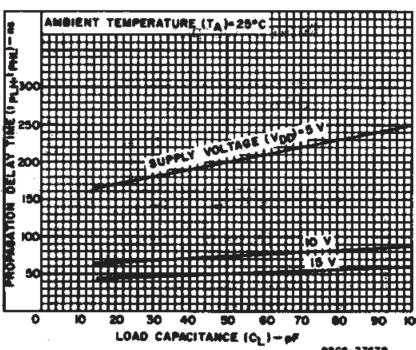


Fig. 8 – Typical propagation delay time (data to Qn) vs. load capacitance.

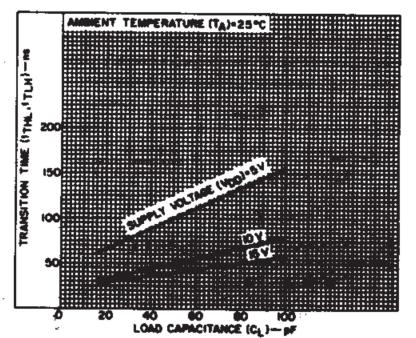


Fig. 9 – Typical transition time vs. load capacitance.

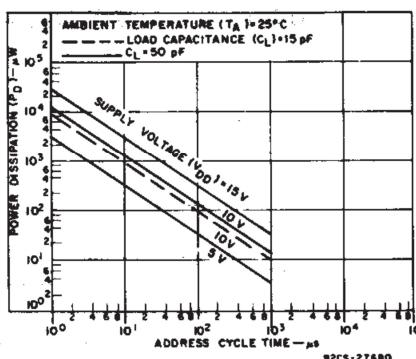


Fig. 10 – Typical dynamic power dissipation vs. address cycle time.

# CD4099B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ C$ ,  $C_L = 50 \mu F$ ,  
 Input  $t_r, t_f = 20 \text{ ns}$ ,  $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	CONDITIONS		LIMITS ALL PACKAGE TYPES		UNITS
	SEE FIG.15*	V <sub>DD</sub> (V)	TYP.	MAX.	
Propagation Delay: t <sub>PLH</sub> , t <sub>PHL</sub>	(1)	5	200	400	ns
		10	75	150	
		15	50	100	
Data to Output, WRITE DISABLE to Output, t <sub>PLH</sub> , t <sub>PHL</sub>	(2)	5	200	400	ns
		10	80	160	
		15	60	120	
Reset to Output, t <sub>PHL</sub>	(3)	5	175	350	ns
		10	80	160	
		15	65	130	
Address to Output, t <sub>PLH</sub> , t <sub>PHL</sub>	(9)	5	225	450	ns
		10	100	200	
		15	75	150	
Transition Time, t <sub>THL</sub> , (Any Output) t <sub>TLH</sub>		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Pulse Width, t <sub>W</sub>	(4)	5	100	200	ns
Data		10	50	100	
		15	40	80	
Address	(8)	5	200	400	ns
		10	100	200	
		15	65	125	
Reset	(5)	5	75	150	ns
		10	40	75	
		15	25	50	
Minimum Setup Time, t <sub>S</sub>	(6)	5	50	100	ns
Data to WRITE DISABLE		10	25	50	
		15	20	35	
Minimum Hold Time, t <sub>H</sub>	(7)	5	75	150	ns
Data to WRITE DISABLE		10	40	75	
		15	25	50	
Input Capacitance, C <sub>IN</sub>	Any Input	5	7.5	pF	

\*Circled numbers refer to times indicated on master timing diagram.

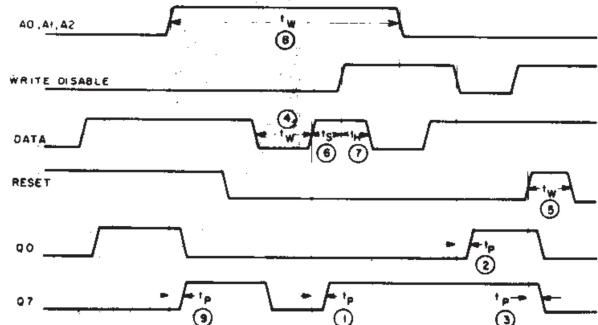


Fig. 15 – Master timing diagram.

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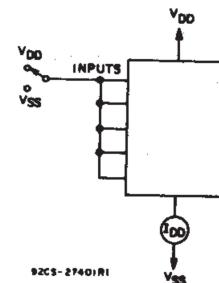


Fig. 11 – Quiescent device current test circuit.

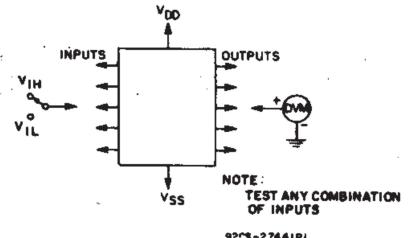


Fig. 12 – Input voltage test circuit.

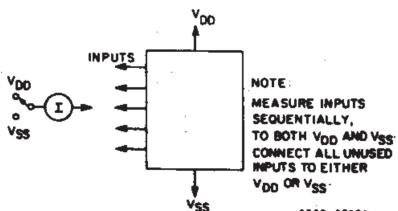
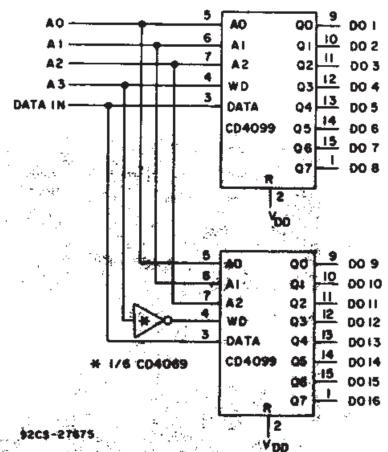


Fig. 13 – Input current test circuit.



92CS-27675

Fig. 14 – 1-of-16 decoder/demultiplexer.

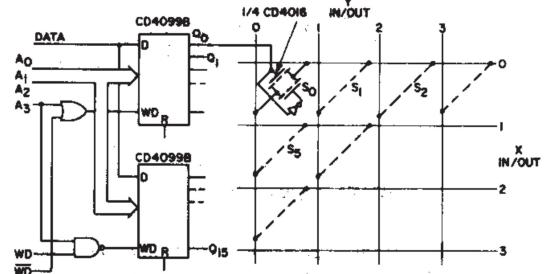


Fig. 16 – Multiple selection decoding – 4 x 4 crosspoint switch.