

CD4585B Types

CMOS 4-Bit Magnitude Comparator

High Voltage Types (20-Volt Rating)

CD4585B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4585B has eight comparing inputs (A_3, B_3 , through A_0, B_0), three outputs ($A < B, A = B, A > B$) and three cascading inputs ($A < B, A = B, A > B$) that permit systems designers to expand the comparator function to 8, 12, 16.....4N bits. When a single CD4585B is used, the cascading inputs are connected as follows: ($A < B$) = low, ($A = B$) = high, ($A > B$) = high.

Cascading these units for comparison of more than 4 bits is accomplished as shown in Fig. 13.

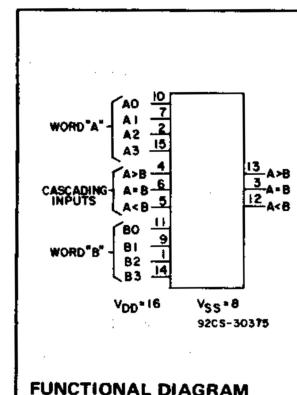
The CD4585B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Expansion to 8,12,16.....4N bits by cascading units
- Medium-speed operation:
compares two 4-bit words
in 180 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μ A at 18 V
over full package temperature range;
100 nA at 18 V and 25°C
- Noise margin (full package temperature range)
range) = 1 V at $V_{DD} = 5$ V
2 V at $V_{DD} = 10$ V
2.5 V at $V_{DD} = 15$ V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Servo motor controls ■ Process controllers



FUNCTIONAL DIAGRAM

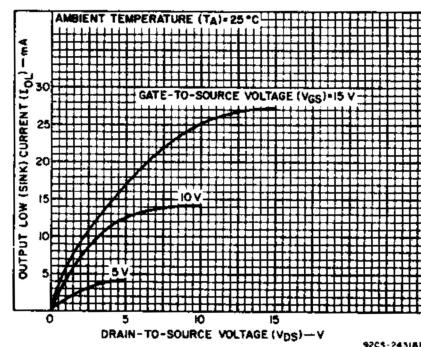


Fig.1 – Typical output low (sink) current characteristics.

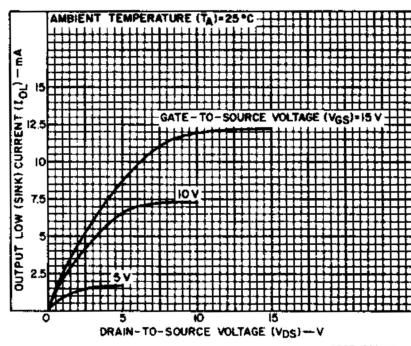


Fig.2 – Minimum output low (sink) current characteristics.

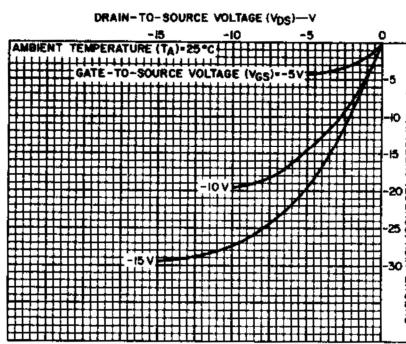


Fig.3 – Typical output high (source) current characteristics.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{STG}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch (1.59 \pm 0.79mm) from case for 10s max +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package Temperature Range}$)	3	18	V

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TRUTH TABLE

INPUTS				COMPARING			CASCAADING			OUTPUTS			
A ₃ , B ₃		A ₂ , B ₂		A ₁ , B ₁		A ₀ , B ₀		A < B	A = B	A > B	A < B	A = B	A > B
A ₃ > B ₃	X			X		X		X	X	1	0	0	1
A ₃ = B ₃	A ₂ > B ₂		X	X		X		X	X	1	0	0	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ > B ₁		X		X		X	X	1	0	0	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ > B ₀	X		X		X	X	1	0	0	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	0		0		1	0	0	0	1	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	0		1		X	0	1	0	0	0
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	1		0		X	1	0	0	0	0
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ < B ₀	X		X		X	X	1	0	0	0
A ₃ = B ₃	A ₂ = B ₂	A ₁ < B ₁		X		X		X	X	1	0	0	0
A ₃ < B ₃	X	X	X	X		X		X	X	1	0	0	0

X = Don't Care

Logic 1 = High Level

Logic 0 = Low Level

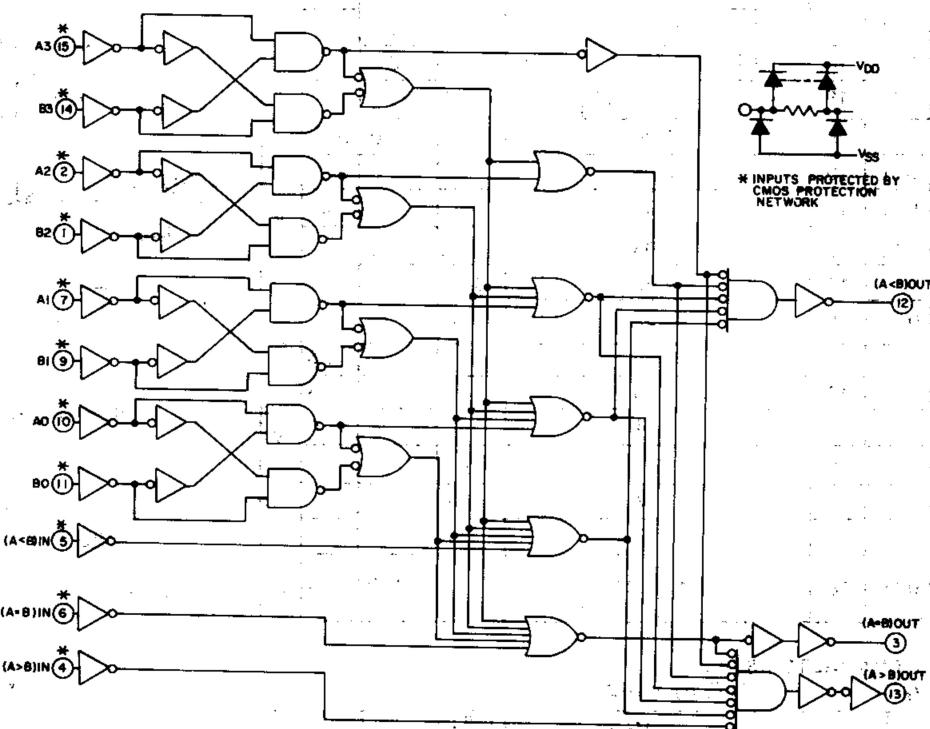


Fig. 4 - Logic diagram.

DRAIN-TO-SOURCE VOLTAGE (V_{DOS})—V

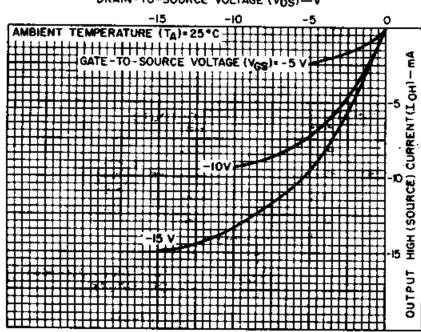


Fig. 5 — Minimum output high (source) current characteristics.

AMBIENT TEMPERATURE (T_A) = 25°C

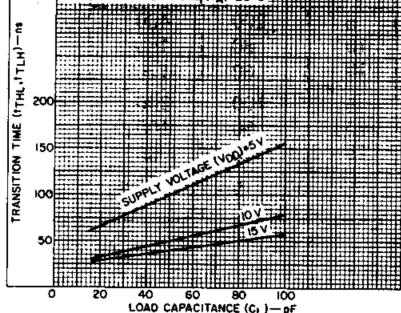


Fig. 6 — Typical transition time as a function of load capacitance.

AMBIENT TEMPERATURE (T_A) = 25°C

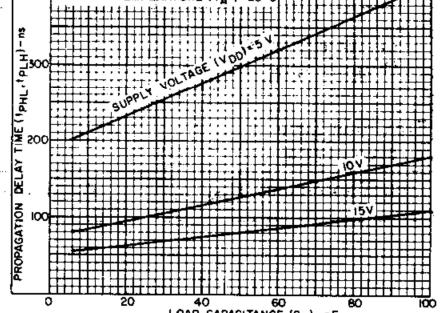


Fig. 7 — Typical propagation delay time ("comparing inputs" to outputs) as a function of load capacitance.

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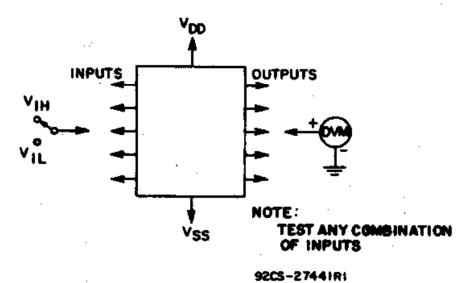
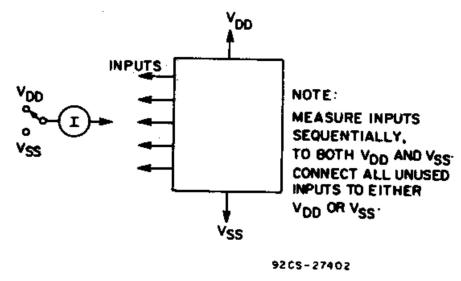
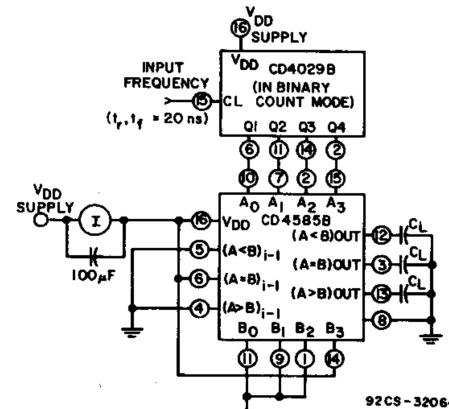
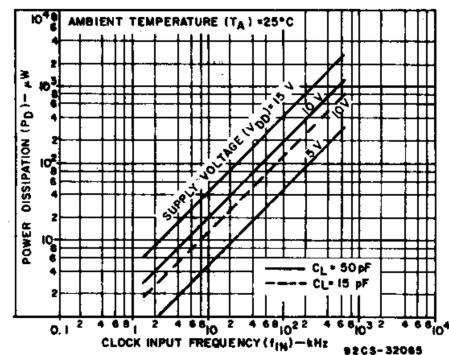
STATIC ELECTRICAL CHARACTERISTICS

CHARAC- TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						U N I T S	
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	-	0,5	5	5	5	150	150	-	0,04	5	μA
	-	0,10	10	10	10	300	300	-	0,04	10	
	-	0,15	15	20	20	600	600	-	0,04	20	
	-	0,20	20	100	100	3000	3000	-	0,08	100	
Output Low (Sink) Current I_{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I_{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage: Low-Level, V_{OL} Max.	-	0,5	5	0,05				-	0	0,05	V
	-	0,10	10	0,05				-	0	0,05	
	-	0,15	15	0,05				-	0	0,05	
Output Voltage: High-Level, V_{OH} Min.	-	0,5	5	4,95				4,95	5	-	V
	-	0,10	10	9,95				9,95	10	-	
	-	0,15	15	14,95				14,95	15	-	
Input Low Voltage V_{IL} Max.	0,5,4,5	-	5	1,5				-	-	1,5	V
	1,9	-	10	3				-	-	3	
	1,5,13,5	-	15	4				-	-	4	
Input High Voltage, V_{IH} Min.	0,5,4,5	-	5	3,5				3,5	-	-	V
	1,9	-	10	7				7	-	-	
	1,5,13,5	-	15	11				11	-	-	
Input Current I_{IN} Max.	-	0,18	18	$\pm 0,1$	$\pm 0,1$	± 1	± 1	-	$\pm 10^{-5}$	$\pm 0,1$	μA

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ C$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	V_{DD} Volts	LIMITS		UNITS
			Typ.	Max.	
Propagation Delay Time: Comparing Inputs to Outputs, t_{PHL}, t_{PLH}		5	300	600	ns
		10	125	250	
		15	80	160	
Cascading Inputs to Outputs, t_{PHL}, t_{PLH}		5	200	400	
		10	80	160	
		15	60	120	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	-	5	7,5	pF



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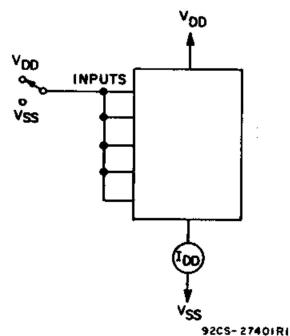
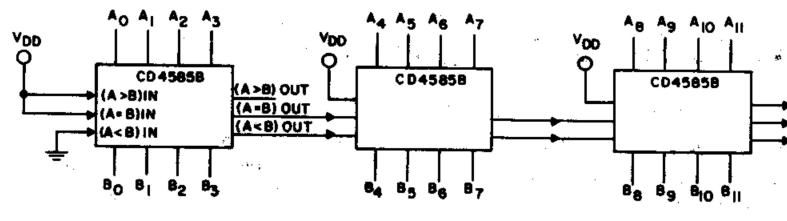


Fig. 12 — Quiescent-device-current test circuit.



$t_p \text{ TOTAL} = t_p \text{ (COMPARE)} + 2 \times t_p \text{ (CASCADE)}, \text{ AT } V_{DD} = 10V$
(3 STAGES)
 $= 120 + 2(80) = 280 \text{ ns (TYP.)}$

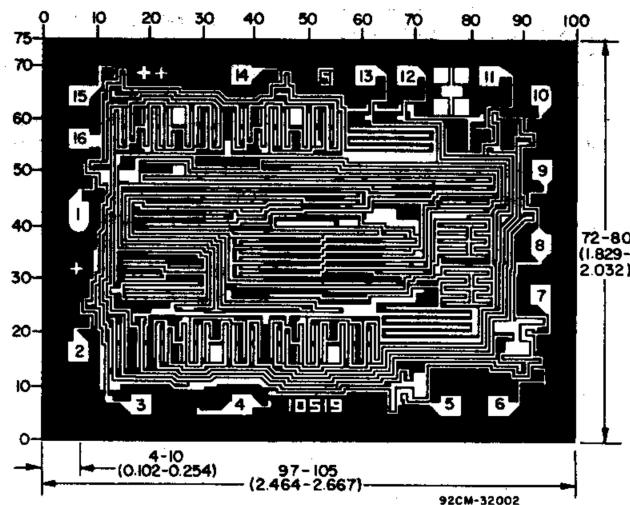
92CM-31007RI

Fig. 13 — Typical speed characteristics of a 12-bit comparator.

TERMINAL ASSIGNMENT

B2	1	16	V _{DD}
A2	2	15	A3
(A=B)OUT	3	14	B3
(A>B) IN	4	13	(A>B) OUT
(A<B) IN	5	12	(A<B) OUT
(A>B) IN	6	11	B0
A1	7	10	A0
V _{SS}	8	9	B1

TOP VIEW 92CS-31006



Dimensions and Pad Layout for CD4585BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).