

CD4510B, CD4516B Types

CMOS Presettable Up/Down Counters

High-Voltage Types (20-Volt Rating)

CD4510B —— BCD Type

CD4516B —— Binary Type

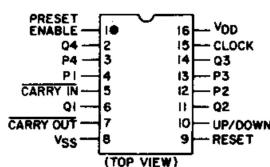
■ CD4510B Presettable BCD Up/Down Counter and the CD4516 Presettable Binary Up/Down Counter. consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The CD4510B will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode.

If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage.

The CD4510B and CD4516B can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage. (See Fig. 15).

These devices are similar to types MC14510 and MC14516.

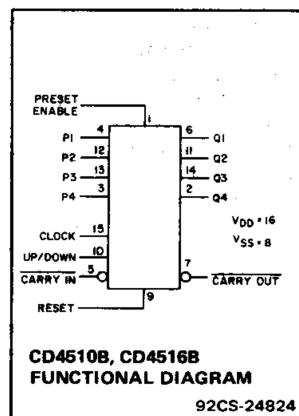
The CD4510B and CD4516B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD4516B types also are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix).



CD4510B, CD4516B
TERMINAL ASSIGNMENT

Features:

- Medium-speed operation – $f_{CL} = 8 \text{ MHz}$ typ. at 10 V
- Synchronous internal carry propagation
- Reset and Preset capability
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range): 1 V at $V_{DD} = 5 \text{ V}$
2 V at $V_{DD} = 10 \text{ V}$
2.5 V at $V_{DD} = 15 \text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4510B, CD4516B
FUNCTIONAL DIAGRAM

92CS-24824

Applications:

- Up/Down difference counting
- Multistage synchronous counting
- Multistage ripple counting
- Synchronous frequency dividers

OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (At $T_A = \text{Full Package-Temperature Range}$)		3	18	V
Clock Pulse Width, t_W	5	150	—	ns
	10	75	—	
	15	60	—	
Clock Input Frequency, f_{CL}	5	—	2	MHz
	10	—	4	
	15	—	5.5	
Preset Enable or Reset Removal Time*	5	150	—	ns
	10	80	—	
	15	60	—	
Clock Rise and Fall Time, t_{rCL}, t_{fCL}^*	5	—	15	μs
	10	—	5	
	15	—	5	
Carry-In Setup Time, t_S	5	130	—	ns
	10	60	—	
	15	45	—	
Up-Down Setup Time, t_S	5	360	—	ns
	10	160	—	
	15	110	—	
Preset Enable or Reset Pulse Width, t_W	5	220	—	ns
	10	100	—	
	15	75	—	

*Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).

*If more than one unit is cascaded in the parallel clocked application, t_{rCL} should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

CD4510B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT $\pm 10\text{mA}$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55 $^\circ\text{C}$ to +125 $^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{STG}) -65 $^\circ\text{C}$ to +150 $^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79\text{mm}$) from case for 10s max +265 $^\circ\text{C}$

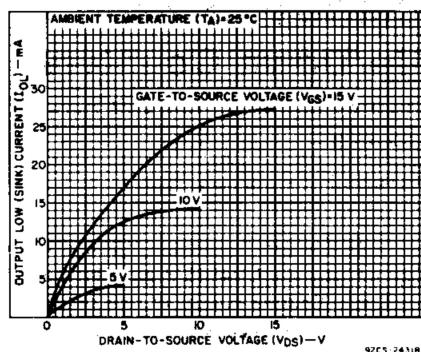


Fig.1 – Typical output low (sink) current characteristics.

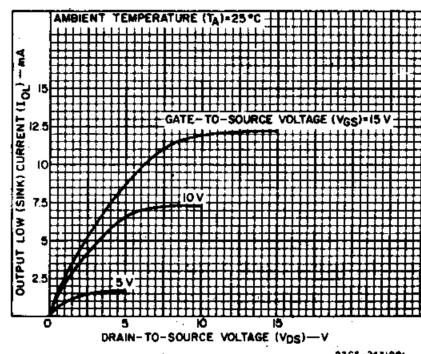


Fig.2 – Minimum output low (sink) current characteristics.

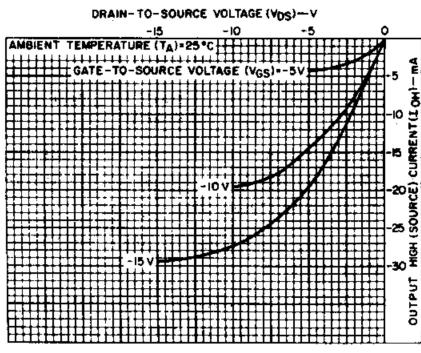


Fig.4 – Typical output high (source) current characteristics.

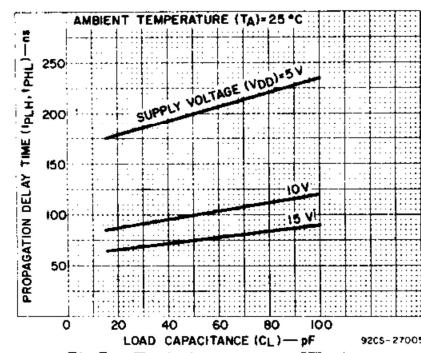


Fig.7 – Typical propagation delay time vs. load capacitance for clock-to-Q outputs.

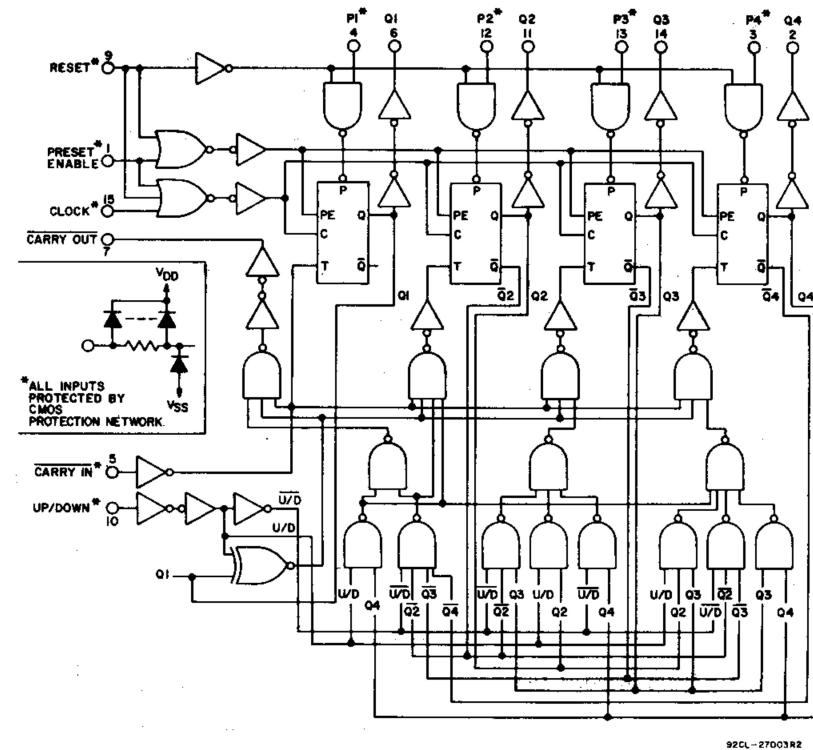


Fig.3 – Logic Diagram for CD4510B.

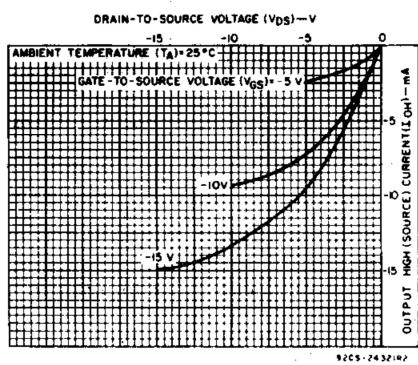


Fig.5 – Minimum output high (source) current characteristics.

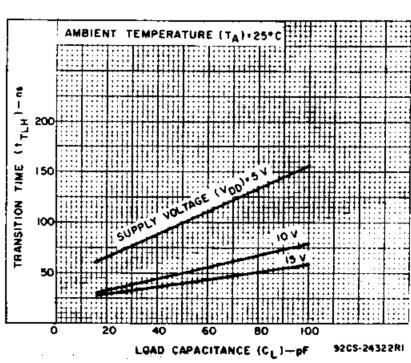


Fig.6 – Typical transition time vs. load capacitance.

CD4510B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	+25	
Quiescent Device Current, I _{DD} Max.	-	0,5	5	5	5	150	150	-	0,04	5		μA
	-	0,10	10	10	10	300	300	-	0,04	10		
	-	0,15	15	20	20	600	600	-	0,04	20		
	-	0,20	20	100	100	3000	3000	-	0,08	100		
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-		mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-		
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-		
Output High (Source) Current I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-		
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-		
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-		
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-		
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0,05				-	0	0,05		V
	-	0,10	10	0,05				-	0	0,05		
	-	0,15	15	0,05				-	0	0,05		
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4,95				4,95	5	-		V
	-	0,10	10	9,95				9,95	10	-		
	-	0,15	15	14,95				14,95	15	-		
Input Low Voltage, V _{IL} Max.	0,5, 4,5	-	5	1,5				-	-	1,5		V
	1,9	-	10	3				-	-	3		
	1,5, 13,5	-	15	4				-	-	4		
Input High Voltage, V _{IH} Min.	0,5, 4,5	-	5	3,5				3,5	-	-		V
	1,9	-	10	7				7	-	-		
	1,5, 13,5	-	15	11				11	-	-		
Input Current I _{IN} Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 ⁻⁵	±0,1	μA	

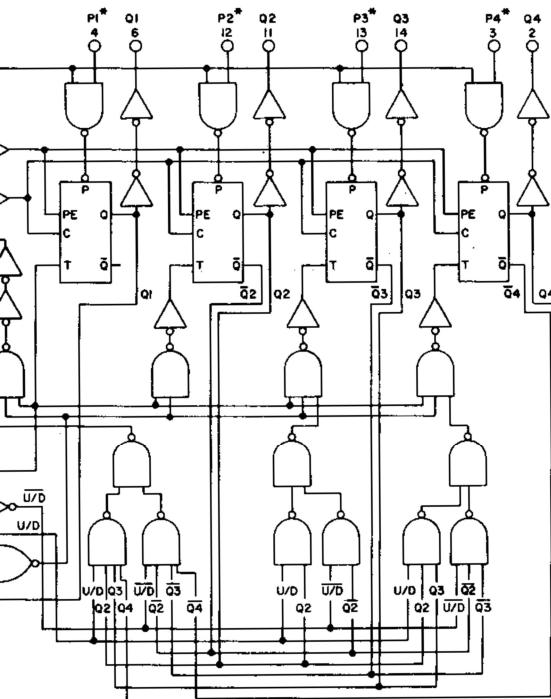


Fig. 16 – Logic Diagram for CD4516B.

92CL-27004R2

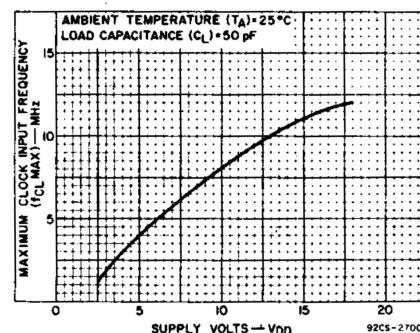


Fig. 8 – Typical maximum clock input frequency vs. supply voltage.

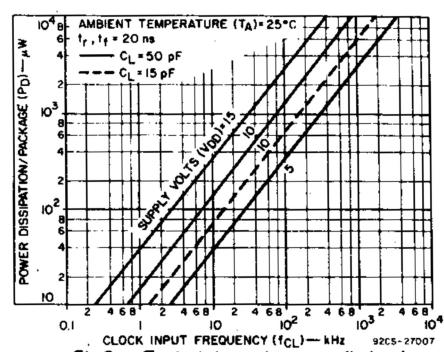


Fig. 9 – Typical dynamic power dissipation vs. frequency.

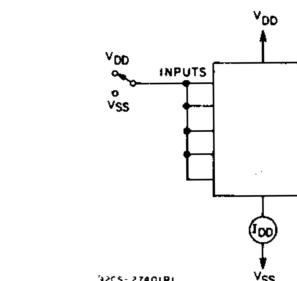


Fig. 11 – Quiescent-device-current test circuit.

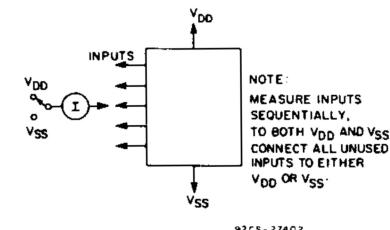


Fig. 12 – Input-current test circuit.

CD4510B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $C_L = 50 \text{ pF}$,
 Input $t_r, t_f = 20 \text{ ns}$, $R_L = 200 \text{ k}\Omega$

Characteristic	Conditions V_{DD} (V)	Limits			Units
		Min.	Typ.	Max.	
Propagation Delay Time (t_{PHL}, t_{PLH}):					
Clock-to-Q Output (See Fig. 10)	5	—	200	400	ns
	10	—	100	200	
	15	—	75	150	
Preset or Reset-to-Q Output	5	—	210	420	ns
	10	—	105	210	
	15	—	80	160	
Clock-to-Carry Out	5	—	240	480	ns
	10	—	120	240	
	15	—	90	180	
Carry-In-to-Carry Out	5	—	125	250	ns
	10	—	60	120	
	15	—	50	100	
Preset or Reset-to-Carry Out	5	—	320	640	ns
	10	—	160	320	
	15	—	125	250	
Transition Time (t_{TTL}, t_{TTH}) (See Fig. 9)	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Max. Clock Input Frequency (f_{CL})	5	2	4	—	MHz
	10	4	8	—	
	15	5.5	11	—	
Input Capacitance (C_{IN})		—	5	7.5	pF
Set-up Time, t_S Preset Enable to J_n	5	25	12	—	ns
	10	10	6	—	
	15	10	5	—	
Hold times, t_H Clock to Carry-In	5	60	30	—	ns
	10	30	4	—	
	15	30	1	—	
Clock to Up/Down	5	30	10	—	ns
	10	30	4	—	
	15	30	5	—	
Preset Enable to J_n	5	70	35	—	ns
	10	40	20	—	
	15	40	20	—	

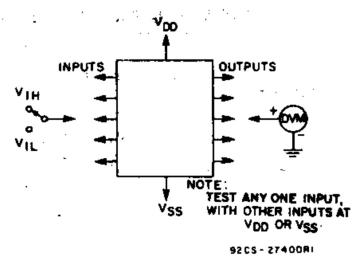


Fig. 13 – Input-voltage test circuit.

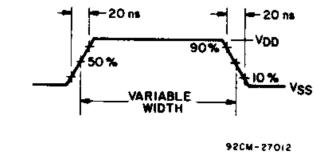
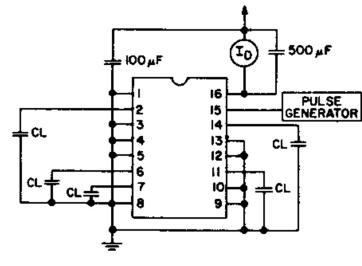
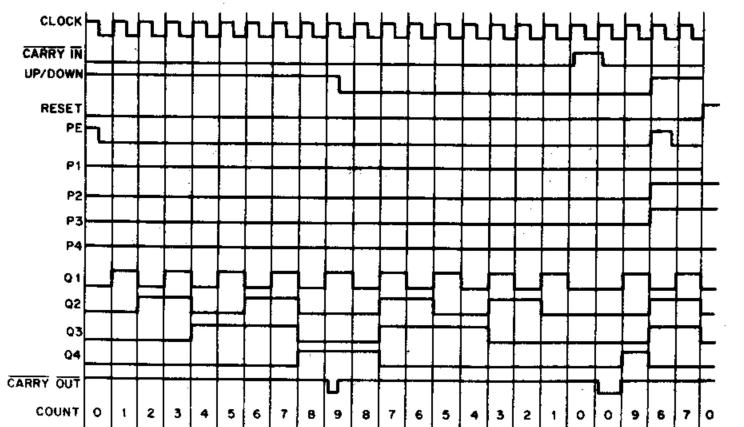


Fig. 14 – Power-dissipation test circuit and input waveform.

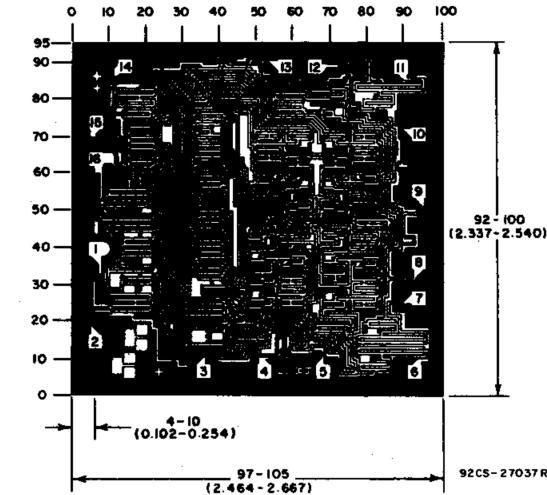
CD4510B Types



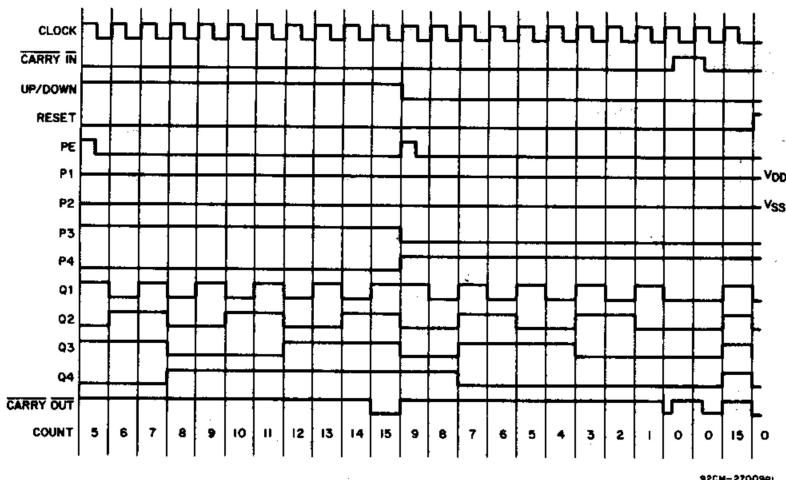
CL	CF	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
1	0	1	0	0	COUNT UP
1	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = DON'T CARE

TRUTH TABLE

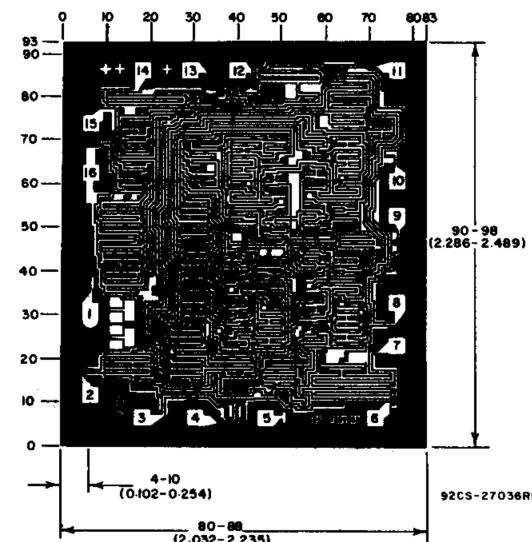


Dimensions and Pad Layout for CD4510BH.

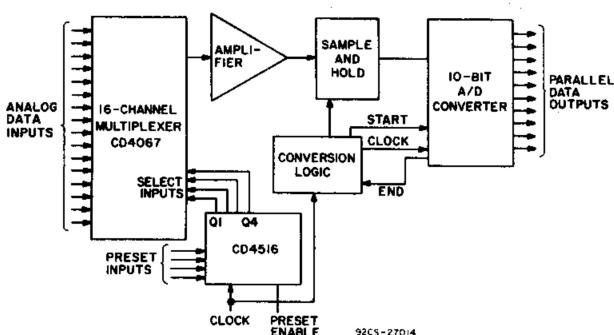


3

COMMERCIAL CMOS
HIGH VOLTAGE ICs



Dimensions and Pad Layout for CD4516BH.



This acquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the CD4516B.

Fig. 17 — Typical 16-channel, 10-bit data acquisition system.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CD4510B Types

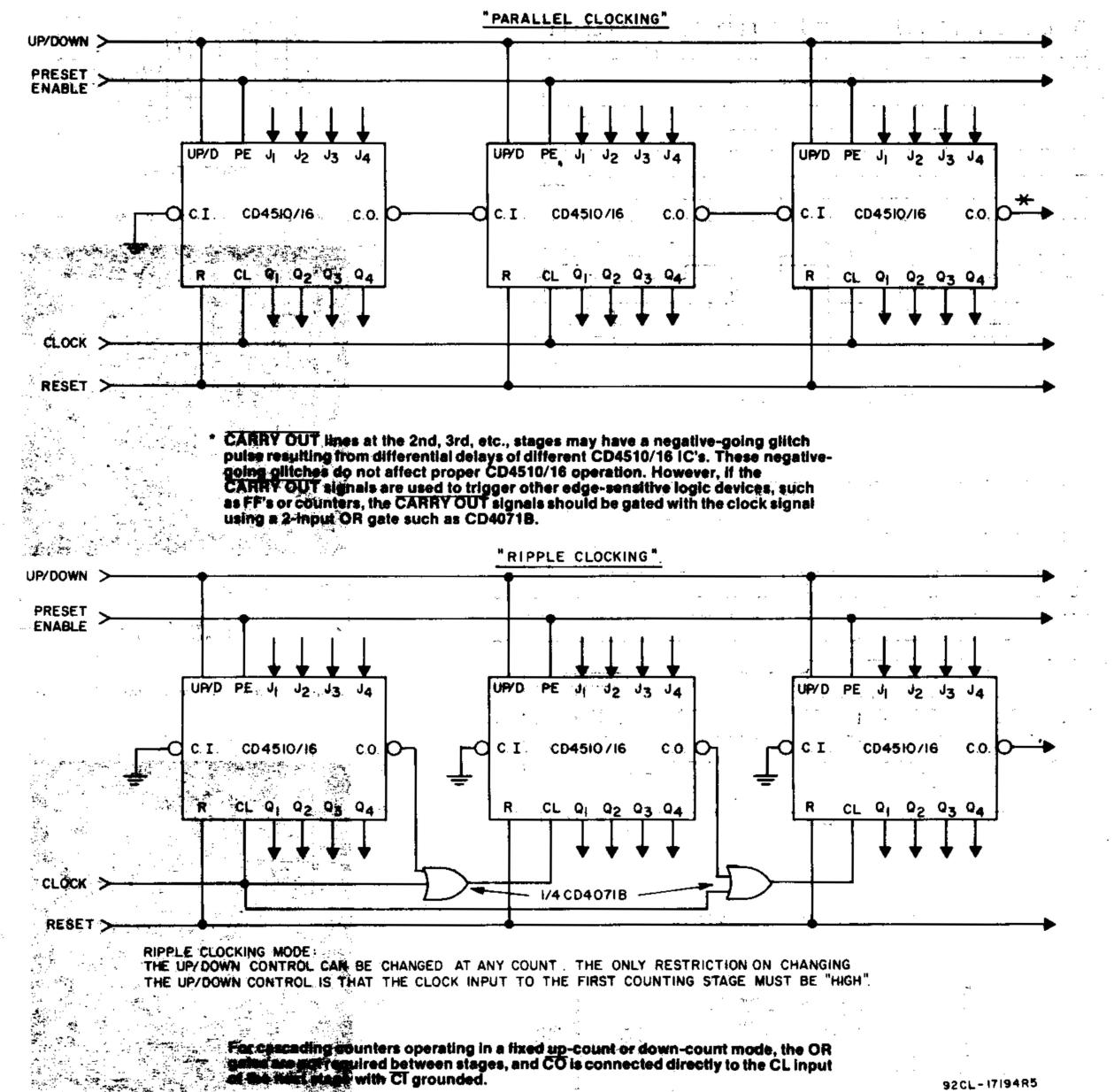


Fig. 18 — Cascading counter packages.