

CD4518B, CD4520B Types

CMOS Dual Up-Counters

High-Voltage Types (20-Volt Rating)

CD4518B Dual BCD Up-Counter CD4520B Dual Binary Up-Counter

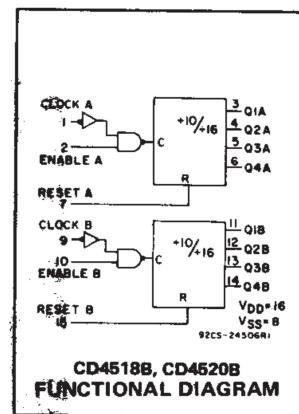
■ CD4518 Dual BCD Up-Counter and CD4520 Dual Binary Up-Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

The CD4518B and CD4520B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Medium-speed operation – 6-MHz typical clock frequency at 10 V
- Positive- or negative-edge triggering
- Synchronous internal carry propagation
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at $V_{DD} = 5$ V
2 V at $V_{DD} = 10$ V
2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



**CD4518B, CD4520B
FUNCTIONAL DIAGRAM**

Applications:

- Multistage synchronous counting
- Multistage ripple counting
- Frequency dividers

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
	1	0	Increment Counter
0		0	Increment Counter
	X	0	No Change
X		0	No Change
	0	0	No Change
1		0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care 1 ≡ High State 0 ≡ Low State

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ± 10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

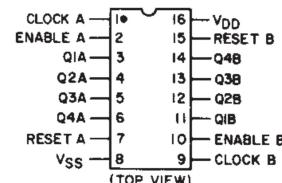
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$ 100mW

OPERATING-TEMPERATURE RANGE (T_A) -55°C to +125°C

STORAGE TEMPERATURE RANGE (T_{stg}) -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max +265°C



**CD4518B, CD4520B
TERMINAL ASSIGNMENT**

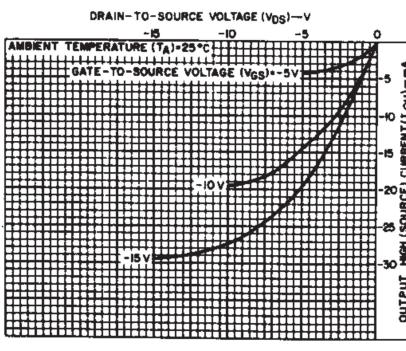


Fig. 3 – Typical output high (source) current characteristics.

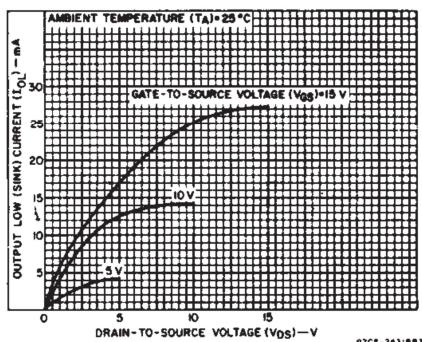


Fig. 1 – Typical output low (sink) current characteristics.

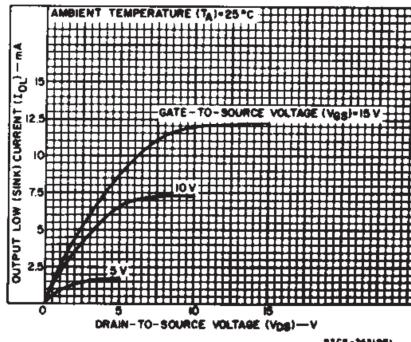
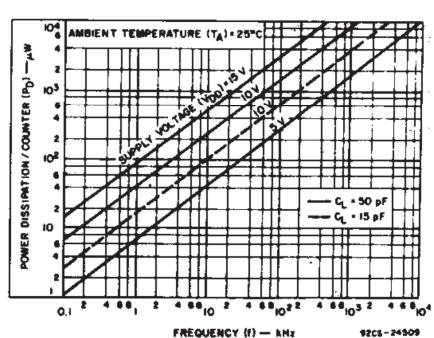
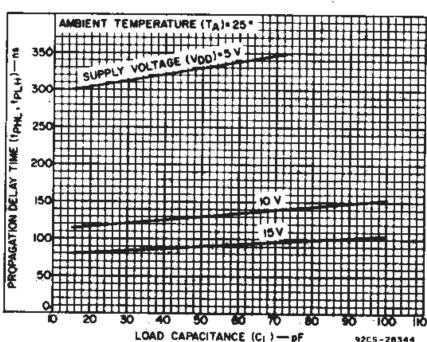
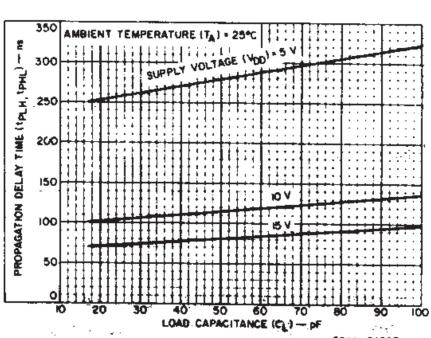
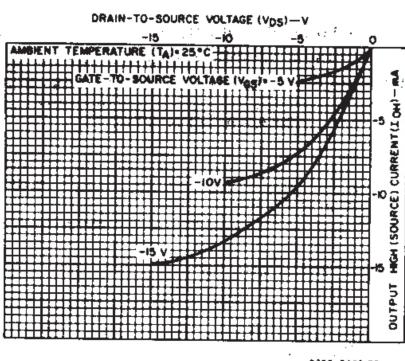
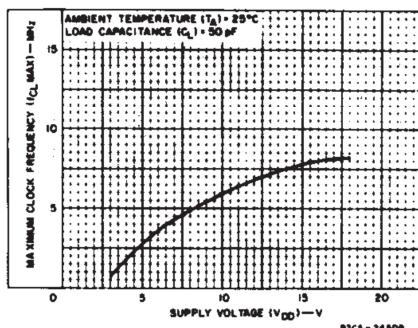
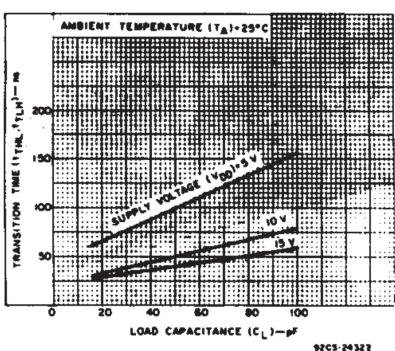


Fig. 2 – Minimum output low (sink) current characteristics.

CD4518B, CD4520B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)						UNITS	
	V_O (V)	V_{IN} (V)	V_{DD} (V)	+25							
				-55	-40	+85	+125	Min.	Typ.		
Quiescent Device Current, I_{DD} Max.	-	0.5	5	5	5	150	150	-	0.04	5	
	-	0.10	10	10	10	300	300	-	0.04	10	
	-	0.15	15	20	20	600	600	-	0.04	20	
	-	0.20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I_{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V_{OL} Max.	-	0.5	5	0.05			-	0	0.05	-	
	-	0.10	10	0.05			-	0	0.05	-	
	-	0.15	15	0.05			-	0	0.05	-	
Output Voltage: High-Level, V_{OH} Min.	-	0.5	5	4.95			4.95	5	-	-	
	-	0.10	10	9.95			9.95	10	-	-	
	-	0.15	15	14.95			14.95	15	-	-	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	-	5	1.5			-	-	1.5	-	
	1, 9	-	10	3			-	-	3	-	
	1.5, 13.5	-	15	4			-	-	4	-	
Input High Voltage, V_{IH} Min.	0.5, 4.5	-	5	3.5			3.5	-	-	-	
	1, 9	-	10	7			7	-	-	-	
	1.5, 13.5	-	15	11			11	-	-	-	
Input Current I_{IN} Max.	-	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1	μA



CD4518B, CD4520B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$. Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that
operation is always within the following ranges:

CHARACTERISTIC	V _{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply Voltage Range (For T_A =Full Package Temperature Range)		3	18	V
Enable Pulse Width, t_W	5	400	—	ns
	10	200	—	
	15	140	—	
Clock Pulse Width, t_W	5	200	—	ns
	10	100	—	
	15	70	—	
Clock Input Frequency, f_{CL}	5		1.5	MHz
	10	dc	3	
	15		4	
Clock Rise or Fall Time, t_{rCL} or t_{fCL}	5	—	15	μs
	10	—	5	
	15	—	5	
Reset Pulse Width, t_W	5	250	—	ns
	10	110	—	
	15	80	—	

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A=25^\circ\text{C}$;
Input $t_r, t_f=20\text{ ns}$, $C_L=50\text{ pF}$, $R_L=200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		V _{DD} V	Min.	Typ.	Max.
Propagation Delay Time, t_{PHL}, t_{PLH} Clock or Enable to Output	5	—	280	560	ns
	10	—	115	230	
	15	—	80	160	
Reset to Output	5	—	330	650	ns
	10	—	130	225	
	15	—	90	170	
Transition Time, t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Maximum Clock Input Frequency, f_{CL}	5	1.5	3	—	MHz
	10	3	6	—	
	15	4	8	—	
Minimum Clock Pulse Width, t_W	5		100	200	ns
	10		50	100	
	15		35	70	
Clock Rise or Fall Time, t_r or t_f	5	—	—	15	μs
	10, 15	—	—	5	
Minimum Reset Pulse Width, t_W	5	—	125	250	ns
	10	—	55	110	
	15	—	40	80	
Minimum Enable Pulse Width, t_W	5	—	200	400	ns
	10	—	100	200	
	15	—	70	140	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

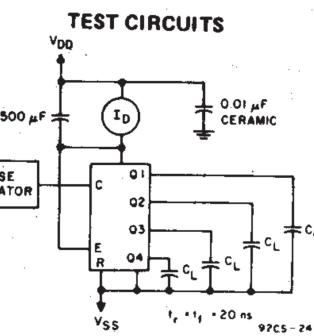


Fig. 10 — Dynamic power dissipation.

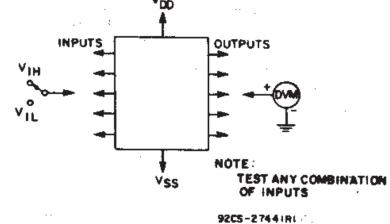


Fig. 11 — Input voltage.

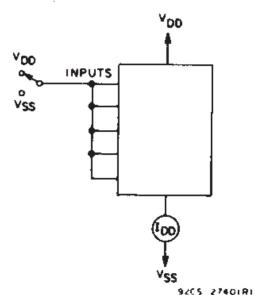


Fig. 12 — Quiescent device current test circuit.

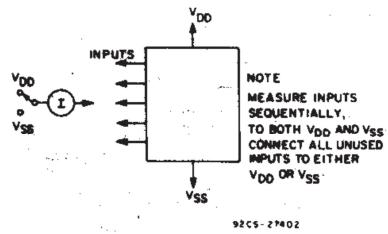


Fig. 13 — Input leakage-current test circuit.

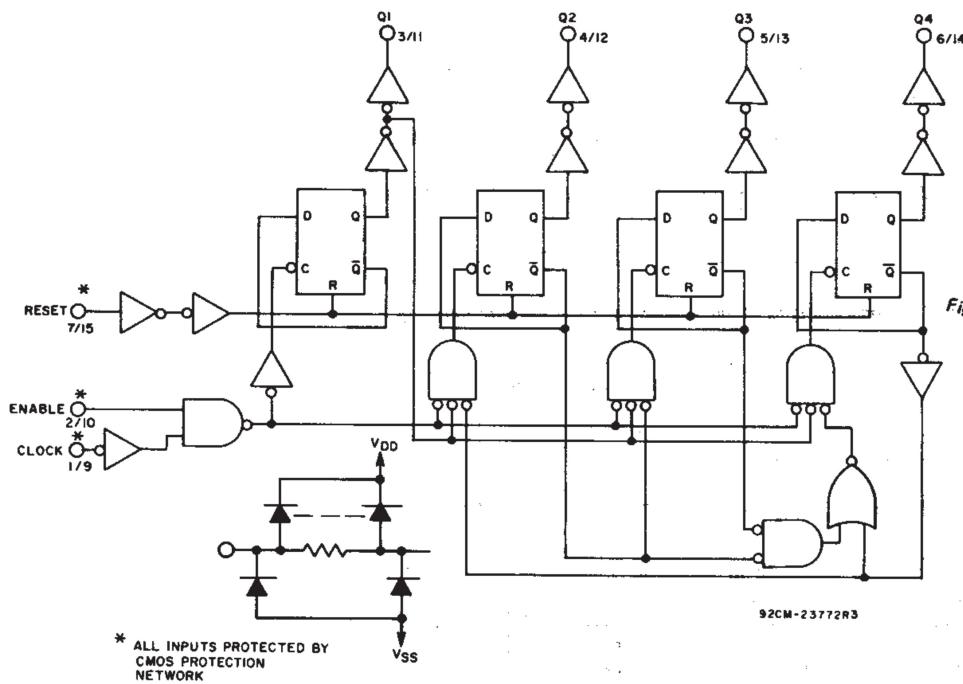
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Fig. 14 — Decade counter (CD4518B) logic diagram for one of two identical counters.

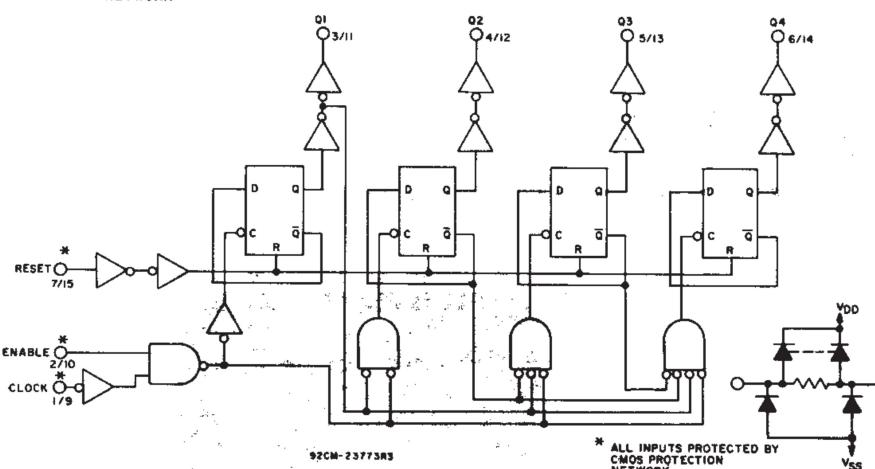


Fig. 15 — Binary counter (CD4520B) logic diagram for one of two identical counters.

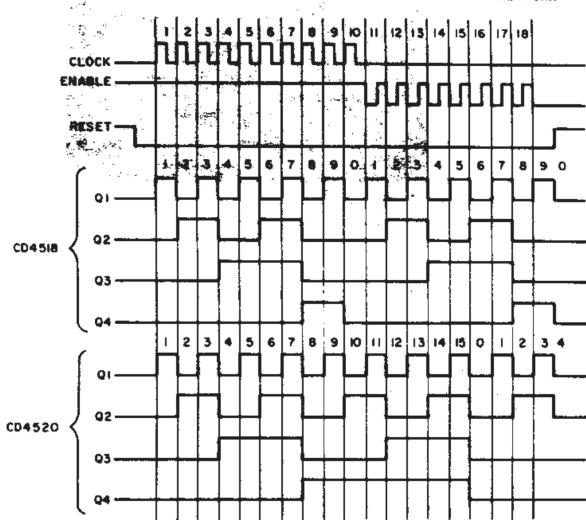


Fig. 16 — Timing diagrams for CD4518B and CD4520B.

CD4518B, CD4520B Types

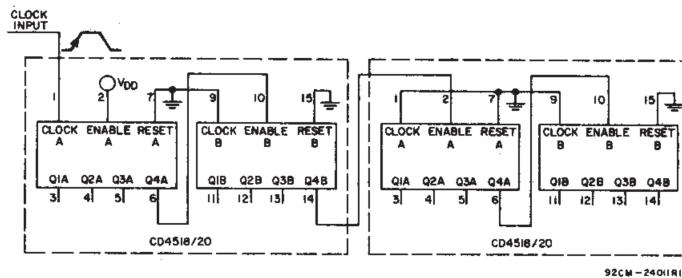
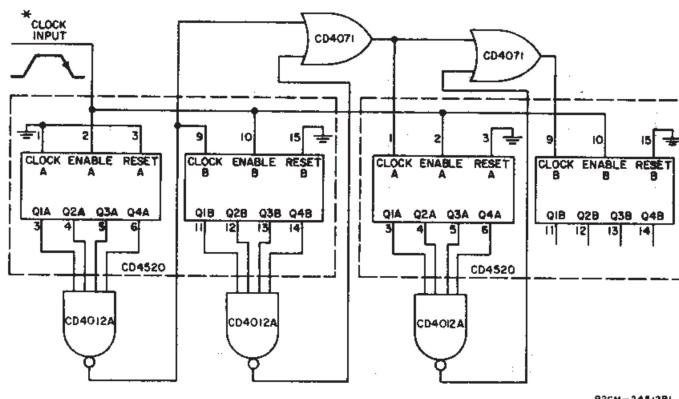
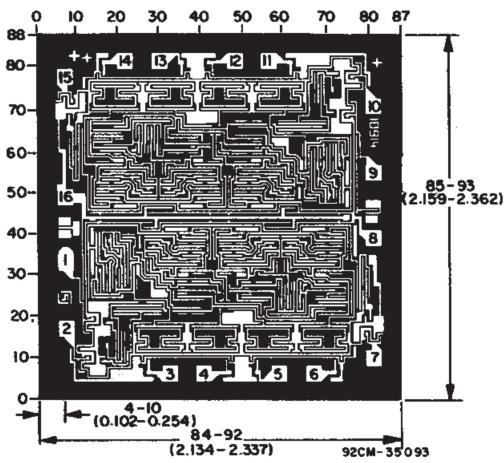


Fig.17 – Ripple cascading of four counters with positive edge triggering.

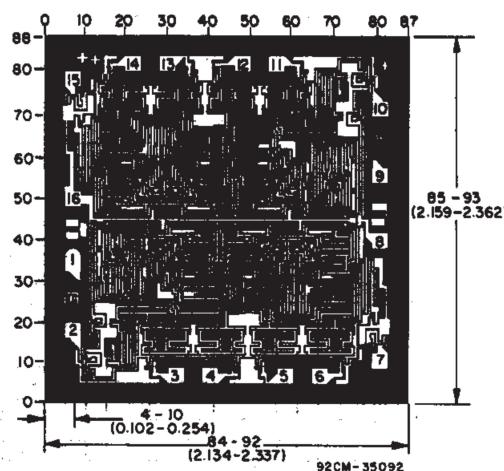


*NOTE:
FOR SYNCHRONOUS CASCADING, THE CLOCK TRANSITION TIME SHOULD BE MADE LESS THAN OR EQUAL TO THE SUM OF THE FIXED PROPAGATION DELAY AT 15 pF AND THE TRANSITION TIME OF THE OUTPUT DRIVER STAGE FOR THE ESTIMATED CAPACITATIVE LOAD.

Fig.18 – Synchronous cascading of four binary counters with negative edge triggering.



Dimensions and pad layout for CD4518BH chip.



Dimensions and pad layout for CD4520BH chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.
Grid gradations are in mils (10^{-3} inch).