

**CMOS**
**Quad Exclusive-OR Gate**
**High-Voltage Types (20-Volt Rating)**

■ CD4030B types consist of four independent Exclusive-OR gates. The CD4030B provides the system designer with a means for direct implementation of the Exclusive-OR function.

The CD4030B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

**MAXIMUM RATINGS, Absolute-Maximum Values:**
**DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )**

Voltages referenced to  $V_{SS}$  Terminal) ..... -0.5V to +20V

**INPUT VOLTAGE RANGE, ALL INPUTS** ..... -0.5V to  $V_{DD}$  +0.5V

**DC INPUT CURRENT, ANY ONE INPUT** .....  $\pm 10\text{mA}$

**POWER DISSIPATION PER PACKAGE (PD):**

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearity at 12mW/ $^\circ\text{C}$  to 200mW

**DEVICE DISSIPATION PER OUTPUT TRANSISTOR**

FOR  $T_A$  = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

**OPERATING-TEMPERATURE RANGE ( $T_A$ )** ..... -55 $^\circ\text{C}$  to  $+125^\circ\text{C}$

**STORAGE TEMPERATURE RANGE ( $T_{stg}$ )** ..... -65 $^\circ\text{C}$  to  $+150^\circ\text{C}$

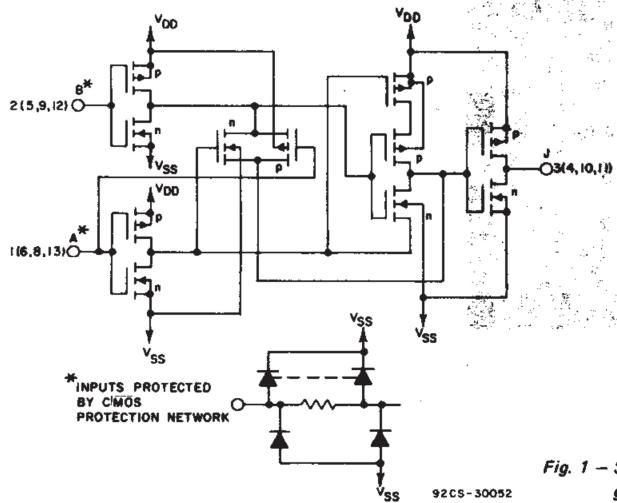
**LEAD TEMPERATURE (DURING SOLDERING):**

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max .....  $+265^\circ\text{C}$

**RECOMMENDED OPERATING CONDITIONS**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A$ = Full Package Temperature Range)	3	18	V


**Features:**

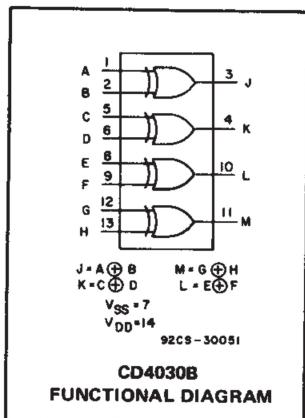
- Medium-speed operation— $t_{PHL}$ ,  $t_{PLH}$  = 65 ns (typ.) at  $V_{DD} = 10\text{V}$ ,  $C_L = 50\text{pF}$
- 100% tested for quiescent current at 20V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1  $\mu\text{A}$  at 18V over full package-temperature range; 100 nA at 18V and  $25^\circ\text{C}$
- Noise margin (over full package-temperature range):

$$1\text{V at } V_{DD} = 5\text{V}$$

$$2\text{V at } V_{DD} = 10\text{V}$$

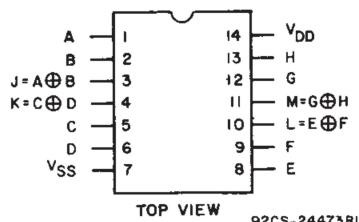
$$2.5\text{V at } V_{DD} = 15\text{V}$$

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"


**Applications:**

- Even and odd-parity generators and checkers
- Logical comparators
- Adders/subtractors
- General logic functions

TERMINAL DIAGRAM  
 Top View



TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

I = HIGH LEVEL

O = LOW LEVEL

## CD4030B Types

### STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	-55	-40	+85	+125	+25			Min.	Typ.
Quiescent Device Current, $I_{DD}$ Max.	-	0,5	5	0,25	0,25	7,5	7,5	—	0,01	0,25	$\mu A$	
	-	0,10	10	0,5	0,5	15	15	—	0,01	0,5		
	-	0,15	15	1	1	30	30	—	0,01	1		
	-	0,20	20	5	5	150	150	—	0,02	5		
Output Low (Sink) Current $I_{OL}$ Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	—	$mA$	
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	—		
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	—		
Output High (Source) Current, $I_{OH}$ Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	—	$mA$	
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	—		
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	—		
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	—		
Output Voltage: Low-Level, $V_{OL}$ Max.	—	0,5	5	0,05			—	0	0,05	$V$		
	—	0,10	10	0,05			—	—	0,05			
	—	0,15	15	0,05			—	0	0,05			
Output Voltage: High-Level, $V_{OH}$ Min.	—	0,5	5	4,95			4,95	5	—	$V$		
	—	0,10	10	9,95			9,95	10	—			
	—	0,15	15	14,95			14,95	15	—			
Input Low Voltage, $V_{IL}$ Max.	0,5,4,5	—	5	1,5			—	—	1,5	$V$		
	1,9	—	10	3			—	—	3			
	1,5,13,5	—	15	4			—	—	4			
Input High Voltage, $V_{IH}$ Min.	0,5,4,5	—	5	3,5			3,5	—	—	$V$		
	1,9	—	10	7			7	—	—			
	1,5,13,5	—	15	11			11	—	—			
Input Current $I_{IN}$ Max.	—	0,18	18	$\pm 0,1$	$\pm 0,1$	$\pm 1$	$\pm 1$	—	$\pm 10^{-5}$	$\pm 0,1$	$\mu A$	

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ C$ ; Input  $t_r, t_f = 20$  ns,  
 $C_L = 50$  pF,  $R_L = 200$  k $\Omega$

CHARACTERISTIC	CONDITIONS			LIMITS		UNITS
	$V_{DD}$ (V)	Typ.	Max.			
Propagation Delay Time, $t_{PLH}, t_{PHL}$	5	140	280			ns
	10	65	130			
	15	50	100			
Transition Time, $t_{THL}, t_{TLH}$	5	100	200			ns
	10	50	100			
	15	40	80			
Input Capacitance, $C_{IN}$	Any Input		5	7,5	pF	

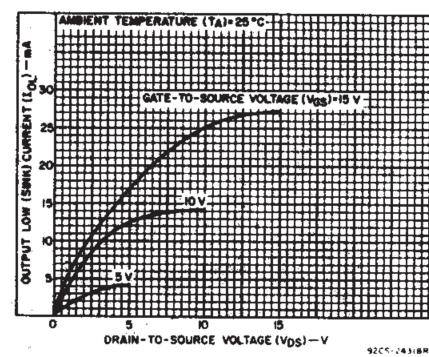


Fig. 2 – Typical output low (sink) current characteristics.

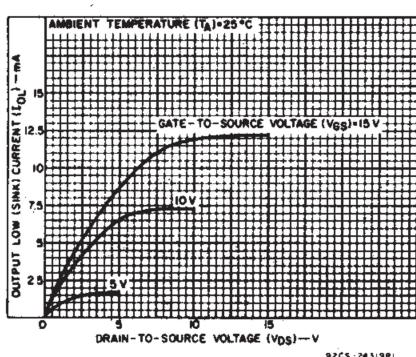


Fig. 3 – Minimum output low (sink) current characteristics.

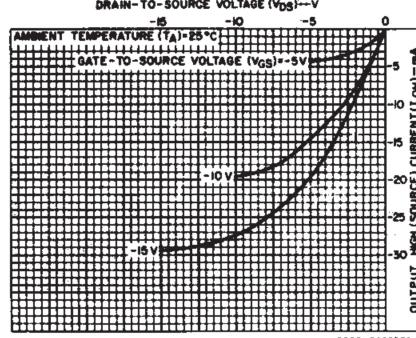


Fig. 4 – Typical output high (source) current characteristics.

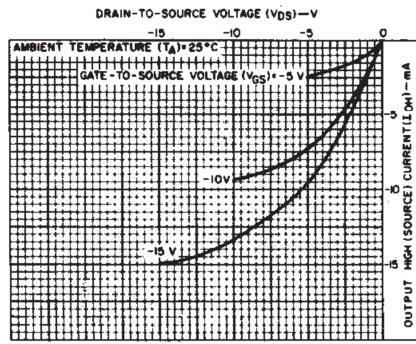


Fig. 5 – Minimum output high (source) current characteristics.

## CD4030B Types

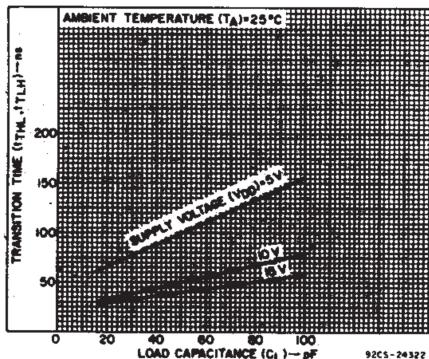


Fig. 6 – Typical transition time as a function of load capacitance.

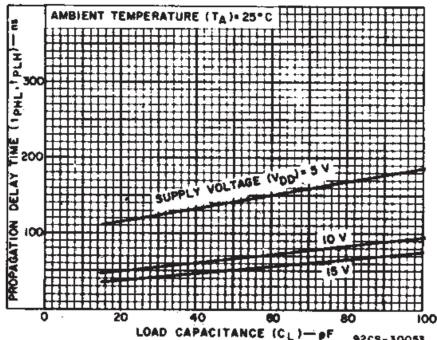


Fig. 7 – Typical propagation delay time as a function of load capacitance.

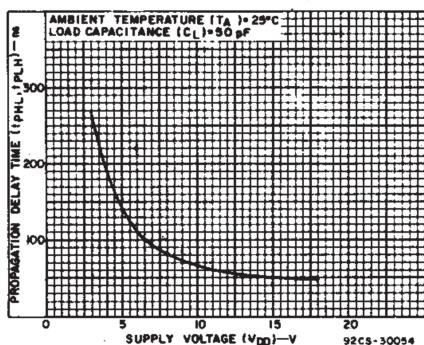


Fig. 8 – Typical propagation delay time as a function of supply voltage.

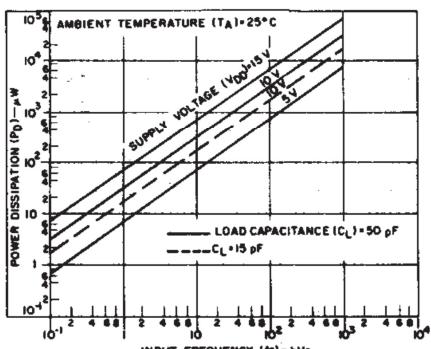


Fig. 9 – Typical dynamic power dissipation as a function of input frequency.

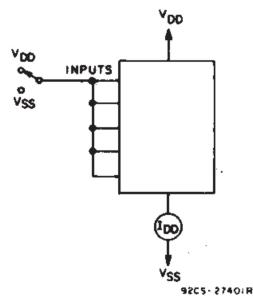


Fig. 10 – Quiescent-device current test circuit.

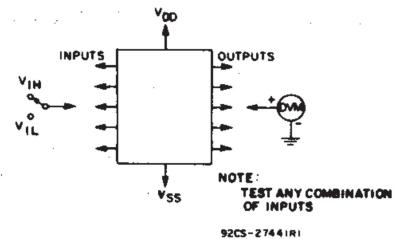


Fig. 11 – Input-voltage test circuit.

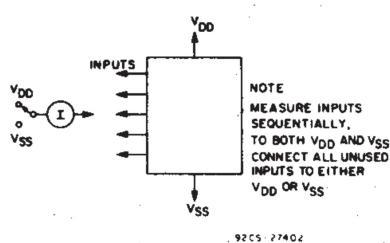


Fig. 12 – Input-current test circuit.

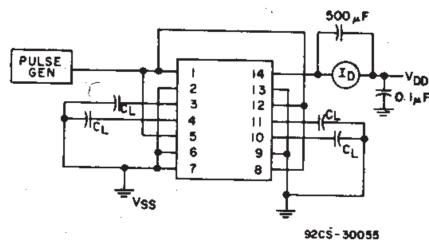
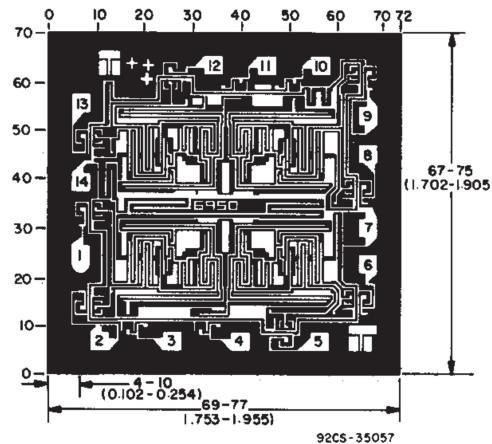


Fig. 13 – Dynamic power dissipation test circuit.



Dimensions and pad layout for CD4030BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).