

IMPLEMENTING 32-BIT WALLACE MULTIPLIER

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REQUIRED CIRCUIT:

64-BIT CARRY LOOKAHEAD ADDER
64-BIT FULL ADDER
64-BIT AND GATE GENERATOR

FILES USED:

☐ WALLACE MULTIPLIER:

- ☐ 32wallace.v(MAIN FILE)
- ☐ 32wallace_tb.v (TEST-BENCH FILE)
- ☐ 32wallace.vcd(GTK_WAVE FILE)

☐ 64-BIT CARRY LOOKAHEAD ADDER:

- ☐ 2kpg.v
- ☐ kpg.v
- ☐ ppc1.v
- ☐ adder64alt.v

☐ 64-BIT FULL ADDER

- ☐ fullAdder.v
- ☐ fourBitAdder.v
- ☐ 16BitAdder.v
- ☐ 32BitAdder.v
- ☐ 64BitAdder.v
- ☐ 3fa.v
- ☐ 3fam.v

☐ 64-BIT AND GATE GENERATOR

- ☐ ppg.v

IMPLEMENTING 64-BIT CARRY LOOKAHEAD ADDER:

PROCEDURE:

- ☐ "Adder64alt.v" IS THE MAIN FILE WHICH ESTABLISHES THE FUNCTIONALITY OF CARRY LOOK AHEAD ADDER.
- ☐ RECURSIVE DOUBLING ALGORITHM IS USED TO GENERATE CARRY PARALLELLY
- ☐ "kpg.v" GENERATES THE 8-BIT STRINGS/CARRY IN THE FORM "k", "p" and "g" WHICH STANDS FOR KILL,PROPAGATE AND GENERATE.

- ❑ “Kpg.v” DEPENDS ON CIRCUIT “2kpg.v” WHICH GENERATES 1-BIT CARRY STRINGS IN THE SAME FORM AS ABOVE
- ❑ “ppc1.v” USES RECURSIVE DOUBLING ALGORITHM TO DIVIDE 64 STRINGS OF CARRY STRINGS INTO TWO GROUPS AT EACH LEVEL.THERE ARE LOG(64) LEVELS/PIPELINE
- ❑ I.E 6 LEVELS

NOTATION:

K= A NOR B(TRUE WHEN BOTH ARE 0)

P=A XOR B(TRUE WHEN EITHER ONE OF THEM IS 1)

G=A AND B(TRUE WHEN BOTH ARE 1)

IMPLEMENTING 64-BIT FULL ADDER:

PROCEDURE:

- ❑ “64BitAdder.v” IS THE MAIN FILE.BOTTOM-UP-APPROACH IS USED TO CONSTRUCT THE ADDER
- ❑ FIRST 1 BIT FULL ADDER IS CONSTRUCTED FIRST AND THEN FOUR BIT FULL ADDER IS CONSTRUCTED AND GOES ALL THE WAY TO 64 BIT ADDER
- ❑ HIERARCHY :1 BIT->4-BIT->16-BIT->32-BIT->64-BIT
- ❑ HERE THE FULL ADDER HAS A MODIFIED PURPOSE ,IT GENERATES SUM AND CARRY BITS SEPERATELY.
- ❑ FOR EXAMPLE 4-BIT FULL ADDER GENERATES 4-BIT SUM AND 4-BIT CARRY OUTPUT BASED ON THE LOGIC :
 - ❑ $SUM = A \oplus B \oplus CARRY_IN$
 - ❑ $CARRY = (A.B) + (B.C) + (C.A)$

IMPLEMENTING WALLACE MULTIPLIER:

PROCEDURE:

HIERARCHY LEVEL/PIPELINE LEVEL:

CONNECTIONS ARE MADE ACCORDING TO LEVEL WISE.REFER THE TREE.INPUTS ARE THE PARTIAL PRODUCTS AND THE OUTPUT IS THE MULTIPLIED RESULT

CIRCUIT DEPTH : 9

PARTIAL PRODUCTS GENERATED: 32

OUTPUT_BIT_LENGTH:MAX 63

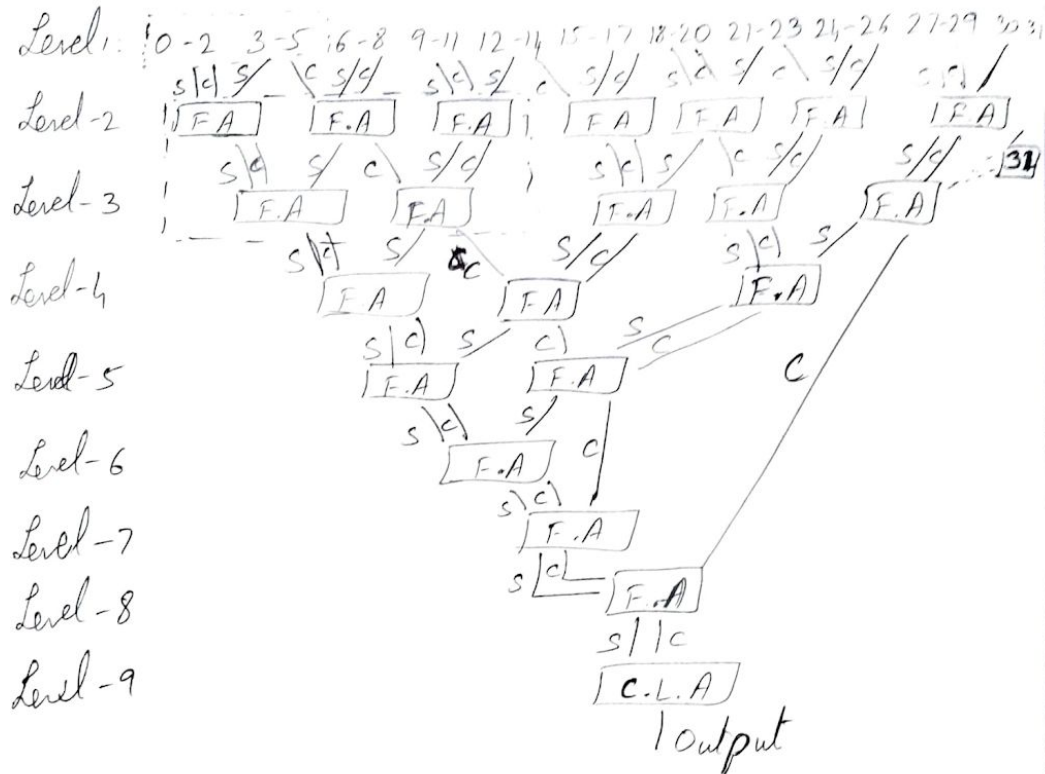
LEVEL-TREE:

Input: $A = 32$ bits $B = 32$ bits

Partial Product Generated: 32

PpG: 1 2 3 4 5 6 7 8 9

25 26 27 31 32



At Level-1 () the dotted box is generated using 3fa.v which takes 3 partial products as input and "Sum" and "Carry" as Output (two:bit width)

At Level-2 through 8, the box (sample at Level-2) takes ~~three~~ five Sum and four Carry products as input and two Sum and two Carry as Output

OUTPUT: TESTBENCH:

```
(base) sharan@OMEN:~/Desktop/course/vlsi_lab/exp5$ iverilog 32wallace_tb.v
(base) sharan@OMEN:~/Desktop/course/vlsi_lab/exp5$ ./a.out
VCD info: dumpfile 32wallace.vcd opened for output.
  0 Input bts:Multiplier=5.419827e+07 and Multiplicand =3.866623e+06;
    Output:
    In Exponential form:Result=2.095643e+14
    Decimal form=      209564281208833

  5 Input bts:Multiplier=1.900000e+01 and Multiplicand =1.500000e+01;
    Output:
    In Exponential form:Result=2.850000e+02
    Decimal form=          285

 10 Input bts:Multiplier=9.943000e+06 and Multiplicand =3.302367e+06;
    Output:
    In Exponential form:Result=3.283544e+13
    Decimal form=     32835435081000

 20 Input bts:Multiplier=4.294967e+09 and Multiplicand =4.282057e+09;
    Output:
    In Exponential form:Result=1.839129e+19
    Decimal form=18391292651155357894

 25 Input bts:Multiplier=2.598300e+04 and Multiplicand =6.419870e+05;
    Output:
    In Exponential form:Result=1.668075e+10
    Decimal form=     16680748221

 35 Input bts:Multiplier=2.882400e+09 and Multiplicand =2.882208e+09;
    Output:
    In Exponential form:Result=8.307676e+18
    Decimal form= 8307675765591249094
```

GTKWAVE FORM:

