# Tri Minh Nguyen

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### **EDUCATION Princeton University**, Princeton, NJ, USA

Sep 2012 – Present

Candidate, Doctor of Philosophy (Ph.D.) in Electrical Engineering

Master of Arts (M.A.) in Electrical Engineering

Adviser: Professor David Wentzlaff

#### University of Texas at Austin, Austin, TX, USA

Sep 2008 – May 2012

Bachelor of Science (B.S.) in Electrical and Computer Engineering

Graduated with High Honors. Cumulative GPA: 3.93 / 4.00

#### RESEARCH INTERESTS & EXPERTISE

**Interests**: manycore, throughput-oriented, GPU architecture, hardware accelerator, machine learning, deep learning (DNN/CNN/LSTM), neuromorphic computing.

**Skills**: architectural simulation, performance modeling, RTL design and verification, Android programming, deep learning frameworks.

Programming fluency: C/C++ 11, Python, Verilog, Java

# RESEARCH EXPERIENCE

#### **Princeton University**

Research Assistant

Sep 2012 - Sep 2018

**Bandwidth compression:** Investigating the problem in throughput-oriented architectures (GPUs/Xeon Phi) and its solutions, including cache compression, link compression, efficient memory layout, efficient HBM/stacked-memory, etc.

**NVM:** Studied nonvolatile memory as a replacement for DRAM and provided a novel and high performance logging system for crash consistency.

#### **Open-source projects:**

- **OpenPITON processor**: Designed the cache system, cache-coherence protocol, network-on-chip protocol, and JTAG debug-port for PITON, a 25-core academic manycore processor. Verified the design with directed and randomized assembly tests. Synthesized the design with industrial tools (Synopsys) and taped out in IBM 32nm process. <a href="http://parallel.princeton.edu/piton/">http://parallel.princeton.edu/piton/</a>
- **PRIME open-source simulator**: key developer of PRIME, a fast, distributed parallel, scalable manycore simulator. https://github.com/PrincetonUniversity/primesim
  Advisor: Professor David Wentzlaff

#### **University of Texas at Austin**

Research Assistant

Sep 2011 – May 2012

- **Hardware accelerator:** Conducted a feasibility study of accelerating drug discovery using FPGA, through studying molecular dynamic (MD) algorithm and analyzing the integer/floating point performance of state-of-the-art FPGAs.
- **GPU:** Identify and optimize GPU workloads with dynamic compilation through similarity matrices. *Advisor: Professor VJ Reddi*

# SELECTED PUBLICATIONS

**Tri Nguyen**, and David Wentzlaff, "PiCL: a Software-Transparent, Persistent Cache Log for Nonvolatile Main Memory," MICRO'18

**Tri Nguyen**, Adi Fuchs, and David Wentzlaff, "CABLE: Cache-based Link Compression for Manycore Architectures," MICRO'18

Tri Nguyen, and David Wentzlaff, "MORC: Manycore-oriented Cache Compression," MICRO'15

Yaosheng Fu, **Tri Nguyen**, and David Wentzlaff, "Coherence Domain Restriction on Massive Scale Systems," in MICRO'15

Michael McKeown, Yaosheng Fu, **Tri Nguyen**, Yanqi Zhou, Jonathan Balkind, Alexey Lavrov, Mohammad Shahrad, Samuel Payne, Xiaohua Liang, Matthew Matl, and David Wentzlaff "OpenPiton: An Open Source Manycore Research Framework," in ASPLOS'16

Michael McKeown, Yaosheng Fu, **Tri Nguyen**, Yanqi Zhou, Jonathan Balkind, Alexey Lavrov, Mohammad Shahrad, Samuel Payne, and David Wentzlaff "*Piton: A 25-core Academic Manycore Processor*," in *HotChips'16* 

WORK EXPERIENCE

#### NVIDIA Research, Redmond, WA, USA

Jun 2017 - Sep 2017

Research Intern

Investigated and characterized the performance of cutting-edge GPU DNN machine learning algorithms including CNN and LSTM. Devised architectural improvements for future GPUs beyond Volta. Characterized GPU performance as a shared virtual GPU in the cloud. Contributed to the development of the internal GPU simulator widely used in company.

Manager: David Nellans

AMD Research, Boxborough, MA, USA

Jun 2016 - Sep 2016

Research Intern

Implemented state-of-the-art hardware compression algorithm for super-computing workloads and evaluated energy savings at the RTL/gate-level. Submitted a patent on a novel compression algorithm specifically designed to reduce data movement energy.

Manager: Greg Sadowski

NVIDIA, Santa Clara, CA, USA

May 2012 – Aug 2012

Intern

Wrote on-die oscilloscope extraction software for quality assurance and used it to analyze transient voltage noise as a cause of failures. Wrote and improved noise virus testing suite to increase fault coverage decrease test time.

Manager: Apoorv Gupta

Samsung, Suwon, South Korea

May 2011 – Aug 2011

Intern

Investigated the feasibility and benefits of data compression for solid-state drives (SSD), including gzip/DEFLATE, and with fixed block-based compression, and using fingerprinting for variable block-size compression.

Manager: Kyungho Kim

TEACHING EXPERIENCE

#### Princeton ELE301 – Design of Real Systems

Fall 2013 & Fall 2017

Assistant Instructor

Developed lab assignments for a new course at university. Led weekly lab sessions and designed Android-to-microcontroller interfacing labs.

## **UT Austin – Probability and Random Processes**

Sep 2011 – Jan 2012

**University Tutor** 

Instructor for the university's free tutoring program.

HONORS & AWARDS

#### Student Travel Grant, MICRO'17, ASPLOS'16, ISCA'15, ISCA'14

Supports from ACM, NSF, SIGMICRO, and others.

University Honors, University of Texas at Austin

2008 - 2012

Dec 2010

**Third place**, Final Project EE345L, Embedded Systems Design, UT Austin

Microcontroller as a gaming device with impressive 3D capability

**First place** in tank simulation AI competition.

Dec 2009

EE319K, Intro to Embedded Systems, UT Austin

**ACTIVITIES** 

## Princeton EE Musical MelodEE,

Mar 2017

Organizer

Eta Kappu Nu Honors Society, UT Austin

Sep 2010 – May 2012

Member

Study abroad, Sungkyunkwan University, South Korea

Jan 2011 – Jun 2011

Shotokai Karate Club, UT Austin

Sep 2008 – May 2010

Member then vice-president

Last updated: July 2018