BÁO CÁO THỰC HÀNH VI MẠCH SỐ

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LAB1

Task 1: Examine and Modify the Setup Files

Khởi động Tools

```
ces_sva_2019.06   license_list.txt              Training
command.log       LISTEN.port                   vcst_command.log
core.163906       LOVE_IC                       vcst_rtdb
Desktop           Music                         vcst_rtdb.bak
Doc               novas.conf                    vcst_session.log
Documents         novas.rc                      vcst_session.log.bak
Downloads         P306                          verdiLog
DVEfiles          Pictures                      Videos
filenames.log     pt_shell_command.log          work
gui_command.log   Public                        Workspace
icc2_command.log  SNPS_TOOL_SETUP.csh
icc2_output.txt   SNPS_TOOL_SETUP.csh.bk.200103
[synopsys1@dell740 ~]$ cd 19200536
[synopsys1@dell740 ~/19200536]$ ls
ces_DCNXT_2021.06.tar.gz  DCNXT_2021.06
[synopsys1@dell740 ~/19200536]$ cd DCNXT_2021.06/
[synopsys1@dell740 DCNXT_2021.06]$ cd lab1
[synopsys1@dell740 lab1]$ dcnxt_shell -topo -gui

                        Design Compiler (R) NXT

              Version T-2022.03-SP4 for linux64 - Aug 24, 2022

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            Inclusivity and Diversity" (Refer to article 000036315 at
                        https://solvnetplus.synopsys.com)
Initializing...
Starting shell in Topographical mode...
*********************************************************
Design Compiler NXT Workshop
The following aliases are available:
 cs                            change_selection
 csa                           change_selection -add
 ga                            get_attribute
 gs                            get_selection
 h                             history
```
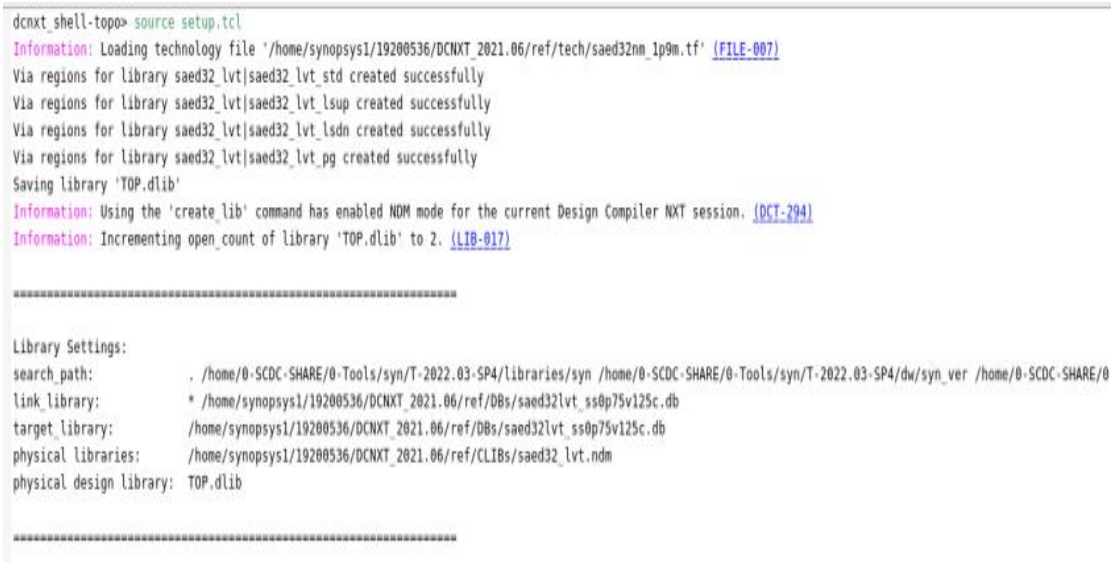

Sửa lại File rm_setup/common_setup.tcl

```
##########################################################################################
#######
# User-defined variables for logical library setup in dc_setup.tcl
##########################################################################################
#######
```

```
set      ADDITIONAL_SEARCH_PATH                "/home/synopsys1/19200536/DCNXT_2021.06/ref/DBs
/home/synopsys1/19200536/DCNXT_2021.06/ref/CLIBs
/home/synopsys1/19200536/DCNXT_2021.06/ref/tech
/home/synopsys1/19200536/DCNXT_2021.06/lab1/rtl
/home/synopsys1/19200536/DCNXT_2021.06/lab1/scripts"  ;#  Directories containing logic libraries,

#  logic design and script files.

Set TARGET_LIBRARY_FILES
"/home/synopsys1/19200536/DCNXT_2021.06/ref/DBs/saed32lvt_ss0p75v125c.db"                    ;
#  Logic cell library files

##########################################################################################
#######
# User-defined variables for physical library setup in dc_setup.tcl
##########################################################################################
#######

set NDM_DESIGN_LIB          "TOP.dlib"              ;#  User-defined NDM design library name

set                                                                    NDM_REFERENCE_LIBS
"/home/synopsys1/19200536/DCNXT_2021.06/ref/CLIBs/saed32_lvt.ndm"              ;#  NDM physical
cell libraries

set                                                                                TECH_FILE
"//home/synopsys1/19200536/DCNXT_2021.06/ref/tech/saed32nm_1p9m.tf"            ;#  Technology
file

set                                                                          TLUPLUS_MAX_FILE
"/home/synopsys1/19200536/DCNXT_2021.06/ref/tech/saed32nm_1p9m_Cmax.tluplus"      ;#   Max
TLUPlus file

set                                                                                MAP_FILE
"/home/synopsys1/19200536/DCNXT_2021.06/ref/tech/saed32nm_tf_itf_tluplus.map"   ;#  Mapping
file for TLUplus

return
```

Sửa lại xong rm_setup/common_setup.tcl bằng cách thêm đường dẫn đến các file và khởi động tool. Nhập source setup.tcl. **Tool báo successfully như hình bên dưới.**



Kiểm tra lại các setting trước đó bằng print các biến đã thiết lập dùng **printvar.**

***Print search path:**

dcnxt_shell-topo> printvar search_path
search_path = ". /home/0-SCDC-SHARE/0-Tools/syn/T-2022.03-SP4/libraries/syn /home/0-SCDC-SHARE/0-Tools/syn/T-2022.03-SP4/dw/syn_ver /home/0-SCDC-SHARE/0-Tools/syn/T-2022.03-SP4/dw/sim_ver /home/synopsys1/19200536/DCNXT_2021.06/ref/DBs /home/synopsys1/19200536/DCNXT_2021.06/ref/CLIBs /home/synopsys1/19200536/DCNXT_2021.06/ref/tech /home/synopsys1/19200536/DCNXT_2021.06/lab1/rtl /home/synopsys1/19200536/DCNXT_2021.06/lab1/scripts"

***Print link to library:**

dcnxt_shell-topo> printvar link_library
link_library = "* /home/synopsys1/19200536/DCNXT_2021.06/ref/DBs/saed32lvt_ss0p75v125c.db"
dcnxt_shell-topo>

***Print target library:**

dcnxt_shell-topo> printvar target_library
target_library = "/home/synopsys1/19200536/DCNXT_2021.06/ref/DBs/saed32lvt_ss0p75v125c.db"
dcnxt_shell-topo>

***Print current library:**

dcnxt_shell-topo> current_lib
TOP.dlib

***Check tlu file:**

```
dcnxt_shell-topo> check_tlu_plus_files

Sanity check for TLU+ vs MW-Tech files:
 max_tlu+: /home/synopsys1/19200536/DCNXT_2021.06/ref/tech/saed32nm_1p9m_Cmax.tluplus
 min_tlu+: **NONE**
 mapping_file: /home/synopsys1/19200536/DCNXT_2021.06/ref/tech/saed32nm_tf_itf_tluplus.map
 max_emul_tlu+: **NONE**
 min_emul_tlu+: **NONE**
 MW design lib: TOP.dlib

--------- Sanity Check on TLUPlus Files -------------
1. Checking the conducting layer names in ITF and mapping file ...
[ Passed! ]
2. Checking the via layer names in ITF and mapping file ...
[ Passed! ]
3. Checking the consistency of Min Width and Min Spacing between MW-tech and ITF ...
[ Passed! ]
----------------- Check Ends ------------------
```

-

```
dcnxt_shell-topo> check_tlu_plus_files

Sanity check for TLU+ vs MW-Tech files:
 max_tlu+: /home/synopsys1/19200536/DCNXT_2021.06/ref/tech/saed32nm_1p9m_Cmax.tluplus
 min_tlu+: **NONE**
 mapping_file: /home/synopsys1/19200536/DCNXT_2021.06/ref/tech/saed32nm_tf_itf_tluplus.map
 max_emul_tlu+: **NONE**
 min_emul_tlu+: **NONE**
 MW design lib: TOP.dlib

--------- Sanity Check on TLUPlus Files -------------
1. Checking the conducting layer names in ITF and mapping file ...
[ Passed! ]
2. Checking the via layer names in ITF and mapping file ...
[ Passed! ]
3. Checking the consistency of Min Width and Min Spacing between MW-tech and ITF ...
[ Passed! ]
----------------- Check Ends ------------------
```

Task 2: Read the Design into DC NXT Memory

***Read và kiểm tra file RTL Verilog và VHDL**

-

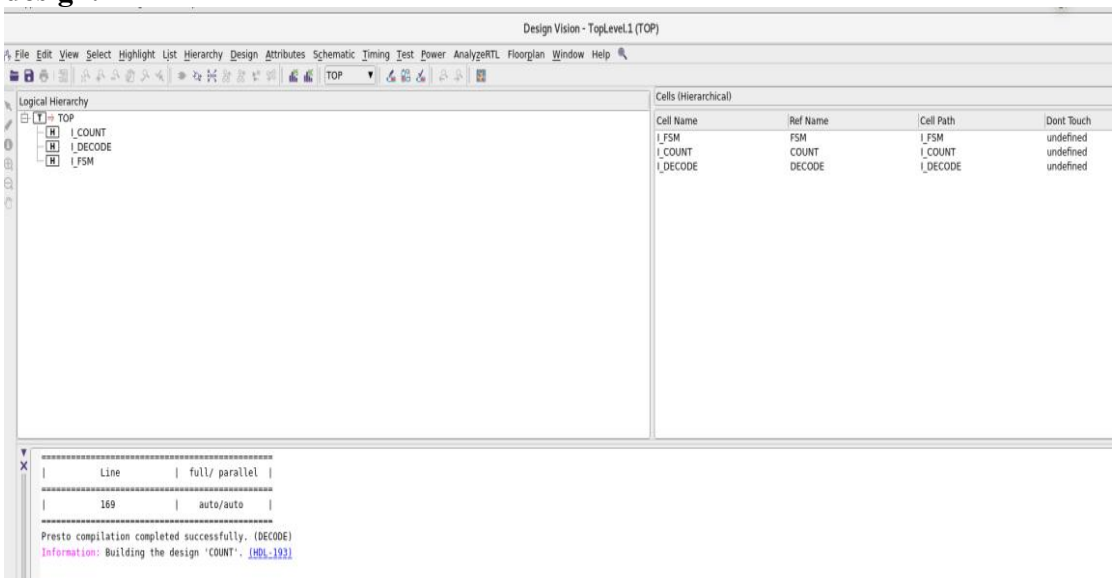
```
dcnxt_shell-topo> analyze -f verilog TOP.v
Running PRESTO HDLC
Compiling source file /home/synopsys1/19200536/DCNXT_2021.06/lab1/rtl/TOP.v
Presto compilation completed successfully.
Loading db file '/home/synopsys1/19200536/DCNXT_2021.06/ref/DBs/saed32lvt_ss0p75v125c.db'
1
```

```
dcnxt_shell-topo> analyze -f vhdl TOP.vhd
Running PRESTO HDLC
Compiling Package Declaration MYTYPES
Compiling Package Body MYTYPES
Compiling Entity Declaration TOP
Compiling Architecture STRUCT of TOP
Compiling Entity Declaration DECODE
Compiling Architecture RTL of DECODE
Compiling Entity Declaration FSM
Compiling Architecture RTL of FSM
Compiling Entity Declaration COUNT
Compiling Architecture RTL of COUNT
Warning:  The entity 'TOP' has multiple architectures defined. The last defined architecture 'STRUCT' will be used to build the design by default. (VHD-6)
Warning:  The entity 'DECODE' has multiple architectures defined. The last defined architecture 'RTL' will be used to build the design by default. (VHD-6)
Warning:  The entity 'FSM' has multiple architectures defined. The last defined architecture 'RTL' will be used to build the design by default. (VHD-6)
Warning:  The entity 'COUNT' has multiple architectures defined. The last defined architecture 'RTL' will be used to build the design by default. (VHD-6)
Presto compilation completed successfully.
```

***Load và link tới RTL dùng** *Eleborate TOP*

```
================================================
|           Line           |  full/ parallel  |
================================================
|           169            |    auto/auto     |
================================================
Presto compilation completed successfully. (DECODE)
Information: Building the design 'COUNT'. (HDL-193)

Inferred memory devices in process
        in routine COUNT line 279 in file
                '/home/synopsys1/19200536/DCNXT_2021.06/lab1/rtl/TOP.vhd'.
=============================================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
=============================================================================================
|      PCint_reg      | Flip-flop |   8   |  Y  | N  | N  | N  | N  | N  | N  |
=============================================================================================
Presto compilation completed successfully. (COUNT)
1
Current design is 'TOP'.
dcnxt_shell-topo>
```

***Sau khi load được cửa sổ hiện TOP design và design của các khối trong TOP design.**



*** List design**

```
dcnxt_shell-topo> list_designs
COUNT   DECODE  FSM     TOP (*)
1
```

*** List library**

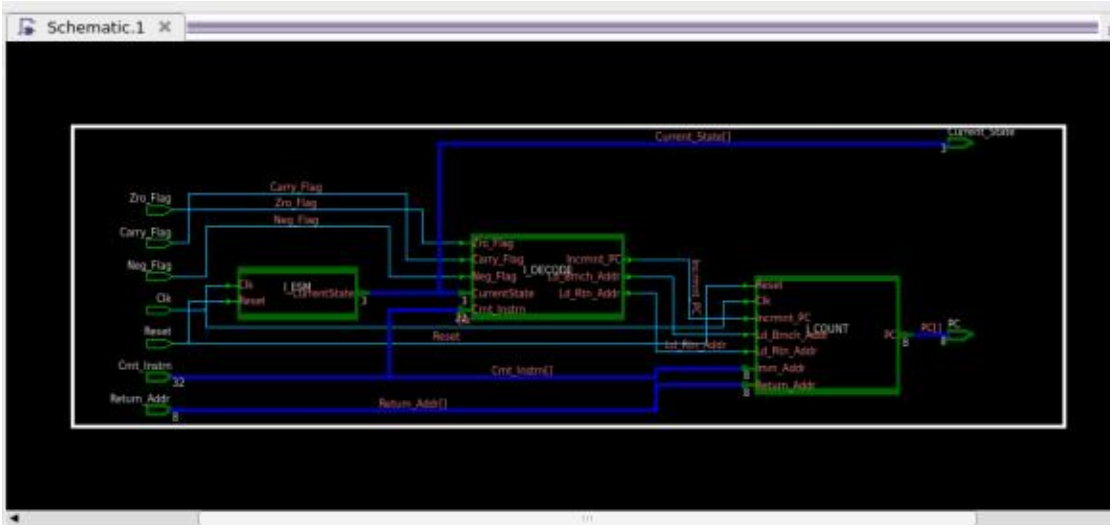
```
dcnxt_shell-topo> list_libs
Logical Libraries:
---------------------------------------------------------------------
Library         File                  Path
-------         ----                  ----
  saed32lvt_ss0p75v125c saed32lvt_ss0p75v125c.db
/home/synopsys1/19200536/DCNXT_2021.06/ref/DBs
  gtech         gtech.db              /home/0-SCDC-SHARE/0-Tools/syn/T-2022.03-
SP4/libraries/syn
  standard.sldb standard.sldb         /home/0-SCDC-SHARE/0-Tools/syn/T-2022.03-
SP4/libraries/syn
1
```

***Save unmapped design in ddc format**

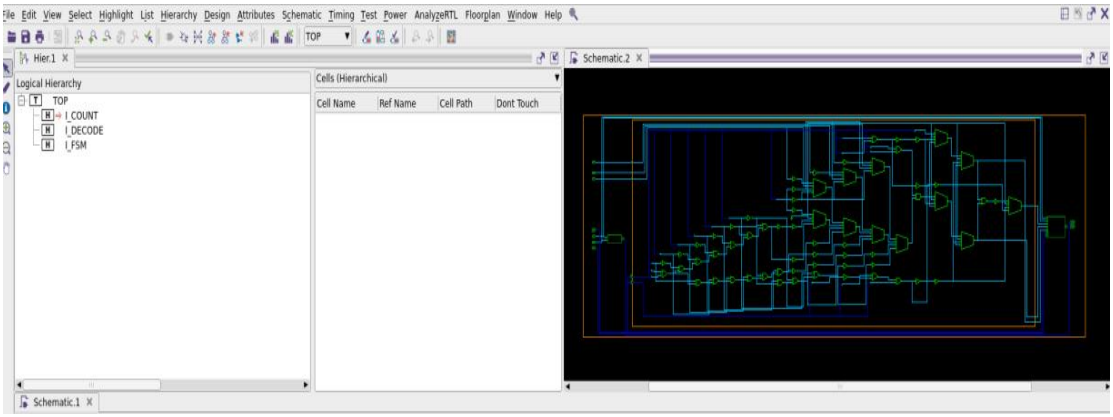
```
dcnxt_shell-topo> write_file -hier -f ddc -output ./unmapped/TOP.ddc
Writing ddc file './unmapped/TOP.ddc'.
```

Task 3: Explore the Schematic View

***Schematic View của TOP design gồm các khối nhỏ ở trong.**

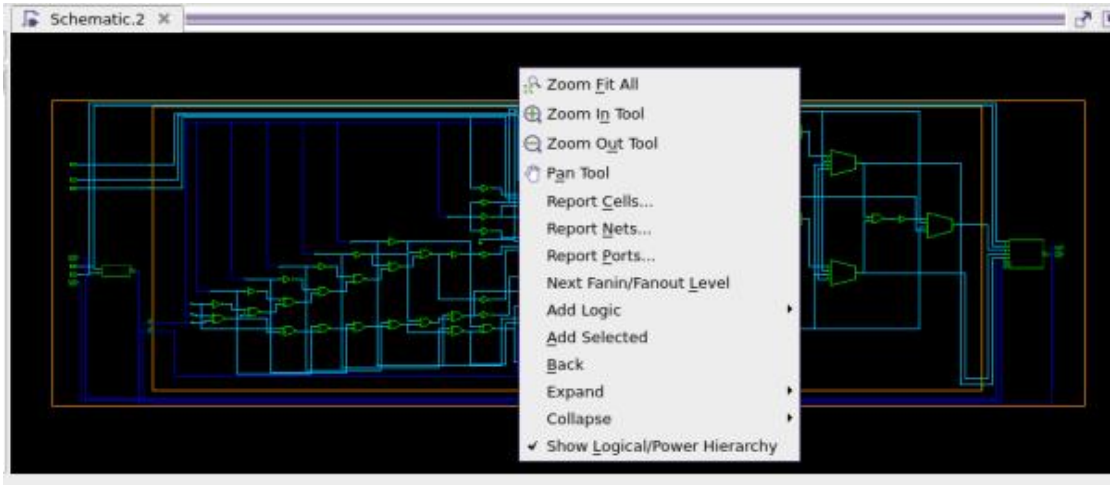


***Bấm vào khối design nhỏ thấy được các cổng logic.**



Task 4: Explore the Mouse Functions

***Bấm chuột phải để zoom in hoặc zoom out design.**



Task 5: Setting Preferred Routing Direction.

***Define routing theo kiểu Horizontal theo các lớp lẻ và Vertical cho các lớp chẵn giúp quá trình routing được dễ dàng khi nối các block lại với nhau không bị trùng và giảm crosstalk.**

```
dcnxt_shell-topo> set_preferred_routing_direction \-layers {M1 M3 M5 M7 M9} \-direction \horizontal
Information: linking reference library : /home/synopsys1/19200536/DCNXT_2021.06/ref/CLIBs/saed32_lvt.ndm. (PSYN-878)
Warning: Default routing directions were assigned to all the layers. (DCT-306)

  Linking design 'TOP'
  Using the following designs and libraries:
  --------------------------------------------------------------------------
  * (4 designs)              /home/synopsys1/19200536/DCNXT_2021.06/lab1/TOP.db, etc
  saed32lvt_ss0p75v125c (library) /home/synopsys1/19200536/DCNXT_2021.06/ref/DBs/saed32lvt_ss0p75v125c.db

1
Current design is 'TOP'.
```

```
dcnxt_shell-topo> set_preferred_routing_direction \-layers {M1 M3 M5 M7 M9} \-direction vertical
Warning: Mismatch in the preferred routing direction for metal layer M1 between the library and the design. (DCT-351)
Warning: Mismatch in the preferred routing direction for metal layer M3 between the library and the design. (DCT-351)
Warning: Mismatch in the preferred routing direction for metal layer M5 between the library and the design. (DCT-351)
Warning: Mismatch in the preferred routing direction for metal layer M7 between the library and the design. (DCT-351)
Warning: Mismatch in the preferred routing direction for metal layer M9 between the library and the design. (DCT-351)
Warning: All metal layers have the same preferred routing direction. (PSYN-884)
1
```

Task 6: Apply Timing Constraints.

*Verify current library kiểm tra có phải là TOP design.

dcnxt_shell-topo> current_design
Current design is 'TOP'.
{TOP}

*Apply timing constraint tới TOP design.

dcnxt_shell-topo> source TOP.con
Current design is 'TOP'.
Warning: The driving cell SDFFARX2_LVT has multiple outputs, -pin is required. (UID-989)
1

Task 8: Generate Reports and Analyze Timing

*Run rc để report violating constraints, kết quả báo không có violated.

Rc

dcnxt_shell-topo> rc
Information: Updating design information... (UID-85)

****
Report : constraint
    -all_violators
Design : TOP
Version: T-2022.03-SP4
Date   : Thu Jan 4 17:23:30 2024
****

This design has no violated constraints.

1
Current design is 'TOP'.

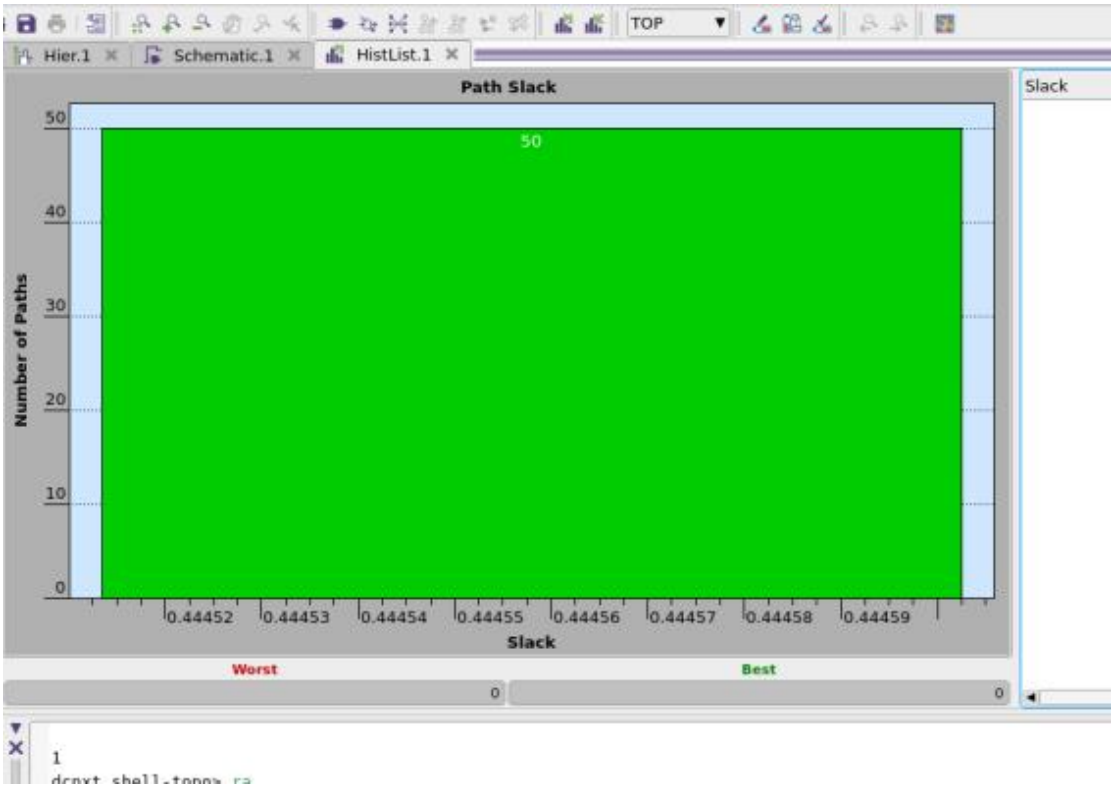
*Run rt để report timing, như hình kết quả bên dưới Slack MET nghĩa là không có vi phạm về timing.

```
dcnxt_shell-topo> rt

****************************************
Report : timing
         -path full
         -delay max
         -max_paths 1
Design : TOP
Version: T-2022.03-SP4
Date   : Thu Jan  4 17:23:56 2024
****************************************

Operating Conditions: ss0p75v125c   Library: saed32lvt_ss0p75v125c

  Startpoint: Neg_Flag (input port clocked by Clk)
  Endpoint: I_COUNT/PCint_reg[0]
            (rising edge-triggered flip-flop clocked by Clk)
  Path Group: Clk
  Path Type: max

  I_COUNT/C96/Z_0 (*SELECT_OP_2.8_2.1_8)                  0.00       1.36 r
  I_COUNT/C98/Z_0 (*SELECT_OP_2.8_2.1_8)                  0.00       1.36 r
  I_COUNT/PCint_reg[0]/next_state (**SEQGEN**)            0.00       1.36 r
  data arrival time                                                  1.36

  clock Clk (rise edge)                                   2.00       2.00
  clock network delay (ideal)                             0.00       2.00
  clock uncertainty                                      -0.20       1.80
  I_COUNT/PCint_reg[0]/clocked_on (**SEQGEN**)            0.00       1.80 r
  library setup time                                      0.00       1.80
  data required time                                                 1.80
  --------------------------------------------------------------------------
  data required time                                                 1.80
  data arrival time                                                 -1.36
  --------------------------------------------------------------------------
  slack (MET)                                                        0.44


1
dcnxt_shell-topo>
```

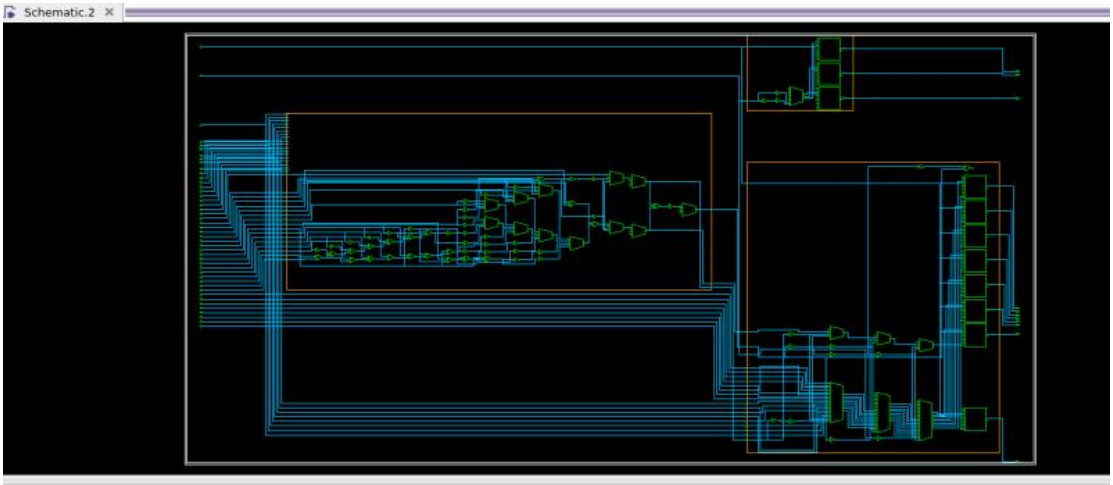
***Run ra để report area, total area là 51.85**

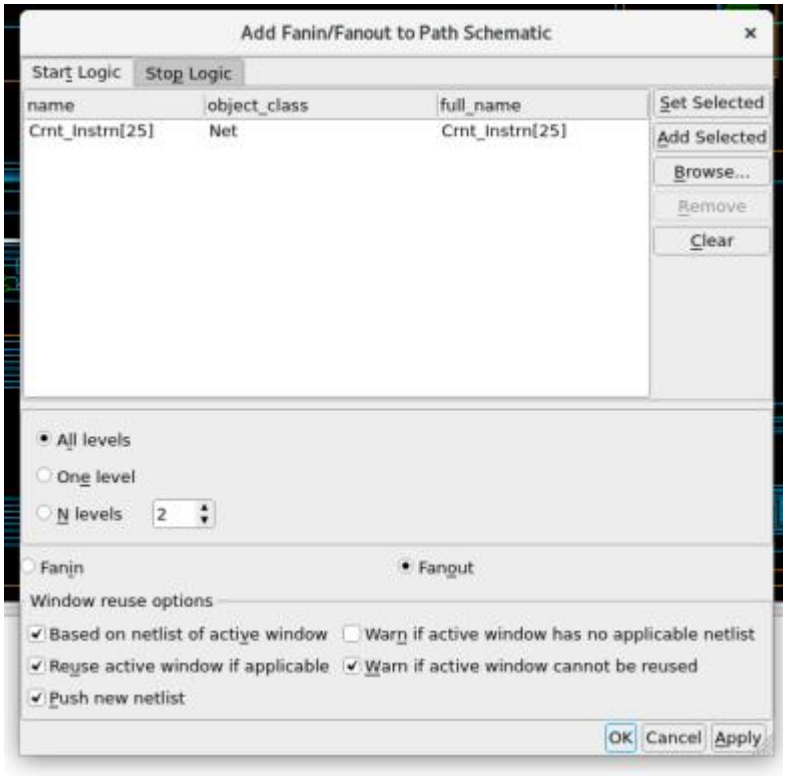
```
dcnxt_shell-topo> ra

****************************************
Report : area
Design : TOP
Version: T-2022.03-SP4
Date   : Thu Jan  4 17:25:02 2024
****************************************

Library(s) Used:

    gtech (File: /home/0-SCDC-SHARE/0-Tools/syn/T-2022.03-SP4/libraries/syn/gtech.db)

Number of ports:                          164
Number of nets:                           298
Number of cells:                          139
Number of combinational cells:             98
Number of sequential cells:                31
Number of macros/black boxes:               0
Number of buf/inv:                         58
Number of references:                       3

Combinational area:                0.000000
Buf/Inv area:                      0.000000
Noncombinational area:             0.000000
Macro/Black Box area:              0.000000
Net Interconnect area:            51.859260

Total cell area:                   0.000000
Total area:                       51.859260
```

***Create path Slack histogram**



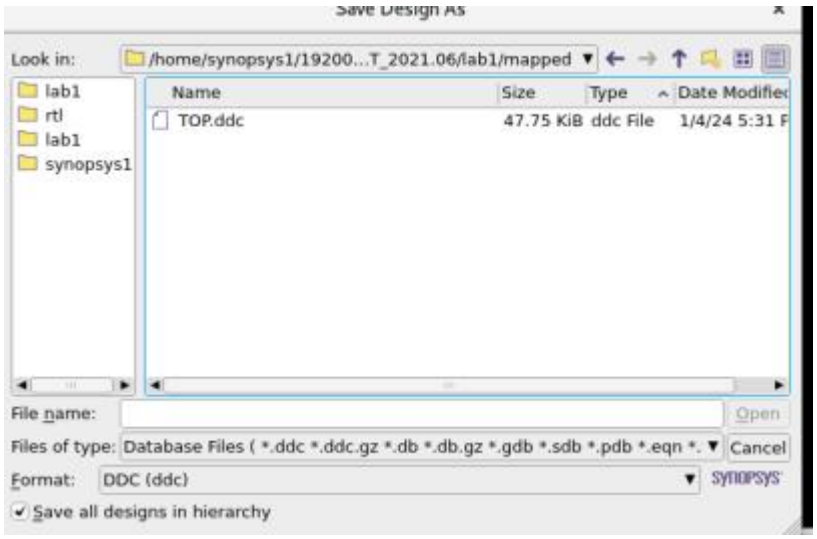
***Create fanin và fanout**





Task 9: Save the Optimized Design

***Save TOP.ddc.**



***Save ASCII output files cần cho ICC2.**

```
dcnxt_shell-topo> write_icc2_files -output ./mapped/TOP_icc2
Using operating conditions 'ss0p75v125c' found in library 'saed32lvt_ss0p75v125c'.
Information: There is no user-defined operating conditions in the design. The tool is inferring operating conditions 'ss0p75v125c' from the library 'saed32lvt_ss0p75v125c'. (OCT-399)
1
```

Task 10: Remove Designs and Exit Design Vision

***Remove all file với fr.**

```
1
dcnxt_shell-topo> fr
Removing physical design 'TOP'
Removing design 'TOP'
Removing design 'FSM'
Removing design 'DECODE'
Removing design 'COUNT'
1
```