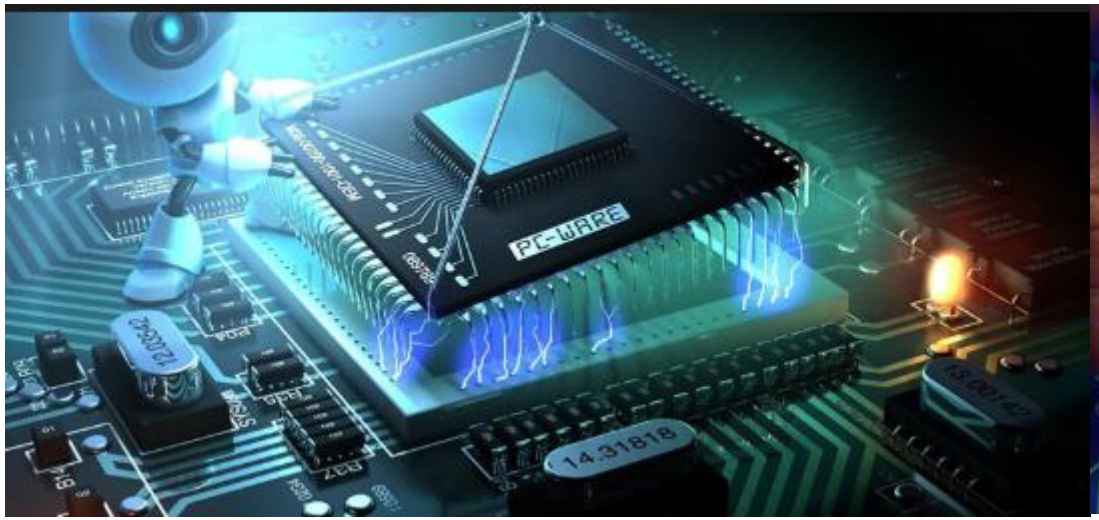


Basics of standard cells

Presentation topics

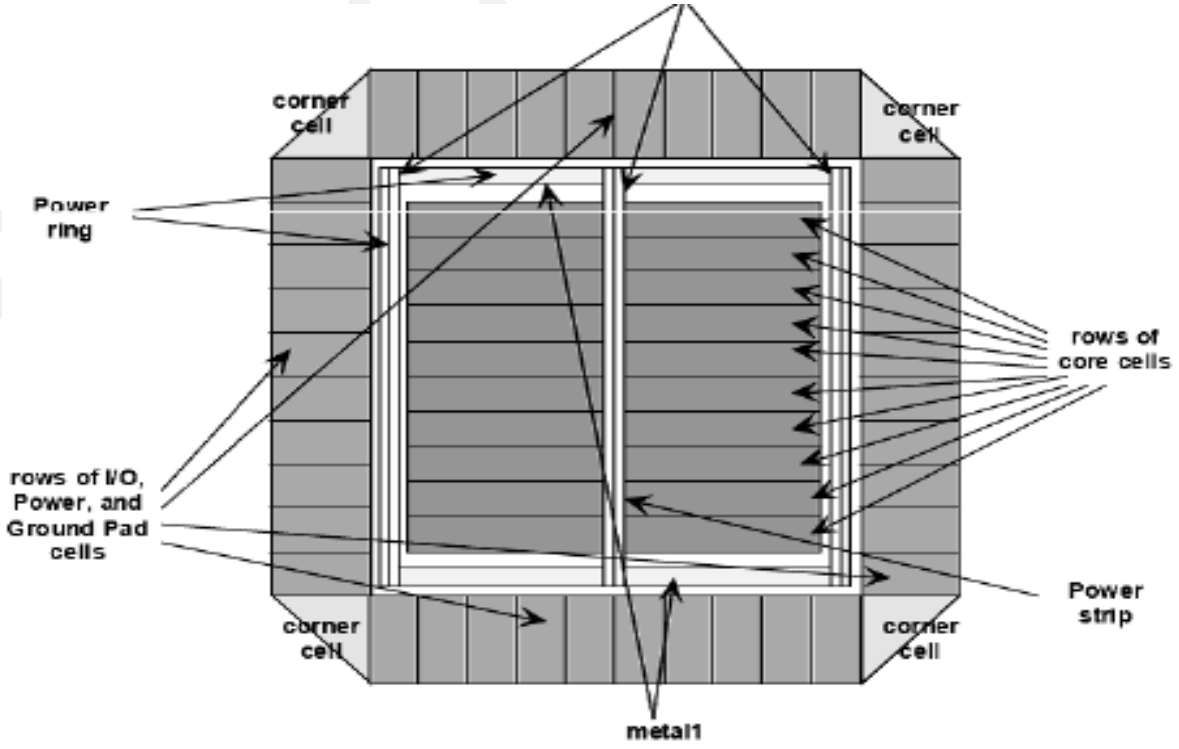
- Need for standard cell libraries
- Categories of cells in standard cell libraries
- Standard cell layout design considerations
- Layout grid settings
- Cell documentation

Introduction

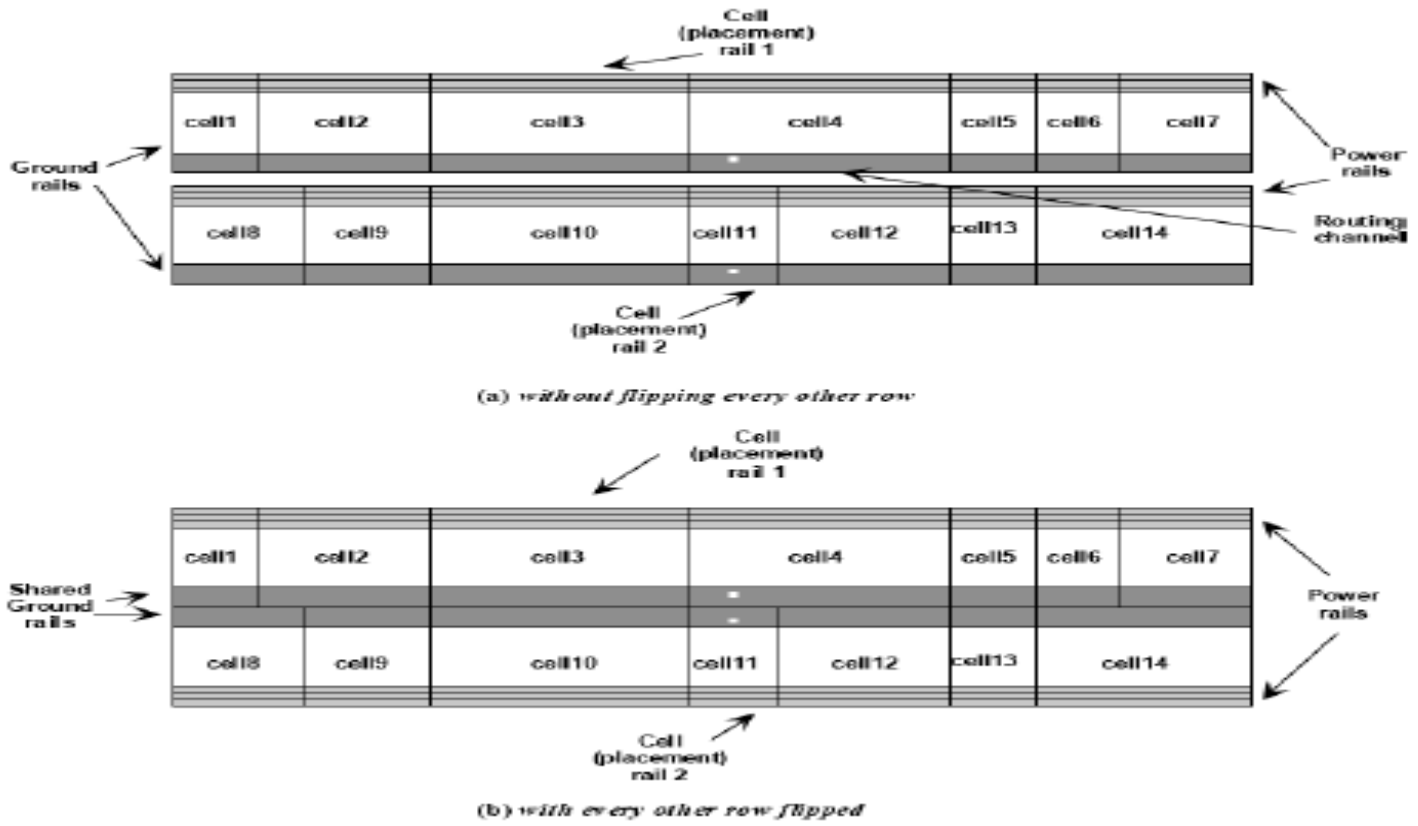
- Standard Cell Libraries:
  - Standard cells are the building blocks in an ASIC design
  - "standard" because of common interface and regular structure
  - Basic cells: inverters, NANDs, NORs, flip-flops, etc.
  - It is desirable to expand library with different variants of the basic cells.
    - For example, basic inverter, 2x inverter, 4x inverter, etc.
  - when automatic synthesis is used, then a larger variety of cells allows the tool more degrees of freedom to optimize a design.

Complete Cell Based Chip

- Core (logic) cells
- Corner cells
- Pad cells (I/O, Power, Ground)



Flipping and Abutment



Abutment

The requirement that cells can be abutted horizontally means that all cells:

- Must have the “same height” or “integer multiple of unit site”
- Must have their VDD and ground rails on the same y-coordinate
- Must have well regions at the same y coordinate, in case the wells also get abutted. This applies to substrate tie / contact wells as transistor wells
- Note that ***abutment occurs when power and ground rails get abutted***

Categories of cells in Standard Cell Libraries

- Negative unate logic cells
- Positive unate logic cells
- Arithmetic cells
- Sequential cells
- Special cells
- Inverted input cells

Drive Strength

Definition : - Drive strengths in a typical standard cell Library.

* X1
* X2
* X4
* X8
* X16
* X32
* X64

X1 may mean a drive strength of 1 i.e. capability to drive a load of say,50fF.

Cell Categories

- Combinational logic
- Sequential cells
- Datapath cells
- Special cells

Combinational Logic

- Inverters
- Buffers
- Tri-state buffers
- Tri-state buffer with enable
- AND (2~4 inputs) gates
- OR (2~4 inputs) gates
- NAND 2(2~4 inputs) gates
- NOR (2~3 inputs) gates
- XOR (2~4 inputs) gates
- XNOR (2~4 inputs) gates

Combinational Logic

- Mux (2~4 inputs) gates
- Full-adder blocks
- Half-adder blocks
- And-Or and Or-And combination gates
- And-Or-Invert (AOI) and Or-And-Invert(OAI) gates

Note:- Each and every cell has more than 1 different driving strength present in the library.

Sequential Cells

- Latch cells.
- Flip-flop cells.
- Scan-able flip-flop cells.

Sequential Cells

Latch cells

– High active with set/reset

– High active with set

– High active with reset

– High active without set or reset

– Low active with set/reset

– Low active with set

– Low active with reset

– Low active without set or reset

Scan flip-flop cells

– Each flip-flop cell listed in the “Flip-Flop Cells” section has a respective version that can be scanned

Sequential Cells

Flip-Flop cells

– Positive edge / Negative edge triggered

– Positive edge / Negative edge triggered with asynchronous set/reset

– Positive edge / Negative edge triggered with asynchronous set

– Positive edge / Negative edge triggered with asynchronous reset

– Positive edge / Negative edge triggered with synchronous set/reset

– Positive edge / Negative edge triggered with synchronous set

– Positive edge / Negative edge triggered with synchronous reset

– Enable flip-flop triggered without asynchronous set/reset

– Enable flip-flop triggered with asynchronous set/reset

– Enable flip-flop triggered with asynchronous set

– Enable flip-flop triggered with asynchronous reset

– Enable flip-flop triggered with synchronous set/reset

– Enable flip-flop triggered with synchronous set

– Enable flip-flop triggered with synchronous reset

Datapath Cells

Full Adder

– 1-bit full adder with inverting carry-in

– 1-bit full adder with inverting carry-out

– 1-bit full adder with carry-out selection

Special Half Adder

– 1-bit half adder with inverting carry-in

– 1-bit half adder with inverting carry-out

Booth Encoder

Booth operator

Compressor cells

Special Cells

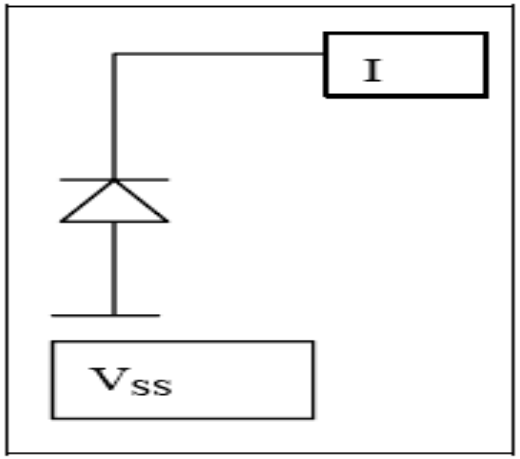
- Clock gating cell
- Antenna fix cell
- Balanced clock cells
- Delay insertion cells
- Tie-high and tie-low cells
- Filler (feed through) cells
- De-coupling cells

Special Cells

Clock-gating cell - Used for reducing power in register banks, by disabling clock toggle during certain cycles

Antenna fix cell - This issue has been considered intensely in 0.18 µm and lower technologies

- Two approaches to solve antenna violations *metal change* and *diode addition*



Special Cells

Balanced clock cells - The balanced clock cells have equal rise time and fall time to maintain the duty cycle in the clock tree

Delay insertion cells

Delay name	Delay value (ns)
DEL005	0.05
DEL01	0.1
DEL015	0.15
DEL02	0.2
DEL0	0.25
DEL1	0.5
DEL2	1.0
DEL3	1.5
DEL4	2.0

Special Cells

Tie-high and tie-low cells

- *tie-high cells* to tie any input to logic level of one (1) and *tie-low cells* to tie any input to a logic level of zero (0)
- Use these cells instead of direct connection to the power rails for better ESD protection

Filler (feed-through) cells

- Filler cells provide continuity for the VDD/VSS power rail, as well as for n-wells.

– Filler cells are used to fill the gap between adjacent cells in place and route tools.

Special Cells

Filler (feed-through) cells

Cell Name	Pitch number
FILL1	1
FILL2	2
FILL4	4
FILL8	8
FILL16	16
FILL32	32
FILL64	64

De-Coupling cells

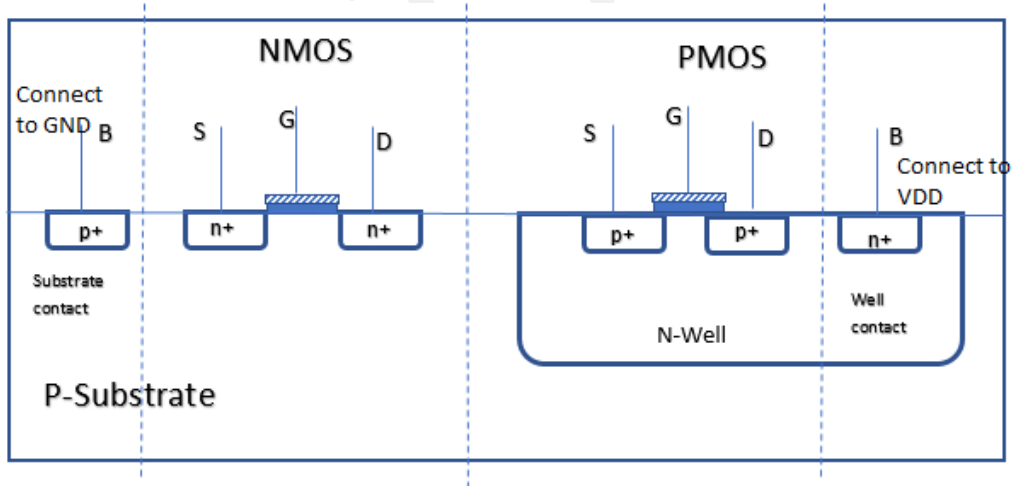
These cells are basically capacitors between power and ground, and can be used for switching noise reduction

Physical only cells in physical design

1. Well tap cells
2. Decap cells
3. Filler cells
4. Antenna cells
5. End cap cells
6. Tie High/Low cells

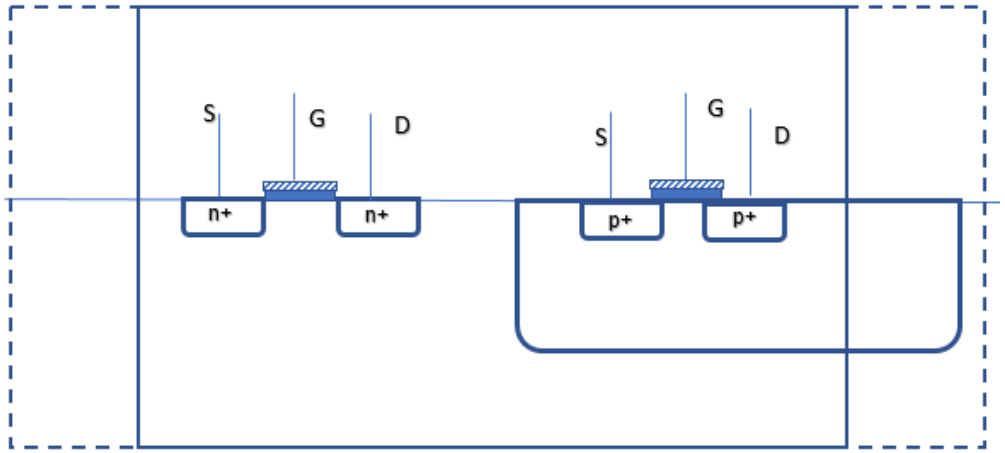
Well tap cells

1. Library cells usually have well taps which are traditionally used so that your n-well is connected to VDD and substrate is connected to GND
2. There will be bulk contacts for NMOS and PMOS to avoid latch up problems
3. Each and every standard cells present inside the digital library having these taps



Well tap cells

- We need only one VDD tap per NWELL (Standard cell row) and single substrate connection
- With tapless library + Well tap cells , Significant area reduction , in turn improves area gain in physical design



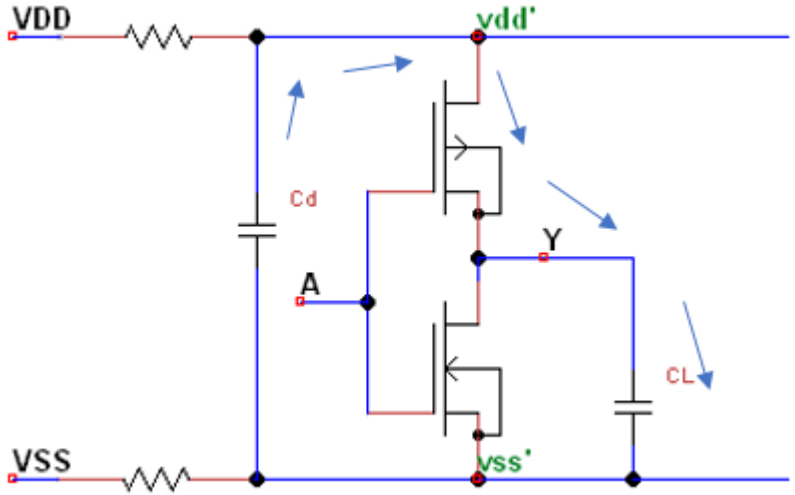
- Single nwell/Substrate tap in a row can cause the latch up problem due to high well/Substrate resistance

Well tap cells

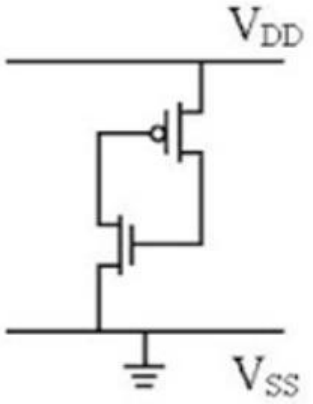
- Well tap cells are added for regular interval with checkboard fashion

Decap cells (Decoupling capacitor)

- Decap cells acts as a local reservoir for providing the charges for surrounding cells to decrease the dynamic IR drop
- Decap cells doesn't have functionality and it has a impact on leakage power



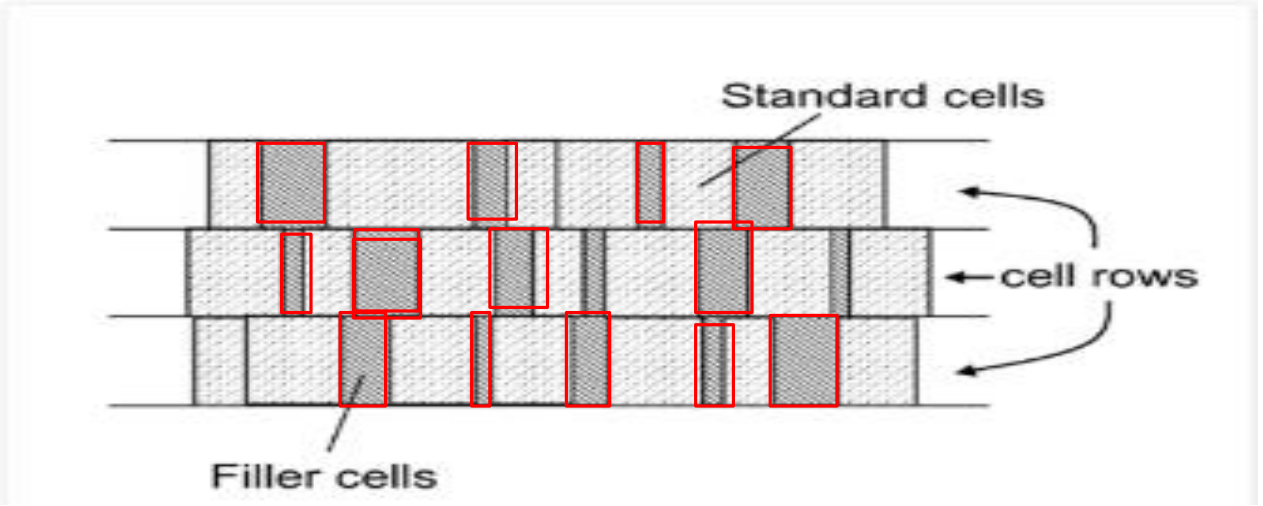
Decap capacitor formation inside inverter



DECAP cell

Filler cells

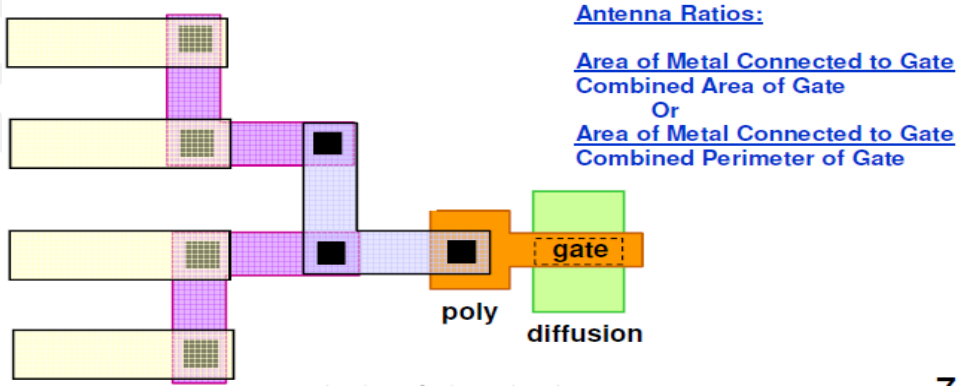
- Filler cells are used to connect the gaps between the cells after placement
- Filler cells are used to establish the continuity of the N- well and the implant layers on the standard cell rows, some of the small cells also don't have the bulk connection (substrate connection) because of their small size (thin cells)
- Filler cells should be added without missing to avoid large base DRC's



Antenna effect

Antenna effect:- Collect charge at polysilicon or metal structures from the processing environment (e.g., reactive ion etch) and develop potentials sufficiently large to cause Fowler Nordheim current to flow through the thin oxide

- The "Antenna Rules" deal with process induced gate oxide damage caused when exposed polysilicon and metal structures connected to a thin oxide transistor
- **Antenna Rules:-** As length of wire increases during processing, the voltage stressing the gate oxide increases. Antenna rules define acceptable length of wires

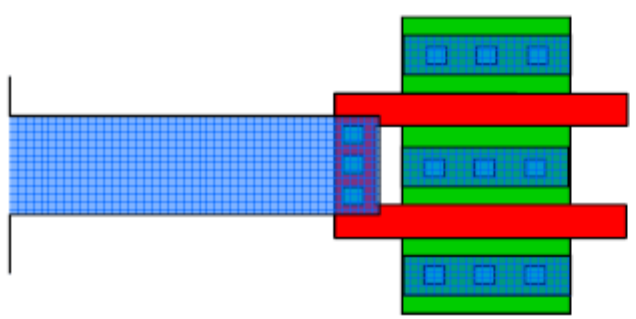


Antenna effect

- The gate of a small MOSFET is tied to a metal 1 interconnect having a large area

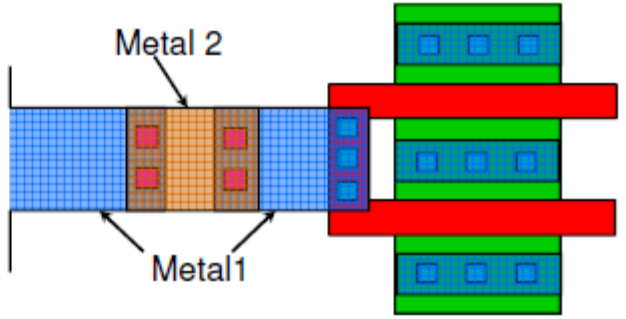
– During the etching of metal 1, the metal area acts as an “antenna,” collecting ions and rising in potential

– The gate oxide breaks down during fabrication



(a)

Layout is susceptible to antenna impact

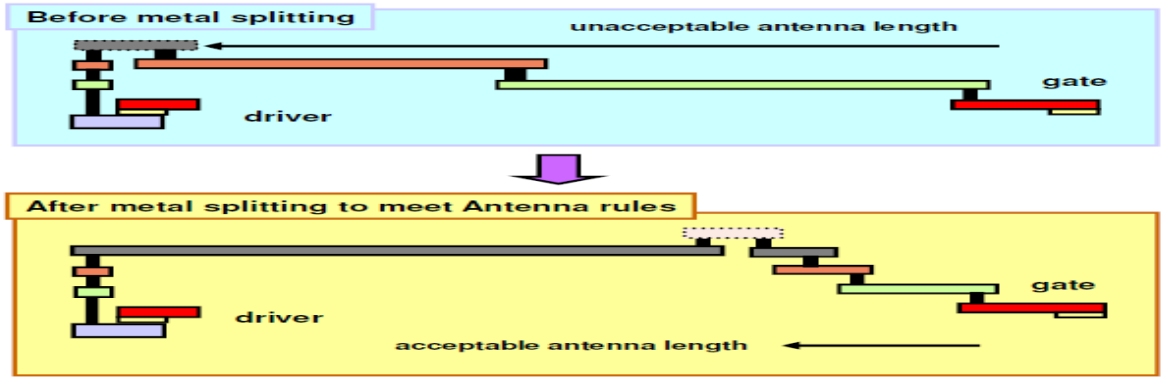


(b)

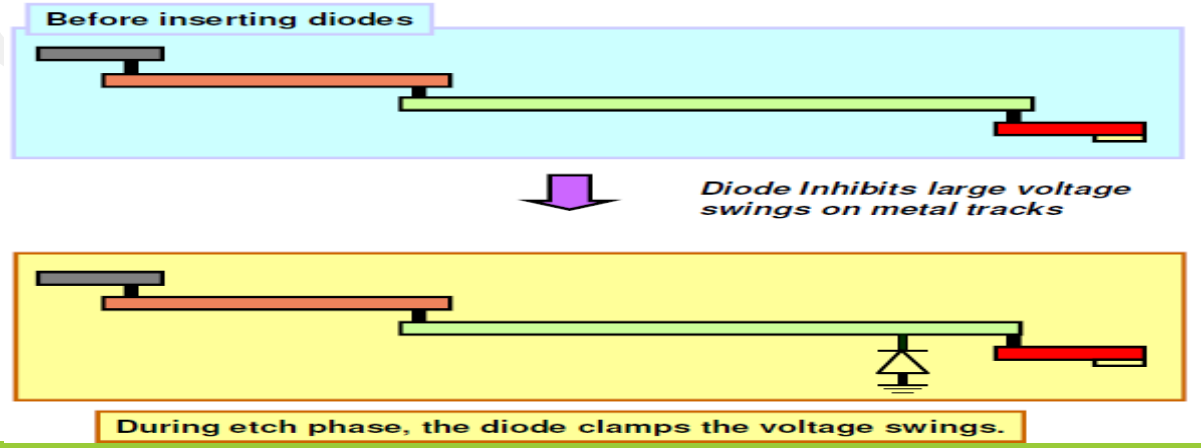
Discontinuity in metal 1 layer to avoid antenna effect

Ways to fix antenna effect

1. Layer hopping/Layer jumping

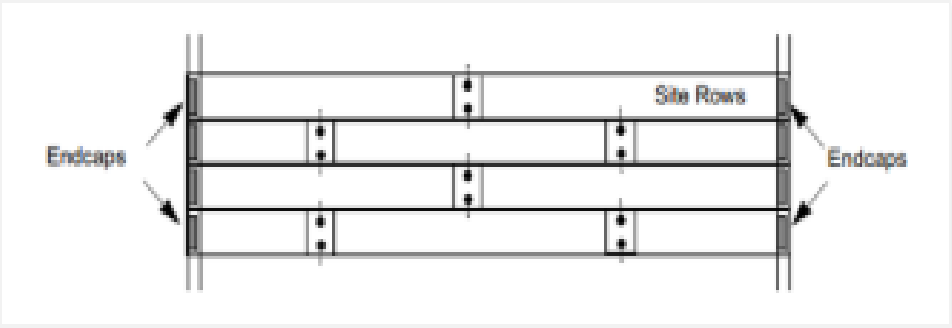


2. Antenna diodes



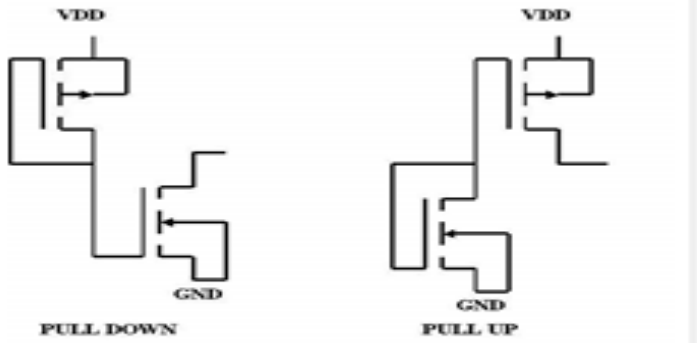
END cap cells

- END cap cells are added to know the end of the row
- These cells are added at both ends of rows



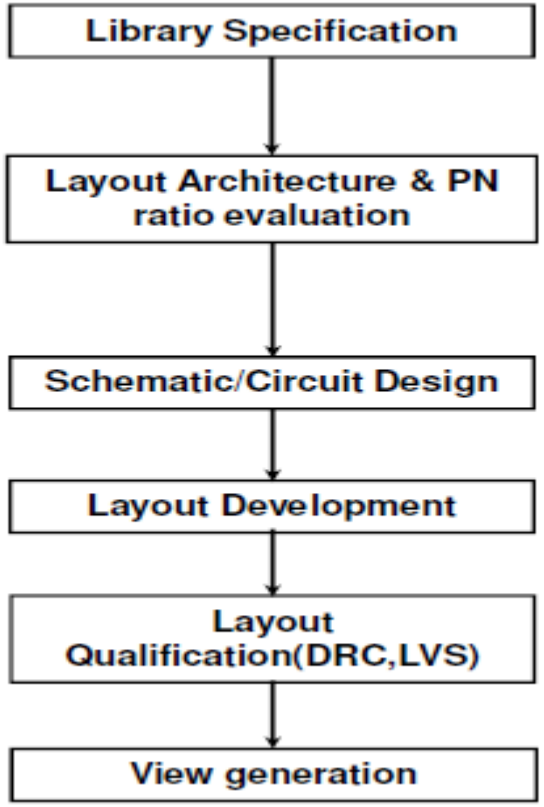
Tie High/Tie low cells

- Tie-high and Tie-Low cells are used to connect the gate of the transistor to either power or ground
- In Lower technology nodes, if the gate is connected to power/ground the transistor might be turned on/off due to power or ground bounce
- The cells which require Vdd (Typically constant signals tied to 1) connect to Tie high cells The cells which require Vss/Gnd (Typically constant signals tied to 0) connect to Tie Low cells



Tie cells

Standard cell Library Development Flow



Quality Metrics

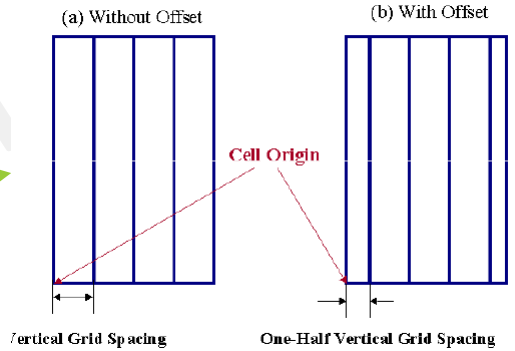
- Once the essential requirements have been met and/or we become experienced in doing layout, so that we can anticipate and potentially plan ahead for these advanced requirements:

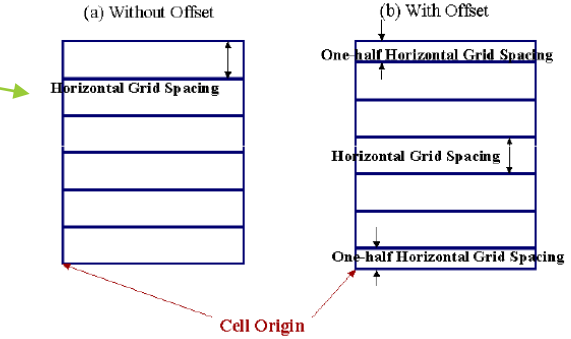
1. Area
2. Performance
3. Manufacturability
4. Maintainability
5. Reliability over the long term (i.e., electro migration)

Etc

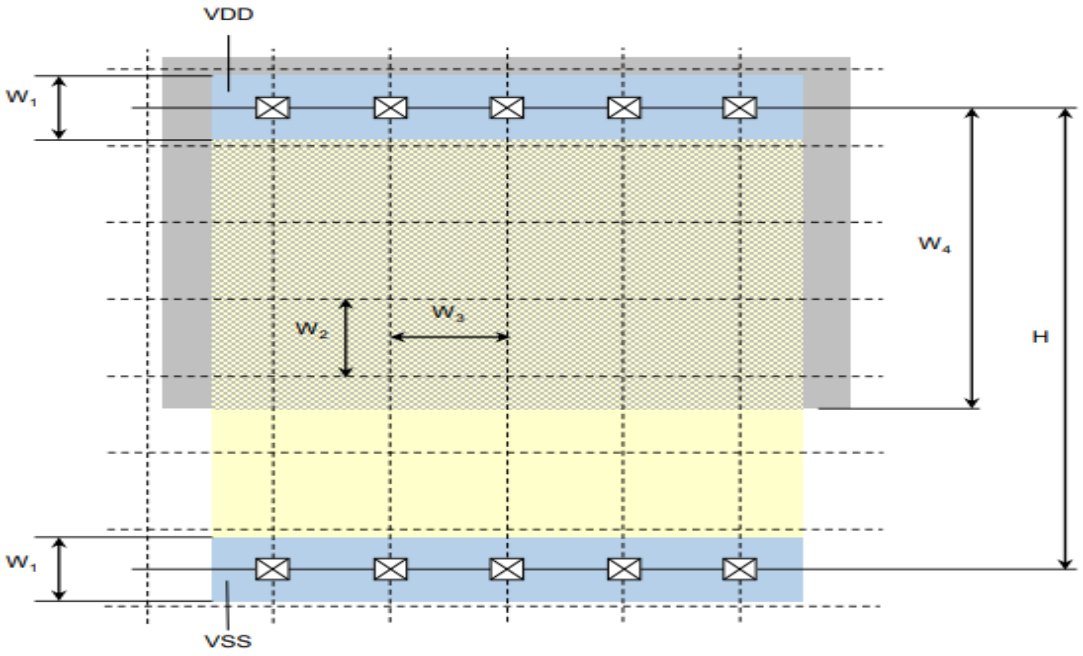
Layout Specifications

1. Drawn Gate Length
2. Layers of Metal
3. Layout Grid
4. Vertical Pitch Grid
5. Horizontal Pitch Grid
6. Cell height (track)
7. Power and Ground Rail width





- Cell height is measured in Tracks
  - A Track is one M1 pitch
  - E.g., An 8-Track Cell has room for 8 horizontal M1 wires.

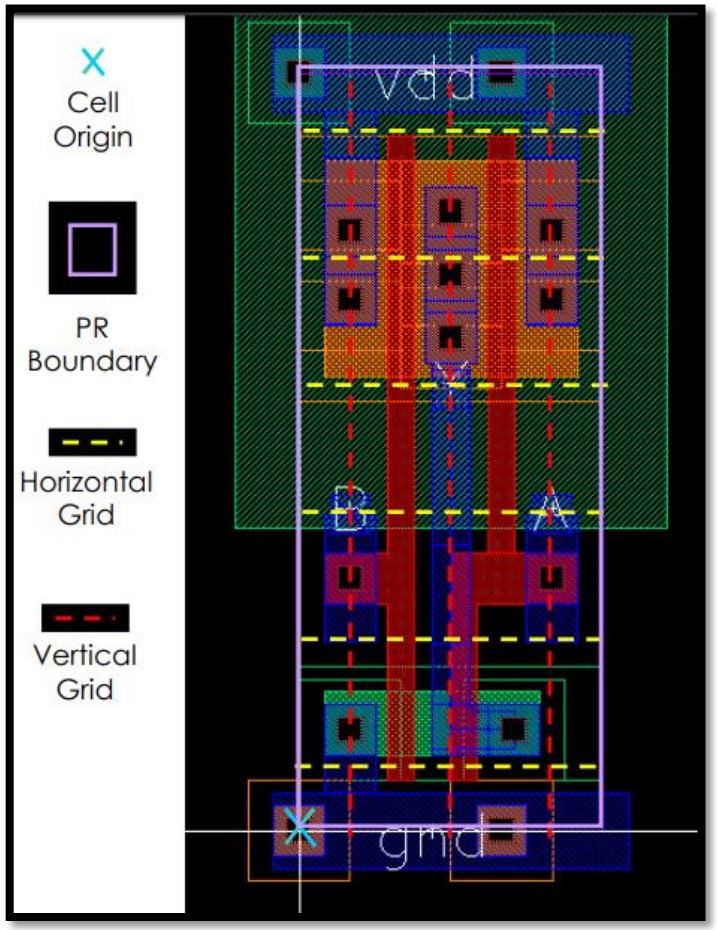


Parameter	Symbol
Cell height (# tracks)	H
Power rail width	W_1
Vertical grid	W_2
Horizontal grid	W_3
N-Well height	W_4

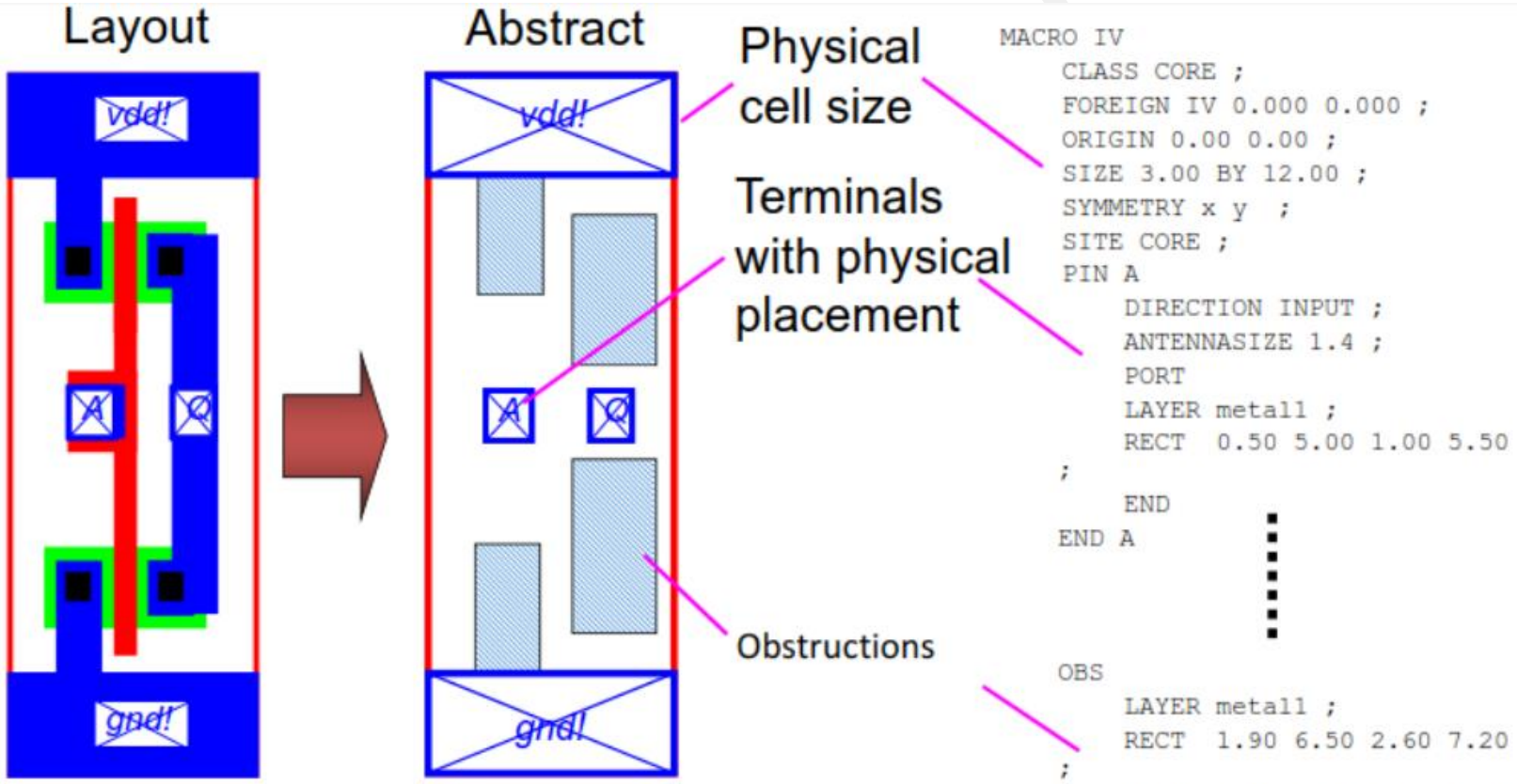
- The more tracks, the wider the transistors, the faster the cells.
  - 7-8 low-track libraries for area efficiency
  - 11-12 tall-track libraries for performance, but have high leakage
  - 9-10 standard-track libraries for a reasonable area-performance tradeoff

- Cells must fit into a predefined grid
  - ✓ The minimum Height X Width is called a SITE.
  - ✓ Must be a multiple of the minimum X-grid unit and row height.
  - ✓ Cells can be double-height, for example.

- Pins should coincide with routing tracks
  - ✓ This enables easy connection of higher metals to the cell.



What is inside the .lef ?




```
MACRO IV
    CLASS CORE ;
    FOREIGN IV 0.000 0.000 ;
    ORIGIN 0.00 0.00 ;
    SIZE 3.00 BY 12.00 ;
    SYMMETRY x y  ;
    SITE CORE ;
    PIN A
        DIRECTION INPUT ;
        ANTENNASIZE 1.4 ;
        PORT
        LAYER metal1 ;
        RECT  0.50 5.00 1.00 5.50
    ;
        END
    END A

    OBS
        LAYER metal1 ;
        RECT  1.90 6.50 2.60 7.20
    ;
        RECT  0.40 4.90 1.00 5.60
    ;
```

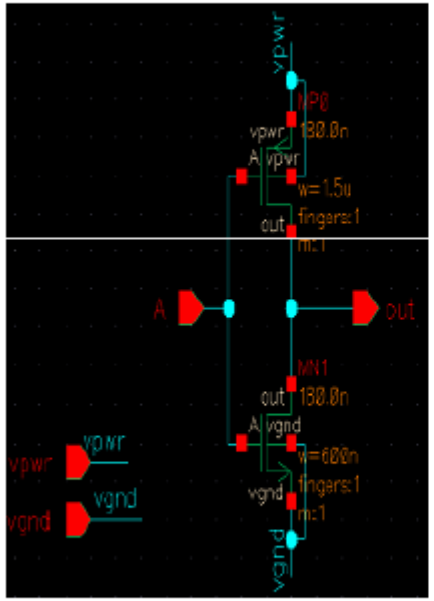
Operating Specifications

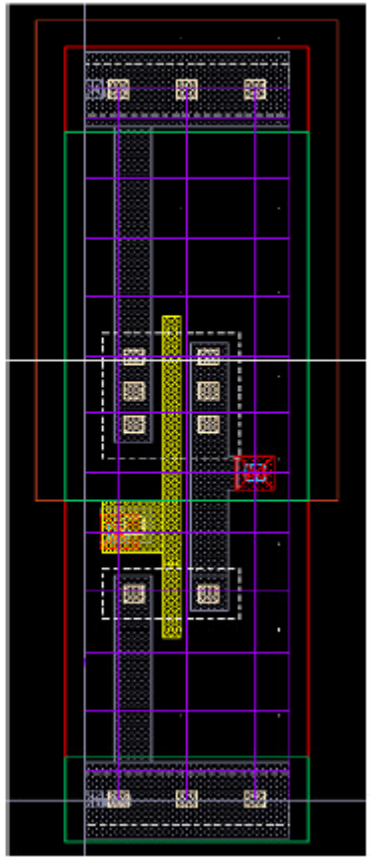
- Operating Conditions
- Leakage Power Conditions,
- Multiple -Voltage Conditions
- Temperature Inversion Conditions.
- Main operating conditions (Example TSMC90nm)

Corner Condition	Process		Voltage	Temperature
	PMOS	NMOS		
Worst	Slow	Slow	0.9*Vdd	125°C
Typical	Typical	Typical	Vdd	25°C
Best	Fast	Fast	1.1*Vdd	0°C
Low Temperature	Fast	Fast	1.1*Vdd	-40°C

Sample layout for inverter

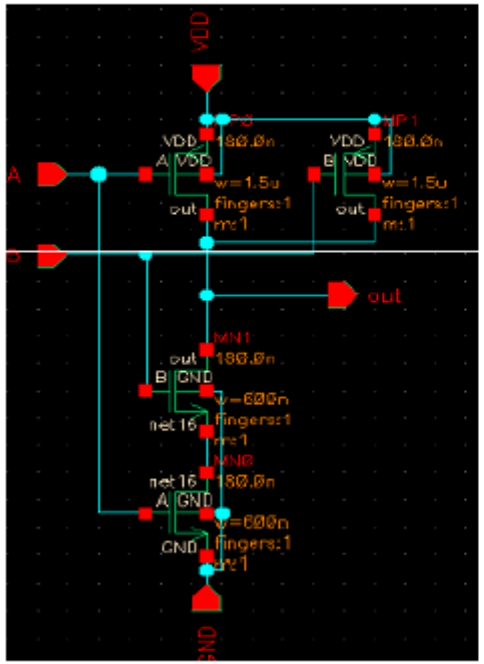
Inverter

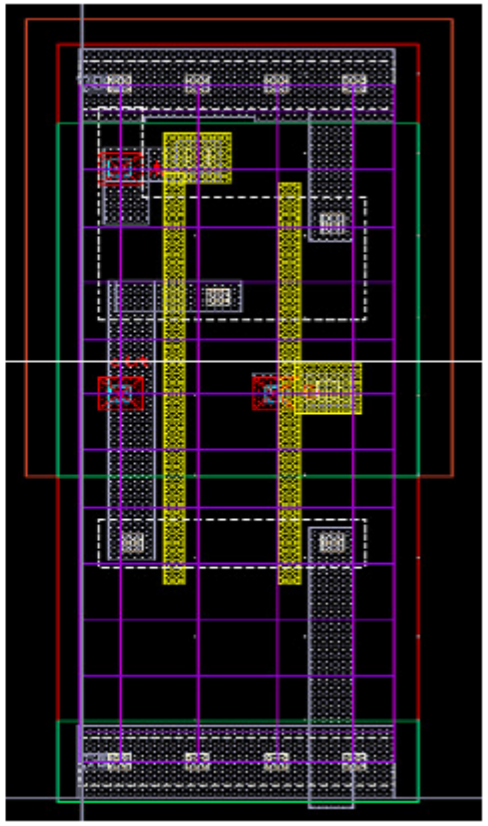




Standard Cell for NAND Gate

2 input NAND Gate





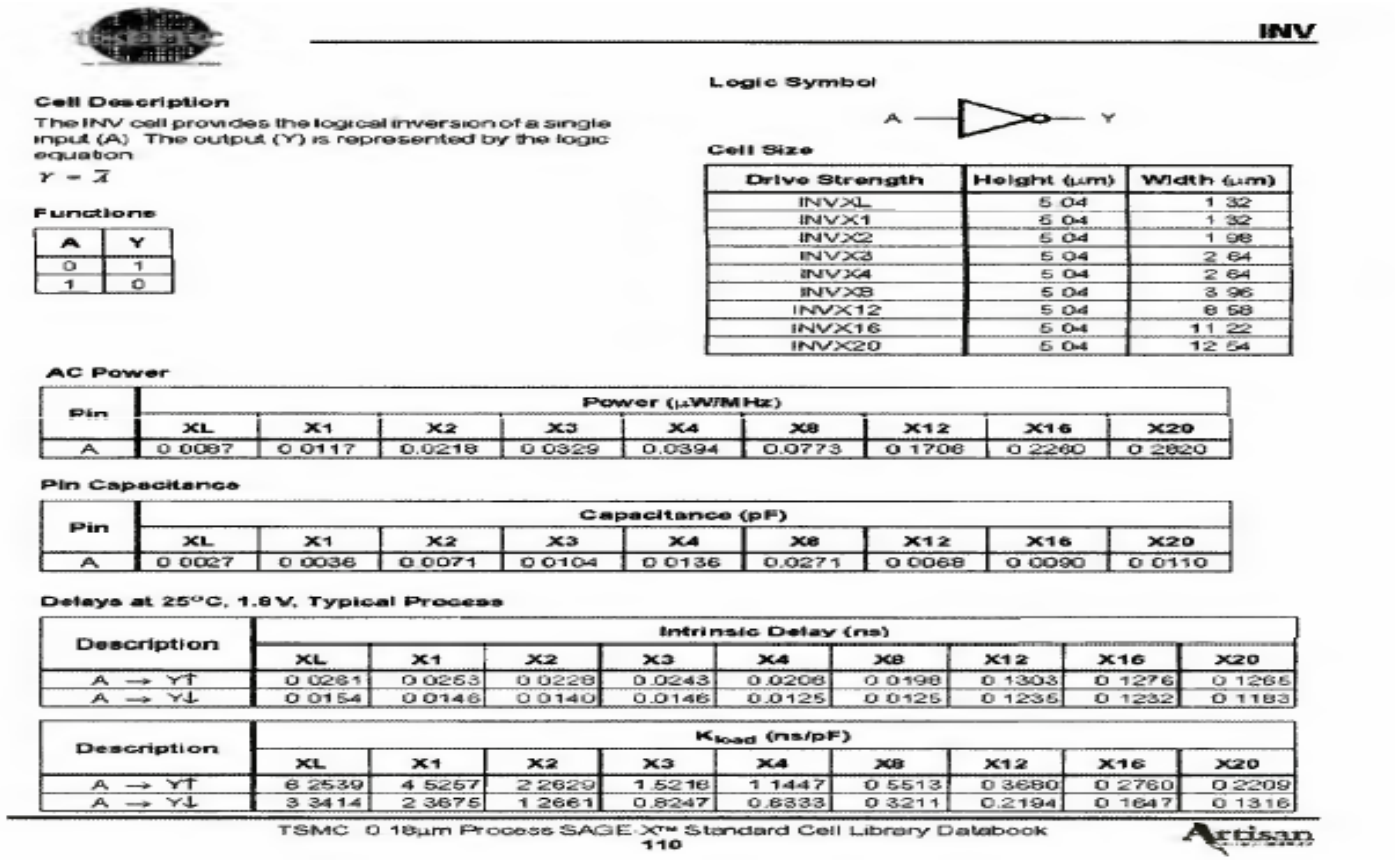
Standard Cell Documentation

- Documentation of a standard cell is nothing but creating a file which consists all the information about that particular cell
- It is required ,as it becomes easy for any designer to collect the required data of that cell

The documentation file consists :

- Logic symbol
- Inputs & outputs
- Load details
- Capacitance details
- Library file used
- Truth table
- Layout
- Transistor level diagram
- Characterization data
- P/N ratio

Inverter



INV

Cell Description

The INV cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation

$Y = \overline{A}$

Functions

A	Y
0	1
1	0

Logic Symbol

A — Y

Cell Size

Drive Strength	Height (µm)	Width (µm)
INVXL	5 04	1 32
INVX1	5 04	1 32
INVX2	5 04	1 98
INVX3	5 04	2 64
INVX4	5 04	2 64
INVX8	5 04	3 96
INVX12	5 04	6 58
INVX16	5 04	11 22
INVX20	5 04	12 54

AC Power

Pin	Power (µW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0 0087	0 0117	0.0218	0 0329	0.0394	0.0773	0 1706	0 2260	0 2820

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0 0027	0 0036	0 0071	0 0104	0 0136	0.0271	0 0068	0 0090	0 0110

Delays at 25°C, 1.8V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0 0261	0 0253	0 0228	0.0243	0.0208	0 0198	0 1303	0 1276	0 1265
A → Y↓	0 0154	0 0146	0 0140	0.0146	0.0125	0 0125	0 1235	0 1232	0 1183

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	6 2539	4 5257	2 2629	1 5216	1 1447	0 5513	0 3680	0 2760	0 2209
A → Y↓	3 3414	2 3675	1 2661	0.8247	0.6333	0 3211	0.2194	0 1647	0 1316


THANKS