Making the Most of the Am186™ER or Am188™ER Microcontroller

AMD

Application Note

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The AMD® Am186™ER and Am188™ER microcontrollers provide a major advancement in systems integration by bringing 32 Kbyte of zero-wait-state RAM onto the microcontroller. This incorporation of system-level RAM onto the controller brings the advantages of reduced system cost, reduced power consumption, and smaller board size. With these advantages comes the challenge of utilizing this new resource to the greatest advantage in a given system. This application note describes how to use an internal chip select to access the internal RAM of the Am186ER controller, and the debugging support provided by the processor for code or data located in this internal RAM. All references in the document to the Am186ER apply equally to the Am188ER microcontroller.

OVERVIEW OF AM186ER CONTROLLER

The 80186 microcontroller and its derivative parts continue to be popular in embedded applications. AMD has been a leader in the continuing development of the 186 with its Am186 product line. AMD's most recent addition to the Am186 family is the Am186ER microcontroller. The Am186ER microcontroller is a direct descendent of the popular Am186EM microcontroller, which was introduced in 1994.

Like the Am186EM microcontroller, the Am186ER microcontroller provides 12 external chip-selects signals, a demultiplexed address bus, 3 timers and a watchdog timer, an asynchronous serial port, a synchronous serial interface, 5 external interrupt pins, 2 DMA channels, and 32 programmable input/output pins. In addition, the Am186ER provides 32 Kbyte of internal, zero-wait-state RAM, and a 4x clock mode. The Am186ER microcontroller is available in speeds up to 40 MHz in a 100-pin PQFP or TQFP package at 3 V with 5-V tolerant I/O.

MEMORY AND CHIP SELECT CONFIGURATIONS

The internal RAM of the Am186ER microcontroller is accessed via an internal chip select. The function of this chip select is similar to the function of traditional 186 external chip selects. The use and configuration of the internal RAM must take place within the context of the total system. The final system configuration will be heavily dependent on the need for external memory or memory-mapped peripherals, and on the allocation of the external chip selects to access these devices. The chip select signals available on the Am186ER microcontroller are summarized in Table 1.

Table 1. Am186ER Microcontroller Chip Select Signals

Chip Select Name	Normal Usage	Number of Signals	Size (total for all associated signals)	Wait States	External Ready	Comments
$\overline{\text{UCS}}$ (Upper Chip Select)	ROM boot code	1	64 Kbyte to 512 Kbyte	From 0 to 3	Configurable to use or ignore external ready	Ending address is always at the top of memory (0xfffff)
$\overline{\text{LCS}}$ (Lower Chip Select)	RAM data	1	64 Kbyte to 512 Kbyte	From 0 to 3	Configurable to use or ignore external ready	Starting address is always at the bottom of memory (0x00000)
$\overline{\text{MCS}}$ (Middle Chip Selects)	Slow memory or memory mapped peripherals	4	8 Kbyte to 512 Kbyte	From 0 to 3	Configurable to use or ignore external ready	Base address must be multiple of total block size
$\overline{\text{PCS}}$ (Peripheral Chip Selects)	I/O or memory mapped peripherals	6	1536 byte	$\overline{\text{PCS}}$3-0 from 0 to 15 $\overline{\text{PCS}}$6-5 from 0 to 3	Configurable to use or ignore external ready	May be mapped to memory or I/O space; $\overline{\text{PCS}}$4 is not available
ICS	Internal RAM	1	32 Kbyte	0	Does not use external ready	Base address must be multiple of 32 Kbyte; not visible externally

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Figure I shows the most common type of memory configuration used with the Am186ER microcontroller. In this configuration, the $\overline{UCS}$ chip select is used to address FLASH or ROM memory which contains the application code. The internal RAM is placed at address 0x00000 and is used for data storage, including the interrupt vector table and the stack. The Peripheral Control Block, PCB, is a 256-byte block through which the on-chip peripheral registers are accessed. The PCB can be memory mapped or I/O mapped. In Figure 1, the PCB is memory-mapped to the memory addresses directly above the internal memory. Other peripheral devices are also memory-mapped using the peripheral chip select ($\overline{PCS}$) signals.

Figure1. 32 Kbyte RAM Configuration

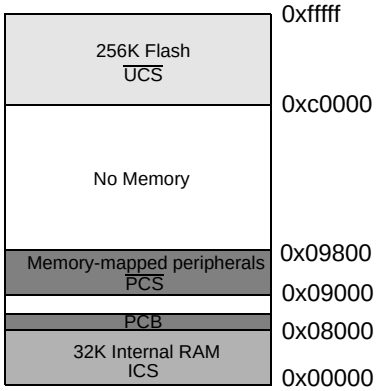
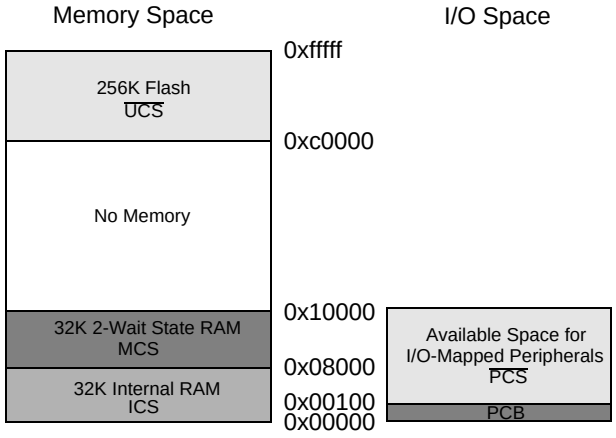


Figure 2 shows a system where 64 Kbyte of RAM is required. The fast internal memory is configured at address 0x00000 to support the interrupt vector table and probably the stack segment. Less frequently used data can be accessed via a slower RAM device enabled via the middle chip select ($\overline{MCS}$) signals. This configuration also demonstrates the ability to map the PCB and off-chip peripherals to I/O space.

Both configurations allow the data segment registers (DS and ES) to be set to address all data without needing to be reprogrammed. If set to 0, DS and ES can access from 0x00000 to 0x0ffff without modification. This allows quick access to all system data. In Figure 2, DS and ES cannot be used to access either the PCB or the I/O-mapped peripherals. These would need to accessed using the Am186ER I/O instructions IN and OUT and their variants, and the dx,ax register pair.

Figure 2. 64 Kbyte RAM Configuration



SETTING UP THE INTERNAL CHIP SELECT

In general, the internal chip select used to access the 32 Kbyte of internal RAM on the Am186ER microcontroller behaves much the same way as the traditional external chip selects. The internal RAM can be configured to be addressed anywhere within the Am186ER microcontroller's 1 Mbyte address space, but the base address must be a multiple of the 32-Kbyte block size. Since the memory being addressed is always guaranteed to respond with zero-wait-states, no wait-state or ready programming is required or provided. Figure 3 shows the Internal Memory Chip Select (IMCS) register and its fields.

The *BA*, or *Base Address*, field specifies bits 19-15 of the 20-bit base address of the internal memory space. Bits 14-0 of the 20-bit base address are zero. This allows the ICS space to be moved to any 32 Kbyte boundary throughout memory. A typical location for the ICS is at address 0x00000 so that it can be used to hold the interrupt vector table.

Overlap of the ICS with other chip selects is only supported if the overlapped chip select is programmed to zero wait-states and to ignore external ready. Overlapping the ICS with any chip select that does not meet these requirements results in unpredictable behavior of the part. If the ICS is overlapped with an external chip select, both chip-select signals will assert for cycles where they overlap. Since the write signals provided during an ICS cycle are exactly the same as those for an external cycle, the write will occur to both devices. On a read, only the data provided by the internal memory will be used by the processor.

Figure 3. The IMCS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA					SR	RE	Reserved								

The *SR*, or *Show Reads*, field can be used for debugging a system using the internal memory. When Show Reads is enabled, the SR bit is set, and the processor drives the data bus with the data read from the internal memory on read cycles. In this way, an emulator or logic analyzer can monitor the data read from the internal memory.

If the ICS is overlapped with another chip select, as discussed above, the external device must not drive data on the bus during read cycles if Show Reads is enabled. This would result in multiple devices driving the data bus. For this reason it is impractical to use the Show Read function with overlapping chip selects.

The *RE*, or *Ram Enable*, field actually enables the internal memory and the associated chip select. When RE is set, the ICS signal is enabled. Unlike the external chip selects, the ICS can be both enabled and disabled during the course of execution. This may be useful in the debug stage of the design.

DEBUG SUPPORT

The Am186ER microcontroller provides support for debugging code or data located in the internal RAM.

Writes to the internal RAM appear as normal Am186ER write cycles which can be viewed using a logic analyzer. The address being written to appears on the multiplexed Address/Data (AD) bus during the T1 clock cycle and on the non-multiplexed Address (A) bus during the second half of T4 through the first half of the following T4 cycle. The data being written into the internal RAM will be present on the AD bus during T2 through T4. This behavior is identical to writes to external zero-wait-state memory, although no external chip select will assert for internal memory writes. A typical write cycle is shown in Figure 4.

Reads from the internal RAM appear as normal Am186ER read cycles. No external chip select will assert for internal memory reads. However, with external memory reads, the external device drives the data onto the AD bus late in T3. For the internal RAM, no external device is placing the data on the bus for the read. The processor drives the data on the internal bus but, in normal operation, the data is not visible externally. This reduces power consumption and noise generation. However, the Internal Chip Select can be configured to drive the data read from the internal RAM out on the Address/Data bus late during T3 via the Show Reads feature discussed above. A normal external memory read cycle is shown in Figure 5. Figure 6 shows a read cycle to the internal memory, and Figure 7 shows a read cycle to internal memory with the Show Reads function enabled.

The Show Reads function allows the use of a logic analyzer for debugging, allowing the viewing of data read from the ICS address range. It also allows emulators to monitor the values written to and read from the internal memory. The Show Reads mode can be entered via software by setting the Show Read bit in the IMCS register. Some emulators may force the processor into Show Read mode by holding the $\overline{\text{SREN}}$ pin low during RESET.

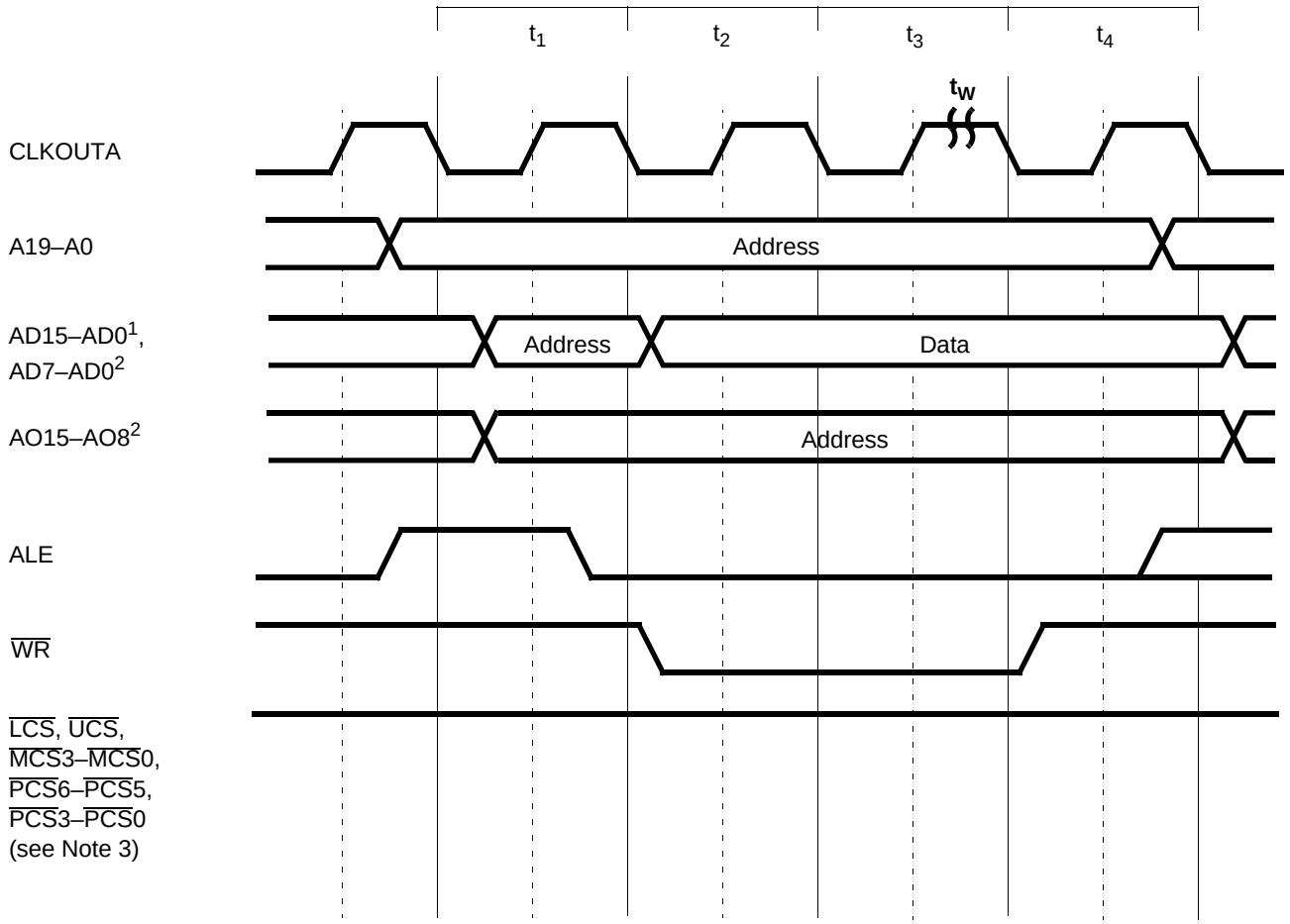
Further support for emulators is provided through the $\overline{\text{IMDIS}}$ pin. When this pin is held low during RESET, the internal memory is disabled regardless of the setting of the RAM Enable (RE) bit in the IMCS register. This allows the use of emulator overlay memory for the programmed ICS accesses without any modification to existing code.

An additional debug mode is available on the Am186ER microcontroller by overlapping the ICS address range with that of a programmed chip select, for example $\overline{\text{LCS}}$. This allows ICS accesses to be signaled externally by the $\overline{\text{LCS}}$ chip select. When used with the Show Reads feature, this allows a logic analyzer to show all data transfers to and from the internal memory. When using this mode, there must be no external memory device attached to the overlapped chip select, or bus contention can result. In addition, the overlapped chip select must be programmed to zero wait-states and to ignore external ready.

SUMMARY

The Am186 family continues to expand, providing new functionality and solutions relevant to the changing nature of embedded applications. The Am186ER microcontroller builds on the popularity of the Am186EM microcontroller by providing the same peripherals and the same pin-out as that part but with the addition of 32 Kbyte of zero-wait-state internal RAM. The Am186ER microcontroller allows many systems to function without any external RAM. Due to the highly integrated nature of the device, it is possible to have a complete system consisting of nothing more than an Am186ER microcontroller and a single external Flash device.

Figure 4. ICS Write Cycle Waveforms



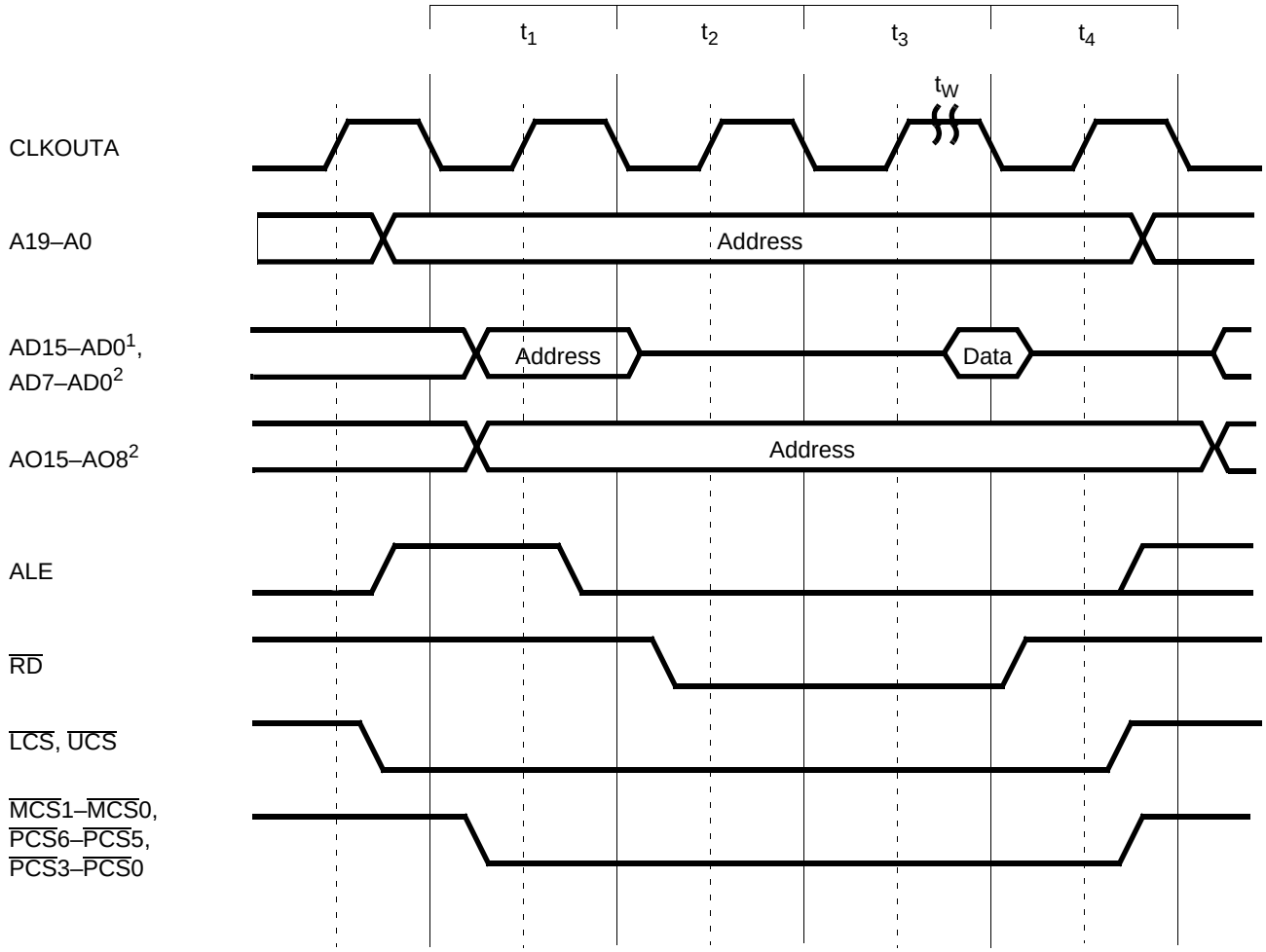
Notes:

1 – Am186ER microcontroller only

2 – Am188ER microcontroller only

3 – External chip selects will only assert for internal RAM accesses if they are programmed to overlap with the ICS address space.

Figure 5. External Memory Read Cycle Waveforms

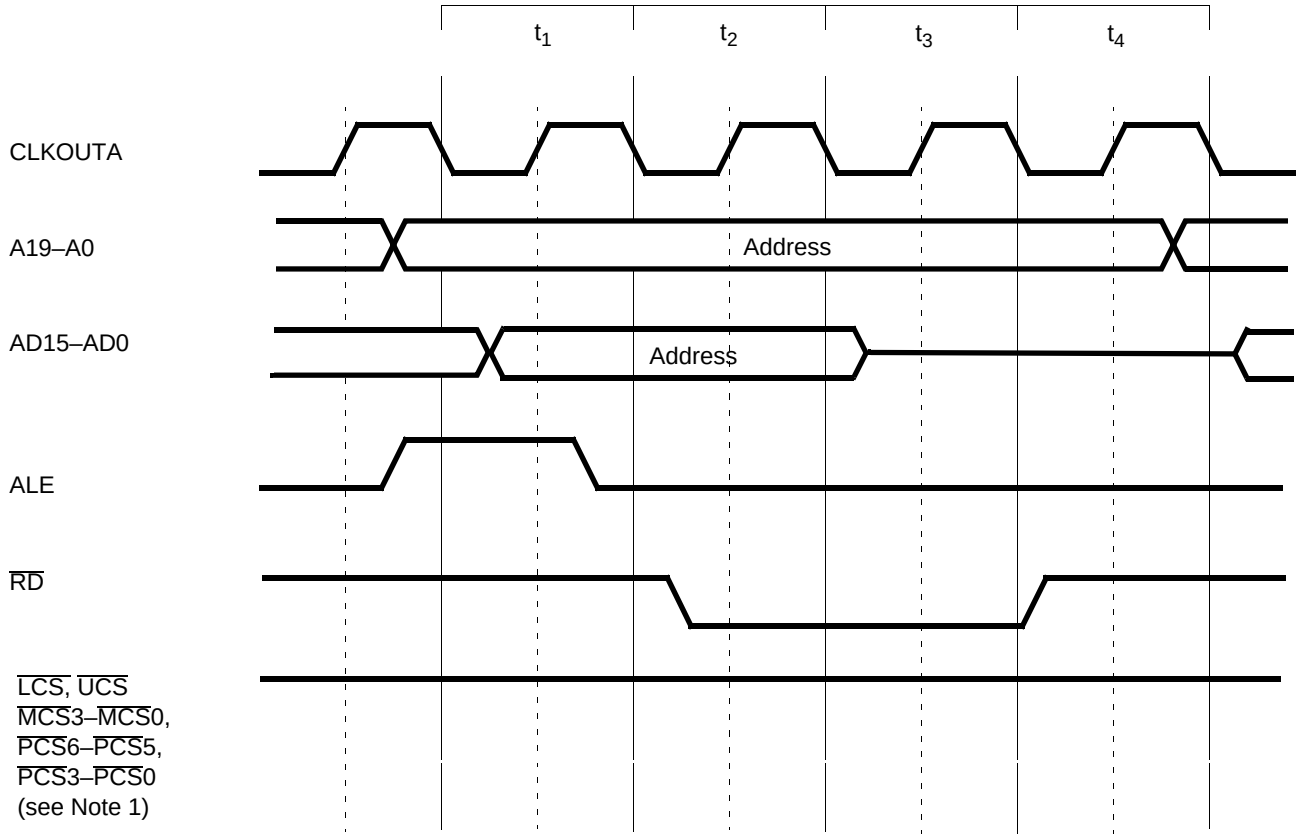


Notes:

1 – Am186ER microcontroller only

2– Am188ER microcontroller only

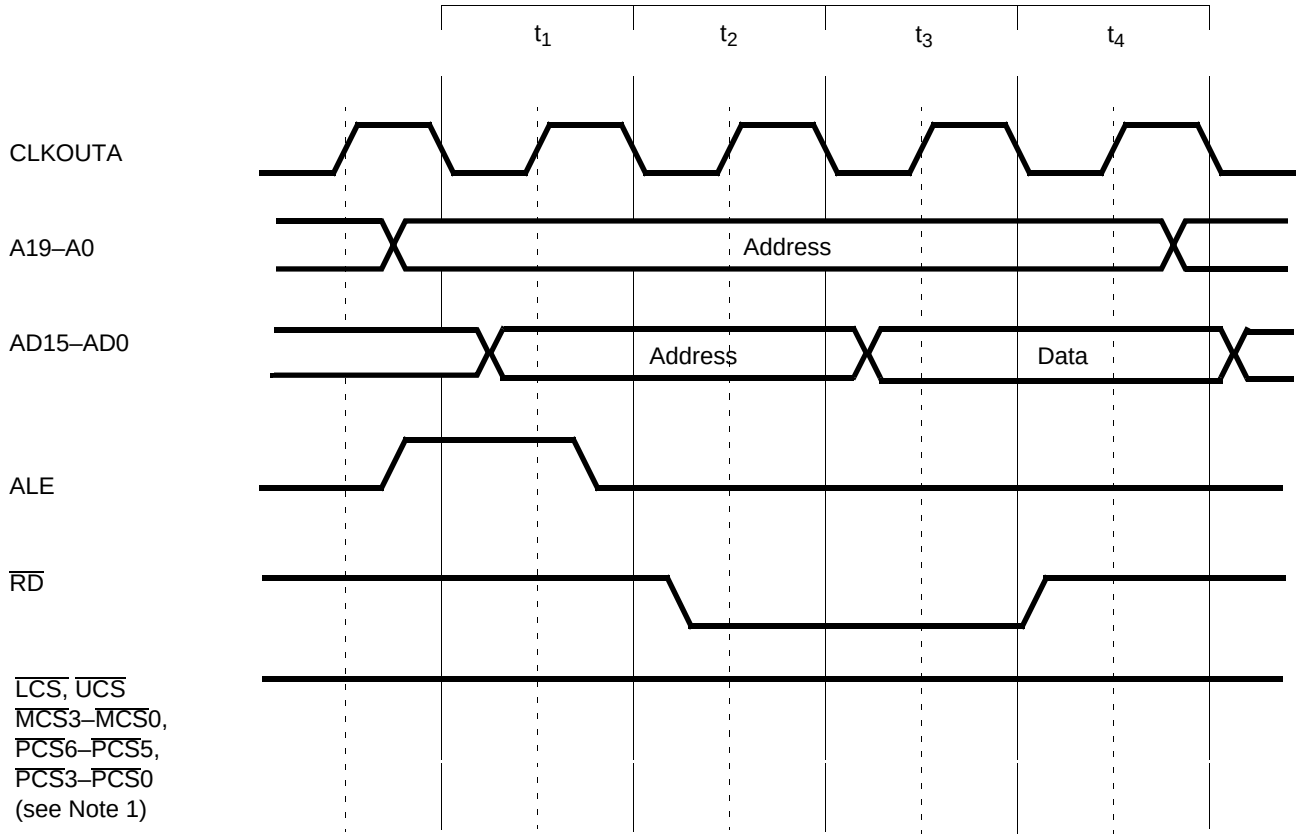
Figure 6. Internal Memory Read Cycle Waveforms



Notes:

1 – External chip selects will only assert for internal RAM accesses if they are programmed to overlap with the ICS address space.

Figure 7. Internal RAM Show Read Cycle Waveforms



Notes:

1 – External chip selects will only assert for internal RAM accesses if they are programmed to overlap with the ICS address space.