HEADLINE

A Semiconductor physics & devices.

B Inverter Working and Useful Formulas.

CMOS Fundamentals

2023

manikanthavaka1@gmail.com

HEADLINE

MANIKANTHA VAKA

8639790077

CMOS FUNDAMENTALS

UNIT 1 INTRODUCTION

➢ Fundamentals of electrons and holes:

Let's begin our discussion from basics which is about atoms, electrons and their properties. As the MOSFET deals with both electrons and holes we need to have a clear idea on what the internal operation is in a circuit.

Let's focus on two special points in this topic:

i) The electronic structure of atoms
ii) The interaction of atoms and electrons with excitation.

✓ **Key points:**

- The electrons in the metal absorb energy from the light, and some of the electrons receive enough energy to be ejected from the metal surface into the vacuum. This phenomenon is called the Photoelectric effect.
- The maximum energy ejected is given by $E = hv - q\Phi$

  Where h = planck's constant 6.626
  V = velocity of electron
  q = magnitude of electric charge
  Φ = characteristic of material used
- When Φ is multiplied by the electronic charge, energy (joules) is obtained which represents the minimum energy required for an electron to escape from the metal into a vacuum. The energy qΦ is called the work function of the metal.
- The electron may shift to an orbit of higher or lower energy, thereby gaining or losing energy equal to the difference in the energy levels (by absorption or emission of a photon of energy).

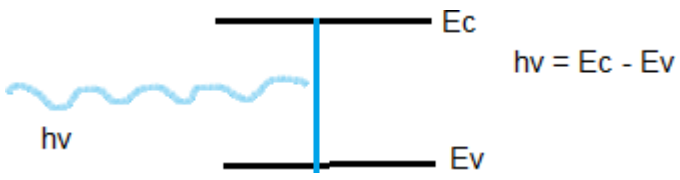


Fig: Electron absorption and emission

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

➢ Semiconductors:

✓ Types of materials:

1. **Conductor:** These materials are sensitive to electricity. It has free movement of electrons. The conduction band and valence overlap with each other (0ev).
2. **Semiconductor:** These materials carry a minimum number of electrons and they are less sensitive to electricity. It has controlled flow of charges. The energy gap between conduction band and valence band is very minimum of range 1ev.
3. **Insulator:** These materials do not have flow of electrons. The energy gap between conduction band and valence band is very high around 6ev.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

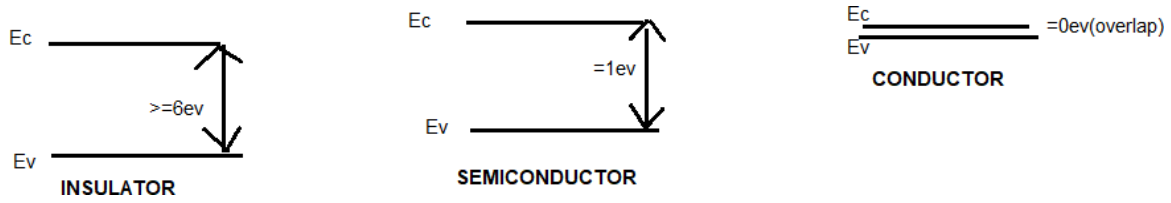


Fig: Types of materials

✓ **Why is semiconductor chosen?**

1. It has control over flow of electrons.
2. It has a large number of carriers.

✓ **Classification of semiconductors:**

1. **Based on Ionic or electronic.**
   Ionic: controlled by ions.
   Electronic: controlled by charges.
2. **Based on elemental or compound.**
   Elemental: It is made of only one material. eg: Si
   Compound: it is made of a mixture of materials. eg: GaAs
3. **Based on single crystalline, poly crystalline or amorphous.**
   Single crystalline: The orientation of atoms in the material is the same.
   Poly crystalline: The orientation of atoms in the material is different.
   Amorphous: The orientation of atoms in material is irregular.
4. **Based on doping.**
   Intrinsic: The purest form of semiconductor.
   Extrinsic: It has external dopants added. It is an impure form of semiconductor.

✓ **Intrinsic Semiconductor**

1. It is the purest form of semiconductor.
2. Examples: Si, Ge
3. These materials have 4 electrons in its valence shell i.e. the filled state of the valence band which forms a strong covalent bond which leads to non – existence of free electrons leading to no further conduction.
4. At 0°K intrinsic semiconductor behaves like an insulator.
5. Applying higher temperatures may lead to conduction.
6.

EG	**0°K**	**300°K**
Si	1.21 ev	1.1 ev
Ge	0.785ev	0.72ev

7. **Hole:** Absence of electron in an incomplete covalent bond.
8. n = ni = p; The intrinsic carrier concentration is equal to the number of holes and electron concentration.
9. Increasing temperature to make these materials conduct is not preferred so we move to extrinsic materials.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

✓ Extrinsic Semiconductor

a) N-type:

1. Intrinsic material + penta valent group (Arsenic, phosphorus, antimony) = n type
2. With the addition of impurity there is donor energy band formation just below the conduction band.

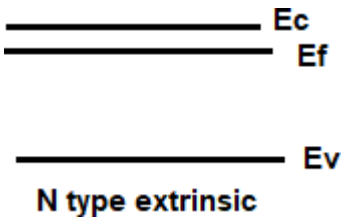


Fig: N type extrinsic semiconductor

3. Due to less band gap the electrons accumulated in the donor energy band moves from the donor energy band to conduction at room temperature. So electrons are the majority charge carriers in n type.
4. The concentration of holes is less in n type in comparison to the intrinsic materials. Due to random movement of electrons we find electron – hole recombination which generates thermal agitation leading to electron-hole pair generation.

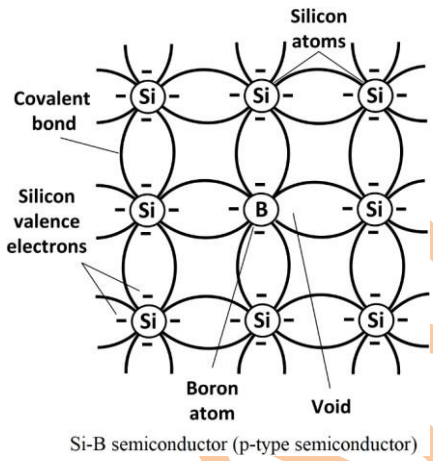


Fig: Si bonding

5. N type semiconductor is electrically neutral because with increase in pentavalent atoms electrons becoming donor ions and upon donating an electron it has a hole i.e. positive charge due to this the increase in electrons increases hole concentration is the same amount thus balancing the charges.

b) P -Type:

1. Intrinsic material + trivalent group (Boron, Aluminium, Gallium, Indium)= p type
2. With the addition of impurity there is acceptor energy band formation just above the valence band.

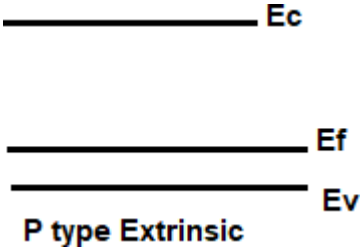


Fig: P type extrinsic semiconductor

3. Due to less band gap the electrons accumulated in the acceptor energy band moves from acceptor energy band to valence band at room temperature. So holes are the majority charge carriers in p type.
4. The concentration of electrons is less in p type in comparison to the intrinsic materials. Due to random movement of electrons we find electron – hole recombination which generates thermal agitation leading to electron-hole pair generation.
5. P type semiconductor is electrically neutral because with increase in trivalent atoms accepts electrons becoming as acceptor ions and upon accepting an electron it has an electron i.e. negative charge due to this the increase in electrons increases hole concentration is the same amount thus balancing the charges.

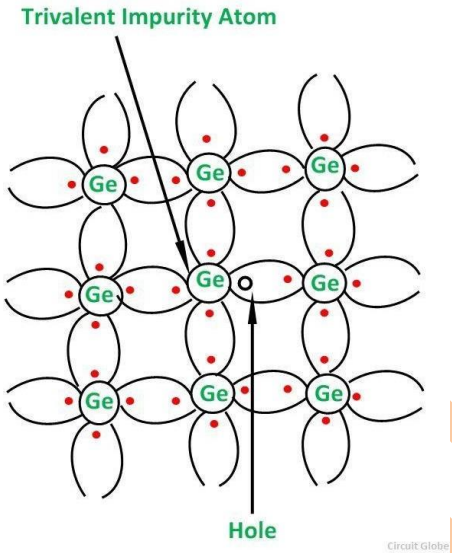


Fig: Ge boning

✓ **Fermi level:**

According to Pauli's exclusion principle the allowable range of electrons in the energy level is given by:
f(E)= 1/(1 + e^(E-EF)/KT).

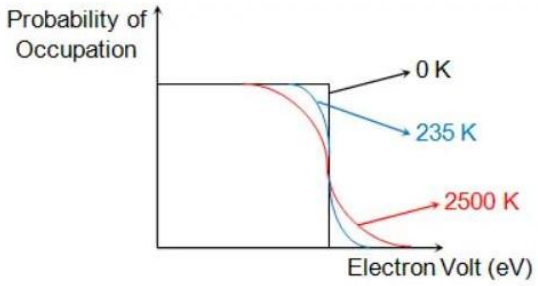
Where f(E) = fermi dirac distribution
E = energy
EF = energy at Fermi level
K = Boltzmann's constant (8.62 x 10^-5 ev/K)
T = absolute temperature

Fermi dirac distribution: It is the probability that an available energy state at E will be occupied by an electron at absolute temperature.

i) f(EF) = [1 + e^(EF -EF)/kT]^ -1 = 1/(1 + 1) = 1/ 2

Thus an energy state at the Fermi level has a probability of 1 /2 of being occupied by an electron.

ii) With T = 0 f(E) = 1/(1 + 0) = 1 when the exponent is negative (E < EF), and is 1/(1 + ∞) = 0 when the exponent is positive (E > EF). This rectangular distribution implies that at 0 K every available energy state up to EF is filled with electrons, and all states above EF are empty.



MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

Fig: Fermi dirac distribution function

✓ Effects of temperature and doping on mobility

The two basic types of scattering mechanisms that influence electron and hole mobility are lattice scattering and impurity scattering.

Lattice scattering: A carrier moving through the crystal is scattered by a vibration of the lattice, resulting from the temperature. The frequency of such scattering events increases as the temperature increases, since the thermal agitation of the lattice becomes greater. So mobility decreases with increase in temperature.

μl = T^(-3/2)

Impurity scattering: The scattering of charge carriers by ionization in the lattice. This occurs in low temperatures which leads to less agitation so mobility increases with decrease in temperature.

μi = T^(3/2)

✓ Diffusion and drift current

Diffusion: The flow of carriers caused due to diffusion of electrons from high concentration to low concentration

Drift: It is the motion of charge carriers under the influence of an external electric field.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

UNIT 2 P-N JUNCTION

➢ PN junction:

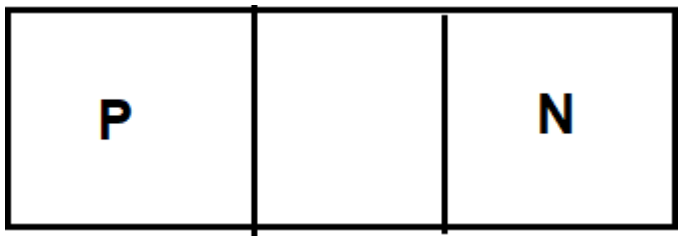


Fig: PN junction open circuit

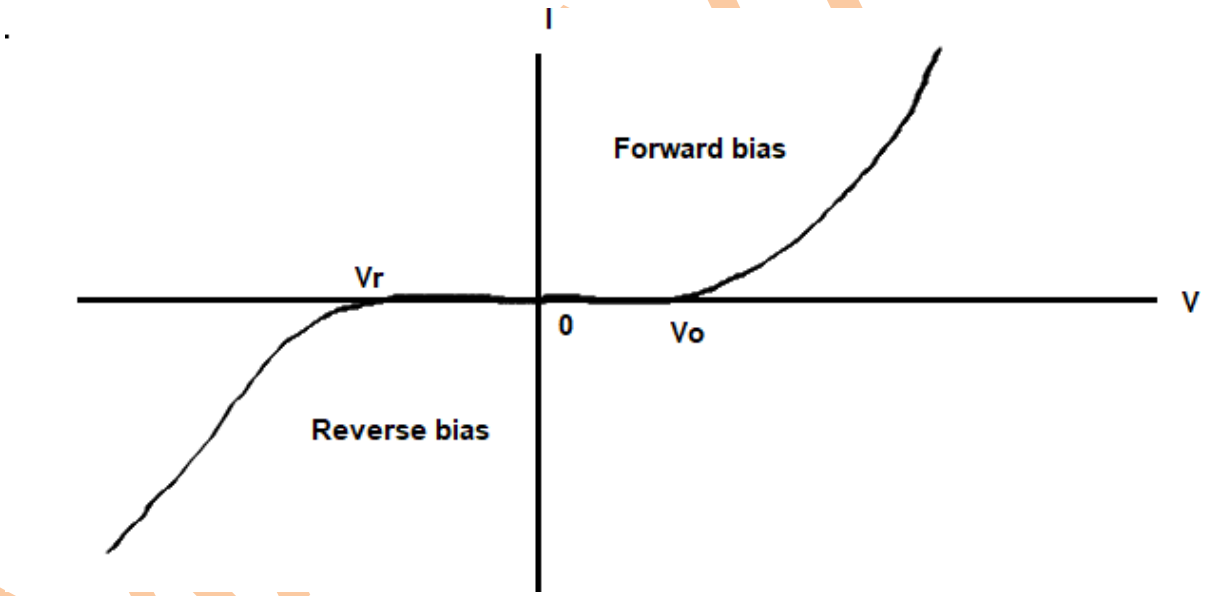


Fig: PN junction characteristics

✓ Open circuit PN-junction:

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

Fig: open circuit PN junction

1) **Diffusion current component:**
   As we have holes as majority in P side and electrons in N side there is concentration gradient on both sides which leads to movement of mobile carriers from both sides towards the other leaving immobile charges at the edges of the P and N side respectively.
   This movement of charges causes the current known diffusion current as the charges are being diffused.

2) **Depletion region/junction/barrier potential:**
   As we see due to diffusion the mobile charges leave the immobile charges which means charges are being depleted off from their respective position forming a depletion region which is also known as space charge region.
3) **Drift current:**
   The minority carriers of P and N side are swept towards the edge of depletion region with the help of electric fields from N type and P type.
   The holes from N type are swept towards the P type and electrons from P type are swept towards the N type. This drifting of charges causes drift current which occurs due to the electric field.
4) **Equilibrium:**
   In open circuit we do not apply any external supply the diffusion and drift currents are equal as they are opposite to each other thus maintaining the PN junction at equilibrium state.
   Idrift = Idiffusion
5) **Contact potential:**
   As the definition of potential states that the amount of work done to move a charge is called potential.
   Due to concentration gradient and electric field we encounter diffusion and drift currents respectively creating potential at the space charge region known as contact potential.
6) **Electric field:**
   The donor atoms from N side are depleted off creating positive charge and acceptor atoms from P side are depleted off creating negative charge.
   As the electric field occurs from positive field to negative field there exists electric field at junction.
7) **Energy band diagram:**

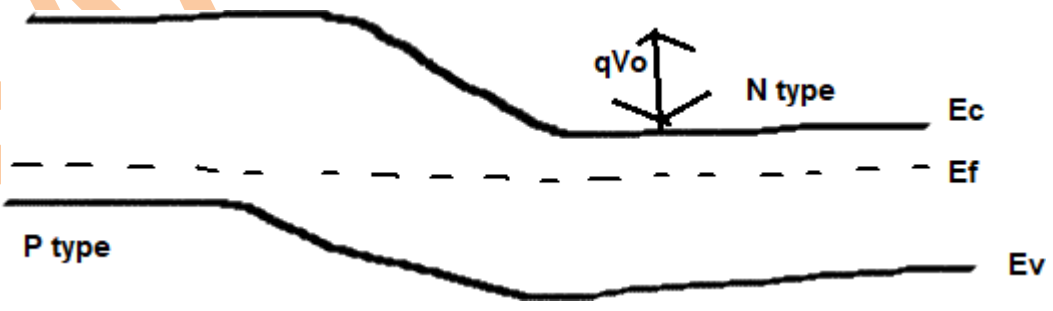


Fig: Energy band diagram of open circuit PN junction

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manikanthavaka1@gmail.com
8639790077

✓ **Forward Bias PN junction:**

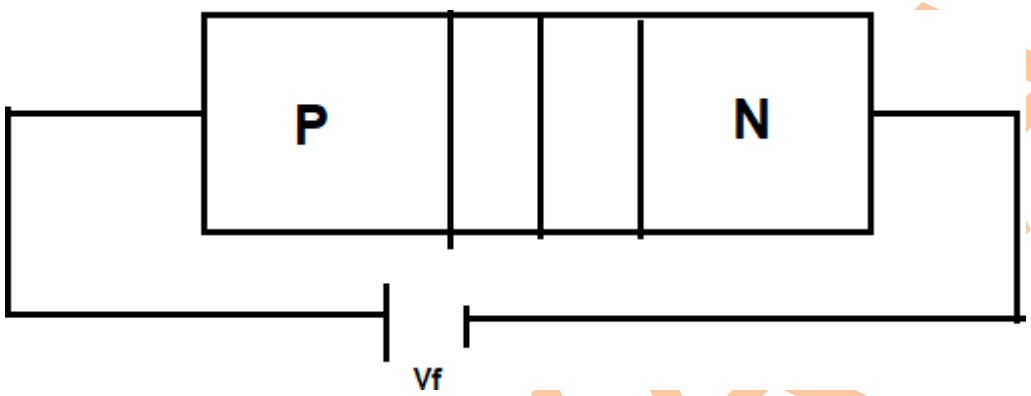


Fig: Forward bias PN junction

1) **Diffusion current component:**
   We apply negative terminal to N type and positive terminal to P type as like charges repel the electrons from N type start diffusing towards P side and the holes from P side start diffusing towards N side.
   This movement of charges causes the current known diffusion current as the charges are being diffused.
2) **Depletion region/junction/barrier potential:**
   As the charges towards the terminal are being depleted off and the space charge region is being filled with the mobile charges there is almost 0 barrier potential i.e. no depletion region or space charge region exists between N and P type in forward bias PN junction. In this region the electrons and holes start to recombine known as electron hole pair generation.
3) **Drift current:**
   The minority carriers of P and N side are swept towards the edge of depletion region with the help of electric fields from N type and P type.
   The holes from N type are swept towards the P type and electrons from P type are swept towards the N type. This drifting of charges causes drift current which occurs due to the electric field.
4) **Equilibrium:**
   In forward bias PN junction the decrease in depletion region causes increase in diffusion current with respect to the drift current.
   E = Idiffusion – Idrift
5) **Contact potential:**
   Due to electron hole pair generation there exists voltage at the depletion region but the barrier voltage reduces with reduction in the depletion region.
   Contact potential = Vo(built in voltage) – Vf(forward bias voltage)

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

6) **Electric field:**

The donor atoms from N side are depleted off creating positive charge and acceptor atoms from P side are depleted off creating negative charge.

As the electric field occurs from positive field to negative field there exists electric field at junction.

But the magnitude of drift current due to reduction in depletion region.

7) **Energy band diagram :**

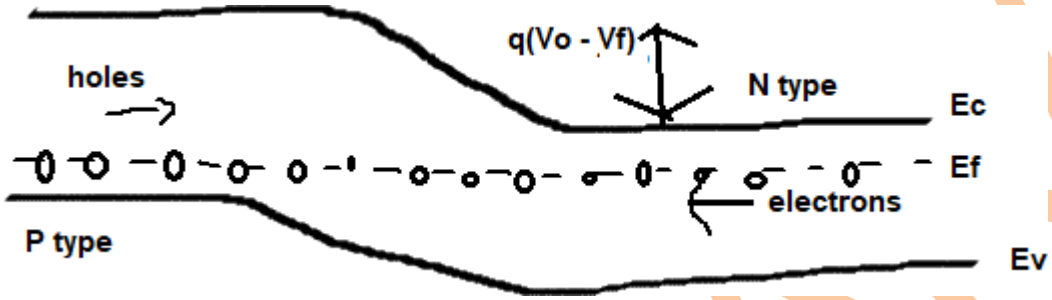


Fig: Energy band diagram of forward bias PN junction

✓ **Reverse bias PN junction:**

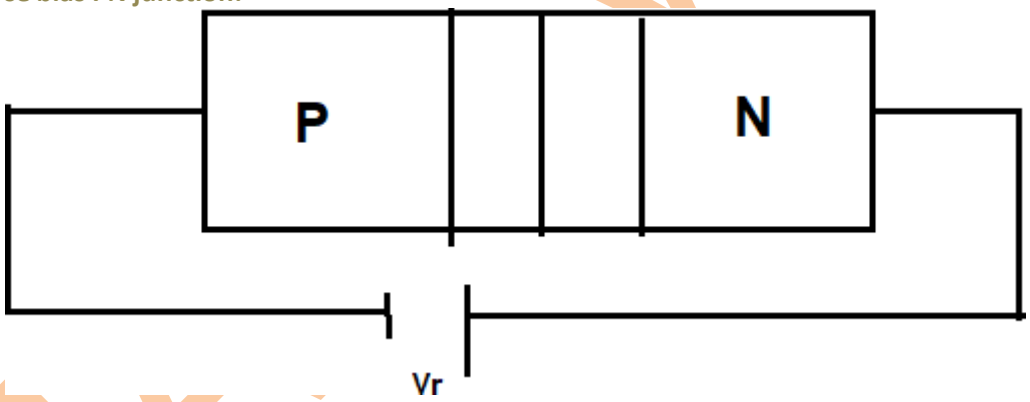


Fig: Reverse bias PN junction

1) **Diffusion current component:**

We apply positive terminal to N type and negative terminal to P type due to unlike charge attraction principle the electrons from N type start diffusing towards positive terminal and the holes from P side start diffusing towards negative terminal.

This movement of charges causes diffusion current which is very minute i.e. negligible amount.

2) **Depletion region/junction/barrier potential:**

As the electrons from N side and holes from P side move towards the P type and N type respectively due to external supply this leads to depletion of charges at the edge of P type and N type creating depletion region.

3) **Drift current:**

As the minority carriers form at the depletion region and majority carriers move towards the terminal the drifting of electrons and holes are equal which could be constant drift current.

4) **Equilibrium:**

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

In forward bias PN junction the increase in depletion region causes almost zero diffusion current and constant drift current.

E = Idrift

5) **Contact potential:**

Due to electron hole pair generation there exists voltage at the depletion region but the barrier voltage increases with increase in depletion region.

Contact potential = Vo(built in voltage) – Vbr(barrier voltage)

6) **Electric field:**

AS depletion region increases the diffusion of charges decreases which increases electric field.

7) **Energy band diagram :**

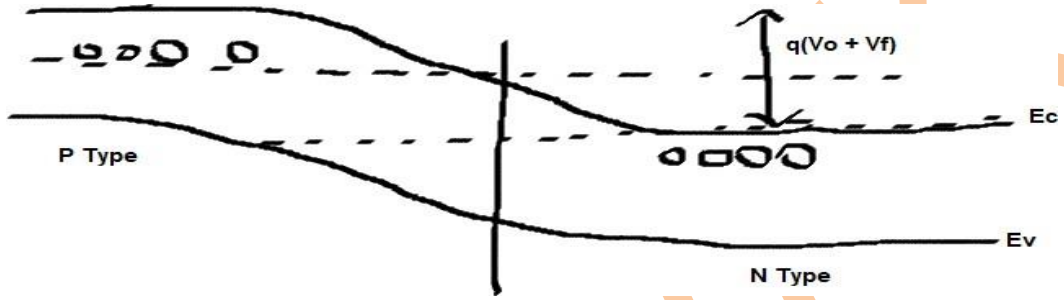


Fig: Energy band diagram of reverse bias PN junction

✓ Reverse bias breakdown:**The breakdown in reverse biased P-N junction diode is due to the strong electric field in the depletionregion when the doping is high.**

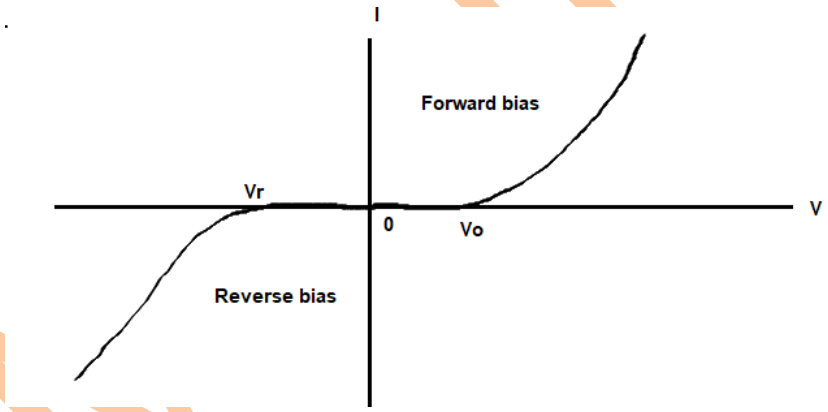


Fig: PN junction diode transfer characteristics

1) **Zener break down:**

When a heavily doped diode is reverse biased then the energy bands become crossed at relatively low voltages.

Zener breakdown occurs when the electric field in the depletion region increases to the point of breaking covalent bonds thereby generating electron-hole pairs. This tunnels the electrons from the P side valence band to the N side conduction band and the holes from N side conduction band to P side

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

valence band. This tunnelling is known as the zener effect.
After the start zener effect a large number of carriers can be generated with negligible increase in junction voltage.
This makes reverse current in the breakdown region large.

2) **Avalanche breakdown:**
This occurs when minority carriers cross the depletion region under the influence of the electric field that attracts the kinetic energy to break covalent bonds. This causes ionization collisions as carriers are free and collide.

✓ Capacitance of PN junction

1) **Junction capacitance/transition capacitance in reverse bias:**
This is due to dipole in transition region
C_{dep} or C_J or C_T = £A/w
2) **Diffusion capacitance in forward bias:**
Rate of change in injected minority carriers in the junction with variation of V_F is depletion capacitance.
$C_D = \tau I/\eta V_T$
NOTE: $W = 2£V_J(N_A + N_D)/(qN_AN_D)$
Open circuit $V_J = V_o$
Forward bias $V_J = V_o - V_F$
Reverse bias $V_J = V_o + V_R$
$V_T = T/11600$
τ =life time of charge
I = forward current

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

UNIT 3 MOSFET

➢ MOSFET:

- MOSFETs are chosen for VLSI applications instead of BJT's because MOSFETs can handle high frequency operations but BJT can't so MOSFETs are preferred over BJTs in VLSI circuits.
- MOSFET stands for Metal Oxide Semiconductor Field Effect Transistor.

1) Enhancement N MOSFET :

a) Zero bias :

At V_G= 0 volts there will be no current flowing in the MOSFET as there is no external supply to the device.

There exists a reverse bias PN Junction with source – P substrate and drain – P substrate. The reverse bias junction has high resistance causing I_G = 0A.

b) V_{GS} >0 Volts

When an external supply is given in a way that the positive terminal of supply is applied to Gate and negative terminal is grounded due to the polarization effect positive charges accumulate at the metal and oxide layer see the orientation of charges towards the external supply there by electrons are oriented towards metal and holes are oriented towards the P substrate. These holes repel with holes of P substrate causing depletion region. As the source and drain are N type electrons are attracted towards the gate by the holes creating accumulation of electrons forming N type channel this is called weak inversion. Once the concentration of electrons in the channel is equal to the concentration of holes in P substrate then it is called as strong inversion.

This state at which channel is formed due to strong inversion makes the current flow in the channel. Due to the flow of current the device gets ON.

The voltage at which strong inversion occurs is called Threshold voltage V_T.

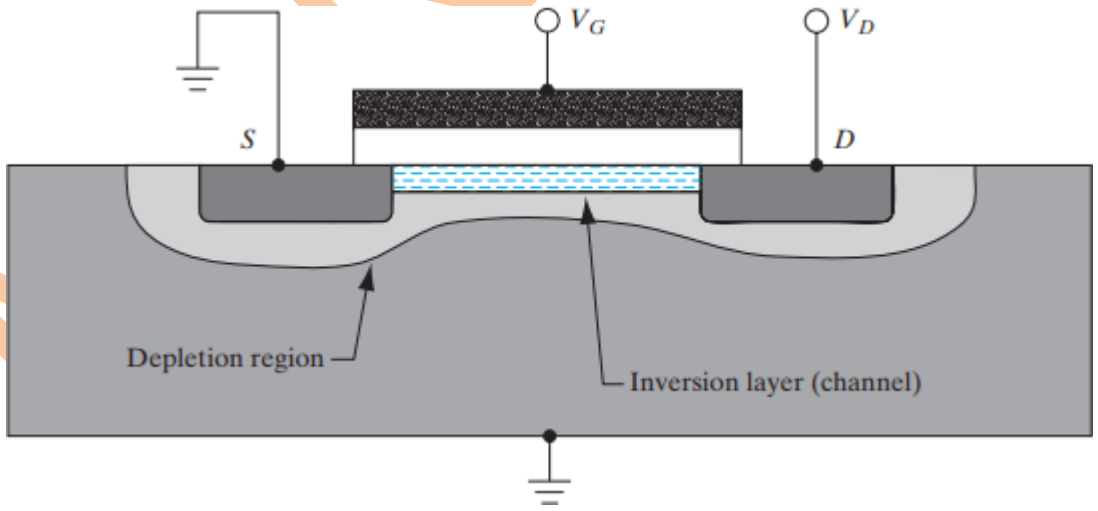


Fig: N-MOSFET in linear mode of operation

POLARIZATION EFFECT: The slight orientation of charges towards the external supply.

WEAK INVERSION: The accumulation of charge in the channel.

STRONG INVERSION: When the concentration of charge carriers in the channel is equal to the charge

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

concentration in the substrate it is called as strong inversion.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

c) $V_{GS} \geq V_T$; $V_{DS} > 0$ (small)

At this condition when $V_{GS} \geq V_T$ the channel starts forming and when drain is given with small external supply the electric field attracts electrons from source to drain causing drain current I_D to flow across the channel.

Due to increase in V_{GS} the electrons from source increases thus increasing the concentration of electrons on the surface of P substrate due to which depth of channel increases which is termed as enhancement of channel so the name of the device "Enhancement N MOSFET".

d) V_{GS} = constant , $V_{DS} > 0$

At this condition when $V_{GS} \geq V_T$ the channel starts forming and when drain is given with small external supply the electric field attracts electrons from source to drain causing drain current I_D to flow across the channel increases linearly.

The increment of current is linear because the channel dimension is not varying as V_{GS} is made constant and the concentration of electrons is fixed due to the constant V_{GS} which makes the channel act as a resistor. As per Ohm's law statement resistor(R) is linear so thus the current increment is linear.

We have negligible voltage drop along the channel as the voltage range from source and drain is small. Due to negligible voltage drop the channel depth is uniform.

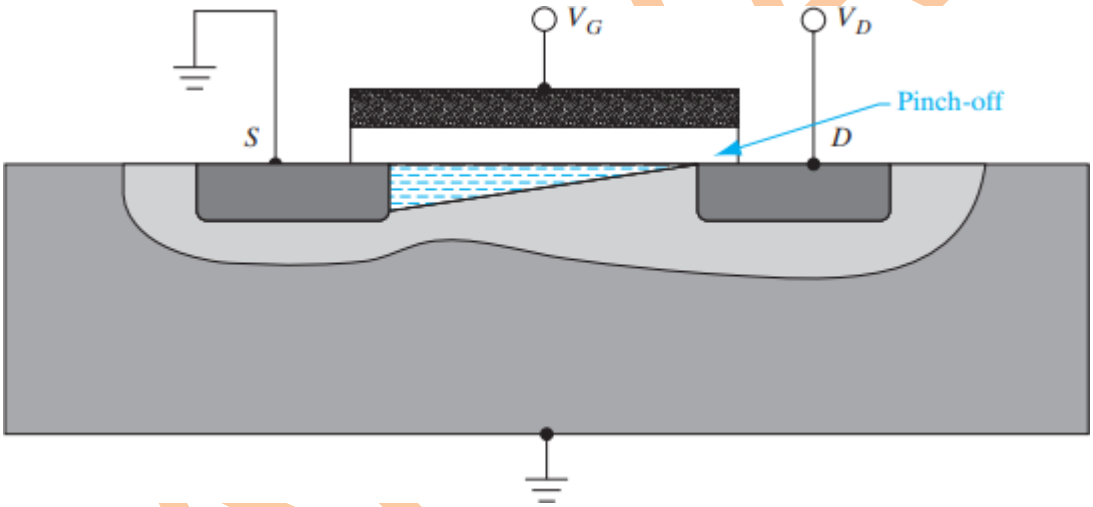


Fig: N-MOSFET in Saturation mode of operation

e) $V_{GS} > V_T$, $V_{DS} >> 0$

With increase in V_{DS} the current increase. The V_{GS} is acting perpendicular on the MOS so its effect is the same all over the channel. The electric field induced due to V_{DS} is varying from source to drain as V_{DS} is increasing and thus the drop from source to drain also increases. This leads to reduction of depth of channel towards drain than at source.

f) $V_{DS} >> 0$

With further increase in V_{DS} the drop from source to drain increases and the gate channel potential reduces from source to drain and thus the depth decreases at drain. At some point of V_{DS} the depth of channel at drain becomes zero, that point is called pinch - off and the voltage is pinch - off voltage.

Pinch – off voltage $V_{DS} = V_{GS} - v_T$

This pinch – off affects the rate of increment of I_D is small as the V_{DS} is high and resistance of the channel is increasing as channel area decreases.

g) $V_{DS} \geq V_{GS} - V_T$, $V_{GS} > V_T$

At this voltage condition due to reverse bias at drain the depletion width of drain increases there by the pinch – off voltage slightly shifts towards the source due to increase in depletion width. At the

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

condition the I_D exists.

As the depletion region forms the electrons from source is being pulled by electric field from drain but at pinch – off region the electric field sweeps the electrons towards drain from source as electrons do not find a path after pinch – off point the velocity starts saturating and thus the mobility of electrons saturates this leads to constant resistance so the I_D becomes saturating.

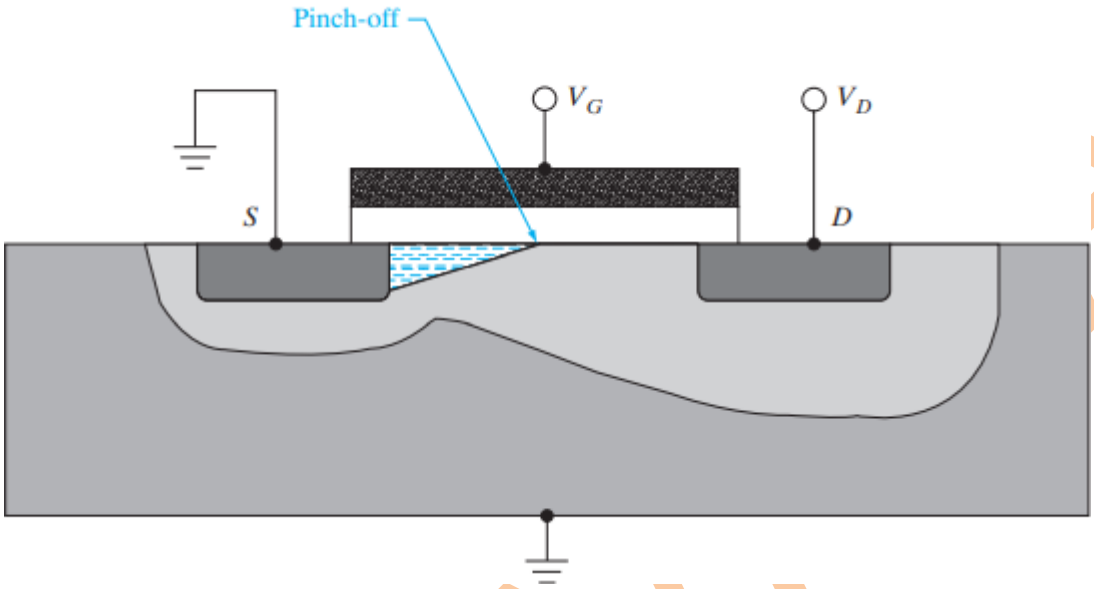


Fig: N-MOSFET in Saturation - pinch- off point

I_D equations:

I. Cut off :

$V_{GS} < v_T$ $I_D = 0$

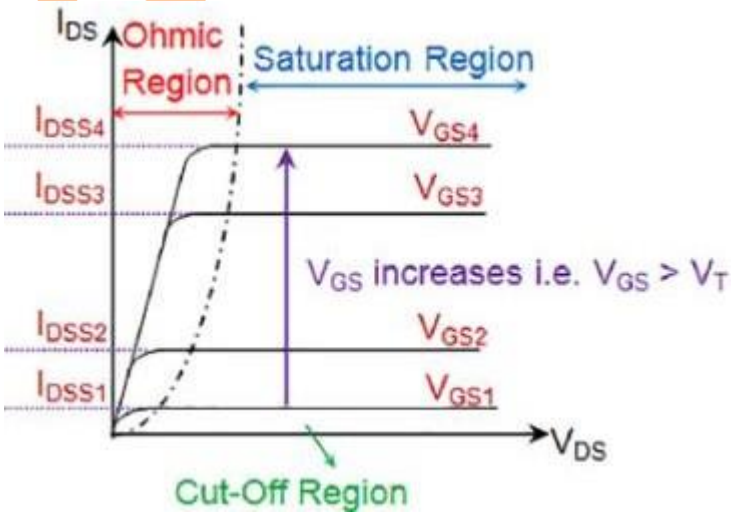
II. Triode region:

$V_{GS} - V_T > V_{DS}$; $I_D = \mu_n c_{ox} W/L[(V_{GS}-V_T)V_{DS} - V_{DS}^2/2]$

III. Saturation region:

$V_{GS}-V_T < V_{DS}$; $I_D = 1/2\mu_n c_{ox} W/L[V_{GS}-V_T]^2$

Drain characteristics:



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manikanthavaka1@gmail.com
8639790077

Fig: Drain characteristics of NMOSFET

Transfer characteristics:

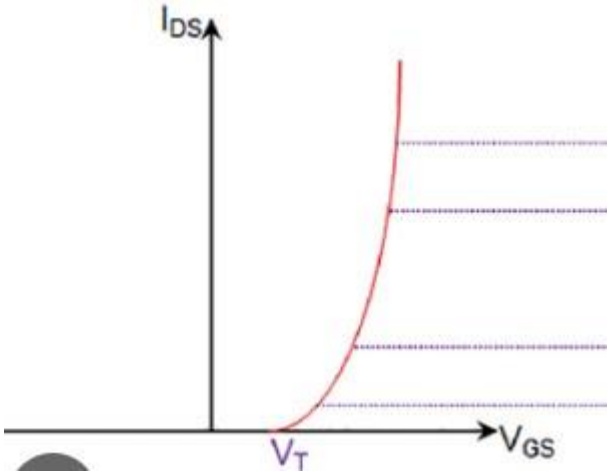


Fig3: Transfer characteristics of NMOSFET

2) Enhancement P MOSFET:

a) Zero bias :

At V_G= 0 volts there will be no current flowing in the MOSFET as there is no external supply to the device.

There exists a reverse bias PN Junction with source – N substrate and drain – N substrate. The reverse bias junction has high resistance causing I_G = 0A.

b) V_{GS} > 0 Volts

When an external supply is given in a way that the negative terminal of supply is applied to Gate and positive terminal is grounded due to the polarization effect negative charges accumulate at the metal and oxide layer see the orientation of charges towards the external supply thereby holes are oriented towards metal and electrons are oriented towards the N substrate. These electrons repel with electrons of N substrate causing depletion region. As the source and drain are P type holes are attracted towards the gate by the electrons creating accumulation of holes forming P type channels this is called weak inversion. Once the concentration of holes in the channel is equal to the concentration of electrons in the N substrate then it is called as strong inversion.

This state at which channel is formed due to strong inversion makes the current flow in the channel. Due to the flow of current the device gets ON.

The voltage at which strong inversion occurs is called Threshold voltage V_T.

c) $V_{GS} \leq V_T$; $V_{DS} < 0$ (small)

At this condition when $V_{GS} \leq V_T$ the channel starts forming and when drain is given with small external supply the electric field attracts electrons from drain to source causing drain current I_D to flow across the channel.

Due to increase in V_{GS} negatively the electrons from drain increases thus increasing the concentration of holes on the surface of N substrate due to which depth of channel increases which is termed as

enhancement of channel so the name of the device “Enhancement P MOSFET”.

d) V_{GS} = constant , $V_{DS} < 0$

At this condition when $V_{GS} \leq V_T$ the channel starts forming and when drain is given with small external supply the electric field attracts electrons from drain to source causing drain current I_D to flow across the channel increases linearly.

The increment of current is linear because the channel dimension is not varying as V_{GS} is made constant and the concentration of electrons is fixed due to the constant V_{GS} which makes the channel act as a resistor. As per Ohm’s law statement resistor(R) is linear so thus the current increment is linear.

We have negligible voltage drop along the channel as the voltage range from drain and source is small. Due to negligible voltage drop the channel depth is uniform.

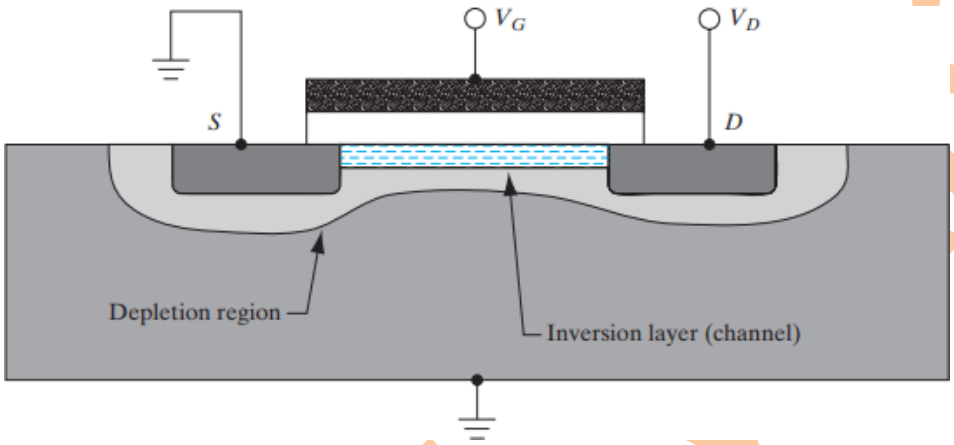


Fig: P-MOSFET in linear mode of operation

e) $V_{GS} < V_T$, $V_{DS} << 0$

With increase in V_{DS} negatively the current increase. The V_{GS} is acting perpendicular on the MOS so its effect is the same all over the channel. The electric field induced due to V_{DS} is varying from drain to source as V_{DS} is increasing negatively and thus the drop from drain to source also increases. This leads to reduction of depth of channel towards source than at drain.

f) $V_{DS} << 0$

With further increase in V_{DS} negatively the drop from drain to source increases and the gate channel potential reduces from drain to source and thus the depth decreases at source. At some point of V_{DS} the depth of channel at source becomes zero, that point is called pinch - off and the voltage is pinch - off voltage.

Pinch – off voltage $V_{DS} = -(V_{GS} - v_T)$

This pinch – off affects the rate of increment of I_D is small as the V_{DS} is high and resistance of the channel is increasing as channel area decreases.

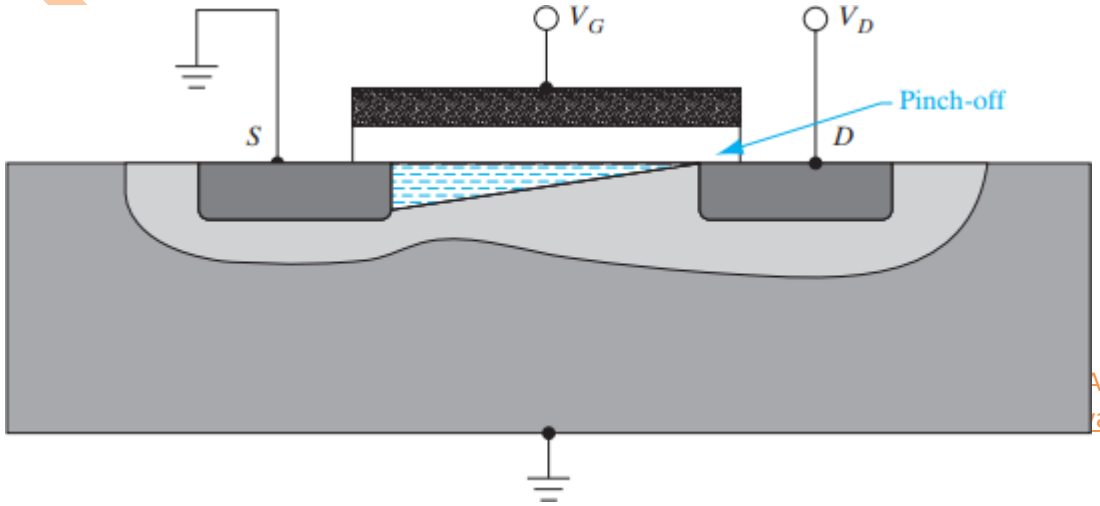


Fig: P-MOSFET in saturation mode of operation

g) $V_{DS} \leq V_{GS} - V_T$, $V_{GS} < V_T$

At this voltage condition due to reverse bias at drain the depletion width of source increases there by the pinch – off voltage slightly shifts towards the drain due to increase in depletion width. At the condition the I_D exists.

As the depletion region forms the electrons from drain is being pulled by electric field from source but at pinch – off region the electric field sweeps the electrons towards source from drain as electrons do not find a path after pinch – off point the velocity starts saturating and thus the mobility of electrons saturates this leads to constant resistance so the I_D becomes saturating.

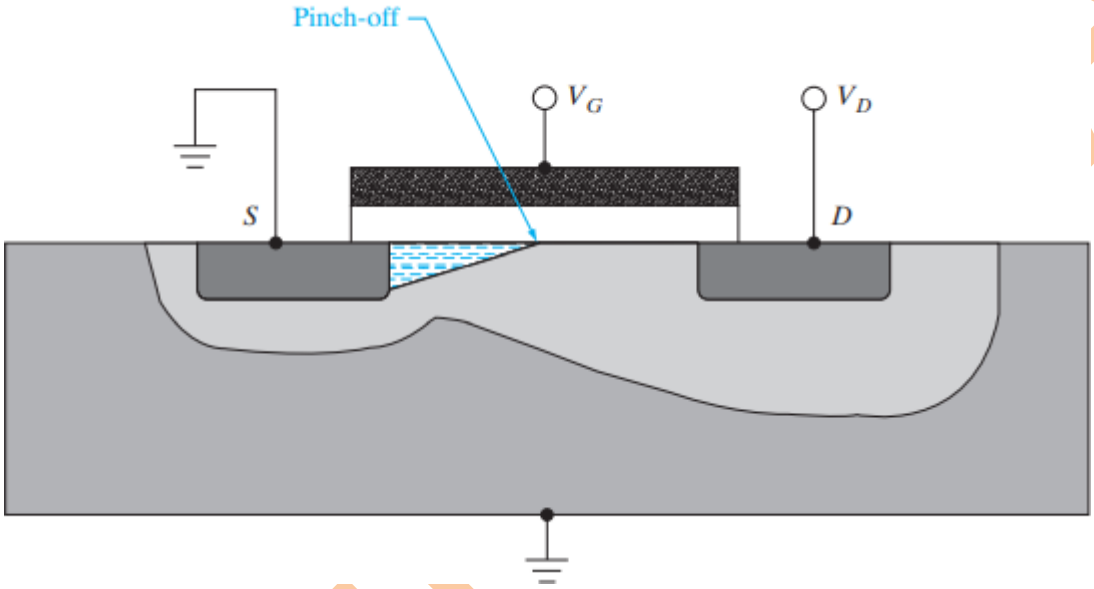


Fig: N-MOSFET in saturation - pinch - off point

I_D equations:

I. Cut off :

$V_{GS} > v_T$ $I_D = 0$

II. Triode region:

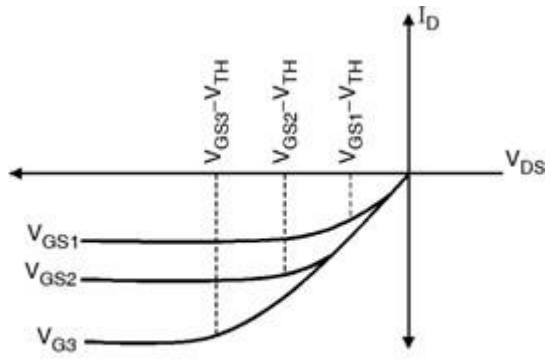
$V_{GS} - V_T < V_{DS}$; $I_D = \mu_n c_{ox} W/L[(V_{GS}-V_T)V_{DS} - V_{DS}^2/2]$

III. Saturation region:

$V_{GS}-V_T > V_{DS}$; $I_D = 1/2\mu_n c_{ox} W/L[V_{GS}-V_T]^2$

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

Drain characteristics:



I-V characteristics of PMOS transistor

Fig: Drain characteristics of PMOSFET

Transfer characteristics:

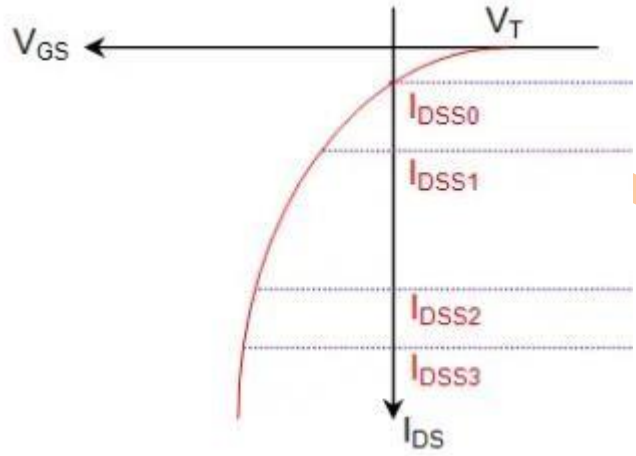
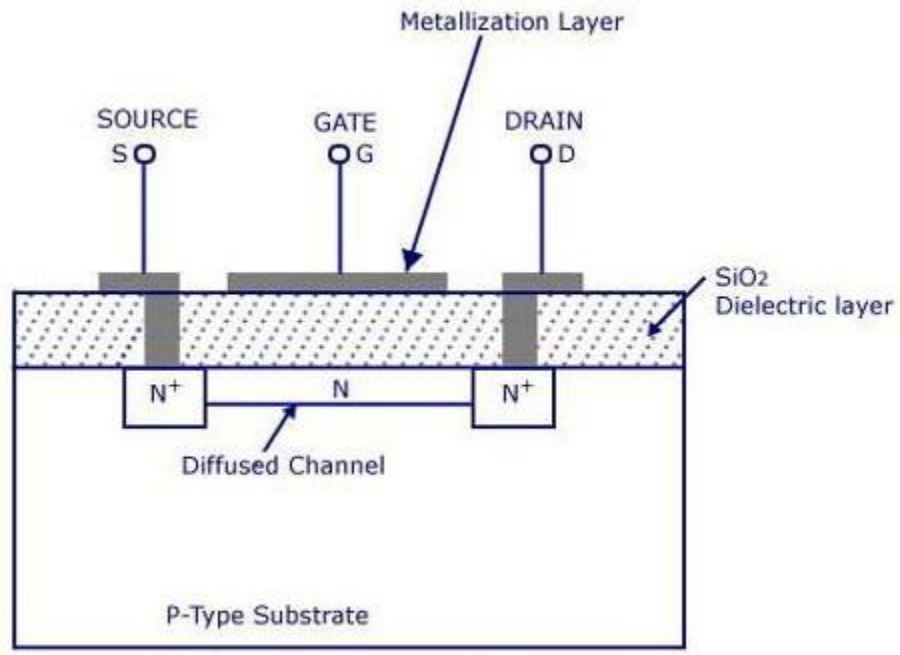


Fig: Transfer characteristics of PMOSFET

3) Depletion N MOSFET:



N-Channel DE-MOSFET Structure

MANIKANTHA VAKA
anikanthavaka1@gmail.com
8639790077

Fig: NMOSFET - depeletion

a) **V_{GS} = 0 volts V_{DS} > 0**

Though the V_{GS} is zero volts but due to external supply at drain and the presence of channel the electric field from drain causes electrons from source to travel from source to drain there by causing drain current.

b) **V_{GS} > 0**

The channel depth increases due to applied supply at the gate and the channel enhances.

c) **V_{GS} < 0**

The channel starts decreasing as gate potential is being reduced this leads to zero current. Thus the depletion of the channel occurs; this is named as "Depletion N MOSFET".

The voltage at which the device starts depleting its channel is called threshold voltage.

5) **Depletion P MOSFET:**

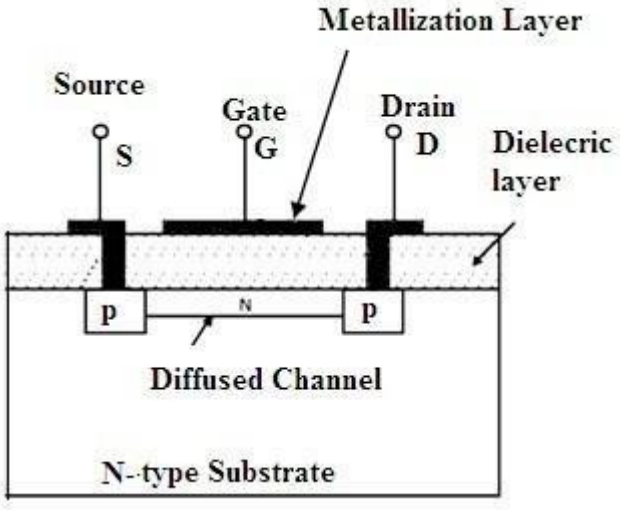


Fig: PMOSFET –depletion

a) **V_{GS} = 0 volts V_{DS} < 0**

Though the V_{GS} is zero volts but due to external supply at drain and the presence of channel the electric field from source causes electrons from drain to travel from drain to source thereby causing drain current.

b) **V_{GS} < 0**

The channel depth increases due to applied supply at the gate and the channel enhances.

c) **V_{GS} > 0**

The channel starts decreasing as gate potential is being increased this leads to zero current. Thus the depletion of the channel occurs this is named as "Depletion N MOSFET".

The voltage at which the device starts depleting its channel is called threshold voltage.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

✓ **Transfer characteristics of E-PMOSFET, E- NMOSFET, D- PMOSFET, D-NMOSFET:**

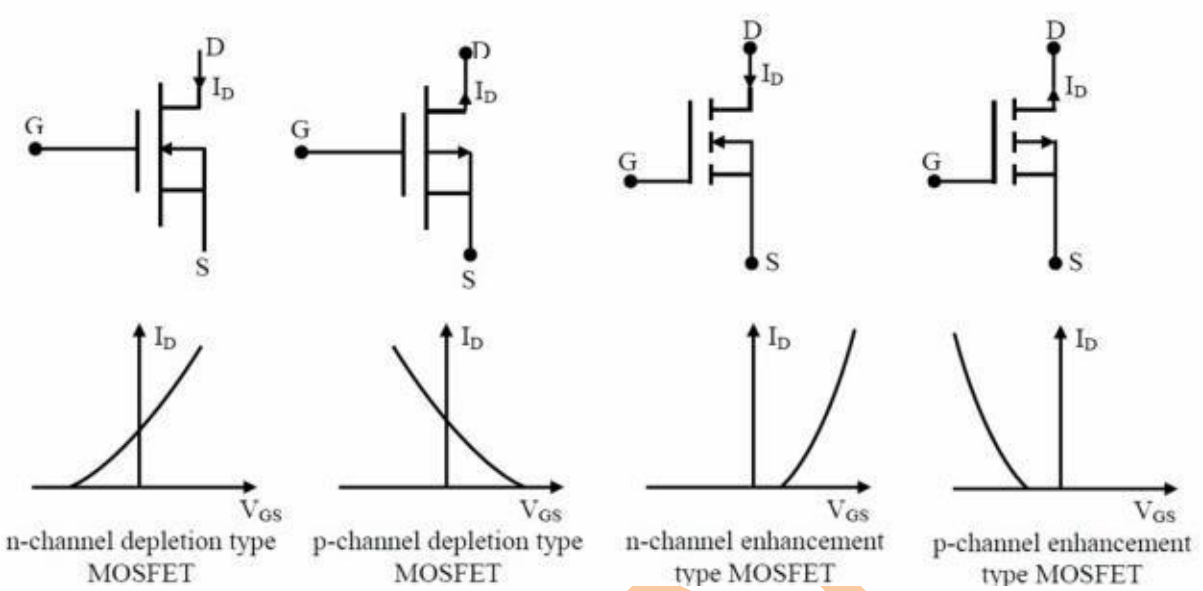


Fig: Transfer characteristics of E-PMOSFET, E- NMOSFET, D- PMOSFET, D-NMOSFET

➢ Energy band diagram:

1) Equilibrium :

In ideal conditions there is no external supply to the device so the energy gap between conduction and valence band is high.

The gap between Evac and Efm is called the work function $q\Phi_m$ is the energy required by an electron to move from Fermi energy to vacuum energy level.

Electron affinity (χ): It is the energy required to move an electron from the conduction band of a semiconductor to vacuum energy.

Ionization energy: The energy required to move an electron from the valence band of semiconductor to vacuum energy.

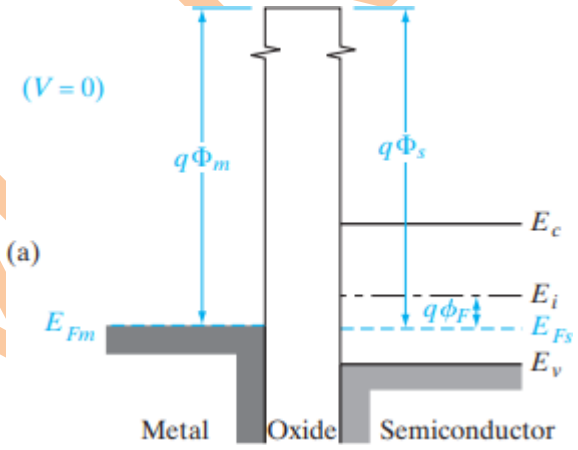


Fig: Equilibrium condition of MOSFET

2) Accumulation:

Accumulation of charges at the channel takes place when we apply $V_{GS}<0$.

As we apply external supply $V_{GS}<0$ the holes get accumulated at the surface this is called accumulation.

The electrons in metal increases so the E_{FM} increases but it is known that the work function

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

of a material doesn't change so E_{VAC} is increased with equal rise of E_{FM} thus tilting the E_{vac} of the oxide layer upwards.

Valence band of bends upwards indicating that the hole concentration towards oxide layer is increased and as the energy gap between conduction band and valence band has to be maintained the conduction band is also tilted upward.

The work function and energy gap has to be maintained with respect to the device property because once they are changed the overall behaviour of the device changes and it no longer behaves as expected.

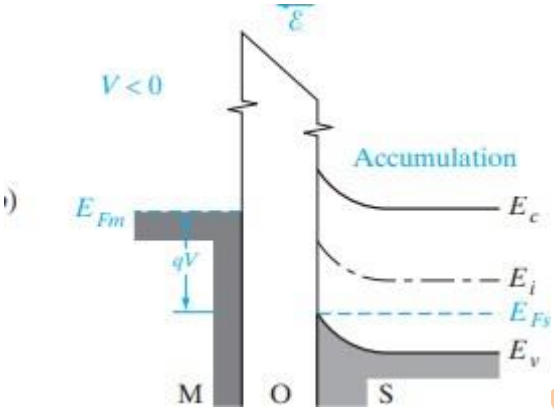


Fig: Accumulation condition of MOSFET

3) Depletion:

The depletion occurs when $V_{GS} > V_T$ and $V_{DS} > 0$ as the electron concentration at channel increases thereby increasing the hole concentration at metal due to the presence of external supply. The conduction band of oxide layer near the semiconductor is tilted upwards indicating the increase of electrons at the semiconductor.

Thus maintaining the work function and energy gap equally the conduction band and valence band are tilted downwards.

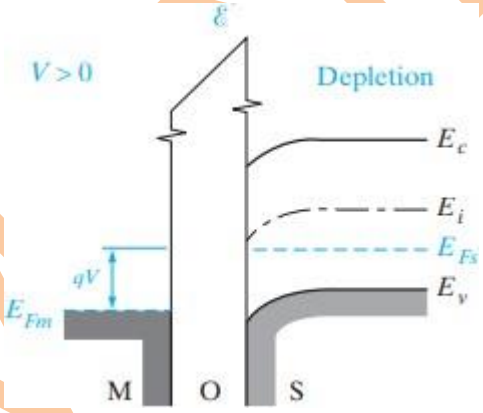


Fig: Depletion condition of MOSFET

4) Inversion:

The inversion occurs when $V_{GS} >> V_T$ and $V_{DS} >> 0$.

The band bending of the valence band is so high because intrinsic energy crosses E_F in N type E_F is above E_I and in P type E_i is below E_F.

Since voltage applied is positive to the gate, electrons travel towards the gate and accumulate near the semiconductor-oxide junction resulting in the development of surface potential. Due to surface potential energy band bending takes place.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

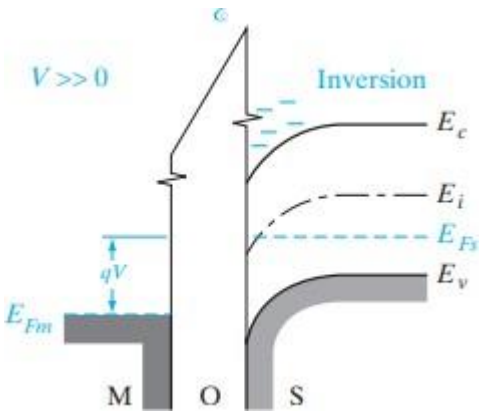


Fig: Inversion condition of MOSFET

➢ VT equation:

- $V_T = V_{to} + \Upsilon\left(\sqrt{(2\emptyset F + VSB)} - \sqrt{2\emptyset F}\right)$

  At $V_{SB} = 0$ $v_T = V_{to}$
- Body bias: V_{SB} if there exists a potential difference between source and substrate it is known as body bias.
-

✓ Check on VSB potential for NMOS for VB = -1v

1. V_S connected to +1v

$V_{SB} = V_S - V_B$

$= 1-(-1)$

$= 2v$

When V_{SB} is connected with forward bias there are chances that the electrons flow might be distorted and current direction will change leading to improper function of the device.

2. V_S connected to 0v

$V_{SB} = V_S - V_B$

$= 1-(0)$

$= 1v$

When V_{SB} is connected with forward bias there are chances that the electrons flow might be distorted and current direction will change leading to improper function of the device.

3. V_S connected to 1v

$V_{SB} = V_S - V_B$

$= 1-(1)$

$= 0v$

When V_{SB} is connected with reverse bias then due to the space charge region there exists a leakage current and the electrons flow can be controlled thereby having a proper functioning device.

So it is recommended to connect source – substrate in reverse bias.

✓ Ideal V_{TO} components:

a. Voltage requirement for depletion charge:

The V_T is affected by the depletion charge and can be computed by Q_d/C_i

As the channel forms there exists a charge in the depletion region and due to parallel plate and dielectric medium the channel acts as a parallel plate capacitor, this charge has some voltage called depletion charge voltage.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

b. Voltage requirement for inversion charge:

The inversion charge is denoted by $2\emptyset F$, it is the potential to form inversion at the channel of a MOSFET.

∴ Ideal V_{to} component = $-Q_d/C_i + 2\emptyset F$

✓ **Real V_{TO} components:**

a. Voltage requirement for depletion charge:

The V_T is affected by the depletion charge and can be computed by Q_d/C_i

As the channel forms there exists a charge in the depletion region and due to parallel plate and dielectric medium the channel acts as a parallel plate capacitor, this charge has some voltage called depletion charge voltage.

b. Voltage requirement for inversion charge:

The inversion charge is denoted by $2\emptyset F$, it is the potential to form inversion at the channel of a MOSFET.

c. $\emptyset_{ms}$: metal semiconductor work function difference

This occurs with the way fabrication chooses the materials for metal and semiconductor. In ideal we consider the same materials so E_F to E_{vac} it was equal for metal and semiconductor. But in reality there exists some difference between E_F and Evac. The metal semiconductor work function difference acts in such a way that there exists a positive potential at the gate terminal due to this band bending down and depletion occurs.

d. Oxide charge: Q_i/C_i:

The positive potential seen at the gate terminal needs to be nullified to bring the device back to ideal condition.

The positive potential is formed due to the process of forming an oxide layer.

∴ The amount of negative potential added to bring the bent bands to flat is called flat band potential = $V_{FB} = - Q_i/C_i + \emptyset_{ms}$

∴ Real V_{to} component = $-Q_d/C_i + 2\emptyset F - Q_i/C_i + \emptyset_{ms}$

✓ **Formation of Oxide charge:**

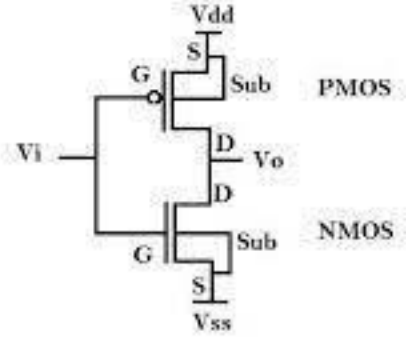
1. In the formation of an oxide layer there may be alkaline metal ions which are acted as they are active causing the positive charge to exist.
2. The Si atom of source and drain at the edge due to physical termination has an electron without bond called dangling bond leading to positive charge. (Dangling bond results in positive charge because O_2 has less electrons with respect to Si so absence of electrons causes positive charge).
3. Due to insufficient oxygen at oxidation process i.e. SiO_2 the Si may not have sufficient O_2 this results in positive charge.
4. Due to defects in the crystalline structure of the oxide layer may cause positive charge.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

UNIT 4 CMOS

➢ CMOS:

- CMOS stands for Complementary Metal Oxide Semiconductor Field Effect Transistor.



G = Gate Terminal
S = Source Terminal
D = Drain Terminal
Sub = Substrate Terminal

Schematic diagram of CMOS Inverter

Fig: CMOS circuit

✓ Advantages of CMOS:

1. High noise margin due to full voltage swing.

2. High input impedance due to $I_G = 0$.

3. Low output impedance, in steady state there always exists a path with finite resistance between output and either V_{DD} or GND, making it less sensitive to noise and disturbances.

4. Ratio less property as the logic of the CMOS does not depend on the W/L ratio of P and N MOSFET.

5. Zero static power dissipation as no direct exists between ground and supply rail under steady state condition.

✓ The analysis of the gate is done with respect to the different design metrics as listed below:

1) Cost, expressed by the complexity and area.

2) Integrity and robustness, expressed by the static (or steady-state) behaviour.

3) Performance, determined by the dynamic (or transient) response

4) Energy efficiency, set by the energy and power consumption.

✓ Logic:

Positive logic = 1: positive potential

Negative logic = 0: negative potential

When V_{in} = 1 and equal to V_{DD} the NMOS transistor is ON while the PMOS is OFF.

When V_{in} = 0 and equal to V_{SS} the PMOS transistor is ON while the NMOS is OFF.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

✓ **Structure of CMOS logic:**

1. Consists of Pull down and Pull up networks.
2. Pull down network has NMOS and Pull up network has PMOS.
3. AND : NMOS is connected in series; PMOS is connected in parallel.
   OR: NMOS is connected in parallel; PMOS is connected in series.
4. Output is a complement of input.
5. Same inputs are given to both NMOS and PMOS.
6. For N inputs 2N transistors are needed.
7. Pull up transistor is the dual of a pull down transistor.

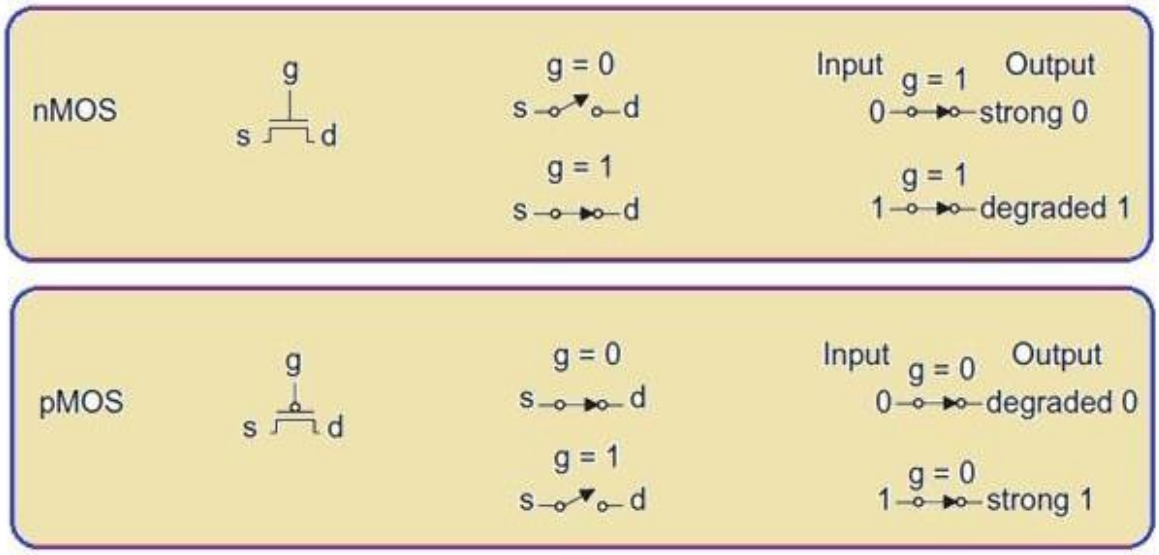
✓ **Strong 0 and Strong 1**

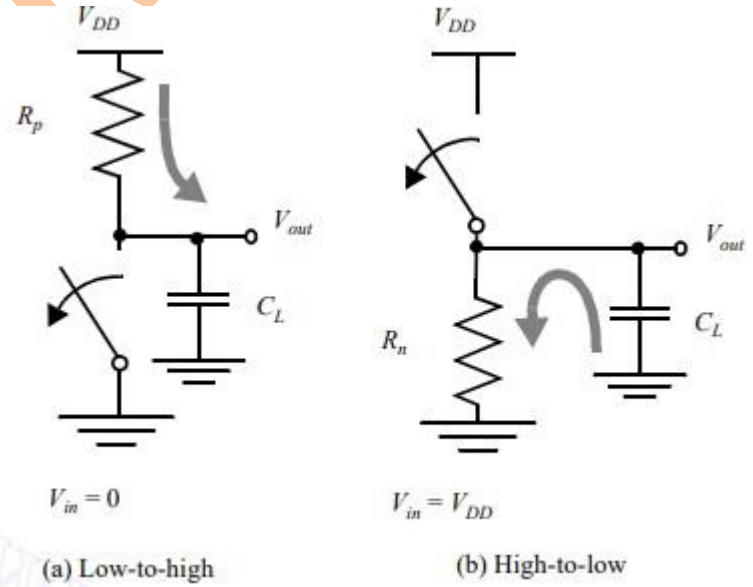
STRONG 0:

When NMOS and PMOS are given with some voltage let's say 5V and VDD with 5V and Vt 0.7V the final voltage at the output due to discharging capacity of the capacitor is found to be 0V for NMOS and for PMOS it is 4.3V as we need complete discharge of the voltage we consider NMOS as strong 0.

STRONG 1:

When NMOS and PMOS are given with some voltage let's say 5V and VDD with 5V and Vt 0.7V the final voltage at the output due to charging capacity of the capacitor is found to be 5V for PMOS and for NMOS it is 0.7V as we need input voltage to be reached as the output voltage so we consider PMOS as strong 1.





MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

Fig: Strong 1 and strong 0

VTC of CMOS:

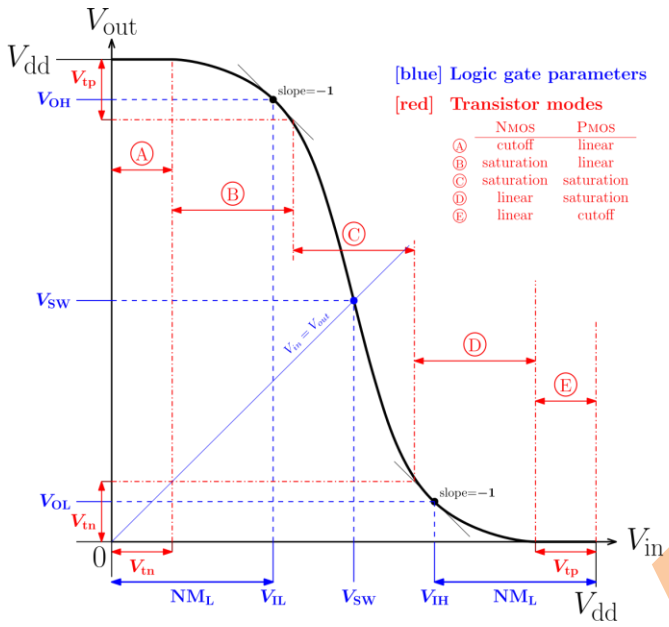


Fig : VTC of CMOS

NOTE:

A fast gate is built either by keeping the output capacitance small or by decreasing the on-resistance of the transistor.

✓ Noise margin:

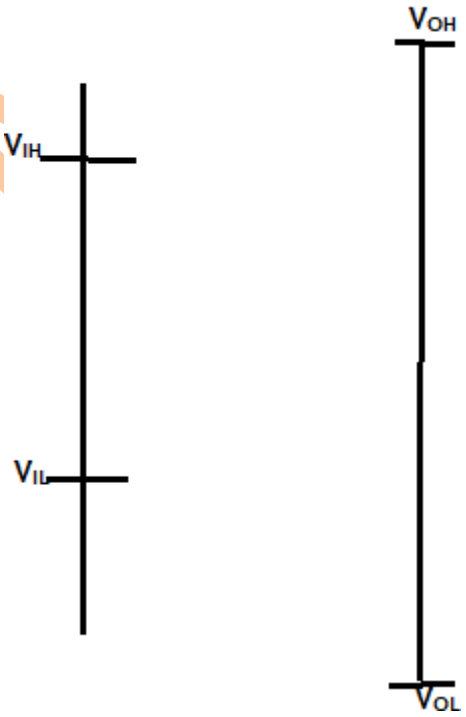
The amount of noise added to input could hold the output at logic 1 or 0 for the applied input without distortion is called noise margin.

$N_{ML} = V_{IL} - V_{OL}$ Low noise margin.

$N_{MH} = V_{OH} - V_{IH}$ High noise margin.

$N_M = (N_{ML} + N_{MH})/2$

Noise margin



MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

Fig : Noise margin of CMOS

VIH and VIL are the operational points of the inverter where $d_{vout}/d_{vin} = -1$.

✓ **Switching Threshold:**

The switching threshold is defined as the point where $V_{in} = V_{out}$. In this region both PMOS and NMOS are always saturated since $V_{DS} = V_{GS}$.

Let us denote switching threshold as $V_M \approx (rV_{DD}) /(1 + r)$

Switching threshold is set by r which is the comparison of the driving strengths of PMOS and NMOS.

V_M is generally located at the middle of the available voltage swing ($V_{DD}/2$).

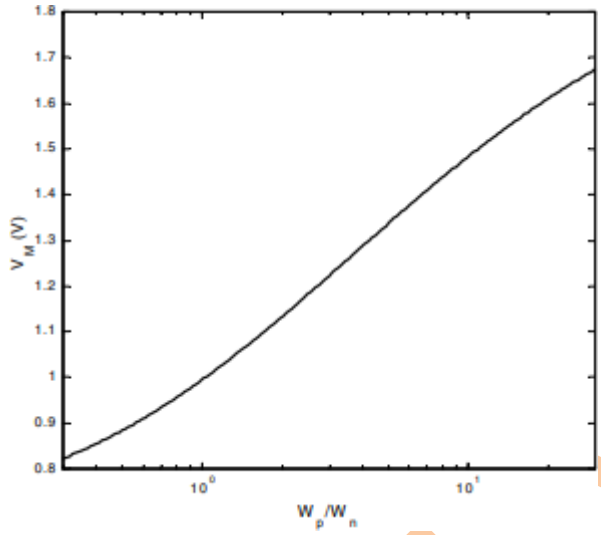
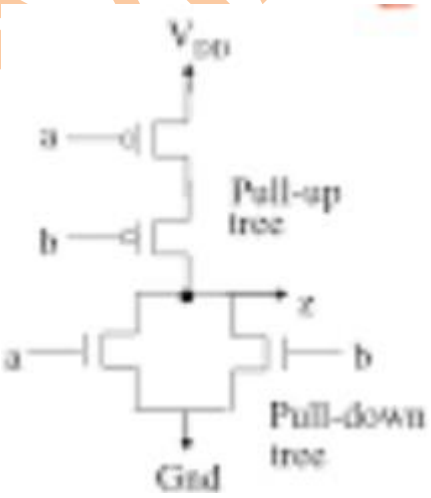


Fig 4: Switching Threshold of CMOS

Let's have analysis based on above graph:

1. VM is relatively insensitive to variations in the device ratio. This means that small variations of the ratio do not disturb the transfer characteristic that much. It is therefore accepted to set the width of the PMOS transistor to values smaller than those required for exact symmetry.
2. The effect of changing the Wp /Wn ratio is to shift the transient region of the VTC. Increasing the width of the PMOS or the NMOS moves VM towards VDD or GND respectively. This property can be very useful, as asymmetrical transfer characteristics are actually desirable in some designs.

✓ **Realizing CMOS with Boolean equations:**



MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

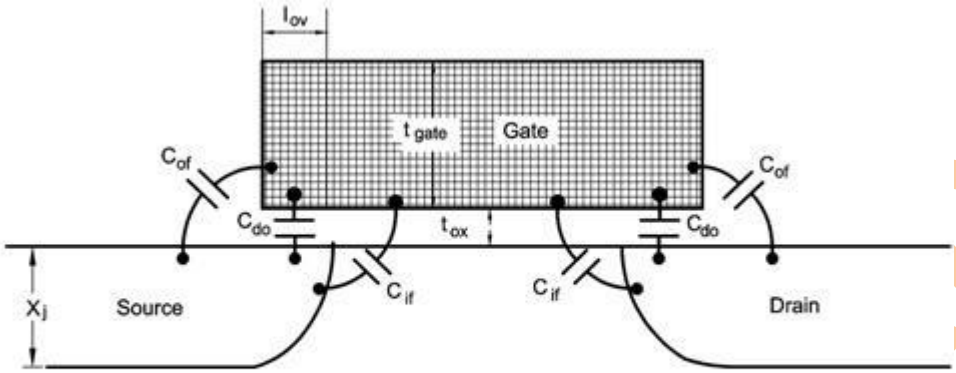
Fig: 2 input nor gate implementation using cmos

✓ CMOS capacitance:

MOSFET capacitances are of three types:

1. Overlap capacitance
2. Channel capacitance
3. Diffusion capacitance

a) Overlap capacitance:



Overlap capacitance in MOSFET

Fig : Overlap capacitance

While fabricating a MOSFET during the etching process there are chances that the gate might overlap with source and drain leading capacitance effect known as overlap capacitance.

$C_{OV} = C_{OX} . X_d . w$

Note: $C_{OX} = £_{ox}/t_{ox}$

W = width of channel

X_d = distance between two parallel plates

b) Channel capacitance:

With varying V_{GS} and V_{DS} and based on region of operation the channel capacitance varies.

1. **$V_{GS} = 0$**
   There exists no channel so capacitance is seen between metal, oxide, semiconductor (P/N substrate).
2. **$V_{GS} > V_T$; $V_{DS}>0$**
   There exists a channel and the dimension of the channel is constant so its linear region of operation and the capacitance is seen between metal, oxide, semiconductor (N/P source and N/P drain).
3. **$V_{GS} > V_T$; $V_{DS}>>0$**
   In this condition the device is at a saturation region of operation and capacitance is between metal, oxide, semiconductor (N/P source).

c) Diffusion capacitance:

As the n^+ is at drain and source is doped on to the P substrate by diffusion mechanism through the PN junction is reverse biased in MOSFET due to this fabrication we see diffusion capacitance between gate and source and in between gate and drain.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

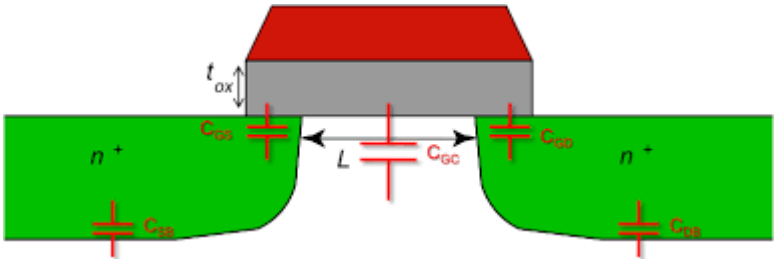


Fig : Diffusion capacitance

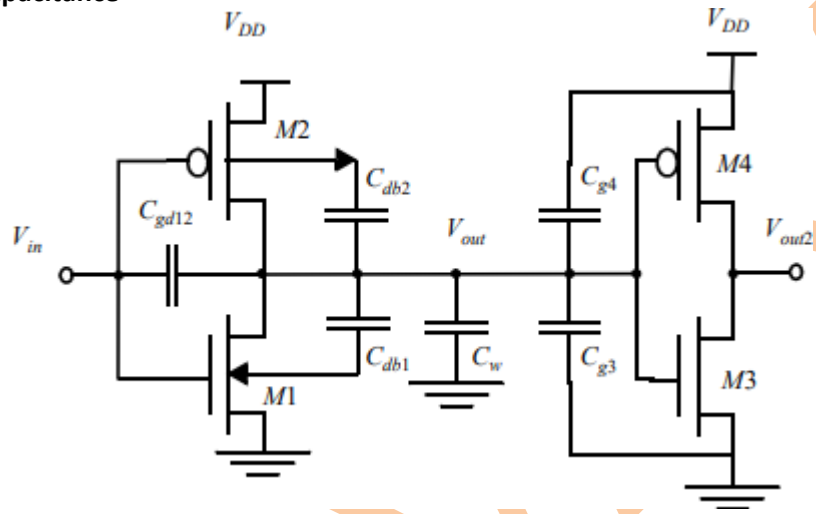


Fig : Internal and external capacitance of CMOS

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

UNIT 5 CMOS INVERTER

➢ CMOS inverter:

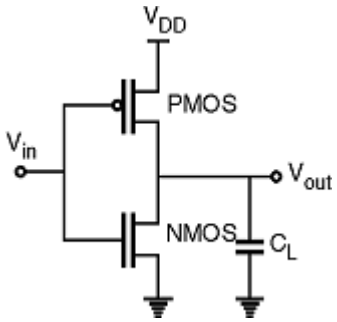


Fig : CMOS Inverter

VIN	Vout	NMOS	Region of operation for NMOS	PMOS	Region of operation for PMOS
< V_{tn}	VOH	Off	Cut off	On	Linear
VIL	≈VOH	On	Saturation	On	Linear
$V_{tn} = V_{DD}/2$	$V_{DD}/2$	On	Saturation	On	Saturation
VIH	≈VOL	On	Linear	On	Saturation
>> (V_{DD}+V_{tp})	VOL	On	Linear	Off	Linear

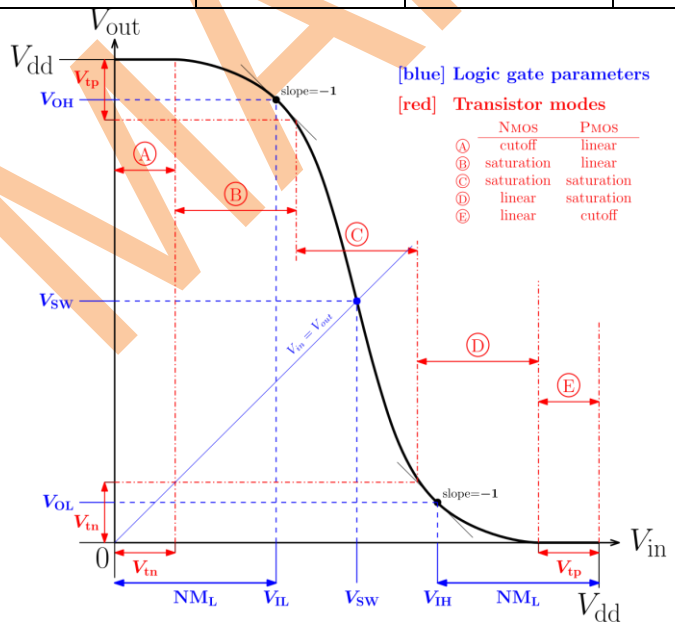


Fig : CMOS inverter characteristics

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

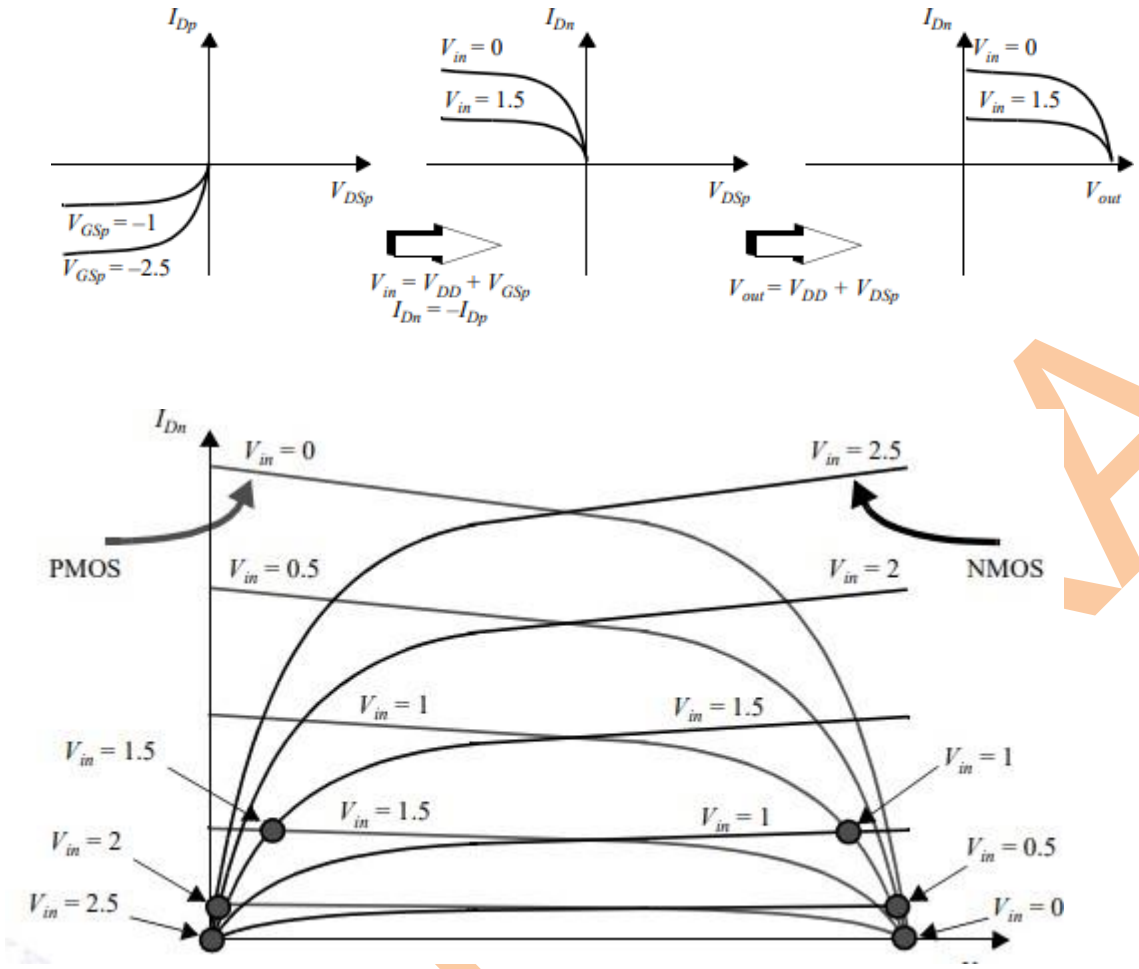


Fig : Operating point of CMOS

➢ Propagation delay:

- The time required by the signal to propagate from input to output.
- The range of clock is considered with respect to 50% of input and 50% of output voltage transitions.
- When a logic 0 is applied to the CMOS then the load capacitor starts charging. And when logic 1 is applied to the CMOS then the load capacitor starts discharging. This charging and discharging time of a capacitor is considered as propagation delay.
- Considering 1st order Rc network the time taken by C_L to charge to 50% of its final voltage is given as:

$V_{OUT} = V_{IN}(1-e^{(-t/\tau)})$

$V_{OUT} = V_{IN}/2$

$V_{IN}/2 = V_{IN}(1-e^{(-t/\tau)})$

$½ - 1 = -e^{(-t/\tau)}$; Let $\tau = RC$

$Ln(1/2) = -t/RC$

$T = 0.69RC$

- The amount of time required for the load capacitor to fully charge by the CMOS is 5τ(5RC).

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

Propagation Delay

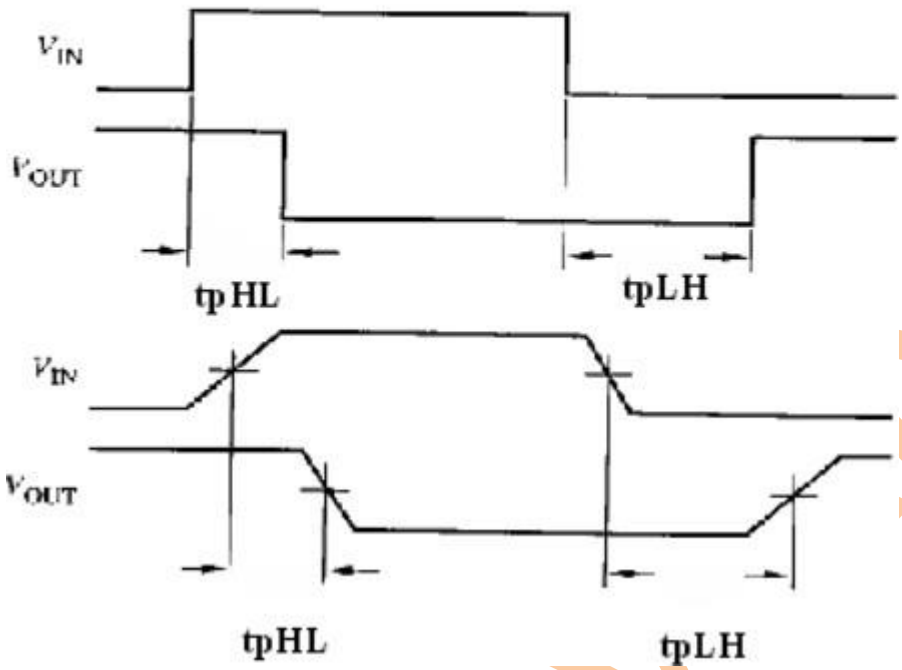


Fig : Propagation delay of CMOS

- T_f = fall time; amount of time taken to move from 90% of input to 10% of output.
- T_r = rise time; amount of time taken to move from 10% of input to 90% of output.

✓ **Techniques to reduce propagation delay:**

1. **Reduce CL :** Remember that three major factors contribute to the load capacitance: the internal diffusion capacitance of the gate itself, the interconnect capacitance, and the fanout. Careful layout helps to reduce the diffusion and interconnect capacitances. **Good design practice requires keeping the drain diffusion areas as small as possible**.

2. **Increase the W/L ratio of the transistors:** This is the most powerful and effective performance optimization. Increasing the transistor size also raises the diffusion capacitance and hence CL . In fact, once the intrinsic capacitance (i.e. the diffusion capacitance) starts to dominate the extrinsic load formed by wiring and fanout, increasing the gate size does not longer help in reducing the delay, and only makes the gate larger in area. This effect is called “self-loading”. In addition, wide transistors have a larger gate capacitance, which increases the fan-out factor of the driving gate and adversely affects its speed.

3. **Increase VDD:** The delay of a gate can be modulated by modifying the supply voltage. This flexibility allows the designer to trade-off energy dissipation for performance. However, increasing the supply voltage above a certain level yields only very minimal improvement and hence should be avoided. Also, reliability concerns (oxide breakdown, hot-electron effects) enforce firm upper-

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

bounds on the supply voltage in deep sub-micron processes.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

- The rise and fall time of a CMOS is not equal because the mobility of electrons is 2.5 times faster than the mobility of holes so to ensure both the rise and fall times to be equal one has to increase the size of PMOS by 2.5 times of NMOS.
- Long interconnect wires can also affect the propagation delay. The whole net length of wire has internal RC which affects the delay.

➢ Power dissipation:

The power dissipation of a CMOS circuit is instead dominated by the dynamic dissipation resulting from charging and discharging capacitances.

1. **Dynamic power dissipation:**

Each time the capacitor CL gets charged through the PMOS transistor, its voltage rises from 0 to VDD, and a certain amount of energy is drawn from the power supply. Part of this energy is dissipated in the PMOS device, while the remainder is stored on the load capacitor. During the high-to-low transition, this capacitor is discharged, and the stored energy is dissipated in the NMOS transistor.

Dynamic power dissipation is seen only when PMOS is on and NMOS is off.

##equation and image

Computing the dissipation of a complex circuit is complicated by the f0 ->1 factor, also called the switching activity. Switching activity is the number of times the CMOS switches from 0 to 1 transition.

Reducing VDD has a quadratic effect on dynamic power, reducing VDD might help in reducing performance but it increases the power dissipation so when the design is power critical reducing VDD does not help. In such cases, reducing effective capacitance will improve performance and power dissipation. Reducing switching times will also reduce power dissipation but the logic of the design is given by the architectural team so having a change in effective capacitance is the main tool given in the designer's hand.

2. **Direct path power dissipation:**

When both NMOS and PMOS are ON we get to see direct path power dissipation as there exists a direct path from VDD to GND.

As both NMOS and PMOS are ON there exists a short circuit current and is called Ipeak.

$P_{DP} = t_{sc}.VDD.I_{peak}.f$

3. **Static power dissipation:**

When both NMOS and PMOS are OFF we get to see static power dissipation.

In every device though it is in off state there exists a leakage current, the same is seen in OFF CMOS leading to static power dissipation.

There are 3 factors affecting the leakage current they are:

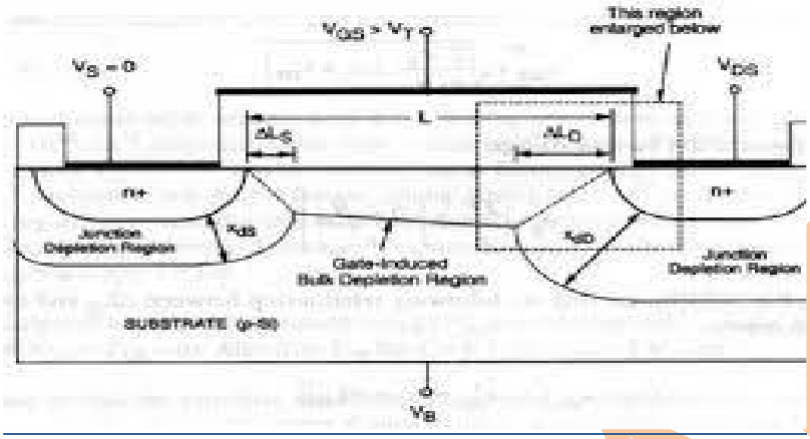
a. The reverse bias connection of PN junction leading to reverse leakage current.
b. Gate induced drain leakage.
c. Due to sub – threshold conduction.

$P_{static} = VDD.I_{leakage}$

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

UNIT 6 SHORT CHANNEL DEVICE

➢ Short channel device:



✓ **A device is said to be short channel if it has following properties:**

1. A device is called a short channel if its channel length is <1µm.
2. If the channel length is in the order of depletion region width at source and drain junction it is a short channel device.
3. If the channel length is in the order of junction depth.

✓ **Reasons for Short channel effect:**

1. High electric field:

As the channel length is less, the electric field between source and drain is high.

2. V_t variations:

The source and drain is already depleted and has to be considered as their junction depth is the same channel length. So V_{GS} for channel formation gets reduced as the depletion region of source and drain helps is pre - existence of channel before applying V_{GS}.

✓ **Short channel effects:**

1. Channel length modulation:

When $V_{DS} > V_{GS} – V_t$ the pinch off moves towards source from drain due to this the depletion width of drain keeps increasing in a manner that the whole channel is occupied by the depletion width of the drain.

Thus the effective channel decreases and is known as channel length modulation.

I_D a 1/L; L is channel length

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{T0})^2 \cdot (1 + \lambda \cdot V_{DS})$$

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

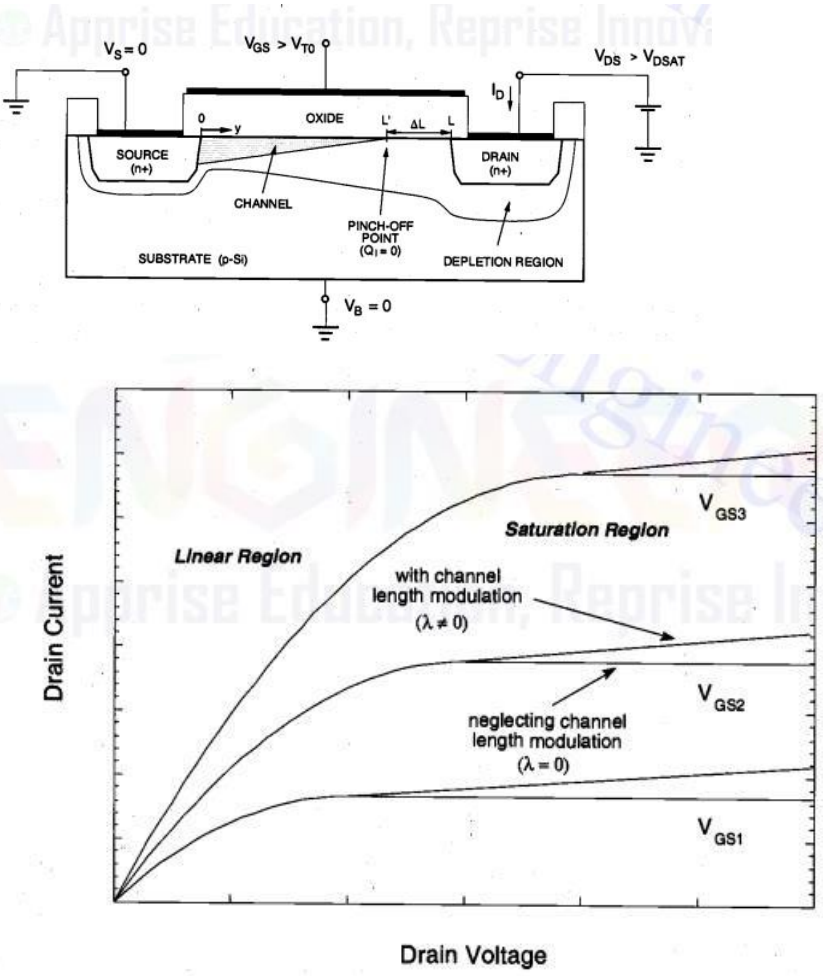


Fig : channel length modulation graph

2. Hot carrier effects:

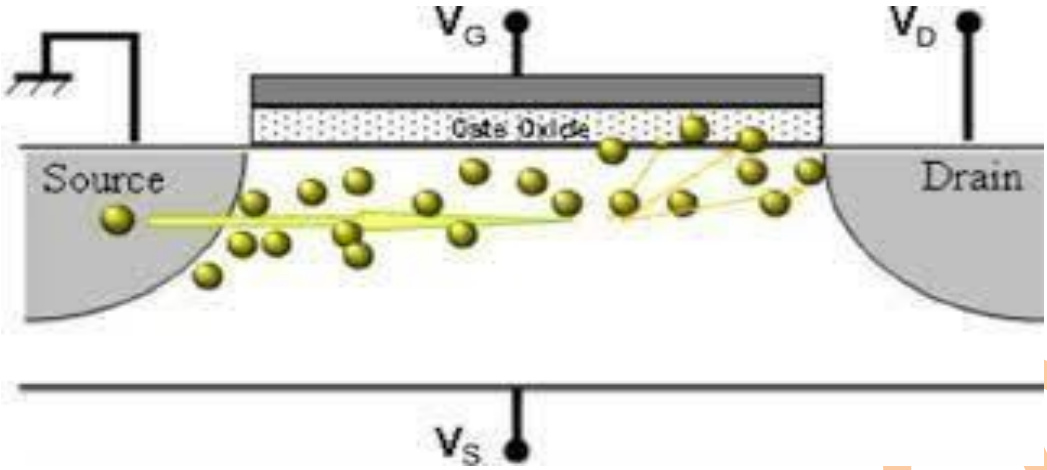
Hot carriers are the high kinetic energy carriers.

As the short channel devices have V_{DS} increasing there by high electric field is generated which leads electrons to flow from source to drain with high kinetic energy these carriers due to high electric field has tendency to break the bond and move to oxide layer from semiconductor channel leading to increase in electron concentration in oxide layer thus we see existence of charge leading to I_G not equal to 0A.

This non - zero I_G makes the device input impedance to decrease.

The electrons that have to reach the gate get trapped in oxide forming a negative charge in the oxide layer thus increasing V_T so V_{GS} has to be increased to nullify this hot carrier effect.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077



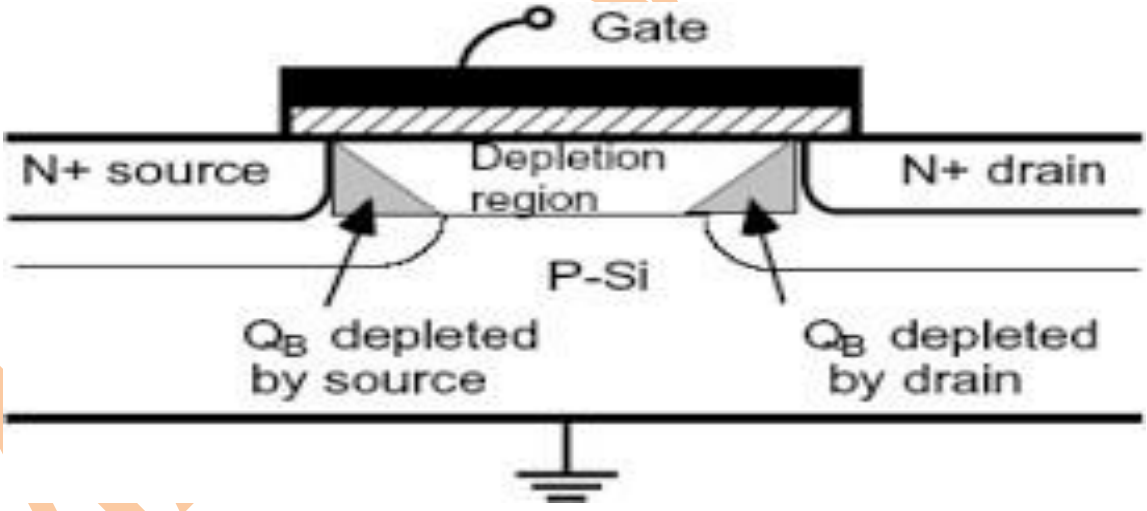
3. Drain Induced barrier lowering:

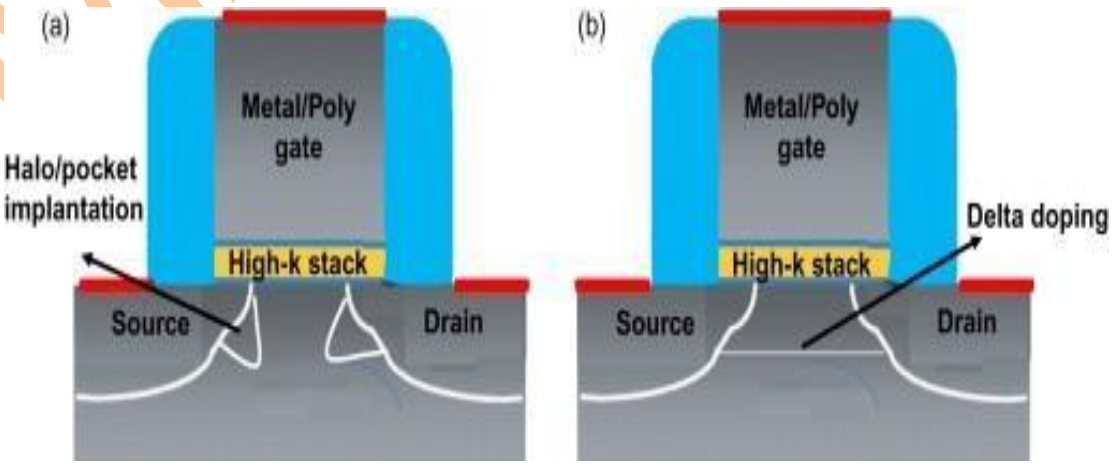
As the channel length is small and V_{DS} is kept increasing thus the depletion region of the drain is increased and thus the electric field increases.

This depletion region causes an electric field around the source due to the charges present in the drain. These charges reduce the junction of source thus known as drain induced barrier lowering as the drain charges are the cause of the reduction in source junction.

Due to presence of charges in the channel region there happens to see the reduction in V_T.

This effect where the channel region is completely getting occupied by depletion regions and resulting in high electric fields is called the **Punch through effect.**





MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

Fig : Drain induced barrier lowering effect cause of punch through effect

4. Electro migration:

We get to see this effect in lower technology nodes as the channel length reduces the interconnect spacing decreasing.

When high current density passes through a metal interconnect, the momentum of current carrying electrons may get transferred to metal ions during collision between them. Due to momentum transfer, the metal ions get drifted in the direction of motion of electrons. Such drift of metal ions from its original position is called electro migration.

This means that when a metal needs to carry a higher density of charges than its capacity we get to see crests and troughs in the metal known as hillocks and voids which means short and open respectively.

When high density of carriers are passed in the metal the atoms get staggered leading to short known as hillocks.

When the hillocks are formed due to a staggering amount of atoms the other region will be depleted of charges as it has less density of charges leading to open holes known as voids.

Current density J is defined as the current following per unit cross-section area.

$$J = I/A$$

Where I is the current and A is the cross-section of the area of interconnect.

As the technology node shrinks, Cross-sectional area of the metal interconnects also shrinks and the current density increases to a great extent in the lower node. Electro migration has been a problem since the 90 nm technology node or even earlier but it gets worse in lower technology node 28nm or lower node.

Depending on the current density, the subject metal ion started drifting in the opposite direction of the electric field. If the current density is high, the interconnect may get affected by EM instantly or sometimes the effect may come after months/years of operation depending on current density. So the reliability of ASIC will depend upon this EM effect.

Mean Time To Failure (MTTF) is an indication of the life span of an integrated circuit. MTTF is calculated using Black's equation as below.

$$\text{MTTF} = \frac{A}{J^N} exp(\frac{Ea}{k.T})$$

Where A = Cross-Section area
J = Current density
N = Scaling factor (normally set to 2)
Ea = Activation energy
K = Boltzmann's constant
T = Temperature in Kelvin

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

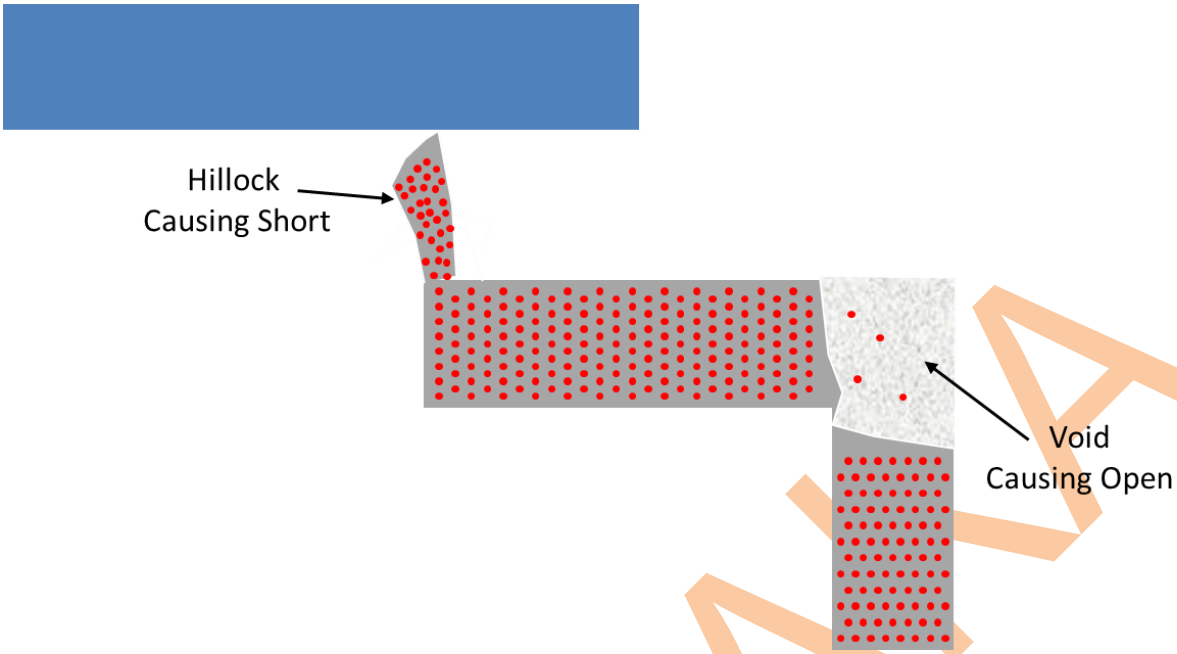


Fig : Electromigration in metal wire

5. Latch up:

The internal structure of CMOS has back to back connected PNP and NPN transistors as feedback in a positive loop.

This back to back connection of PMOS and NMOS leads to a low impedance path from supply to ground that allows heavy current flow in the path which could damage the device.

This low impedance path can be over - come by decreasing the R (resistance) or by creating guard rings or by forming shallow isolation trench between PMOS and NMOS.

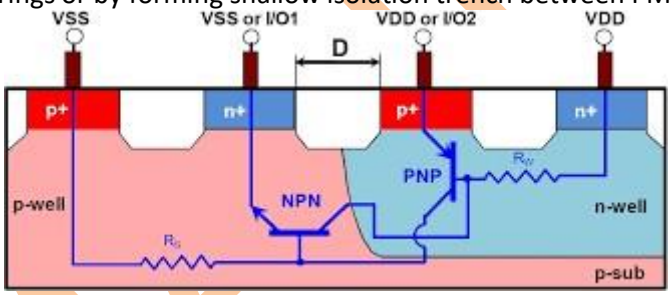


Fig : Back to back connection of NPN transistor in CMOS

6. Sub - threshold conduction:

As V_{DS} is increased and the channel is occupied by depletion region of drain leading to increase in electric field and thus the presence of channel before threshold is attained by the device it is called as subthreshold conduction.

Thus the conduction occurs when $V_{GS} < V_T$.

This effect can lead to damage to the device due to high current.

So in a short channel device we need to ensure how fast the V_{GS} starts reducing below V_T so that the I_d is reduced by a factor of 10. This principle is called the slope factor.

Once slope factor of a device is taken to consider the damage of the device.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

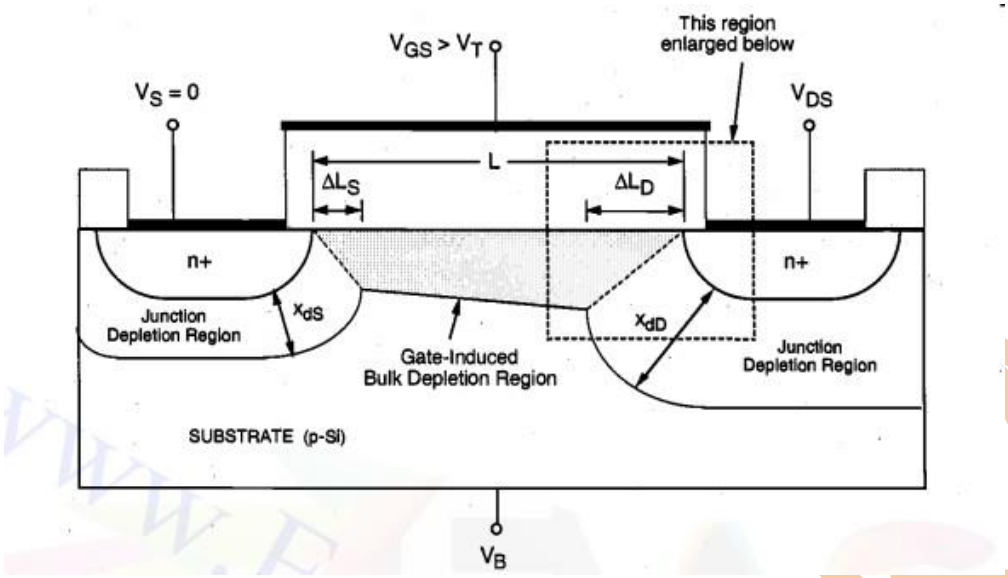


Fig : subthreshold conduction

7. Gate induced drain leakage:

GIDL occurs when the gate partially overlaps source and drain and when V_{DS} is high and V_{GS} is at low potential.

The gate drain overlap region is present due to band to band tunnelling effect as the depletion region of drain keeps increasing in a manner that at some point of V_{DS} the electrons from valence band tunnel towards the oxide's conduction band known as band to band tunnelling effect.

This tunnelling effect leads to leakage current at drain which is induced by the gate thus gate induced drain leakage.

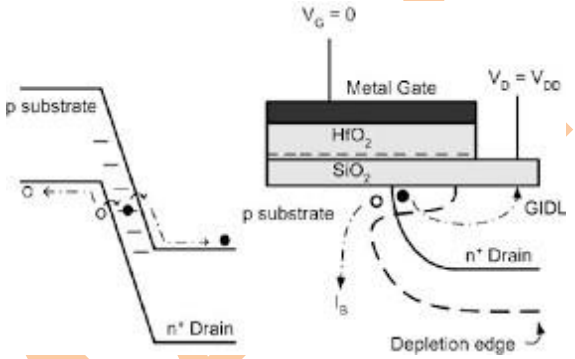


Fig : Gate induced drain leakage

8. Body bias effect:

Body effect refers to the change in the threshold voltage of the device when there is a difference between substrate(body) and source voltages. Body bias is usually the lowest voltage in the chip. However, if we were to connect Vbuilt to a voltage lower than VSS (Source voltage), there is an increased flow of carriers between these source-bulk junctions thereby increasing the width of the depletion region. This in turns increases the minimum gate voltage needed to achieve channel inversion.

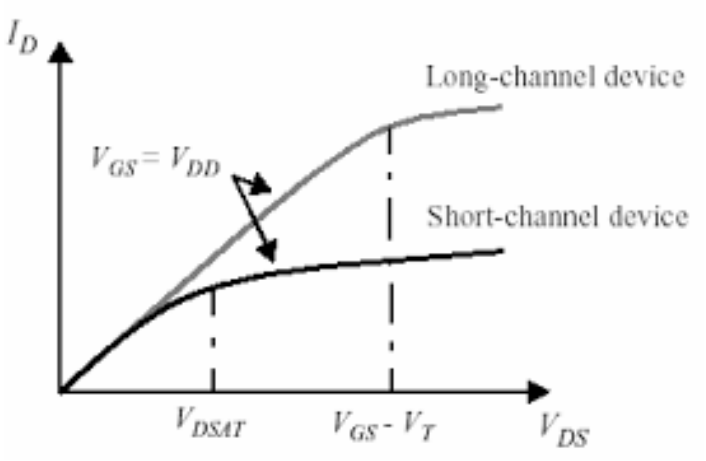
9. Velocity saturation:

As there exists drain's depletion region over the channel region due to the presence of V_{DS} the electric field saturates the mobility of electrons at the pinch off point thereby creating saturation of current before the device could enter into the saturation region.

$V_{DS} < V_{DSsat}$

Due to the existence of saturation prior to the V_{DSsat} the saturation of the device is extended and the drain current is small.

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077



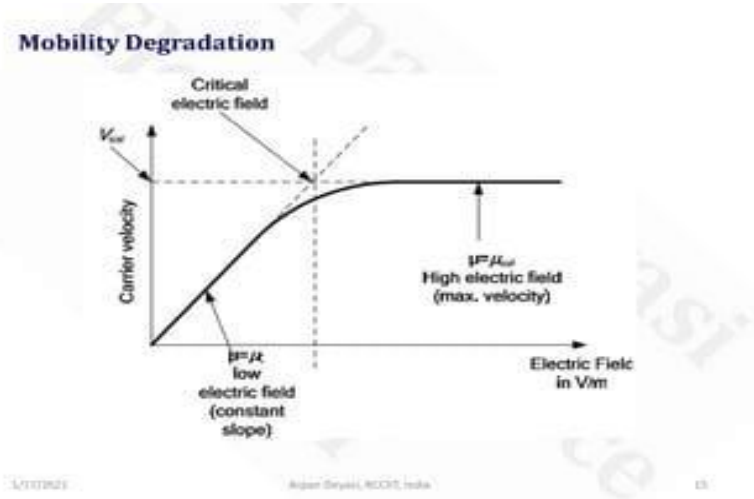


Fig 7: Velocity saturation curve

USEFUL FORMULAS

- **Formulas**

1. Resistance

R = ρL/A

2. Conductivity

σ = neμ

3. Capacitance

C = dq/dv

4. Oxide capacitance

$C_{ox} = \varepsilon_{ox}/t_{ox}$

5. Diffusion charge density

$J_{diffusion} = qD_n \Delta_n$

6. Drift charge density

$J_{drift} = q\mu nE$

7. Electron and hole concentration

N = p = n_i : in intrinsic semiconductor

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077

$N = N_D$: N type semiconductor

$P = N_A$: P type semiconductor

8. Velocity

$V_d = \mu E$

9. Current density

$J = I/A$; σEA

10. Current

$I = V/R$; $ne\mu A$

11. LATTICE SCATTERING AND TOTAL SCATRING

$1/u = 1/u1 + 1/u2\ldots$

12. V_T equation

$V_T = V_{to} + \Upsilon\ (\sqrt{(2\emptyset F + VSB)} - \sqrt{2\emptyset F}\ )$

13. PN junction voltage

$V_O = KT/q(N_A * N_D/n_i^2)$

MANIKANTHA VAKA
manikanthavaka1@gmail.com
8639790077