Timing Analysis

Timing Path Groups and Types

- **Timing paths are grouped into** *path groups* **according to the clock associated with the** *endpoint* **of the path.**
- **There is a** *default path group* **that includes all asynchronous paths.**
- **There are two timing** *path types*: *max* **and** *min*.
  - **Path type: max - reports timing paths that check setup violations.**
  - **Path type: min - reports timing paths that check hold violations.**
- **Design Compiler works primarily on the most critical path in each** *path group*.

Timing Path Groups and Types

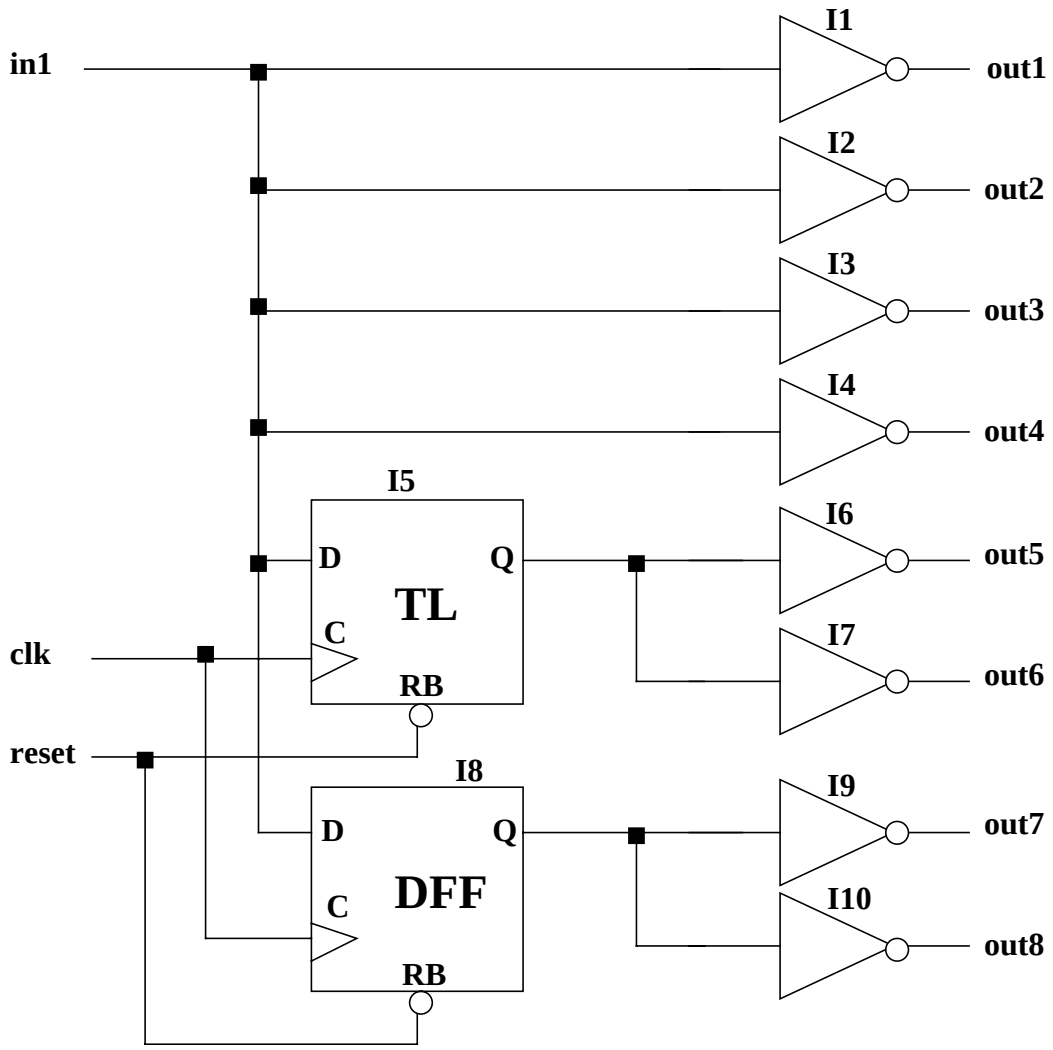
group_path [**-weight** weight_value] [**-critical_range** range_value]
-name group_name [**-from** from_list] [**-through** through_list] [**-to** to_list]

- **Separates specific paths into a path group. Avoids some violating paths blocking others. Also for multiple critical paths to a single endpoint.**
- **The violations are multiplied by weight_value to determine the cost. Allows important paths to be improved at the cost of less important ones. 0.0 <= weight_value <= 100.0 (default 1.0)**
- **The critical_range determines which paths other than the worst violator in the group will be optimized. All paths whose timing violation is within critical_range of the worst violator are optimized. Often improves results with a cost of longer compile times.**
- **The variable compile_default_critical_range may be used to change the default critical range. (0.0)**

Example:

```
group_path -name txclav_out -to TXCLAV
```

Timing Paths Example



Timing Paths Example (cont.)

```
source -echo -verbose ../../general_tcl/ppcec_libs.include.tcl

read_file -f verilog try.v

source -echo -verb ../../general_tcl/ppcec_general.include.tcl
create_clock clk -period 20000 -waveform {0 10000}
remove_driving_cell [get_ports clk]
set_clock_skew -propagated {clk}
set_dont_touch_network {clk}

set_false_path -from reset

set_input_delay -max 7500 -clock clk in1
set_input_delay -min   10 -clock clk in1

set_output_delay 6000 -clock clk -clock_fall {out1 out7}
set_output_delay 11000 -clock clk {out2 out6 out8}

set_output_delay 18000 -clock clk -clock_fall out3
set_multicycle_path -setup 2 -to out3
set_multicycle_path -hold  1 -to out3

set_output_delay 18000 -clock clk out4
set_multicycle_path -setup 2 -from in1 -to out4
set_multicycle_path -hold  1 -from in1 -to out4

set_output_delay 2000 -clock clk -clock_fall {out5}

set_load 0.2 [all_outputs]
set_resistance 100 [get_nets "*"]

report_timing -path full -input_pins -delay max -nworst 4 -
max_paths 10000 > try.timing_report
report_timing -path full -input_pins -delay min > try.timing_min

quit
```

Timing Paths Example (cont.)

```
Startpoint: in1 (input port clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: clk
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                    0.00       0.00
clock network delay (propagated)         0.00       0.00
input external delay                  7500.00    7500.00 f
in1 (in)                               142.37    7642.37 f
i1/INPUT1 (iinvc)                        0.33    7642.70 f
i1/OUTPUT1 (iinvc)                    1469.09    9111.79 r
out1 (out)                              14.66    9126.45 r
data arrival time                                9126.45

clock clk (fall edge)                10000.00   10000.00
clock network delay (propagated)         0.00   10000.00
output external delay                -6000.00    4000.00
data required time                               4000.00
-----------------------------------------------------------
data required time                               4000.00
data arrival time                               -9126.45
-----------------------------------------------------------
slack (VIOLATED)                                -5126.45
```

Timing Paths Example (cont.)

```
Startpoint: in1 (input port clocked by clk)
Endpoint: out1 (output port clocked by clk)
Path Group: clk
Path Type: max

Point                                     Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                     0.00       0.00
clock network delay (propagated)          0.00       0.00
input external delay                   7500.00    7500.00 r
in1 (in)                                247.42    7747.42 r
i1/INPUT1 (iinvc)                         0.33    7747.75 r
i1/OUTPUT1 (iinvc)                      865.39    8613.14 f
out1 (out)                               14.66    8627.80 f
data arrival time                                 8627.80

clock clk (fall edge)                  10000.00   10000.00
clock network delay (propagated)           0.00   10000.00
output external delay                  -6000.00    4000.00
data required time                                 4000.00
-----------------------------------------------------------
data required time                                 4000.00
data arrival time                                 -8627.80
-----------------------------------------------------------
slack (VIOLATED)                                  -4627.80
```

Timing Paths Example (cont.)

```
Startpoint: in1 (input port clocked by clk)
 Endpoint: out2 (output port clocked by clk)
 Path Group: clk
 Path Type: max

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock clk (rise edge)                    0.00       0.00
 clock network delay (propagated)         0.00       0.00
 input external delay                  7500.00    7500.00 f
 in1 (in)                               142.37    7642.37 f
 i2/INPUT1 (iinvc)                        0.33    7642.70 f
 i2/OUTPUT1 (iinvc)                    1469.09    9111.79 r
 out2 (out)                              14.66    9126.45 r
 data arrival time                                9126.45

 clock clk (rise edge)                20000.00   20000.00
 clock network delay (propagated)         0.00   20000.00
 output external delay                -11000.00   9000.00
 data required time                               9000.00
 -----------------------------------------------------------
 data required time                               9000.00
 data arrival time                               -9126.45
 -----------------------------------------------------------
 slack (VIOLATED)                                 -126.45
```

Timing Paths Example (cont.)

```
Startpoint: in1 (input port clocked by clk)
 Endpoint: out3 (output port clocked by clk)
 Path Group: clk
 Path Type: max

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock clk (rise edge)                    0.00       0.00
 clock network delay (propagated)         0.00       0.00
 input external delay                  7500.00    7500.00 f
 in1 (in)                               142.37    7642.37 f
 i3/INPUT1 (iinvc)                        0.33    7642.70 f
 i3/OUTPUT1 (iinvc)                    1469.09    9111.79 r
 out3 (out)                              14.66    9126.45 r
 data arrival time                                9126.45

 clock clk (fall edge)                30000.00   30000.00
 clock network delay (propagated)         0.00   30000.00
 output external delay                -18000.00  12000.00
 data required time                              12000.00
 -----------------------------------------------------------
 data required time                              12000.00
 data arrival time                               -9126.45
 -----------------------------------------------------------
 slack (MET)                                      2873.55
```

Timing Paths Example (cont.)

```
Startpoint: in1 (input port clocked by clk)
 Endpoint: out4 (output port clocked by clk)
 Path Group: clk
 Path Type: max

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock clk (rise edge)                    0.00       0.00
 clock network delay (propagated)         0.00       0.00
 input external delay                  7500.00    7500.00 f
 in1 (in)                               142.37    7642.37 f
 i4/INPUT1 (iinvc)                        0.33    7642.70 f
 i4/OUTPUT1 (iinvc)                    1469.09    9111.79 r
 out4 (out)                              14.66    9126.45 r
 data arrival time                                9126.45

 clock clk (rise edge)                40000.00   40000.00
 clock network delay (propagated)         0.00   40000.00
 output external delay                -18000.00  22000.00
 data required time                              22000.00
 -----------------------------------------------------------
 data required time                              22000.00
 data arrival time                               -9126.45
 -----------------------------------------------------------
 slack (MET)                                     12873.55
```

Timing Paths Example (cont.)

```
  Startpoint: in1 (input port clocked by clk)
  Endpoint: i8 (rising edge-triggered flip-flop clocked by
clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (propagated)         0.00       0.00
  input external delay                  7500.00    7500.00 r
  in1 (in)                               247.42    7747.42 r
  i8/D (dffrpc)                            0.26    7747.69 r
  data arrival time                                7747.69

  clock clk (rise edge)                20000.00   20000.00
  clock network delay (propagated)         1.57   20001.57
  i8/C (dffrpc)                            0.00   20001.57 r
  library setup time                   -2012.22   17989.35
  data required time                              17989.35
  -----------------------------------------------------------
  data required time                              17989.35
  data arrival time                               -7747.69
  -----------------------------------------------------------
  slack (MET)                                     10241.67
```

Timing Paths Example (cont.)

```
 Startpoint: i8 (rising edge-triggered flip-flop clocked by
clk)
  Endpoint: out7 (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (propagated)         1.57       1.57
  i8/C (dffrpc)                            0.00       1.57 r
  i8/Q (dffrpc)                         2353.59    2355.16 f
  i9/INPUT1 (iinvc)                        0.99    2356.15 f
  i9/OUTPUT1 (iinvc)                    1484.35    3840.50 r
  out7 (out)                              14.66    3855.16 r
  data arrival time                                3855.16

  clock clk (fall edge)                10000.00   10000.00
  clock network delay (propagated)         0.00   10000.00
  output external delay                -6000.00    4000.00
  data required time                               4000.00
  -----------------------------------------------------------
  data required time                               4000.00
  data arrival time                               -3855.16
  -----------------------------------------------------------
  slack (MET)                                       144.84
```

Timing Paths Example (cont.)

```
Startpoint: i8 (rising edge-triggered flip-flop clocked by clk)
Endpoint: out8 (output port clocked by clk)
Path Group: clk
Path Type: max

Point                                     Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                     0.00       0.00
clock network delay (propagated)          1.57       1.57
i8/C (dffrpc)                             0.00       1.57 r
i8/Q (dffrpc)                          2353.59    2355.16 f
i10/INPUT1 (iinvc)                        0.99    2356.15 f
i10/OUTPUT1 (iinvc)                    1484.35    3840.50 r
out8 (out)                               14.66    3855.16 r
data arrival time                                 3855.16

clock clk (rise edge)                 20000.00   20000.00
clock network delay (propagated)          0.00   20000.00
output external delay                -11000.00    9000.00
data required time                                9000.00
-----------------------------------------------------------
data required time                                9000.00
data arrival time                                -3855.16
-----------------------------------------------------------
slack (MET)                                       5144.84
```

Timing Paths Example (cont.)

```
Startpoint: in1 (input port clocked by clk)
Endpoint: i5 (positive level-sensitive latch clocked by clk)
Path Group: clk
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                    0.00       0.00
clock network delay (propagated)         0.00       0.00
input external delay                  7500.00    7500.00 r
in1 (in)                               247.42    7747.42 r
i5/D (itlripc)                           0.34    7747.76 r
data arrival time                                7747.76

clock clk (rise edge)                    0.00       0.00
clock network delay (propagated)         0.97       0.97
i5/C (itlripc)                           0.00       0.97 r
time borrowed from endpoint           7746.79    7747.76
data required time                               7747.76
-----------------------------------------------------------
data required time                               7747.76
data arrival time                               -7747.76
-----------------------------------------------------------
slack (MET)                                         0.00

Time Borrowing Information
-------------------------------------------
clk pulse width                      10000.00
library setup time                   -1363.35
-------------------------------------------
max time borrow                       8636.65
actual time borrow                    7746.79
-------------------------------------------
```

Timing Paths Example (cont.)

```
 Startpoint: i5 (positive level-sensitive latch clocked by
clk)
  Endpoint: out5 (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (propagated)         0.97       0.97
  time given to startpoint              7641.73    7642.71
  i5/D (itlripc)                           0.00    7642.71 f
  i5/Q (itlripc)                        1657.49    9300.20 f
  i6/INPUT1 (iinvc)                        0.99    9301.18 f
  i6/OUTPUT1 (iinvc)                    1529.34   10830.52 r
  out5 (out)                              14.66   10845.18 r
  data arrival time                                10845.18

  clock clk (fall edge)                10000.00   10000.00
  clock network delay (propagated)         0.00   10000.00
  output external delay                -2000.00    8000.00
  data required time                               8000.00
  -----------------------------------------------------------
  data required time                               8000.00
  data arrival time                              -10845.18
  -----------------------------------------------------------
  slack (VIOLATED)                               -2845.18
```

Timing Paths Example (cont.)

```
 Startpoint: i5 (positive level-sensitive latch clocked by
clk)
  Endpoint: out6 (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (propagated)         0.97       0.97
  time given to startpoint              7641.73    7642.71
  i5/D (itlripc)                           0.00    7642.71 f
  i5/Q (itlripc)                        1657.49    9300.20 f
  i7/INPUT1 (iinvc)                        0.99    9301.18 f
  i7/OUTPUT1 (iinvc)                    1529.34   10830.52 r
  out6 (out)                              14.66   10845.18 r
  data arrival time                                10845.18

  clock clk (rise edge)                20000.00   20000.00
  clock network delay (propagated)         0.00   20000.00
  output external delay                -11000.00    9000.00
  data required time                               9000.00
  -----------------------------------------------------------
  data required time                               9000.00
  data arrival time                              -10845.18
  -----------------------------------------------------------
  slack (VIOLATED)                               -1845.18
```

Timing Report Order

1. max paths before min paths
2. path groups in alphabetical order
3. paths ordered from worst timing to best timing within each group

Min Timing Path Example

```
Startpoint: in1 (input port clocked by clk)
 Endpoint: i8 (rising edge-triggered flip-flop clocked by clk)
 Path Group: clk
 Path Type: min

 Point                                    Incr       Path
 -----------------------------------------------------------
 clock clk (rise edge)                    0.00       0.00
 clock network delay (propagated)         0.00       0.00
 input external delay                    10.00      10.00 f
 in1 (in)                               142.37     152.37 f
 i8/D (dffrpc)                            0.26     152.63 f
 data arrival time                                 152.63

 clock clk (rise edge)                    0.00       0.00
 clock network delay (propagated)         1.57       1.57
 i8/C (dffrpc)                            0.00       1.57 r
 library hold time                       11.69      13.26
 data required time                                 13.26
 -----------------------------------------------------------
 data required time                                 13.26
 data arrival time                                -152.63
 -----------------------------------------------------------
 slack (MET)                                       139.37
```

Fixing Hold Time Violations

set_fix_hold clock_list

- **Used to fix hold time violations relative to the clock(s). Buffers will be added to lengthen the path as long as the setup constraint path is not violated.**
- **set_cost_priority can be used to give the min_delay constraints higher priority. [Note: Hold-time violations are often circuit bugs; setup violations 'only' limit the operating frequency.]**
- **Min paths should be checked using both BCS and WCS libraries, if possible.**

Example:

```
set_fix_hold [all_clocks]
```