ECE5019	COMPUTER AIDED DESIGN FOR VLSI	L	T	P	J	C
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Pre-requisite	**Nil**				**v 1.0**	

Course Objective :

The course is aimed to

1. imbibe the students with the fundamentals of graphs, the relevance and, their applications to VLSI design automation.
2. introduce the students with relevant examples the estimation of computational complexity and the general classes of computational problems.
3. explain With relevant examples and algorithms demonstrate partitioning, floor planning, area routing, clock routing and pin assignment of physical design flow

Expected Course Outcome :

At the end of the course students will be able to

1. Formulate the graphs for the given problems;
2. Calculate and analyse the computational complexity of physical design algorithms;
3. Partition a given design.
4. Express and change the floorplans in an abstract manner and use computer algorithms to make large and optimized floorplans
5. Make optimized placements on the silicon chip and perform complex routing using algorithms and computer codes.
6. Design clock trees to distribute the clock signals on the chip while satisfying various constraints like clock skew and wire length.

Student Learning Outcomes (SLO): **1, 6**

Module:1	**Introduction to course**	**5 hours**

Y Chart- Physical design top down flow- Review of graph theory: complete graph, connected graph, sub graph, isomorphism, bi partite graph tree.

Module:2	**Computational complexity of algorithms**	**4 hours**

Big-O notation- Class P- class NP -NP-hard- NP-complete.

Module:3	**Partitioning**	**6 hours**

Problem formulation- Group Migration Algorithm: Kernighan-Lin Simulated annealing based Partitioning.

Module:4	**Floor planning**	**6hours**

Stock Meyer algorithm- Wong-Liu algorithm (Normalized polish expression)- Integer Linear Programming (ILP) based floor planning.

Module:5	**Pin Assignment and Placement**	**7hours**

Pin Assignment: Concentric circle mapping, Topological pin assignment- Power and ground routing.

Placement: Wire length estimation models for placement - Quadratic placement- Sequence pair technique.		
Module:6	**Routing**	**8hours**
Routing: Grid routing- Maze routing- Line Probe algorithms, Weighted Steiner tree approach. Global routing: Rectilinear routing(spanning tree, steiner tree)-Dijkstra's algorithm-routing by ILP Detailed routing: Problem formulation- Two layer channel routing : Left Edge algorithm, Dogleg router- Net Merge channel router - Three-layer channel routing - HVH, VHV router- Introduction to switch box routing.		
Module:7	**Clocking Tree Topologies**	**7hours**
Clocking tree topologies: H-tree, Xtree- Method of Means and Medians (MMM)- recursive geometric matching- Elmore delay model to calculate skew- Buffer insertion in clock trees- Exact Zero skew clock routing algorithm. Clock mesh topologies: uniform and non-uniform mesh.		
Module:8	**Contemporary issues:**	**2hours**
	Total Lecture hours:	**45hours**

Text Book(s)	
1.	Andrew B. Kahng, Jens Lienig, Igor L. Markov, JinHu,VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer, 2011.
2	H. Yosuff and S.M. Sait, VLSI Physical Design Automation – Theory and Practice, Cambridge India, 2010.
3.	Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer India, 2011.
Reference Books	
1.	S. Sridhar, Design and Analysis of Algorithms, Paperback – OUP, 2014.
2.	John OkyereAttia, PSPICE and MATLAB for Electronics: An Integrated Approach,CRC Press, 2010.
3.	Ganesh M.Magar, Swati R.Maurya Rajesh K.Maurya, Graph Theory & Applications, Technical Publications, 2016.
4	Brian Christian and Tom Griffiths , Algorithms to Live By: The Computer Science of Human Decisions, William Collins, 2017.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).		
Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016