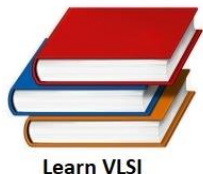
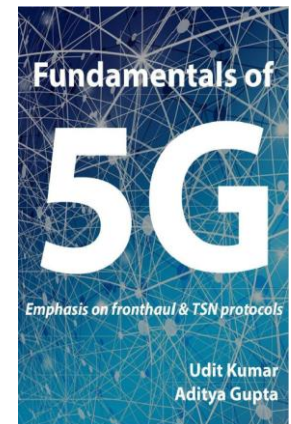
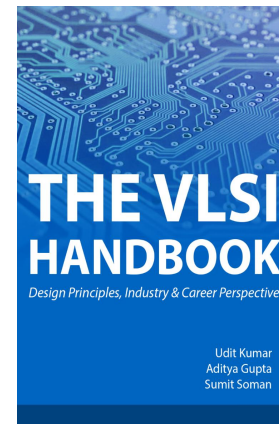


How to start career in VLSI?

Udit Kumar, PhD, IIT Delhi.

16+ years experience, Author

<https://www.linkedin.com/in/udit-kumar-phd-iit-delhi>



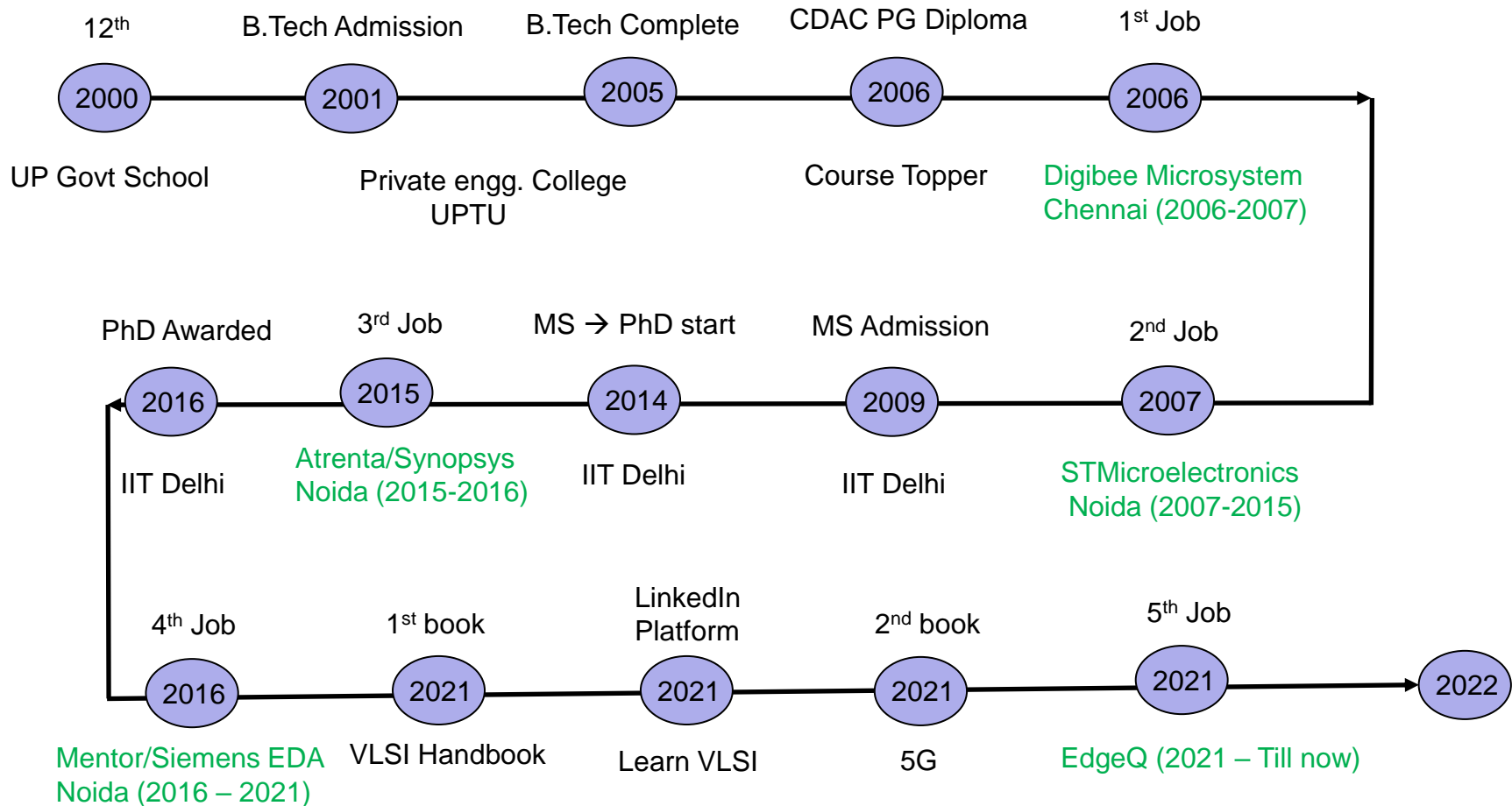
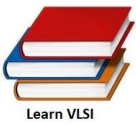
LinkedIn: <https://www.linkedin.com/company/learnvlsi>

Website: <https://www.sites.google.com/view/learnvlsi>

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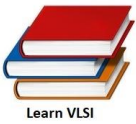
- Challenges for Students
- Dilemmas for higher studies
- VLSI work profile and Key areas
- Study topics
 - Common, Design & Verification, Design specific, Verification specific, Implementation/PD, DFT topics
- Projects
- Job Search Preparation
- LinkedIn Profile and Resume Preparation
- An effective way of using reference
- Open-source tools

About me: Udit Kumar



- The world is full of good and helping people.
- Continuous effort is key.

Statutory warning



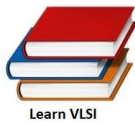
- The intention of this presentation is to give guidance to the students and learners.
- Consider shared information as advice only, We explicitly disclaim any liability resulting from these suggestions/guidance.
- Each individual may have different situation, so final decision must be taken by Individual only after consideration of everything.

Electronics is everywhere



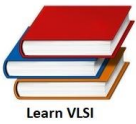
Electronics play key role of any modern device.

Challenges for Students



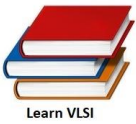
- There is gap in the academic study vs Industry expectations.
- Universities/Colleges are having limited VLSI faculties, and less alumni network.
 - ⦿ Especially for tier 2 and tier 3 colleges.
- Many people want to switch from other profile to VLSI profiles or Starting job after Career Break.
- Lack of guidance and awareness is a big challenge for students & candidates at the early stage of their careers.

Dilemmas for higher studies



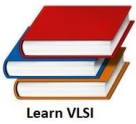
- Training Vs Masters
 - ⦿ Short term trainings are good to provide a decent degree of exposure.
 - ⦿ Master degree provides a chance to get a brand name and in-depth understanding of the field.
- Salaries and Growth are similar.
- Do 6 months course from a good training Institute
 - ⦿ CDAC Pune is one of the best.
- Master should be done from a reputed Institute, otherwise same struggle even after spending 2 years.

Motivation for PhD



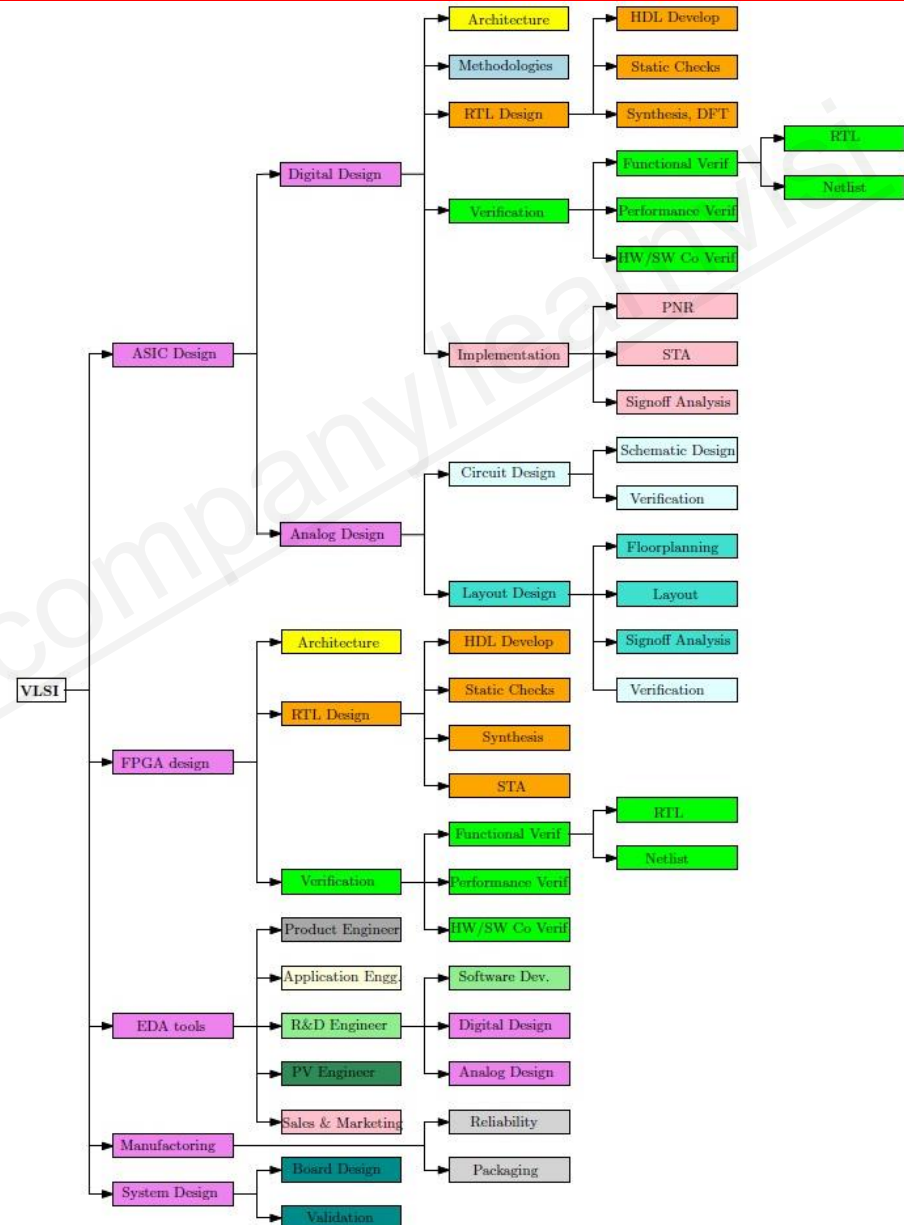
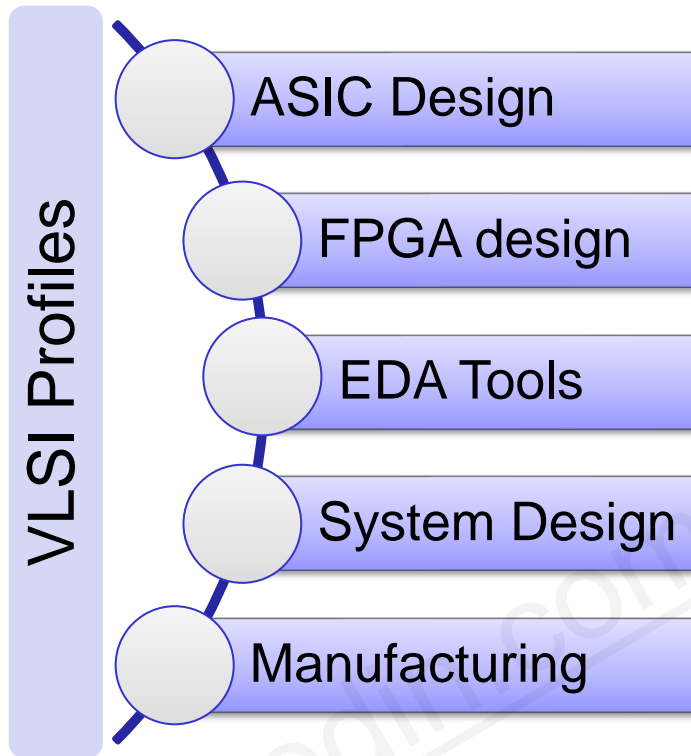
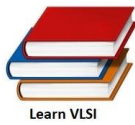
- Different candidate has different motivation, e.g.
 - ⊙ Building the career in research, both in corporate & academics.
 - ⊙ Building the career into teaching.
 - ⊙ Gaining the expertise into own interest area.
- Benefits of PhD
 - ⊙ PhD is a training process, preparing students to systematically analyze, solve and present the problem.
 - ⊙ Opportunity to learn in a wider scope, which is many times not possible in your routine job.
 - ⊙ If Graduation is from less known place, so doing PhD from a reputed University also brings brand value.

Key areas

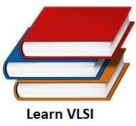


- At starting stage of career
 - ⊙ Our focus should be to enter the field, the profile can be changed over time.
 - ⊙ Our focus should be on learning in any job vs the salary.
 - ⊙ Initial 5 years of the learning will shape the future of the career.
- Key Profiles
 - ⊙ Design and Verification (DV)
 - ⊙ Physical Design (PD)
 - ⊙ DFT
 - ⊙ EDA/CAD/Flow development
- Design Verification (DV) and Physical design (PD) needs more people.

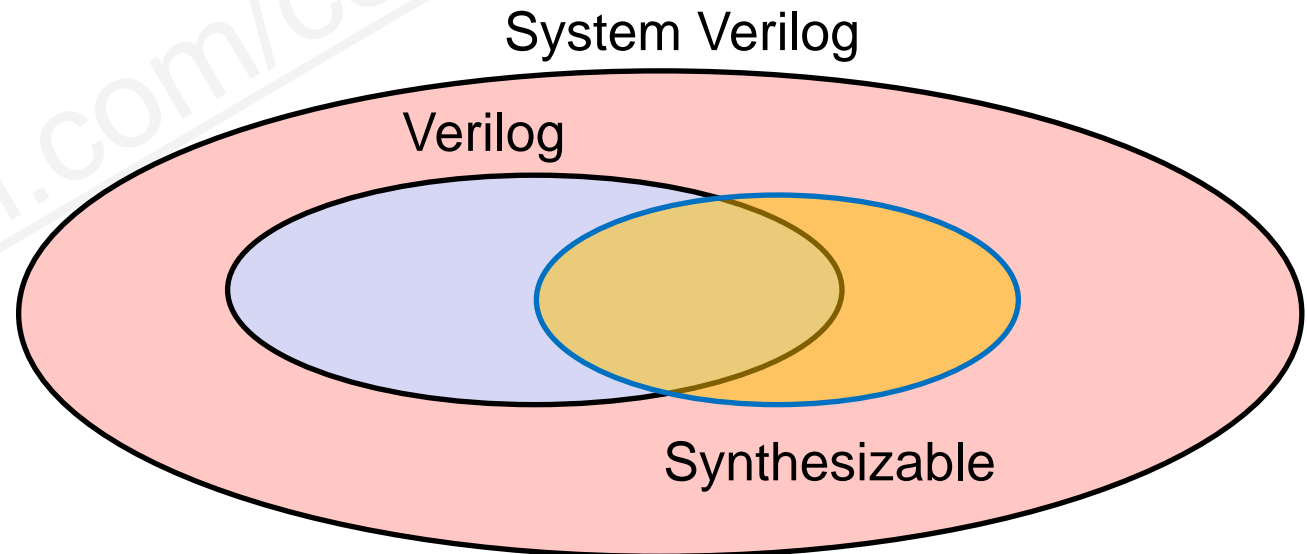
VLSI Industry work profiles and roles



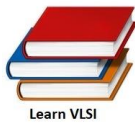
Verilog HDL is good to start with



- Learning one language is good enough to start the career.
- Verilog is having short learning curve than VHDL.
- Our focus should be to understand Hardware modelling fundamentals vs running for a new language.
- System Verilog is superset of Verilog.
- Learning System Verilog is incremental to Verilog learning.

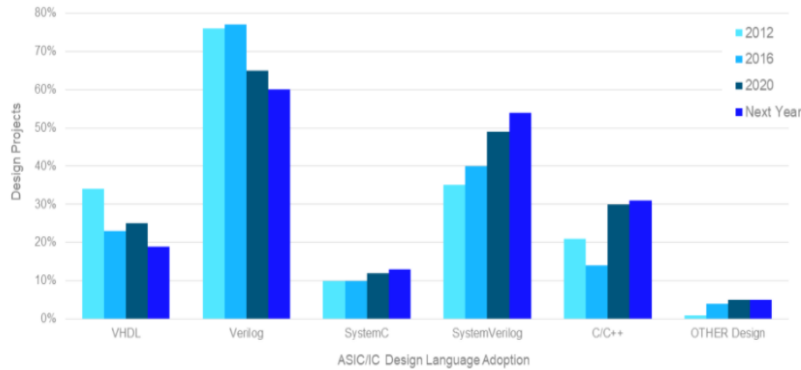


Language usage for Design/Verification and ASIC/FPGA



Design

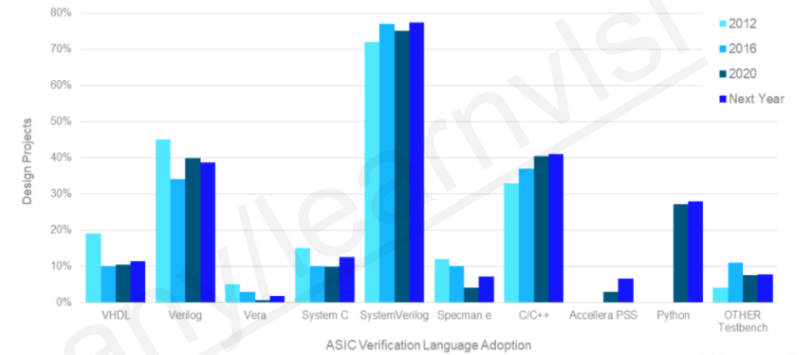
ASIC



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study
Page 1 © Siemens 2020 | 2020-10-15 | Siemens Digital Industries Software | Where today meets tomorrow.

Multiple answers possible
SIEMENS

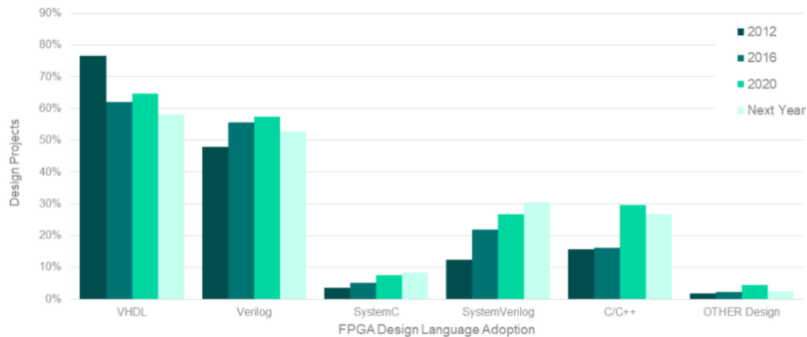
Verification



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study
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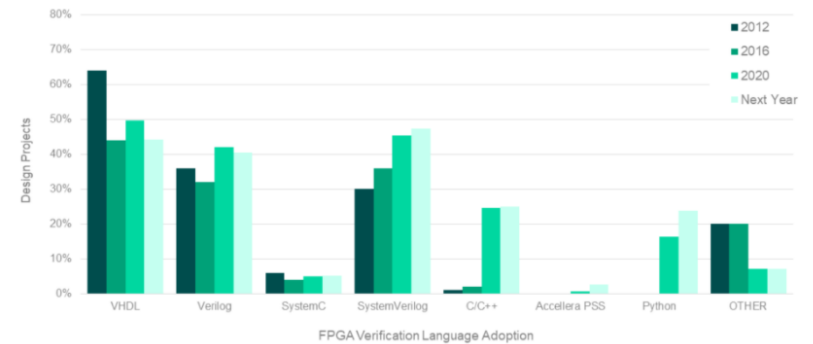
Multiple answers possible
SIEMENS

FPGA



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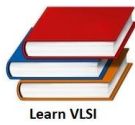
Multiple answers possible
SIEMENS



Source: Wilson Research Group and Mentor, A Siemens Business, 2020 Functional Verification Study
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Multiple answers possible
SIEMENS

Common topics across profiles 1/2

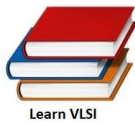


- A positive learning attitude is one of the important skill checked during interview.
- Linux knowledge
 - ⦿ Start using Linux system from Graduation time.
 - ⦿ If you are having windows based machine, use mobaxterm (No need for dual windows or virtual box)
- Good Understanding of Digital Design
 - ⦿ Digital Design by M. Morris Mano
 - ⦿ Digital Circuit Design by Salivahanan (Indian Author)
- Knowledge of Verilog
 - ⦿ Book: Verilog HDL by Samir Palnitkar
 - ⦿ Verilog Frequently Asked Question by Shivakumar

Presentations

[HDL Design using Verilog](#)
[RTL Design Guidelines](#)

Common topics across profiles 2/2



- Learn About Frequently used design blocks
 - ⊙ Sync-Async reset, Clock dividers, Level to Pulse, Pulse to Level, Clock gating, Signal stretcher, Sequence detector etc.
 - ⊙ Asynchronous FIFO concepts.

- Must be able to write directed testbenches.

- Flow Fundamentals

- ⊙ Fundamentals of Synthesis
- ⊙ Basic Static timing analysis
 - Setup hold time, Metastability, slack
 - clock Skew, clock period calculation.
- ⊙ Basic about DFT

- Good to have topics but not mandatory

- ⊙ Shell scripting
- ⊙ Python scripting
- ⊙ TCL scripting (tcltutor.exe is a free utility)
- ⊙ Makefile

Presentations

- [FSM Design](#)
- [Sync and Async Reset](#)
- [Setup and Hold time](#)
- [Static timing analysis](#)
- [FIFO](#)
- [FIFO Depth Calculation](#)
- [Asynchronous FIFO1, FIFO2](#)

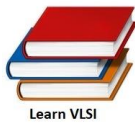
- Good understanding of Synchronous and Asynchronous FIFO
- CDC Basics.
- Basic of timing Constraints.
- Low Power RTL Design.
- Understanding of event queue in Verilog
- Flow Fundamentals
 - Fundamentals of Synthesis
 - Basic Static timing analysis
- Basic of FPGA
- Good to have but not mandatory
 - TCL Scripting
 - Learn AHB, AXI protocol
 - UPF Low power design
 - Basics of System Verilog
 - System Verilog for Verification by Chris Spear

Presentations

- [Clock Domain Crossing](#)
- [Low Power RTL Design](#)
- [VLSI Synthesis & STA](#)
- [Synthesis & GLS](#)
- [Design compiler](#)
- [Verilog Event Queue](#)
- [Delta Delay & events in Verilog](#)
- [UPF](#)
- [How to code Synthesizable RTL](#)
- [Memories](#)

Asynchronous FIFO and Clock Domain Crossing is even asked with experienced person, and ~35% interviewer time goes around these topics

Verification topics

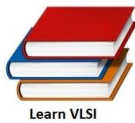


- Basics of System Verilog
 - ⊙ System Verilog for Verification by Chris Spear
- Basic of UVM
 - ⊙ Must be able to create UVM based verification environment.
- Must be able to write a random, self checking testbenches.
- Verification Coverage
- Understanding of event queue in Verilog
- Flow Fundamentals
 - ⊙ Fundamentals of Synthesis
 - ⊙ Basic Static timing analysis
- Basic of FPGA
- Good to have but not mandatory
 - ⊙ Communication between Software and Hardware using DPI and PLI
 - ⊙ TCL Scripting
 - ⊙ Learn AHB, AXI protocol

Presentations

- [Code Coverage](#)
- [Verification Testbench](#)
- [System Verilog](#)
- [UVM Basics](#)
- [Verilog Event Queue](#)
- [Delta Delay & events in Verilog](#)

Implementation/PD topics



- Understanding of CMOS, MOSFET design
- Timing constraints
- Basic of UPF based low power design
- Flow Fundamentals
 - ⊙ Fundamentals of Synthesis
 - ⊙ Basic Static timing analysis
- Physical design flow
 - ⊙ Learn fundamental of Floor planning, Power planning, Placement, CTS, Physical verification
 - ⊙ Physical design is an art, so along with theory, we must run complete flow on few basic designs.
- TCL scripts

Presentations

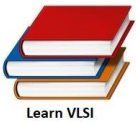
- [VLSI Physical Design](#)
- [Clock Tree Synthesis](#)
- [Physical Verification](#)
- [UPF](#)

- DFT basics
- Scan insertions
- BIST
- Stuck ATPG & Simulations.
- At-speed ATPG & Simulations.
- Memory BIST
- Flow Fundamentals
 - Fundamentals of Synthesis
 - Basic Static timing analysis
- TCL scripts

Presentations

- [VLSI Testing](#)
- [DFT](#)
- [DFT](#)
- [BIST](#)

Use of various scripting language



- Almost all EDA tools are using TCL for automation.
- Makefile is useful to manage the various steps of the project.

- Example TCL file

```
set design top
```

```
set_attr library "FrontEnd/synopsys/fsa0m_a_t33_generic_io_ss1p62v125c.lib  
FrontEnd/synopsys/fsa0m_a_generic_core_ss1p62v125c.lib "
```

```
source ../script/rc_setup.tcl
```

```
set_attribute lef_library "BackEnd/lef/header6_V55.lef BackEnd/lef/fsa0m_a_generic_core.lef " /
```

```
set_attribute hdl_search_path {../rtl/eigen ../rtl/svc ../rtl} /
```

```
read_hdl -v2001 {node.v ph_update.v topology.v serial_divide_uu.v serial_node.v serial_ph_update.v  
core.v top.v}
```

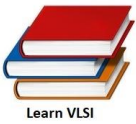
```
read_hdl -vhdl {<file_list>}
```

```
elaborate top
```

```
uniquify top
```

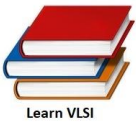
```
read_sdc ../constraints/synthesis_constraints.sdc
```

Project Ideas



- Semiconductor is driven by following applications
 - AI: Number of design with Inference engine are higher than trainings applications.
 - 5G: ORAN (Open RAN) is providing opportunities for new players. Lot of FPGA based companies are coming up.
 - Automotive: Electronics is differentiators. Automotive Ethernet, Time sensitive networking playing a big role.
 - IOT: New applications involving Hardware along with Software Apps.
- Hardware designs are moving towards high configurability with elastic functionality.
 - RISC V is perfect match.
- Opensource tool provides a good baseline and lot of improvement potential, good to use for academic projects.
- Try to solve a practical problem in the project.

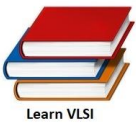
Reading Styles



- It has been observed that students are keep on changing study materials, books etc. This is not a good approach.
- Take one book and read that thoroughly.
 - ⦿ If you are not able to understand any specific topic, you can explore on internet and come back.

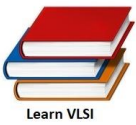
[linkedin.com/company/learnvlsi](https://www.linkedin.com/company/learnvlsi)

Networking and focus is Key



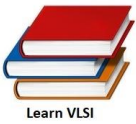
- Finding the right job is like selling a product to your target customers.
- Networking play a big role.
- Do not distribute the focus, like running for every job.
- During the job search create balance of improving learning and finding out interview opportunity.
- Learning is life long activity, After each interview, document all interview questions and identify your area of improvement and work on that.
- Cracking Interview is an art, and you need to learn the skills of bringing the interviewer into your area of expertise.

LinkedIn Profile and Resume preparation



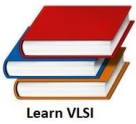
- LinkedIn is one of the main job search engine.
- Put up complete information into LinkedIn and Resume, It should have
 - ⊙ Concise and to the point information.
 - ⊙ Most of time, hiring person will do resume shortlisting based upon first page itself.
 - ⊙ First page of the resume must give a complete profile overview.
 - Next page(s) is only for details and mainly useful during the interview.
 - ⊙ Project information is important, must give a good overview, at least 2-4 lines for each project.
- Build LinkedIn profile over time and mention profile link in resume.
 - ⊙ LinkedIn profile can also be useful to find out common connections.

LinkedIn Profile Preparation



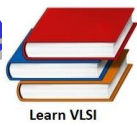
- LinkedIn is a professional Platform, and not a social media, So use this carefully.
- You can do some relevant courses available on LinkedIn.
- Just commenting on other posts for just engagement does not look good.
- You can share your professional milestones, get engaged into professional discussion etc.

Resume Preparation



- Use an email id name which is easy to type (short, and look professional)
- In the LinkedIn profile, You may update the profile link to a meaningful name.
- Always forward your resume in pdf format
 - Doc formatting does not remain same across version.
- Resume naming
 - Resume naming must include your name, e.g.
<FirstName>_<LastName>_<expifAny>_resume.pdf
 - Do not send resume like
 - <> - Copy.pdf
 - <> (<number>).pdf

An Example of LinkedIn Profile with incomplete information



- I have the following observations
 - LinkedIn profile is incomplete. It is having only information about BTech college. A resume is attached, but putting the information in the LinkedIn profile will be good. Please consider adding the following information to LinkedIn
 - Project details
 - Highschool/Intermediate details
 - Training details
 - Resume is missing following information
 - a) Passout years for Btech, 12th, 10th
 - b) Passing percentage
 - c) Project details: One line information only for project, that does not reflect details.
 - d) Added resume as two separate pdf documents and not a single document with two pages.

Hiring HR/companies get a lot of resumes, and a resume is the first interface to reflect candidate strengths. Hiring people are short of time, and each resume hardly gets a few seconds.

So please work on profiles, and reflect that in the resume. LinkedIn is a good platform to get jobs.

About

I have completed my b.tech in ECE in 2021.
Now i am searching job as a Test Engineer
About my skills C, Python, Manual Testing, SDLC, Unit Testing, Application Testing, Black Box testing, SQL

Featured

Image

resume1

Image

resume2

Activity

877 followers

... commented on a post • 4d

Ready to join

1,877

2,185 co

... commented on a post • 5d

Ready to join

130

126 co

Show all activity →

Education



Dr. A.P.J. Abdul Kalam Technical University
Bachelor of Technology - BTech. Electronics And Communication Engineering
2018 - 2021

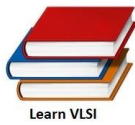
Skills

Pycharm

Positive Psychology

Functional Testing

An effective way of using reference



- Just sending resume to your known contacts is not effective.
- To make reference more effective, the resume must be forwarded wrt to an Job ID, this leads high chances of conversion into interview calls.
 - ⦿ Search open position first and send resume wrt to an open position.
- Reference are helpful, but only relying on references is not good. This limits your reach.
- Make your own way, make connections. Search for open position in the company
 - ⦿ Use company careers pages (Yes, this is effective 😊, I got my last job from this).
 - ⦿ Use LinkedIn (Connect to companies HR).
 - ⦿ Connect with genuine hiring agencies.

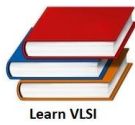
Open Source tools



Goal	Title	Webpage
Web based IDE for simulation	EDA Playground	https://www.edaplayground.com
Simulation	Icarus Verilog	http://iverilog.icarus.com
Simulation	Verilator	https://www.veripool.org/wiki/verilator
RTL to GDSII	Qflow	http://opencircuitdesign.com/qflow/index.html
RTL to GDSII	Open lane	https://github.com/efabless/openlane
RTL to GDSII	Alliance	http://coriolis.lip6.fr/
RTL Synthesis	Yosys	https://github.com/YosysHQ/yosys
STA	OpenTimer	https://github.com/OpenTimer/OpenTimer
STA	OpenSTA	https://github.com/The-OpenROAD-Project/OpenSTA
Layout editor, extraction, & DRC tool	Magic	https://github.com/RTimothyEdwards/magic
LVS	netgen	http://opencircuitdesign.com/netgen/index.html
Detailed Routing	Qrouter	http://opencircuitdesign.com/qrouter/index.html
Placement	Graywolf	https://github.com/rubund/graywolf
PCB Design	easy day	https://easyseda.com/
Circuit drawing and schematic capture tool.	XCircuit	http://opencircuitdesign.com/xcircuit/index.html
DesignSpark	PCB Design	https://www.rs-online.com/designspark/
Fritzing	PCB Design	https://fritzing.org/

Reference: Book “The VLSI Handbook: Design Principles, Industry and Career Perspectives”, Udit Kumar, Aditya Gupta, Sumit Soman

Useful Websites



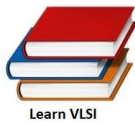
- Learn VLSI LinkedIn page
<https://www.linkedin.com/company/learnvlsi>

- Useful Websites

Topic	Webpage
Design and Verification	http://www.sunburst-design.com/
Verification	http://www.testbench.in/
Verification	http://www.asic-world.com/
Verification	https://verificationguide.com/
Design and Verification	http://www.vlsi-expert.com/
VLSI SoC Design	http://vlsi-soc.blogspot.com/
Design and Verification	http://www.sunburst-design.com/
VLSI ASIC	http://asic.co.in/
ASIC Design and Methodology	https://www.edaboard.com/
Verification Academy By Mentor	https://verificationacademy.com/

Reference: Book “The VLSI Handbook: Design Principles, Industry and Career Perspectives”, Udit Kumar, Aditya Gupta, Sumit Soman

Useful Books



- To get overview of VLSI Industry: “The VLSI Handbook: Design Principles, Industry & Career Perspectives” by Udit Kumar, Aditya Gupta, Sumit soman.
- Useful Books

Goal	Title	Author
Digital Design	Digital Design	M.Morris Mano
Digital Design	Digital Design	John F. Wakerly
Verilog	Verilog HDL	Samir Palnitkar
System Verilog	Verilog and System Verilog Gotchas	Stuart Southerland
VHDL	VHDL: Programming by Example	Douglas L. Perry
Verification	System Verilog for Verification	Chris Spear
Verification	Writing Testbenches Using System Verilog	Janick Bergeron
Synthesis	Advanced Chip Synthesis	Himanshu Bhatnagar
Timing	Sta for nanometer design	Bhaskar
CMOS	CMOS VLSI Design	Neil Weste and David Harris
Analog Design	Design of Analog CMOS Integrated Circuits 1st Edition	Behzad Razavi
Electronic circuits	Electronic circuits	Milman and Halkis
Analog Design	CMOS VLSI Design	Weste.
Electronic circuits	Linear integrated circuits	Roy Choudhry
Analog Design	Microelectronic Circuits	Kenneth C. Smith Adel S. Sedra
Circuit theory	Electronic devices & circuit theory	Boylestad
Verilog FAQ	Verilog Frequently Asked Questions	Shivakumar & N. Balachander
Verification FAQ	Cracking Digital VLSI Verification Interview: Interview Success	Ramdas M & Robin Garg

Conclusion

- A dedicated effort of 3-6 months is good enough for job search preparation.
- In today words, It is completely possible to prepare yourself, without any need of training institutes.
- VLSI field has huge potential and offer lucrative career.



Thank You

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“The VLSI Handbook: Design Principles, Industry & Career Perspectives” available on [Amazon!](#)



Book Contents

Introduction & market

Semiconductor Ecosystem

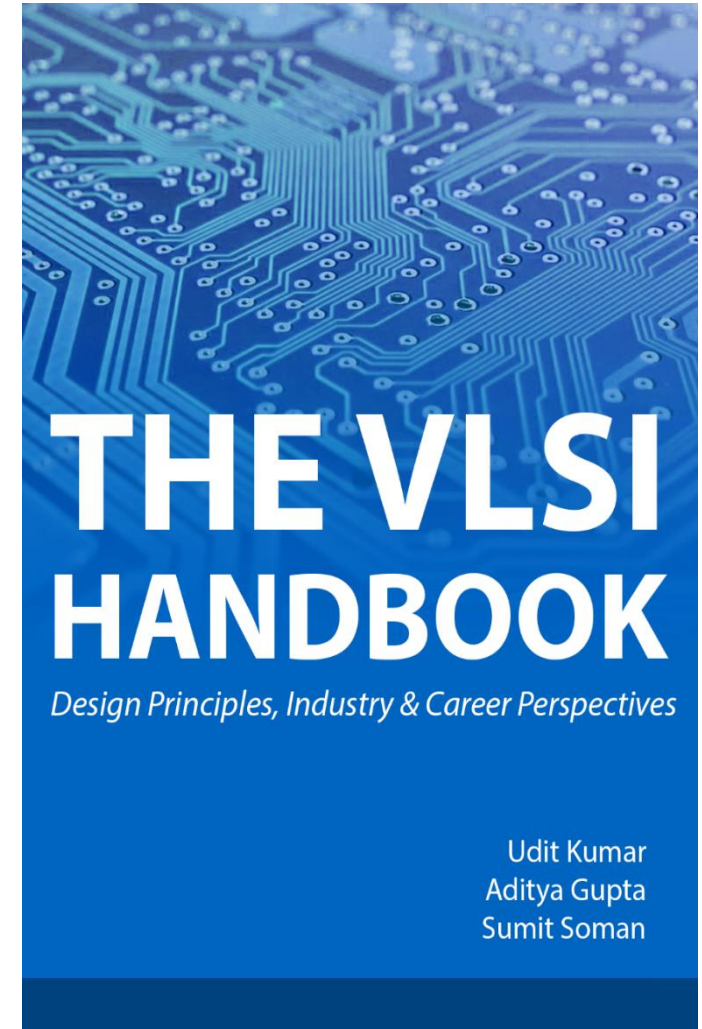
SoC Development

IP Design

FPGA aided Development

Emerging Semiconductor Applications: AI, 5G, Automotive

VLSI Resources, FAQ

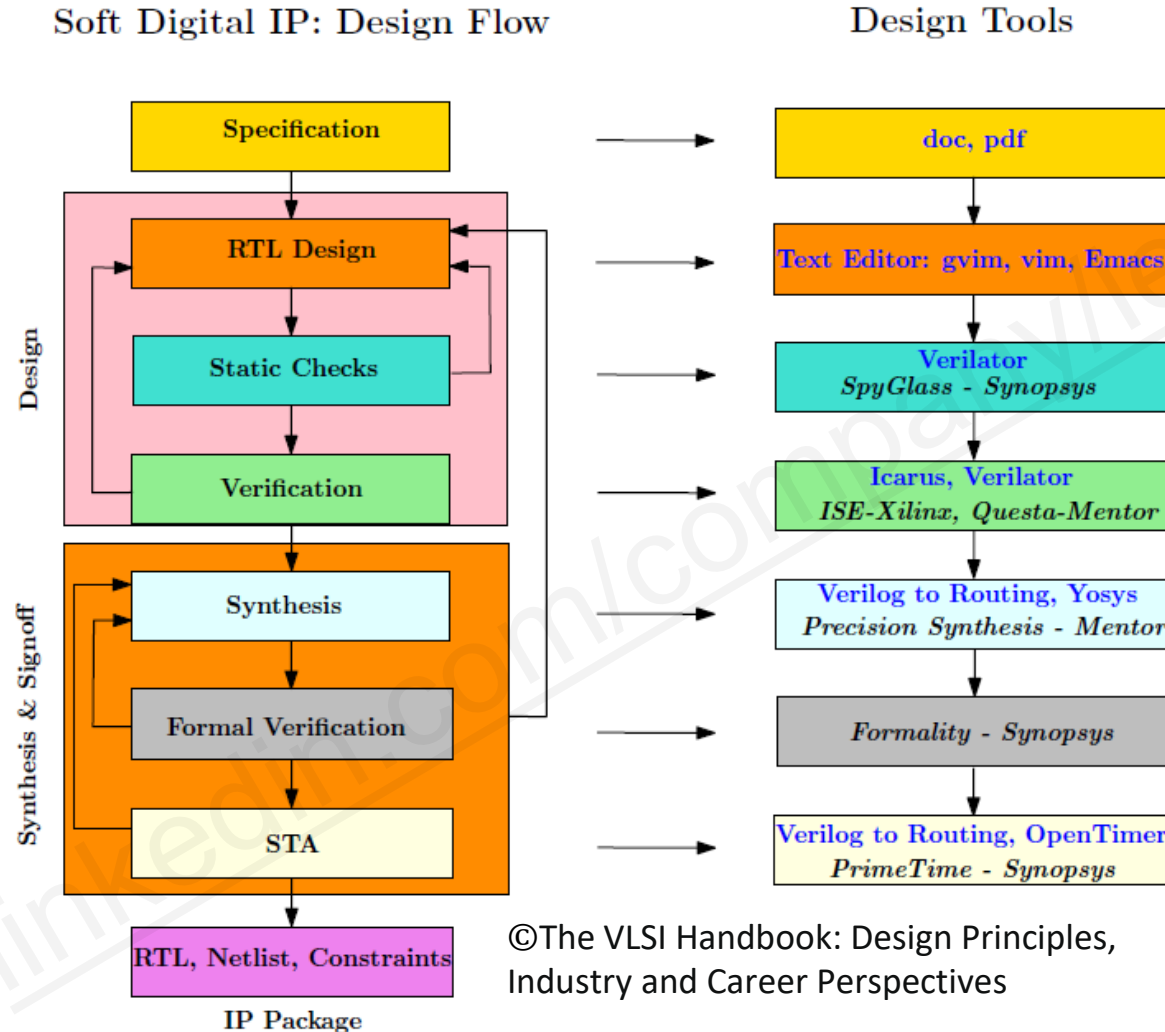
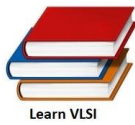


The Authors have accumulated experience of 30+ years.

Book has been reviewed and recommended by Industry experts:

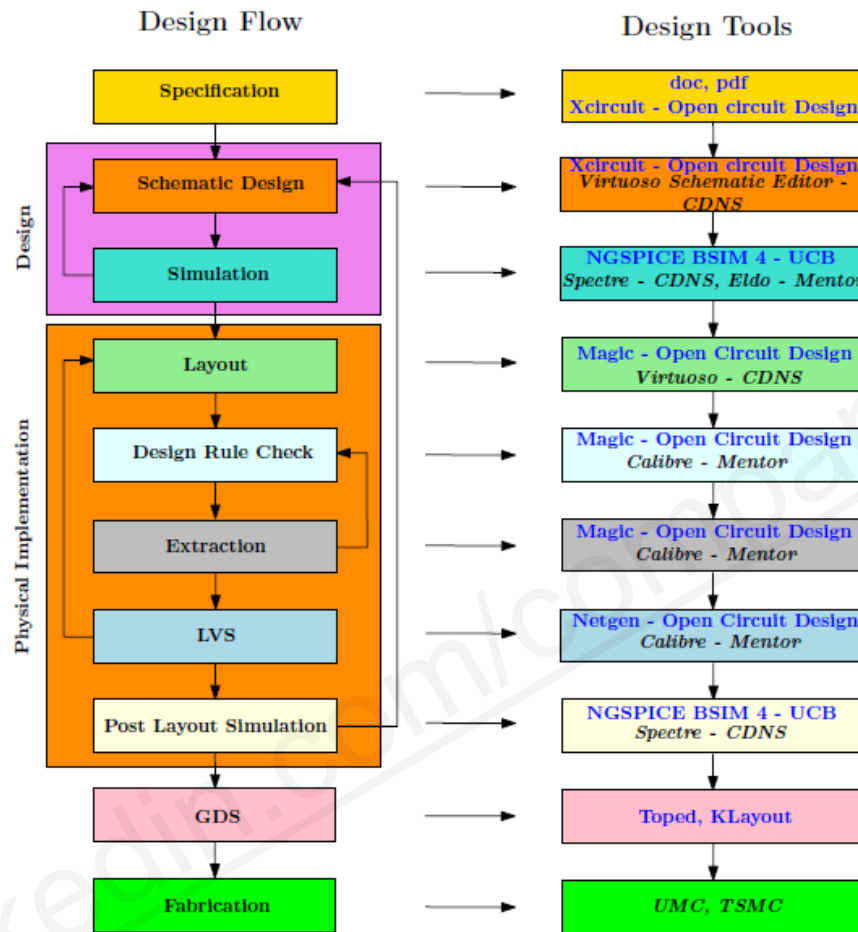
Intel, Qualcomm, NXP, Xilinx, Siemens EDA, Synopsys etc.

Soft Digital IP Design Flow



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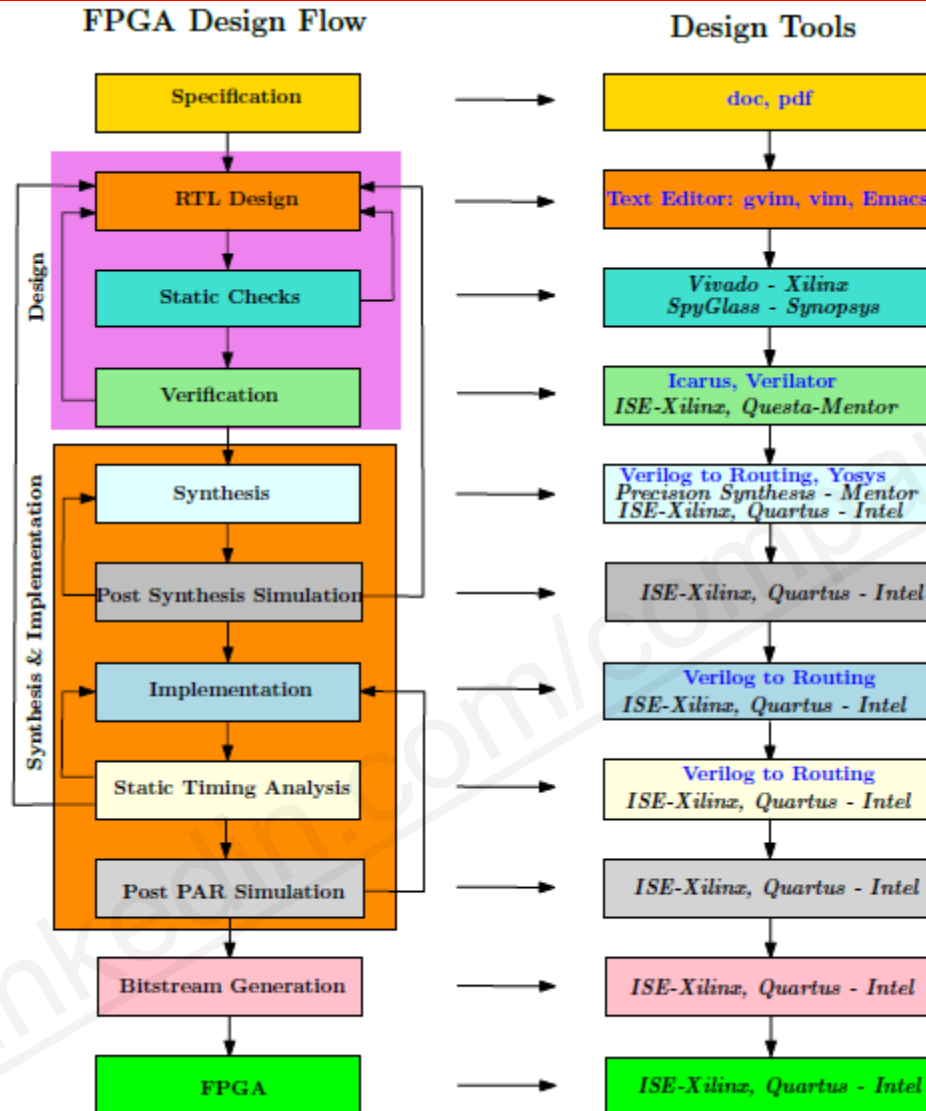
Analog IP Design Flow



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FPGA Design Flow



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