ECE5025	SYSTEM ON CHIP DESIGN	L	T	P	J	C
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Pre-requisite	**Nil**				**v 1.0**	

Course Objective:

The course is aimed to

1. Introducing design, optimization, and programing a modern System-on-a-Chip.
2. Detailing SoC design with on-chip memories and communication networks, I/O interfacing.
3. Making them understand about signal integrity aware SoC design and Scheduling algorithms.

Expected Course Outcome:

At the end of the course the student will be able to

1. Demonstrate an ability to identify, formulate and treat complex issues in the field of system-on-chip from a holistic perspective.
2. Improve the performance of SoC based design by various advanced techniques.
3. Apply SystemC for system design.
4. Use interconnection structures in a SoC / NoC based system design.
5. Apply static timing analysis for a SoC based design.
6. Analyse the cause and eliminate the issues relevant to signal integrity and scheduling.

Student Learning Outcomes (SLO): 1,5

Module:1	**Introduction**	**3 hours**

Architecture of the present-day SoC - Design issues of SoC- Hardware-Software Co design – Core Libraries – EDA Tools.

Module:2	**Design Methodology for Logic, Memory and Analog Cores**	**6 hours**

SoC Design Flow – guidelines for design reuse – Introduction- Efficiency of application specific hardware- Target architectures for HW/SW partitioning -System Integration, Embedded memories – design methodology for embedded memories – Specification of analog cores.

Module:3	**Introduction to System C for SoC Design**	**7 hours**

Co-Specification- System Partitioning- Co-simulation, Co-synthesis & Co-verification –SystemC and Co-specification and Co-simulation.

Module:4	**SoC and NoC Interconnection Structures**	**7hours**

SoC Interconnection Structures- Bus-based Structures- AMBA Bus.Network on Chip -NoC Interconnection Structures-Topologies- routing- flow control- network components(router/switch, network interface, Links).

Module:5	**STA for SoC Design**	**7 hours**

Timing paths and its Timing Optimization- Slow to High and High to low frequency timing path- Half cycle timing path- Latch time borrowing- Interface Logic Model design and analysis for SoC design.

Module:6	**Signal Integrity Aware SoC design**	**7 hours**
Signal Integrity overview- EMI (Electro Magnetic Interference) and its protection- ESD and its Protection- Delay- Noise- glitches and its protection- Transmission lines- ringing. Crosstalk and Glitch analysis-Types of Glitches- Glitch Threshold and propagation- Noise Accumulation with Multiple aggressor- Aggressor timing correlation- Crosstalk Delay analysis -Timing Verification using crosstalk delay-Positive and Negative crosstalk- aggressor victim timing correlation- aggressor victim functional correlation.		
Module:7	**Scheduling**	**6 hours**
Introduction and need for HLS- Major steps-Scheduling and Allocation- Binding/Assignment- Concept of Scheduling, Heuristic Scheduling Algorithm.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Michael J. Flynn, Wayne Luk,Computer System Design: System on chip,Wiley-Blackwell, First Edition, 2011.
2.	J. Bhasker, RakeshChadha,STA for Nanometer design – A practical approach, Springer, First Edition, 2010.
Reference Books	
1.	Jose L. Ayala,Communication Architectures for Systems-on-Chip, CRC Press, First Edition, 2011.
2.	Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, System-on-Chip Test Architectures: Nanometer Design for Testability, Morgan Kaufmann, First Edition, 2010.
3.	Ahmed Jerraya and Wayne Wolf, Multiprocessor Systems-on-Chips (Systems on Silicon Series), Morgan Kaufmann, First Edition, 2010.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016