Simple DRAM Model Design and Its Verification Env. (Host Behaviour to be designed)

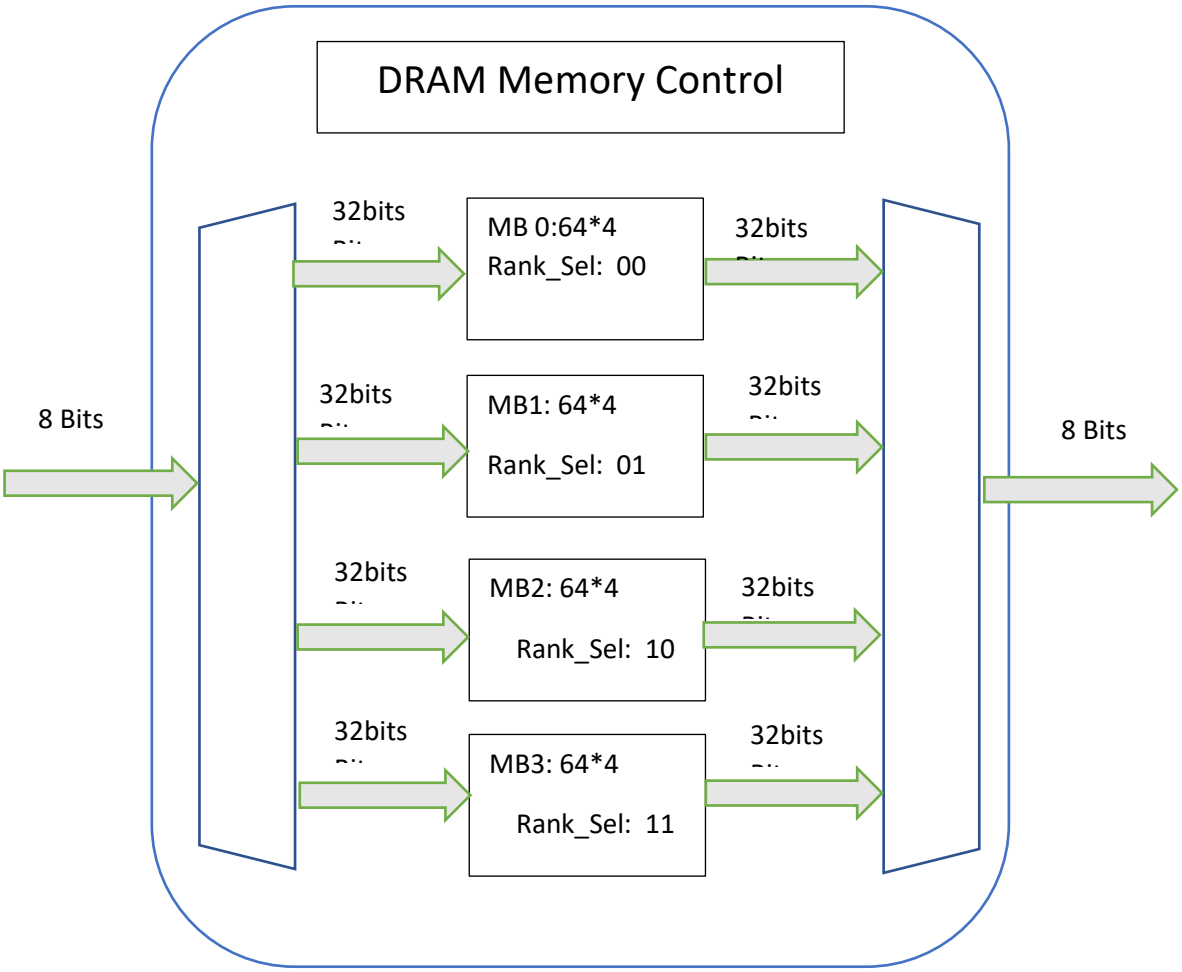
```
Interface Signal List DUT
=========================
reset_n:          Input, Width 1bit, Active low Reset
clock:            Input, Width 1bit,
data_in:          Input, Width 8bits
col_address:      Input, Width 8bits: Max. 64 address {c1,c0] = 2'b00
row_address:     Input, Width 2bits: Max. 4 row address
bank_sel:         Input, Width 2bits: Max. 4 banks
act_cmd:          Input, Width 1bit
pre_cmd:          Input, Width 1bit
wr_cmd:           Input, Width 1bit
rd_cmd:           Input, Width 1bit
ref_cmd:          Input, Width 1bit
data_mask:       Input, Width 1bit
dqs:              In-Out, Width 1bit


data_out:        Output, Width 8bits
```

Ref Model Design:

Basic Functional Block for Data Path

Note: Internal functionality may differ. Total 16 Block of Memory of size 256 bytes (Burst address range 64) is used.



Minimum Delay for cmd to cmd and cmd to data

- Act command with bank_sel and row address to Read command with Col address, Bank_Sel: 2 cycles.
- Read command with Col address and Bank_Sel to Read data out: (4 Cycles → 8 Cycles)
- Act command with bank_sel and row address to Write with Col Address: 2 cycles
- Write Command with address to Write data out: (4 Cycles → 8 Cycles)
- Read command with Address to Read First Data: (4 Cycles) Last data (8^{th} Cycles)
- Act to Act Command Different Bank -> 2cycles
- Pre to Ref command → 16 Cycles
- Ref to Act Command → 64 Cycles
- Pre to Act Command → 16 Cycles
- Wr command OR Rd command to Pre-charge Command → 10 Cycles
- Wr command to Next Write / Read command → 10 Cycle
- Rd command to Next Write / Read command → 10 Cycle
- One Ref to next Reference maximum delay is 2048 Cycles

Invalid Command sequence

- Act to Pre. Command
- Act to Act Same bank
- Act to Ref. Command
- Read to Ref. Command
- Write to Ref. Command
- Any command to command < Minimum Delay

Valid Command sequences: Few selected are define below

Important Note: that Min Delay define above must be followed

- Simple Write: Act -> Wr -> Pre-> Ref
- Simple Read: Act-> Rd-> Pre-> Ref
- Simple Wr followed by Read: Act-> Wr -> Rd-> Pre-> Ref
- Simple Ref followd by Wr/RD: Pre->Ref->Act->Wr->Rd->Pre->Ref
- Activate all 4 banks : perform Wr to 4 bank Read to 4 bank : Act_B0-> Act_B1->Act_B2->Act_B3->Wr_B0->Wr_B1->Wr_B2->Wr_B3-> Rd_B0->Rd_B1->Rd_B2->Rd_B3-> PRE-> Ref
- Write Burst 64 times (All Col_Addr Change) Read burst 64 Times: Pre->Ref->Act->Wr->Wr->Wr->Wr…. 64 times -> Rd->Rd->….64times->Pre->Ref
- Pre->Ref -> Delay of 2047 Cycle -> REF (Must work)

Few Selected TEST Conditions as Ref. You can create XLS or Doc for test plan

- Test 1: Write One burst of data and read back, must get same data from same address
  - **Patten:** 0x00, 0xff, 0xaa, 0x55
  - **Sequence:** Act BK0 -> Write Command-> Write Data -> Read Command -> Read Data-> pre-All -> Ref All
  - **What to Verify:** Data integrity in score board for Write and Read , Timings etc.
  - Status: PASS/Fail
- Test 2: Activate 4 bank and Write and Read multiple burst
  - **Pattern:** 0xd5,0xaa,0x55,0x5d , Data can be incremental, or Other pattern also.
  - **Sequence:** Act Bk0->Act BK1-> Act Bk2-> Act BK3-> Write multiple burst (64) and Read Multiple Burst (64). Total Data 256 (64 * Burst of 4) → Pre All-> Ref All
  - **What to Verify:** Data integrity in score board for Write and Read , Timings etc.
    Status: PASS/Fail