ECE6026	MIXED SIGNAL IC DESIGN	L	T	P	J	C
		2	0	0	4	3
Pre-requisite	**ECE5016-Analog IC Design**				**v 1.0**	

Course Objective:

The course is aimed to

1. introduce the design aspects of dynamic analog circuits and analog-digital interface electronics in CMOS technology.
2. Specify design implement ADC & DAC.

Expected Course Outcome:

At the end of the course the student will be able to

1. Understand the theory of discrete-time signal processing and its implementation using analog techniques.
2. Realizing Sample and Hold Circuits using MOS by considering the non-idealities.
3. Analyse CMOS based Switched Capacitor Circuits.
4. Understanding basics of Data Converters.
5. Analyse the architectures of ADCs and DAC.
6. Understand the oversampling converter architecture.
7. Gain mixed-signal design experience using Cadence EDA tools.

Student Learning Outcomes (SLO):	**1,5,17**

Module:1	**Sampling**	**3hours**

Introduction – sampling - Spectral properties of sampled signals - Oversampling – Anti-alias filter design. Time Interleaved Sampling - Ping-pong Sampling System - Analysis of offset and gain errors in Time Interleaved Sample and Hold.

Module:2	**Sampling Circuits:**	**3 hours**

Sampling circuits- Distortion due to switch - Charge injection - Thermal noise in sample and holds - Bottom plate sampling - Gate bootstrapped switch -Nakagome charge pump. Characterizing Sample and hold - Choice of input frequency.

Module:3	**Switched Capacitor Circuits:**	**4hours**

Switched Capacitor (SC) circuits– Parasitic Insensitive Switched Capacitor amplifiers - Non idealities in SC Amplifiers – Finite gain - DC offset - Gain Bandwidth Product. Fully differential SC circuits - DC negative feedback in SC circuits.

Module:4	**A/D and D/A Converters Fundamentals:**	**2hours**

Data converter fundamentals: Offset and gain Error - Linearity errors - Dynamic Characteristics – SQNR - Quantization noise spectrum.

Module:5	**Analog to Digital Converter Architectures:**	**4 hours**

Flash ADC - Regenerative latch - Preamp offset correction - Preamp Design - necessity of up-front sample and hold for good dynamic performance. Folding ADC - Multiple-Bit Pipeline ADCs and SAR ADC.

Module:6	**Digital to Analog Converter Architectures:**	**5hours**	
DAC spectra and pulse shapes - NRZ vs RZ DACs. DAC Architectures: Binary weighted - Thermometer DAC - Current steering DAC - Current cell design in current steering DAC - ChargeScaling DAC - Pipeline DAC.			
Module:7	**Oversampling Converter:**	**7hours**	
Benefits of Oversampling -Oversampling with Noise Shaping - Signal and Noise Transfer Functions - First and Second Order Delta-Sigma Converters. Introduction to Continuous-time Delta Sigma Modulators - time-scaling - inherent antialiasing property - Excess Loop Delay - Influence of Op-amp nonidealities - Effect of Op-amp nonidealities - finite gain bandwidth - Effect of ADC and DAC nonidealities - Effect of Clock jitter.			
Module:8	**Contemporary issues:**	**2hours**	
	Total Lecture hours:	**30hours**	

Text Book(s)	
1.	Frank Ohnhauser, Analog-Digital Converters for Industrial Applications Including an Introduction to Digital-Analog Converters Springer Publishers, First Edition, 2015.
2.	David Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley & Sons Inc., 2012.
Reference Books	
1.	Ahmed M.A.Ali, High Speed Data Converters IET Materials, Circuits & Devices, First Edition, 2016.
2.	S.Pavan,R. Schreier and Gabor.C.Temes, Understanding Delta – Sigma Data Converters, IEEE Press, First Edition, 2017.

Mode of Evaluation: Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

Typical Projects

1. Design of Flash ADC
2. Design of High Speed Sample and Hold Amplifier.
3. Design of Charge Pump Circuit.
4. Design of Switched Capacitor Integrator
5. Design of Current – Steering DAC

Mode of Evaluation :Review I, II & III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016