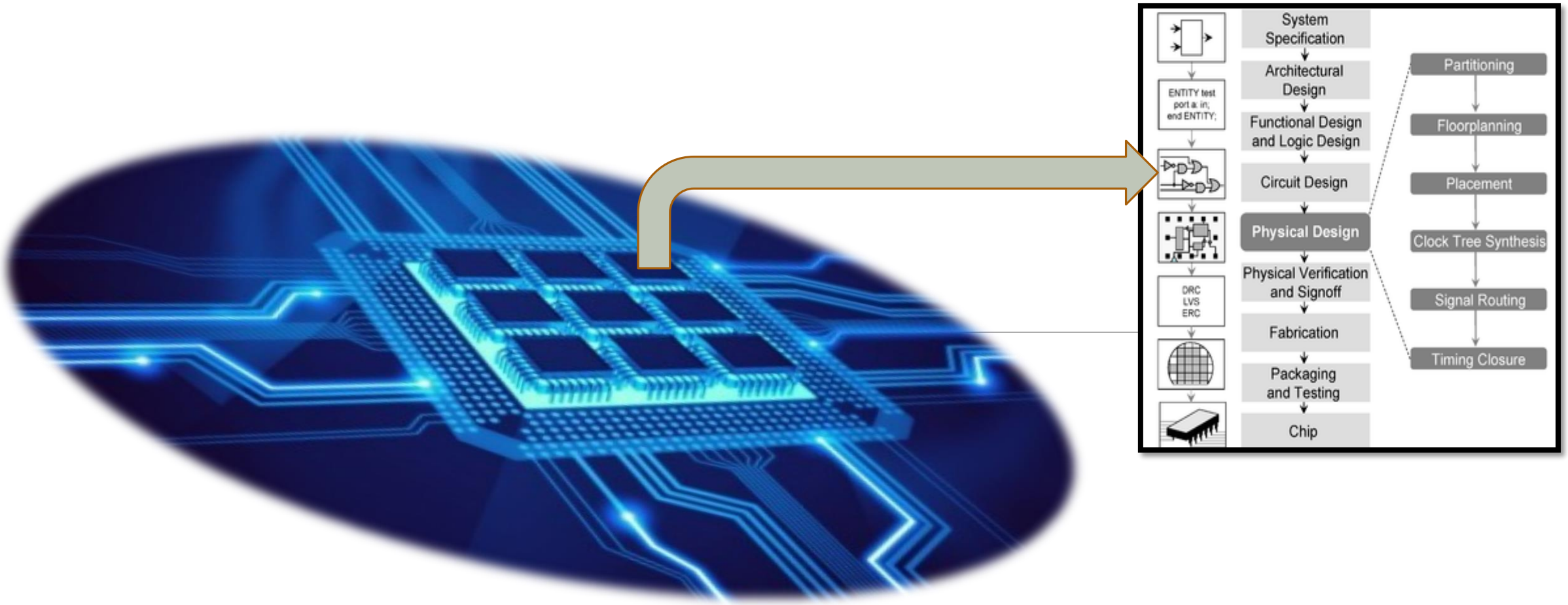
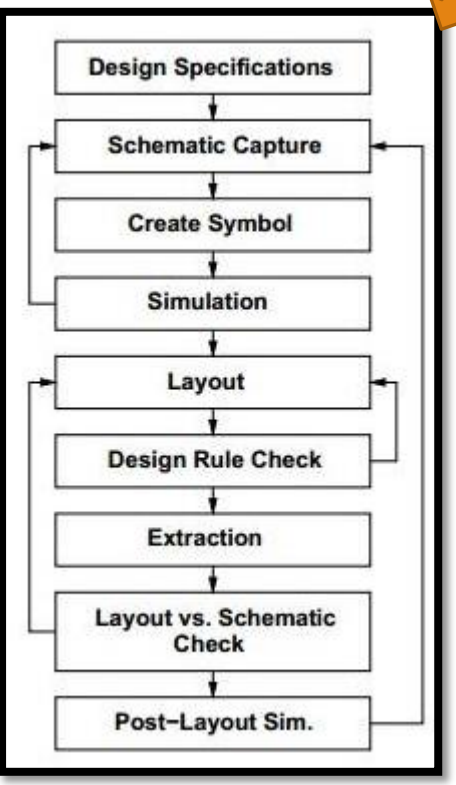
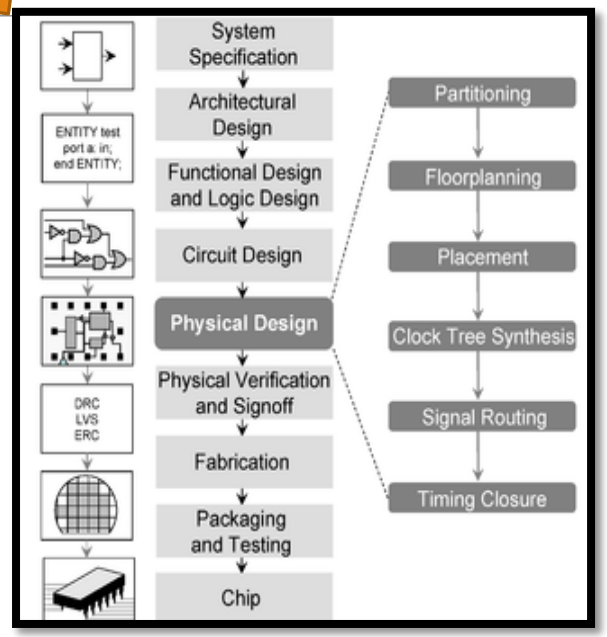
# ASIC design training



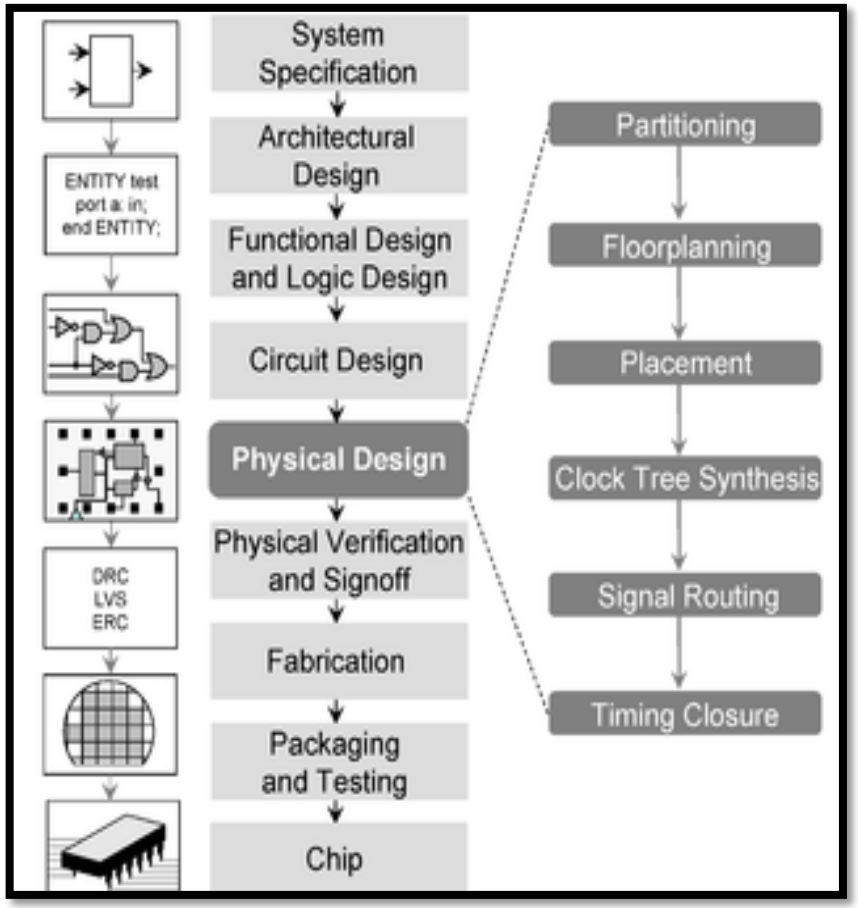
# *Flow comparison b/w Custom and semi custom design*




| FULL CUSTOM DESIGN | SEMI CUSTOM DESIGN |
|---|---|
| All mask layers are customized in full custom design | It uses pre-designed logic cell(and gates, OR gate, multiplexers) known as standard cells. |
| In full custom design, all logic cells, circuits or layouts are designed specifically. Design doesn't use pretested or pre-characterized cells. | Designer used pre-tested or pre-characterized cell. |
| This approach is considered only when there is no suitable existing | Widely used |
| Offers high performance lower cost as compared to semi. | More cost. Low performance. |
| Design time and complexity is more. | Design time and complexity is less |



# *Brief about ASIC flow*



# *Why HDL ?*

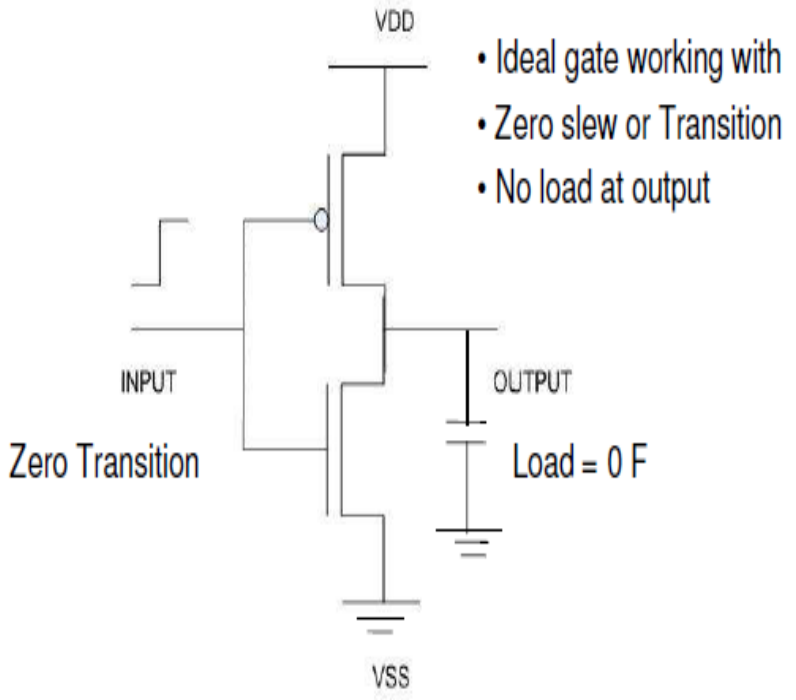
- Programming language used to describe the behavior of digital circuits

- Difference b/w HDL and Software language
  - Every piece of line represents a hardware
  - We can mimic the behavior of the hardware using HDL languages
  - Assembly language is used to access the basic machine instructions of the CPU

# *Key terminologies in VLSI design – Delay*

- Intrinsic delay (Cell delay)

- Net delay or interconnect delay or wire delay



# *Quiz*

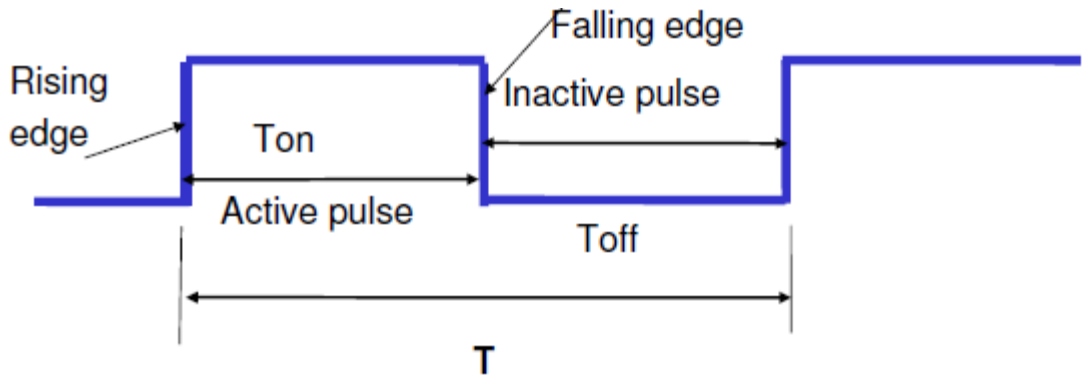
Q1 - What are the factors that impact the cell delay?

Q2 - How is the cell delay impact due to Rise/Fall transition?

Q3 - What are the factors that impact the net delay?

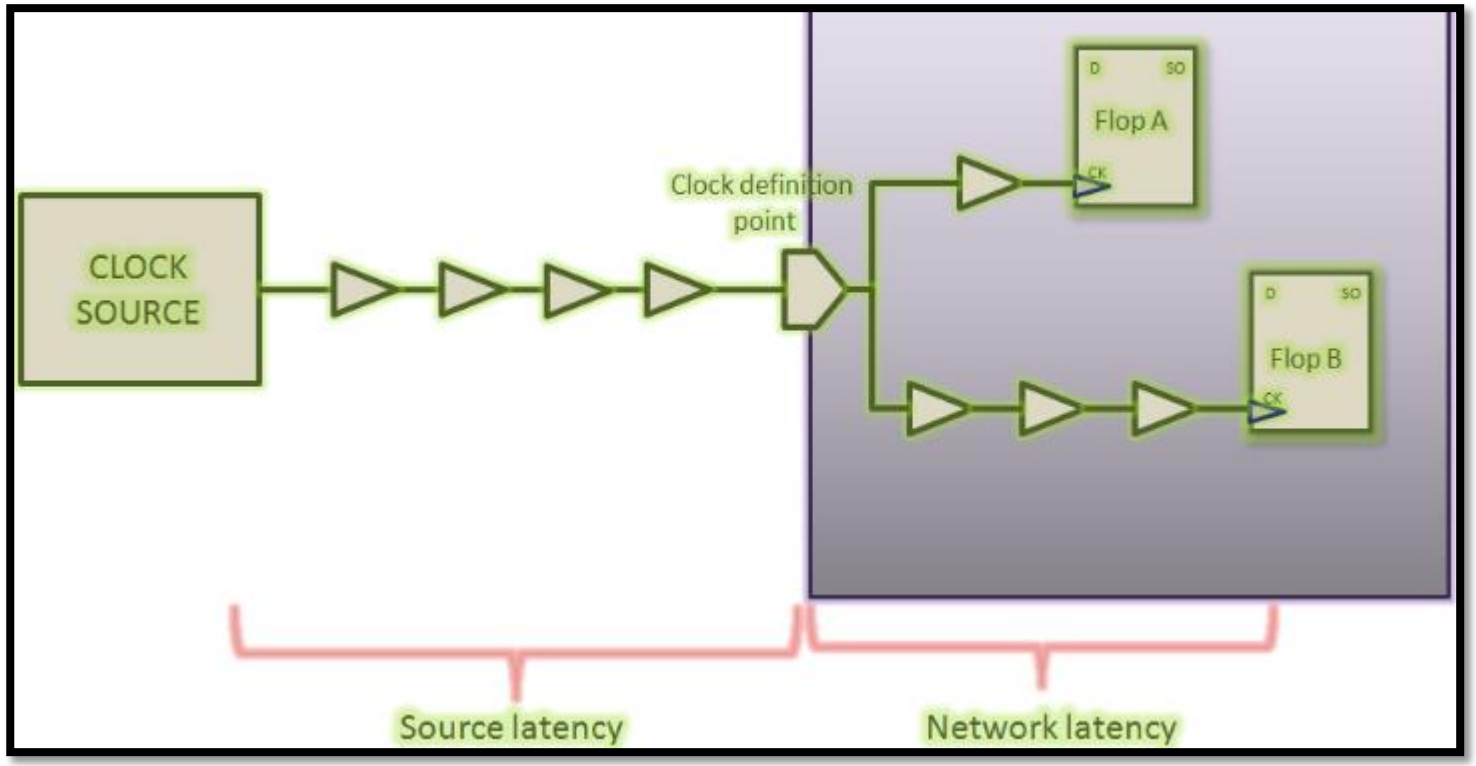
# *Key terminologies in VLSI design – clock*

- **Clock** is source of regular periodic pulses
- **Rising edge** - Transition from 0 -> 1
- **Falling edge** – Transition from 1 -> 0
- **Pulse width** – Difference in time between active and inactive state of the signal
- **Duty cycle** – Ton/ (Ton+ Toff)



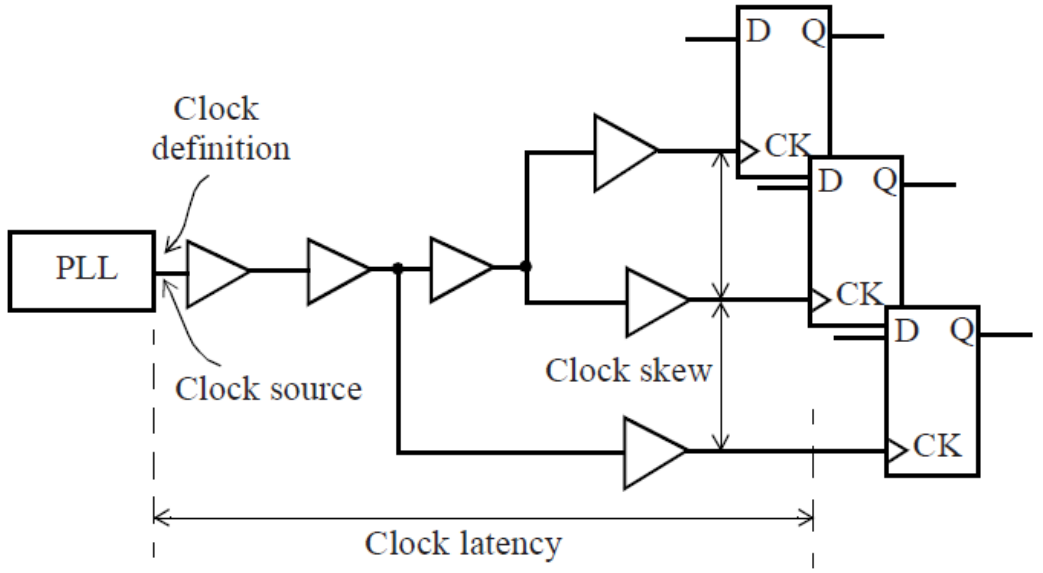
# *Key terminologies in VLSI design – Clock latency*

**Clock latency-** It's time taken for clock signal to reach from source to clock pin of register/ Macro (Sink pin of cell)

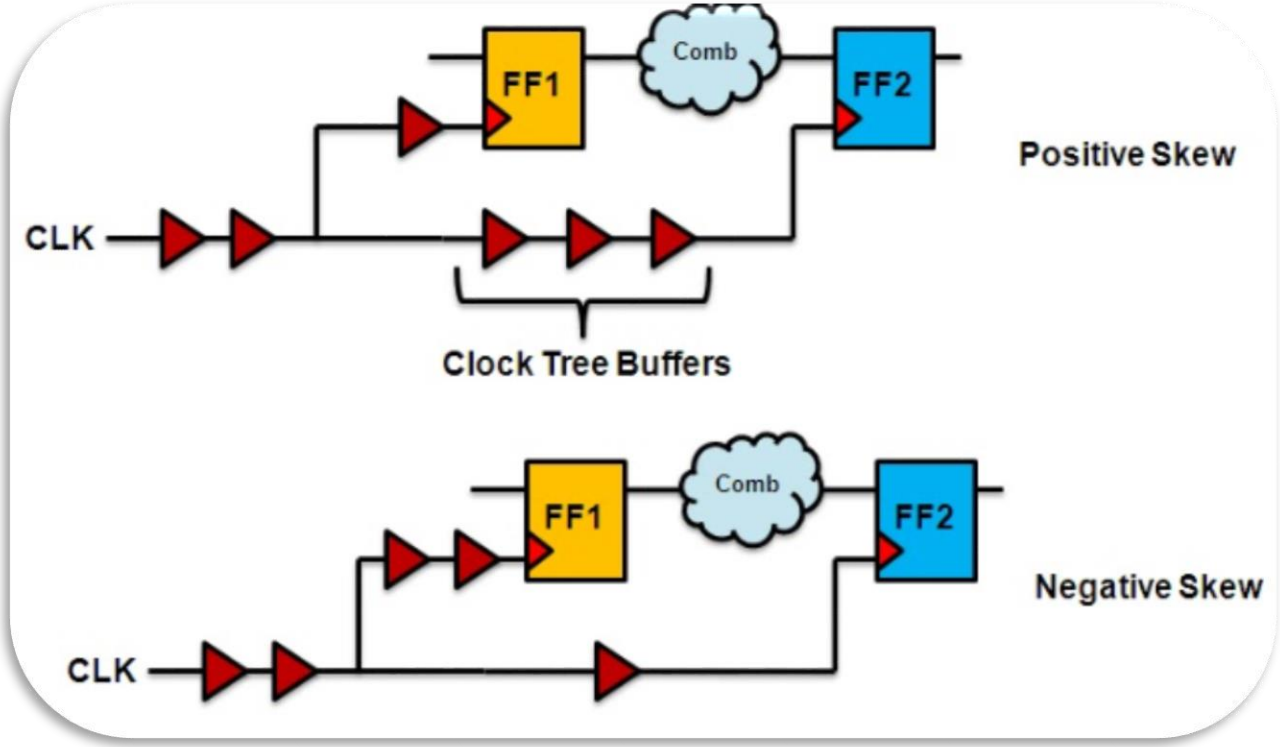


# *Key terminologies in VLSI design –clock skew*

- **Clock skew –** Relative delay difference in the clock reaching b/w the flops in the design
- There are two types of clock skew
  - Positive skew
  - Negative skew



# *Types of skew*



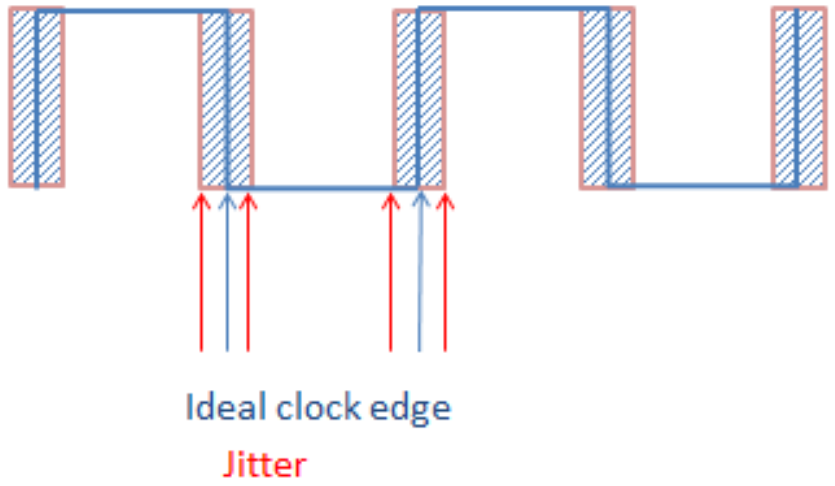

**Note:-** We will see impact of +/- Skew on Setup/Hold timing in later slides

# *Causes of clock skew*

- Difference in wire length
- Gates (buffers) on the paths
- Flip-flops working with different edge of clock/Different clock

# *Key terminologies in VLSI design – clock jitter*

- Clock jitter is the uncertainty on when the clock edges occur
- Clock jitter is caused by imperfections in the clock oscillators.



# *Introduction to libraries in ASIC design*

- Technology specific library
- Logical/Timing library
- Physical library

# *Technology specific library (Tech lef)*

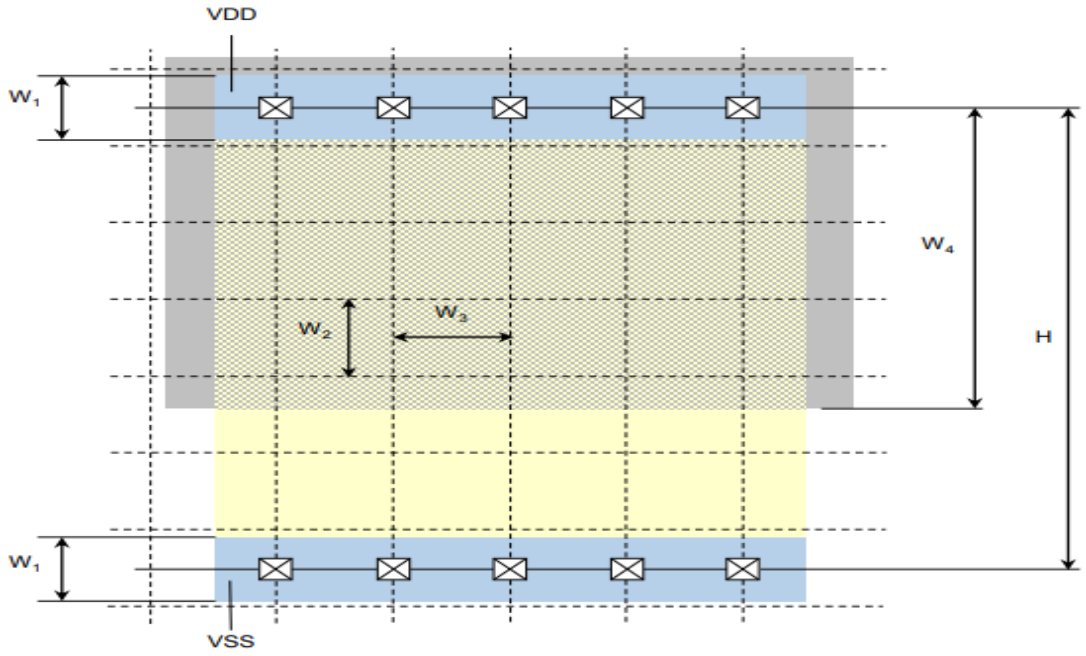
- Technology LEF Files contain (simplified) information about the technology for use by the placer and router
  - Layers and layer types
  - Sites (x and y grids of the library) – i.e., double height cells!
  - Via definitions
  - Design Rules
  - Parasitic and Antenna data.

```
LAYER MET1
  TYPE ROUTING ;
  PITCH 3.5 ;
  WIDTH 1.2 ;
  SPACING 1.4 ;
  DIRECTION HORIZONTAL ;
  RESISTANCE RPERSQ .7E-01 ;
  CAPACITANCE CPERSQDIST .46E-04 ;
END MET1

LAYER VIA
  TYPE CUT ;
END VIA
```

# *Technology lef conti..*

- Cell height is measured in Tracks
  - A Track is one M1 pitch
  - E.g., An 8-Track Cell has room for 8 horizontal M1 wires.




| Parameter | Symbol |
|---|---|
| Cell height (# tracks) | H |
| Power rail width | $W_1$ |
| Vertical grid | $W_2$ |
| Horizontal grid | $W_3$ |
| N-Well height | $W_4$ |

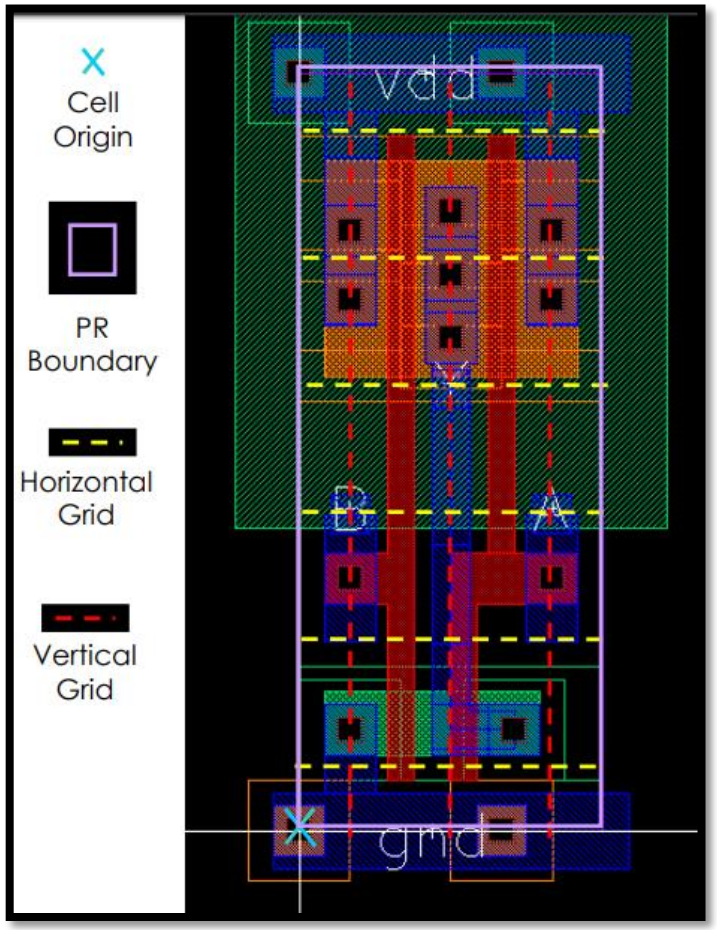
# *Technology lef conti..*

- The more tracks, the wider the transistors, the faster the cells.
  - 7-8 low-track libraries for area efficiency
  - 11-12 tall-track libraries for performance, but have high leakage
  - 9-10 standard-track libraries for a reasonable area-performance tradeoff

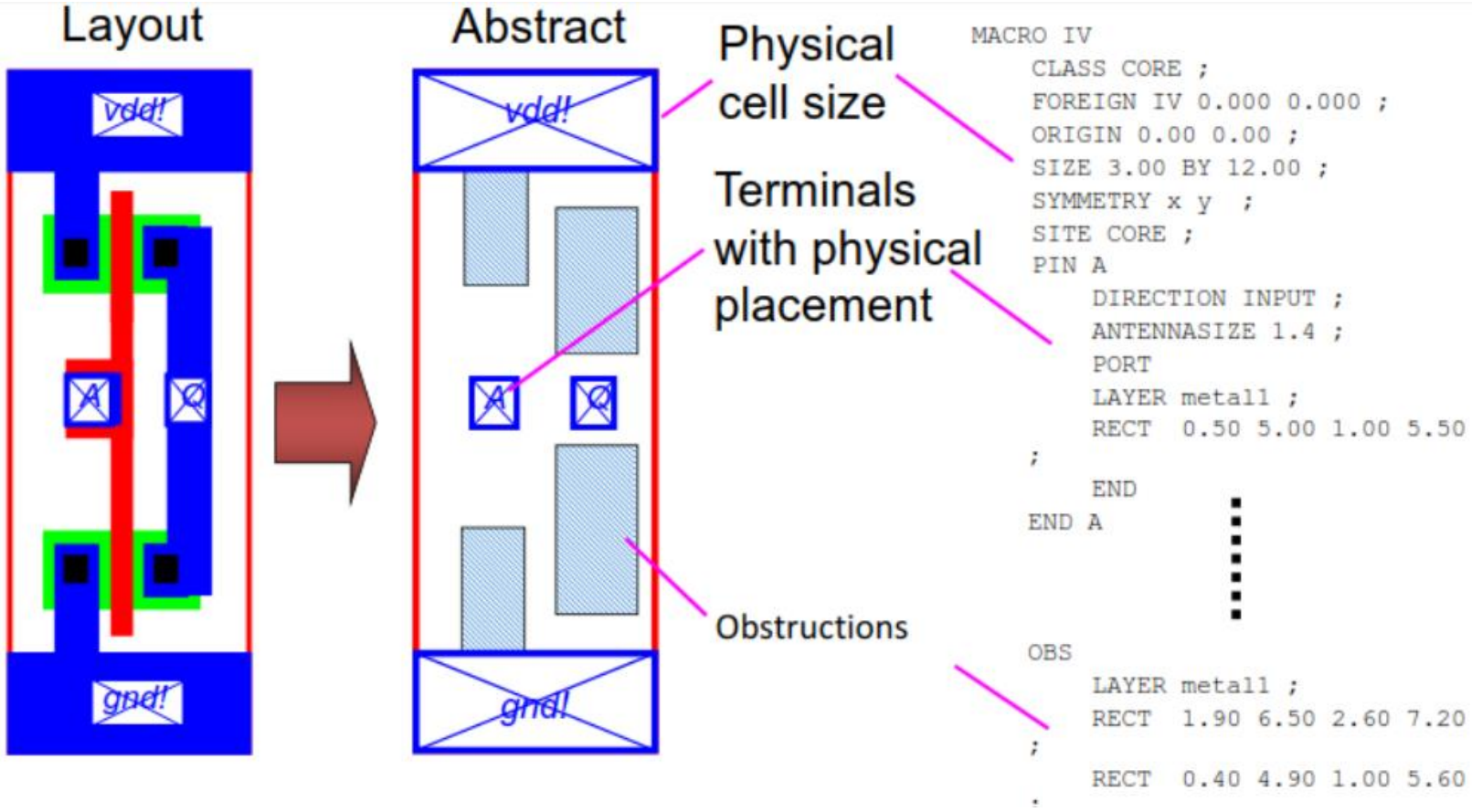
# *Technology lef conti..*

- Cells must fit into a predefined grid
  - ✓ The minimum Height X Width is called a SITE.
  - ✓ Must be a multiple of the minimum X-grid unit and row height.
  - ✓ Cells can be double-height, for example.

- Pins should coincide with routing tracks
  - ✓ This enables easy connection of higher metals to the cell.

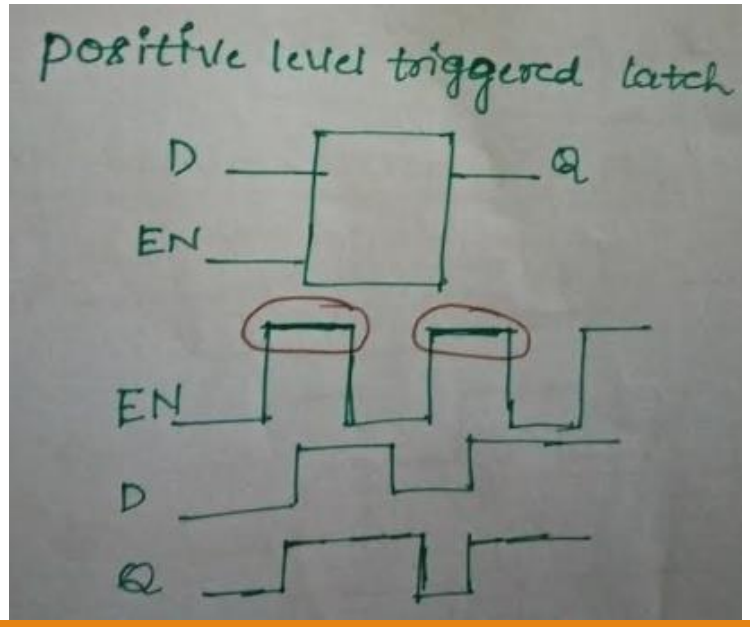


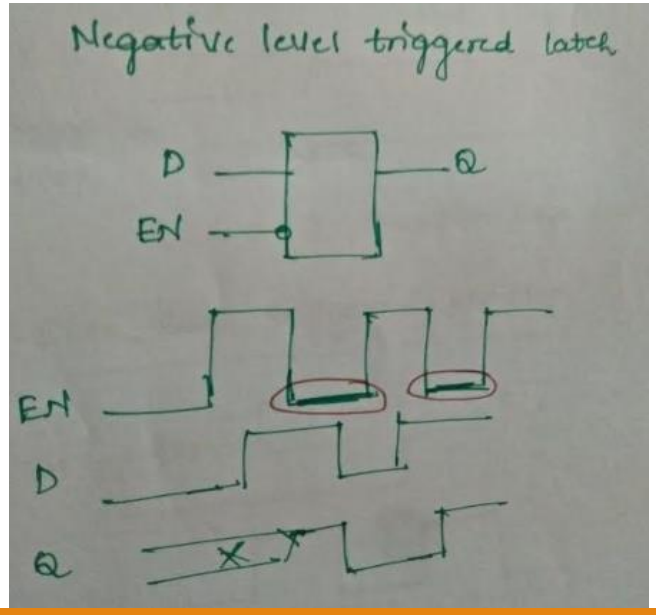
# *What is inside the .lef ?*



# Latch

- Latch is a one bit storage element and it checks input continuously & changes the output whenever there is a change in input
- Mainly latches are of two types
  - ✓ Positive level
  - ✓ Negative level



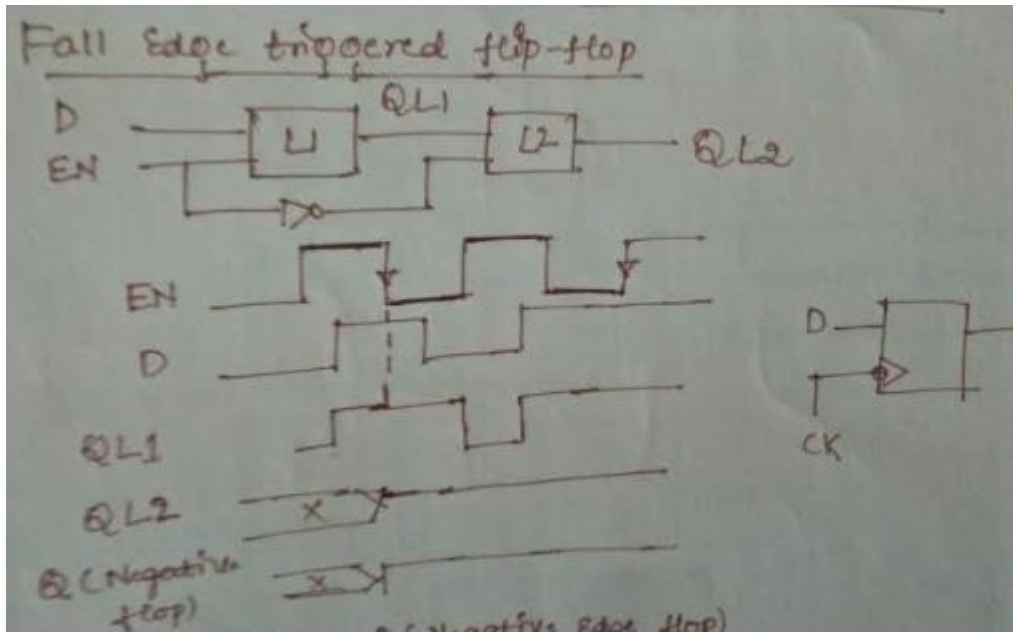



# *Difference between latch and flip-flop*

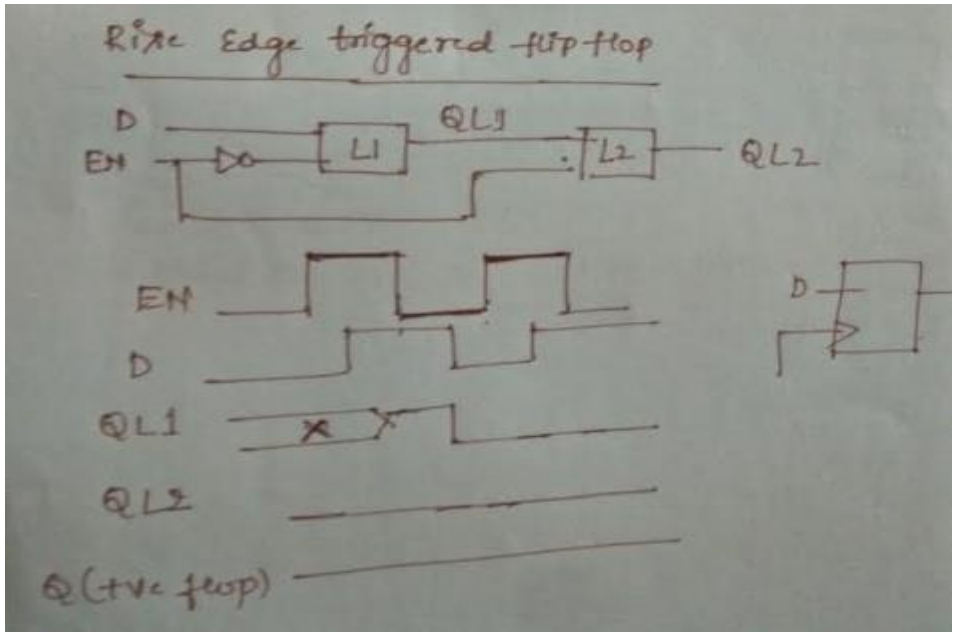
| Latches | Flip Flops |
|---|---|
| Latches are building blocks of sequential circuits and these can be built from logic gates | Flip flops are also building blocks oof sequential circuits. But, these can be built from the latches. |
| Latch continuously checks its inputs and changes its output correspondingly. | Flip flop continuously checks its inputs and changes its output correspondingly only at times determined by clocking signal |
| The latch is sensitive to the duration of the pulse and can send or receive the data when the switch is on | Flipflop is sensitive to a signal change. They can transfer data only at the single instant and data cannot be changed until next signal change. Flip flops are used as a register. |
| It is based on the enable function input | It works on the basis of clock pulses |
| It is a level triggered, it means that the output of the present state and input of the next state depends on the level that is binary input 1 or 0. | It is an edge triggered, it means that the output and the next state input changes when there is a change in clock pulse whether it may a +ve or -ve clock pulse. |

# *Example- Flip-flop realization using latches*

Fall edge triggered flip-flop




rise edge triggered flip-flop



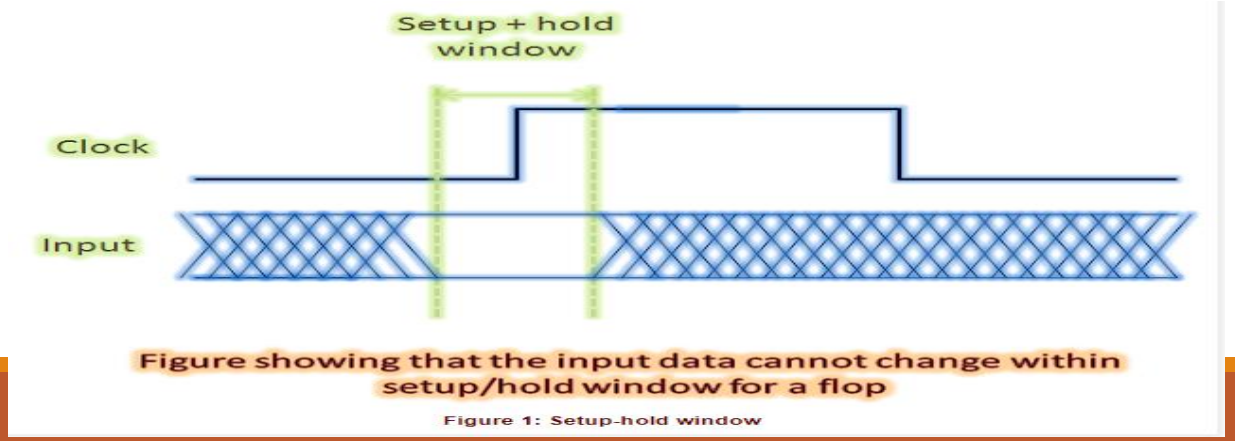
# *Setup/Hold time*

**Setup Time:**

- ✓Amount of time the data at the synchronous input (D) must be stable before the active edge of clock
- ✓ In other words, each flip-flop (or any sequential element, in general) needs some time for the data to remain stable before the clock edge arrives, such that it can reliably capture the data. This duration is known as **setup time**

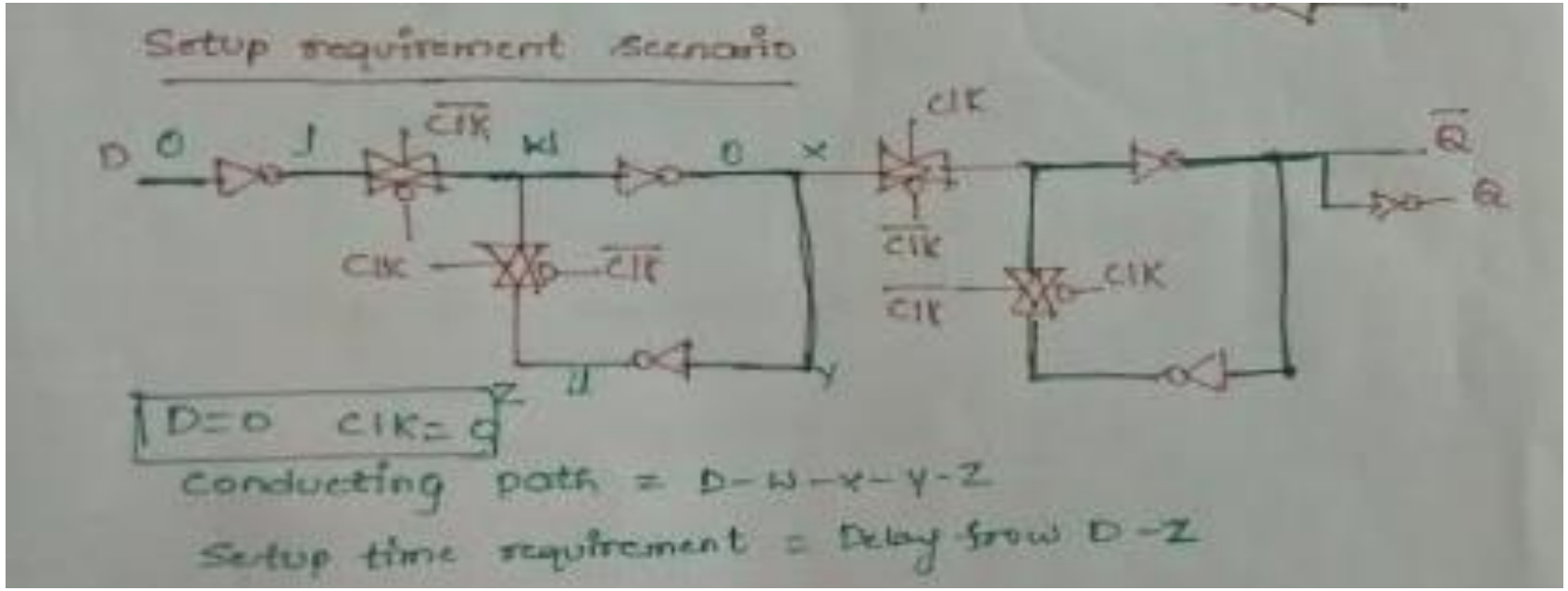
**Hold Time:**

- ✓Amount of time the data at the synchronous input (D) must be stable after the active edge of clock
- ✓Similar to setup time, each sequential element needs some time for data to remain stable after clock edge arrives to reliably capture data. This duration is known as **hold time**



# *Reasons for setup/Hold time ?*

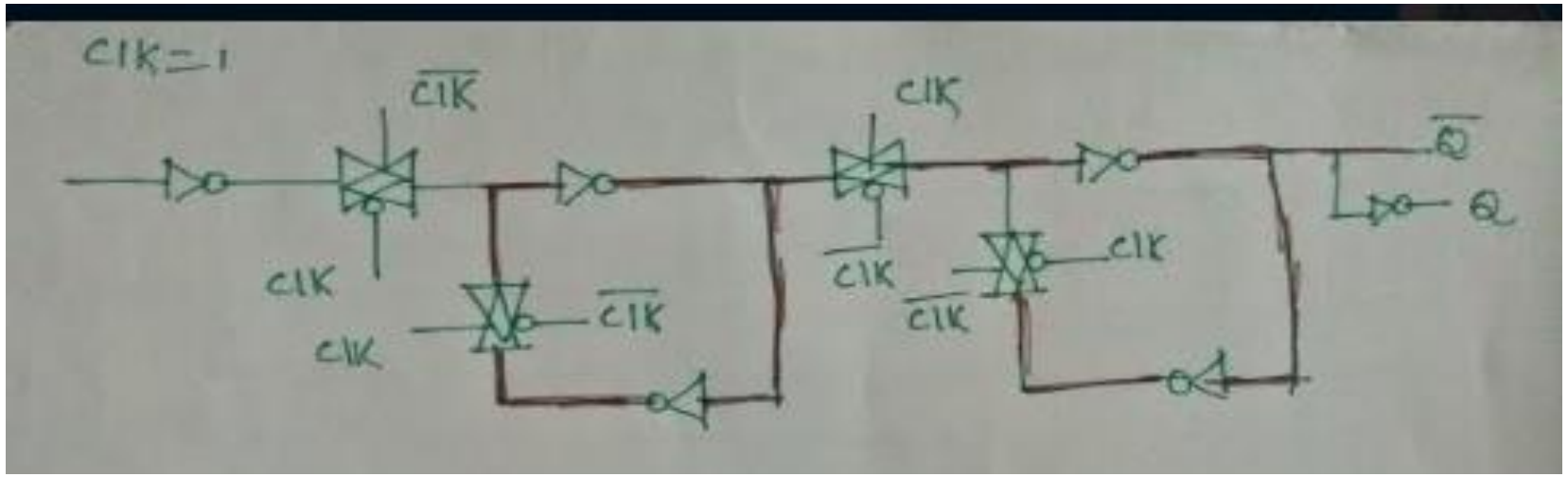
# Reason for SETUP Time




- when D = 0 and CLK is LOW, input D is reflected at node Z so that W = 1, Y = 0, and Z = 1 and it will take some time to traverse the path D-W-X-Y-Z. The time that it takes data D to reach node Z is called the SETUP time
- Any data sent before the setup time, as defined above, will produce a stable value at node Z. This defines the reason for the setup time within a flop

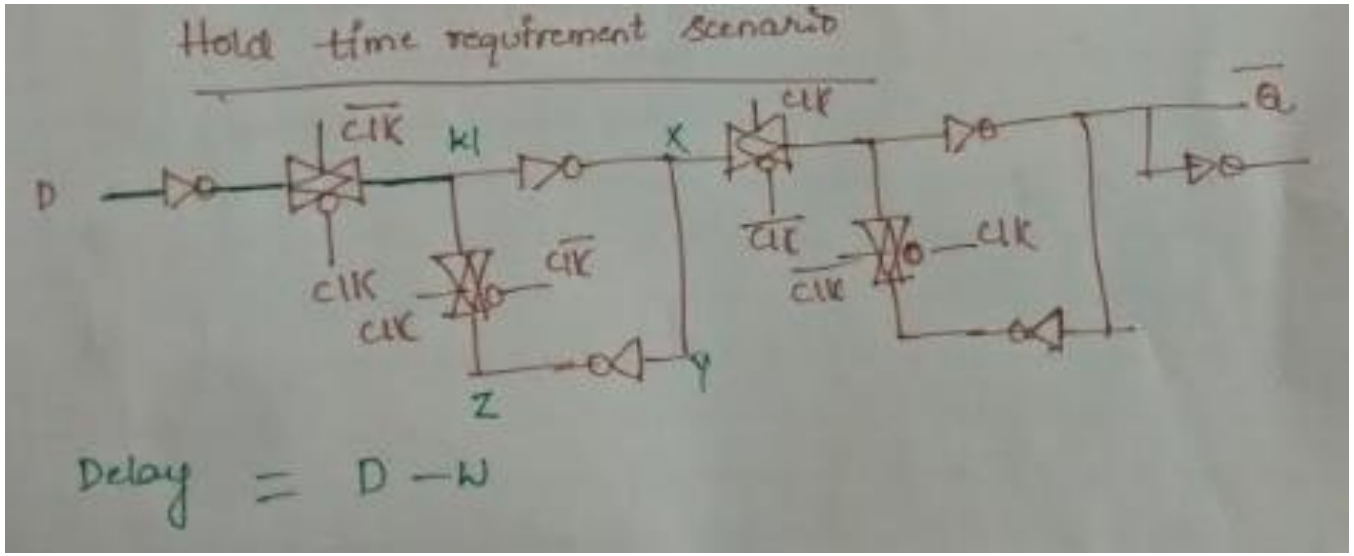
# *Reason for SETUP Time cntd..*

After active edge of clock , latched data present at first latch o/p passed to second latch



# *Reason for HOLD Time*

- After the clock edge, there is a certain time before the transmission gate itself closes completely. If any new data change now passes through this gate before its completely closes, the original data is now corrupted and hence correct data cannot come out of the RHS latch, hence hold time is required.



# *Max frequency of a design*

- Max frequency must be determined by locating the longest path among all the flip-flop paths in the circuit

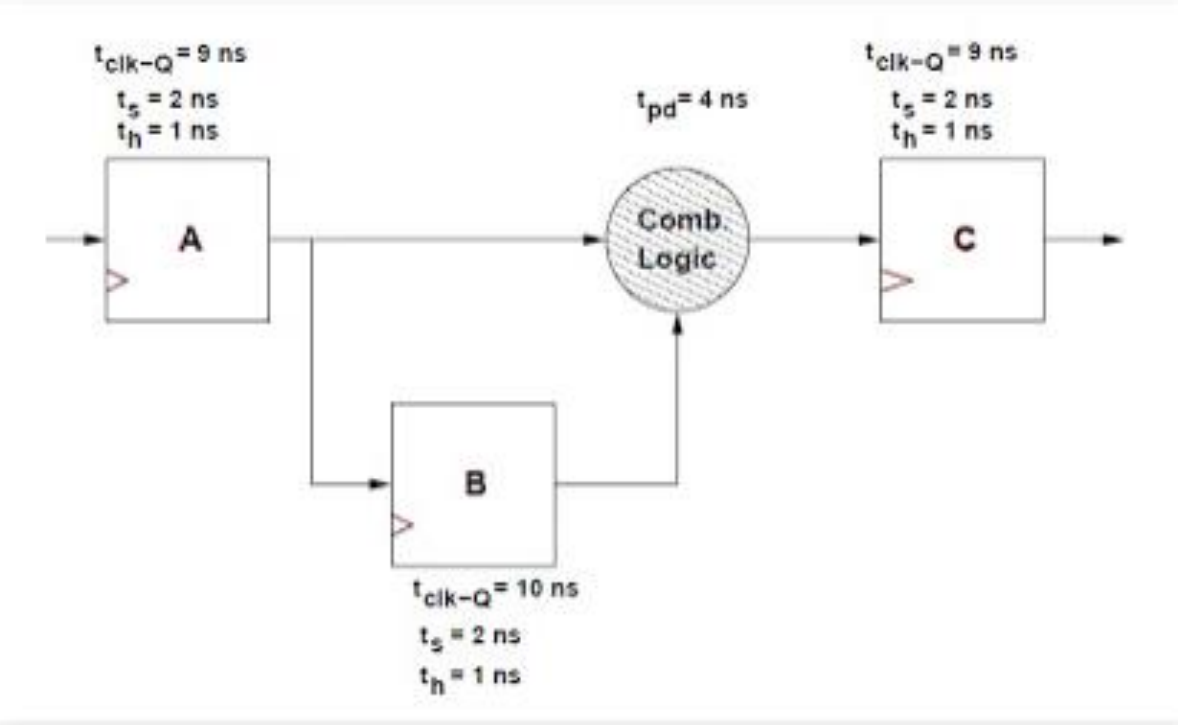
- General rule of thumb to calculate the max frequency

Minimum clock period = (Max data path delay ) – (Min data path delay)  -> Without considering the clock path

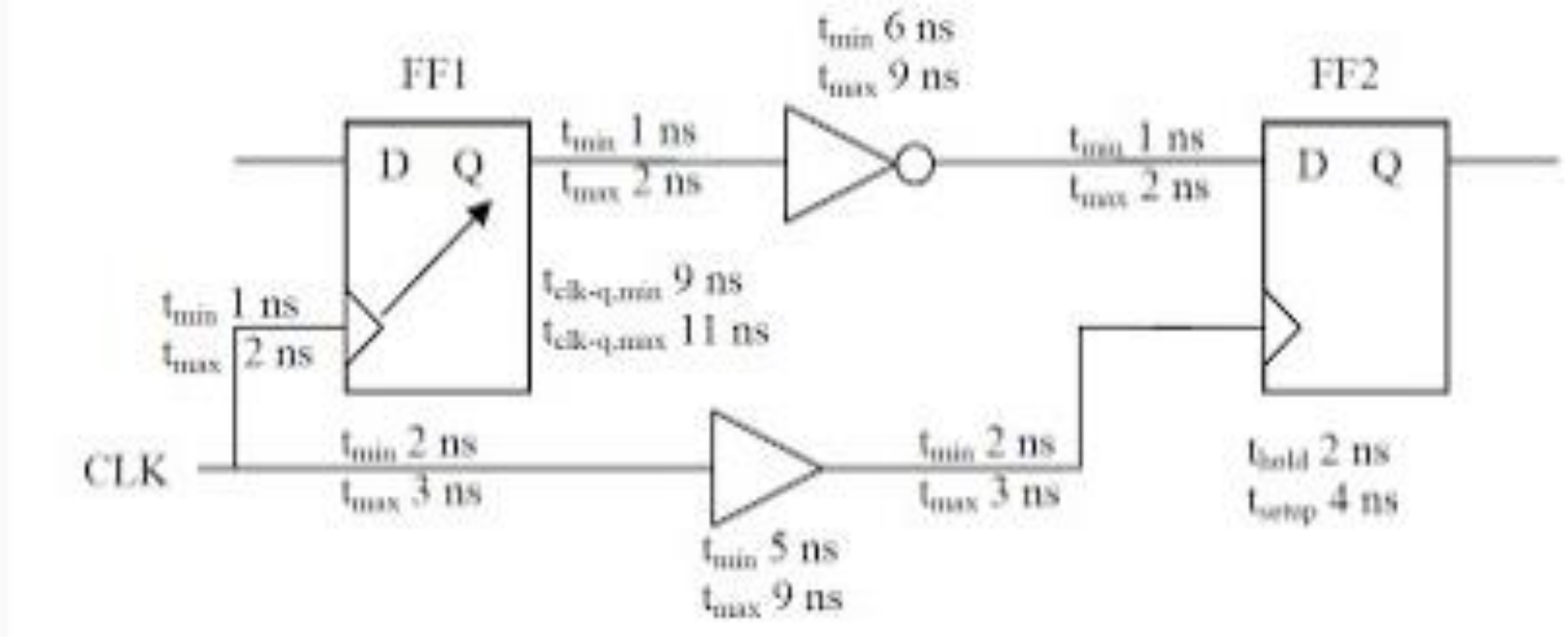
Max clock frequency = 1/ (Min clock period)

# *Examples of max frequency calculation*

Example 1 (No clock path delay defined in this example)




# *Example 2 (Clock min/Max considered)*




Thank you