(1) Chip utilization depends on ___

- Only on standard cells
- Standard cells and macros
- only on macros
- Standard cells macros & IO pads.

(2) Power switch off (PSO) | Power gating technique in low power is used to reduce

- Dynamic power
- Leakage power
- Internal power
- A & B

(3) Why do we re-order scan chains during placement?

- Because scan chains are group of flipflop.
- It does not have timing critical path.
- Existing scan is not physical aware
- None

(4) Best floorplan is achieved by

- Minimize area & delays
- Minimize total length of wire
- Maximize Routability
- all of the above
- a & c

(5) Delay of a cell depends on which factors?

- output transition and input load.
- Input transition and output load
- Input transition and output transition

- Input load and output load.

(6) Concept of fixing timing violations by adjusting clock arrival times at the registers in preCTS stage is called.

- Useful skew
- Time borrowing
- Slack adjustment
- There is no such ~~fix~~.

(7) Congestion can be resolved by

- Cell padding
- path groups
- Non Default Rules
- All of the above

(8) Clock buffers are preferred than normal buffers in clock Tree Building because of.

- 50% duty cycle
- Better Power
- Better area
- lesser transition.

(9) How will be build clock tree for a divided by 2 generated clock?

- Skew groups
- Defining ignore pins
- Defining through pins
- A & C.

(10) What is routing congestion in the design?

- Ratio of required routing tracks to available routing tracks
- Ratio of available routing tracks to required routing tracks
- Depends on the routing layers available
- None of the above.

(11) Orientation of a cell/Memory is obtained from

- TECH LEF
- CELL LEF
- .LIB
- QRC TECH FILE

(12) What is the effect of high drive strength buffer when added to long nets

- Delay on the net increases
- Capacitance on the net increases
- Delay on the net decreases
- IR drop reduces.

(13) In OCV timing check, for setup time, ___.

- Max delay is used for launch path & Min delay for capature path.
- Min delay is used for launch path & Max delay for capture path.
- Both Max delay is used for launch & capture path.
- Both Min delay is used for capature & launch paths.

(14) Clock specification file is dependent on

- Synopsis Design Constraints
- .LIB
- LEF
- Timing Corners.

(15) To prevent latch-up, which of the following cells are used.

- Tie cells
- Welltap cells
- Decap cells
- End cap cells

(16) Channel b/w macros will use the following kind of blockage

- soft Blockage
- Partial Blockage
- Hard Blockage
- Any of the above.

17. High fan-out net synthesis happens in which stage of VLSI flow?

- Synthesis
- preCTS
- CTS
- postCTS

18. Block A operates at 0.9V & Block B operates at 1V and is switchable. What kind of low power cells need to be added for paths between A & B?

- State retention cells
- Level shifter cells
- Isolation cells
- B & C.

19. DRC rule in physical design tools check the following.

- spacing
- Maximum allowed Density
- Opens
- A & C

20. Which of the following metal layer has Maximum resistance?

- Metal 2
- Metal 3
- Metal 4
- Metal 5.

21. CRPR stands for —

- Cell Reconvergence Pessimism Removal
- Cell Reconvergence preset Removal
- Clock Reconvergence Pessimism Removal
- Clock Reconvergence preset Removal

22. More IR drop is due to —

- Increase in metal width
- Increase in metal length
- Decrease in metal length
- Lot of metal layers.

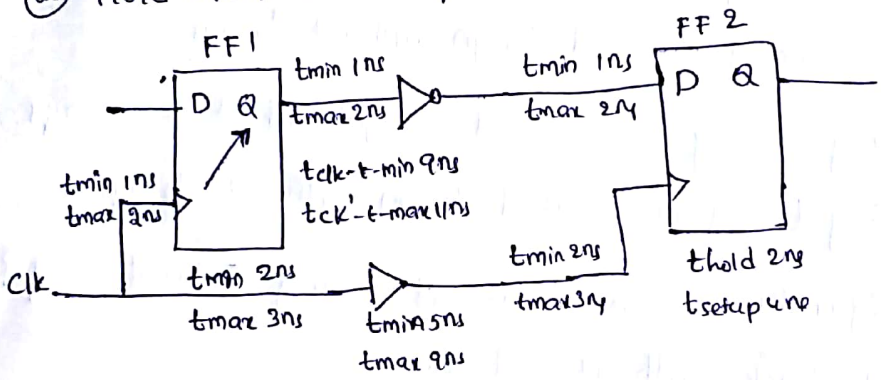
(23) Pitch of the wire is ____

- Min width
- Min spacing
- Min width - Min spacing
- Min width + Min spacing.

(24) What is the goal of CTS ?

- Minimum IR Drop
- Minimum EM
- Minimum skew
- Minimum slack.

(25) Hold slack for this path is ____



- 9ns
- 1ns
- 15ns
- -1ns.

(26) In a reg to reg timing path Tclocktoq delay is 0.5ns & TCombo delay is 5ns and Tsetup is 0.5ns then the clock period should be ____

- 1ns
- 3ns
- >= 6ns
- 6ns

(27) Which of the following is having highest priority at final stage (post routed) of the design ____ ?

- Setup violation
- skew
- Hold violation
- None

(28) In a reg to reg path if you have setup problem where will you insert buffer.

- close to Launch flop
- Close to capture flop
- Medtan of the net
- Any legal location allowed on the timing path.

(29) Timing sanity check means (with respect to PD) _____ ?

- Checking timing of routed design without net delays.
- checking timing of placed design with net delays
- Checking timing of unplaced design without net delays
- checking timing of routed design with net delays.

(30) Which configuration is more preferred during floorplanning?

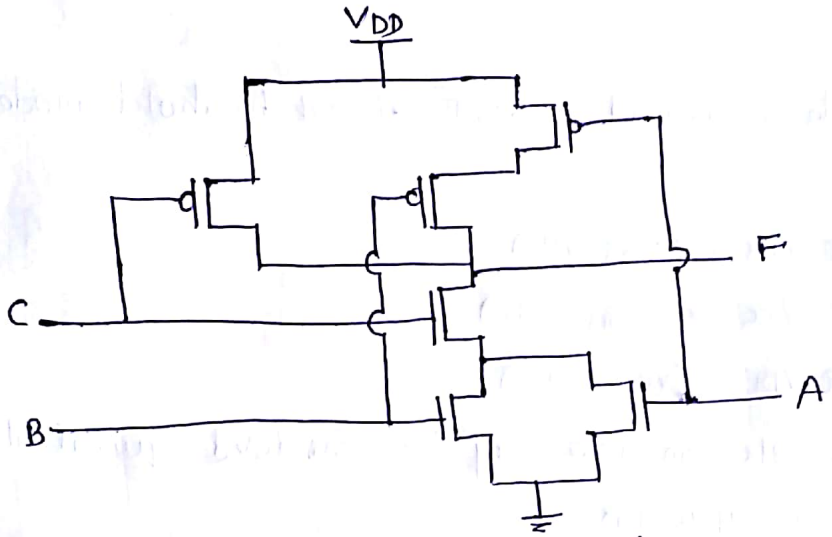
- Double back with flipped rows
- Double back with non flipped rows
- With Channel spacing blw rows and no double back
- With Channel spacing blw rows and double back.

1 mark

① For technology nodes below 65nm the cell CMOS delay ——
as temperature decrease

- Increases
- Decreases
- remains same
- none of these

② Find the correct boolean function for the following ckt.



- $((AB)+C)'$
- $((A+B)C)'$
- $(A'+B')C'$
- $(A'B')+C'$

③ The effective channel length of a MOSFET in a saturation decreases with increase in

- gate voltage
- drain voltage
- source voltage
- body voltage

④ The threhold voltage depends on ——

- Doping of channel
- Voltage blw source & substrate
- Temperature
- All of the above

⑤ A CMOS ckt only consumes a significant amount of power.

- when warming up

- when cooling off
- during output transitions
- during input transitions

(6) When the PMOS and NMOS are interchanged with one another in an inverter, it will act as ?

- Buffer
- Inverter
- AND gate
- OR gate

(7) For Enhancement mode n-channel MOSFET at subthreshold mode.

- $V_{GS} < V_{th}$
- $V_{GS} > V_{th}$ & $V_{DS} < (V_{GS} - V_{th})$
- $V_{GS} > V_{th}$ & $V_{DS} > (V_{GS} - V_{th})$
- $V_{GS} > V_{th}$ & $V_{DS} > (V_{GS} - V_{th})$

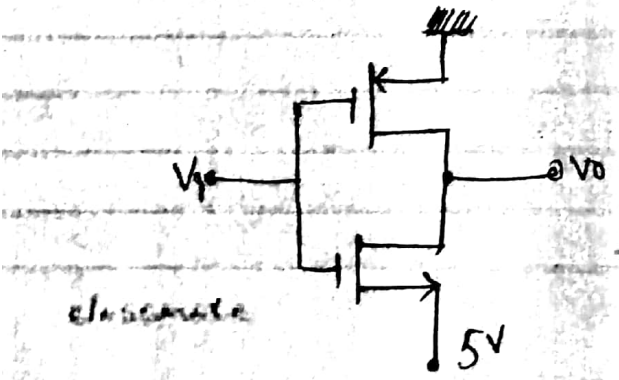
(8) The MOSFET switch in its on-state may be considered equivalent to

- Resistor
- Capacitor
- Inductor
- None of the above.

(9) What happens to delay if we include a resistance at the o/p of a CMOS circuit ?

- Increases
- Decreases
- Remains same

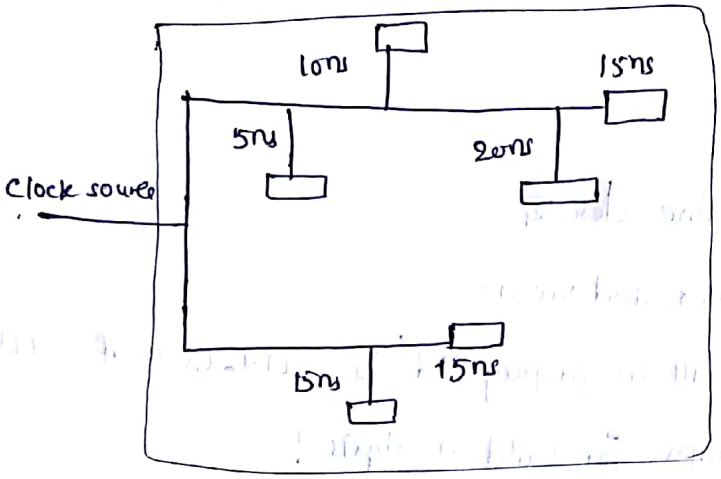
(10) The threshold voltage for each transistor in figure is 2V. For this ckt to work as an inverter, V_i must take the values



- -5V & 0 V
- -5V & 5 V
- 0V & 3V
- 3V & 5V

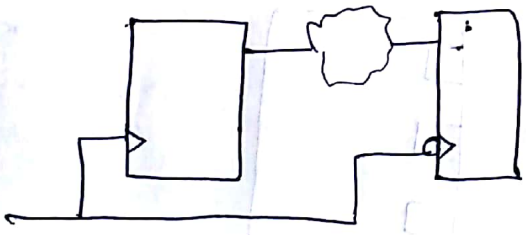
5Marks ⑤

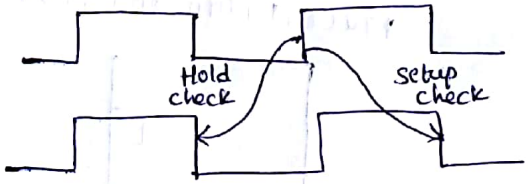
① What's the Insertion delay, global skew and the lowest local skew from the following clock tree built.



- 15ns Insertion delay, 5ns global skew and 0ns local skew
- 20ns Insertion delay, 5ns global skew and 5ns local skew
- 20ns Insertion delay, 15ns global skew and 5ns local skew
- 20ns Insertion delay, 15ns gobal skew and 0ns local skew

② What's the hold slack formula in this case where a path starts from positive edge triggered flop to negative edge triggered flop (Tclk is clock period; Thold is hold time; Tskew is clock skew; Tdata is data delay)?





- Tslack = Tclk/2 - Thold - Tskew + Tdata
- Tslack = Tclk/2 + Thold - Tskew + Tdata
- Tslack = Tclk + Thold - Tskew + Tdata
- Tslack = Thold - Tskew + Tdata

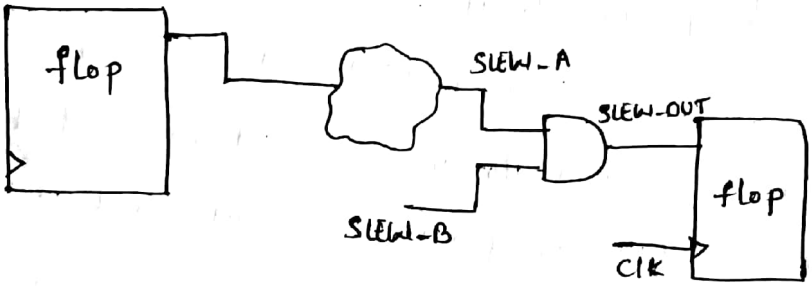
③ set_timing_derate_early 1.05

set_timing_derate_late 0.95

With the flat derates applied as above, what will happen to setup slack?

- Increase
- Decrease
- Remains same as before derates
- Depends on my corner and view.

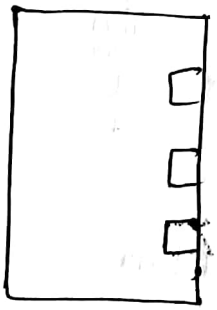
④ Which slew value will be propagated to SLEW_OUT if SLEW_A is 80ps and SLEW_B is 100ps for hold analysis?



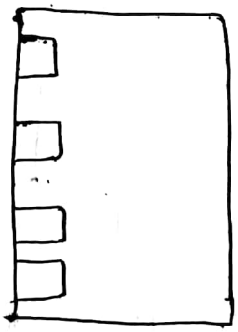
- 80 PS
- 100 PS
- 90 PS
- 180 PS

⑤ Calculate the channel width b/w the following macros in a design using 5 metal layers with a pitch of 0.4u, spacing of 0.2u, width of 0.2u for metal4 and metal5; pitch of 0.2u, spacing of 0.1u, width of 0.1u for metal2 and metal3.

Macro1 (pins in met3)

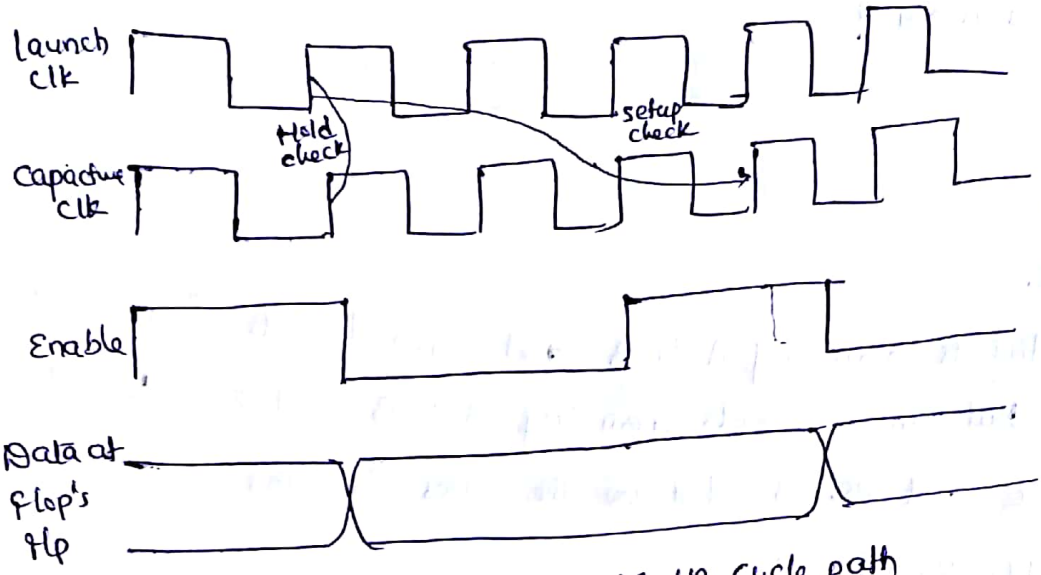


Macro2 (pins in met5)



- >= 1.4u
- >= 0.7u
- >= 0.56u
- >= 2.8u

⑥ Find the clock cycle used in the provided scenario:



- single Cycle
- Half cycle path
- Multi Cycle path
- False path.

1Mark:

① The sum of ages of 5 children born at the intervals of 3 years each is 50years. What is the age of the youngest child?

- 4 years
- None of these
- 8 years
- 10 years

② What is the probability of getting a sum 9 from two throws of a dice?

- 1/8
- 1/6
- 1/12
- 1/9

③ The average weight of 8 person's increases by 2.5kg when a new person comes in place of one of them weighting 65kg. what might be the weight of the new person?

- 89kg
- Data Inadequate
- 76kg
- 85kg

④. What is the sum of two consecutive even numbers, the different of whose squares is 84 ?

- 34
- 38
- 46
- 42

⑤ Two bus tickets from city A to B and three tickets from city A to C cost Rs.77 but three tickets from city A to B and two tickets from city A to C cost Rs. 73. what are the fares for cities B and C from A ?

- Rs.17, Rs.13
- Rs.13, Rs.17
- Rs 4, Rs.23
- Rs.15, Rs.14

⑥ A two digit number is such that the product of the digits is 8. when 18 is added to the number, then the digits are reversed. The number is :

- 18
- 24
- 81,
- 42

⑦ Look at this series : 31, 29, 24, 22, 17, __ what number should come next ?

- 15
- 14
- 13
- 12

⑧ A boat can travel with a speed of 13 km/hr in still water. If the speed of the stream is 4 km/hr. find the time taken by the boat to go 68 km downstream.

- 2 Hours
- 5 Hours
- 3 Hours
- 4 Hours

(9) A, B and C can do a piece of work in 20, 30 & 60 days respectively. In how many days can A do the work if he is assisted by B and C on every third day?

- 18
- 15
- 16
- 12

(10) In a garden, there are 10 rows, and 12 columns of mango trees, the distance blw the two trees is 2 metres and a distance of one metre is left from all sides of the boundary of the garden. The length of the garden is..

- 24 m
- 20 m
- 22 m
- 26 m

1 mark

(1) Decode the following Ascii message.

10100111010100101011000100101100 1
01000001001000100000110100101000100

- STUDY_HARD
- STUDY HARD
- study_hard
- study hard

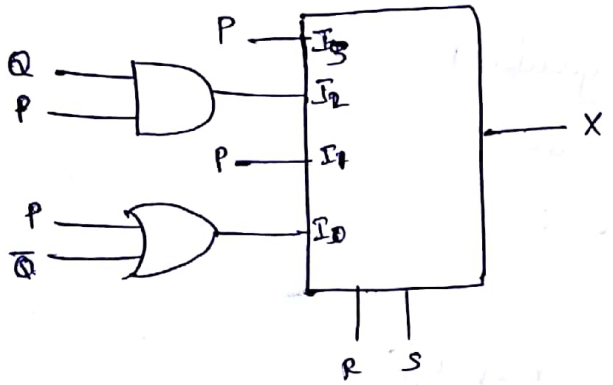
(2) A clock signal with a period of 1 s is applied to the input of an enable gate. The o/p must contain six pulses. How long must the enable pulse be active?

- Enable must be active for 0s
- Enable must be active for 3s
- Enable must be active for 6s
- Enable must be active for 12s.

③ An 8-bit serial in/serial out shift register is used with a clock frequency of 150KHz. What is the time delay between the serial i/p and the Q3 output?

- 1.67 s
- 26.67 μs
- 26.7 ms
- 267 ms

④ For the ckt shown in the following. I_0-I_3 are inputs to the 4:1 mux R(MSB) and S are control bits. The output Z can be represented by



- $PQ + PQ's + Q'R's'$
- $PQ' + PQR' + P'Q's'$
- $PQ'R' + P'QR + PARS + Q'R's'$
- $PQR' + PQRS' + PQ'R's + Q'R's'$

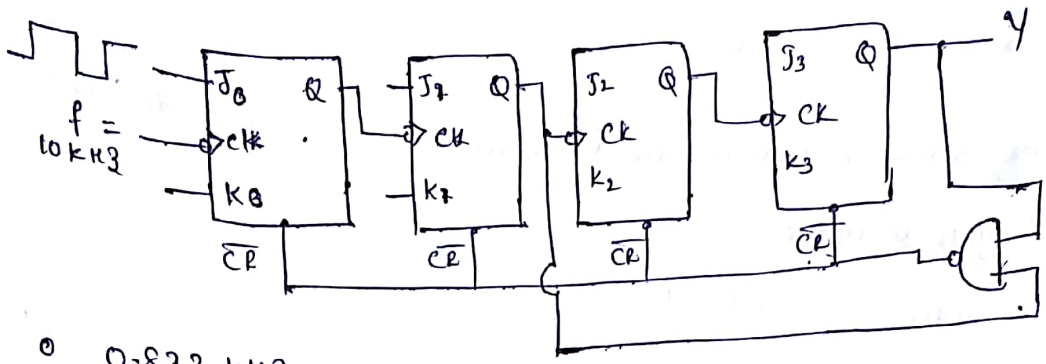
⑤ What are the minimum number of 2 to 1 mux required to generate a 2 i/p AND gate and a 2 i/p EX-OR gate?

- 1 and 2
- 1 and 3
- 1 and 1
- 2 and 2

⑥ On the third clock pulse, a 4 bit Johnson sequence is $Q_0=1$ $Q_1=1$ $Q_2=1$ and $Q_3=0$. On the fourth clock pulse, the sequence is ____

- $Q_0=1$, $Q_1=1$, $Q_2=1$, $Q_3=1$
- $Q_0=1$, $Q_1=1$, $Q_2=0$, $Q_3=0$
- $Q_0=1$, $Q_1=0$, $Q_2=0$, $Q_3=0$
- $Q_0=0$, $Q_1=0$, $Q_2=0$, $Q_3=0$

(7) In the figure, the J & K i/p's of all the four flip flops are made high. The frequency of the signal at o/p Y is.



- 0.833 kHz
- 1.0 kHz
- 0.91 kHz
- 0.77 kHz.

(8) A 16 bit module 16 ripple counter uses JK flipflops. If the propagation delay of each flipflop is 50 nsec. the maximum clock frequency that can be used is equal to ___ (in MHz).

- 12
- 1
- 5
- 9

(9)

(10) An 8 bit successive approximation analog to digital communication has full scale reading of 2.55V and its conversion time for an analog input of 1V is 20 μs. The conversion time for a 2V input will be

- 10 µs
- 40 µs
- 20 µs
- 50 µs

1Mark

① If A = 4'b1xxz and B = 4'b1xxx, then A === B will return

- o 1
- o z
- o x
- o 0

② If time scale is defined as timescale 10ns/1ns and #1.55 a=b; then 'a' gets 'b' after

- • 10 ns
- o 15.5 ns
- o 11 ns
- o 16 ns

③ In the given code snippet, statement 2 will executed at

```
Initial
begin
#5x=1'b0; // statement 1
#15y=1'b1; // statement 2
End
```

- • 15
- o 5
- o 20
- o current simulation time

④ Which logic level is not supported by verilog?

- • U
- o z
- o x
- o None of the above

⑤ Which level of abstraction level is available in Verilog but not in VHDL?

- • Behavioral level
- o Dataflow level
- • Gate level
- o Switch level

1 mark

① Consider the following C function:

```
int f(int n)
{
  static int i = 1;
  if (n >= 5)
    return n;
  n = n + i;
  i++;
  return f(n);
}
```

- 5
- 6
- 7
- 8

The value returned by f(1) is

② Loss in precision occurs for typecasting from —

- char to short
- float to double
- long to float
- float to int

③ The loop in which the statements within the loop are executed least once is called —

- do-while
- while
- for
- goto

④ What is the output of the program given below ?

```
#include
int main()
{
 enum status { pass, fail, atkt };
 enum status stud1, stud2, stud3;
 stud1 = pass;
 stud2 = atkt;
 stud3 = fail;
printf ("%d, %d, %d\n", stud1, stud2, stud3);
 return 0;
}
```

- 0 0, 1, 2
- 1, 2, 3
- 0 0, 2, 1
- 0 3, 2, 1

⑤ The value of j at the end of the execution of the following C program:

```
int incr (int i)
{
   static int count = 0;
   count = count + i;
   return (count);
}
main()
{
   int i, j;
   for (i=0; i<=4; i++)
     j = incr(i);
}
```

- 0 10
- 0 4
- 0 6
- 0 7