ECE5015	DIGITAL IC DESIGN	L	T	P	J	C
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Pre-requisite	**Nil**					**v 1.0**

Course Objective:

The course is aimed to

1. apply the models for state-of-the-art VLSI components, fabrication steps, hierarchical design flow and semiconductor business economics to judge the manufacturability of a design and assess its manufacturing costs.
2. focus on the systematic analysis and design of basic digital integrated circuits in CMOS technology.
3. enhance problem solving and creative circuit design techniques.
4. emphasize on the layout design of various digital integrated circuits.
5. focus on the methodologies and design techniques related to digital integrated circuits.

Expected Course Outcome :

At the end of the course the student will be able to

1. Understand design metric and MOS physics
2. Design layout for various digital integrated circuits.
3. Design the CMOS inverter with optimized power, area and timing.
4. Design static and dynamic digital CMOS circuits.
5. Understand the timing concepts in latch and flip-flops.
6. Design CMOS memory arrays.
7. Understand interconnect and clocking issues.

Student Learning Outcomes (SLO):	**5,6,14**

Module:1	**Introduction:**	**3 hours**

Issues in Digital IC Design- Quality Metrics of a Digital Design - MOS Transistor Theory.

Module:2	**Fabrication Technologies:**	**7 hours**

VLSI Manufacturing Process Steps - Crystal Growth - Wafer cleaning – Oxidation - Thermal Diffusion - Ion Implantation – Lithography –Epitaxy – Metallization -Dry and Wet etching and Packaging.

Fabrication of MOSFET with Metal Gate and Self-aligned Poly-Gate Processes with details on CMOS Design Rules and Layouts, Fabrication of CMOS inverter with details on Design Rules and Layouts.

Module:3	**The CMOS Inverter:**	**5 hours**

Static CMOS Inverter- Static and Dynamic Behavioural Practices of CMOS Inverter – Noise Margin.

Components of Energy and Power – Switching -Short-Circuit and Leakage Components.

Technology scaling and its impact on the inverter metrics - Passive and Active Devices.

Module:4	**Static & Dynamic CMOS Design:**	**8 hours**

Complementary CMOS -Ratioed Logic (Pseudo NMOS, DCVSL) - Pass Transistor Logic -

Transmission gate logic - Dynamic Logic Design Considerations - Speed and Power Dissipation of Dynamic logic -Signal integrity issues -Domino Logic.		
Module:5	**CMOS Sequential Logic Circuit Design:**	**5 hours**
Introduction - Static Latches and Registers - Dynamic Latches and Registers - Pulse Based Registers - Sense Amplifier based registers -Latch vs. Registerbased pipeline structures.		
Module:6	**Designing Memory & Array structures:**	**7 hours**
SRAM and DRAM Memory Core - memory peripheral circuitry - Memory reliability and yield - Power dissipation in memories.		
Module:7	**Interconnects and Timing Issues:**	**8 hours**
Resistive, Capacitive and Inductive Parasitics - Computation of R, L and C for given inter-connects - Buffer Chains - Timing classification of digital systems - Synchronous Design - Origins of Clock Skew/Jitter and impact on Performance - Clock Distribution Techniques - Latch based clocking - Synchronizers and Arbiters -Clock Synthesis and Synchronization using a Phase-Locked Loop.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45 hours**
Text Book(s)		
1.	Jan M. Rabaey, AnanthaChadrakasan, BorivojeNikolic, Digital Integrated Circuits: A Design Perspective, PHI, Second Edition, 2016.	
2.	Neil.H, E.Weste, David Harris, Ayan Banerjee, CMOS VLSI Design: A Circuit and Systems Perspective, Pearson Education, Fourth Edition, 2011.	
Reference Books		
1.	Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis and Design, McGraw-Hill, Fourth Edition, 2014.	
2.	Sorab K Gandhi, VLSI Fabrication Principles: Si and GaAs, John Wiley and Sons, Second Edition, 2010.	
Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).		
List of Projects (Indicative)		
1. Design and simulate a 16-bit comparator by using 8T full adders 2. Pass transistor logic based ALU design using low power full adder design 3. Design of high performance power efficient flip-flop using transmission gates 4. Design of high performance 5:32 decoder using 2:4,3:8 mixed logic line decoders. 5. Design of current comparator using FINFET 6. Analysis of leakage current and leakage power reduction during reduction in CMOS SRAM cell 7. Design of encoder for a 5GS/S 5 bit flash ADC 8. Design a 65 nm reliable 6T CMOS SRAM cell with minimum size transistors		
Mode of Evaluation:Review I, II and III		

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016