ECE5016	ANALOG IC DESIGN	L	T	P	J	C
		3	0	2	0	4
Pre-requisite	**Nil**				**v 1.0**	

Course Objectives :

The course is aimed to

1. analyze and design single-ended and differential IC amplifiers.
2. understand the relationships between devices, circuits and systems.
3. emphasize the design of practical amplifiers, small systems and their design parameter trade-offs.

Expected Course Outcome :

At the end of the course the student will be able to

1. Analyse low-frequency characteristics of single-stage amplifiers and differential amplifiers.
2. Analyse high-frequency response and noise of amplifiers.
3. Understand the feedback concepts.
4. Analyse and Design of High Gain Amplifiers.
5. Understand stability analysis and frequency compensation techniques of amplifiers.
6. Understand the basic concepts, non-idealities and applications of PLLs.
7. Design and characterize amplifiers according to design specifications in Cadence CAD software.

Student Learning Outcomes (SLO): **1,5,17**

Module:1	**Current source and Amplifier design:**	**8hours**

MOS Device models, MOS Current Sources and Sinks, Current Mirror: Basic Current Mirrors, Cascode current Mirrors. Bandgap references. Single stage Amplifies: Basic concepts, Common Source stage, Common Gate stage, Cascode stage. Differential stage: Single ended and Differential operation. Basic Differential Pair.

Module:2	**Frequency response and Noise analysis of Amplifiers:**	**8hours**

Miller effect, Frequency response of Common Source stage, Common Gate stage, Cascode stage and Differential pair. Noise in Amplifiers: Common Source stage, Common Gate stage, Cascode stage, Differential pair. Noise Bandwidth.

Module:3	**Feedback Amplifiers:**	**7hours**

Ideal feedback equation, Gain sensitivity, Effect of Negative Feedback on Distortion, Types of Feedback Amplifiers. Feedback configurations: voltage-voltage, current-voltage, current-current, voltage-current feedback. Practical configurations and Effect of loading.

Module:4	**Operational Amplifier**	**8hours**

Common mode Feedback circuits, Op Amp CMRR requirements, Need for Single and Multistage amplifiers, Effect of loading in Differential stage. Performance Analysis: DC gain, Frequency response, Noise, Mismatch, Slew rate of cascode and two stage Op Amps, Fully Differential Op Amps, Common-Mode feedback loop stability.

Module:5	**Stability analysis**	**4 hours**

Basic Concepts, Instability and the Nyquist Criterion, Stability Study for a Frequency-Selective

Feedback Network, Effect of Pole Locations on Stability		
Module:6	**Frequency compensation**	**4hours**
Frequency Compensation: Concepts and Techniques for Frequency Compensation – Dominant pole, Miller Compensation, Compensation of Miller RHP Zero, Nested Miller, Compensation of two stage OP Amps.		
Module:7	**Phase Locked Loops**	**4hours**
Problem of Lock acquisition, Phase Detector, Basic PLL and its dynamics, Charge-pump PLL, Non-ideal effects in PLL: PFD/CL non idealities, Jitter, Delay Locked Loop, Applications.		
Module:8	**Contemporary issues:**	**2hours**
	Total Lecture hours:	**45hours**

Text Book(s)	
1.	BehzadRazavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, Second Edition, 2017.
2.	David Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley & Sons, Inc., Second Edition, 2012.
Reference Books	
1.	Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, UK, Second Edition, 2010.
2.	R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, IEEE Press Series on Microelectronic Systems, Wiley Publications, Third Edition, 2010.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Challenging Experiments (Indicative)		
1	Analysis and Design of Common Source Amplifier with Diode Connected Load and Suggest a Circuit to achieve higher gain.	4 hours
2	Analysis and Design of Common Gate Amplifier with Resistive load and Current Source load. Justify the results in terms of input impedance of the circuit.	4 hours
3	Analysis and Design of Simple Current Mirror and Suggest a circuit to minimize the error in the output current.	4 hours
4	Analysis and Design of Differential Amplifier with Active load and Current Source Load.	6 hours
5	Analysis and Design of Cascode Amplifier and Suggest a Circuit to overcome Voltage Headroom Limitation.	4 hours
6	Analysis and Design of Two-Stage Opamp with Frequency Compensation.	8 hours
	Total Laboratory hours:	30 hours

Mode of Evaluation:Continuous assessment of challenging experiments /Final Assessment Test (FAT).

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016