DESIGN FOR TESTABILITY

GENERATING TESTS FOR LARGE CIRCUITS IS VERY TIME CONSUMING. ONE WAY TO GET AROUND THIS PROBLEM IS TO CONSTRAIN OR MODIFY THE DESIGN TO MAKE TEST GENERATION EASIER

MOST DFT TECHNIQUES ARE TARGETET TO SEQUENTIAL CIRCUITS WHERE TEST GENERATION IN GENERAL IS A DIFFICULT PROBLEM

IF TESTING IS NOT CONSIDERED DURING THE DESIGN PHASE VERY LOW FAULT COVERAGES CAN RESULT IN ADDITION TO HIGH TEST GENERATION TIMES
=> DFT SAVES MONEY + TIME!

DFT TECHNIQUES CAN BE DIVIDED INTO:

- AD HOC TECHNIQUES
- STRUCTURED DESIGN TECHNIQUES
- SELF-TEST + BUILD-IN TESTING

THE OBJECTIVE OF DFT IS TO IMPROVE THE CONTROLLABILITY AND OBSERVABILITY OF INTERNAL CIRCUIT NODES SO THAT THE CIRCUIT CAN BE TESTED EFFECTIVELY:

CONTROLLABILITY:

THE ABILITY TO SET OR RESET INTERNAL NODES FROM THE PRIMARY INPUTS

OBSERVABILITY:

THE ABILITY TO OBSERVE THE VALUE OF AN INTERNAL NODE AT THE PRIMARY OUTPUTS

THESE ARE TWO GOOD MEASURES OF THE TESTABILITY OF A CIRCUIT, i.e. HOW EASY IT IS TO TEST. DESIGN FOR TESTABILITY ATTEMPTS TO IMPROVE CIRCUIT TESTABILITY BY MAKING THE INTERNAL NODES MORE CONTROLLABLE AND OBSERVABLE

AD-HOC DFT TECHNIQUES

(I) Test Points

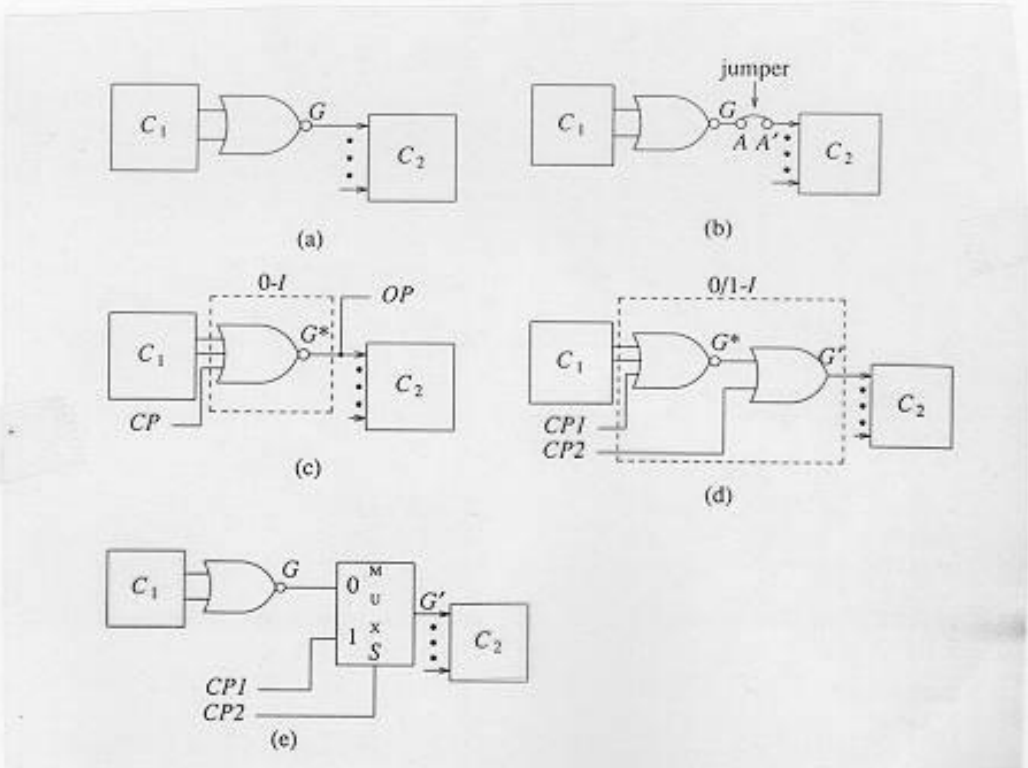
(a) ORIGINAL CIRCUIT

(b) "JUMBER": EXTERNAL TEST EQUIPMENT CAN OBSERVE AND/OR INJECT LOGIC VALUES ON A/A'.

(c) Ø-CONTROLLABILITY PLUS OBSERVABILITY

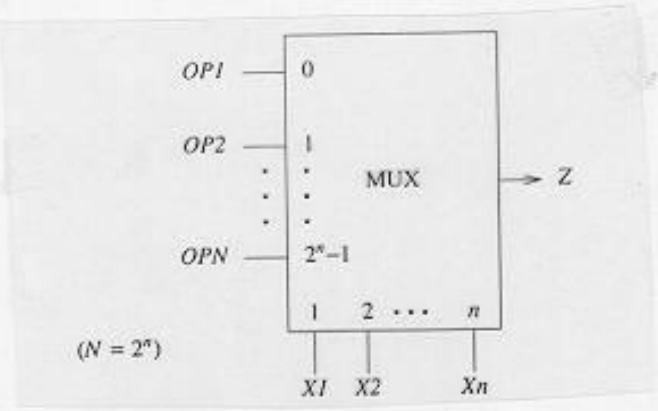
(d) Ø-1-CONTROLLABILITY

(e) 0-1-CONTROLLABILITY VIA THE USE OF A MULTIPLEXER

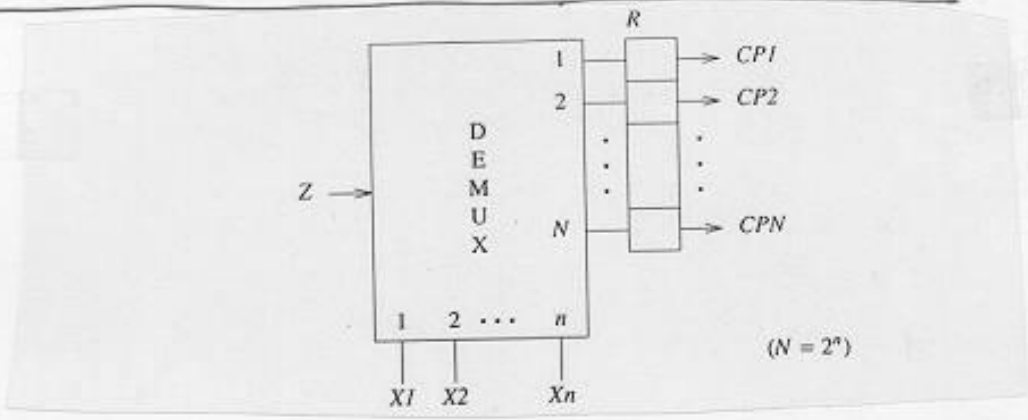


USING TEST POINTS REQUIRE A SIGNIFICANT NUMBER OF I/O PINS. TO ALLEVIATE THE PROBLEM WE USE THE FOLLOWNG TRADE OFFS:

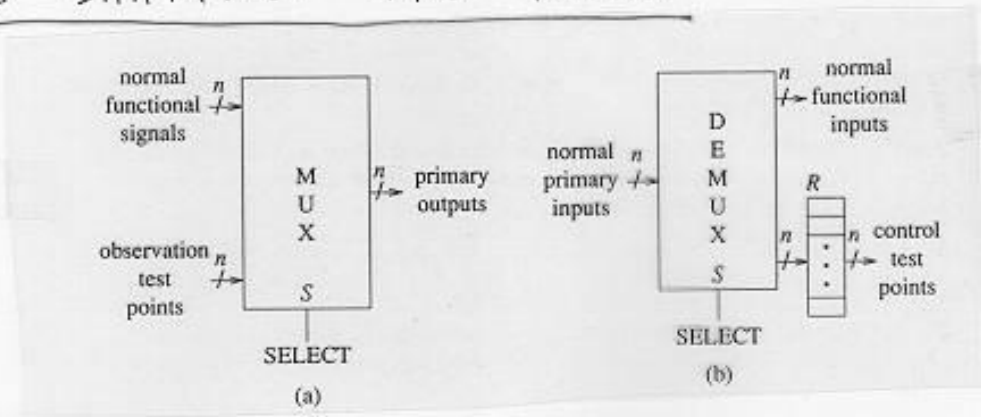
MULTIPLEXING OBSERVATION POINTS



CONTROLLABILITY VIA A DEMULTIPLEXER



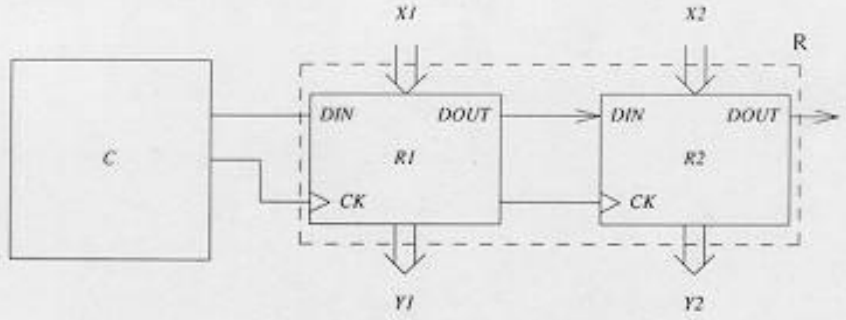
TIME SHARING I/O PORTS



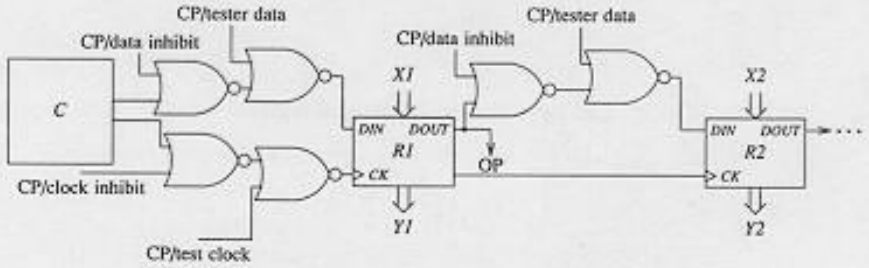
(II) Initialization

DESIGN CIRCUITS SO THAT IT IS EASY TO INITIALIZE THEM

(III) Counter and Shift Register Partitioning



(a)



(b)

REGISTER
$R = R_1 + R_2$
WITHOUT TESTABILITY FEATURE

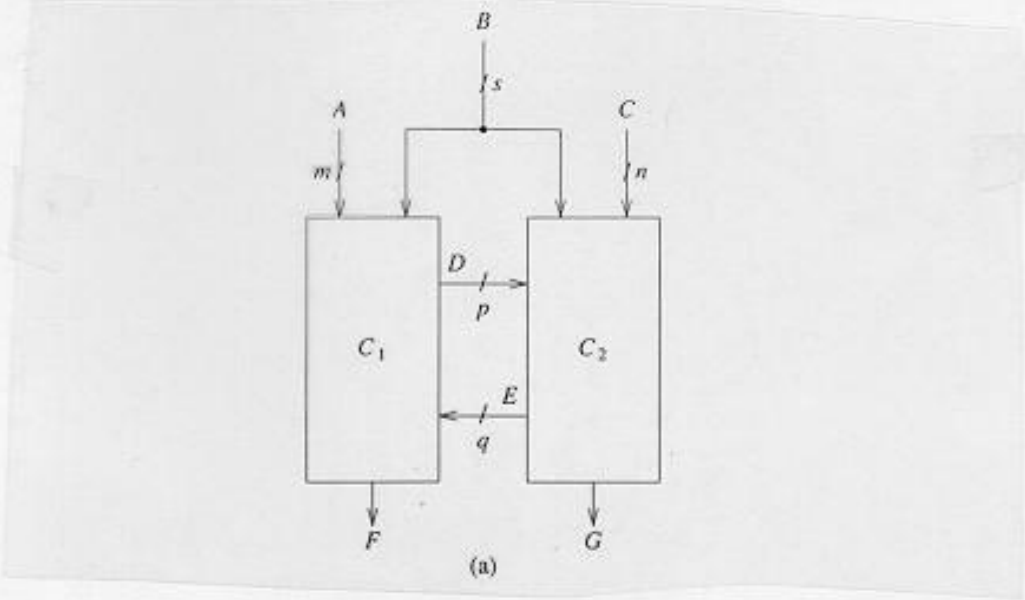
... WITH TESTABILITY FEATURE

SAVINGS:

16-bit counter needs $2^{16} = 65536$ clock cycles.

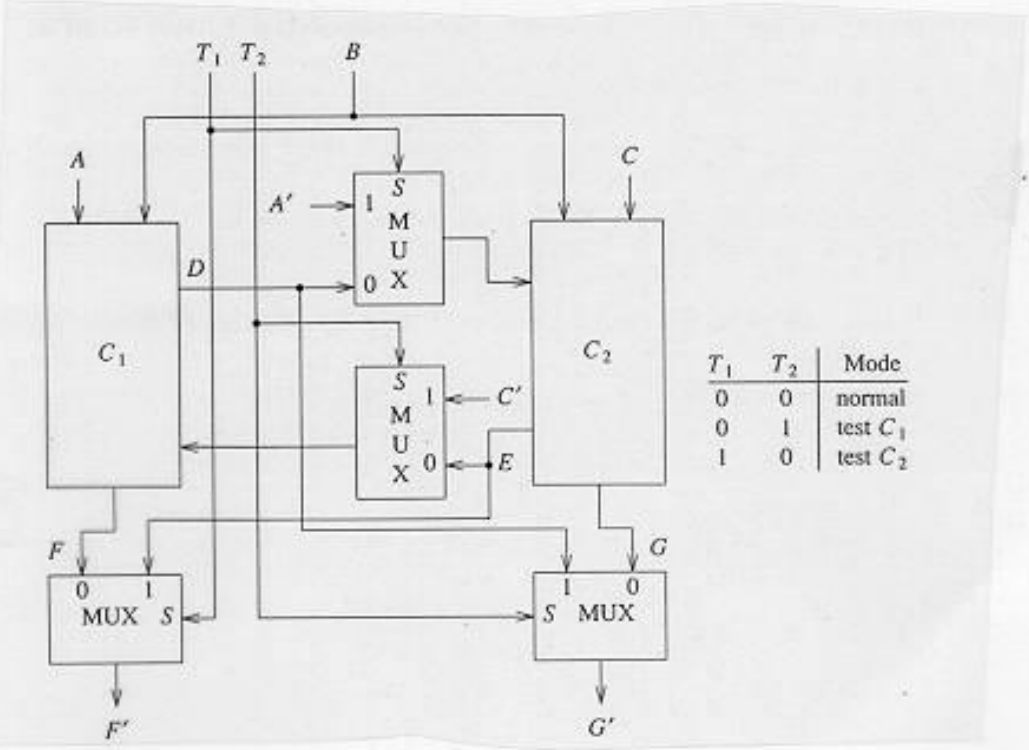
"Partitioned" in 2 8-bit counters it needs $2 \cdot 2^8 = 512$ clock cycles.

(IV) Partitioning of large combinational structures



INSERT MULTIPLEXERS BETWEEN THE LARGE COMBINATIONAL STRUCTURE $C = C_1 + C_2$:

- $T = 00$ normal operation
- $T = 01$ tests C_1 as inputs to C_1 are A and C' and it outputs to F G'
- $T = 10$ tests C_2



T_1	T_2	Mode
0	0	normal
0	1	test C_1
1	0	test C_2

Control points usually are:

- control, address, data buses
- enable/hold to microprocessors & memories
- data select to MUXes
- clock, presets to FFs, counters, shift registers

Observation points usually are:

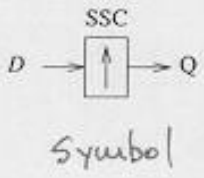
- stem lines with high Fanout
- redundant signal lines
- outputs of MUXes
- FFs, counters, shift registers
- address, control, data buses

DFT WITH SCAN REGISTERS

TEST POINTS ARE EXPENSIVE IN TERMS OF I/O PINS. SCAN REGISTER (MADE WITH SCAN CELLS) IS A REGISTER WITH BOTH SHIFT AND PARALLEL-LOAD ABILITY. ITS SCAN CELLS CAN BE USED AS OBSERVATION AND/OR CONTROL POINTS.

TRADE OFF: Saves I/O pins increases test time and area overhead

SCAN CELL

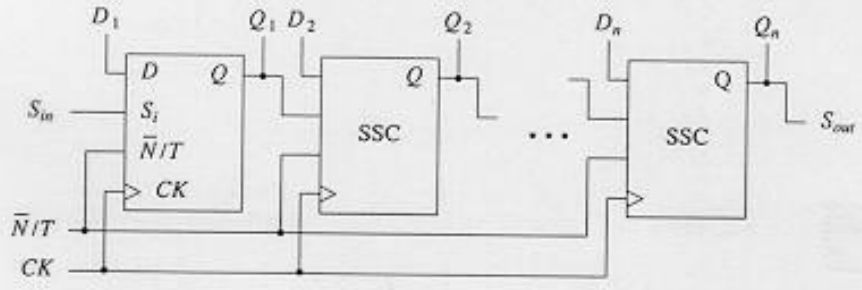


Symbol

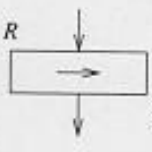
$\bar{N}/T = 0$ loads From D

$\bar{N}/T = 1$ loads From S_i

SCAN REGISTER



(c)



Symbol

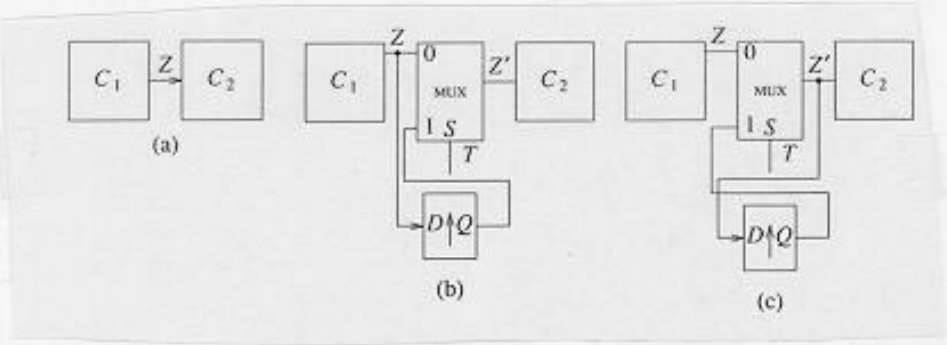
$\bar{N}/T = 1$ shifts From S

$\bar{N}/T = 0$ loads in parallel

SCAN IN: loading From S_{in}

SCAN OUT: reading From S_{out}

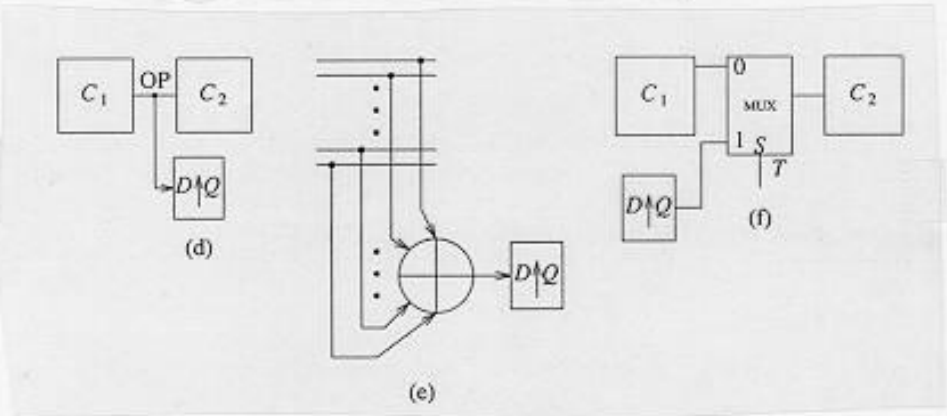
Simultaneous Controllability and Observability



ORIGINAL CIRCUIT

TWO VARIANTS OF SIMULTANEOUS CONTROLLABILITY AND OBSERVABILITY (DEPENDING OF MUX's SELECT LINE)

NON-SIMULTANEOUS TECHNIQUES



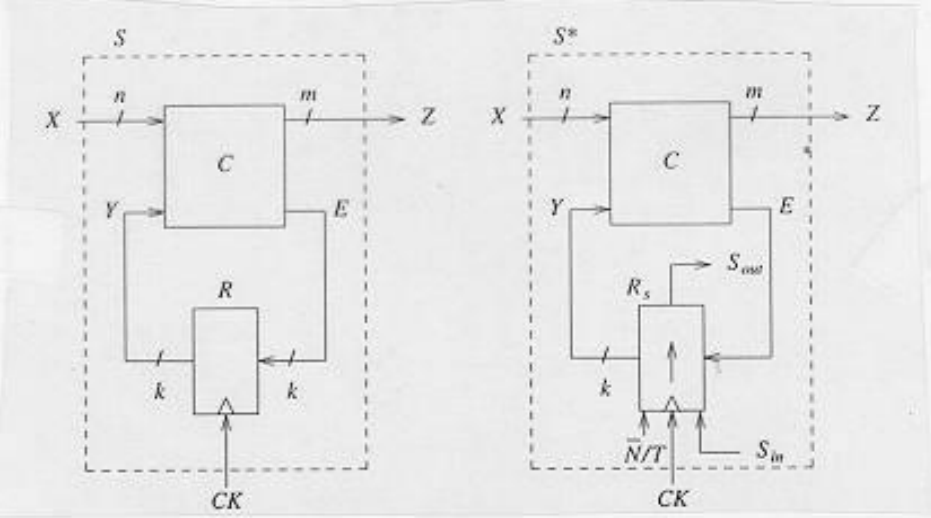
OBSERVABILITY

OBSERVABILITY THROUGH COMPACTION

CONTROLLABILITY

GENERIC SCAN-BASED DESIGNS

FULL SERIAL INTEGRATED SCAN



ORIGINAL CIRCUIT →

MODIFIED CIRCUIT WITH SCAN REGISTER R_s ←

TEST GENERATION + FAULT DETECTION ON MODIFIED CIRCUIT:

Run PODEM on combinational structure assuming Y and E are pseudo inputs/outputs.

You get a sequence of

(x_1, y_1) (x_2, y_2) ... test vectors

(z_1, e_1) (z_2, e_2) ... responses

To test the device:

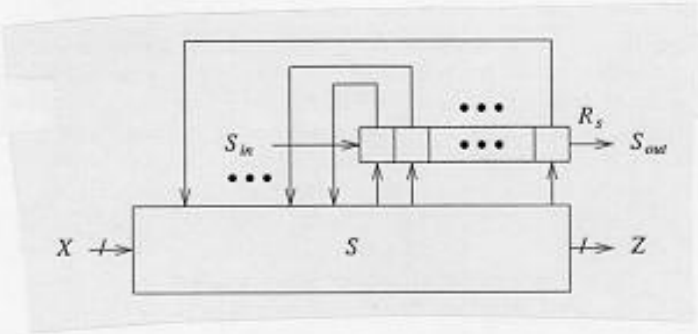
Scan in y_1 and at k^{th} clock cycle apply x_1.

After clock cycle load e_1 in R_s

and observe z_1 etc...

ISOLATED SERIAL SCAN

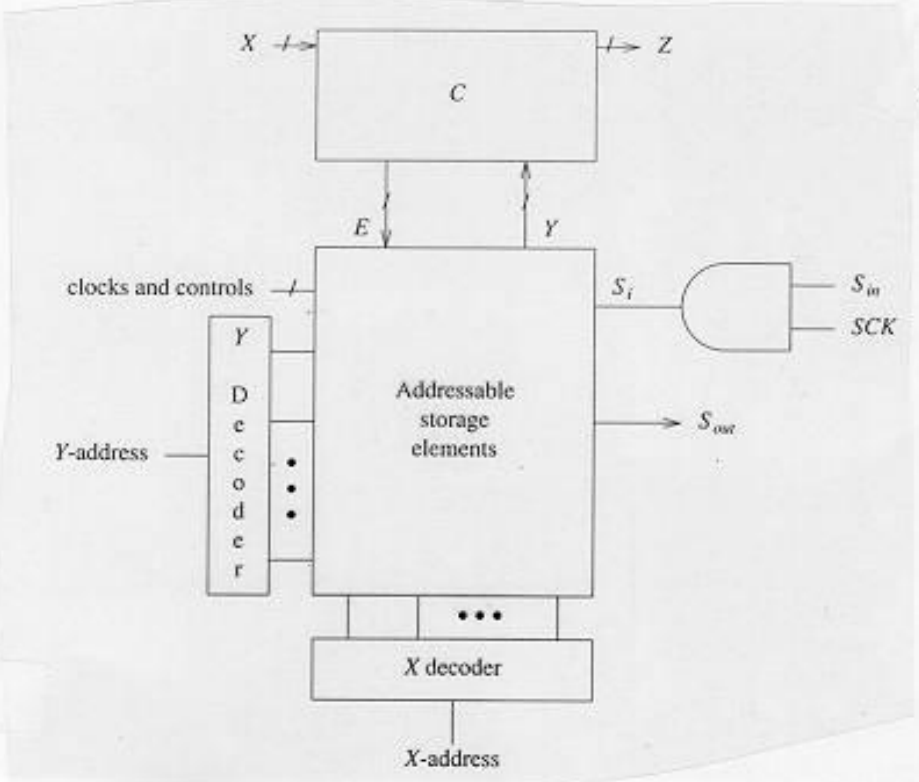
SCAN REGISTER IS NOT IN DATA PATH AS BEFORE (see figure below)



IF $|R_s| = |R|$ THEN WE HAVE FULL ISOLATED SCAN:

- accomodates on-line testing vs. full serial
- hardware overhead

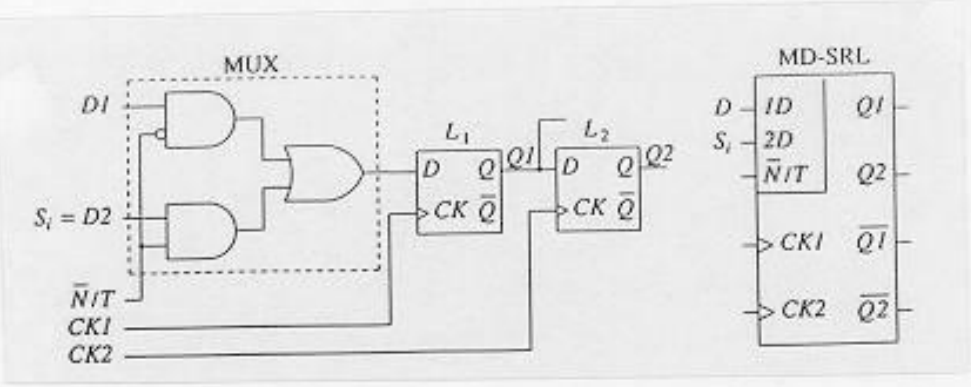
NON-SERIAL SCAN



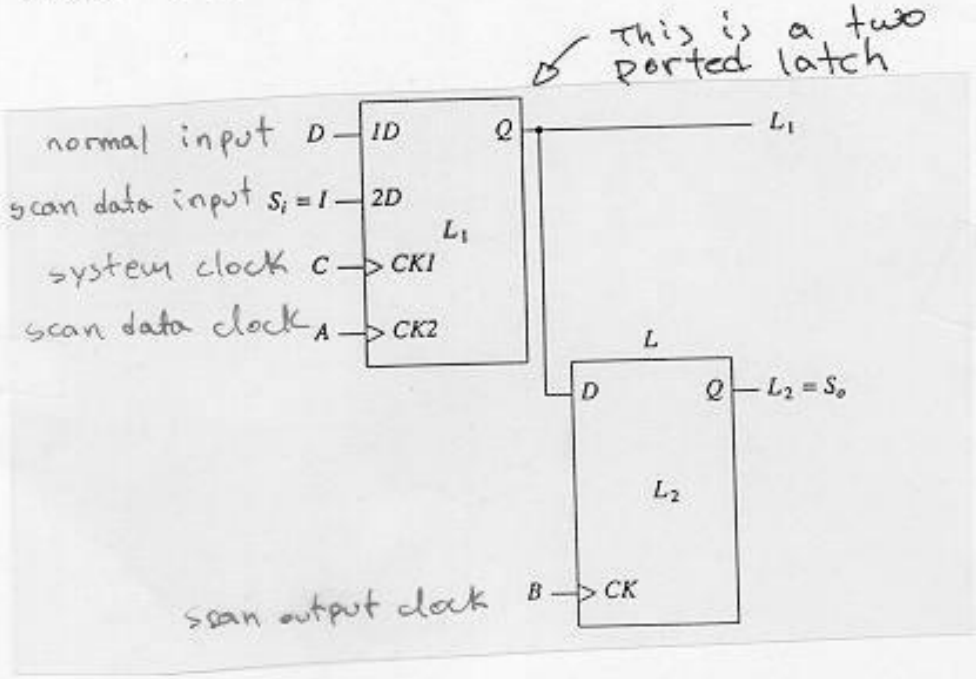
improves scan-in/scan-out time but increases hardware overhead

SCAN CELL DESIGNS

MOST OF THE TIMES IT IS USEFUL TO SEPARATE SYSTEM CLOCK FROM SCAN CLOCK:



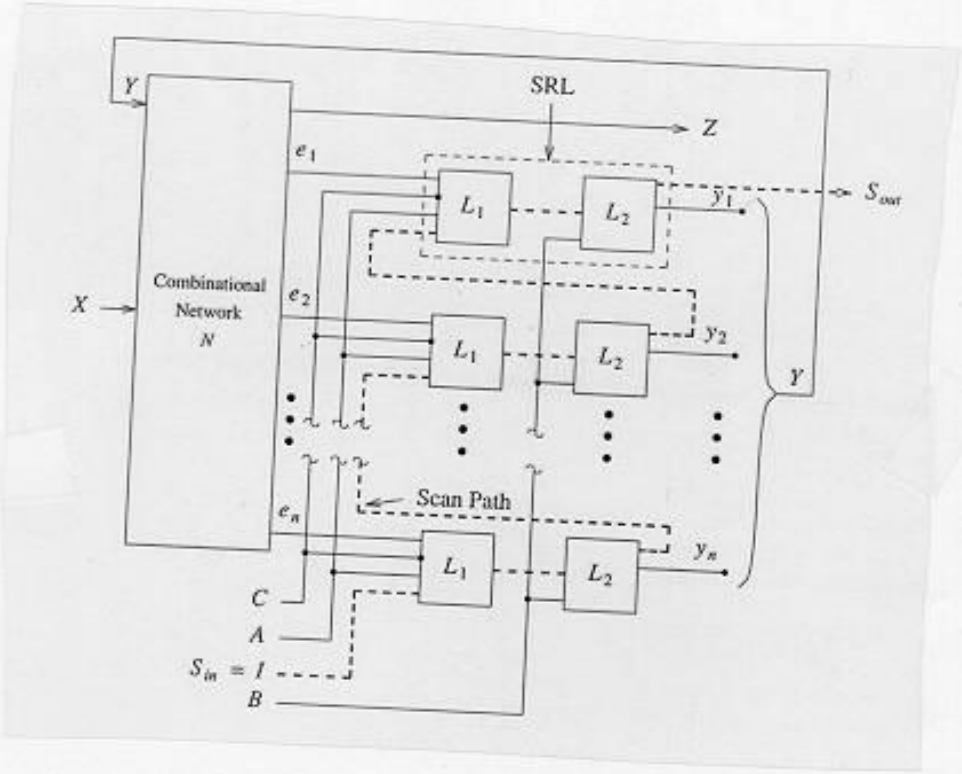
TO AVOID PERFORMANCE DEGRADATION DUE TO MUX THE FOLLOWING 2-PORT SHIFT REGISTER LATCH WAS DESIGNED BY IBM:



NOTE: ONLY C-B OR A-B CLOCKS CAN BE ENABLED AT ANY TIME!

Level Sensitive Scan Design

THE FOLLOWING DOUBLE-LATCH DESIGN USES THE DESIGN CELL DEVELOPED BY IBM AND SHOWN BEFORE.



THERE OTHER LSSD SCHEMES WITH LESS GATES, MORE CLOCKING ETC. FINAL DECISION IS BASED UPON THE # OF ADDED COMBINATIONAL LOGIC TO THE CIRCUIT (TRADE-OFF)

LSSD cont.

A SEQUENTIAL CIRCUIT IS LEVEL SENSITIVE IF ITS STEADY STATE RESPONSE TO ANY INPUT STATE CHANGE IS:

- independent of its inertial delays
- independent of the order which inputs change

IBM's DISCIPLINE ACHIEVES THIS WITH LSSD.

DESIGN RULES:

- All internal latch storage must be implemented with hazard-free latches
- The two latches in the SLR must be controlled by two non-overlapping clocks
- All (respective) clocks for the same latch in the SLR must originate from same clock source

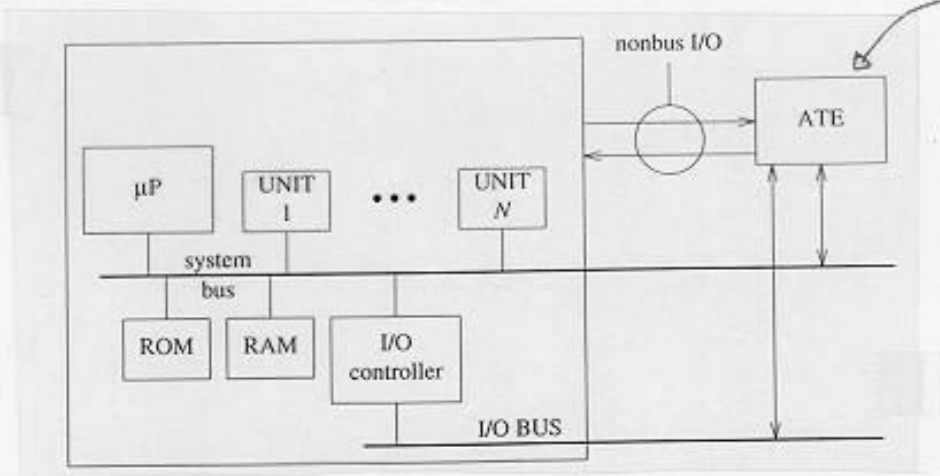
ADVANTAGES:

Design is race free, hazard immune, and LSSD is not intrusive on design process

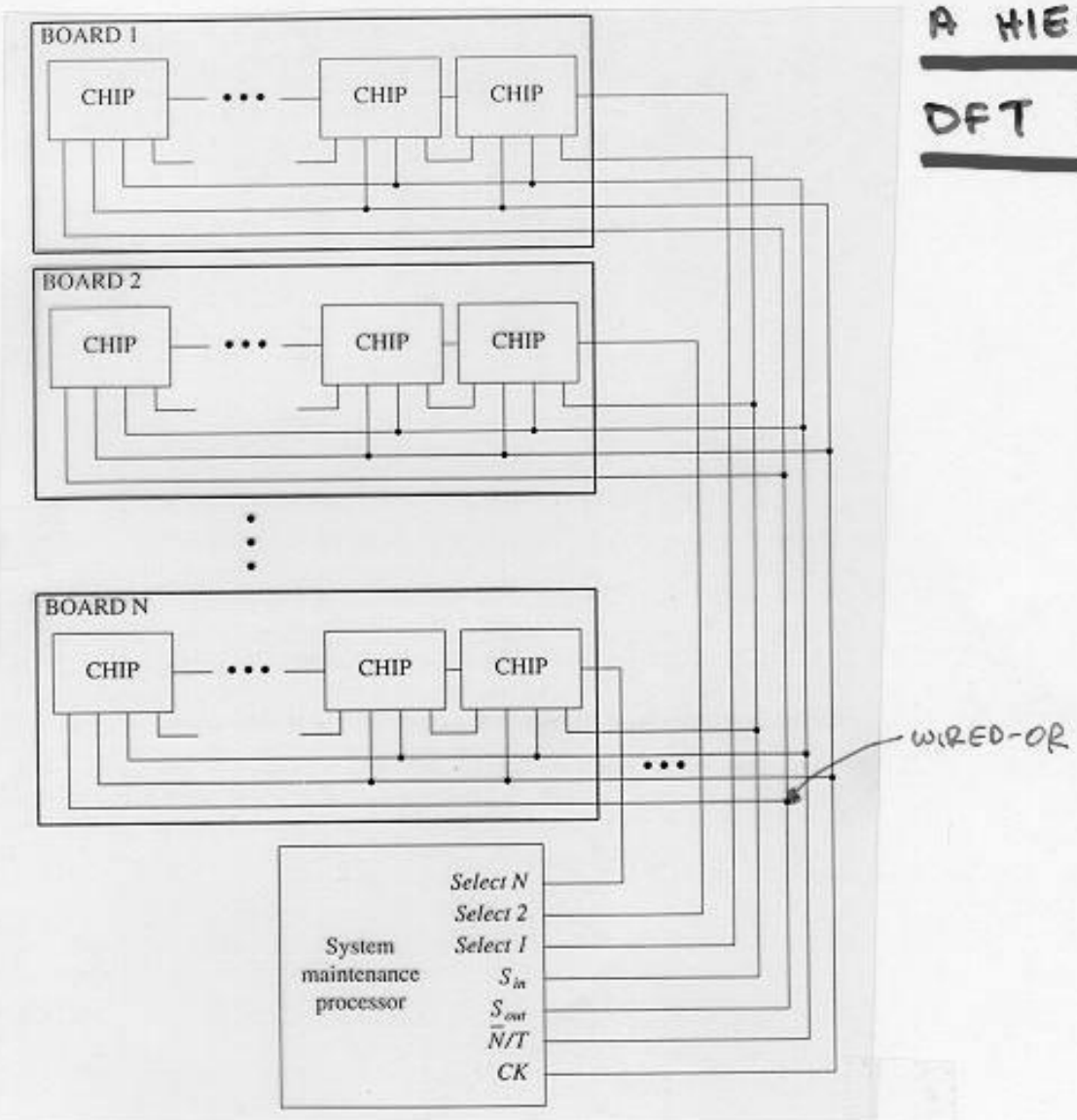
DISADVANTAGES:

Latches are complex, overhead 4-20% in chip area, introduces 4 extra I/O pins and all timing is controlled by external clocks

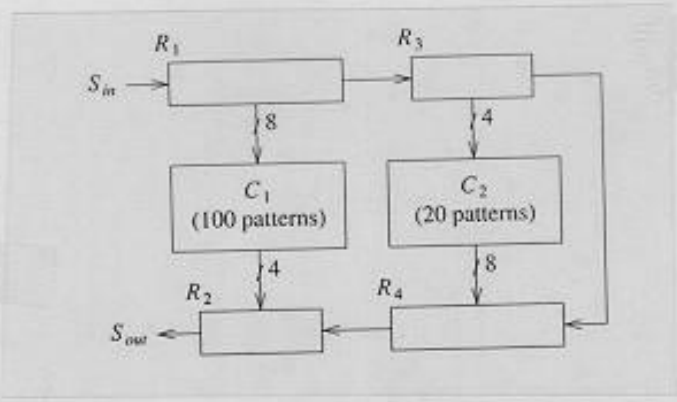
SYSTEM LEVEL TESTING



A HIERARCHICAL DFT APPROACH



MULTIPLE TEST SESSIONS



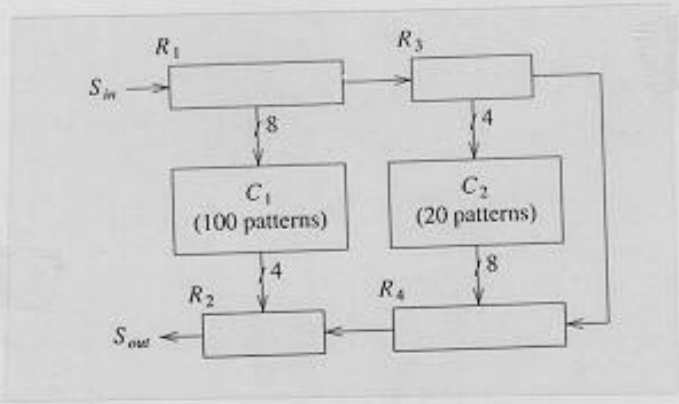
TESTING IN OVERLAPPED MODE:

Test them as partly as one block of logic and partly as separate blocks.

- Test C_1 and C_2 with 20 patterns 12 bits wide — 12 x 20 clock cycles
- Test C_1 with remaining 80 patterns each 8 bits wide — 80 x 8 clock cycles

Total: 640 clock cycles

MULTIPLE TEST SESSIONS



TESTING IN "TOGETHER MODE":

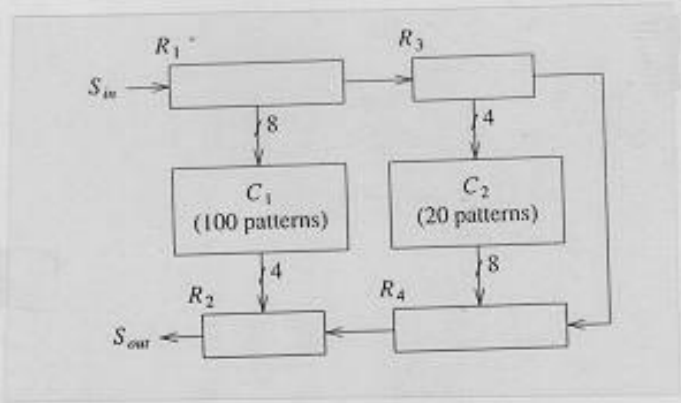
C_1 requires 100 patterns

C_2 requires 20 patterns

Total: 100 × 12 clock cycles

We ignore time to load R_2 and R_4 as well as scanning out Final result.

MULTIPLE TEST SESSIONS



TESTING IN "SEPARATE MODE":

While C_1 is tested, C_2/R_3/R_4 are ignored (and vice versa)

Testing C_1: 8×100 clock cycles

Testing C_2:

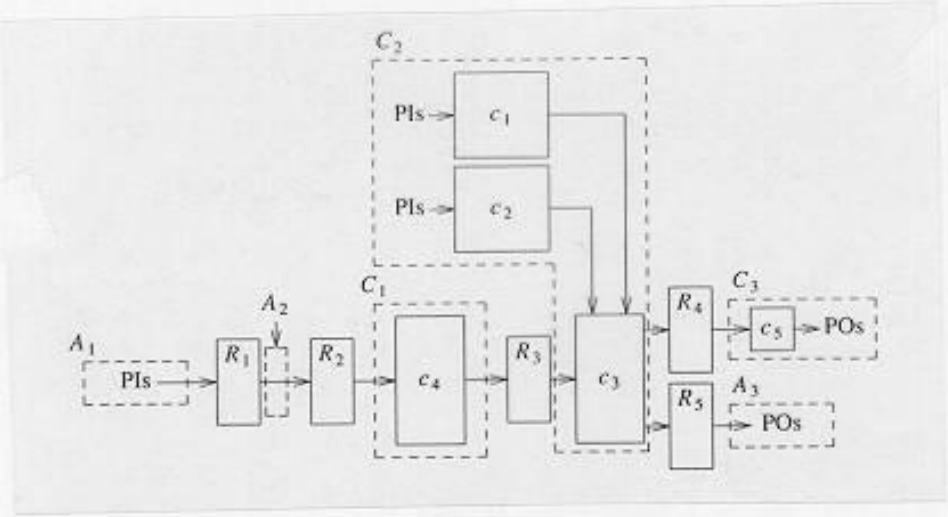
redirect R_4 to a PO and pad input test paterns with 4 don't cares

8×20 clock cycles

Total: 960 clock cycles vs. 1200 before

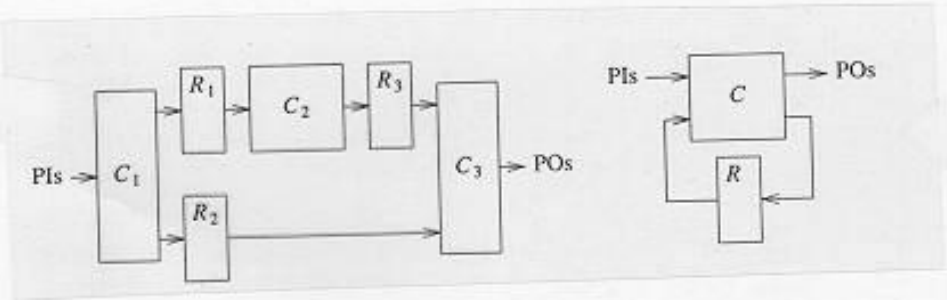
CASE STUDY: BALLAST PARTIAL SCAN

CLOUD: A MAXIMAL REGION OF COMBINATIONAL (NON-EMPTY) LOGIC



BALANCED SEQUENTIAL CIRCUIT (or B-STRUCTURE):
WHEN FOR ANY TWO CLOUDS IN THE CIRCUIT ALL SIGNAL PATHS GO THROUGH THE SAME NUMBER OF REGISTERS.

=> Circuit above is B-STRUCTURE below they're not



PROPOSITION

Any sequential circuit can be a B-STRUCTURE by replacing a set of appropriate registers into scan registers
(NP-Complete problem)

DEFINITIONS

- C_B is the combinational equivalent of B-STRUCTURE S_B when FFs are replaced by wires
- Largest # of registers on any path S_B between two clouds is depth of S_B

Let $t_1\ t_2 \dots t_n$ vectors testing C_B, where (intuitively): $t_i = t_i^{PI} + t_i^{PPI}$ → scan inputs
↳ PIs

ALGORITHM: Testing S_B (depth d)

Scan t_i^{PPI} and apply t_i^{PI}

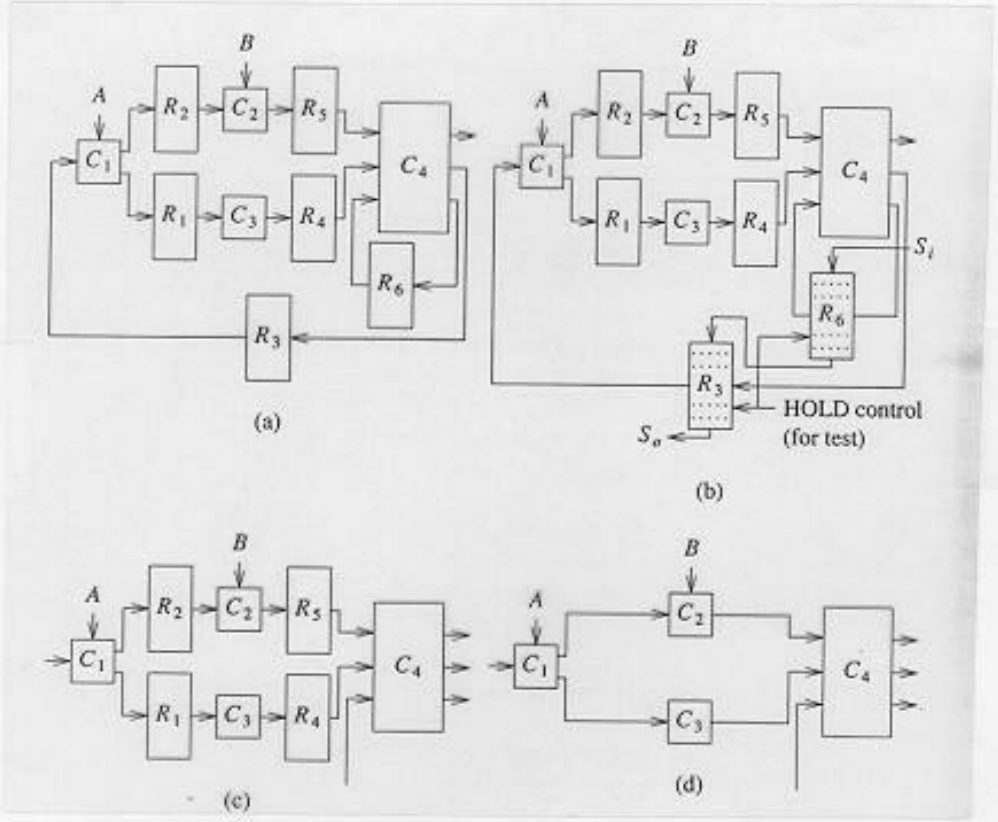
Hold values above and clock circuit d times

Place scan path in normal mode and clock it once

Observe POs

REPEAT w/ NEXT VECTOR

Ex:



(a) original circuit

(b) R_3/R_6 selected as scan registers

(c) replacing scan registers with PIs/POs

(d) C_B (depth = 2)

clock cycle 1: results at R_1/R_2

clock cycle 2: results at R_5/R_4

clock cycle 3: results at POs