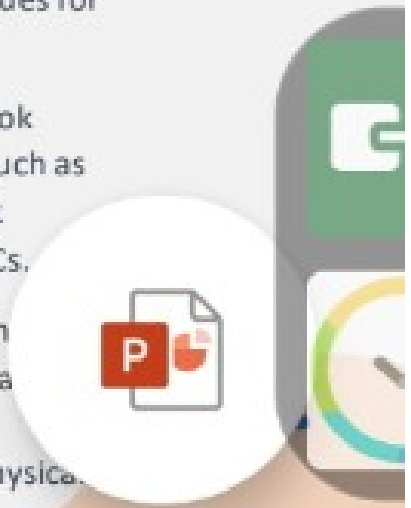
Books to be referred to become physical design engineers

1."Physical Design Essentials: An ASIC Design Implementation Perspective" by Kunal P. Ghosh and Sadiq M. Sait: This book provides a comprehensive overview of the physical design flow for ASIC (Application-Specific Integrated Circuit) implementation. It covers topics such as floorplanning, placement, clock tree synthesis, routing, and physical verification. The book explains the underlying principles of each stage and provides practical insights and techniques for achieving efficient and high-quality physical designs.

2."Physical Design for 3D Integrated Circuits" by Kuan-Neng Chen, Yao-Wen Chang, and Hung-Ming Chen: This book focuses on the physical design challenges and techniques specific to 3D integrated circuits (ICs). It covers topics such as 3D IC stacking technologies, thermal and power integrity, floorplanning, and interconnect optimization. The book provides an in-depth understanding of the unique considerations and methodologies required for designing 3D ICs.

3."Physical Design Automation of VLSI Systems" by Sachin S. Sapatnekar: This book explores the automation of ph design processes in VLSI systems. It covers topics such as floorplanning, placement, routing, clock tree synthesis, a performance optimization. The book provides insights into algorithmic techniques, optimization strategies, and challenges associated with physical design automation. It also discusses the impact of process technologies on physica design.



Books to check out for verification engineers

1."SystemVerilog for Verification: A Guide to Learning the Testbench Language Features" by Chris Spear and Greg Tumbush: This book provides a comprehensive guide to using SystemVerilog for verification. It covers the language constructs and features specific to verification, such as classes, randomization, and functional coverage. The book includes numerous examples and practical tips to help you build effective testbenches.

2."ASIC/SoC Functional Design Verification: A Comprehensive Guide to Technologies and Methodologies" by Ashok B. Mehta: This book offers a comprehensive overview of functional design verification methodologies for ASICs and SoCs (System on Chips). It covers key concepts, techniques, and methodologies used in verification, including simulation, assertions, coverage-driven verification, and formal verification. The book also discusses emerging trends and challenges in functional verification.

3."Verification Methodology Manual for SystemVerilog" by Janick Bergeron, Eduard Cerny, Alan Hunter, and Andy Nightingale: This book, commonly referred to as the "VMM book," provides a detailed explanation of the Universal Verification Methodology (UVM) based on SystemVerilog. UVM is a widely adopted methodology for verification in the industry. The book covers the principles and usage of UVM, including testbenches, sequences, and configuration objects. It also offers insights into advanced topics like constrained-random testing and functional coverage.

Online courses for physical design engineers (1)

1.Physical Design Flow" by NPTEL (National Programme on Technology Enhanced Learning): This course provides a comprehensive understanding of the physical design flow in the VLSI industry. It covers topics such as floor planning, placement, clock tree synthesis, routing, and physical verification. The course includes hands-on exercises using industry-standard tools.

2."VLSI Physical Design: From Graph Partitioning to Timing Closure" by Coursera: Offered by the University of Illinois at Urbana-Champaign, this course focuses on the entire physical design process. It covers graph partitioning, placement algorithms, clock tree synthesis, routing, and timing closure. The course includes practical assignments to reinforce the concepts.

3."Advanced VLSI Design and Physical Design" by VLSI System Design (VSD) Academy: This online course provides in-depth knowledge of advanced VLSI design and physical design techniques. It covers topics such as floor planning, placement, clock tree synthesis, routing, and optimization. The course includes hands-on labs using industry-standard EDA (Electronic Design Automation) tools.

Online courses for physical design engineers (2)

4. "ASIC Physical Design Flow and Challenges" by Udemy: This course provides a detailed overview of the physical design flow for ASIC (Application-Specific Integrated Circuit) designs. It covers various stages of physical design, including floorplanning, placement, clock tree synthesis, routing, and physical verification. The course also discusses challenges and techniques for achieving better performance and lower power consumption.

5. "Physical Design and Verification of VLSI Circuits" by NPTEL (National Programme on Technology Enhanced Learning): This course focuses on the physical design and verification aspects of VLSI circuits. It covers topics such as timing analysis, clock tree synthesis, routing, and power optimization. The course also introduces physical verification techniques to ensure the design meets the manufacturing requirements.

Books to check out for RTL designers

1."Digital Design and Computer Architecture" by David Harris and Sarah Harris: This book provides a comprehensive introduction to digital logic design and computer architecture. It covers topics such as combinational and sequential logic, datapath and control unit design, memory systems, and input/output. It also discusses various design methodologies and tools used in the industry. The book provides a solid foundation for RTL design and is widely regarded as an excellent resource for beginners.

2."RTL Hardware Design Using VHDL: Coding for Efficiency, Portability, and Scalability" by Pong P. Chu: This book focuses on using VHDL (VHSIC Hardware Description Language) for RTL design. It covers the syntax and features of VHDL and provides practical guidance on writing efficient, portable, and scalable RTL code. The book explains design methodologies, coding styles, and verification techniques. It also includes numerous examples and exercises to reinforce the concepts.

3."Digital Integrated Circuits: A Design Perspective" by Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic: This book is a comprehensive guide to digital integrated circuit design. It covers a wide range of topics, including digital design principles, CMOS technology, circuit characterization and performance estimation, timing issues, and power optimization techniques. The book provides a solid understanding of the underlying principles of digital circuits and their impact on RTL design.

Online Courses for design verification engineers (1)

1."VLSI CAD: Logic to Layout" by NPTEL (National Programme on Technology Enhanced Learning): This course provides a comprehensive overview of the entire VLSI design flow, including design verification. It covers the fundamentals of digital design, introduces verification concepts, and explores simulation and debugging techniques.

2."SystemVerilog Verification for Professionals" by Udemy: SystemVerilog is a widely used hardware description and verification language. This course focuses on SystemVerilog-based verification methodologies and covers topics such as testbench development, constrained-random testing, and functional coverage. It also introduces advanced verification concepts like assertions and UVM (Universal Verification Methodology).

3."Advanced VLSI Design and Verification" by VLSI System Design (VSD) Academy: This online course provides in-depth knowledge of advanced VLSI design and verification techniques. It covers topics such as design verification planning, functional coverage, code and functional coverage-driven verification, and assertion-based verification. The course also includes hands-on labs using industry-standard tools.

Online Courses for design verification engineers (2)

4. "UVM (Universal Verification Methodology) in SystemVerilog" by Doulos: UVM is a widely adopted verification methodology in the semiconductor industry. This course provides a comprehensive introduction to UVM and its application in SystemVerilog-based verification environments. It covers the key concepts, classes, and libraries used in UVM and demonstrates their usage through practical examples and exercises.

5. "ASIC Verification" by edX: Offered by the University of Colorado Boulder, this course covers the fundamentals of ASIC (Application-Specific Integrated Circuit) verification. It introduces verification techniques, including simulation, testbenches, and functional coverage. The course also explores advanced verification topics such as assertions, property checking, and formal verification

Roadmap to become VLSI Engineer (4)

9. Apply for Entry-Level Positions:
    1. Begin applying for entry-level positions in VLSI companies or semiconductor firms. Look for job openings for VLSI design engineers, physical design engineers, or verification engineers. Highlight your education, practical experience, and project portfolio in your resume and cover letter. Leverage your network and connections made during your networking efforts.
10. Continue Learning and Growing:

    Once you enter the VLSI industry, continue learning and expanding your skill set. Gain experience by working on diverse projects and collaborating with experienced professionals. Pursue professional certifications or specialized training courses to enhance your expertise in specific areas of VLSI.

RTL design engineer courses (1)

1."VLSI CAD: Logic to Layout" by NPTEL (National Programme on Technology Enhanced Learning): This course provides a comprehensive overview of the entire VLSI design flow, including RTL design, logic synthesis, and physical design. It covers essential concepts and techniques used in RTL design and introduces tools such as Verilog HDL and Synopsys Design Compiler.

2."Digital Integrated Circuit Design" by edX: Offered by Purdue University, this course covers digital circuit design at the transistor level. It delves into RTL design principles, timing analysis, and introduces concepts such as finite state machines and Datapath design.

3."Verilog for Beginners" by Udemy: This course focuses on Verilog HDL, which is widely used for RTL design. It covers the basics of Verilog syntax, modeling digital circuits, and designing RTL components.

RTL design engineer courses (2)

4. "System Verilog Verification for Professionals" by Udemy: Verification is an essential aspect of RTL design. This course teaches System Verilog, a hardware description and verification language. It covers testbench development, functional verification techniques, and advanced verification concepts.

5. "ASIC/FPGA Design and Verification: A Start-Up Guide" by Coursera: This course introduces ASIC (Application-Specific Integrated Circuit) and FPGA (Field-Programmable Gate Array) design. It covers RTL design, simulation, synthesis, and verification methodologies.

6. "Introduction to Digital Systems Design" by Coursera: This course, offered by the University of Illinois at Urbana-Champaign, introduces the fundamentals of digital systems design. It covers topics such as combinational and sequential logic design, Verilog HDL, and FPGA implementation.

Roadmap to become VLSI Engineer (1)

1.Acquire a Strong Educational Foundation:

1. Obtain a bachelor's degree in electrical engineering, electronics engineering, or a related field. This will provide you with a solid understanding of the fundamental principles of electronics and digital design.

2.Focus on VLSI Coursework:

1. During your undergraduate studies, take elective courses or specialized modules that cover topics specific to VLSI design, such as digital systems design, semiconductor devices, integrated circuit design, and computer architecture.

3.Gain Hands-on Experience:

1. Seek out internships or co-op positions at VLSI companies or research institutions. This will give you practical exposure to the industry and an opportunity to work on real-world VLSI projects. Apply your theoretical knowledge to solve problems and gain valuable insights into the design process.

Roadmap to become VLSI Engineer (2)

4. Pursue Advanced Education (optional):

1. Consider pursuing a master's degree or Ph.D. in VLSI design, microelectronics, or a related field. Advanced degrees can enhance your knowledge and make you a more competitive candidate for positions in the industry. Engage in research projects and collaborations with professors or industry experts to gain further expertise.

5. Develop Proficiency in Industry Tools:

1. Familiarize yourself with industry-standard tools used in VLSI design, such as Cadence, Synopsys, Mentor Graphics, and Xilinx. These tools are commonly used for designing, simulating, and verifying integrated circuits. Practice using them through academic projects, internships, or personal projects.

6.Build a Portfolio of Projects:

1. Create a portfolio showcasing your VLSI design projects. This can include designs you worked on during your coursework, internships, or personal projects. Highlight your role, design challenges, and outcomes achieved. A strong portfolio will demonstrate your practical skills and problem-solving abilities.

Roadmap to become VLSI Engineer (3)

7. Network and Connect with Professionals:

1. Attend VLSI conferences, workshops, and industry events to network with professionals in the field. Join online forums, LinkedIn groups, and social media communities focused on VLSI. Engage in discussions, seek guidance, and learn from experienced practitioners. Building a network can lead to job opportunities and valuable connections.

8. Stay Updated on Industry Trends:

1. The field of VLSI is rapidly evolving, with new technologies, methodologies, and design techniques emerging regularly. Stay updated on the latest trends, research papers, and industry developments through publications, conferences, webinars, and online resources. Continuous learning will keep your skills relevant and marketable.

CAD Engineer

1.CAD (Computer-Aided Design) Engineer:

1. Job Description: Developing and maintaining EDA tools and software used in VLSI design, including design automation, simulation, and analysis tools.
2. Key Skills: Proficiency in programming languages (such as C++ or Python), understanding of algorithms and data structures, knowledge of EDA tool flows and software development methodologies.

DFT Engineer

DFT (Design for Testability) Engineer:

•**Job Description:** Designing integrated circuits with testability features to ensure efficient testing and diagnosis during the manufacturing process.

•**Key Skills:** Knowledge of DFT techniques (such as scan chains, test compression, and boundary scan), understanding of fault models and testability metrics, familiarity with ATPG (Automatic Test Pattern Generation) tools

Resources:

1.DFT Techniques and Methodologies:

1. **Online Courses:**
    1. "Digital VLSI Testing" by NPTEL on SWAYAM platform
2. **Books:**
    1. "Testing of Digital Systems" by Kamran Eshraghian and Eshraghian Dijiang

2.EDA Tools:

1. Most EDA tool vendors provide documentation, tutorials, and user guides for their tools. Visit the websites of Synopsys, Mentor Graphics, and Cadence to access their resources.
2. Tool-specific training courses or workshops conducted by EDA tool vendors or authorized training providers can be beneficial.

Post Silicon Validation engineer

•Develops and executes validation plans for integrated circuits (ICs) after manufacturing.

•Conducts functional and performance testing to ensure ICs meet design specifications.

•Analyzes and debugs issues to identify root causes and provides solutions.

•Collaborates with design, DFT, and manufacturing teams to ensure successful product validation.

•Validates and verifies ICs in real-world environments to ensure reliability and functionality.

1.Books:

1. "Post-Silicon Validation for Modern VLSI Systems" by Laung-Terng Wang
2. "Validation of Communications Systems with SDL: The Art of SDL Simulation and Reachability Analysis" by Elvira Albert, Albert Benveniste, and Klaus-Dieter Schewe

2.Online Courses:

1. "VLSI CAD: Logic to Layout" by NPTEL on SWAYAM platform
2. "Introduction to VLSI Systems" by Udemy

3.EDA Tools:

1. Familiarize yourself with industry-standard EDA tools used for post silicon validation, such as simulation tools (ModelSim, VCS), hardware debuggers (JTAG-based debuggers), and scripting languages (Perl, Python).

Analog design engineer

1.Analog/Mixed-Signal Design Engineer:

1. **Job Description:** Designing analog and mixed-signal circuits for integrated systems, including amplifiers, filters, and analog-to-digital converters.
2. **Key Skills:** Strong understanding of analog circuit design principles, proficiency in using CAD tools for analog design, knowledge of circuit simulation and layout techniques, familiarity with industry-standard specifications (such as IEEE).
3. Resources to Learn:
    1. **Online Courses:**
        1. "Introduction to VLSI Systems" by NPTEL on SWAYAM platform
        2. "Analog IC Design" by NPTEL on SWAYAM platform
    2. **Books:**
        1. "Analysis and Design of Analog Integrated Circuits" by Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer
        2. "CMOS Analog Circuit Design" by Phillip E. Allen and Douglas R. Holberg

Analog Layout engineer

1.Analog Layout Engineer:

1. Job Description: Creating the physical layout of analog and mixed-signal circuits, including transistor-level design and layout optimization.
2. Key Skills: Proficiency in analog layout tools (such as Cadence Virtuoso), knowledge of layout techniques for analog circuits, understanding of IC fabrication processes and design rules.

Verification Engineer

1.Verification Engineer:

1. **Job Description:** Ensuring the correctness and functionality of integrated circuits by designing and executing verification tests.
2. **Key Skills**: Proficiency in verification methodologies (such as SystemVerilog or UVM), understanding of digital design principles, familiarity with simulation and debugging tools, knowledge of scripting languages.
3. Resources to Learn:
    1. **Online Courses:**
        1. "Digital VLSI Verification Fundamentals" by NPTEL on SWAYAM platform
        2. "VLSI CAD: Logic Verification" by NPTEL on SWAYAM platform
    2. **Books:**
        1. "SystemVerilog for Verification: A Guide to Learning the Testbench Language Features" by Chris Spear and Greg Tumbush
        2. "UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology" by Ray Salemi

LET'S DISCUSS More on the Roles in the VLSI industry

VLSI Design Engineer

1.VLSI Design Engineer:

1. Job Description: Designing and implementing integrated circuits (ICs) and digital systems using hardware description languages (HDLs) and CAD tools.
2. Key Skills: Strong understanding of digital logic design, proficiency in HDLs (such as Verilog or VHDL), knowledge of ASIC or FPGA design flow, familiarity with EDA (Electronic Design Automation) tools.
3. Resources to Learn:
    1. Online Courses:
        1. "VLSI CAD: Logic to Layout" by NPTEL on SWAYAM platform
        2. "Digital VLSI Design with Verilog" by Coursera/University of Illinois
    2. Books:
        1. "Digital Design and Computer Architecture" by David Harris and Sarah Harris
        2. "ASIC/SoC Functional Design Verification" by Ashok B. Mehta

Physical design engineer

1.Physical Design Engineer:

1. **Job Description:** Implementing the physical layout of integrated circuits, including floor planning, placement, and routing.
2. **Key Skills:** Strong knowledge of physical design concepts, proficiency in using EDA tools (like Cadence or Synopsys), understanding of IC fabrication processes, familiarity with scripting languages (e.g., TCL, Perl, Python).
3. Resources to Learn:
    1. **Online Courses:**
        1. "VLSI Physical Design: From Graph Partitioning to Placement" by NPTEL on SWAYAM platform
        2. "VLSI CAD: Placement and Routing" by NPTEL on SWAYAM platform
    2. **Books:**
        1. "Physical Design Essentials" by B. Saravanan and S. Srinivasan
        2. "VLSI Physical Design Automation: Theory and Practice" by Sadiq M. Sait and Habib Youssef

12. Manufacturing and testing

- The semiconductor foundry fabricates the ASIC based on the provided design data.
- Conduct post-fabrication testing and characterization to validate the functionality and performance of the chip.

Roles in Industry with respect to Design specification in ASIC Design Flow:

- **Manufacturing Engineer:** Oversees the fabrication process at the semiconductor foundry.
- **Test Engineer:** Conducts post-fabrication testing and characterization to validate the functionality and performance of the ASIC

FPGA Design Flow and Roles in the industry at each step

FPGA VS ASIC

Functionality	ASIC	FPGA
Placing	In ASIC design, placement refers to the process of determining the physical location of logical elements (gates, standard cells, macros, etc.) on the chip. It involves optimizing for power, timing, and area constraints, as well as considerations like signal integrity and manufacturability. Placement is typically performed using advanced place-and-route tools that consider the entire chip's floorplan.	In FPGA design, placement refers to the process of mapping the logical elements (LUTs, flip-flops, etc.) of the design onto specific locations within the FPGA's programmable fabric. While placement is also important for optimizing timing, power, and area, it is more constrained by the fixed resources available in the FPGA. The placement step in FPGA design is often performed by the FPGA synthesis tool.
Routing	ASIC Design: In ASIC design, routing refers to the process of creating the physical connections (metal routing tracks) between the placed logical elements. It involves determining the optimal path for each signal and addressing challenges such as signal integrity, congestion, and timing closure. Complex algorithms are used to find the best routing solutions, and the process is typically performed with specialized tools.	FPGA Design: In FPGA design, routing refers to the process of configuring the interconnections between the placed logical elements using the programmable routing resources within the FPGA. The FPGA's programmable routing fabric allows for flexible interconnection between different parts of the design. The routing is performed by the FPGA synthesis tool during the place-and-route process.
Flexibility	ASIC Design: In ASIC design, the placement and routing steps are tightly integrated into the overall physical design flow and are optimized specifically for the target chip. The placement	FPGA Design: In FPGA design, the placement and routing steps are part of the design flow but are more flexible. Since FPGAs are reprogrammable devices, the placement and routing can be

8. Routing

- Connect the placed cells using metal routing tracks to establish interconnections.
- Optimize the routing for signal integrity, timing, and manufacturability.
- Perform design rule checks (DRC) to ensure compliance with manufacturing constraints.

Roles in Industry with respect to Design specification in ASIC Design Flow:

- **Physical Design Engineer:** *Handles the routing of interconnections, optimizing for signal integrity, timing, and manufacturability.*

9. Physical verification

- Conduct a series of checks to ensure the correctness and integrity of the physical design.
- Perform DRC to verify that the layout meets the manufacturing rules.
- Run layout versus schematic (LVS) checks to ensure the consistency between the layout and the netlist.

Roles in Industry with respect to Design specification in ASIC Design Flow:

- **Physical Verification Engineer:** *Conducts various checks to ensure the correctness and integrity of the physical design. Performs Design Rule Checks (DRC) and Layout versus Schematic (LVS) checks.*

10. Design for Testability

- Perform additional checks to enhance the manufacturability of the design.
- Optimize the layout for yield, reliability, and process variations.
- Address any identified design issues or violations.

Roles in Industry with respect to Design specification in ASIC Design Flow:

- **Design for Testability:**
- *DFT Engineers work on integrating testability features into the design, including test access mechanisms, built-in self-test (BIST) circuits, scan chains, and boundary scan (JTAG) logic.*
- *They also define the test architecture, test modes, and test patterns that will be used to validate the functionality and performance of the ASIC*

5. Design Synthesis

- Convert the RTL description into a gate-level representation using a synthesis tool.
- Perform logic optimization, mapping the design to a library of standard cells.
- Generate a netlist, which represents the design in terms of gates and their interconnections.

Roles in Industry with respect to Design specification in ASIC Design Flow:

- **RTL Design Engineer:** *Ensures that the RTL code is synthesizable and optimized for synthesis.*
- **Synthesis Engineer:** *Uses a synthesis tool to convert the RTL description into a gate-level representation. Performs logic optimization and mapping to a library of standard cells.*

6. Design Optimization

- Fine-tune the design for area, power, and timing optimization.
- Analyze and optimize critical paths to meet the desired performance.
- Perform floor planning to determine the optimal placement of major design blocks.

Roles in Industry with respect to Design specification in ASIC Design Flow:

- **Design Engineer:** *Analyzes the synthesized design, identifies critical paths, and optimizes the design for area, power, and timing.*
- **Timing Engineer:** *Works on timing closure, ensuring that the design meets the required timing constraints.*

7. Physical design

- Perform detailed placement of cells in the chip layout.
- Optimize the placement for power, timing, and signal integrity.
- Conduct clock tree synthesis to distribute clock signals efficiently.

Roles in Industry with respect to Design specification in ASIC Design Flow:

- **Physical Design Engineer:**
- *Performs detailed placement of cells, floor planning, and power distribution network design.*
- *Conducts the placement and routing of cells, optimizing for area, power, timing, signal integrity, and manufacturability.*
- *Designs and optimizes the clock tree to ensure proper clock*

2. Architectural design

- Develop a high-level architecture of the ASIC, including major functional blocks and their interconnections.
- Explore different design options and trade-offs to meet the requirements.
- Perform feasibility analysis and select the most suitable architecture.

Roles in Industry with respect to Design specification in ASIC Design Flow:

- **System Architect:** *Develops the high-level architecture, identifies major functional blocks, and defines the overall system behavior.*
- **Design Engineer:** *Works with the system architect to refine the architectural design, explore design options, and perform feasibility analysis.*

3. RTL Design

- Create the Register Transfer Level (RTL) description of the ASIC using a hardware description language (HDL) like Verilog or VHDL.
- Define the functionality, data paths, control structures, and interfaces at a lower level of abstraction.

Roles in Industry with respect to Design specification in ASIC Design Flow:

- **RTL Design Engineer:** *Converts the architectural design into a Register Transfer Level (RTL) description using HDLs like Verilog or VHDL. Defines the functionality, data paths, control structures, and interfaces at a lower level of abstraction.*

4. Functional verification

- Develop a testbench to verify the correctness of the RTL design.
- Write test cases and generate stimulus to exercise the design.
- Simulate the design and compare the results with the expected behavior.

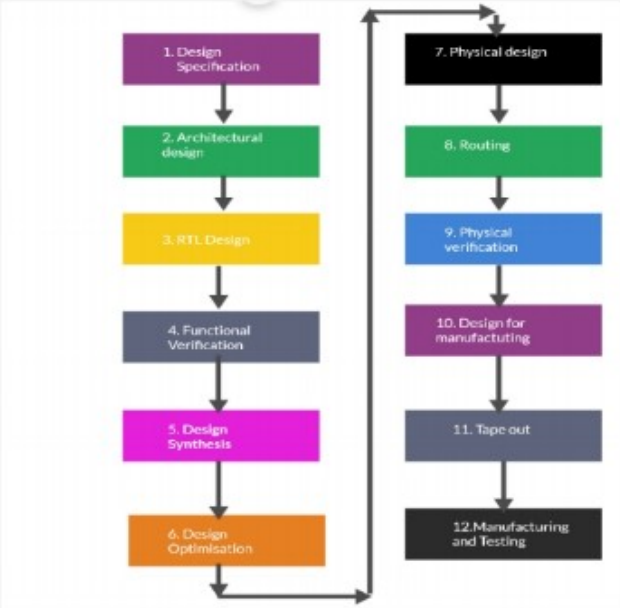
Roles in Industry with respect to Design specification in ASIC Design Flow:

- **Verification Engineer:** *Develops the verification plan, writes test cases, and creates the testbench. Performs simulation and debugging to ensure the correctness and functional completeness of the RTL design.*

Silicon Community - Session 0- ASIC/FPGA Design Flow. Roadmap to Semiconductor industry

Varun Kouda

ASIC design Flow and roles in the industry in each step



1. Design Specification

- Define the functional and performance requirements of the ASIC based on the application it will be used for.
- Determine the key specifications such as power consumption, speed, size, and cost.

Roles in Industry with respect to Design specification in ASIC Design Flow:

- **System Architect:** *Defines the high-level requirements and functional specifications of the ASIC based on the application requirements and customer needs.*