SpyGlass® 4.7.1 Release Notes

This *Release Notes* document highlights new features and enhancements made in the SpyGlass 4.7.1 release. This release supersedes all the prior SpyGlass releases. This document contains the following topics:

Atrenta® Legacy Support Policy

Our policy is to support the current and two prior major releases of the software. For example, with the 4.7.0 release, support for releases prior to 4.5.0 of the SpyGlass platform ceases. For details on our legacy support policy, please refer to the Support page of our website.

If one of your installations is still using an un-supported release, please contact Atrenta support or your local salesperson. We will work with you to develop a plan to continue support of that release until you are able to move to a supported release.

Our intention in supporting this policy is to improve the quality of our service by allowing our team to focus on current release optimization. While moving to this process, we do not want to create undue hardship for you. Contact us soon so that we may develop a support plan that meets your needs.

Thank you for your cooperation and understanding.

Best Regards,

The Atrenta Team

Platform Support

Rule-Checking

SpyGlass 4.7.1 was developed and tested on the following platforms:

Hardware Platform	Compiled and tested on...	Also tested on...
Intel x86 (32 bit)	RHEL 4.0	RHEL 4.8, RHEL 5.2, RHEL 5.6, RHEL 6.0, SUSE 10 SP2, SUSE 11 SP1, CENTOS 5.4
AMD Opteron (32/64-bit)	RHEL 4.0	RHEL 4.8, RHEL 5.2, RHEL 5.6, RHEL 6.0, SUSE 10 SP2, SUSE 11 SP1, CENTOS 5.4
Intel Xeon/EMT64 (64-bit)	-	RHEL 4.8, RHEL 5.2, RHEL 5.6, RHEL 6.0, SUSE 10 SP2, SUSE 11 SP1, CENTOS 5.4

NOTE: *On the Linux 64-bit platform, 64-bit SpyGlass binaries are executed by default. To enforce 32-bit binary execution, use the* `-32bit` *command-line option except on the RHEL 6.0 platform. The* `-32bit` *command-line option does not work on the default 64-bit installation of the RHEL 6.0 platform because the required 32-bit libraries are not installed on the 64-bit installation.*

NOTE: *For best results while using the Graphical User Interface (GUI), it is recommended to use 16-bit color depth and a minimum resolution of 1024x768.*

Custom Product Building

For SpyGlass 4.7.1 custom product development, compile custom products on the following platforms:

Hardware Platform	To use on	Compile on	Additional spygenlib Command-line Option required
Intel IA (32 bit)	RHEL 4.0, RHEL 5.0, SLES 9.0, SLES 10.0	RHEL 4.0	
AMD Opteron (64 bit)	RHEL 4.0, RHEL 5.0, SLES 9.0, SLES 10.0	RHEL 4.0	-64bit
Intel Xeon/EMT64 (64-bit)	RHEL 4.0, RHEL 5.0, SLES 9.0, SLES 10.0	-	-64bit

NOTE: *SpyGlass 3.8.x and later versions are not available on the HPUX platform.*

NOTE: *For Linux 32-bit and Linux 64-bit platforms, the compiler version is gcc 4.2.4.*

NOTE: *For Solaris 32-bit and Solaris 64-bit platforms, the compiler version is Sun Studio 11.*

Supported Platforms

The details of the supported platforms are described below:

- The following table defines the supported platforms for Atrenta license servers in 2007-June 2010 (SpyGlass 3.8.x, 3.9.x, 4.0.x, 4.1.x, 4.2.x, 4.3.x) - Flexlm version 9.5:

Hardware Platform	Baseline support (compiled & tested on)	Also supported (tested on)
Sun Sparc (32 bit and 64 bit)	Solaris 8	Solaris 9, Solaris 10
Intel x86 (32 bit)	RHEL 4.0	RHEL 5.0 SLES 9.0, 10.0

Hardware Platform	Baseline support (compiled & tested on)	Also supported (tested on)
AMD Opteron (32/64 bit)	RHEL 4.0	RHEL 5.0 SLES 9.0, 10.0
Intel Xeon/EMT64 (64-bit)	-	RHEL 4.0, 5.0 SLES 9.0, 10.0

- The following table defines the supported platforms for Atrenta license servers starting July 2010 (SpyGlass 4.4.0 onwards) - Flexlm version 11.7:

Hardware Platform	Baseline support (compiled & tested on)	Also supported (tested on)
Sun Sparc (32 bit and 64 bit)	Solaris 10.0	Solaris 9, Solaris 10
Intel x86 (32 bit)	RHEL 4.0 (Update 2)	RHEL 5.0, 5.1, 5.2, 5.3, 5.4 SLES 10.0, 10.0-SP3
AMD Opteron (32/64 bit)	RHEL 4.0 (Update 2)	RHEL 5.0, 5.1, 5.2, 5.3, 5.4 SLES 10.0, 10.0-SP3
Intel Xeon/EMT64 (64-bit)	-	RHEL 4.0 (Update 2), 5.0, 5.1, 5.2, 5.3, 5.4 SLES 10.0, 10.0-SP3

- The following table defines the supported platforms for Atrenta license servers starting July 2012 (SpyGlass 4.7.1 onwards) - Flexlm version 11.10:

Hardware Platform	Baseline support (compiled & tested on)	Also supported (tested on)
Sun Sparc (32 bit and 64 bit)	Solaris 10.0	Solaris 9, Solaris 10
Intel x86 (32 bit)	RHEL 4.0	RHEL 4.8, RHEL 5.2, RHEL 5.6, RHEL 6.0, SUSE 10 SP2, SUSE 11 SP1, CENTOS 5.4
AMD Opteron (32/64-bit)	RHEL 4.0	RHEL 4.8, RHEL 5.2, RHEL 5.6, RHEL 6.0, SUSE 10 SP2, SUSE 11 SP1, CENTOS 5.4
Intel Xeon/EMT64 (64-bit)	-	RHEL 4.8, RHEL 5.2, RHEL 5.6, RHEL 6.0, SUSE 10 SP2, SUSE 11 SP1, CENTOS 5.4

Licenses

Starting with the SpyGlass 4.7.1 release, Atrenta has upgraded to FlexNet Publisher version 11.10 from Flexera Inc.

To successfully check out licenses in the SpyGlass 4.7.1 release (or later), users must restart the license server by using a higher version of lmgrd (version 11.10 or higher) and Atrenta vendor daemon file (version 11.10). This is a one time activity.

All the license server utility files and Atrenta vendor daemon files for the 11.10 version are present under the SpyGlass installation directory, SpyGlass-4.7.1/SPYGLASS_HOME/flexlm_v1110/<platform>.

Users must set the license environment variable `ATRENTA_LICENSE_FILE` or `LM_LICENSE_FILE` in the **port@server** format rather than the file name format.

Re-compilation Requirements

When a new SpyGlass version is released with new features and enhancements, some user components need to be re-compiled to take advantage of the new features.

This section describes different user components and need to re-compile, if any.

VHDL Libraries

Pre-compiling VHDL libraries is a standard feature.

Normally, you do not need to re-compile the VHDL libraries when the object model format or the dump location has not changed. When the object model format is changed, SpyGlass prompts you to re-compile based on the internally maintained magic number.

Need to Recompile

VHDL libraries compiled with previous versions of SpyGlass are not compatible with this version of SpyGlass. Therefore, the user should recompile their libraries.

Verilog Libraries

SpyGlass provides the facility to precompile Verilog libraries and use them just like precompiled VHDL libraries (standard feature).

Normally, you do not need to re-compile the Verilog libraries when the object model format or the dump location has not changed. When the object model format is changed, SpyGlass prompts the user to re-compile based on the internally maintained magic number.

Need to Recompile

Verilog libraries compiled with previous versions of SpyGlass are not compatible with this version of SpyGlass. Therefore, the user should

recompile their libraries.

SpyGlass-format Gate Libraries

SpyGlass format gate libraries (.sglib files) are created by pre-compiling Synopsys Libraries (.lib files) by using SpyGlass Library Compiler (SpyGlass library compiler). The SpyGlass Library Compiler is enhanced with every release to support more gate cell types and/or enhanced to improve working of already supported gate cell types.

Need to Recompile

Working with Libraries Compiled Prior to 4.2.0 Release

Such libraries are compatible across releases. However, it is always recommended to recompile them using the latest SpyGlass library compiler for the following reasons.

- Netlist models of library cells that are stored in the sglib are optimized in every release. Therefore, using an optimized netlist of library cells will show improvements in SpyGlass runtime.
- The loading process of sglibs was greatly improved in the SpyGlass 4.2.0 release. However, an sglib that is compiled prior to the 4.2.0 release takes much longer to load as compared with an sglib compiled with the 4.2.0 or post 4.2.0 release.

Gate libraries compiled prior to 4.2.0 used to store the original .lib itself in an encrypted format, which was parsed again during usage. Therefore, it was compatible across releases. However, re-parsing resulted in significant .sglib load time, which has been improved starting from the 4.2.0 release.

Working with Libraries Compiled with the 4.2.0 and Post 4.2.0 Release

The SpyGlass library compiler flow was completely overhauled in the 4.2.0 release, and instead of storing .lib files in an encrypted format, SpyGlass started storing the .lib object model in a binary format. This significantly improved the .sglib load time, but this has required the need for re-compilation with every release.

Starting with SpyGlass 4.6.0, backward compatibility support for sglibs has been added. This means it is not mandatory (although it is still highly recommended) that you recompile incompatible sglibs.

In the backward compatibility mode, SpyGlass re-parses encrypted .lib files stored in sglib. This results in a higher load time of libraries as compared to reading the .lib object model in a binary format. Therefore, for better performance, it is always recommended to recompile sglibs with the latest SpyGlass library compiler release.

NOTE: *Please note the following points:*

- In backward compatibility mode, SpyGlass supports mixing of .sglib files compiled with pre SpyGlass 4.2.0 releases and .sglib files compiled with the SpyGlass 4.2.0 and post SpyGlass 4.2.0 releases.

  In such case, SpyGlass reports a message on screen describing the mixing of sglib information.

- The spyglass_reports/SpyGlass/sglib_version_summary.rpt has been improved in SpyGlass 4.6.0 to provide detailed information about the following:

  - An sglib name, the SpyGlass library compiler version used to create the given .sglib file, and status of sglib. This status helps a user to decide whether recompilation is necessary or not.
  - A series of major enhancements and other changes made in the SpyGlass library compiler from the given .sglib version to the required SpyGlass library compiler version.

If any of these features and enhancements (missing in the existing .sglib files) is relevant for your run, recompile the .lib files by using the required SpyGlass library compiler version.

You can also view the spyglass_reports/SpyGlass/sglib_version_summary.rpt report in GUI by clicking the *ReportSglibVersionSummary* rule message.

From SpyGlass 4.6.0 onward, this version summary report will always be generated whenever an sglib is specified. Prior to SpyGlass 4.6.0, this report was generated only when the `-enable_sglib_debug` command was specified.

Custom Product Shared Objects

Custom product shared objects (.spyso files) remain compatible across SpyGlass releases.

Need to Recompile

You need to re-compile the custom product shared objects in the following cases:

- The source code itself has changed (change in rule design, use of new API functions, etc.)
- The supported compiler has changed (only for C++-based rule primitives).

Future Support Notices

This section outlines planned changes in future releases. Please contact support@atrenta.com if these plans might negatively impact your usage of SpyGlass.

End of Life Announcement - 32-bit Linux Support

As is a standard industry practice, Atrenta retires older software from time to time in order to improve our focus on newer and better products. This focus will help us to continue to deliver best-in-class, cutting-edge technology for you. To facilitate this process, we are announcing an end-of-life (EOL) plan for 32-bit Linux support.

The EOL period will continue for 14 months from the release date of SpyGlass 4.7.1. The details of our EOL policy may be found at:

http://www.atrenta.com/support/support-policies/atrenta-end-of-life-%28eol%29-process.htm5

We believe the usage for this capability is extremely low. Because of this, SpyGlass 4.7.1 will be the last release that will contain 32-bit support in the standard release tree. We will still fix bugs for the software using our standard EOL policy, but if you require 32-bit software releases beyond SpyGlass 4.7.1, contact your local Atrenta sales person to make a special request.

Rules to be Deprecated

- The following rules will be removed in future SpyGlass releases:

Rule name	Future Release	Reason for removal	Replacement Rule (if any)
W34	-	The problem reported by this rule can be handled by most of the commercial compilers.	None
W256	-	The functionality of this rule is covered by the STX_VE_1366 rule.	STX_VE_1366

Rule name	Future Release	Reason for removal	Replacement Rule (if any)
ELAB_3516	-		None
LPPLIB11	-	Functionality of this rule is covered by the LPPLIB06 and LPSVM53 rules	LPPLIB06 and LPSVM53
LPPLIB10	-	Functionality of this rule is covered by the LPPLIB06 rule	LPPLIB06
LPPLIB05	-	Functionality of this rule is covered by the LPSVM04 rule	LPSVM04
V2KConstruct-ML	-	By default, Verilog 2000 is supported in SpyGlass.	None
SDC_MergeBlocks	-		None
PEPWR04	5.0	Functionality of this rule is covered by the PEPWR21 rule	PEPWR21
PEPWR15	5.0	Functionality of this rule is covered by the PEPWR20 rule	PEPWR20
PEPWR16	5.0	Functionality of this rule is covered by the PEPWR21 rule	PEPWR21
PEPWR17	5.0	Functionality of this rule is covered by the PEPWR20 rule	PEPWR20
PESTR04	5.0	Functionality of this rule is covered by the PESTR21 rule	PESTR21
PESTR15	5.0	Functionality of this rule is covered by the PESTR20 rule	PESTR20
PESTR16	5.0	Functionality of this rule is covered by the PESTR21 rule	PESTR21
PEPWR17	5.0	Functionality of this rule is covered by the PEPWR21 rule	PESTR20
PEPWR04	5.0	Functionality of this rule is covered by the PEPWR21 rule	PEPWR21
PEPWR15	5.0	Functionality of this rule is covered by the PEPWR20 rule	PEPWR20
PEPWR16	5.0	Functionality of this rule is covered by the PEPWR21 rule	PEPWR21
PEPWR17	5.0	Functionality of this rule is covered by the PEPWR20 rule	PEPWR20

Rule name	Future Release	Reason for removal	Replacement Rule (if any)
PESTR04	5.0	Functionality of this rule is covered by the PESTR21 rule	PESTR21
PESTR15	5.0	Functionality of this rule is covered by the PESTR20 rule	PESTR20
PESTR16	5.0	Functionality of this rule is covered by the PESTR20 rule	PESTR21
PESTR17	5.0	Functionality of this rule is covered by the PESTR20 rule	PESTR20
Clock_sync01, Clock_sync02	-	Functionality of this rule is covered by the Ac_sync* and Ac_unsync* rules	Ac_sync*, Ac_unsync*
Clock_sync03a, Clock_sync03b, Clock_sync03c	-	Functionality of this rule is covered by the Ac_conv01, Ac_conv02, and Ac_conv03 rules	Ac_conv01, Ac_conv02, Ac_conv03
Reset_sync01, Reset_sync03	-	Functionality of this rule is covered by the Ar_sync01, Ar_unsync01, Ar_synccdeassert01, and Ar_asyncdeassert01 rules	Ar_sync01, Ar_unsync01, Ar_synccdeassert01, Ar_asyncdeassert01
Ac_cdc04a	-	Functionality of this rule is covered by the Ac_datahold01a rule	Ac_datahold01a
Reset_check05	-	Functionality of this rule is covered by the Reset_info01 rule	Reset_info01

Parameters to be Deprecated

The following parameters of the SpyGlass Power family will be deprecated in a future SpyGlass release:

- `pe_reduction_effort_level`
- `pe_report_nongated_power`

Commands to be Deprecated

The following commands will be deprecated in the SpyGlass 5.0 release:

- `set_option lang` <*language*> project file command
- `-lang` command-line option

Documentation of Patch Releases

For *Micro*/*Patch* releases of SpyGlass (such as 4.6.2.3 or 4.6.2.5), the version number and the release date in the documentation will be updated only for those documents that have been updated for that release. All the other documents that have no updates will have the version number and release date of the previous release (the base release for that *Micro*/*Patch* release).

For *Major*/*Minor* releases of SpyGlass (such as 4.6.2 or 4.7.0), the version number and the release date in the documentation will be updated for ALL documents, irrespective of whether or not a document has been updated in that specific *Major*/*Minor* release.

Overview of SpyGlass 4.7.1 Release

Besides performance improvements, SpyGlass version 4.7.1 has the following enhancements:

SpyGlass Core

The enhancements in SpyGlass Core are described below:

- Report violations for missing DesignWare packages.

  Prior to the SpyGlass 4.7.1 release, the SpyGlass DesignWare run (triggered by the `set_option dw yes` command) used to proceed despite of the missing DesignWare packages. This resulted in fatal violations in the downstream flow if these packages were used in the design.

  Now, SpyGlass run aborts in case of the missing DesignWare packages.

  In such cases, set the `SPYGLASS_DC_PATH` variable to specify the path from where SpyGlass can pick DesignWare packages.

  If you do not set this variable properly, SpyGlass looks for the path specified in the `SPYGLASS_DC_DWARE_FILES_PATH` and `SPYGLASS_DC_DW_FILES_PATH` keys in the configuration file (.spyglass.setup). If you have not specified these keys, SpyGlass reports an error and exits.

NOTE: *This enhancement is applicable only if you set the following command in the project file:*

```
set_option dw yes
```

- Print individual goal summary for each goal belonging to a regression.

  The `-showgoals` command prints the individual goal summary for each goal belonging to all the regressions defined in a project file.

  This behavior will be controlled through a command in a future release.

SpyGlass RTL Modification Engine (RME)

The enhancements in RME are described below:

- Added support to expand statements inside the `generate_for` loop.

SpyGlass can now expand statements inside the `generate_for` loop to avoid scope or hierarchy change for the associated signals.

Earlier, the statements were expanded outside the `generate_for` loop resulting in the scope or hierarchy change for the associated signals.

- Added support to expand statements inside `generate_if` and `generate_case` to avoid scope or hierarchy change for the associated signals.
- RME does not add the *atrenta* prefix for the newly created ports.
- Added support for the save-restore flow for power reduction.
- Removed the limitation related to `` `define `` and `` `include ``.

Atrenta Console

The enhancements in Atrenta Console are described below.

- Added the GuideWare 2.0 comparison utility.

  This utility enables you to compare methodologies or goals in terms of the following:

  - ❒ The manner they were mapped in the previous releases.
  - ❒ The difference in terms of their rules, parameters, and products.

  One methodology or goal is called the reference data and the other methodology or goal is called the target data. The target data is compared with the reference data.

  The following figure shows the comparison results in the *Methodology Configuration Window*:

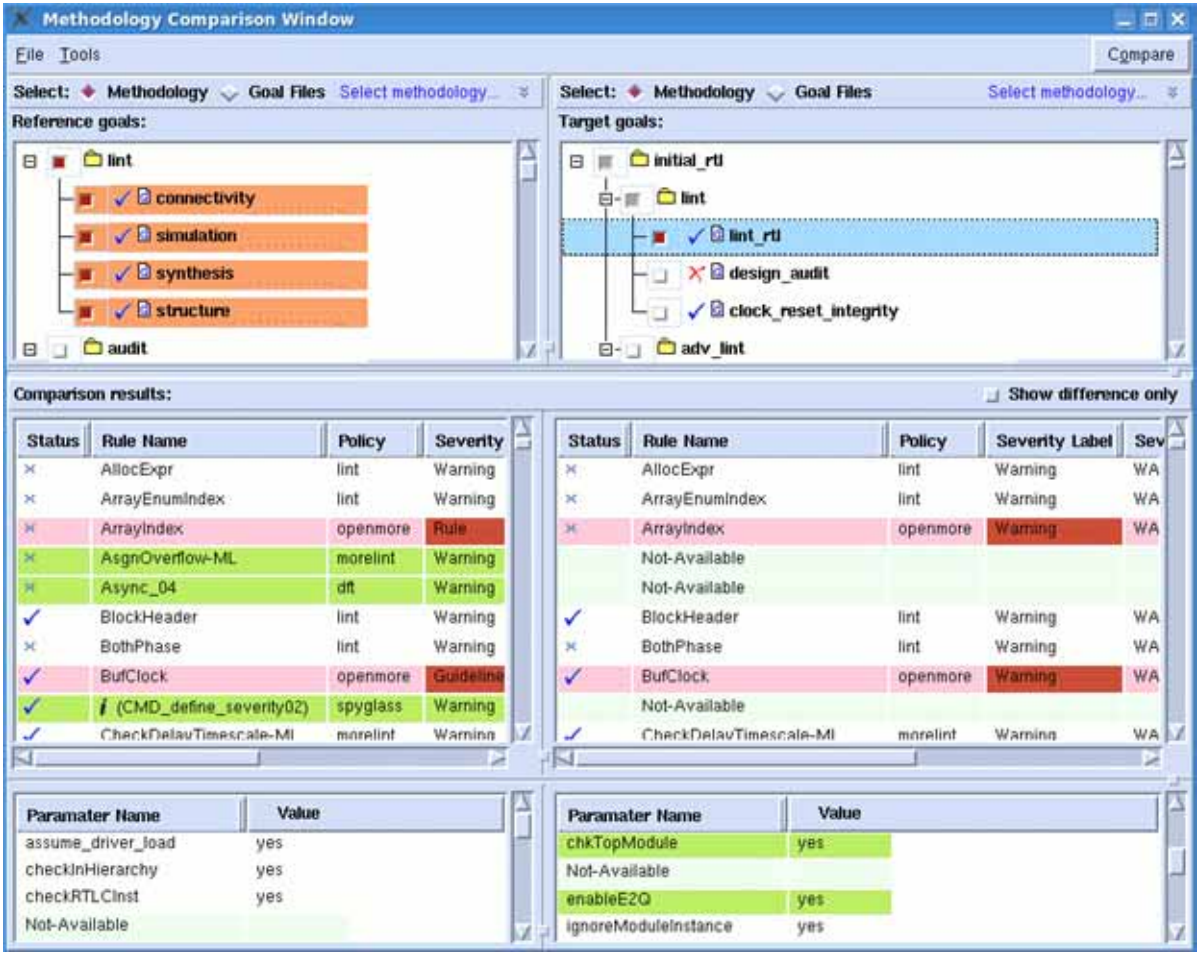

FIGURE 1.

To invoke the above window, select the *Tools -> Goal(s) with Goal(s)* menu option of the *Methodology Configuration Window*.

For details, refer to the description of this menu option in the *Atrenta Console Reference Guide*.

- Performance improvements

  The areas of performance improvements are as follows:

- ❒ Reduction in the initial GUI load time.
- ❒ Reduction in the goal switching time.
- ❒ Control of the Atrenta Console migration flow at the batch end under the `-gen_project` command.

  If you specify this command, the batch run will create project files that can be directly loaded in Atrenta Console.

Atrenta Products

This section describes the enhancements to the Atrenta products.

Base SpyGlass

The following enhancements are made in Base SpyGlass:

- Enhanced the `nocheckoverflow` parameter to accept rule names as argument, as shown in the following example:

  ```
  set_parameter nocheckoverflow W164a
  ```

  The above setting means that the `nocheckoverflow` parameter will be applicable only for the *W164a* rule.
- No rule checking is done for the nested modules that contain unsupported synthesis constructs.
- Added support for the SystemVerilog interface in following comment-related rules:

SpyGlass STARC Solution		
STARC-3.5.6.4	STARC-1.3.1.5a	STARC-1.3.1.5b
STARC-2.8.1.5	STARC-2.8.5.2	
SpyGlass morelint Solution		
FindStringsInComment-ML	CheckSynthPragma-ML	CoveragePragma-ML
PragmaComments-ML		
SpyGlass Lint Solution		
W464	W351	

SpyGlass ERC Solution

This section describes the enhancements to the SpyGlass ERC solution.

Modified Rules/Parameters/Constraints

- Enhanced the *clockPinsConnectedToClkNets* rule to report violations for latches having the EN pin connected to a predefined clock net through a combinational logic.
- Enhanced the violation message of the *checkOPPinConnectedToNet_a* rule to match with its severity *Warning*.

SpyGlass Lint Solution

This section describes the enhancements to the SpyGlass Lint solution.

Added Rules/Parameters/Constraints

- Added the following parameter:

Parameter name	Description	Used By
report_blackbox_inst	Specifies if the W110 rule should report a violation for port width mismatch for black box instances.	W110

Modified Rules/Parameters/Constraints

- You can enable the *W504* rule by using the `-fullpolicy` command-line option.
- Added support for the `strict` parameter in the following rules:

Rule Names			Rule Behavior
W494	W494a	W494b	If you set the strict parameter to yes or any of these rule names, such rules report a violation for partially unused ports.
W337			If you set the strict parameter to yes or this rule name, this rule reports violations for the string type variables that are used as case items.

- Enhanced the *W111* rule to support the `$signed` and `$unsigned` Verilog system functions inside the `for` loop.
- Enhanced the *W415a* rule to report a violation for multiple assignments to the same signal within the `for` loop.

  In such cases, this rule reports the following violation:

```
Signal <signal-name> is being assigned multiple times
( assignment within same for-loop ) in same always block
[Hierarchy: '<hier-path>']
```

SpyGlass morelint Solution

This section describes the enhancements to the SpyGlass morelint solution.

Added Rules/Parameters/Constraints

- Added the following parameters:

Parameter name	Description	Used By
check_param_association	Enables the ParamOverrideMismatch-ML rule to check for instances where a parameter is overridden through named association.	ParamOverrideMismatch-ML
check_xassign_casedefault	Enables the NoAssignX-ML rule to check for the default clause of the case statement, which has a static value containing X on the RHS of the assignment.	NoAssignX-ML
dccompat	Enables rule checking according to the Design Compiler ™ conventions.	SignedUnsignedExpr-ML
ignore_multidim	Enables the ResetFlop-ML rule to suppress violations from flip-flops, which are formed from multidimensional signals.	ResetFlop-ML

Parameter name	Description	Used By
ignore_unloaded_inst	Enables the UndrivenInTerm-ML rule to ignore combinational cells and look for a valid load when the checkInHierarchy parameter is also set to yes.	UndrivenInTerm-ML
report_floating_source	Enables the UndrivenInTerm-ML rule to print the actual floating net names in the violation message.	UndrivenInTerm-ML

Modified Rules/Parameters/Constraints

- The *AsgnOverflow-ML* rule is switched-off and will be deprecated in a future SpyGlass release.

  The functionality of this rule is covered by the *W164a* rule of the SpyGlass lint solution.

- Enhanced the *ConstantInput-ML* rule to check the inputs of a grey box, and report a violation if the input is tied to a constant.

- Enhanced the *HangingFlopOutput-ML* rule to report a violation if the output of a flip-flop is connected to a top-level output and is also connected with an unused signal.

- Enhanced the default behavior of the *NoAssignX-ML* rule to not report a violation for the 'X' usage in the `default` clause of the `case` statement.

  Set the `check_xassign_casedefault` parameter to `yes` to report such cases.

- Enhanced the *ParamWidthMismatch-ML* rule to work on the `ELABDU` view so that the rule can calculate width as per the overridden parameter value.

- Enhanced the *UndrivenInTerm-ML* rule to show hierarchical schematic when the `checkInHierarchy` parameter is set.
- Enhanced the *ParamWidthMismatch-ML* to work on the `ELABDU` view so that this rule can calculate the width as per the overridden parameter value.

SpyGlass simulation Solution

This section describes the enhancements to the SpyGlass simulation solution.

Added Rules/Parameters/Constraints

- Added the following parameter:

Parameter name	Description	Used By
check_complete_sensitivity_list	Enables the sim_race01 rule to check for the implicit always block.	sim_race01

Modified Rules/Parameters/Constraints

- Made following enhancements in the *sim_race01* rule:
  - It does not report a violation for the race between the combination and sequential assign block.
  - It does not report a violation for the race between the `always_comb` block and the other `assign`/`always` block.

SpyGlass STARC Solution

This section describes the enhancements to the SpyGlass STARC solution.

Modified Rules/Parameters/Constraints

- Enhanced the *STARC-1.1.1.3* rule (Verilog and VHDL) to support the EDIF, SDF, and Windows keywords.

  Now violations, this rule reports violations for the following list of words:

ABSOLUTE	cell	celltype	edif	DELAY	HOLD
IOPATH	NET	VIEW	SETUP	CON	AUX

COM1	COM2	COM3	LPT1	LPT2	PRN
NUL					

- Added support for the `effort_level` parameter in the *STARC-1.6.2.2* rule to improve the rule performance.

SpyGlass STARC2005 Solution

This section describes the enhancements to the SpyGlass STARC2005 solution.

Added Rules/Parameters/Constraints

- Added the following rules under the *STARC05-2.10.3.2b_s* rule group:
- Added the following rule:

Rule Name	Purpose
STARC05-2.10.3.2b_sa	Reports a violation if the RHS width is greater than the LHS width in an assignment.
STARC05-2.10.3.2b_sb	Reports a violation if the RHS width is less than the LHS width in an assignment.

Modified Rules/Parameters/Constraints

- Enhanced the *STARC05-2.7.2.3* rule to check for sequential blocks.
- Added support for the `allviol` parameter in the following rules:

STARC05-1.1.3.3e	STARC05-3.1.4.2	STARC05-1.6.3.1
STARC05-1.6.3.2	STARC05-1.6.2.2a	

SpyGlass STARCad-21 Solution

This section describes the enhancements to the SpyGlass STARCad-21 solution.

Modified Rules/Parameters/Constraints

- Enhanced the *setup_blockfile* prerequisite rule to not report violations for any unset parameter, if its dependent rule is not selected.

However, if any parameter-dependent rule is run and the corresponding parameter is not set, this rule will continue to report violations for the missing parameter values.

SpyGlass Advanced Lint Solution

This section describes the enhancements to the SpyGlass Advanced Lint solution.

Added Rules/Parameters/Constraints

- Added the following parameter:

Parameter name	Description	Used By
staticnet_scope	Specifies the type of nets to be checked by the Av_staticnet01 rule.	Av_staticnet01

Modified Rules/Parameters/Constraints

- Enhanced the default behavior of the *Av_staticnet01* rule to check for flip-flops only.
- Enhanced the default behavior of the *Av_deadcode01* to check inside the `if` statements and `case` statements only without checking inside the `default` labels.
- Enhanced the `dead_code_scope` parameter to support the following values:

Value	Purpose
case	Enables the Av_deadcode01 rule to check for the case constructs.
case_without_default	Enables the Av_deadcode01 rule to check for the case constructs.
condasgn	Enables the Av_deadcode01 rule to check for conditional assignments only.

SpyGlass CDC Solution

This section describes the enhancements to the SpyGlass CDC solution.

Added Rules/Parameters/Constraints

- Added the following rule:

Rule Name	Purpose
Setup_quasi_static01	Reports signals that are likely to be quasi-static signals in a design.

- Added the following constraints:

Constraint Name	Purpose
quasi_static_style	Use this constraint to specify criteria based on which SpyGlass should infer quasi-static signals in a design.
no_convergence_check	Use this constraint to specify net names that should not be checked for convergence.

- Added the following parameters:

Parameter name	Description	Used By
reset_reduce_pessimism	Specifies criteria to infer certain resets in a design other than the resets inferred by setting the `use_inferred_resets` parameter to `yes` or running the Reset_info01 rule.	Reset Information Rules, Reset Synchronization Rules, Reset Checking Rules, Reset Information Rules, and Param_clockreset04
check_input_coverage	Configures the Clock_info18 rule to report a violation for only input ports of the top-level design unit.	Clock_info18

Modified Rules/Parameters/Constraints

- Improved the messages and schematic generated by the *Ac_unsync01*, *Ac_unsync02*, *Ac_sync01*, *Ac_sync02*, and *Ac_psync01* rules.

  This enhancement may impact:

  - Waivers if a failure reason was used in the waiver commands.
  - Performance up to 10%.

- Enhanced the process of inferring clocks in a design.

  The clock_reduce_pessimism value is added to the `clock_reduce_pessimism` parameter.

  When you specify this value, SpyGlass infers clocks from all the inputs of a two-input gate even when one of its inputs is a definite clock candidate.

  For details, refer to the documentation of the `clock_reduce_pessimism` parameter in the *SpyGlass CDC Rules Reference Guide*.

- Enhanced the *Clock_sync05* and *Clock_sync06* rules to not report a violation if a port is driving or is driven by a quasi-static signal.

- Allowing combinational logic for the entire design.

You can now apply the `allow_combo_logic` constraint to top-level module. This way, the combinational logic can be allowed for the whole design.

- Enhanced the *Reset_check04* rule to not check for flip-flop outputs other than synchronizers.
- Improved the runtime of the `enable_debug_data` parameter up to 30%.

SpyGlass Constraints Solution

This section describes the enhancements to the SpyGlass Constraints solution.

Added Rules/Parameters/Constraints

- Added the following rule:

Rule Name	Purpose
Clk_Gen34	Reports a violation if duplicate clocks exist in the SDC file.
SDC_Methodology71	Reports a violation if the -min argument of the set_drive constraint is greater than the -max argument.

- Added the following parameter:

Parameter name	Description	Used By
tc_clk_register	Specifies if clock ports are registered.	Block11

Modified Rules/Parameters/Constraints

- Made the following enhancements in the *Block11* rule:
  - Added support for the false path constraints.
  - Enabled the checks for clock paths through the use of the `tc_clk_register` parameter.

- Enhanced the *Clk_Gen13* rule to report a violation if a clock name matches with the name of a block port.
- Enhanced the *Inp_Del02* rule to support the `set_max_delay` constraint.
- Enhanced the *Clk_Gen32* rule to traverse beyond sequential cells to search for master clocks.
- Enhanced the *Clk_Uncert02a* rule to only check for simple clock uncertainty and ignore all the inter-clock uncertainties.
- Enhanced the *SDC_GenerateIncr* rule to generate a report for the objects that do not generate I/O delays.

SpyGlass DFT Solution

This section describes the enhancements to the SpyGlass DFT solution.

Added Rules/Parameters/Constraints

- Added the following rule:

Rule Name	Purpose
Clock_27	Detects edge inconsistency between CGC and the driven flip-flops in the capture mode.

- Added the following parameters:

Parameter name	Description	Used By
dft_treat_primary_inputs_as_x_source	Specifies if primary ports should be considered as the 'X' source.	BIST_04
dft_check_test_mode_conflicts	Specifies if a conflict should be considered if the simulation value coming from a fan-in cone (internal driver) has: • Conflicting non-X (0 | 1) value as compared to the specified test_mode value • Conflicting non-X (0 | 1) value as compared to the specified test_mode value or unknown value ('X' or 'U').	Info_test mode_co nflict_01

Modified Rules/Parameters/Constraints

- Enhanced the *Info_logicalRedundant* rule to report LR (Logical Redundant) stuck at nodes along with the associated faults for better debugging.
- Enhanced the *Info_scanwrap* rule, as described below:
  - This rule reports incremental gain in the control, observe, and fault count by insertion of each `scan_wrap` constraint on a block.

    Earlier, this rule reported the total incremental gain for all the inserted `scan_wrap` constraints.
  - When you run the *Info_scanwap* rule or both the *Info_scanwap* and *dumpBlackBox* rules, the scan_wrap.rpt report shows the incremental gain.

    However, when you run only the *dumpBlackBox* rule, there is no change in report.

- Enhanced the *Info_untestable* rule to show incremental effect of the `test_mode` constraints on the blockage of faults for better debugging.
- Enhanced the *BIST_04* rule, as described below:
  - This rule reports one example of each category of X-generator for every flip-flop.
  - This rule reports the total count of X-generators for every flip-flop of each category of the X-generator.

SpyGlass DFT DSM Solution

This section describes the enhancements to the SpyGlass DFT DSM solution.

Added Rules/Parameters/Constraints

- Added the following rule:

Rule Name	Purpose
CG_07	Detects edge inconsistency between CGC and the driven flip-flops in the atspeed mode.

Modified Rules/Parameters/Constraints

- Updated the order of steps shown in the report generated by the *Info_transitionCoverage_audit* rule.

  The change in the order of steps is done to improve the performance of this rule.

SpyGlass DFT MBIST Solution

This section describes the enhancements to the SpyGlass DFT MBIST solution.

Modified Rules/Parameters/Constraints

- Enhanced the message of the *MBist_SGDC_03* rule to report the bit width of the source and target.

Other Enhancements

- Enhanced the following commands:

Command	Enhancement
mb_set_prefix_n_suffix	The -module_prefix and -file_prefix arguments of this command now also accept the NO_PREFIX value.
mb_remove_instance	This command can accept a hierarchical path in the -instance argument.
mb_insert_instance	This command now supports the parameter_map option for VHDL. This option enables users to insert parameterized instances in a design. Earlier, this option was supported only for Verilog designs.

- Added the `mb_replace_instance` and `mb_insert_instance` Tcl commands.

  When you specify these commands, SpyGlass does not allow RTL modification inside the instances that are inserted or replaced through these commands.
- Added sanity checks to check the parameter values specified by the `set_parameter` command in the Tcl flow.

SpyGlass Power Family

This section describes the enhancements to the SpyGlass Power family.

Added Rules/Parameters/Constraints

- Added the following rules:

Rule Name	Purpose
PECWL	Generates a custom wireload from a netlist design with spef files. You can use this wireload to estimate the capacitance of RTL designs in case your existing technology libraries do not have wireload tables.
PESTR30	Estimates the depth of a path in a design. Use this rule to estimate the depth of an enable added by the power reduction rules while adding a new enable or strengthening an enable.

- Added the following parameter:

Parameter name	Description	Used By
pe_prop_fastest_clock	Propagates the fastest clock in a clock network. This helps in performing clock power estimation in the worst case.	PECHECK04, PEPWR02, PEPWR03, PEPWR04, PEPWR05, PEPWR13, PEPWR14, PEPWR15, PEPWR16, PEPWR17, PEPWR20, PEPWR21, PEPWR22, PEPWR23, PEPWR24, PEPWR25, PESTR03, PESTR04, PESTR05, PESTR06, PESTR13, PESTR15, PESTR16, PESTR17, PESTR20, PESTR21, PESTR22, PESTR23, PESTR24, PESTR25, and PESTR26

- Added the `set_power_scaling` constraint.

  Use this constraint to add scaling factors on various power numbers while doing power estimation. This enables you to account for calibration based on prior information.

Modified Rules/Parameters/Constraints

- Modified the schematic highlighting of the following rules such that these rules highlight the effected register in a different color:

PESTR08	PRSTR09	PESTR10	PESTR11	PESTR12

Other Enhancements

- Added support for the 5.0 version of FSDB.

  This version is generated from the 2012.01 version onwards of the Springsoft tools. SpyGlass will continue to read the older versions of FSDB as well.

  However, since the FSDB generated by the SpyGlass rules will be of the 5.0 version, you need the 2012.01 onwards version of the Springsoft tools to read these files. Therefore, it is recommended to migrate to the newer version of the Springsoft tools in case you use the FSDB generated by SpyGlass.

- Detect buffers based on slew values.

  Earlier, for high fan-out nets and un-buffered clock nets, SpyGlass used to estimate buffers based on the `max_capacitance` and `fanout_load` attributes of cells.

  From this release onwards, SpyGlass can detect buffers based on slew values. The buffering is done to maintain a consistent slew in the whole design.

  Use the `pe_slew_based_buffering` parameter to enable this feature.

NOTE: *You must recompile the sglib files with the SpyGlass 4.7.1 version to estimate buffers based on slew values.*

- Added a new flow to generate a simulation SGDC file for the modified RTL in the power reduction run.

  In the power reduction run, when Power Fix generates a new RTL, you may want to run power estimation on the new RTL. However, the simulation file corresponding to the new RTL may not be available. As a result, power estimation may not be accurate.

  To solve this problem, a new flow is introduced in which while generating a new RTL, SpyGlass generates a new SGDC file that contains the activity information of the corresponding new RTL. You can use this SGDC file in the power estimation run.

  To enable this flow, use the `pe_generate_equiv_sim_file` parameter.

- Made significant improvements in the runtime of the SpyGlass SEC solution.

  In addition, the number of partially analyzed results is reduced and SpyGlass is able to prove most of the verification.

- Upgraded the synthesis optimization engine used by SpyGlass Power Family.

  This upgrade is primarily done to improve runtime with small improvements in QoR (reduction in area).

  Since the engine has been upgraded, you may notice an increase in the area (fall in QoR) for some designs. However, the overall trend is in the positive direction.

SpyGlass Power Verify Solution

This section describes the enhancements to the SpyGlass Power Verify solution.

Added Rules/Parameters/Constraints

- Added the following rules:

Rule Name	Purpose
LPLSH06	Reports a violation if the location of a level shifter in the UPF is not compatible with the main rail of the cell.
LPISO04D	Reports a violation if the isolation power net is not the primary power supply of the domain in which an isolation cell will be inferred.
LPERC01A	Checks if the supply net of a driver is working at a different voltage than the supply net of the receiver.
LPERC01B	Checks if the supply net of driver is less-on than the supply net of receiver.
LPERC02A	Checks if the input supply net of a power switch is operating at a different voltage than the output supply net.
LPERC02B	Checks if the input supply net of a level-shifter or power switch is less-on than the output supply net.

Rule Name	Purpose
LPERC03A	Checks if the supply net connected to the backup power pin is less-on than the primary supply net.
LPERC04A	Checks for power/ground supply pin connection with supply nets.
LPERC04B	Checks if the driver is a hanging net or is a supply net undefined in the power intent.
UPF_lowpower17	Reports a violation if the isolation power net is not declared in the domain in which the isolation cell will be inferred.

- Added the following parameters:

Parameter name	Description	Used By
lp_dump_ls_in_multi_supply_rpt	Specifies whether level shifter information be provided in the lp_multi_supply_instance report.	UPF_lowpower15
lp_check_aon_buffer	Specifies whether to check the AON buffers.	LPERC03A

SpyGlass Physical Base Solution

Following are the major enhancements to the SpyGlass Physical Base solution:

- Improved debugging

  The fan-in and fan-out source and end points for the nodes having large fan-in and fan-out cones can be annotated on the *Logic Congestion* GUI. This helps in debugging.

- Added support for pure netlist designs.

  Input netlist is not modified during the design read and optimization step.

- Added support for the `set_clock_groups` SDC command.

- Improved the runtime for timing optimization and STA.

- Improved the QoR for timing optimization and STA.

Added Rules/Parameters/Constraints

- Added the following rules:

Rule Name	Purpose
PHY_LogicDepth_MM	Reports the timing paths starting or ending at a hard-macro or a black box instance, which exceeds specified logic depth.
PHY_LogicDepth_MM_Delay	Reports the timing paths starting or ending at a block.

- Added the following parameter:

Parameter name	Description	Used By
phy_enable_netlist_flow	Enables or disables the netlist flow in the SpyGlass Physical run.	Prefloorplan rules

Modified Rules/Parameters/Constraints

- Changed the default value of the `phy_cong_module_size_high` parameter from -1 (unset value) to 1 million instances.

  This means that the congestion score is not computed for RTL modules greater than one million instances.

SpyGlass TXV Solution

This section describes the enhancements to the SpyGlass TXV solution.

Other Enhancements

- Made the following improvements in the MCP control logic detection:
  - Detection of MCP control logic from the MUX present in the data path.

- Detection of MCP control logic from library cell.

- Added the new domain computation flow.

  This flow contains the following three modes:

  - STA-compliant mode: Interprets FP/SCU/SCG to come up with the domain information.
  - STRICT-mode (Recommended): You must specify all clocks in the single `set_clock_groups -asynchronous` command (no ambiguity).
  - SGDC mode: Read domains from the SGDC file.

Documentation

The following changes are made in SpyGlass help:

- Added related topics for various topics in the HTML help set.

  To view the related topics, perform any of the following actions:

  - Click the *Related Topics* link (Related Topics) present at the bottom of the HTML page.
  - Click the related topics button ( ) present on the toolbar of the HTML page.

  The related topics appear in a pop-up window, as shown in the following figure:

FIGURE 2. Related Topics

When you click a related topic in the above pop-up window, the corresponding HTML page is displayed. To go back to the previous page, click the *Back* button of the browser.

- Added a landing page in HTML help.

  This page provides multiple entry points to access the SpyGlass HTML help. It is the first page that appears when you invoke the SpyGlass HTML help.

  To return to the landing page, click the *Welcome to SpyGlass* link in the *Contents* tab, as shown in the following figure:

FIGURE 3. Link to the Landing Page

- The *Search* tab is now the default tab in the SpyGlass HTML help set.
- You can invoke SpyGlass HTML help in any of the following ways:
  - ❒ By clicking the *Help -> SpyGlass Help* menu option in the Atrenta Console GUI.
  - ❒ By running the `spyhelpviewer` utility present in the <SpyGlass-installation-path>/SPYGLASS_HOME/bin/ directory.
- You can invoke the SpyGlass PDF help in any of the following ways:
  - ❒ By clicking the *Help -> SpyGlass Manuals* menu option in the Atrenta Console GUI.
  - ❒ By running the `spydocviewer` utility present in the <SpyGlass-installation-path>/SPYGLASS_HOME/bin/ directory.
- Added Frequently Asked Questions (FAQs) to provide help on using the SpyGlass help set (HTML and PDF).

  You can view FAQs in any of the following ways:
  - ❒ By clicking the *How to Use SpyGlass Help (FAQs)* link in the landing page.

- By clicking the *Documentation FAQs* link in the *Contents* tab, as shown in the following figure:

FIGURE 4. Link to FAQs

List of Incidents Fixed in the SpyGlass 4.7.1 Release

VI #	EW #	Title
44629	73681	vhFileName not returning architecture name
50468	77346	Check to catch the scenario where a supply is used without having declared in the domain.
50839	77249	New rule request to check the level shifter location is compatible with the std_cell_main_rail attribute.
51348	77816	UPF: LPSVM57 issues: message & multiple strategies
51393	77858, 79383	{ENH} Reset_check07 rule should not consider combo logic inside reset synchronization logic/cell.
52496	78322	Issue in license queuing feature - license are not released even after the job is completed
53594	79281	txv_datasheet_report link active even though the report was not created
54284	79651	GuideWare and Methodology doc not visible in HTML help
55221	80072, 87335	False violation of Reset_check04
55429	80405	New LP rule required to check iso cell inferred in switchable PD
56964	81087	False Reset_sync02 violation
57638	81524	Constraints doesn't work for registers defined locally in always block
58589	82326	Missing Clk_Gen32 violation
58649	82549	{ENH} consider set_max_delay on Inp_Del02
58653	82403	Enhancement in RTL174c rule!
58709	82587	{ENH} Input drive minimum value is greater than input drive maximum value.
58985	82800	SetBeforeRead-ML causes false violation when for-loop is used
59197	82767	{ENH} Add support of set_false_path on Block11
59199	82733, 88224	{ENH} Enhancement in Clk_Gen13
59629	82972	GenSDC : Wrong master clock of generated clock
59983	83491	Enhance RULE_RTL125
60020	83505	Enhance RULE_VLG041
60140	83444	{ENH} Need option to specify prefix for virtual clocks during SDC to SGDC conversion

VI #	EW #	Title
60356	83551	Add option to consider fastest clock's activity for power estimation through MUX logic
60519	83655, 87671, 87770, 87895, 88764	False WRN_27 in case of parameterized interface
60953	83017, 88617	ENH: Rule to flag multiple usage of same clock name in the SDC file
61015	83725	Please change the srp link in the custom policy to starc.
61201	84013	UndrivenInTerm-ML should ignore non-driving inputs inside logic which is leading to deadcode
61791	81500	parse –v/-y in same language as of design files
62059	84502	Multiple Resets Identification
62087	84421	Clk_Uncert02a rule doesn't report the unconstrained issue
62175	84526	gen_sdc dropping bits on set_input_delay bus
62195	84550	enhancement in Clock_Gen07 rule
62211		Modify the instances inside a 'generate-if' or 'generate-case' statement inside the generate block itself
62333	84607	UndrivenInTerm-ML rule should report hierarchical floating driver info in the violation message
62640	83027	{ENH} Enhancement in Clk_Lat04a to flag for zero set_clock_latency when -source is specified
62689	84856, 87603	Now good way to compare goal to goal or sub-methodology to sub-methodology
62913	84912	GenSDC : Use $SPYGLASS_HOME in tech files path in SPNC
62944	85035	sg_shell/adc - fatals on NETS.
63074	85145	Using rulename with strict option does not work for some STARC rules
63245	88292	ParamOverrideMismatch-ML rule should flag for overriding parameters by name under some switch
63246		ResetFlop-ML rule should not flag for memory registers
63406	85391	Incorrect UndrivenInTerm-ML violation - driver is BBOX output
63439	81524	Constraints doesn't work for registers defined locally in always block
63459	85470, 80528	Failed to properly filter Clock_sync06 violations due to quasi-static or cdc_false_path

VI #	EW #	Title
63478	85430, 87244	set_isolation_control keeps space or blank between {}
63688	81462	sim_race01 violation
63752	85580	STARC-2.5.2.1 causes false violation
63845	85665	Constraints cross reference not working
63858	85284, 89022, 90050	waiver runtime issue
63983	85734	{Enh} Normal buffers in a daisy chain of PSW's not flagged
64031	82643	Custom rule did not flag
64096	88587	Rule should flag if an initialized register not controlled by set/reset/enable control logic
64162		False WRN_64 violation
64189	85915	SpyGlass STARCAD-21 policy generates a false Info message about missing 'control_file' parameter
64195	85845	Custom rule of custom policy !
64287		False W111 violation
64328		Av_staticnet should be improved to narrow the scope of check
64351	85915	Need Rule Dependency chart from kernel so that policies team can control pre-requisite rule runs
64383	85985	OVL file is not processed when top of design is compiled into a library
64444	86014	The mapfile flow does not honor "-allow_module_override"
64445	85442	Request for easier "dial like" tuning of power numbers
64446	85439, 85348	FlopEConst not reporting all flops even with allviol=yes
64484	85941	LPLSH03 message improvement
64520	86073	Netlist Optional review - Custom rule severity to be WarningFlow
64521	86074	Netlist Optional review - Custom rule severity to be Info
64575	86101	Enh: Print only useful info in W448_Report
64636	86023	RTL - Optional review : infoDff and infoNUseDff
64638	86025	RTL-Optional review : Overlap between custom rules
64679	86184, 86183	SpyGlass synthesize as latch, which should get infer as Flop
64771	86242	Enh: Lack of input constraints should be flagged

VI #	EW #	Title
64783	86215, 88580	mapfile compilation flow using file extension fails when source files are specified with “-v .sv"
64786	86259, 87107	mapfile compilation flow issue with -v files
64936	86155, 86351, 87458	Add support of "inside" construct in system verilog
65146	86958	SpyGlass performance problem on STARC 1.2.1.3
65162		Provide support for 'parameter_map' for a vhdl module to be inserted through 'mb_insert_instance'
65189	86965	False SYNTH_5274 message
65190	86412	sdc2sgdc does not care about time unit for generated SGDC
65260	87056	Incorrect STX_VE_266 errors
65296	87070	{ENH} Need a new check to flag if backup_power is off when primary_power is on
65418	87160	{ENH} Enhancement to check LS input and output supply PSTs
65540	84656	ErrorAnalyzeBBox is not flagged on a cell defined inside 'celldefine
65542	87209	W337 warning for code supported by other simulators and synthesizers
65544	89092	Reload Project in Console GUI gives message about Multiple Tops
65575	87242	False Clk_gen02/03 violations because of non detection of clock pin in lib file
65608	87260	DFT DSM transition coverage long runtime issue
65639	87284	The documentation of SYNTH_5199, SYNTH_5355 is not helpful
65689		Error messages on screen o/p
65728	87325, 88588	{ENH} Need SGDC constraint to mimic parameter 'no_convergence_check'
65818	87426	False STARC-2.1.1.2 message.
65866		GenSDC should generate multiple generated clocks based on multiple master clocks in its source
65943	87525	pin not found issue while trying to find pin through Hierarchical Search
65953	87530	Spyglass is analyzing the path through the ICG cell and hence comboloop is detected

VI #	EW #	Title
66015	87612	W123 causes false violation
66020	87674	Need to show LR (Log. Redundant) category in the textual fault report
66060	87671	False WRN_64 on an interface port when index is explicitly mentioned
66063	87661	ParamWidthMismatch-ML always uses parameter default values
66108	87538	{ENH} Rule to flag wrongly inserted negative ICGC -- Clock_27 / CG_07
66112	87705	False SetBeforeRead-ML violation on packed structure member
66113	87712	Very long run time for rule STARC-2.8.1.4
66119	87726	Output PIN of BBOX cannot be used as add_port_state
66132	87224	{ENH} Enhance the behavior of LPSVM53 to not check for the data pins
66133	86426	Modify custom rule to report at leaf level so all the violations can be waived with the single "waive -du" waiver option
66194	87738	Some SpyGlass-LP rules do not report error/warnings but they do not appear in no_msg_reporting_rules.rpt
66230	87718	False Ac_conv03 violation
66280	87842	ErrorAnalyzeBBox error message consistency issue between libhdl and classic flows
66298	87841	False violations of STARC-2.3.1.5a and STARC02-2.3.1.5a
66302	87789	SpyGlass Adv-CDC is taking 10+ hrs. to run a design
66349	87879	False Ac_conv03 violation
66374	87805	{ENH}Rule to catch that PWS o/p enable is connected to a PWS i/p enable in a daisy chain and the fanout of PWS o/p enable is one
66392	87882	Synthesis error is not dumped in moresimple report
66405	87907	STX_VE_911 with SpyGlassInternalFatal INTERNAL_FATAL
66414	87921	There should be documentation for is_isolated attribute in rule reference guide
66474	87935, 87680, 88512	False Clock_glitch02 violation
66554	87984	{ENH} Improve debug capability for faults blocked by testmode

VI #	EW #	Title
66555	87986	{ENH} Rule to show how many undetectable faults could be fixed by scan wrapper
66593	88031	SpyGlassInternalWarning WRN_901 message reported
66643	88058	SignedUnsignedExpr-ML missing signed conversion issues flagged by other synthesis tool
66645	87955	-enableSV does not work during rule check, when verilog design is precompiled with -enableSV
66707	88091	STX_VE_416,STX_VE_417 and STX_VE_418 reports incorrect line numbers
66715	88095	Syntax error while handling .* implicit port connection with wildcard
66717	88122	Enh: rollback of for-generate under a placeholder scope
66719	88063	Enhancement required in custom rule
66743	88043	SpyGlass performance on STARC-1.2.1.2 and STARC-1.6.2.2
66750	88141	STX_VE_349 - Task or function cannot be used unless declared earlier
66757	88134	{ENH} Request for new ERC checks for SpyGlass-LP
66771	88154	Missing violation of STARC-2.8.1.3 and STARC05-2.8.1.3 and DuplicateCase-ML
66775	88157, 88489	W494 warning not getting reported when part-select is used in the rtl.
66795	88171, 88242	False SGDCSTX_008 messages
66938	88214, 88820	Incorrect sim_race01 violations
66998		Recognizing FSM's in System verilog
67010	88306	STARC05-2.7.2.3 does not flag for 'default: begin end'
67015	88305	multiple parameter definition in instantiation causes tool crash
67016	88062	Missing violation of Av_bus01
67038	88318	Missing Ac_sync01 violation
67065	88320	-dw for DW_data_sync_na is not working
67090	88323	false behavior of STARC05-2.8.1.4
67096	89052	False LPSVM04A with -threshold option
67117	88210	False UPF_lowpower08 violations
67181	88389	Missing Reset_sync02 violation
67193	88356	Rule ConstantInput-ML takes very long time

VI #	EW #	Title
67203	88118	False violation of UndrivenInTerm-ML & UnloadedOutTerm-ML
67216	88399, 89151, 89150	LPLSH05 false violation
67303	88478, 77452	-nocheckoverflow parameter need to support rule name (-nocheckoverflow=W164a)
67320	88494, 89172	EDIF, SDF, Windows keywords support for STARC-1.1.1.3
67387	88324	False Ac_conv02 rule violation
67409	88530	Cross reference to constraint does not work
67441	88536	False violation of CombLoop for a vhd testcase with for loop
67492	88563	WRN_1024 always flags for signed conversion of SV interface data
67495	88598	False LPCONN01 violation
67538		mthresh values not getting updated properly in console mode
67590		Av_deadcode01 should flag reason of deadcode to distinguish messages
67591		Av_deadcode01 should not flag messages of default clause in case statement under an option
67603	88624	clockPinsConnectedToClkNets does not recognize an inverted clock as a valid clock
67624	88599	Discrepancy in synthesized netlist
67677	89026	WRN_64 getting flagged pointing part select is out of range
67679	88677	RME does not add prefix "atrenta" for all new ports
67692	88696	Memory leak causing machine hang
67700	88674	rule W362 false warning for width mismatch
67706	88691	{ENH} Support of -isolation_supply_set option to set_isolation UPF command
67788	88713	waivers are lost in console upon opening and closing the waiver window
67884	88798	W164c bug with subtraction term
67934	88776	False violation of W415a
68012	88031	SpyGlassInternalWarning WRN_901 message reported
68040	87907	STX_VE_911 with SpyGlassInternalFatal INTERNAL_FATAL
68152	88653	Preference "Handle meta characters in waiver generation" has no effect

VI #	EW #	Title
68188	88915	BIST_04 - The message should flag if latch is also in input cone. (Spec change)
68215		Allow hierarchical path in -instance field of mb_remove_instance command
68219	88775	False W156 violation
68236	88950	Ar_sync_group rules do not flag
68243	88872	{ENH} MCP rule for checking on start/end options for flops on clock domains with diff frequency
68250		Enh: Create a parameter for BIST_04 to allow primary inputs that are directly registered
68255	88901, 89132	Fatal error when specifying port/signal name in elements field of set_retention command
68259	88959	Incorrect sdc2sgdc conversion leading to false Sgdc_clockreset02 errors
68264	88956	core dump caused by memory explosion: SG_ASSERT_ERROR:src/amgGenDwBoundary.cxx
68279		CKA/CKB Timing Arcs being flagged as 'not valid' (SDC_36)
68286	88863	FP / MCP Unevaluated due to complex clocks - Txv_MCP01
68287		switch -vlog2001_generate_name for unnamed generate blocks in SV mode not working
68305		mb_replace_instance: difference in behavior when top is used in the instance name or not
68360	88995	Use of internal name including Atrenta_External_Domain
68368	88997	Incorrect file path given in Audit report
68392	88962	false error sim_race01
68393	88736	vn2Net is not giving the correct net path name list for multi-dimensional net name
68397	89010	False ISO04A violation
68457	88941, 89686	False LPSVM08 due to with -source option applied on both inputs and outputs in case of feedthrough
68469	86215, 88580	Kernel Support for mapfile compilation flow using file extension
68485	89054	Add a note in policy guide for '-update' argument support in UPF Version 2.0
68511	89071, 89073	Unexpected SYNTH_5255 error

VI #	EW #	Title
68554	89075	UPF setup rules running for non-LP goals if UPF is called up in sgdc file
68556		STX_VE_605 Illegal use of identifier
68582	89123	Waiver not being applied on repeat runs of power_est_average goal
68596	89139	Incorrect value on generic map inside "translate_off" pragma for generate instance
68619	89113	False Diagnose_02 reported on the EN and CLR pins of scan flops with D pin connected to 0
68641	89060	Custom document to be updated for custom rules
68642	88794	Internal error in 3rd party licensing tool
68655	88948	Hang while running rule LPLSHPR
68662	89074	SYNTH_5407 Synthesis issue
68684	89105	False LPSVM22 violation
68705		STX_VH_628 violation reported incorrectly
68730	89208	W415a does not flag when for-loop is used
68749	89050	False LPSVM09 violation in postlayout LP check
68758	89186	The doc of ELAB_6311 should remove as this rule does not exist
68833	89238	Restore support for creating schematics in hierarchical CDC flow
68869		Clarify documentation of UndrivenNet-ML behavior when -checktopDU is set
68876	89259	STX_VE_481 is reported for VHDL config file.
68883		Show_Case_Analysis issue (rule by copy) issue in GUI
68892	89285	Problem in creating 'qualifier' constraint through GUI constraint editor
68913	89335	False STX_VE_481 error when UDP contains `ifdef directive
68916	89304	Not able to load vdbfile in spyglass 4.6.2.2
68922	89336	False violation of HangingFlopOutput-ML when flop o/p is connected to a top level o/p and also connected with an unused signal
68931	89315	PR autofix could not fix RTL imported by `include command

VI #	EW #	Title
68998	89362	Avoid assign statement in ATRENTA_AND_1 and ATRENTA_OR_1
69000	89354	scanwrap constraint does not allow hierarchical instance name as argument
69004	89378	False SYNTH_5230 error
69005	89380	LPISO04A flags missing strategy where no_isolation is specified
69007		incomplete RME files (sgdc and prj) in case of non-top module forced as top/no modification to top
69010	89366	{ENH} Modification in SpyGlass parameter for C28
69030	69030	FP NonTop result, if start/end point referred by [get_clocks] is blocked
69078	89401, 89408, 89711	RME Hangs when module name is variable defined in another file.
69090	89358	{ENH} Add a parameter to control UPF_lowpower15 to report missing connect_supply_net on LS
69094	89441	Cannot waive PESTR12 message
69095	89434	{ENH} LPLSH05 rule "message 3" is missing strategy name
69104	89310	False violation of LPISO04A
69105		Kernel not recognizing preset/reset pins of lib cell as reset
69111		Sec unknown destination flop false error
69112		RME generates non existing "-y" paths in sources_1.f
69113		Soc_07 violation is not reported with 4.6.2 while it is reported with 4.7.0
69116	89467	SG falsely reporting W111 and W240 issues
69119	89409	All the power autofix documentation should say to use atrenta_generated_imp_design.f file
69143	89500, 89503	AdvLint false violation for reset signals
69157	89430	False LPSVM53 violation
69202	89521	Hang during rule analysis
69208	89531, 89526, 89551	References to ELAB_546 , ELAB_550 and ELAB_611 need to be removed as these rule is not flagged anymore
69212	89277	Abnormal Termination
69214	89553	Abnormal Termination due to parameter=0

VI #	EW #	Title
69224	89560	Spreadsheet for rule LPLSH04 fails to open
69225	89555	RME switches bit directions, merged an upto signal in downto format as it has to be connected to downto signal -
69229	89561	Txv MCP/FP spreadsheet issue
69250	89558	Ac_sync02 false handshake
69254	89136	PDR exists with PARTIAL_PASS in 1 second even though time is available
69257	89349	False LPSVM22 violation, correct isolation signal is not reaching the enable when passes through two buffer cell
69261	89348	False LPSVM09 violation
69263	89487	False LPLIB_check02 violation (related_power_pin/ related_ground_pin are not read for bus pins)
69269	89492	False LPERC04A violations - ground supply considered as a power supply.
69278	89601	Hierarchical references fail when multi-level structure declared inside generate statement
69286	89602	FSM not recognized by Spyglass
69288	89542	Missing LPSVM53 violation
69290	89486, 88936	False LPERC02A violations
69294	89605	Tying part of ports to X in instantiation, synthesizes all ports as tied to 0
69336	89629	Incorrect severity is mentioned in document "SpyGlass_ERCRules_Reference" for few rules
69381	89656	Huge increase in memory requirement for custom rule
69386	89289	Spyglass cause UPFSEM_4 Fatal error when supply nets specified as 'power_domain.supply_set_handle.function'
69415	89543	FSM Viewer disappears when turning on case analysis
69416	89698	False Ar_unsync01 violation
69436	89550, 89556	References to ELAB_3613 and ELAB_3618 need to be removed as these rules are not flagged anymore
69444	89697	Spyglass v4.7.0 does not queue for "datasheet" and "dashboard"
69455	89723	SYNTH_5407 error: shift (stream) operator fails at port connection under some circumstances
69463	89731	False RTL054b reported

VI #	EW #	Title
69530	89748	Spyglass crash
69532	89750	Wrong calculation of integer const function
69533	89654, 89513	LP_CROSSING_DATA takes too much time
69536	89763, 90090	Abnormal termination at Av_clkinf01rule while running audit goal
69547		Enh. mb_set_prefix_n_suffix should allow specifying '-wire_naming_style'
69569	89765	mbist-dft-FIXED-PRS file in SpyGlass installation area is not up-to date
69586	89754	PESTR11 message not getting waived by waive -ip
69641	89801	MCP abnormal termination
69644	89804	sg_shell : Incremental waiver application issue
69646	89807	av_case03 and typedefs causes false warning and disappears when typedef not used
69659	89802	Documentation improvements for SpyGlass Exit Codes in user guide
69691	89843	Crash reported:LICENCING ERROR: Internal error occurred in third party licensing tool.
69700	89749	Incremental Schematic Behavior in 4.7 on a precompiled cell
69709	89811	Block_Summary.csv needs to be added to the documentation under CDC-REPORT
69711	89859	V4.7.0 based CDC run indicates that a multi-bit bus connection is shown as single bit
69762	89839	Incorrect SDC_286 error message
69802	89816	STARC05-3.1.4.2 doesn't support -allviol parameter
69817	89666	False violation LPISO04A when using "set_related_supply_net" command
69838	89895	The following rule(s) have been marked obsolete
69849	89744	False LPSVM53 violations
69873	89950	set_case_analysis disappears when expanding nets
69929		PDR exists with PARTIAL_PASS in 1 second even though time is available
69978	83444	{ENH} Need option to specify prefix for virtual clocks during SDC to SGDC conversion

VI #	EW #	Title
69980	89979	False error STX_VE_1190 for system verilog interface array instance with modport
69988		Segmentation fault on SystemVerilog construct
69991	89882	Licensing message in moresimple.rpt misleading
70023	90043	Adv-Lint Av_fsm02 rule not reporting correct line in RTL
70029	89803	-gen_compat_waiver not able to convert message waiver of spyglass 4.6.1 to 4.7.0 version
70052	90065	Abnormal termination at SGDC_waive31 while precompiling VHDL
70055	90060	Discrepancy in pe_summary report
70071		False STX due to struct array label expression (Segmentation fault on SystemVerilog construct)
70121	90112	False SYNTH_5175 message on 'ascending attribute in vhdl
70142	90145	Abnormal termination
70186	90148	Invalid STX_VE_277 fatal under esoteric conditions (streaming >> op, includes, generates)
70206	90171	Crashing on Rule Diagnose_Scanchain″ -- Cause: Bbox related memory optimization + assumption failure
70230	90163	false flagging of "parameter control_file not specified" for rule BOTH_SETRESET
70247	90197	Fatal lplib_check01 - enable attribute not picked up in library under strange conditions
70290	90216	-report STARC_2414 does not generate correct report if STARC02-2.4.1.4 is not specified with "-rules"
70309	90233	SpyGlass fatals out on unregistered/obsolete rule
70373	90258	False DES040a message in Netlist Checks
70384	90246	W120 does not honor generic value when description uses generic in if-generate
70415	90190	RME generated source.f does not handle 'gen_block_options'
70451	90307	Incorrect UndrivenInTerm-ML violation due to incorrect port size generation during synthesis
70475	90123	LPSVM47 is not reported in pre-layout netlist whereas correctly flags for post layout netlist
70476	90299	Mandatory fields are not auto populated during interactive constraint addition

VI #	EW #	Title
70478	90296	Lack of documentation on Ac_sanity07 and associated parameter
70480	90303	False Ac_sanity07 violation
70525	90356	Custom rule title needs to be changed
70535	90367	Documentation of custom rule - add examples
70559	90348	Msg Summary table view is lost after waiving a message
70576	90324	Ac_cdc08 Partially-Proved in 4.7.0 version
70682	90476	Severity of custom rules to be changed
70708	90491	False violation of DES065a: reporting the cells which are not in the clock path
70763	89680	In SpyGlass GUI , cannot change project name and fill top module name in Read Option
70786	90470	Spyglass CDC - Waveform Crash
70804	90569	Cannot Restore session with the copied Results tar bundle
70867	90568	Enable detection for MCP verification
70888	90623	Abnormal termination with SpyGlass 4.7.0
71032	90701	define macro cannot be recognized during fromto check -> define inside a file passed through -v option
71172		SpyGlass Terminator Signal: 11 [SIGSEGV (Segmentation fault)] during CDC run

Overview of SpyGlass 4.7.0 Release

Besides performance improvements, SpyGlass version 4.7.0 has the following enhancements:

SpyGlass Core

The following enhancements are made in SpyGlass Core:

- Added support for encrypting design files.

  Use the `spyencrypt` utility to encrypt design files. You can use the encrypted design files for SpyGlass analysis just like un-encrypted design files.

  For details, refer to the Working with *Encrypted Design Files* section of *Atrenta Console User Guide*.

- Deprecated the `FLATDU2_WOL` view.

  All rules registered with this view are internally moved to the `FLATDU2_WL` view.

- Due to some changes in the internal object model of VHDL libraries, there is an increase in the size of generated VHDL libraries and memory consumed by the VHDL object model.

SpyGlass RTL Modification Engine (RME)

Added support to generate project files (.prj files).

This way, files modified by the SpyGlass RME can run in Atrenta Console easily.

Atrenta Console

The enhancements in Atrenta Console are described below.

- Improved the PG netlist view in the schematic.

  The improvements are described below:

- Appropriate symbols appear to identify instance types, such as AND, OR, and MUX within a rectangular box representing a PG netlist view.
- Placement of power and ground pins is corrected.

  Now, power pins appear on the top of the rectangular box, and ground pins appear at the bottom of rectangular box.

  Earlier, these pins were displayed along with input and output pins, as shown in the following figure:

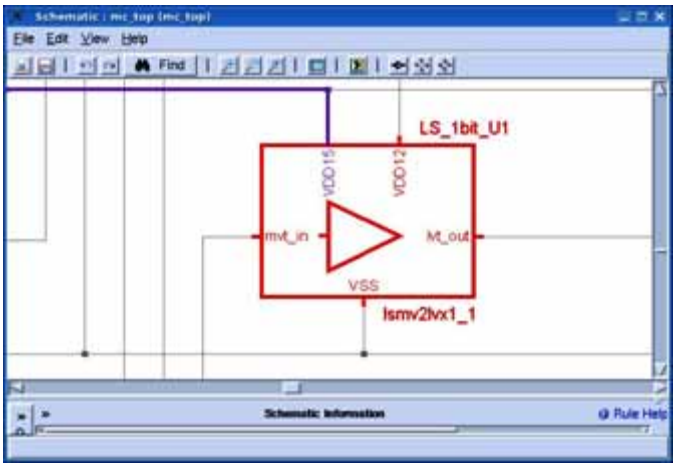

FIGURE 5. Placement of power and ground pins prior to Spyglass 4.7.0

- Added support to open liberty files from the schematic.

  To view the definition of the cells defined in liberty files, right-click on a cell in the schematic and select the *Open Liberty File* option from the shortcut menu, as shown in the following figure:

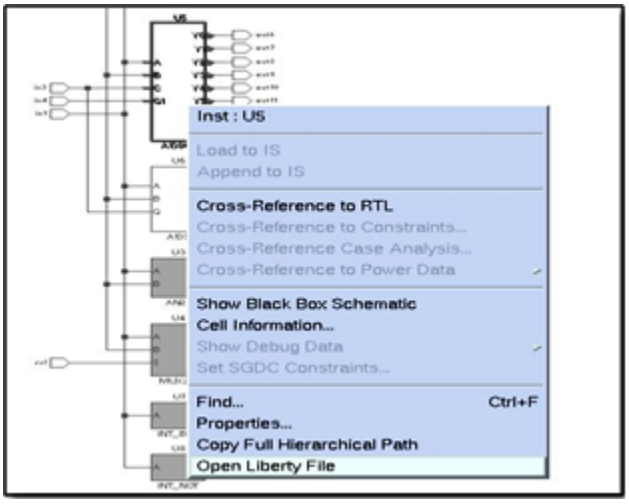

FIGURE 6. Accessing liberty files from schematic

For details, refer to the *Viewing Liberty Files* topic in *Atrenta Console Reference Guide*.

- Added the capability to restore the previous view of the schematic.

  Earlier, probing and traversal in the incremental schematic did not reload the schematic to its original state.

- Added support to set a default editor program for reports and log files, and the set a line flag for the editor.

  The following options are added in the *Miscellaneous* page of the *Preferences* dialog:

Option	Description
Use external editor for displaying reports/logs	Select this option to open reports and log files in the text editor specified by the *Specify external editor program* field.
Specify external editor line flag	This field sets the line flag (line number format) specific to an editor, which is specified in the *Specify external editor program* field.

For details on the above options, refer to *Atrenta Console Reference Guide*.

- Added support to abstract logic between the start and end points in the schematic.

  In this type of abstraction, all objects between the start and end points are abstracted for better schematic display.

  However, based on the functionality of a rule, certain objects are not abstracted between the start and end points, as shown in the following figure:

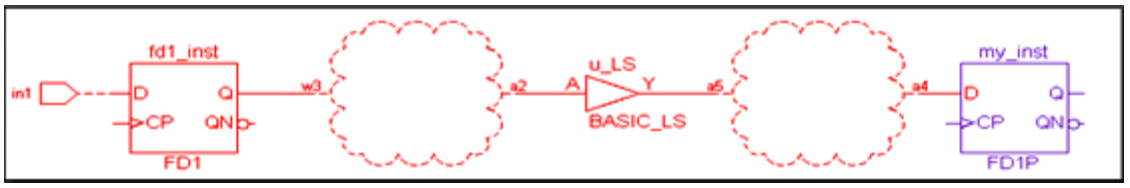

FIGURE 7. Schematic abstraction

NOTE: *Currently, level shifters are not abstracted along with other objects.*

For details, refer to the *Abstraction between Start and End Points* topic in *Atrenta Console Reference Guide*.

- Improved the performance in case-analysis annotation.

  The improvements are described below.

  - A product can automatically load static attributes along with violations.
  - In the SpyGlass DFT solution, attributes whose number is not a constant (dynamic data) are automatically loaded.

    You can generate dynamic data by using the `define_tag` and `atspeed_clock_frequency` constraints.
  - Load time of static violations has improved as they are selectively loaded for visible objects.
  - Removed any option related to the selective or complete mode from the GUI so that you cannot specify these modes.

    Now, based on the type of auxiliary violation selected, SpyGlass automatically loads that violation in selective or complete mode.

- Removed the need to specify a language mode, such as `vhdl`, `verilog`, or `mixed`.

  If you do not specify a language mode:

  - SpyGlass runs in the `mixed` mode by default.
  - SpyGlass creates the *<goal-name>*.spq file, and the *MCS* window does not save different language goal files (*<goal-name>*-*<language>*.spq).

- Disallow SDE invocation.

  Atrenta Console is now the only GUI supported. If you specify `-gui=sde` on the command-line or in the .spyglass.setup file, SpyGlass reports a warning that SDE is deprecated.

- Spreadsheet improvements.

  Support for cell-based editing is added so that products can configure each cell individually according to their requirement.

  This avoids erroneous editing of non-editable cells.

- Enhanced the re-drawing of schematic.

  SpyGlass stores user's actions and adds objects in the schematic to make the view as close as possible to the original view.

- Added symbols in schematic to show different strategies present in UPF files.

  - Currently, only level shifters and isolation strategies are shown.
  - From the schematic, you can cross-probe to a UPF file where the corresponding strategy is defined. See the following figure:

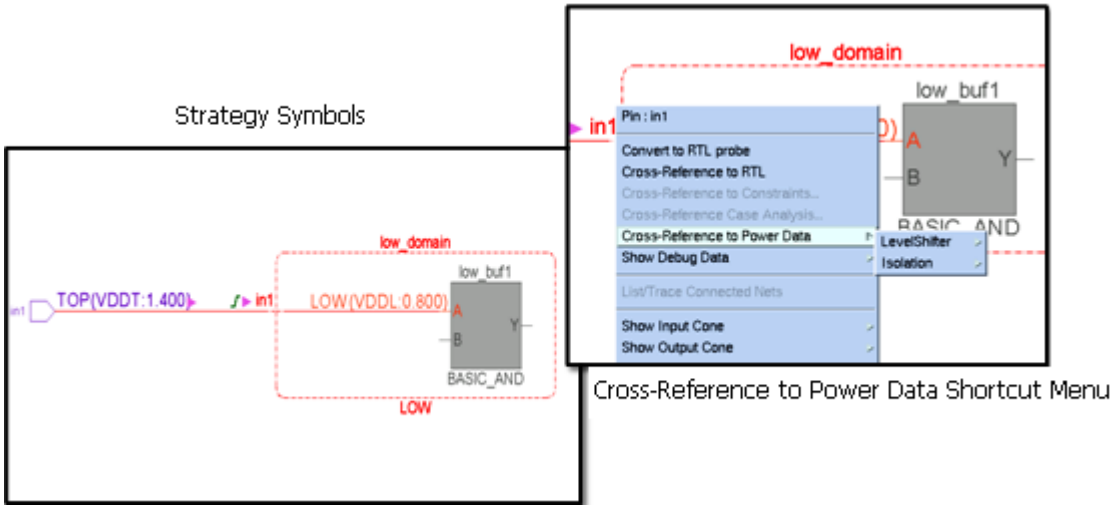

FIGURE 8. Cross-probing to a UPF file

- Enhanced the *DataSheet* report.

  The enhancements are described below:

  - Replaced the existing *Gate Counts* data with more appropriate SpyGlass Physical provided statistics, as shown in the following figure:

Design Statistics Collapse

Statistic	Count
Synthesizable gates (NAND2 equivalent)	70752
Total area	0.1585 mm^2
Registers	4018
Latches	318
Tristates	0

FIGURE 9. SpyGlass Physical provided statistics

In the above figure:

- *Synthesizable gates (NAND2 equivalent)* displays SpyGlass Physical data only.
- *Total area* displays SpyGlass Physical data only.
- *Registers*, *Latches*, and *Tristates* displays SpyGlass Physical or SpyGlass Audits data.

❒ Added new sections to show timing and congestion data from SpyGlass Physical solution. The sample data is shown in the following figures:

Timing Collapse

Clock	Period	Number of Failing Paths	Maximum Logic Levels
clk	2.500 ns	0	0

FIGURE 10. Timing data

Congestion Collapse

Module Name	Hierarchical Instance Name	Standard Cell Count	Internal Congestion Score	Peripheral Congestion
tpcc_piu_GlueLogic	I_tpcc_piu	10112	10.00	High
tpcc_piu	I_tpcc_piu	13403	7.10	High
tpcc_core	I_tpcc_core	26939	4.97	Low

FIGURE 11. Congestion Data

■ Enhanced the *DashBoard* report.

The enhancements are described below:

❒ Made the following improvements in the *CDC* section:

- This section shows failed properties in addition to the synchronization coverage data, as shown in the following figure:

CDC	Completed	Synchronization coverage = 45% (318/704)		Synchronization coverage > 90%	
	Completed	Failed properties = 5% (6/119)		Failed properties = 0%	

FIGURE 12. The CDC section showing default items

- When you run the goals of the SpyGlass CDC solution, SpyGlass extracts additional partially-proven properties and average and minimum depth of the partially-proven properties. You can display these properties optionally in the report.

  By default, these optional properties do not appear in the report unless you set the success criteria for these properties.
  You can set additional variables in addition to the default items, as shown in the following example:

  ```
  set_design_objective CDC -criteria
  {synchronization_coverage>90%,cdc_failed_properties
  =0%,cdc_partial_proven_properties<20%,
  cdc_average_depth<10,cdc_minimum_depth>5}
  ```

  When you include the optional items (last three items in bold in the above example), the overall *CDC* section appears like the following:

CDC	Completed	Synchronization coverage = 45% (318/704)		Synchronization coverage > 90%	
	Completed	Failed properties = 5% (6/119)		Failed properties = 0%	
	Completed	Partially-proven properties = 45% (54/119)		Partially-proven properties < 20%	
	Completed	Average depth of partially-proven properties = 107		Average depth of partially-proven properties < 10	
	Completed	Minimum depth of partially-proven properties = 5		Minimum depth of partially-proven properties > 5	

FIGURE 13.

- ❒ Added the metrics of the SpyGlass Advanced Lint solution in the report.

- If SpyGlass analysis contains the metrics of the SpyGlass Advanced Lint solution, then by default, the *DashBoard* report shows failed properties and maximum cyclomatic complexity metrics. This is shown in the following figure:

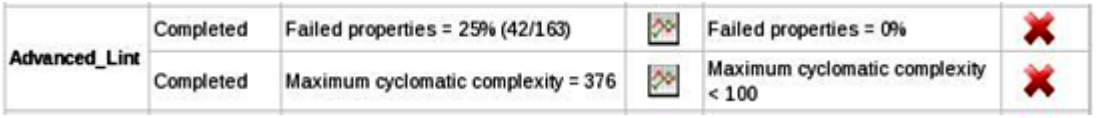

FIGURE 14. The default items from the SpyGlass Advanced Lint solution

- Similar to the *CDC* section, SpyGlass extracts optional items, such as partially-proven properties and average and minimum depth of partially-proven properties that you can optionally display.

  You can set optional variables in addition to the default items, as shown in the following example:

```
set_design_objective Advanced_Lint -criteria
{advanced_lint_failed_properties=0%,
advanced_lint_partial_proven_properties<20%,
advanced_lint_average_depth>25,
advanced_lint_minimum_depth>10,
maximum_cyclomatic_complexity<100}
```

  When you include the optional items (last three items in bold in the above example), the overall *Advanced_Lint* section appears like the following:

FIGURE 15.

- Added the SpyGlass Physical section in the report.

  By default, the following items appear in this section, provided the data for these items is available from SpyGlass analysis:

  - Total area
  - Synthesizable gates (NAND2 equivalent)
  - Registers
  - Number of congested module instances
  - Number of timing paths failing in core
  - Number of timing paths failing on periphery

  The following optional items appear by explicitly their setting success criteria:

  - Latches
  - Tristates
  - Top module congestion
  - Maximum logic levels in core
  - Maximum logic levels on periphery
  - Timing slack in core
  - Timing slack on periphery
  - Floorplan timing slack on periphery
  - Floorplan timing slack in core

- Added the ability to hide certain sub-design objectives.

  In addition to the capability of hiding a product from the report, you can also hide certain sub-design objectives within a product.

  Specify such objectives by using the `-item <list>` argument of the `hide_design_objective` command in the success criteria file, as shown below:

  ```
  hide_design_objective <CDC/Power/DFT/ Constraints>
  [-item {item_list}] [-top {<top_list>}]
  ```

- Made other enhancements, as described below:

- The summary line of the *Quality Goals* section shows *Failed Goals* instead of *Fatal=0,Error=0* to make it in sync with the *Design Objectives* section where *Failed Objectives* is shown.
- If a particular goal run resulted in a fatal violation, the summary line of the *Quality Goals* section shows *FATAL* in the *Run Status* column. Earlier, it showed *Not Complete*.
- If you do not set a success criteria in the *Design Objectives* section, the report now does not show the  icon in the *Pass/Fail* column.
- If you do not set a particular success criteria and SpyGlass analysis did not generate the corresponding default display item, the report does not show the corresponding entry of that item.
- The `set_design_objective` command is enhanced to accept the new success criteria value `display_only`. Set this value if you do not want to compare the value produced by SpyGlass analysis for certain objectives, but just want to show them in the report.

  The following command sets the respective power objectives as *Display Only* items:

  ```
  set_design_objective Power -criteria
  {switching_power=display_only,total_power=
  display_only,leakage_power=display_only
  ```

- Waivers are considered for the content of design objectives, if the waivers are applicable as a part of original analysis.

  For example, *CDC Synchronization coverage*, *Failed Properties*, and *Partial Proven Properties* are influenced by waivers.

  Any waivers created and applied in the GUI after the original analysis are not considered until the next SpyGlass analysis.

Atrenta Products

This section describes the enhancements to the Atrenta products.

Base SpyGlass

The following enhancements are made in Base SpyGlass:

- The `block_profile` GuideWare goal shows correct file path in the Audit.rpt report.
- Added support for multi-line in messages of the following rules for easy debugging:

Verilog	W552	W553	W415a
	DuplicateCase-ML	STARC-2.1.3.1	STARC-2.8.1.6
Verilog+VHDL	STARC05-2.8.1.3		

- Added support for the `checkfullbus` parameter in the following rules:

W120	W528	UnUsedFunctionInput-ML

  Set this parameter to `yes` to report signals that are completely unused.

- Hierarchy format for rules reporting hierarchy information is made consistent.

  Following is the new hierarchy format:

  `Hierarchy: '<hierarchy_path>']`

  The following rules are impacted by this change:

Product Name	Rules
SpyGlass lint solution	W415a, W453, W110, W122, W163, W328, W456, W456a, W488, W552, W553, W66, W69, W88, W107, W116, W120, W123, W156, W159, W162, W224, W263, W314, W316, W362, W423, W446, W468, W484, W486, W497, W498, W502, W563, W164c, W259, W86, W110a, W17, W111, W240, W241, W71, W287a, W287c, W494, W495, W528, W395, W164a, W164b
SpyGlass OpenMore solution	NotInSens, NotReqSens, ArrayIndex

Product Name	Rules
SpyGlass morelint solution	AsgnOverflow-ML, SigAssignX-ML, SigAssignZ-ML, NoBitArray-ML, IfWithoutElse-ML, SensListRepeat-ML, RegInputOutput-ML, NonConstReset-ML, SynthElabDuName-ML, DisallowCaseX-ML, DisallowCaseZ-ML, DisallowXInCaseZ-ML, SelfDeterminedExpr-ML, PartConnPort-ML, SetBeforeRead-ML, SigAssignX-ML, SigAssignZ-ML, GenvarUsage-ML, UnUsedFunctionInput-ML
SpyGlass STARC solution	STARC-3.2.3.2, STARC-2.1.3.1, STARC-2.1.3.2, STARC-2.1.5.3, STARC-2.1.6.1, STARC-2.2.2.1, STARC-2.2.2.2, STARC-2.3.3.1, STARC-2.3.3.2, STARC-2.3.4.1, STARC-2.6.2.2, STARC-2.8.2.1, STARC-2.8.3.1, STARC-2.8.3.4a, STARC-2.8.3.4b, STARC-2.10.3.1, STARC-2.10.3.2a, STARC-2.10.3.2b, STARC-2.10.3.2c, STARC-2.10.5.1, STARC-2.10.6.1, STARC-2.10.6.5, STARC-1.1.1.8, STARC-1.1.1.11, STARC-2.5.1.5a, STARC-2.9.1.1, STARC-2.9.2.1, STARC-2.9.2.2, STARC-2.10.1.5c
SpyGlass STARC 2002 solution	STARC02-2.8.2.1, STARC02-2.2.2.2a, STARC02-2.2.2.2b
SpyGlass STARC 2005 solution	STARC05-2.1.3.1, STARC05-2.1.6.1, STARC05-2.3.4.1, STARC05-2.6.2.2, STARC05-2.8.2.1, STARC05-2.8.3.4a, STARC05-2.10.3.1, STARC05-2.10.5.1, STARC05-2.10.6.5, STARC05-2.10.8.2, STARC05-2.10.8.3, STARC05-1.1.1.8v, STARC05-2.5.1.5b, STARC05-2.10.3.1v

- Added support for *Case-Inside* and *Foreach* in the following rules:

W499	W123	W414	W496a	W215	W216	W289
W496b	W342	W343	W467	W19		

- Enhanced the new width flow.

  The enhancements are described below:

  - The `new_flow_width` parameter is enabled by default.

    Therefore, all fixes made in width-related rules from the SpyGlass 4.5.0 release onwards are enabled.

- Enhanced the *W164a* rule with the following changes:
  - In a concat operator, the width of expression containing 'constant' should be taken at least 32 bits if its natural width is less than 32 bits, with the condition that expression is not the first element of the concat operator.

    For example, for {a,(b + 128)}, width of (b + 128) should be at least 32 bits because of 128.

    Similarly, for {(b + 128),a}, width of (b + 128) should be its natural width, as (b + 128) is the first element.
  - Valid sign extensions by using $signed in multiplication operation are considered only as sign extension, and extra width value is not added.
- Enhanced the *STARC-2.10.6.1* rule.

  No overflow is generated for a valid sign extension concat expression in a binary operator. Consider the following example:

```
wire signed [5:0] a,b;
wire signed [6:0] c;
assign c = {a[5],a} + {b[5],b};
```

  In the above expression, both operands of the binary operator are valid sign extension expressions. Therefore, there is no overflow in this case.
- Added support for the new parameter check_unsign_overflow in the *W164a*, *W164b*, *STARC-2.10.3.2b*, *STARC02-2.10.3.2b*, and *STARC05-2.10.3.2b* rules.

  Set this parameter to yes so that violations for *unsigned signals* due to a valid *sign extension* are not suppressed, as shown in the following example:

```
wire signed [6:0] out;
wire [5:0] a,b;
assign out = {a[5],a} + {b[5],b}; //expression is
                                  //unsigned.
```

- Enhanced the *STARC-2.10.6.1* and *W484* rules.

  In a binary expression having at least one concatenation expression, overflow is not generated if the number of continued streams of 0's in the right of the concat expression is greater than the width of the other

operand.

SpyGlass ERC Solution

This section describes the enhancements to the SpyGlass ERC solution.

Modified Rules/Parameters/Constraints

- Enhanced the *FloatingInputs* rule.

  This rule now does not report a violation for the SpyGlass-generated buffer whose input is undriven.

SpyGlass Lint Solution

This section describes the enhancements to the SpyGlass lint solution.

Modified Rules/Parameters/Constraints

- Added support for the `not_used_signal` parameter in the *W528* rule.

  Use this parameter to specify a list of signals for which this rule should not report a violation.

- Added support for interfaces and packages in the *W193* rule.
- Enhanced the *W504* rule.

  This rule now does not report violations for SystemVerilog integer ports.

- Added support for the `check_initialization_assignment` parameter in the *W415a* rule.

  Set this parameter to `yes` so that this rule does not report a violation for `initialization` and `assign` statements.

SpyGlass morelint Solution

This section describes the enhancements to the SpyGlass morelint solution.

Modified Rules/Parameters/Constraints

Enhanced the *NoGenLabel-ML* rule.

This rule now does not report violations for:

- Duplicate labels of the same `if-else` branch.

- Duplicate labels of case items within the same `case` statements.

SpyGlass OpenMore Solution

This section describes the enhancements to the SpyGlass OpenMore solution.

Added Rules/Parameters/Constraints

- Added the following parameter:

Parameter name	Description	Used By
ignore_iopad	Specifies if violations should be reported for combinational loops that traverse input and output terminals of a pad cell	CombLoop

Modified Rules/Parameters/Constraints

- Enhanced the *RegOutputs* rule.

  This rule now does not report violations for top-level ports that act as a clock or reset inside a design.

SpyGlass simulation Solution

The following enhancements are made to the SpyGlass simulation solution.

Added Rules/Parameters/Constraints

- Added the following rule:

Rule Name	Purpose
sim_loop01	Detects simulation loops in designs

SpyGlass STARC/STARC2002/STARC2005 Solution

This section describes the enhancements to the SpyGlass STARC/ STARC2002/STARC2005 solution.

Added Rules/Parameters/Constraints

- Added the following parameter:

Parameter name	Description	Used By
check_var_in_condition	Specifies if violations should be reported for variables used inside a condition of if-else, case or while loop, used as a loop index of for loop, or used as array index of a variable	STARC-2.3.2.4

Modified Rules/Parameters/Constraints

- Enhanced the *STARC-2.6.2.2* rule.

  This rule now does not report violations for signals that are assigned in an `always` block in a reset condition and read in the `else` part.

- Added support for the `strict` parameter in the *STARC02-2.10.3.7* rule.

  Set this parameter to `yes` to report a violation for a based number that has all zeros.

- Added support for the `strict` parameter in the *STARC-2.10.3.5* rule.

  Set this parameter to `yes` to report violations for constants used with integer variables.

SpyGlass timing Solution

This section describes the enhancements to the SpyGlass timing solution.

Added Rules/Parameters/Constraints

- Added the following parameter:

Parameter name	Description	Used By
check_mux_select_pins	If set to yes, the LogNMux rule additionally checks for the mux-select line and report violations if the number of select input pins in a LogN MUX is greater than the limit specified by the logmux_max parameter.	LogNMux

SpyGlass Advanced Lint Solution

This section describes the enhancements to the SpyGlass Advanced Lint solution.

Added Rules/Parameters/Constraints

- Added the following rules:

Rule Name	Purpose
Av_complexity01	Reports design characteristics and complexity for all RTL modules and FSMs in a design (cyclomatic complexity)
Av_Info_Case_Analysis	Highlights case analysis information and power ground simulation values in the schematic

Other Enhancements

- Added support for cyclomatic complexity analysis.

  Cyclomatic complexity is a measure of design complexity based on branching analysis.

  A complex RTL is hard to maintain, reuse, and verify. Complex designs also take longer to implement while meeting timing, area, and power budgets.

- Improved FSM recognition.

  Added support to state vector for which multiple assignments are used in an RTL to provide the next state.

- Added the following goals under the adv_lint directory:

audit	fsm	redundancy	xgeneration	verify

SpyGlass CDC Solution

This section describes the enhancements to the SpyGlass CDC solution.

Added Rules/Parameters/Constraints

- Added the following rules:

Rule Name	Purpose
Ac_psync01	Reports synchronized isolation enables
Ac_punsync01	Reports unsynchronized isolation enables
Ac_psetup01	Reports setup issues for isolation enables
Ac_upfsetup02	Reports when appropriate isolation/level shifter strategy on domain element is not specified

- Added the following parameters:

Parameter name	Description	Used By
fa_opt_clock_fsm	Used to optimize user-specified clock periods so that ratio between periods of synchronous clocks can be maintained	
enable_ac_sync_qualdepth	Used to report qualifier name and depth in the .csv files of the Ac_sync_group rules	Ac_sync_group rules

- Added the *Ac_sync_qualifier* report.

  This report shows used and unused qualifiers reported by the *Ac_sync01* and *Ac_sync02* rules.

Modified Rules/Parameters/Constraints

- Improved the quality of results (QoR) of the rules performing functional checks.

  The improvements are described below:

  - There are few partially-proved assertions for all the functional check rules.
  - The *Ac_fifo01* rule reports correct failures in case of uninitialized read/write pointers.
  - Abstraction for the *Ac_datahold01a* rule is added through the `fa_abstract` parameter to improve results.

- Enhanced the *Ac_fifo01* rule to detect more FIFOs due to more accurate block path analysis.
- Added a new failure reason reported by the *Ac_unsync01* and *Ac_unsync02* rules.

  Different domain synchronous resets are not considered for data synchronization checks. Such resets are reported as an unsynchronized source with the following failure reason in the message of the *Ac_unsync01* and *Ac_unsync02* rules:

  `Unsynchronized synchronous reset`

- Enhanced the *Ac_abstract01* rule to add the `-combo no` argument in the generated constraints during abstraction of a block.

  This argument is added when an input port is synchronized inside a block and the `abstract_port/input` constraint is specified for such port.

- Enhanced the *Ac_cdc01a* rule to check for crossings synchronized by the *Synchronizing Cell Synchronization Scheme*.

  Therefore, the *Ac_cdc01b* rule will not check for such crossings now.

- Enhanced the *Clock_sync09* rule.

  This rule now does not report violations for a source that is synchronized multiple times at the destinations having the same qualifier.

  Earlier, this rule reported violations if an enable net, which is directly connected to the destination, is not same.

- Enhanced the *Ac_glitch03* rule with the following changes:

- Updated the severity from *Warning* to *Error* for messages when functional checks are not performed.
- Improved the message for clarity.
- Updated the ordering of the reported failure reasons based on their criticality.

- Enhanced the messages of the *Param_clockreset02* and *Param_clockreset07* rules to make them consistent with Atrenta Console.
- Enhanced the CDC structural rules to consider domains of virtual clocks specified by the `clock` constraint.

  The following enhancements are made in this context:

  - A clock specified by the `clock` constraint with the `-tag` argument, and not the `-name` argument, is considered as a virtual clock.
  - For a virtual clock, a domain specified by the `-domain` argument of the `clock` constraint is considered during CDC analysis.
  - The *Propagate_Clocks* rule reports an informational message for propagated virtual clocks.
  - Appropriate validation checks are performed on virtual clocks.
- Enhanced the *Ac_initstate01* rule to check clocks for primary and black box output only.

  All the other clocks are not considered for functional verification.

Other Enhancements

- Enhanced the SoC (hierarchical) flow with the following changes:
  - Migration of top-down constraints now occurs for all blocks in one go instead of each block at a time.
  - The `-names` and `-inputs` arguments of the `abstract_port` constraint are renamed to `-sync_names` and `-related_ports`, respectively.
  - The new argument `-scope` is added to the `abstract_port` constraint.

    When you specify `-scope cdc`, the `abstract_port` constraints are generated by the SpyGlass CDC solution.

- The following commands are added to specify a directory to save an abstract view (generated SGDC file) of a block:

Mode in which SpyGlass is Used	Command
Atrenta Console GUI	Specify the -block_abstract_directory <directory> command in the *Other Command Line Option(s)* field under the *Set Read Options* tab.
Project File/sg_shell	set_option block_abstract_directory <directory>
Batch	-block_abstract_directory <directory>

  By default, the abstract view is saved in the spyglass_reports/abstract_view/cdc directory.

- It is mandatory to specify block interface information for the blocks used in the SoC flow. You can specify the block RTL from which SpyGlass automatically extracts the block interface information.

- Improved the run-time up to 10% for the rules performing functional checks.

- The default value of the `hier_wild_card` parameter will be changed to `no` in a future SpyGlass release.

  Currently, if the value of the `hier_wild_card` parameter is set to `yes` (default) and you specify wildcard expressions in the `cdc_false_path` constraint, SpyGlass reports the following warning:

```
WARNING - wild-card used in cdc_false_path: Default value of
parameter hier_wild_card will be changed to "no" in next
release to match wild-card specified with explicit
hierarchies only, so you must specify the hierarchies
explicitly (e,g *.*cfg instead of *cfg)
```

- Changed the names and domains of virtual clocks reported in messages and reports.

  For virtual clocks specified on output ports of an abstracted block, SpyGlass modifies the clock names by adding a block instance name as a prefix. This modified name appears in the messages and reports generated by rules reporting such clocks.

A similar enhancement is made for domain names on clock output of an abstract block.

- Added support for power-aware CDC verification.

  Support is added to verify non-instrumented RTL where power intent is captured in the UPF format. This feature enables early verification of CDC issues around an isolation logic at the RTL level. Synchronization checks on the isolation logic are performed before the logic is introduced in the design.

  The *Ac_psync01*/*Ac_punsync01*, *Ac_psetup01*, and *Ac_upfsetup02* rules report synchronized and unsynchronized crossings as well as setup issues. See the following figure:

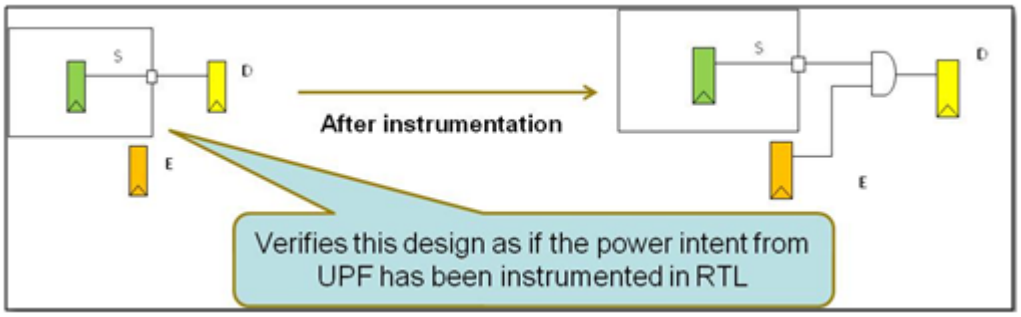

FIGURE 16. Non-instrumented checks

For more details, refer to the *Working with Power Aware CDC Verification Rules* topic of *SpyGlass CDC Rules Reference Guide*.

SpyGlass Constraints Solution

Added support for SDC mode merge.

This feature enables you to optimize your design for each functional mode irrespective of conflicting requirements.

A consolidated SDC file represents a hypothetical mode, which covers all the timing scenarios of individual modes. Merged constraints cannot under-constraint any path or a design object any more than the individual modes. This approach helps drive implementation tools (such as synthesis, static timing analysis, and place route) on a single mode to save runtime.

Currently, only two modes can be merged at a time. This feature is limited to a well-defined set of SDC constructs, as follows:

- `set_case_analysis` and `set_disable_timing`
- `set_input_delay` and `set_output_delay`
- `set_false_path` and `set_multicycle_path`
- `set_min_delay` and `set_max_delay`
- `create_clock`, `create_generated_clock`, and `set_clock_sense`

The mode merge SDC file has comments for each constraint providing traceability to individual modes. Results are reported in the mode merge spreadsheet, showing individual mode constraints, merged constraints, and reasons for merging/dropping. This is shown in the following figure:

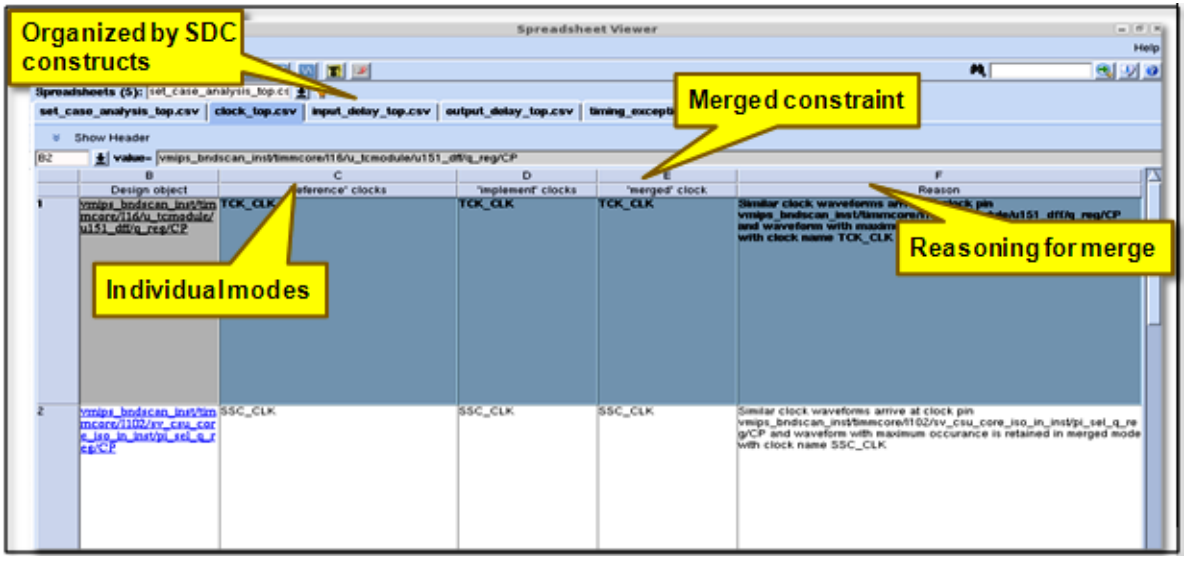

FIGURE 17. Mode merge spreadsheet

Added Rules/Parameters/Constraints

- Added the following rules:

Rule Name	Purpose
SDC_ModeMerge	Generates a merged mode SDC by merging SDC constraints defined in the two different modes
SDC_Methodology70	Verifies specification of the `comment` argument of SDC constraints

- Added the following parameters:

Parameter name	Description	Used By
tc_comments_cmd_file	Specifies the file containing the name of constraints to be checked by the SDC_Methodology70 rule. This rule reports violations if the -comment argument is missing in the constraints in SDC.	SDC_Methodology70
gen_c2cVerify	Enables the SDC_GenerateIncr rule to verify clock-to-clock false paths through the SpyGlass TXV solution.	SDC_GenerateIncr
tc_source_syn_clks	Enables the support for source synchronous clock interfaces.	Clk_Gen02, Clk_Gen08, Op_Del09, Clk_Gen23
equiv_sdc_clock_prefix	Specifies a naming convention for mapping virtual clocks	

Modified Rules/Parameters/Constraints

- Enhanced the *SDC_GenerateIncr* rule with the following changes:
  - Added support for automatic verification of false paths through the SpyGlass TXV solution.

    Formal verification is used to verify false paths and clock uncertainty commands. This capability is controlled by the `gen_c2cVerify` parameter.

Set this parameter to:

- `Yes` to generate false paths/uncertainty for clock crossing pairs after formal verification.
- `No` to continue the current flow of the *SDC_GenerateIncr* rule.

SpyGlass reports results in an easy-to-read spreadsheet, as shown in the following figure:

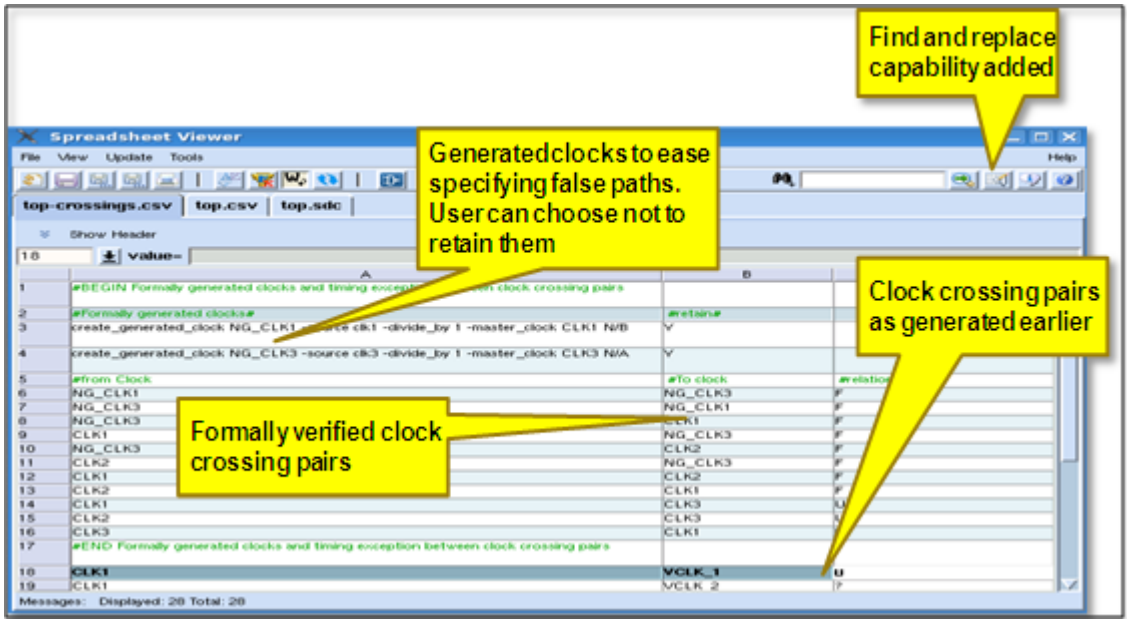

FIGURE 18. Spreadsheet output

- ❒ Added the find and replace functionality in the spreadsheet editor shown in *Figure 18* for pattern based replacements.
- ❒ A new SGDC file is generated for the design containing the output SDC file path. This way, you can review all the constraints in a single file.
- ❒ Added support for the SDC 1.9 version. Therefore, the `comment` field is now supported in the spreadsheet interface for the following SDC commands:

create_clock	create_generated_clock	group_path
set_clock_group	set_false_path	set_max_delay
set_min_delay	set_multicycle_path	

- Added support for an absolute path of a parameter file in the output SDC.
- Added support for `$SPYGLASS_HOME` in the `tech_files_location` variable.
- The '?' symbol now appears to identify generated parameters for which no value is defined.
- The `sdc` extension is automatically applied to the name of an output SDC file.

For details on the above enhancements, refer to the documentation of the *SDC_GenerateIncr* rule in *SpyGlass Constraints Rules Reference Guide*.

- Enhanced the *Clk_Gen02*, *Clk_Gen08*, *Op_Del09*, and *Clk_Gen23* rules to consider source synchronous clocks.

  During SpyGlass analysis, the above rules consider these clocks to avoid false violations. These clocks are used in high performance data transfers. The same clock is used to generate data as well as clock.

  Timing of data signals `DOUT` is referenced to `CLKOUT`, which is generated by the same source `CLKIN`, as shown in the following figure:

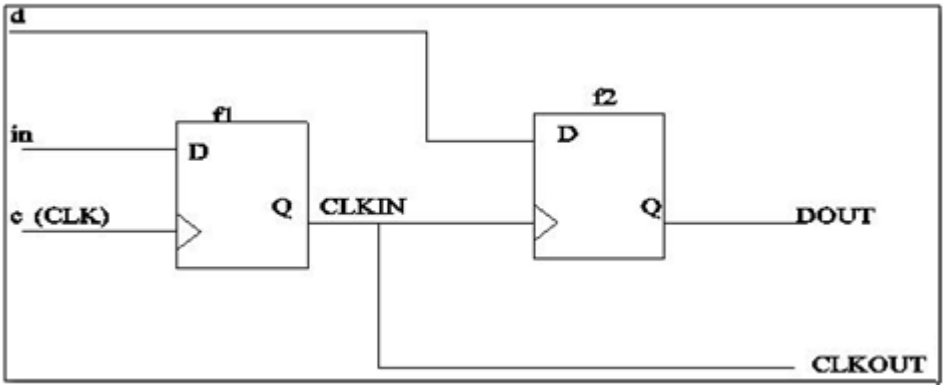

FIGURE 19. Source synchronous interfaces

The specified rules support this interface only if the `source_synchronous_clocks` parameter is set to `yes` (default value).

- Enhanced the *Op_Del09* rule.

  This rule now does not report multiple violations for multiple schemas.

- Enhanced the *Clk_Uncert11* rule to report a violation if inter-clock uncertainty hold value is greater than or equal to the setup value.
- Enhanced the *Inp_Trans01* rule to report violation for blocks specified by using the `chip` parameter.
- Enhanced the *Equiv_SDC* rule with the following changes:
  - During an equivalence check between two SDC files, if the same clocks are propagated through a MUX, the `set_case_analysis` is considered equivalent.
  - Virtual clock equivalence updated.
    - Added naming convention based mapping.
    - Added ambiguous clock based mapping.
    - Mapping is only allowed to a single virtual clock.
    - In-equivalence violation is reported in the same format as that of real clock in-equivalence.

- Added the `equiv_sdc_clock_prefix` parameter to specify a naming convention for mapping virtual clocks.

For details on the above enhancements, refer to the documentation of the *Equiv_SDC* in *SpyGlass Constraints Rules Reference Guide*.

Other Enhancements

- Moved the *Clk_Gen01b*, *Clk_Gen05*, and *Clk_Gen06* rules from the `redundancy_check` goal to the `clock_consis` goal.
- Removed the *Inp_Trans07* rule from the `io_delay` goal.
- Added the new GuideWare goal `domain_check` to check for clock domain consistency.
- Added support for the SoC flow by using abstraction.

  Currently, only GuideWare rules are supported in this flow.

SpyGlass DFT Solution

This section describes the enhancements to the SpyGlass DFT solution.

Added Rules/Parameters/Constraints

- Added the following rules:

Rule Name	Purpose
Clock_26	Reports overwriting of the testclock constraint in the shift or capture mode
Soc_00	Generates an abstract view of a design
Soc_08	Checks if paths between user-specified nodes exist. For all the existing paths, this rule reports an informational message is displayed. For all extra paths or no paths, this rule reports a warning message.

- Added the `require_strict_path` constraint.

  This constraint defines a connectivity check for the path between the two specified pins. For details on this constraint, refer to the *SpyGlass Consolidated Constraints Application Note*.

Modified Rules/Parameters/Constraints

- Added support for automatic back annotation of data in the schematic in the following SoC rules:

Soc_01	Soc_01_Info	Soc_02	Soc_02_Info

- Enhanced the *Soc_05* rule to validate assumptions on an abstract view.

  For details, refer to the *SpyGlass SoC Methodology Guide*.

Other Enhancements

- Use the *TA_09* rule instead of the *TA_01*, *TA_02*, and *TA_06* rules.

  The *TA_09* rule provides a better and consolidated functionality of the above three rules.
- Added support for full SoC flow. For details on this flow, refer to the *SpyGlass SoC Methodology Guide*.

SpyGlass DFT DSM Solution

This section describes the enhancements to the SpyGlass DFT DSM solution.

Added Rules/Parameters/Constraints

- Added the following rules:

Rule Name	Purpose
Info_enabledFlops	Generates a report of enabled flip-flops (sorted on hierarchy) per domain
Atspeed_25	Reports a violation for combinational reconvergence to asynchronous pins of flip-flops
Atspeed_26	Reports overwriting of the `atspeed` clock constraint in the atspeed mode
Atspeed_27	Reports convergence at asynchronous pins of flip-flops

- Added the following parameter:

Parameter name	Description	Used By
dftDsmConvergingPathsLimit	Limits the number of converging paths	Atspeed_27

- Added the following Tcl commands:

Tcl Command	Purpose
dsm_capture_ieee1500_data	Captures results from core to chain
dsm_capture_ieee1500_instruction	Captures results from IR to chain
dsm_read_ieee1500_data	Reads content of a data chain
dsm_read_ieee1500_instruction	Reads content of an IR chain

Modified Rules/Parameters/Constraints

- Added support for automatic back-annotation of data in the schematic in the *Atspeed_12* and *Atspeed_13* rules.

SpyGlass DFT MBIST Solution

This section describes the enhancements to the SpyGlass DFT MBIST solution.

Other Enhancements

- Added support to override a vendor-specified connection with a user-specified connection.
- Automated the clock connection support.

  The `mb_clock_choice` Tcl command is added for this enhancement.
- Added support to perform MBIST insertion for any level of block at any stage.
- Added support for consolidated link resolution in the Tcl top-down flow.

  In the top-down approach, the sources.f file is created at each stage.

  With this enhancement, another sources.f is created at the end of all

stages. This file contains data of all the stages. As a result, you do not have to refer to individual sources.f of every stage.

SpyGlass Power Family

This section describes the enhancements to the SpyGlass Power family.

Modified Rules/Parameters/Constraints

- Enhanced the *PESTR27* rule and the auto_activity.sgdc file to report activity and probability values up to three decimal values.
- Enhanced the *PESAE07* rule to handle asynchronous memories.
- Enhanced the *PESAE06* rule to consider registers with explicit enables.

  This rule will now run in the ESYNTH mode. Earlier, this rule considered instantiated enables only.

Other Enhancements

- Improvements in the activity engine and related rules.

  Enhanced the auto_activity.sgdc file to show the source of activity information.
- Improvements in power reduction results, as described below.
  - Power saving on an average is improved by a factor of two as compare to the previous releases on customer test cases available at Atrenta.
  - Modified the power reduction goals to achieve improved power savings.
- Improved the flexibility of Power Fix.

  The following enhancements are made in this context:
  - Added support to configure power-reduced RTL to adhere to specific rule guidelines of the SpyGlass STARC solution and the SpyGlass lint solution.

    When SpyGlass Power Reduce introduces registers for creating an enable logic, you can choose a register style to be introduced by using the rme_config constraint.

- Added support for controlling which nets to skip while creating enables by using the `set_dont_use_net` constraint.

- Divided the SpyGlass Power Fix flow into two SpyGlass runs.

  This helps in achieving better quality of results in generating power reduced RTL.

- Improved the reliability of Sequential Equivalence Checking (SEC).

  Fast structural checks are added for manually modified RTL to catch errors before performing time-consuming formal checks. These checks include count mismatch for registers, output ports, and multiple drivers.

  For automatically modified RTL, SEC may fail on certain registers in rare cases. To regenerate the RTL with the changes on such removed registers, a second pass flow is added. This improves stability by trading off a bit of power reduction.

- Disk space and performance improvements, as described below:

  - Significant reduction is achieved in the disk space requirement by reducing the dump file size.
  - Significant improvement is achieved in performance of SEC due to clock abstraction.

SpyGlass Power Verify Solution

This section describes the enhancements to the SpyGlass Power Verify solution.

Added Rules/Parameters/Constraints

- Added the following rules:

Rule Name	Purpose
UPF_lowpower15	Reports multi-supply cells with missing connect_supply_net command
UPF_lowpower16	Reports multi-supply cells with missing create_supply_set command
LPPLIB19A	Reports when a bias supply net connected is less always-on with respect to a power supply net

- Added the following parameter:

Parameter name	Description	Used By
lp_check_same_voltage_path	Enables the LPLSH04 rule to report all strategies in the same voltage path as redundant	LPLSH04

- Added the lp_mutli_supply_instance.rpt report generated by the *UPF_lowpower15* rule.

  This report contains multi-supply instances with missing `connect_supply_net`.

Modified Rules/Parameters/Constraints

- Enhanced the *LPLSH04* rule to report violations for redundant level shifter rules/strategy found on the same voltage path only when there is more than one such strategy.

  Set the *lp_check_same_voltage_path* parameter to `yes` to report all strategies present in the same voltage path as redundant.

- Added support for schematic abstraction in the following rules:

LPSVM26	LPSVM40	LPISO04	LPISO05	LPPSW02
LPPSW03	LPPSW04			

  The Atrenta Console GUI is enhanced to support schematic abstraction for the above rules.

- Improved schematic highlight (in the *Incremental Schematic* window) for the *LPPLIB04* rule.

Other Enhancements

- Added the UPF 2.0 support.

  The enhancements corresponding to this support are described below:

  - Added support for the `-diff_supply_only`, `-source`, and `-sink` argument of the `set_isolation` command.

As a result, all isolation rules are enhanced to consider these arguments as well. This is explained in the following example:

```
# Select only connections to certain path using -source/
# -sink domain
set_isolation S1 -domain DA -sink SS_DB


#Strategy would not be applicable if the source
#and sink work at same supply
set_isolation S2 -domain DA -sink SS_DC
-diff_supply_only true
```

- Added support for bias net checking.

  Bias supply should be ON if the main supply is ON. The *LPPLIB19A* and *UPF_lowpower16* rules are added to perform bias net related checks, as shown in the following example:

  ```
  #Check the bias pin connection to correct bias supply net
  create_supply_set  SS1 -function {VDD power} /
  -function {VDDBIAS nwell}
  ```

- Added support for schematic cross-probing to UPF.

  Isolation and level shifter strategies appear on domain boundaries. This enables you to cross-probe the strategies from the schematic to UPF file, as shown in the following figure:

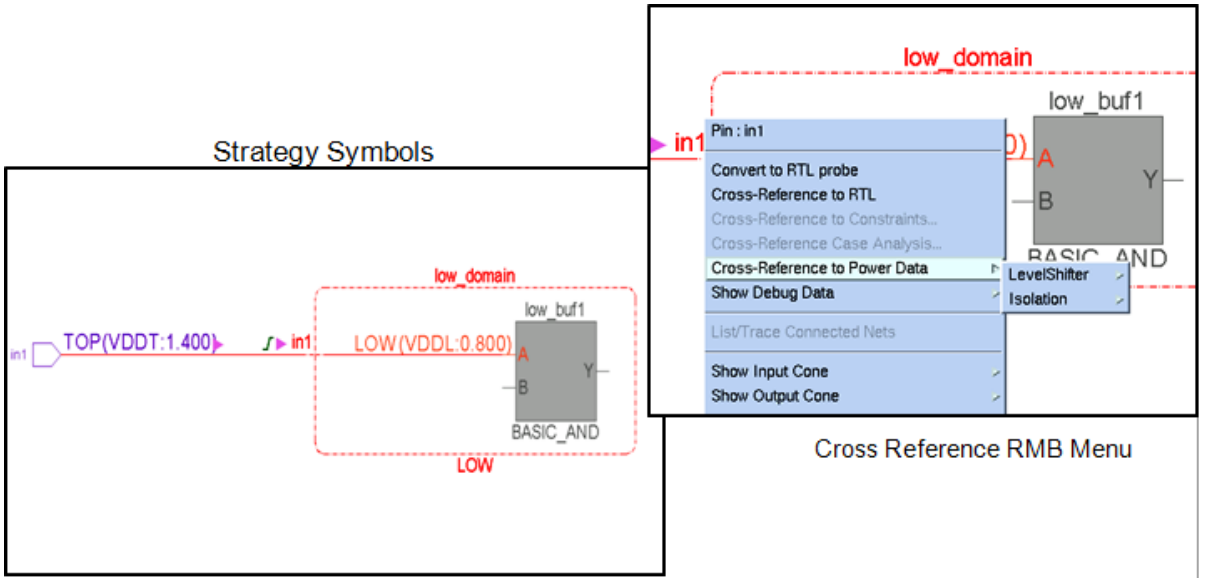

FIGURE 20. Cross-probing from schematic to UPF

- Renamed the value `jaguar` to `du` of the `sortmethod` option.

  SpyGlass reports a warning if you set the value of this option to `jaguar`.

SpyGlass Physical Base Solution

This section describes the enhancements to the SpyGlass Physical Base solution.

- Added the logical congestion debug GUI.

  This debug GUI is added to present the congestion report in a graphical manner. This way, you can understand the result intuitively and also debug the same to determine the root cause of a problem in the RTL structures.

  These enhancements cover both internal congestion and peripheral congestion.

  The following figure shows the sample debug GUI:

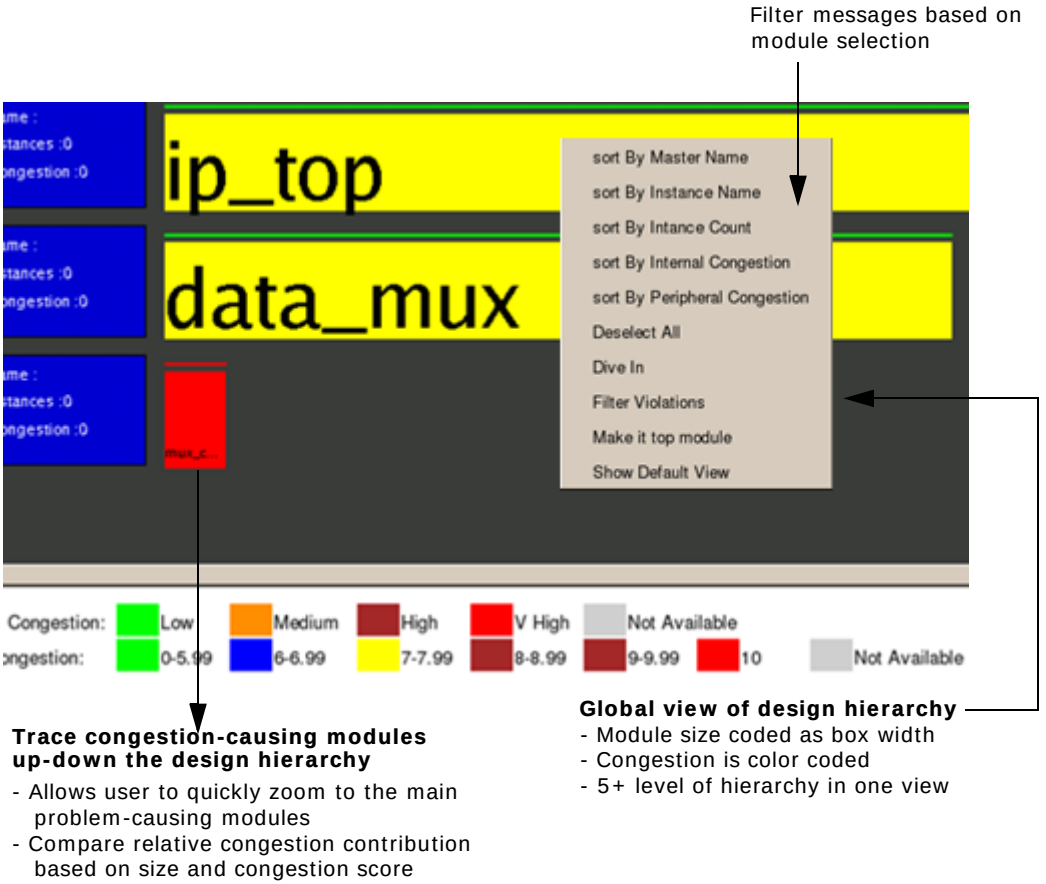

FIGURE 21. Debug GUI

- You can generate histograms for the following rules:
  - *PHY_FaninCone*
  - *PHY_FaninCone_MM*
  - *PHY_FanoutCone*
  - *PHY_FanoutCone_MM*

  To generate a histogram, click the histogram icon in the spreadsheet. The X-axis in the histogram is the respective node number from the

spreadsheet and the Y-axis is the fan-in or fan-out value.

The following figure shows the sample histogram:

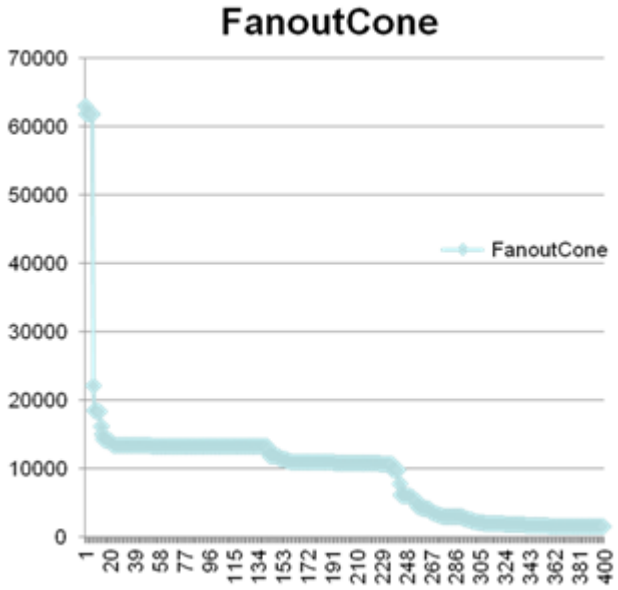

FIGURE 22. Histogram

- Added support for the save-restore feature in the SpyGlass Physical Base flow.

  Use the `phy_enable_restore_mode` parameter to enable or disable this feature.

  By default, this parameter is set to `false`. In this case, the SpyGlass Physical Base solution saves the design database of the current run.

  In the subsequent runs, you can set this parameter to `true` if there is no change in the input data. This will restore the design database stored in the previous session and will run the selected rules on the restored database, thereby saving a lot of time.

- The SpyGlass Physical Base solution is integrated with and supported on the *IP Kit*.

  The SpyGlass Physical Base solution provides data for *Area*, *Timing*, and *Congestion* for the *IP Kit* datasheet and dashboard.

Added Rules/Parameters/Constraints/Goals

- Added the following rule:

Rule Name	Purpose
PHY_Dashboard	Generates the Dashboard and Datasheet metrics.

- Added the following parameters:

Parameter name	Description	Used By
phy_enable_restore_mode	Enables or disables the save-restore mode.	All rules
phy_criticalobjects_logicdepth_mode	Selects a variant of a logical depth rule to be used for critical object calculation.	PHY_CriticalObjects
phy_clockdetail_core_threshold	Identifies the grossly failing core paths.	PHY_ClockDetail
phy_clockdetail_peri_threshold	Identifies the grossly failing peripheral paths.	PHY_ClockDetail
phy_gatearea_threshold	Specifies the maximum threshold for the total gate area of a design.	PHY_GateArea
phy_gatecount_threshold	Specifies the maximum threshold for the total gate count of a design.	PHY_GateCount
phy_report_clockdomain_crossing_paths	Specifies whether the timing paths in a clock domain crossing should be considered.	PHY_ClockDetail, PHY_LogicDepth*, and PHY_Timing

- Added the following goals:

Goal Name	Purpose
physical_analysis_genericlib	Runs the selected SpyGlass Physical Base pre-floorplan rules by using the SpyGlass Physical Base generic library. These rules report violations pertaining to the area, timing, and congestion aspects of an RTL design.
physical_analysis_congestion	Runs the selected SpyGlass Physical Base pre-floorplan rules by using the specified vendor library to analyze and debug the congestion aspects of an RTL design.
physical_analysis_signoff	Runs the selected SpyGlass Physical Base pre-floorplan rules by using the specified vendor library to sign-off for area, timing, and congestion aspects of an RTL design.

Modified Rules/Parameters/Constraints/Goals

- Changed the default value of the `phy_enable_hbo` parameter from `false` to `true`.
- Fine-tuned the default values of parameters for different goals to generate more meaningful reports.

Deprecated Rules/Parameters/Constraints/Goals

Deprecated the `physical_analysis_prefloorplan` goal.

This goal will be completely removed from the SpyGlass 5.0 release.

Use the `physical_analysis_signoff` goal in place of this goal.

SpyGlass TXV Solution

The SpyGlass TXV solution is substantially changed in this release.

For any deployment of this release, it is recommended to contact Atrenta.

See the following figure for highlights of the enhancements to the SpyGlass TXV for this release:

	What has changed	What has not
Verification	• New MCP verification flow • Added support for set_clock_groups	• No change in FP verification • No change in glitch check
Generation	• Generate set_clock_groups	• No change in C2C FP generation
Setup	• New domain computation (beta)	• Default setup unchanged
Reporting and debug	• New centralized report pointing to detailed reports • Removed all old rules – only two rules for FP/MCP verification • MCP spreadsheet improvement based on new verification flow	• No change in FP debug
STA-flow	• Removed MCP identification which was under option	• No change in FP identification

FIGURE 23. Highlights of changes to the SpyGlass TXV solution

Added Rules/Parameters/Constraints

- Added the following rules:

Rule Name	Purpose
Txv_FP01	Performs FP verification
Txv_MCP01	Performs MCP verification
Txv_DomainConflict	Reports conflicts while inferring domain
Txv_DomainMissing	Reports missing domain information
Txv_DomainMatrix	Checks overall clock/domain matrix
Txv_SCG01	Verifies the set_clock_group command

- Added the following parameters:

Parameter name	Description	Used By
txv_mcp_max_reported_paths	Sets the number of paths per enable of a MCP that will be displayed in the detailed spreadsheet report	Txv_MCP01
txv_group_mcp_paths	Groups reported paths of an enable in detailed spread sheet	Txv_MCP01
txv_mcp_clock_enable	Allows verification assuming enable is embedded in clock path	Txv_MCP01
txv_max_partition_per_constraint	Controls the maximum limit of enable per MCP for functional verification	Txv_MCP01
txv_mcp_exit_at_first_failure	Exits verification at the first failure for an MCP	Txv_MCP01
txv_extract_domain	Selects a mode in which domain will be inferred	Txv_DomainConflict, Txv_DomainMissing, Txv_DomainMatrix
new_domain_flow	Enables the new domain flow	Txv_FP01, Txv_MCP01
txv_mcp_detect_hier_cg	Detects an enable across module boundaries	Txv_MCP01
txv_mcp_enable_at_fast_side	Considers enable only at the first side for first to slow or slow to first type of MCPs	Txv_MCP01

Modified Rules/Parameters/Constraints

- Enhanced the *Txv_C2C_Fp* rule to generate the `set_clock_groups` constraint along with the `clock` to clock `set_false_path` constraints.

Deprecated Rules/Parameters/Constraints

- Removed all rules from the SpyGlass TXV solution. Functionality of all these rules is covered by the new rules *Txv_FP01* and *Txv_MCP01*.
- Removed the following parameters:
  - `txv_mcp_check_source_toggle`
  - `txv_verify_mcp_path_high_effort`
  - `txv_mcp_verify_incompletes`

Other Enhancements

- Added a new enabled-based flow for MCP verification

  This flow improves QoR, performance, and debug capability and is less sensitive to initialization.

  This flow has replaced the earlier data path based MCP verification.
- Combined all reports in the single report, txv.rpt. This centralized report points to all the detailed reports.

  Information in this report includes:
  - Major options used while running the SpyGlass TXV solution.
  - Setup information about clocks, resets, initialization, etc.
  - A summary of exception verification results.
  - An accurate count of exceptions (include MCPs with parse errors).

  The following figure shows the sample report:

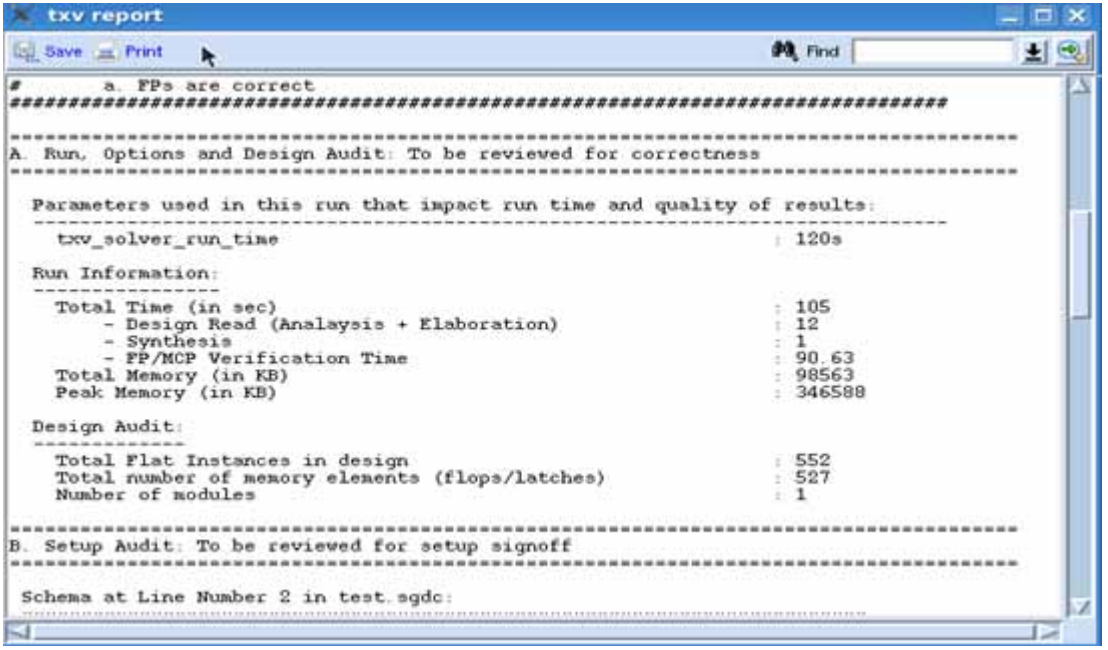

FIGURE 24. Sample SpyGlass TXV report

- Added support for two-level spreadsheets to display MCP-related violations, that is, violations related to `set_multicycle_path` constraints.

  The first level spreadsheet is a summary spreadsheet that contains violations related to different `set_multicycle_path` constraint specifications. When you click on a particular violation in this spreadsheet, another spreadsheet appears displaying details of the selected violation.

  Other spreadsheet improvements include:

  - ❒ One line per user MCP regardless of the result or number of paths.
  - ❒ List of initialization rate per MCP - easier to decide QoR.
  - ❒ One line per partition (enable detected by SpyGlass) - may cover many paths.
  - ❒ Results of analysis for each partition (enable).

For more details, see *Figure 25* and *Figure 26*.

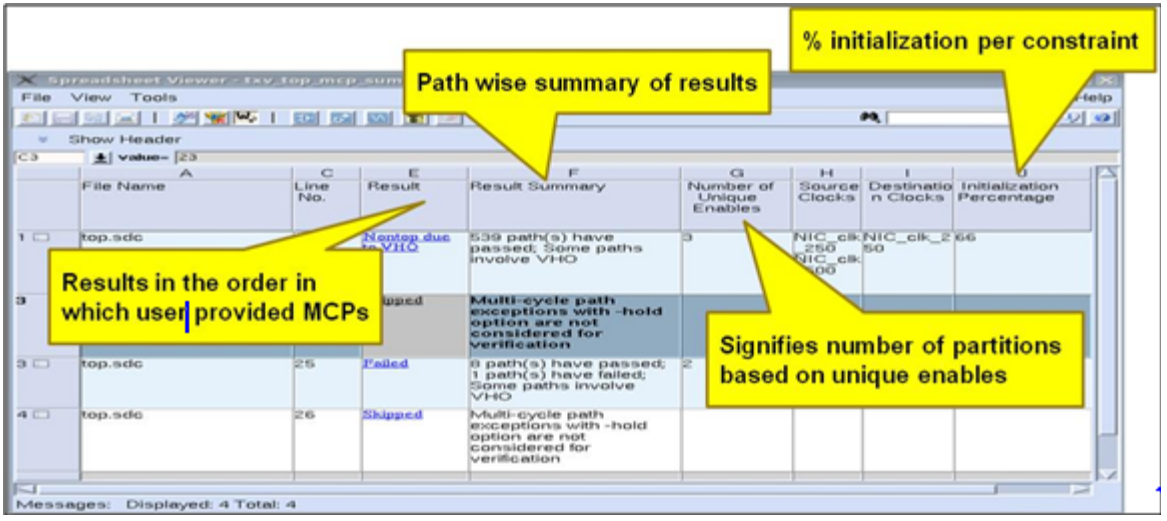

FIGURE 25. SpyGlass TXV spreadsheet improvements - I

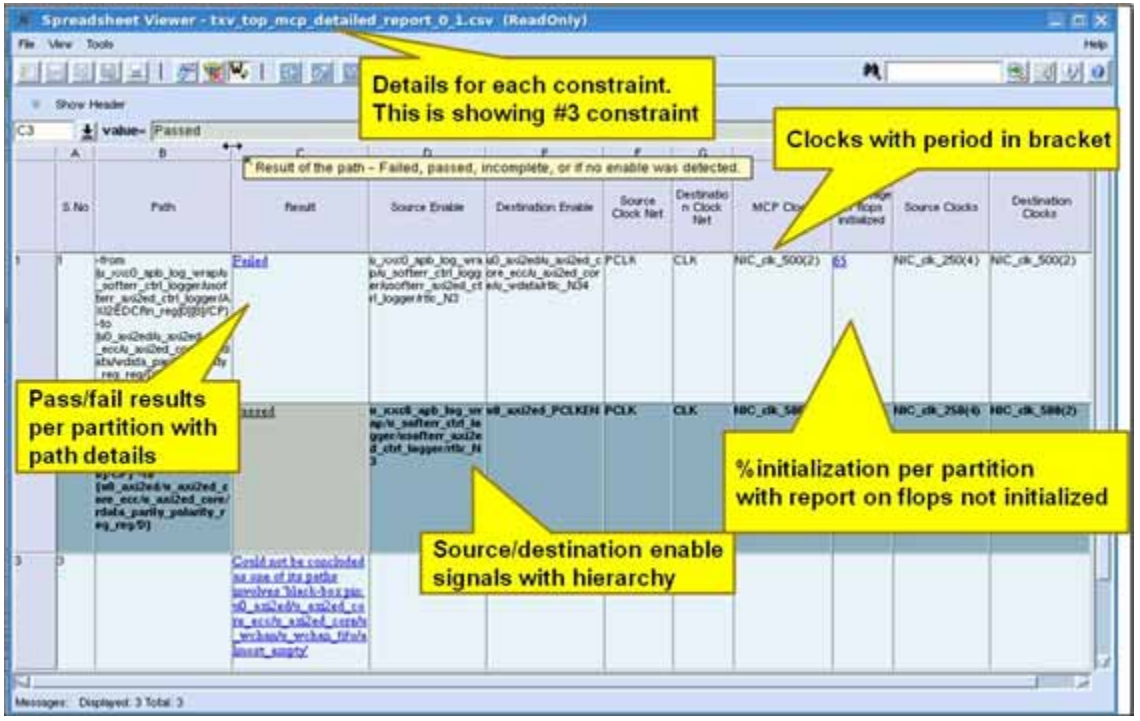

FIGURE 26. SpyGlass TXV spreadsheet improvements - II

- Added the new domain computation flow. This flow contains the following three modes:
  - STA compliant mode: Interprets FP/SCU/SCG to come up with domain information.
  - STRICT mode (Recommended): You must specify all clocks in a single `set_clock_groups -asynchronous` command and ensure there is no ambiguity in this command.
  - SGDC mode: Reads domains from SGDC files.

  The *Txv_DomainConflict*, *Txv_DomainMissing*, and *Txv_DomainMatrix* rules are added as a part of the new domain computation flow.
- The `set_clock_group` is now verified by the SpyGlass TXV solution.
- The SpyGlass TXV solution does not support MCP in the STA flow.

- Introduced the abstraction of clock tree logic to help the completion of verification for designs with complex clock trees.
- With the new SpyGlass TXV flow, there is significant reduction in SpyGlass TXV run time. However, for single path MCPs, the run time can increase.

Documentation

Considerable changes have been made to the SpyGlass help set. The following table briefly describes the changes:

Added Documents	SpyGlass_SoCMethodology_UserGuide.pdf
	SpyGlass_ReleaseSummary.pdf
	SpyGlass_MBISTMethodology_UserGuide.pdf
Renamed Documents	SpyGlass_AutoVerifyRules_Reference.pdf renamed to SpyGlass_AdvancedLintRules_Reference.pdf
	SpyGlass_AutoVerifyMethodology_UserGuide.pdf renamed to SpyGlass_AdvancedLintMethodology.pdf
Removed Documents	SpyGlass_IPWaivers_AppNote.pdf Relevant content from this document is moved to the Waiving Messages topic of Atrenta Console User Guide.
	SpyGlass_WaiversFilters_AppNote.pdf Relevant content from this document is moved to the Waiving Messages topic of Atrenta Console User Guide.
	SpyGlass_RegExpr_AppNote.pdf Relevant content from this document is moved to the Using Regular Expressions and Wildcard Characters topic of Atrenta Console User Guide.
	SpyGlass_WhatsNew.pdf The SpyGlass_ReleaseSummary.pdf document introduces the top-level features of the new release and replaces the SpyGlass_WhatsNew.pdf document.
	SpyGlass_SDEToConsole_AppNote.pdf

List of Incidents Fixed in the SpyGlass 4.7.0 Release

VI #	EW #	Title
20470	16339, 24713	Inconsistency in Hierarchy messages
28107	25352, 74343	Ac_cdc04 should be enhanced for AND gate synchronization
40134	70427, 83175	set_case_analysis in Equiv_SDC_Dual_Design
42268	71494	Total execution/ run time to be reported explicitly in spyglass.log
45678	74379	Specify period for virtual clock
45686	74380, 75158	While saving the .prj file, "projectcwd" & "current_methodology" should be saved with relative path
47185	75509	Generate report of multi supply instances in design
48832	76536	Memory Lib power different between third party tool and SpyGlass
50221	77243	{ENH} When something functional has been altered should the project file be requested to be save
50683	77466	disable popup windows when GUI starts
51097	77683	Erroneous detection of changed project file
51136	77613	SpyGlass IS view should provide the capability to view the content of the liberty file
51137	77614	SG IS view (with power view enabled) does not save the logic expanded
51378	77851	[Enh]: Enhancement for report capability about flip flop for each clock domain
51415	77861	[Enh] : Need message for overwrite for clock constraint in sgdc
51776	77991	Add a feature of manual interruption while schematic takes times to load
51881	77615	Enhancement request to change the font size of the text in schematic viewer
51922	78166	'LogNMux' missing violation case
52161		Usability: Remove need to specify language (remove need to specify verilog, vhdl, mixed)

VI #	EW #	Title
52461	78448	{ENH} Need enhancement to provide relationship between the real & virtual clock in sgdc file!
52570	78003	Deprecate FLATDU2_WOL rules as Spyglass is doing flattening twice
52606	78550	Enhance LPPLIB04 / LPPLIB07 message and schematic
52636	78560	Flag a message in log file or at screen output if any template is not found while reading the order file
53182	79030	{ENH} A way to avoid the popups saying " following rules or rule groups are no longer used by the policies"
53555	83462	Need a switch to flag Elab Error for Zero Size Multi-Concat expressions
53574	79091	{ENH} Add a parameter to ignore comb loop through IO pad
53649	79339	stop doc in Console shows SDE examples
53684	79360	Report viewing enhancements
53876		sg_shell: issue around custom report generation
53943	79466	SEC_FATAL2 doesn't create a violation in the msg tree
54088	79501	spyglass -showgoal option should not require -batch option
54544	85097	false UPF_lowpower09 pointing out that this supply port is connected to more than one supply netF f
54695	79907	Incremental GenSDC : Default value in crossings file should be "F"
54975	79957	Incorrect Waveform
55097	80079, 80933, 82687	False Clock_sync09 violations
55351	85147	Audit2FileNameDump needs to be added in the rtl_handoff/audit/block_profile template
55650	80416, 88078	Support of IEEE protected HDL files
55651	80416	Support of IEEE protected HDL files
55902	80589	“enable/disable power view” leads to schematic redraw
55946	80593	[Enh] :: Allow generate if without labels if no instances generated
55948	80590	[Enh] :: capability to open liberty file from the schematic

VI #	EW #	Title
56056		SoC CDC: Top down constraints migration should migrate all blocks in single run
56380	80380, 82112	In the case of using generate, rule checking should not happen inside `else when the condition is matched for `if
56564	80905	Txv MCP High Effort does not detect enable logic
56605	80862	[Enh] :: RegOutputs should not report on clock outputs
56804	80970	Add support of specifying virtual clock as synchronized with another real clock
56974	80588	Enh: To maintain the schematic when changes are done in the preferences (In Incremental schematic Mode)
57051	81150	False W164 violation when sign extension is done in a $signed function
57058	81127	[Enh] :Enhancement request to check reset tree with Atspeed_22
57114	81179	Enh: For UnUsedFunctionInput-ML Rule
57128	81183	STARC02-2.10.3.7 and STARC05-2.10.3.7 do not flag 1'b00
57457	80066	Metastability using Ac_meta01
57478	81408	Incorrect parameter value reported in elab_summary report
57536	81459	Expected symbol for PG netlist display
57581	81482	False Clk_Gen23
57585	81429	Message which highlights parameters specified multiple times.
57654	81486	[RULE-REQUEST] :: User expects to check no other connection between -from and -to
57687	81538	Enhancement for custom methodology Selection in console window
57881	81876	Spreadsheet view should have more intuitive default settings for column text alignment
57903	81481	Enh: Waiver Arguments present in Group1 category
57917	81881	SGDC Constraint Editor Window needs better default pane sizes
57918	81882	SGDC Constraint Editor Window size needs to be maintained between sessions, projects

VI #	EW #	Title
57920	81884	SGDC Constraint Editor Window needs to offer quasi_static, input, output constraint types
58023	83480	SG_SGP_func_int: Concorde generating SYNTH_5165 warning with garbage parameter value on custom design
58055		LIBINFO_705 should ignore "related_power_net" checking on internal pins
58112	82047	STARC-2.10.3.5 false violation
58271	82149	LS and AO should not be part of schematic abstraction
58503	82302	STARC-2.10.3.2b does not flag
58725	82624	{ENH} Need support of not_used_signal parameter in W528 VHDL
58735	82637	V2K construct "always @ * " not reported in moresimple report
58765	82364, 85153	Missing 'qualifier' option in SGDC Constraint Editor
58827	82322	Enhancements in W415a rule
58842	82307	False Ac_fifo01 violation
58881	82686	When templates are run in Seq. mode, it doesn't switch to analyze results tab automatically
59160	87130	SpyGlass should not report violation on Precompiled DesignWare Libraries and Package files
59362	83035	Lint run taking ~54G memory using 4.5.0.2 compared to 42G in 4.4.1
59422	88847	CRASH in testcase related to escaped name (add/lookup not working in module port table)
59806	83306	False SYNTH_5243 error
59812	83331	STARC-2.6.2.2 produces false violation
59871	83378	Generate a report which contains hierarchical path of qualifier signals
59992	82184, 87792	SYNTH_5243 violation on a design getting passed by another synthesis tool
60039	83527	ENH_36::Custom rule
60094	83570	NEW_RULE_4:: Custom rule
60105	83573	NEW_RULE_6:: Custom rule
60114	83392	W415a false warning

VI #	EW #	Title
60117	83576	NEW_RULE_8:: Custom rule
60121	83579	NEW_RULE_11:: Custom rule
60129	83585	NEW_RULE_18:: Custom rule
60201	83398	Please remove project type in the "Import Sources" menu of the GUI
60250	83446	GenSDC: Absolute path required of param SDC inside generated sdc
60293	80335, 86929, 87541	4.5.0 console/SDE slower than 4.3.6
60312	82948	GUI issue with the "other cmd line" field
60318	82297	Project Summary Report gives wrong results
60641	86061	Update documentation/man pages to indicate way to specify negative value
60646	83708	Ac_cdc01a doesn't check crossings using sync_cell
60674	83656	FlopClockConstant rule gives false positives for manually instantiated cells
60680	83715	Please add a tcl mechanism for "continue on error" when TCL_ERROR is returned by a command
60766		W504 Message needs to be updated to reflect synthesis of integers
60924	84001	False violation for clockPinsConnectedToClkNets
60944	84008	Synchronized signal not recognized as valid qualifier
60975	83954, 89244	[MBIST-DFT] disabling automated clock connection
61031	81459	Expected symbol for PG netlist display
61069	84054, 84107	[MBIST-DFT] [Enh] mb_clock_choice: enlarge the scope to select clock net also for a shared collar
61163	83597	UndrivenOutPort-ML flags to celldefine library
61486	84277	clockPinsConnectedToClkNets reporting even when clock nets are defined
61714		Different UI options do not preserve previously selected directory (Open File operation)
61797	77613	SpyGlass IS view should provide the capability to view the content of the liberty file
61801		Usability: Remove need to specify language (remove need to specify verilog, vhdl, mixed)

VI #	EW #	Title
61843	84395	W415a messages not being reported within a generate block of code
62297	82149	LS and AO should not be part of schematic abstraction
62402	84591	{ENH} Search should not expand all modules in Module View
62527	84529, 83340	False violations of STARC-2.3.2.4
62614		Confusing details given for simulation_data constraint
62626	84616	run_goal is not working after running group run in project file
62640	83027	{ENH} Enhancement in Clk_Lat04a to flag for zero set_clock_latency when -source is specified
62711	84877	Tool re-processes all the .lib file list again if it finds the any non-compatible sglib
62800	84934, 85385	Enh: W528 should only flag when no bits in a bus are used
62837	84972	{ENH} Enhancement in message of LPSVM04A
62902	84980	FSM one hot state assignment
62913	84912	GenSDC: Use $SPYGLASS_HOME in tech files path in SPNC
62921	85007	W120 too noisy, should have an option to report only when complete vectors are unused
62927	84909	Merging of custom rules
62943	85034	sg_shell/adc - fatal error cdc_false_path on 2D arrays
62980	85016	Inconsistent start window from sg_shell gui_start command
63010	84831	'File not found' message is missing in spyglass.log
63040	79466	SEC_FATAL2 doesn't create a violation in the msg tree
63059	85141	Spyglass/sg_shell does not properly queue
63085		Incorrect W122 violation
63100	85144	cdc_false_path with wildcard in SGDC fatals in sg_shell, works in Console
63127	85355	False W-164a and W528 warnings
63243		Confusing MBist_SGDC_04 Fatal message is reported during bottom-up flow when only design query command is run

VI #	EW #	Title
63260	83576	NEW_RULE_8:: Custom rule
63261	85161	{ENH} Enhancement in spread sheet for CDC rules
63267	85300	memory_port constraints cannot handle certain memory pins
63387	85369	implicit width mismatch not being caught
63484	85378	False Negative: LPSVM04
63515	85515	SpyGlass stuck while checking Ac_init01
63531	85227	Behavior of custom rule with -chip parameter
63549	85514	False SYNTH_5129 violation
63605	85144	cdc_false_path with wildcard in SGDC fatals in sg_shell, works in Console
63663	85393	STARC-1.3.1.2 and SynchReset-ML flag from V4.5.0
63673	85634	Enhance LIBWARN_35 and LIBWARN_36 warnings as per updated list of possible values
63696	85605	STARC-2.10.6.1 should not flag for signed addition
63774	85690, 88194	enable_gateslib_autocompile should be on by default
63939	85752	Missing 3rd decimal while generating activity value
64022	85751	CDC rule SGDC_output01 reporting negative indexes for arrays
64045	85768	Dashboard silent on non-existing waiver reports
64058		Enhancement Request: Including Logic optimization for Lint rule W18
64069	84930	Request of message and severity change for Ac_glitch03 rule
64126	85822	False UndrivenInTerm-ML warnings
64131	85871, 85933, 86257, 88965	Long run time in W392 rule
64160		Have an option for 'mb_report_instances' to return an array of instances
64234	85939, 88407	SoC flow not working for some CDC goals - e.g. clock-reset-integrity
64259	85889	Pragma "//spyglass disable_block ALL" does not work for files which are added using `include directive

VI #	EW #	Title
64351	85915	Need Rule Dependency chart so that development team can control pre-requisite rule runs
64476		Reset as source should not be checked for data crossing
64491	84616	run_goal is not working after running group run in project file
64530	86068	Datasheet does not handle multiple methodologies cleanly, we should document this limitation.
64576	86112	False SYNTH_5191 error
64640	86130	False checkSGDC_01 when using SoC flow
64661	85954	MCS issue - removed rule does not remove its "overloadrule" line, causes false warning
64701	86198	Multiple values not recognized by .lib attribute "default_connection_class'
64715	86209	Exit code details for sg_shell
64717	85659	Txv_MCP_Nontop false alarm
64726	86212	The -DEBUG switch should specify exactly what is missing while generating datasheet report
64732	85141	Spyglass/sg_shell does not properly queue
64780	86244	Redundant warning for generate if/case
64822	86219	W122 false violation when only attribute of a signal is used in always block
64886	86308	sgdc -import is not supported by tcl or console. Please remove.
64889	86156	UPF wildcard support without escape characters requested by customer
64898	86315	Change default value of 'new_flow_width' parameter
64911	84926	Missing LPSVM12B on front-end netlist when running custom template
64968	86213	The -DEBUG switch should specify exactly what is missing while generating dashboard report
65013	86420	spyglass_lc is causing FATAL on *.lib file
65046	86399	Parallel run issue
65084	86927	Issue regarding waiver window
65107	86284, 87978	False message of W240 rule for 1-dimensional unpacked array

VI #	EW #	Title
65208	86983	SpyGlass run taking huge amount of time while synthesis
65230	87005	SpyGlass-PE run causes memory allocation failure during 'rme_exit' rule checking => check for DW modules
65255	86156, 88795	LPLSH04 ignores -rule and -threshold fields
65258	86987	sg_shell should support the ability to return a user-defined exit value
65318	87079	Equiv_SDC_Dual_Design shows Error for same design and same SDC
65381	87106, 87207	LIB syntax errors while generating sglib
65393	83576	NEW_RULE_8::RULE_RTL208
65396	87163	SDC Parsing errors point to the wrong constraint file
65435	81481	Enh: Waiver Arguments present in Group1 category
65442	87102	Custom rule behavior to be changed
65512	86990	POMA model should be created even if the clock is equal to zero
65520	87186	Undefined cell 'fd4q' is instantiated in the synthesized netlist from another synthesis tool for DW components
65539	79907	Incremental GenSDC: Default value in crossings file should be "F"
65540	84656	ErrorAnalyzeBBox is not flagged on a cell defined inside 'celldefine
65602	87176	Modify the message in 'action' column in coverage audit report to mitigate the issue of 'uncontrollable testmode pins'
65632	87270	Crash during LPPLIB17
65662	87299	Report info from spyglass.out not reported in spyglass.log
65786	87392	Incorrect W210 Warnings
65793	87359	{ENH} LPLSH04 message enhancement
65819	87425	Use of macros for instantiation with ifdef result in incorrect line numbers for violations
65832	87422	Methodology Guide needs to include a note that cdc_gen_inputs does incremental generation
65855	87447	FSM depth is shown as empty field in report

VI #	EW #	Title
65857	85629	Fatal error due to output constraint in the abstract.sgdc
65877	87376, 87529, 87659, 88778	SV: SYNTH_5170 should be reported as Warning for zero replicator in concatenation when there are other non-null items in expr
65885	87466	{ENH} Add ability to edit path in open project dialog
65901	87435	Output ports seen as input for stopped module
65931	86181	SDC_02 false alarm
65933	87391	Possible false LPISO04a / LPSVM22 violation reported
65968		Incorrect schematic for FP_Verif03/04
65985	87552, 88700	False SDC_214
66005	87556	False violation of Equiv_SDC
66041	87648	SpyGlass fails with .lib errors
66043	87653	Hang (or very high run time) in rule Latch_02
66061	87717, 87602, 87823, 87956, 88564	Incorrect ErrorAnalyzeBBox error is due to incorrect ELAB_6312 error
66069	87638	STX_VE_389 error for use of real, whereas another tool report is clean
66106	87682	Incorrect synthesis causing false violations
66125	87744	ignoredu option is not working if we use single quote in project file, as described in user guide
66127	87747	{ENH} There should be the reference of ignore_summary.rpt and stop_summary.rpt in user guide
66158		UndrivenInTerm-ML error wrongly getting flagged
66159	87668	Warning message incorrect in the case of IO_Consis04
66210	87742	False W163 violation on parameter override
66215	87787	SpyGlass crash while synthesis
66235	87814, 89042	Abnormal termination while checking "Ac_conv02" Rule
66255	83578	NEW_RULE_10:: Custom rule
66257	87802	MCS dumps overloadrule for all 3 formats
66259	87798	W164b calculates output width of multiplications with constants incorrectly
66261	87830	Incorrect LPSVM09 violation

VI #	EW #	Title
66282	87844	Runtime issue on W123
66290	87815	false STX_VH_2 violation with ignorefile option
66312	87857	Missing SYNTH_5303 error violation
66336	85752	Missing 3rd decimal while generating activity value
66363		Disable pop-ups during SpyGlass Console startup
66364	87874	SpyGlass crash while flattening
66398		Goals created with MCS are still having -mixed inside file as well as part of the name
66409	87477	False STX_VE_1267 for the hierarchical use of data types
66410	87900	False violation: Equiv_SDC_Block when MCP is defined as ‘u1/rr/Q_reg’ instead of ‘u1/rr/Q_reg/CLR’
66417	87919	Spyglass reports "ERROR [38] E198" error while parsing .lib file
66460	87774	Enhance Coverage_audit step-1 message to include "Info_forcedScan”
66473	87891	Fatal error of sgdc generated by sdc2sgdc, while using generate instance
66484	87951	{ENH} Request to add enough debugging information in IS for Diagnose_testclock
66505	87918	Missing files for modules in dead hierarchy in design_database.csv file
66513	87971	Rule W175 to handle localparams,
66529	87934	False ELAB_445 error
66540	87796, 88511, 89002	Expecting clock definition at the output of clock gate or clock mux - due to blackbox
66570	88015	Loading project state in GUI takes huge time
66593	88031	SpyGlassInternalWarning WRN_901 message reported
66594	87931	Blank UI Set Read Option window.
66603	88028	Unacceptable time to switch goals in Console
66611	88040	Memory Allocation failure
66614	88010	False SYNTH_5255: SG treats unsigned integers as signed for bit indexing calculation
66619	88046	testclockFrequency constraints is not documented in DFT rule guide & consolidated SGDC doc

VI #	EW #	Title
66634	87916, 87867	False BB_DFT011 second issue
66677	88073	nocheckoverflow not respected for counter cases that are checked with check_counter_assignment
66702		Wrong rtl is generated. 'genvar' from one generate block appears in a different generate block
66725	88061	GW rule STARC-2.10.6.1 gives incorrect warning for RHS using concatenation
66738	88146	False violation for PESTR13
66774	88150	False ELAB_3580 on parameterized interface
66780		Only mixed file is getting modified even though methodology has verilog and VHDL files present
66797	88153	SpyGlass crashes during elaboration
66812	88084	Propagation of set_case_analysis is incorrect in ac_conv01 incremental schematic, leads to incorrect analysis
66822	88231	Abnormal termination while checking rule W164c on custom design
66823	87164	Cannot get ac_cdc01a PP's to go away, even with long fa_time
66859	88159	Generic parameter passing from VHDL top to Verilog instantiated module raises false ELAB_3580
66889	88101	Spyglass run cropped up with some Internal Warnings
66891	88208	Abnormal termination while running Equiv_SDC_Dual_Design
66915	88253	False ELAB_3580 on nested records.
66929	88155	False SYNTH_5199 error
66932	88256	False SYNTH_5387 error
66939	88265, 88329	Atrenta Console terminated abnormally
67020	88317	Destination FF missing in incremental schematic of BB_DFT013(Clock_17)
67022	88257	SpyGlass-LP RGX runtime issue
67036		More fields required in tab file generated from Waivers
67153	88000	{ENH} Enhance the doc of LPPLIB06
67198	88391	SPYGLASS TERMINATED WHILE Checking "Txv_Warn01" Rule

VI #	EW #	Title
67215	88418	SpyGlass hangs while checking PEPWR20
67264	88425	{ENH} The default version of upf not documented
67281	87907	STX_VE_911 with SpyGlassInternalFatal INTERNAL_FATAL src/velexCrIncludeFile.cpp
67285	88427	Error specifying clocks on SV structures
67299	88445	Abort on message tag text file reading
67315	88484	Incorrect violation message in the example of STARC-1.2.1.3 in document
67317	88486	CDC documentation related to allow_combo_logic parameter
67318		Hierarchical waiver import issue with absolute path and $ENV path in sg_shell
67319	88096	Abnormal termination during incremental elaboration of DW components
67364	88487	The Ac_xclock01 has incorrect explanation in Reference guide.
67417	88523	False LPISO05 violations
67428	88518	Clock_info01 infers structurally incorrect domain relationships in generated_clocks.sgdc
67433	88545	resolve field for create_supply_net not documented
67444	88543	RME issue - RTL fixed by autofix does not have the RME ID per spreadsheets
67450	88547	Issue with Autofixed VHDL for Async_07
67459	88498	Hang while checking Propagate_Clocks
67461	88235	set_option param inconsistent behavior
67468	88621	False SYNTH_5198 for the attached testcase
67484	88527	W116 hangs when 1D array is incorrectly used as 2D array
67486	88574	Severity overload does not work for SYNTH_5167 and SYNTH_5170
67493	88377	Ambiguous 'Atrenta_External_Domain' message
67535	88577	The message of SGDC_reset_validation04 is not correct
67537	88140	checkUPF_existence - documentation is not clear that in which case Fatal/Error/Warning will occur

VI #	EW #	Title
67539	88600	Documentation update for BB_ RTL133
67579		Memory corruption in unified regression runs
67587		Av_deadcode01 schematic highlight is incorrect and referring to unwanted nets
67588		Av_deadcode01 schematic highlight is incomplete
67660	88669	SG complains about label redefinition in mutually exclusive IF/ELSE clauses
67669	88651	LPSVM09 does not flag when connect_supply_net incorrectly connected
67678		Add mbist result summary section on stdout and mbist_moresimple.rpt
67705	88692	UPF Parser does not recognize supply_set references
67746		SYNTH_5251 violation
67800	88742	Need to annotate test_mode values on the incremental schematic of Diagnose_testclock
67843	88708	STARC-2.10.3.5 violation discrepancy with shift operators
67877	88803	False Atspeed_11 violation
67887	88767	{ENH} Separator in csv file provided as input to the tool
67896	88818	Recursive includes with guardbands fatal in SG but pass in third party tools
67903	88821	X-generation during update cycle
67933	88990	Wrong generic map parameter on uniquified VHDL instance
67936		Crash for customer on PESAE06
67951		[MBIST-DFT]: Feedback/improvement on mb_clock_choice command
67991	88827	Remove the Ac_usync* message related to strict_sync_check
67999	88835, 88770	False violation of LPISO05 due to incorrect handling of -source field of set_isolation
68012	88031	SpyGlassInternalWarning WRN_901 message reported
68020	88866	Abnormal termination during Analysis of SV file
68066	88881	Internal SYNTH_5407 error when encountering streaming operator (>>) in certain context

VI #	EW #	Title
68079		Long runtime in UPF_PRD_ISO_ASSOCIATION and LPSVM53
68106	88837	UPF_lowpower12 violations should not flag when source in domain A to sinks in domain A and domain B.
68119	88879	GUI schematic much slower in console than SDE
68163	88896	Crash in PEVLESSINIT rule
68180	88911	[MBIST-DFT]: Change default value for -memory_clock_pin
68264	88956	core dump caused by memory explosion: SG_ASSERT_ERROR
68312	88771	Console error "* The following rules or rule groups could not be found in the defined policies"
68413	88996	Improve W442f rule documentation
68443	89046	Incorrect bit assignment in rtl generated -> buffer added for local signal in nested for loop
68488	89068	Preserve Signal assignment/parameter assignment inside translate_off/on pragma for re-instantiated instance in VHDL
68510	89069	Unexpected SYNTH_5251 error
68561		Gigantic power numbers ~65 WATTS
68578		Bug: Schematic is not visible for multiple Clock_04 violation
68583	89133	Lots of identical SpyGlass Internal Warnings FLAT_502 INTERNAL_WARNING
68662	89074	SYNTH_5407 Synthesis issue
68677		selective autofix not working for multidim nets
68701	89187	SpyGlass reports a false Diagnose_testclock warning
68857	89281	Dashboard failed to generate when no top is specified in prj file
68921	89345	Crash at Clock_sync09 rule