# ASIC Physical design

## ASIC design flow

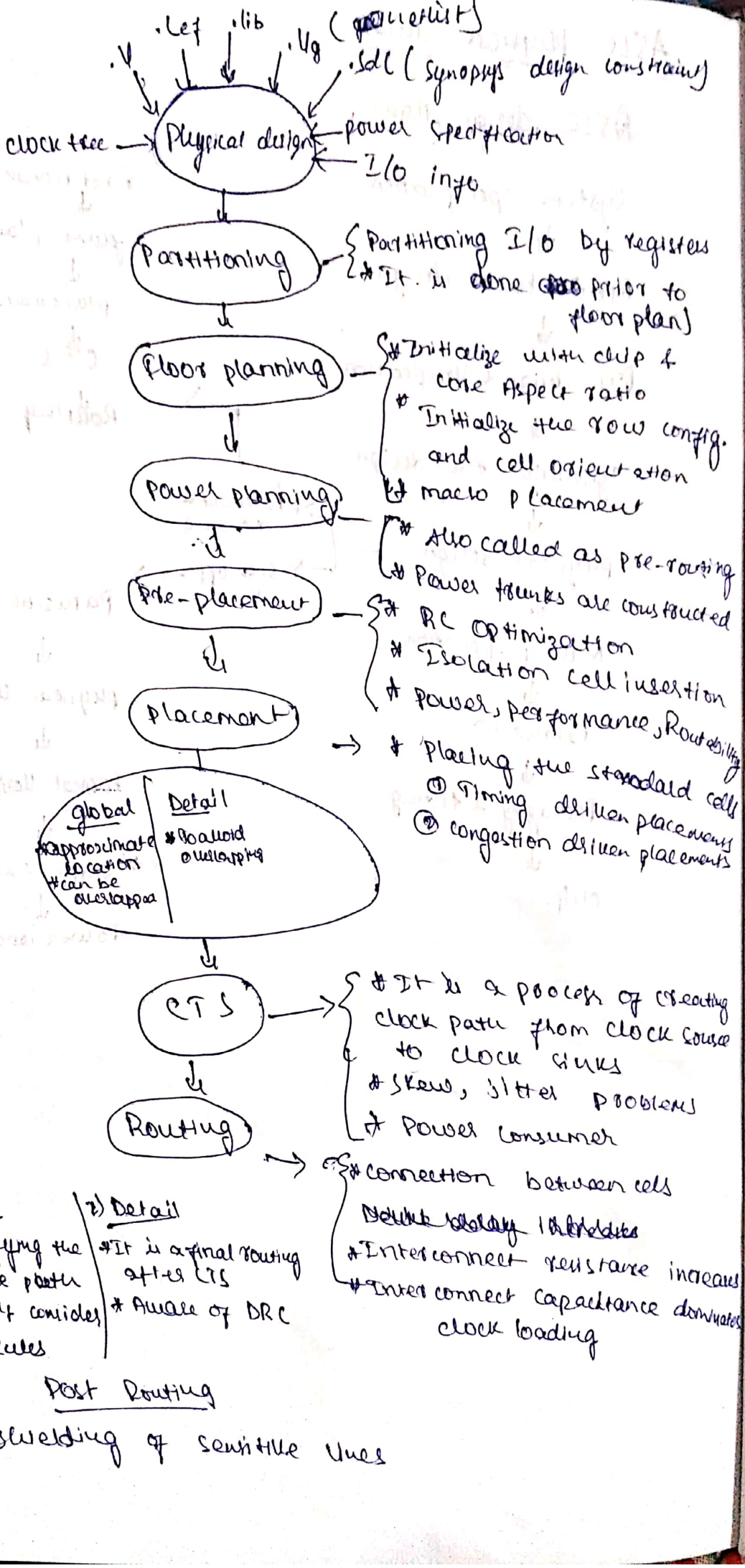
System specification
↓
Architectural design
↓
RTL design & Verification
↓
Synthesize the design
↓
physical design → Placement & routing
↓
Mask preparation
↓
Fabrication
↓
Packaging & testing
↓
Chip.

physical design → signoff →

Partitioning
↓
floor-planning
↓
placement
↓
CTS
↓
Routing

signoff →

Parasitic Extraction
↓
physical Verification
↓
Formal Verification
↓
Static timing Analysis
↓
Power analysis




1) Global
* Identifying the routable paths
* Doesn't consider DRC Rules

2) Detail
* It is a final routing after CTS
* Aware of DRC

Post Routing

1) Shielding of sensitive lines

## Physical verification (DRC)

→ checking physical layout data against fabrication-specific rules.

→ Violating DRC might result in a non-functional circuit or low yield

## LVS (Layout Versus Schematic)

→ Verifies the connectivity of a Verilog netlist and layout netlist.

→ It doesn't compare functionalities

→ LVS check Examples :- short net, open net, Extract Error (Parameter mismatch), compare Errors,

## ERC (Electrical rule check)

To confirm the Electrical connectivity of a IC design

→ To locate devices connected between power and ground

→ To locate device with missing connection

## Formal Verification

→ Verify the two representations of circuit design exhibits same behaviour

→ Power checks

## Parasitic Extraction

→ It provides the Electrical information (connectivity resistance, capacitance, and Inductance).

→ These Extractions is used to calculate the delay

**STA** :- Analysis of digital circuit to determine if the timing constraints imposed are met and to check the design is working properly

## Power analysis

It is to measure the power consumption of a device, it may also provide, harmonic distortion, peak, mean and many more parameters.