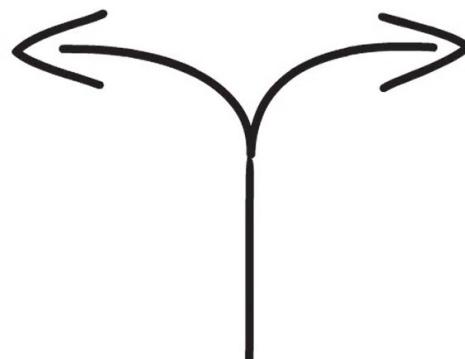


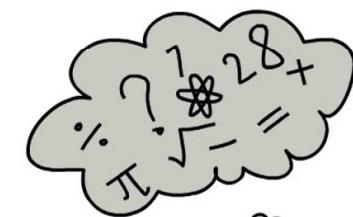
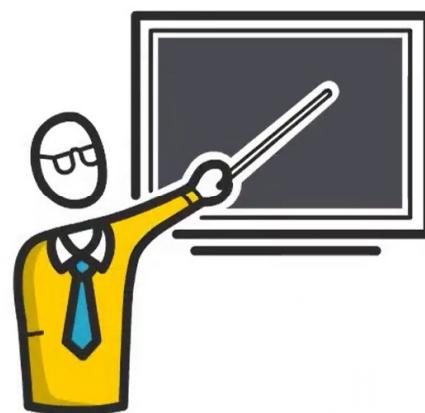
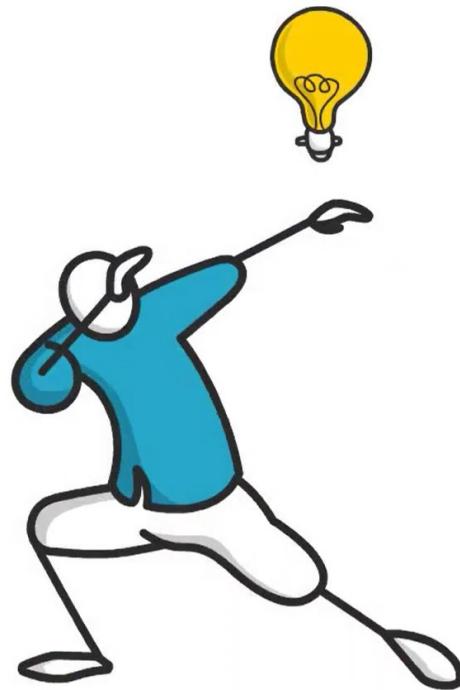
# STATIC TIMING ANALYSIS



**SIMPLE**

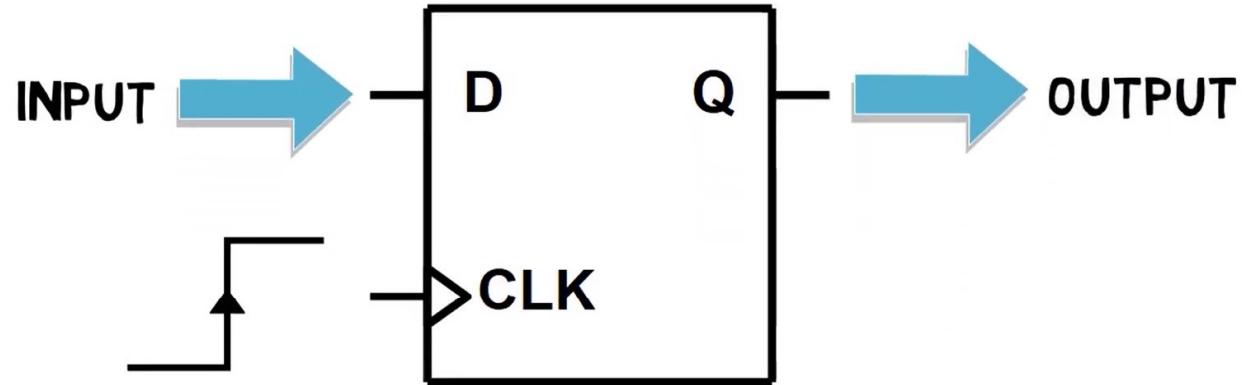


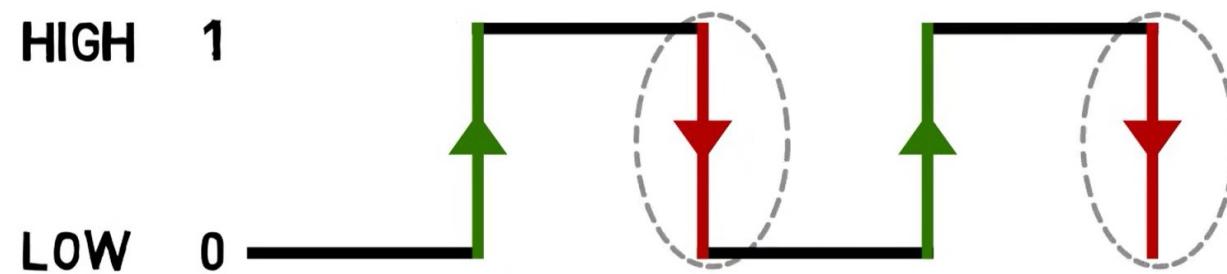
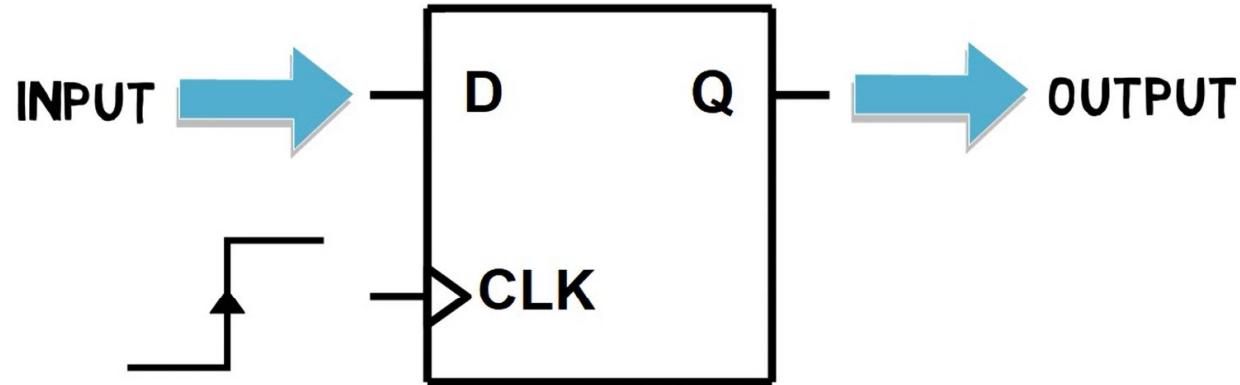
**COMPLEX**



**STA-1**

**Introduction  
to  
Setup and Hold Times**

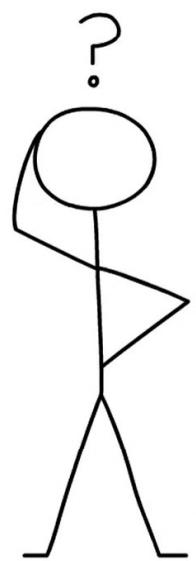
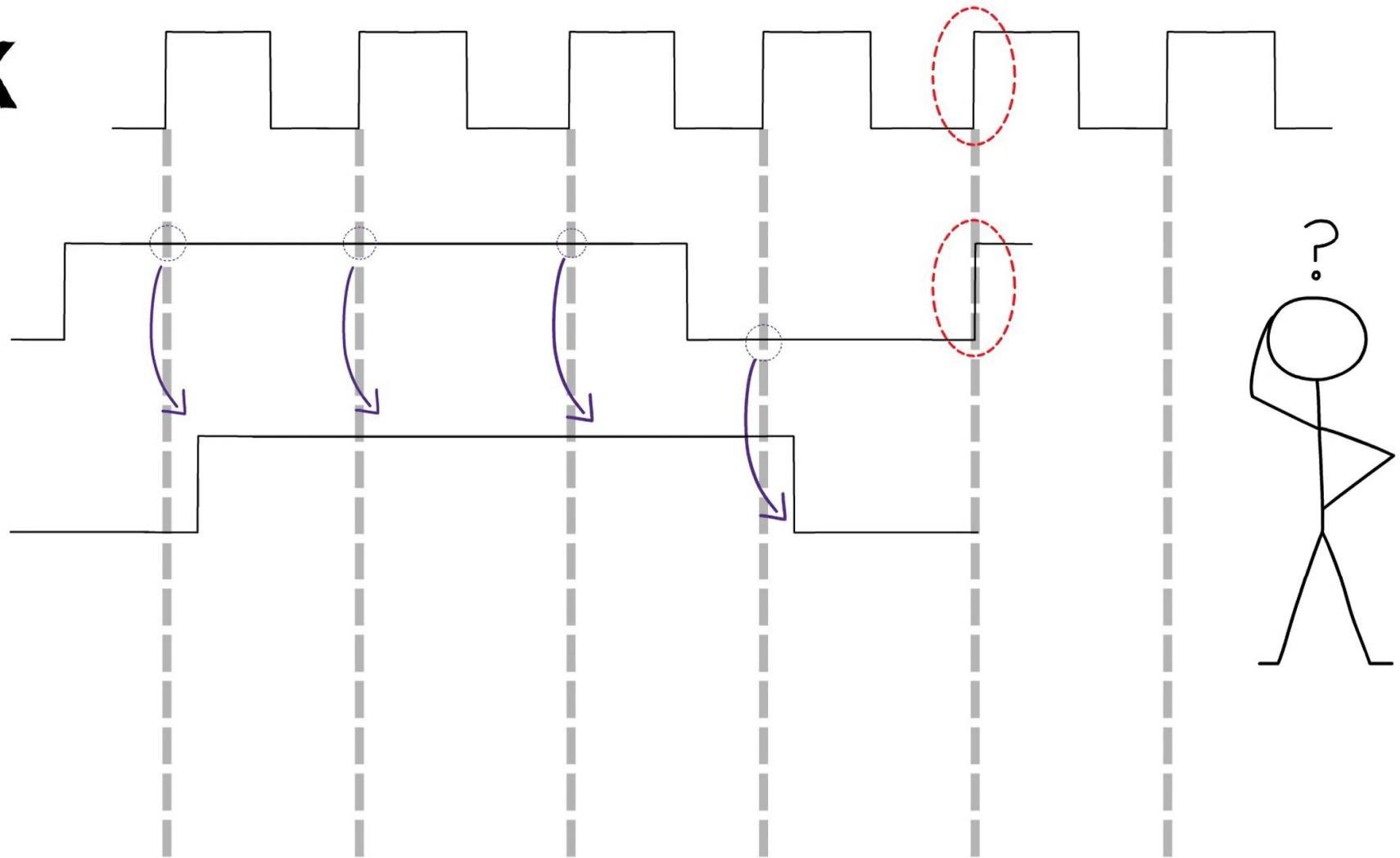




**CLK**

**D**

**Q**



**SETUP TIME** is defined as the minimum amount of time before the clock's active edge that the data must be stable for it to be latched correctly

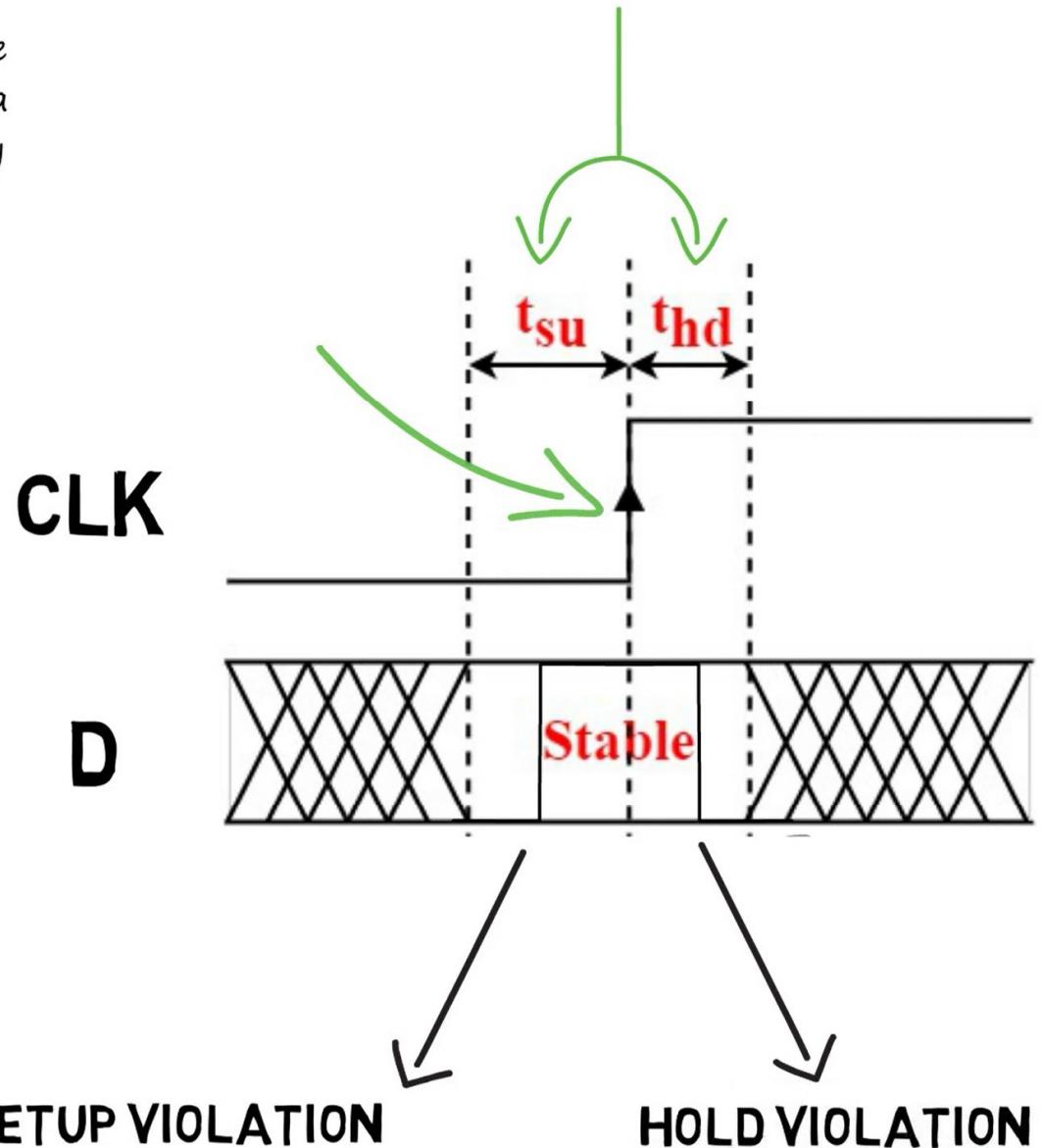
**HOLD TIME** is defined as the minimum amount of time after the clock's active edge during which data must be stable.

**SETUP TIME** is defined as the minimum amount of time before the clock's active edge that the data must be stable for it to be latched correctly

**HOLD TIME** is defined as the minimum amount of time after the clock's active edge during which data must be stable.



## TIMING VIOLATION

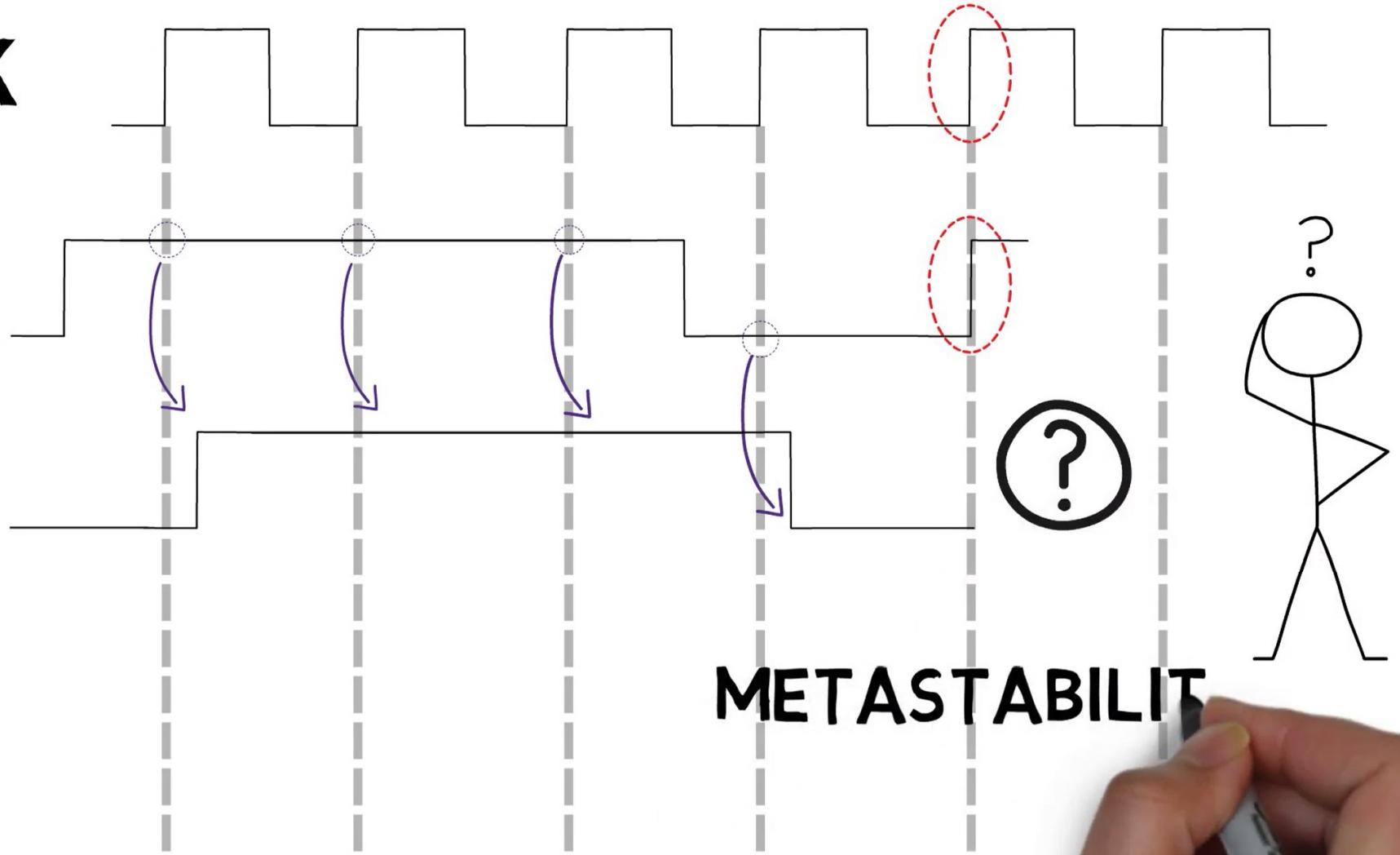


**CLK**

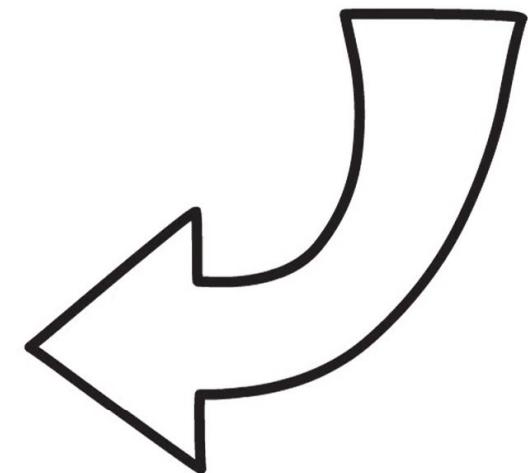
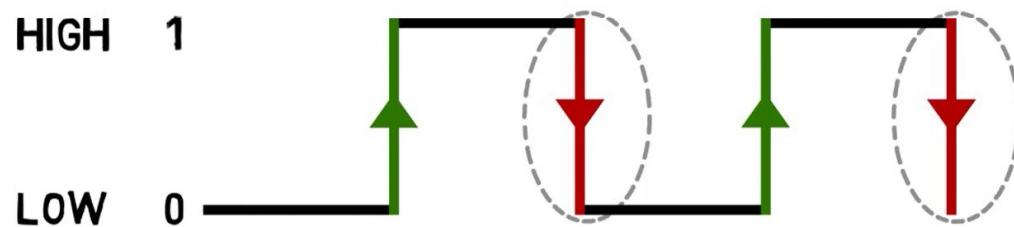
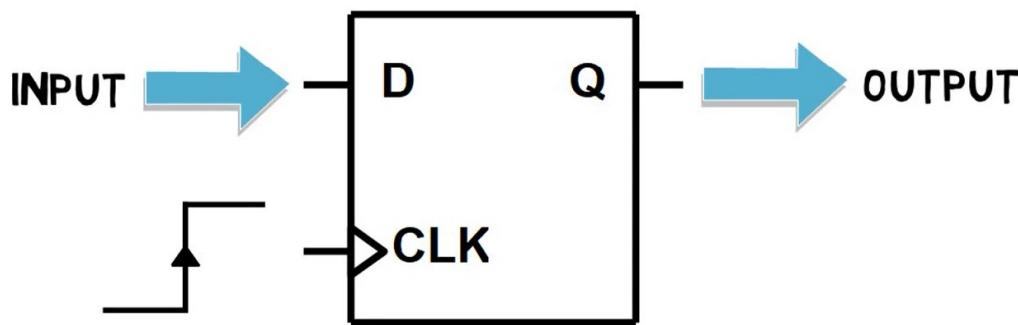
**D**

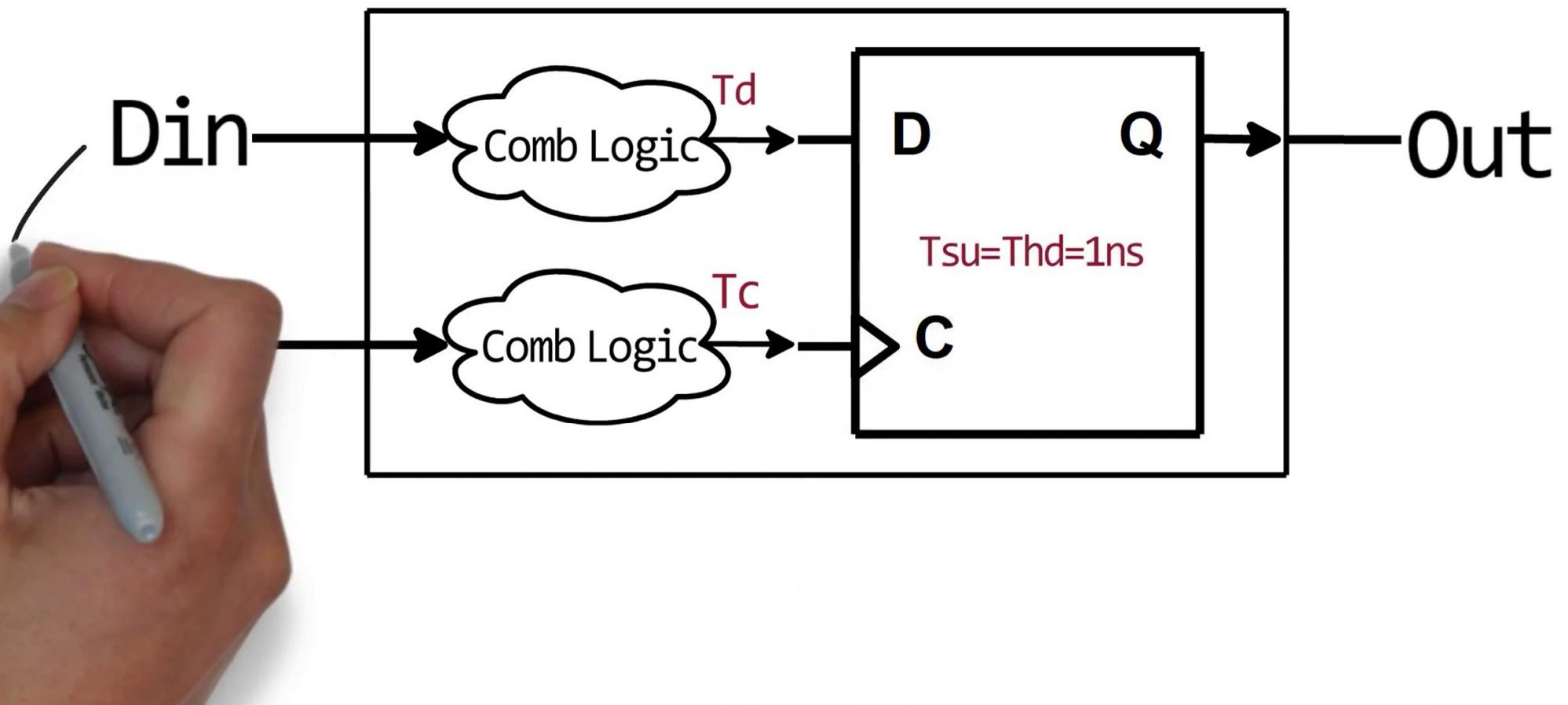
**Q**

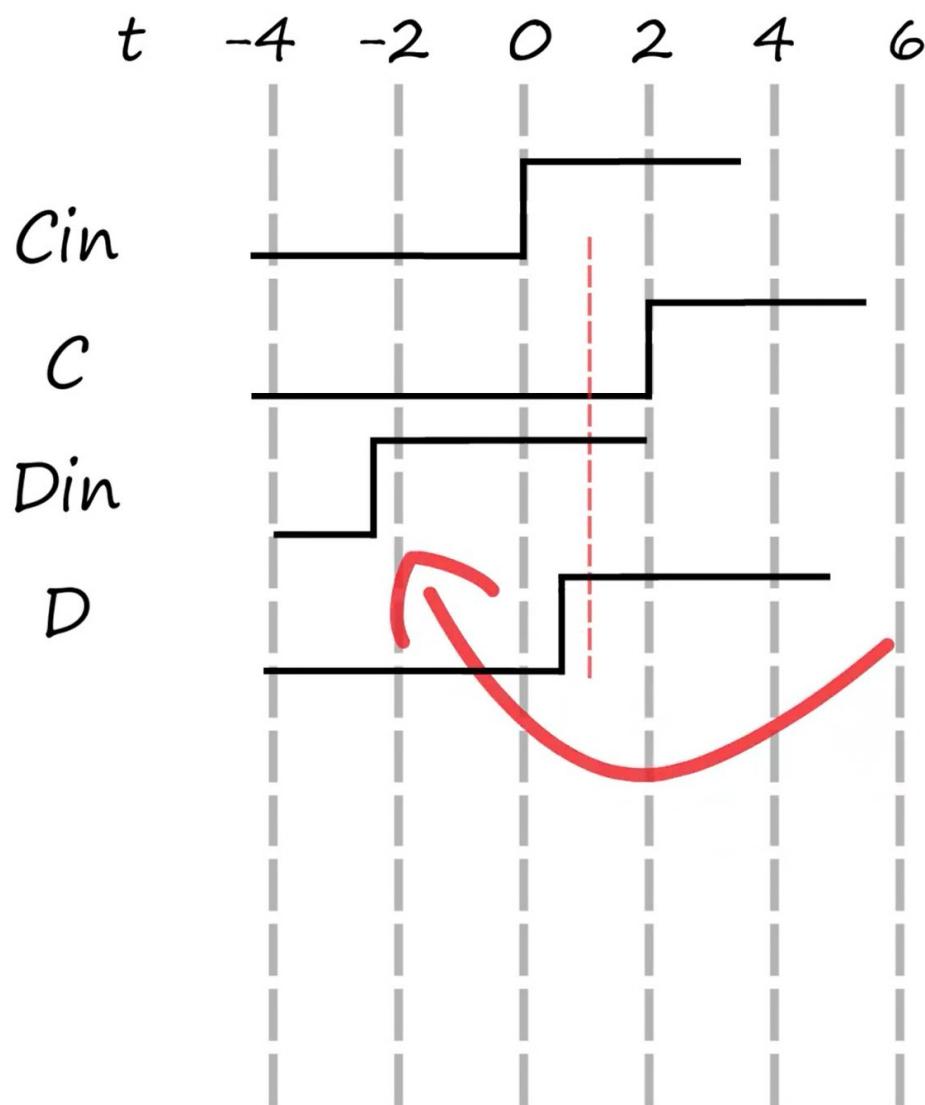
**METASTABILITY**



# FLIP FLOPS

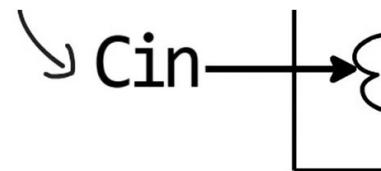






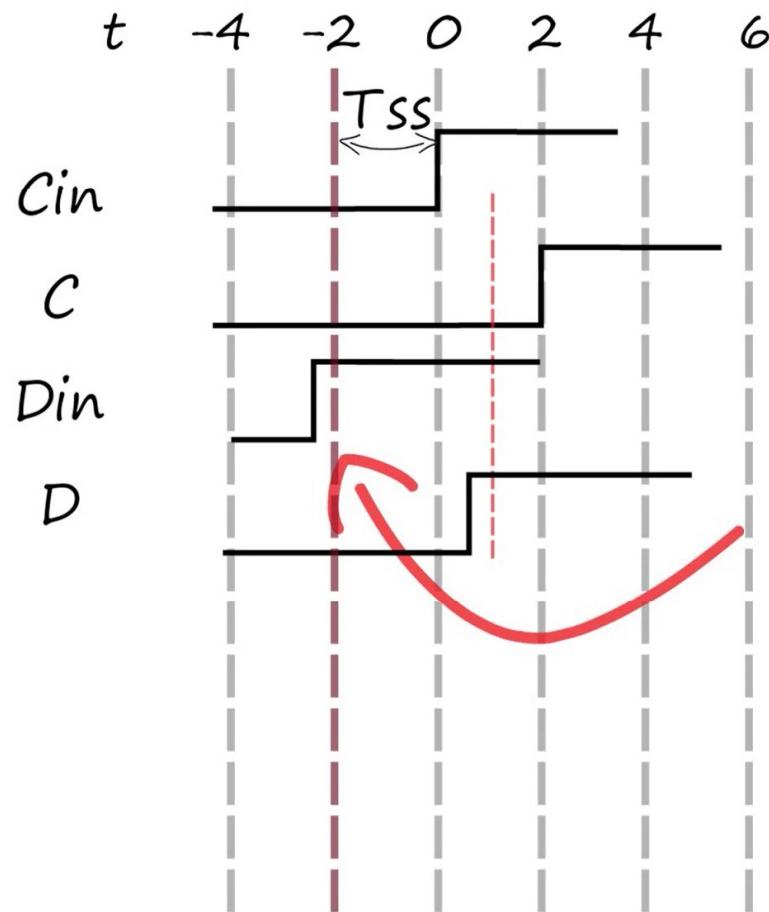
$T_d = 3\text{ns}$   
 $T_c = 2\text{ns}$

**SETUP VIOLATION**



$T_d$

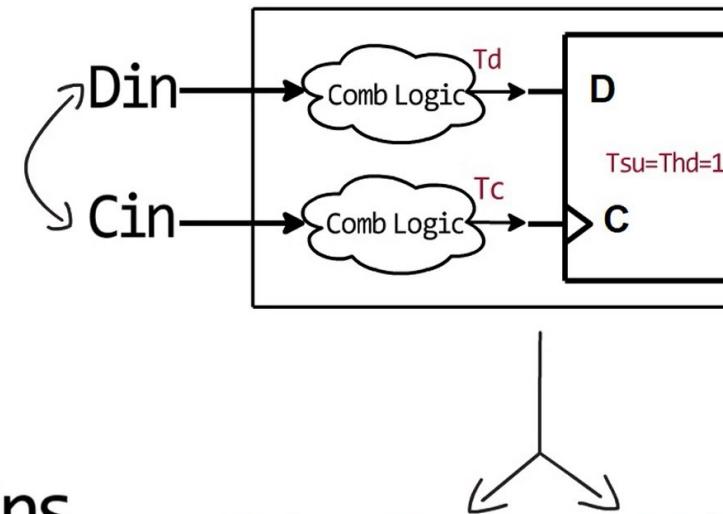
# Case-1



$$T_d = 3\text{ns}$$

$$T_c = 2\text{ns}$$

$$T_d - T_c + T_{su} = 3 - 2 + 1 = \boxed{2\text{ns}}$$



$$\underline{T_d > T_c}$$

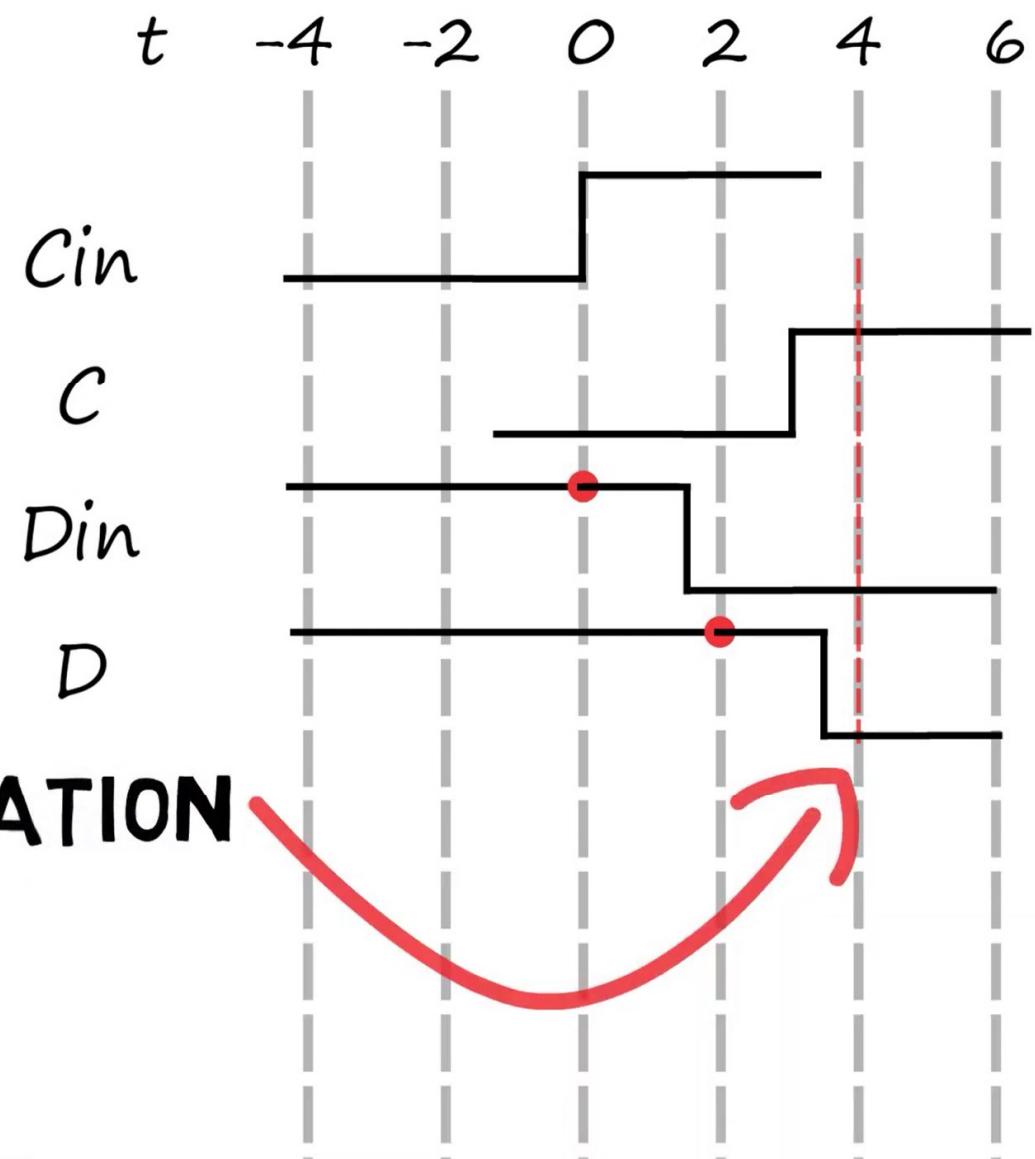
$T_d$

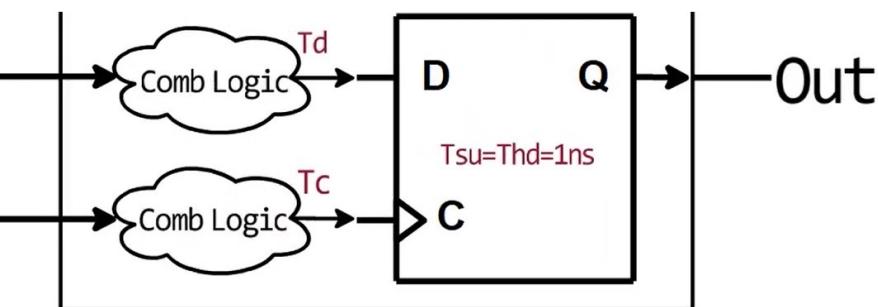


$\rightarrow$   
 $T_d < T_c$

$T_d = 2\text{ns}$   
 $T_c = 3\text{ns}$

**HOLD VIOLATION**





$T_d > T_c$

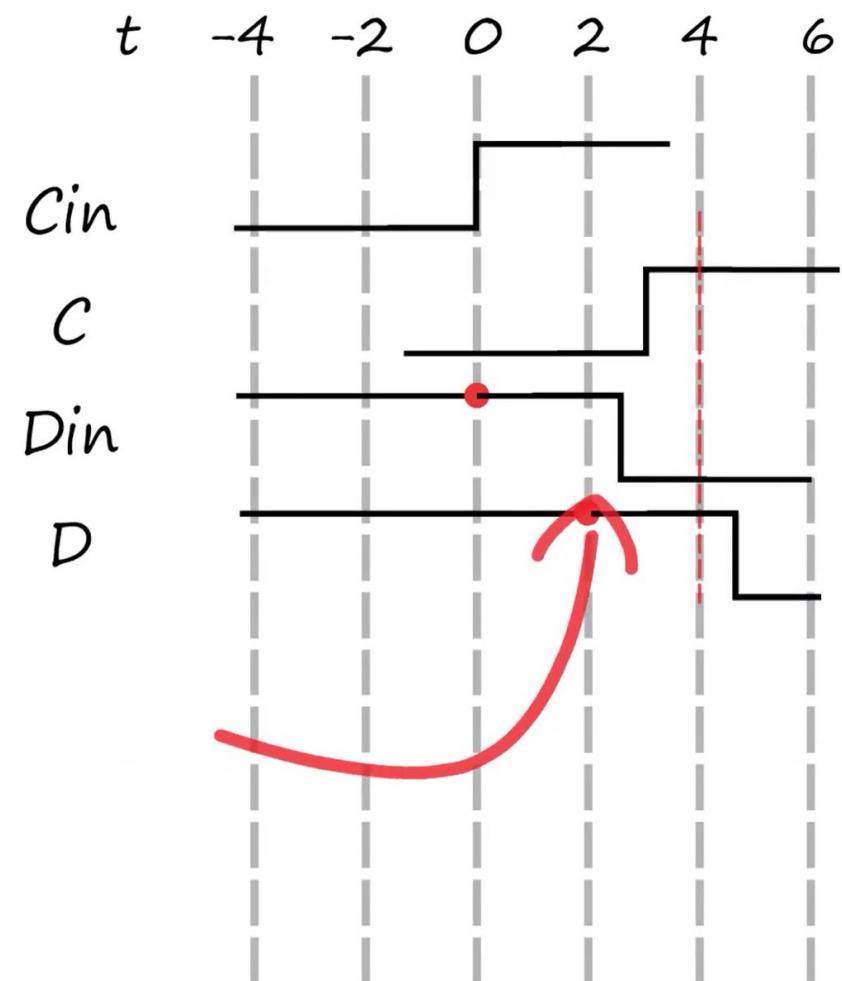
$T_d < T_c$

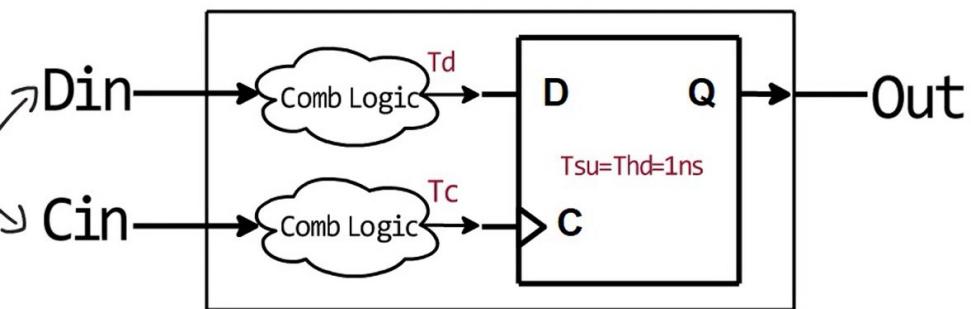
$$T_d = 2\text{ns}$$

$$T_c = 3\text{ns}$$

$$2 + 1 = \boxed{2\text{ns}}$$

## Case-2





$T_d > T_c$

$T_d < T_c$

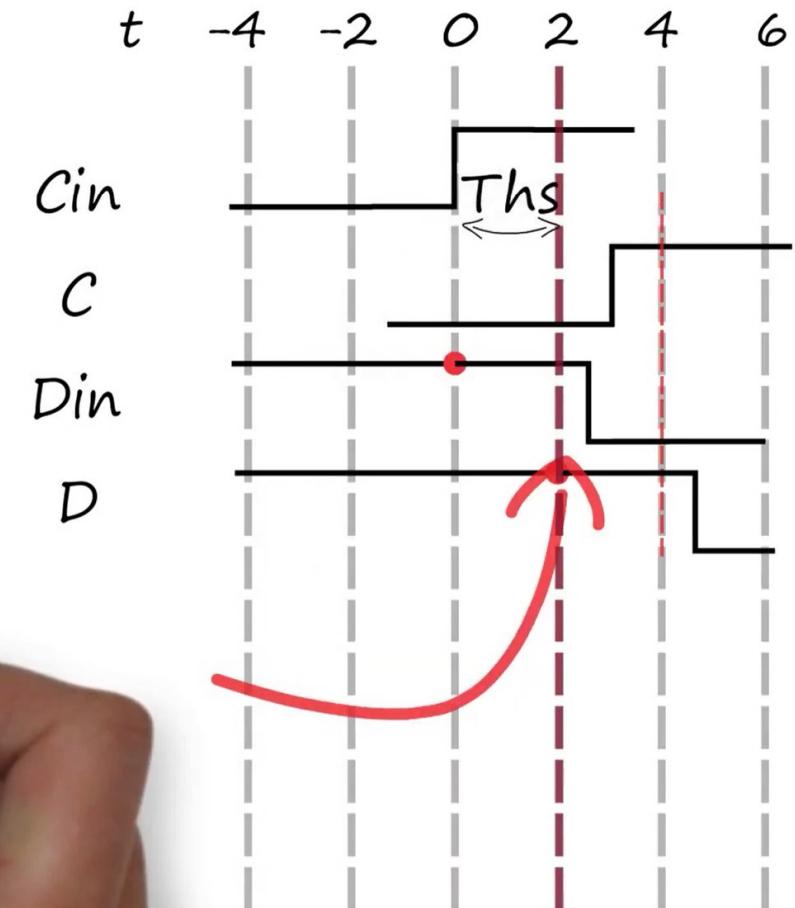
$$T_d = 2\text{ns}$$

$$T_c = 3\text{ns}$$

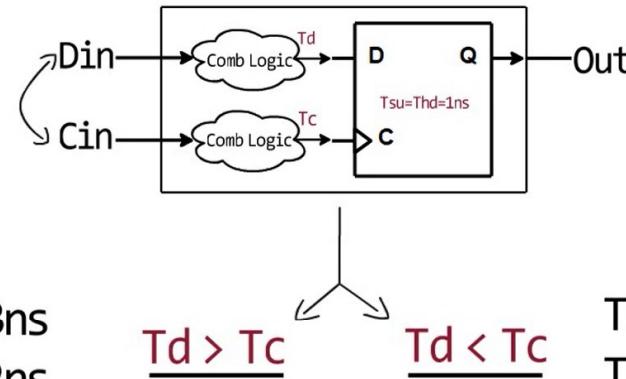
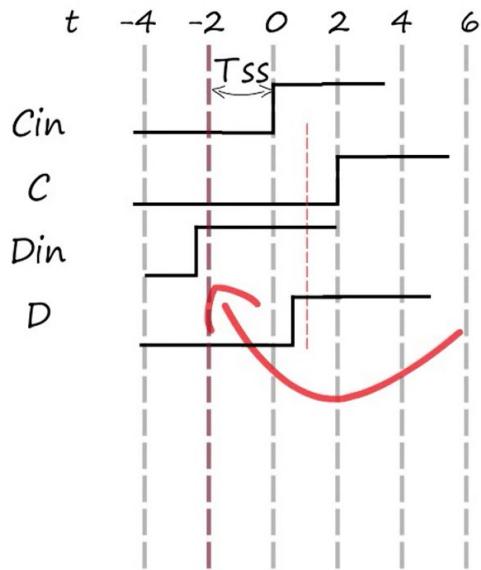
$$u = 3 - 2 + 1 = 2\text{ns}$$

$$T_c - T_d + Thd = 3 -$$

## Case-2



## Case-1



$$T_d = 3\text{ns}$$

$$T_c = 2\text{ns}$$

$T_d > T_c$

$$T_d = 2\text{ns}$$

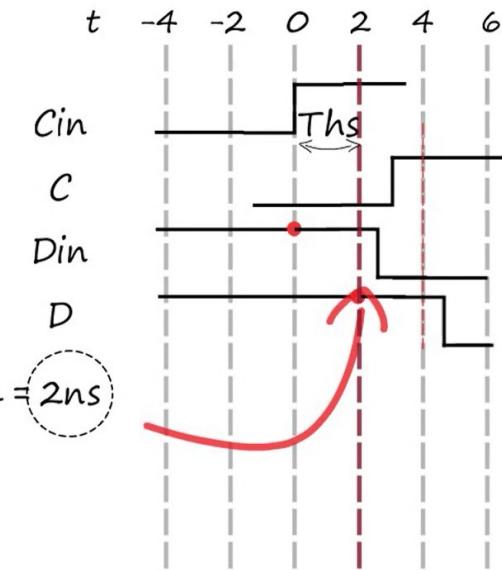
$$T_c = 3\text{ns}$$

$T_d < T_c$

$$T_d - T_c + T_{su} = 3 - 2 + 1 = 2\text{ns}$$

$$T_c - T_d + Thd = 3 - 2 + 1 = 2\text{ns}$$

## Case-2



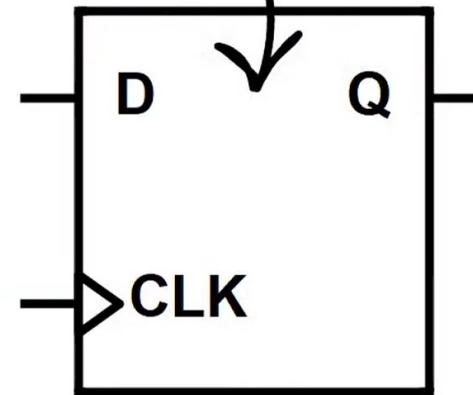
Setup and Hold Times  
with respect to a System

# **STATIC TIMING ANALYSIS**

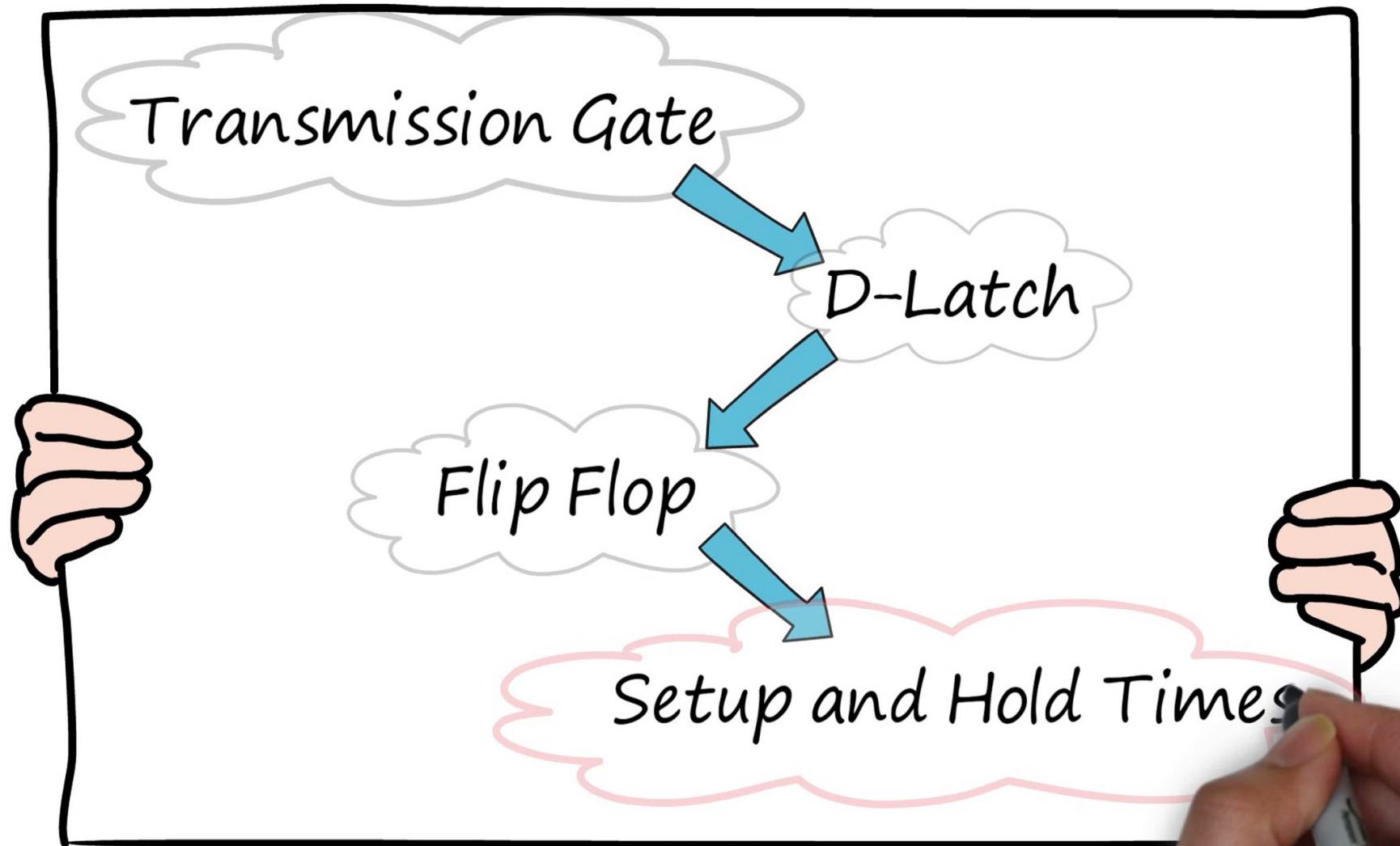
## **PART-2**

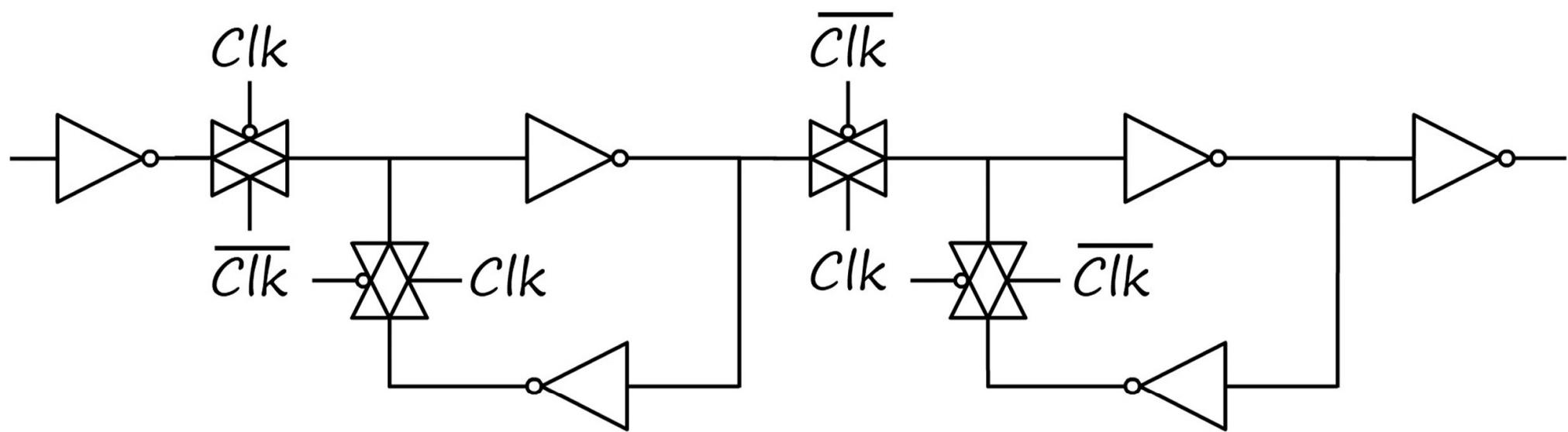
W

-Y?

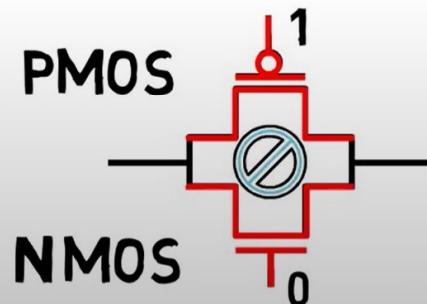
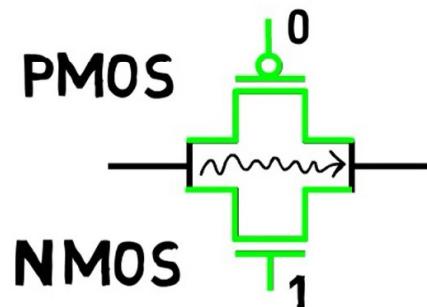
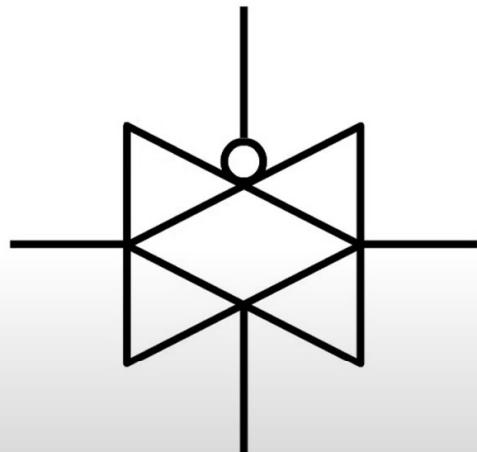


Flip Flop





# Transmission Gate



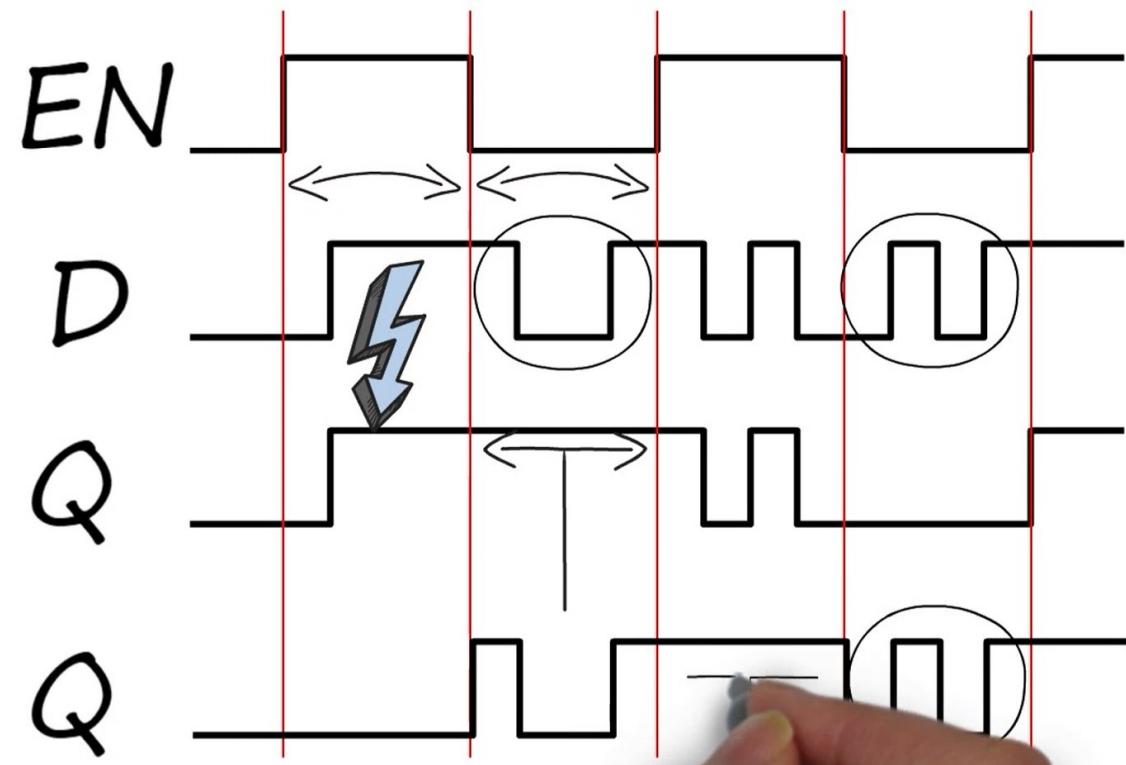
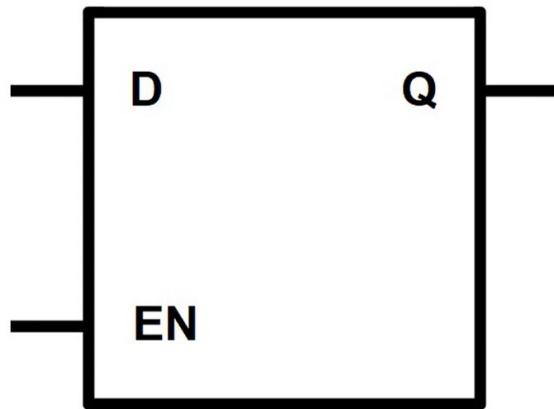
Closed Switch



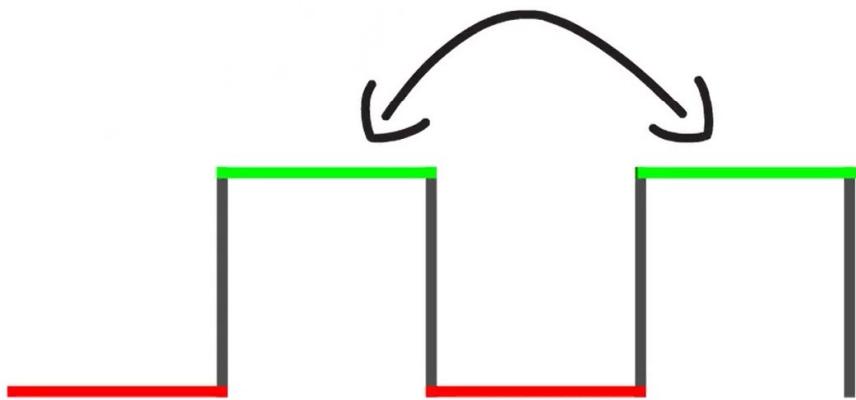
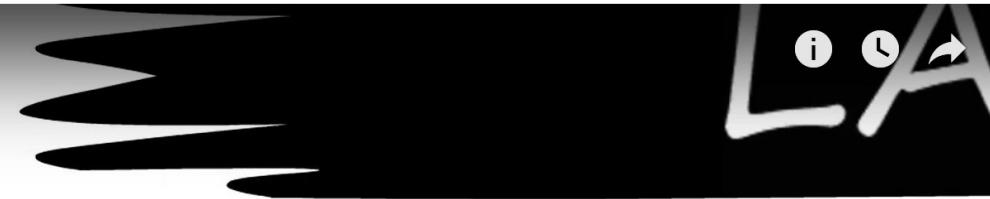
Open Switch



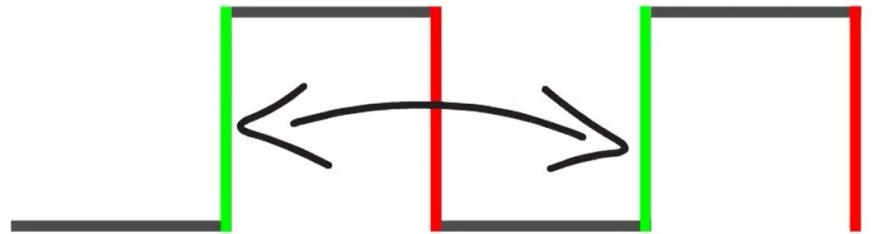
# POSITIVE LEVEL SENSITIVE D-LATCH



(For Negative Level sens.)

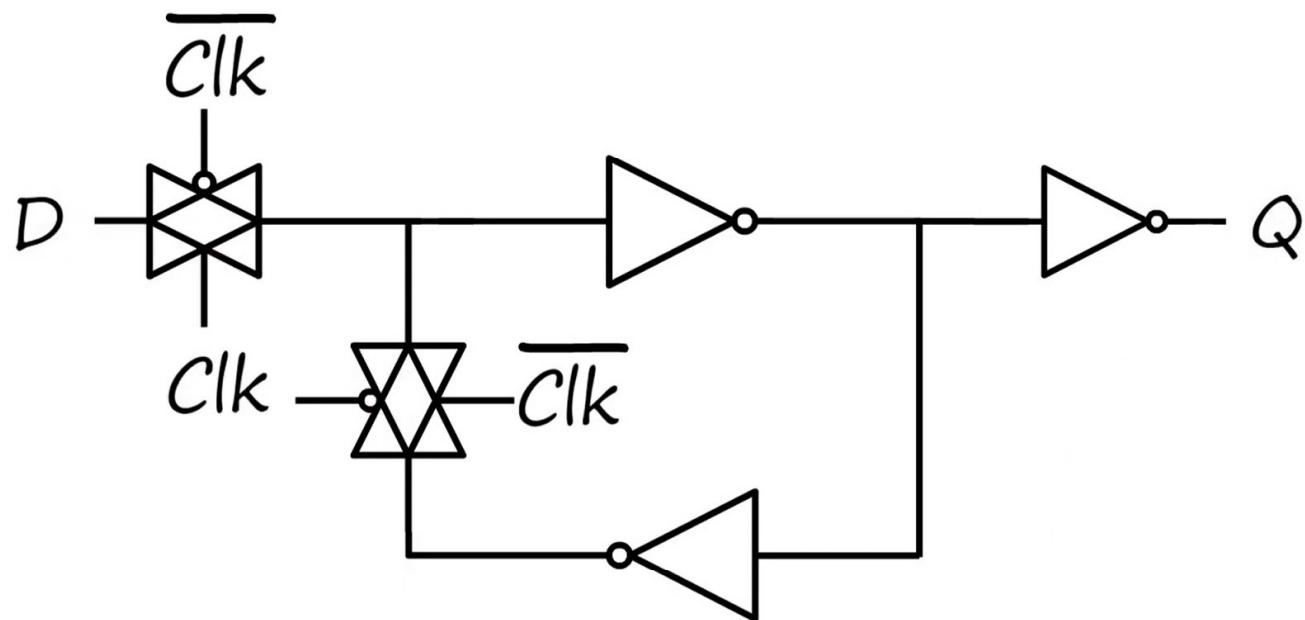


*Latch : Level Sensitive*



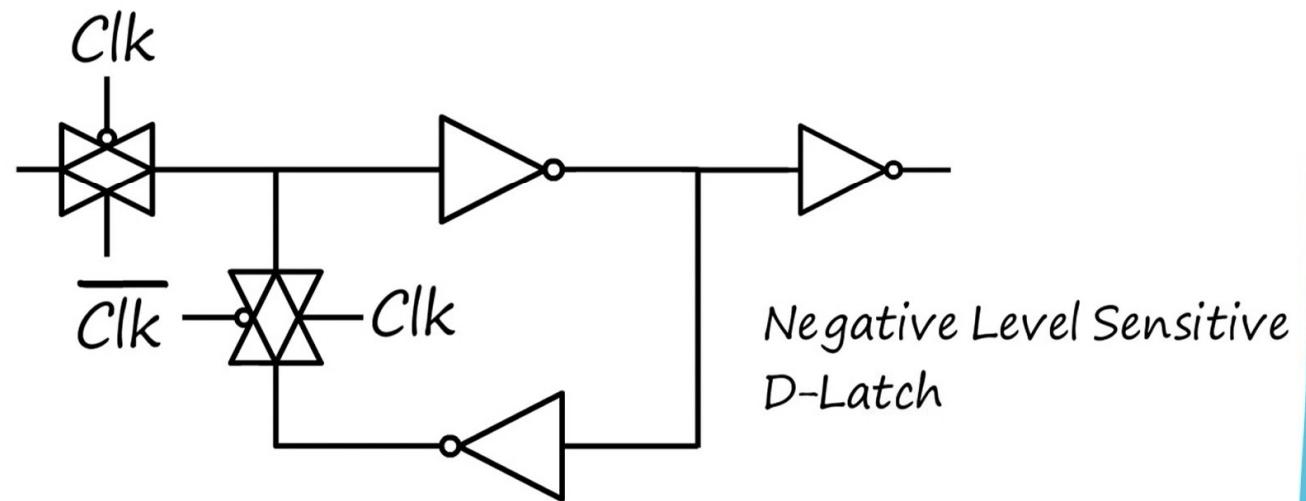
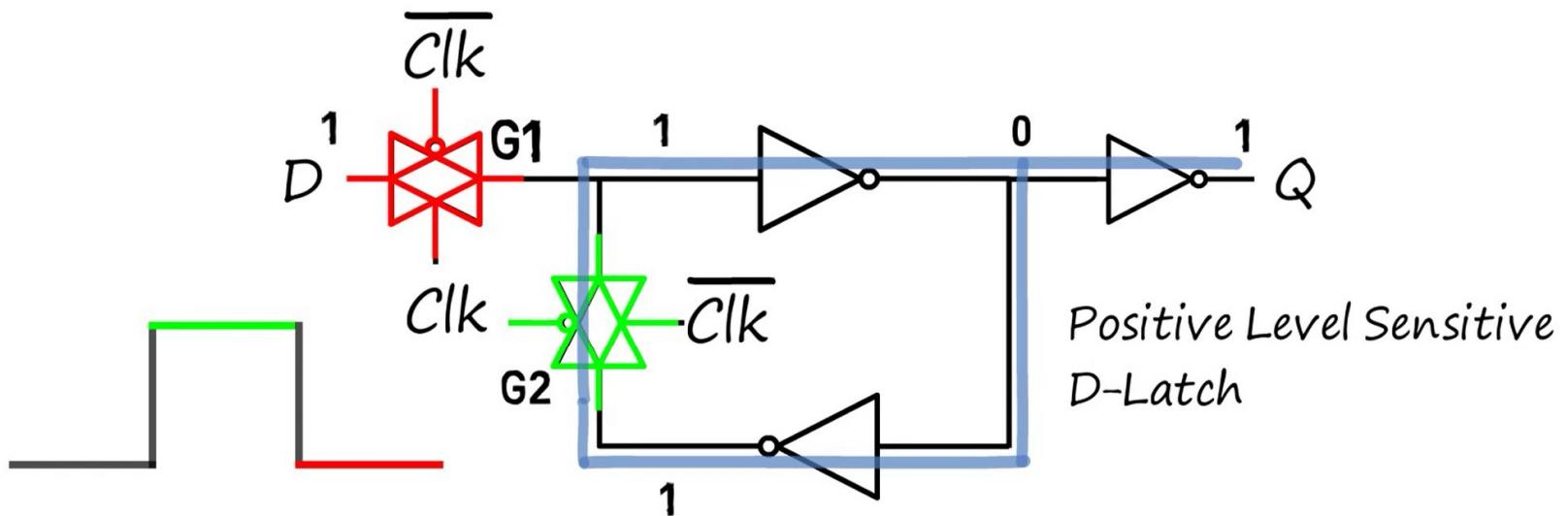
*Flip Flop : Edge Sensitive*

# INTERNAL STRUCTURE OF A LATCH

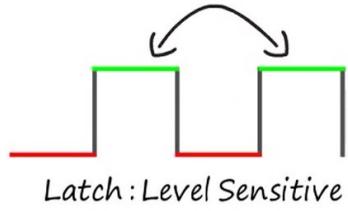


itive

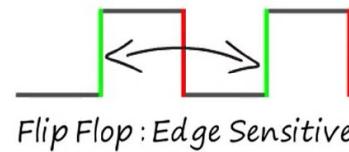
CH



# LATCH

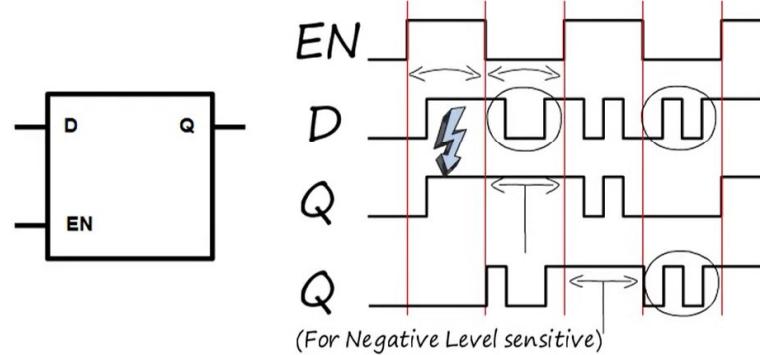


Latch : Level Sensitive

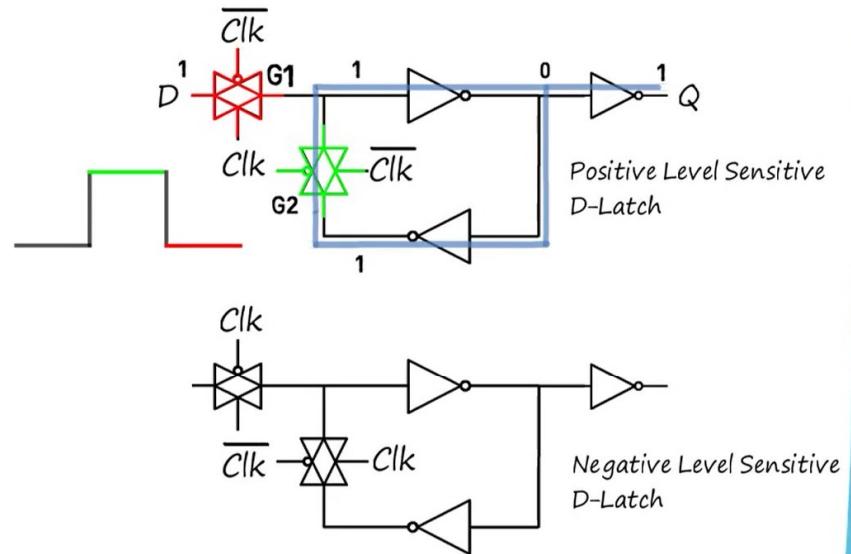


Flip Flop : Edge Sensitive

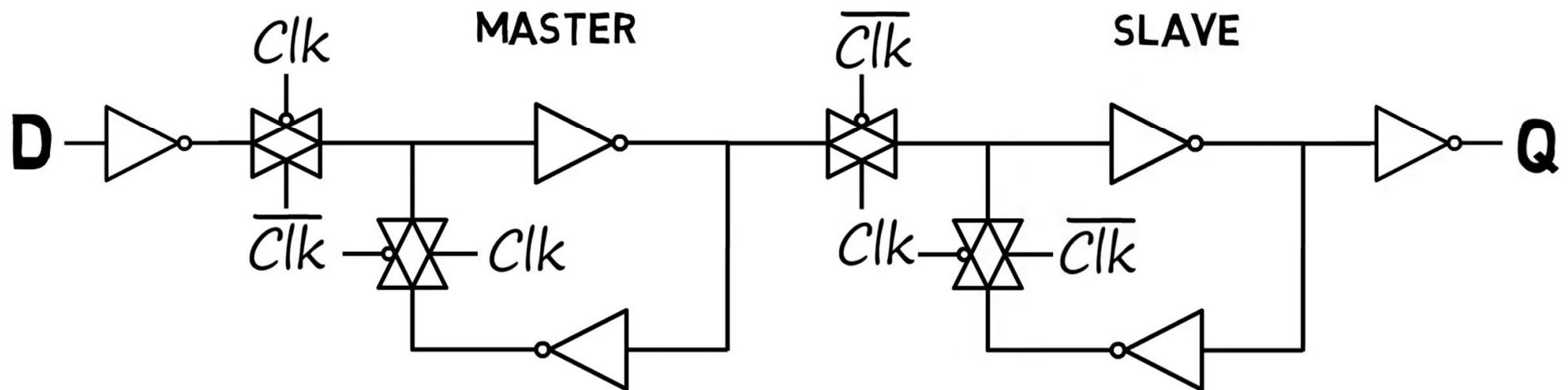
## POSITIVE LEVEL SENSITIVE D-LATCH



## INTERNAL STRUCTURE OF A LATCH

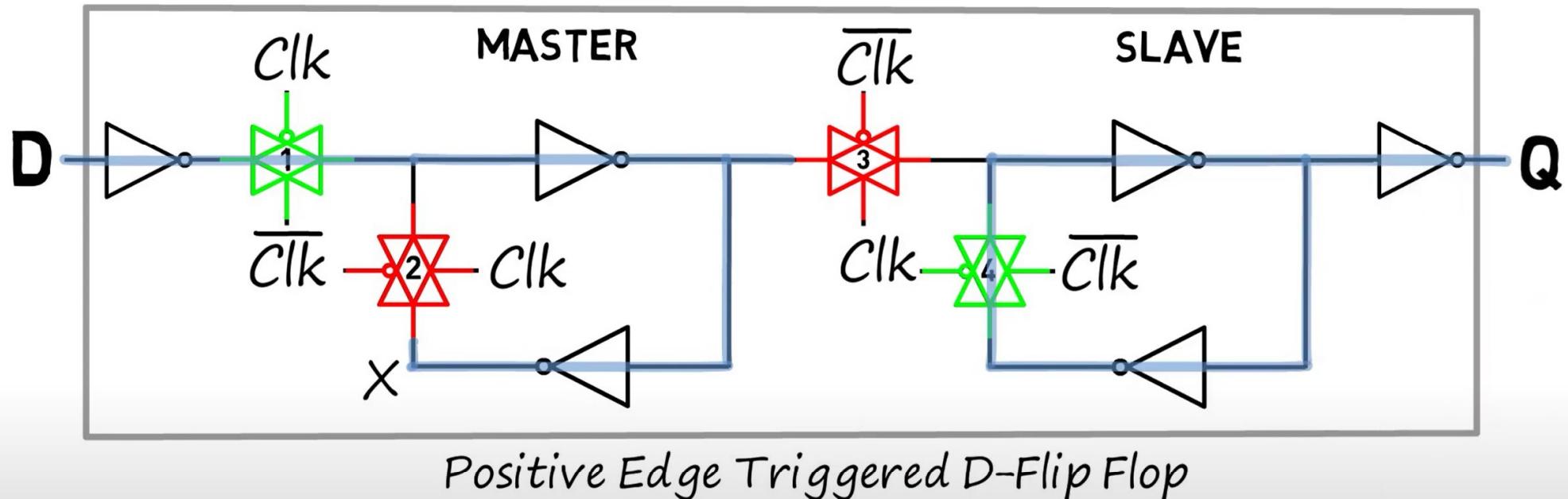


# Flip Flop



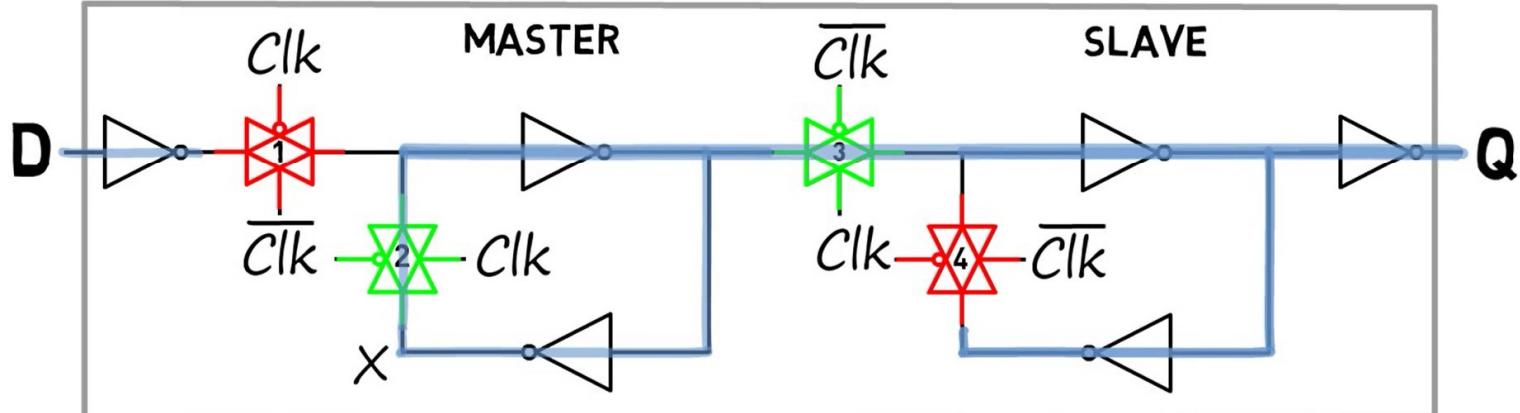
Positive Edge Triggered D-Flip Flop

# Flip Flop



**Clk**

# Flip Flop



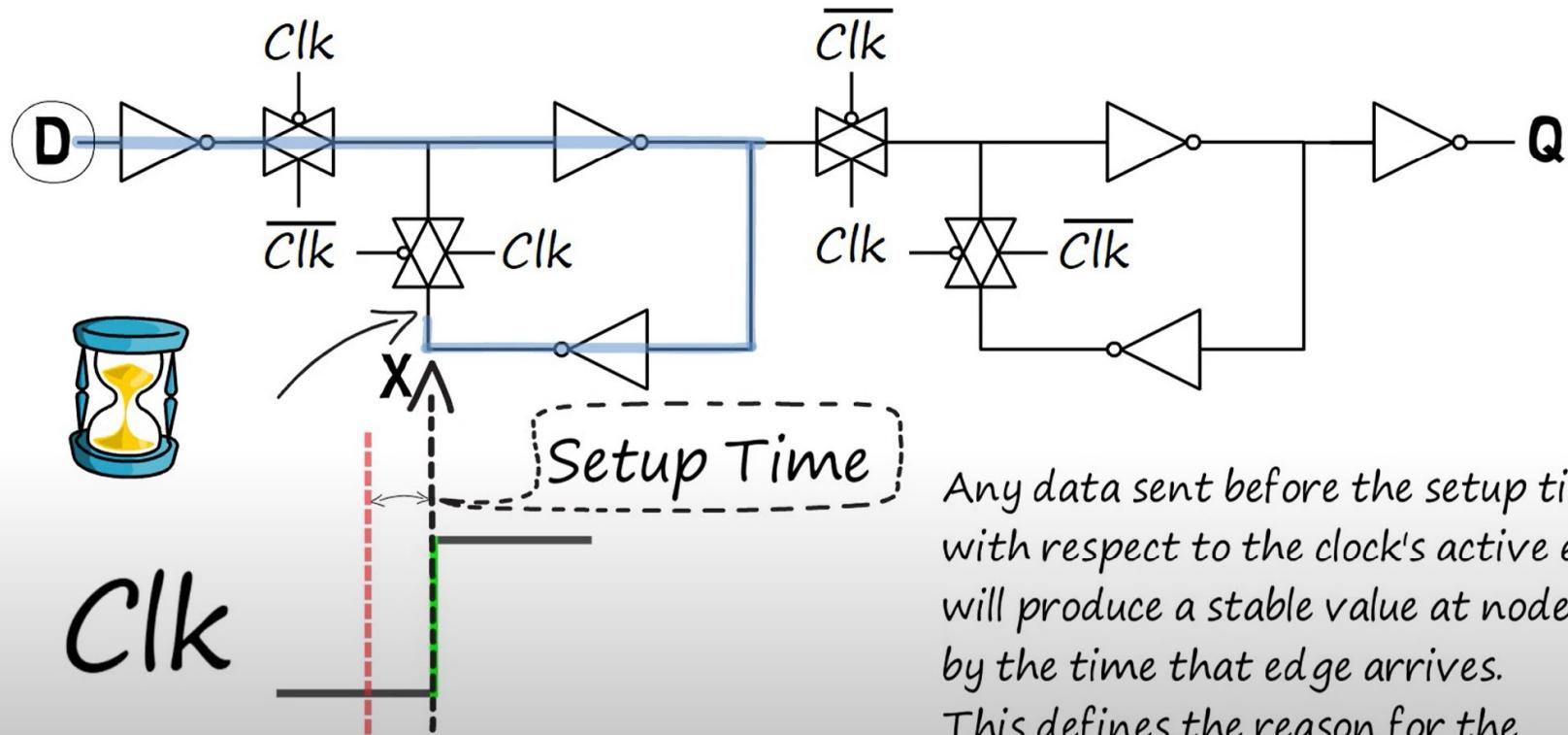
Positive Edge Triggered D-Flip Flop

$Clk$



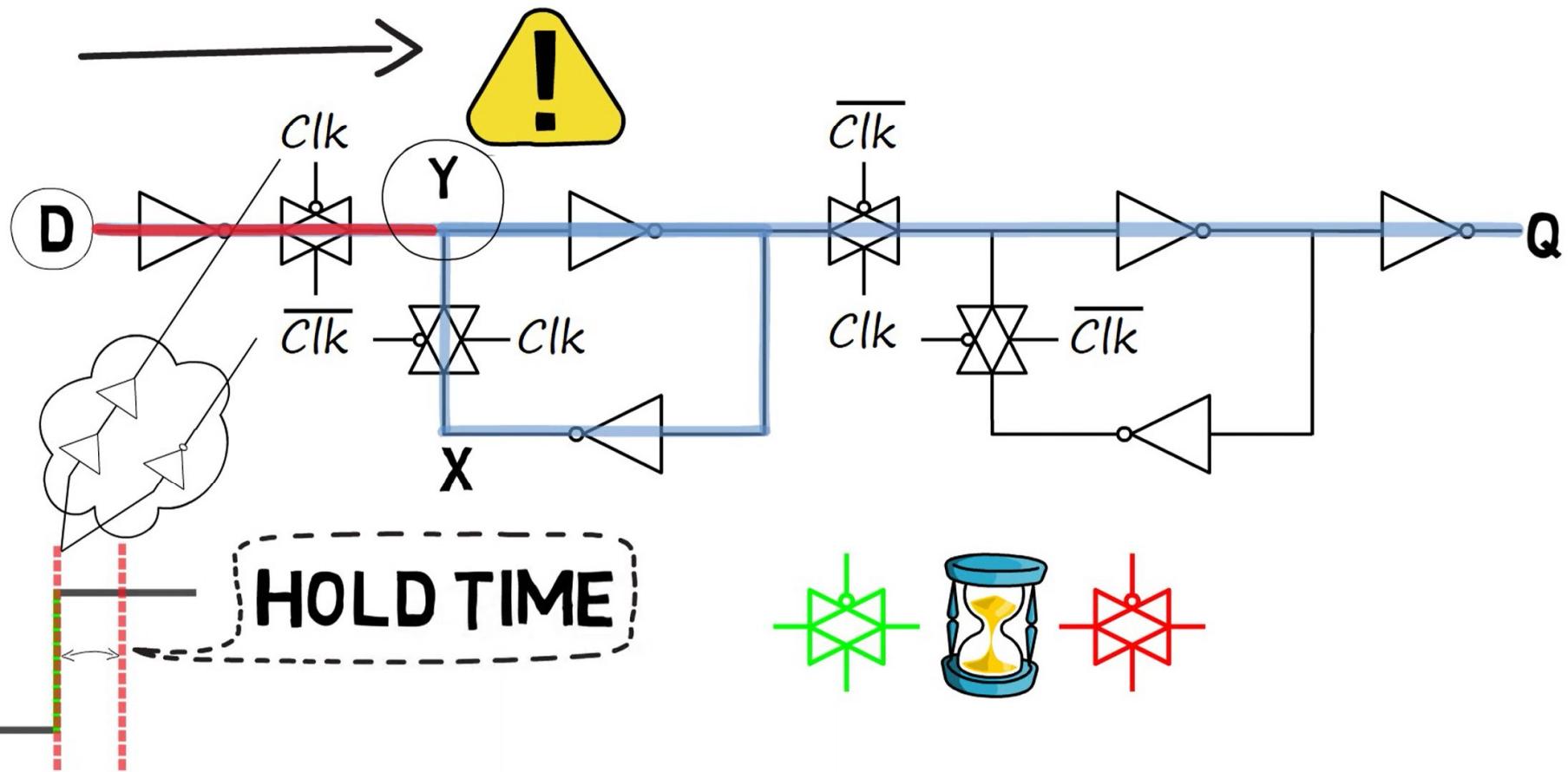
When the  $Clk$  goes LOW, the Slave latching circuit is enabled and there is no change in output. Any change in input is reflected at node  $X$  which is reflected in the output at the next positive edge of  $Clk$ . And this process continues.

# SETUP TIME

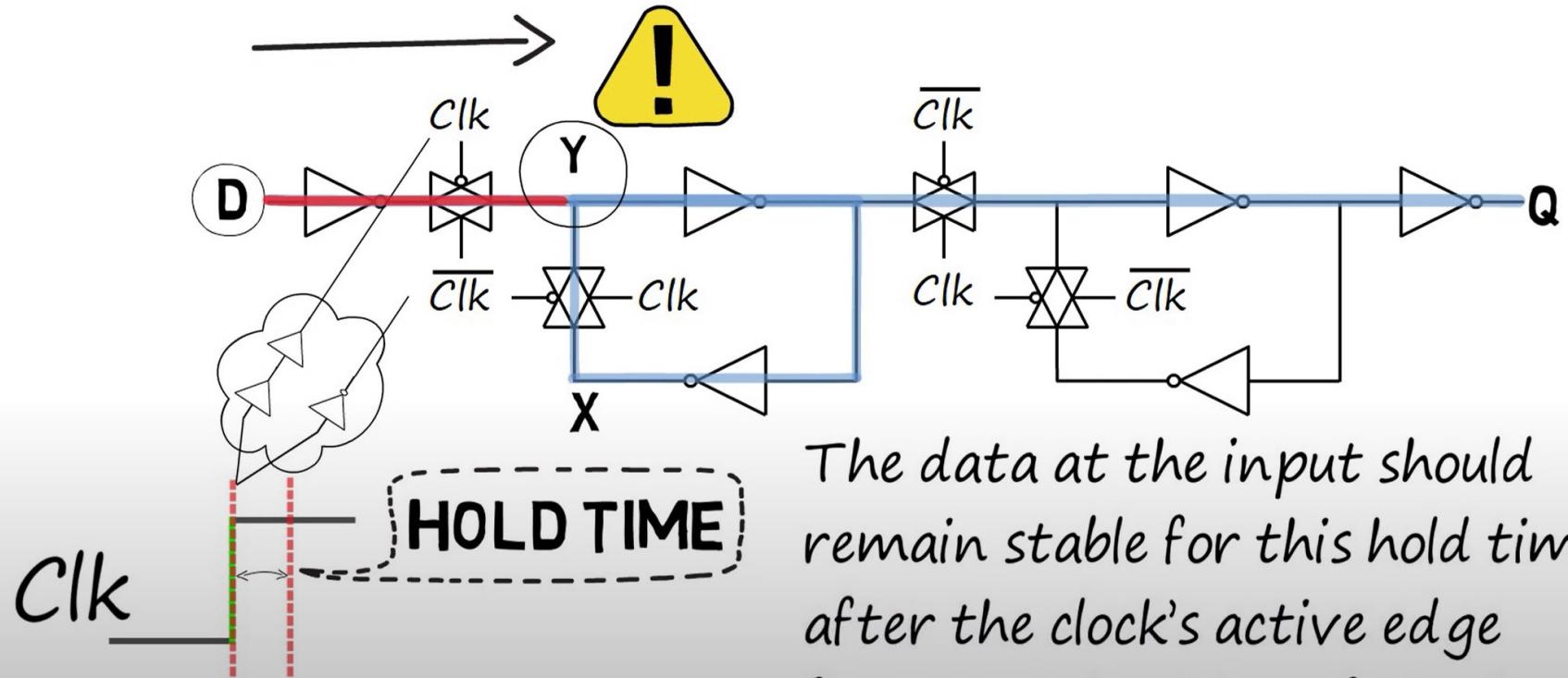


Any data sent before the setup time, with respect to the clock's active edge, will produce a stable value at node  $X$ , by the time that edge arrives. This defines the reason for the setup time within a Flip Flop.

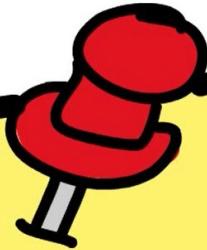
# HOLD TIME



## HOLD TIME



The data at the input should remain stable for this hold time after the clock's active edge for proper latching of the data.

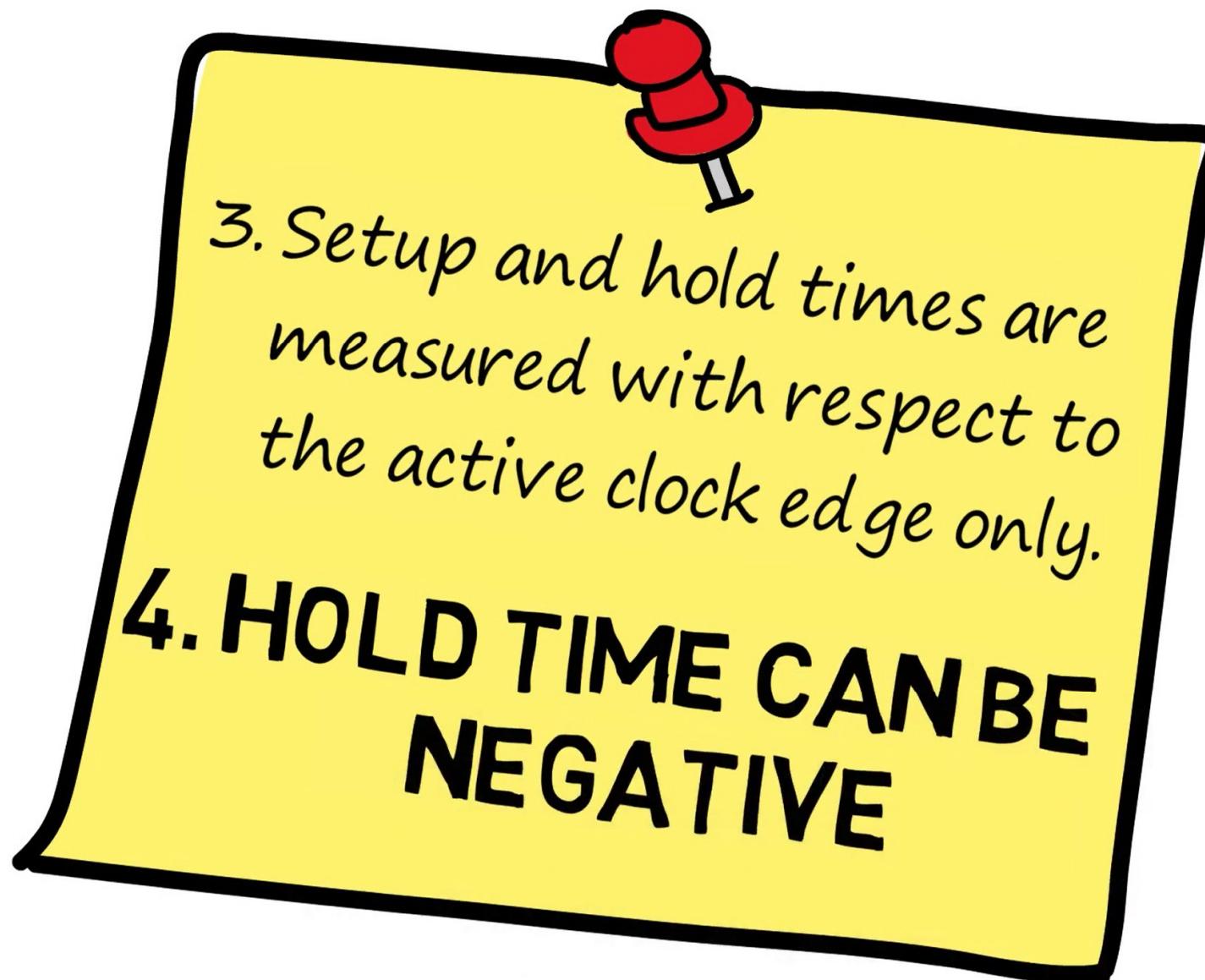
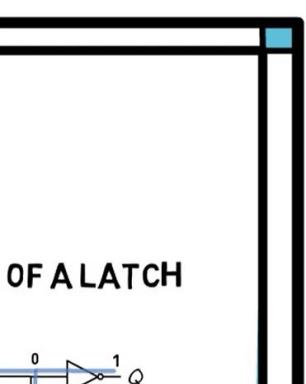
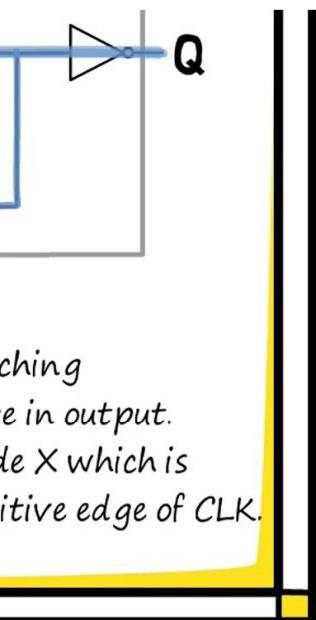


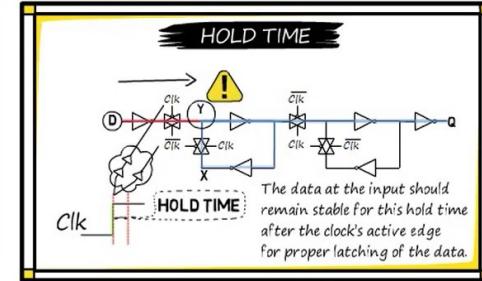
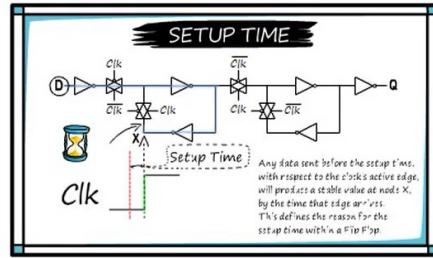
1. Setup violation may cause incorrect data to be captured
2. Hold Violation may cause incorrect data to be latched

D

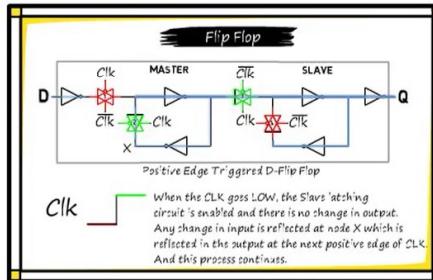
Clk

Latch : Level Ser

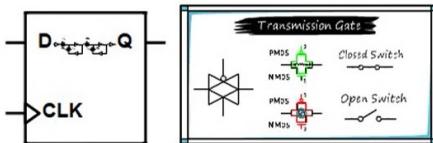
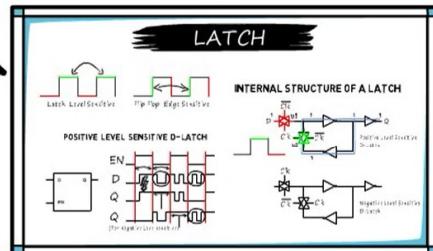
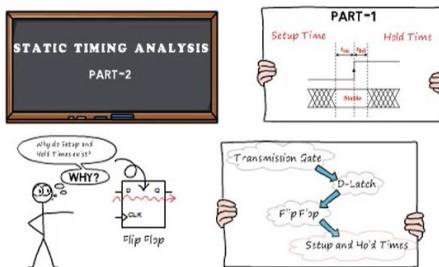




1. Setup violation may cause incorrect data to be captured
2. Hold Violation may cause incorrect data to be latched



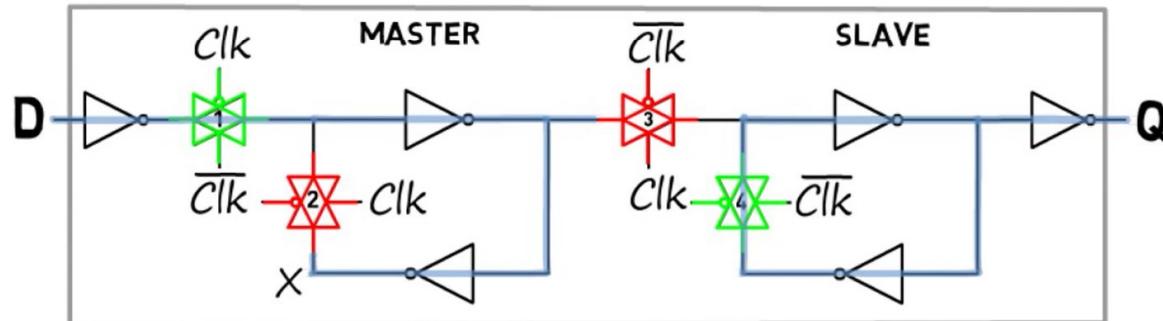
3. Setup and hold times are measured with respect to the active clock edge only.
4. **HOLD TIME CAN BE NEGATIVE**



# **STATIC TIMING ANALYSIS**

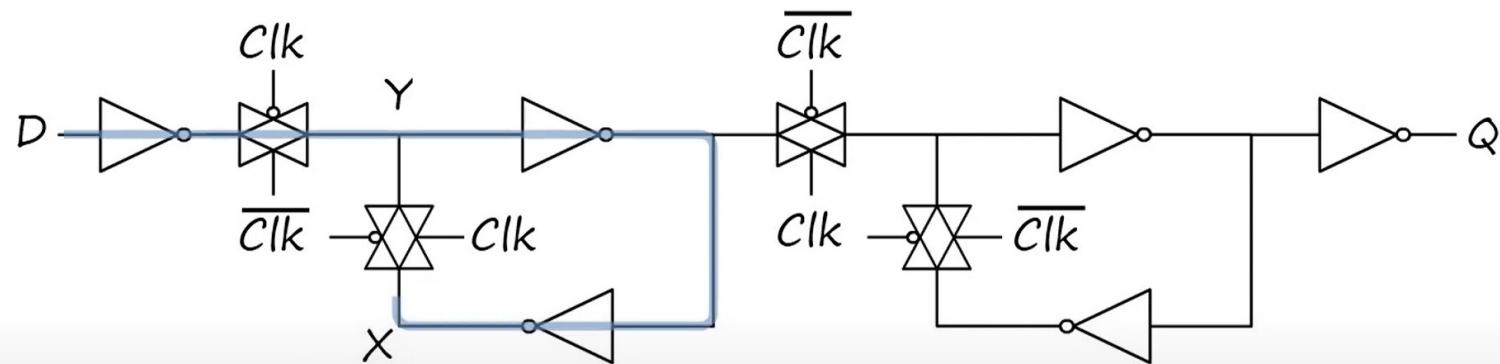
**PART-3**

## PART-2



Reason for Existence of  
Setup and Hold Times

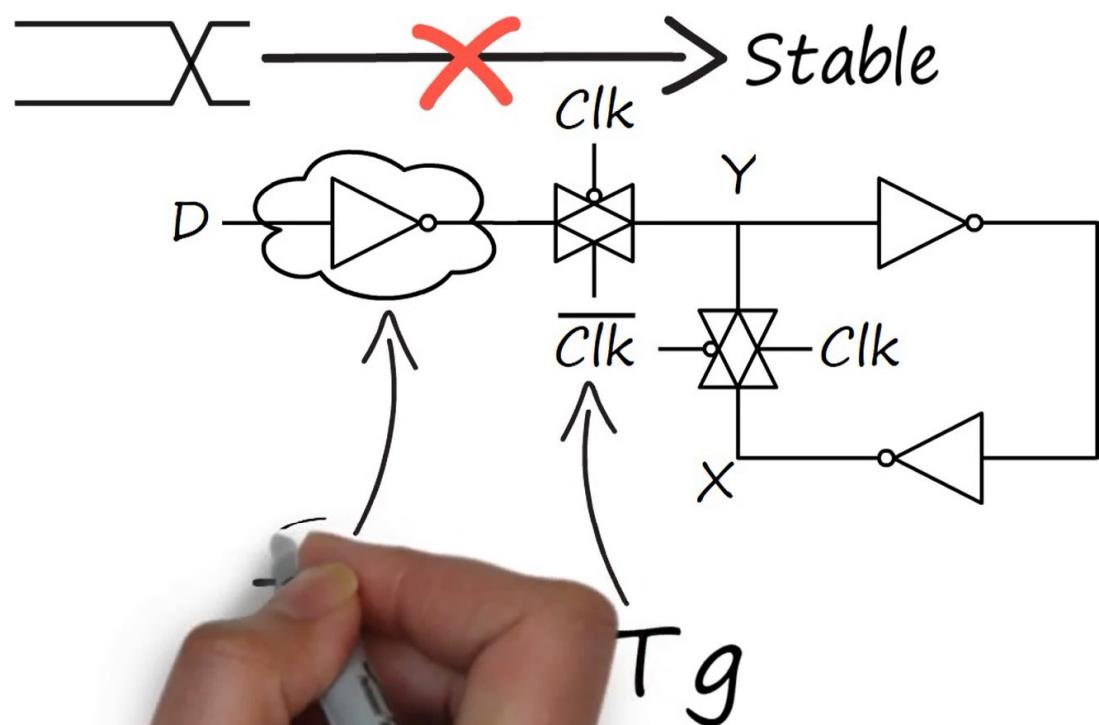
Setup Time is always Positive



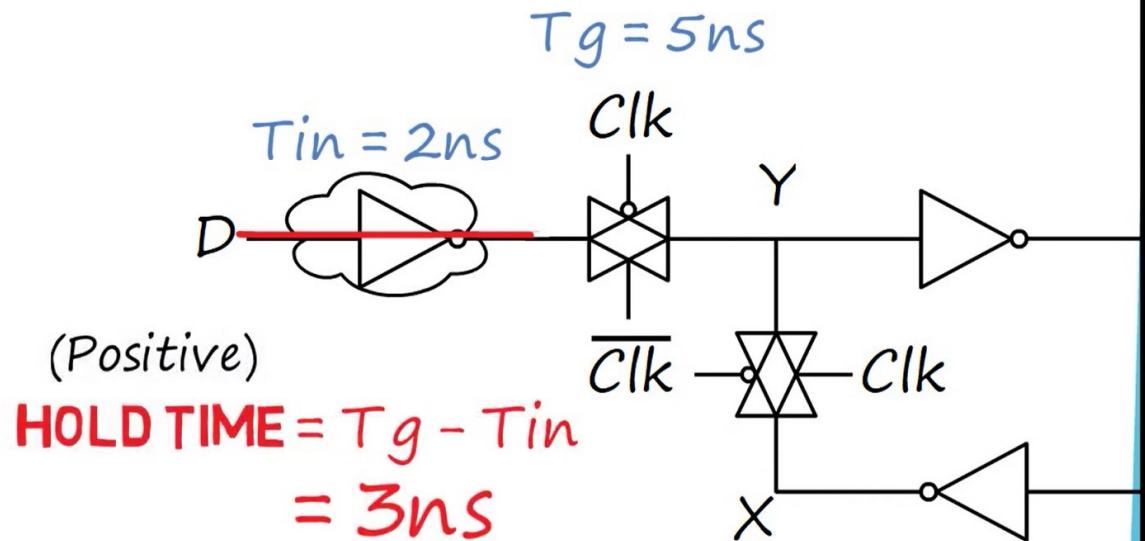
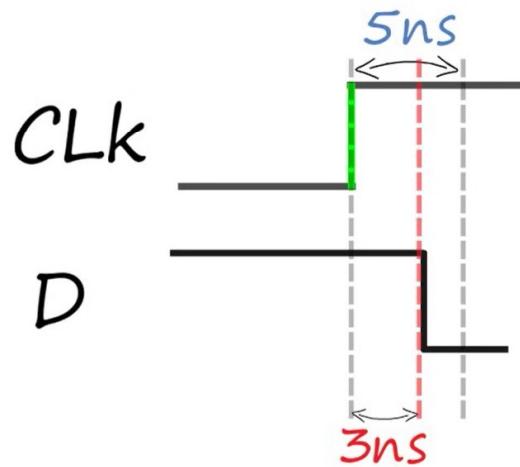
# 2 Different Delays

For how long the data at the input needs to be stable after the active edge of the clock.

This is to avoid corrupting the already present data at node Y that needs to be latched at that edge.

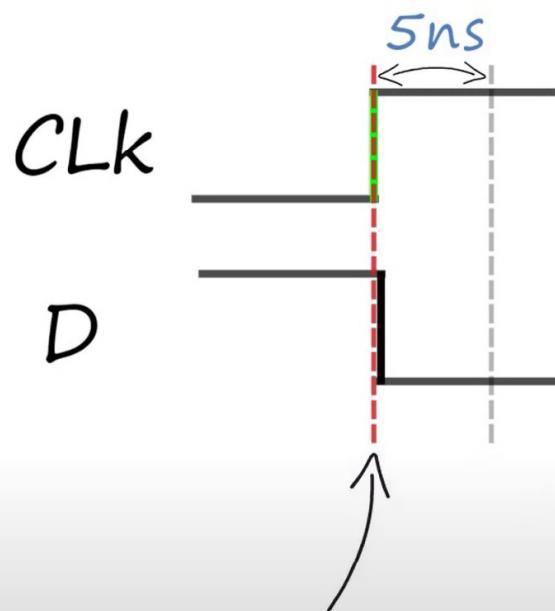


## Case 1: $Tg > Tin$

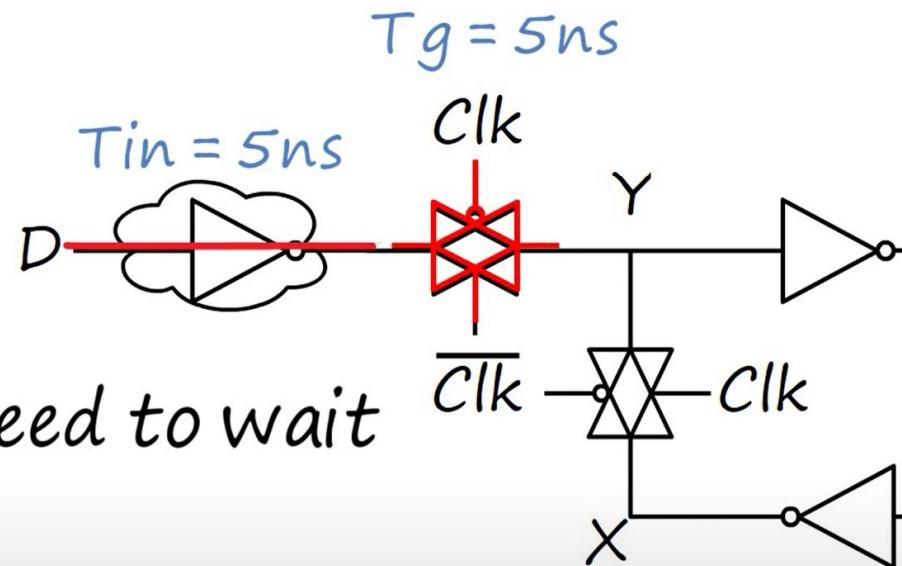


If we are able to maintain a stable value at *D* for only 3ns after the clock edge, any change afterwards will take 2ns to reach the transmission gate and by that time it would have turned off completely.

Case 2 :  $Tg = Tin$

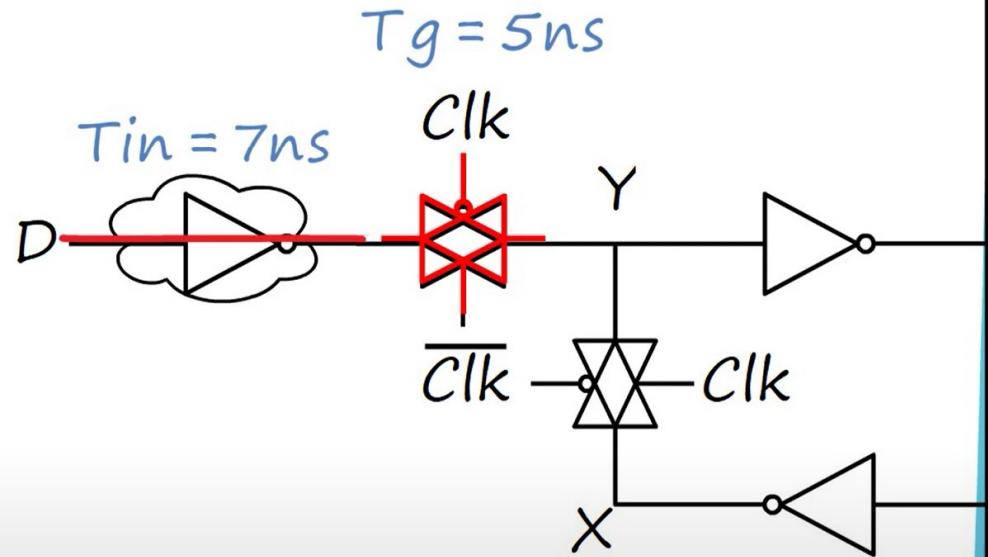
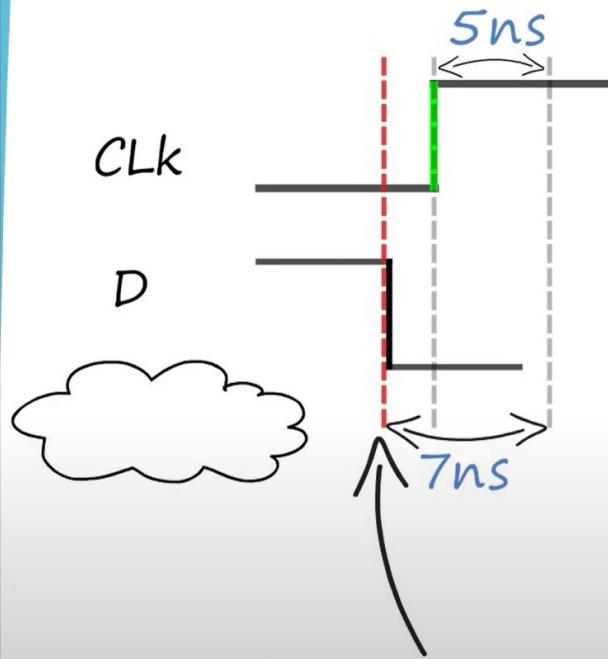


No need to wait



$$\text{HOLD TIME} = Tg - Tin = 0$$

## Case 3: $Tg < Tin$



$$\text{HOLD TIME} = Tg - Tin = -2\text{ns}$$

(Negative)

# Summary Of Hold Time

$$\text{Hold Time} = T_g - T_{in}$$

1.  $T_g > T_{in}$  : **POSITIVE**

2.  $T_g = T_{in}$  : **ZERO**

3.  $T_g < T_{in}$  : **NEGATIVE**

## STATIC TIMING ANALYSIS

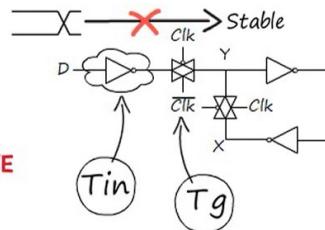
### PART-3

# NEGATIVE HOLD TIME

For how long the data at the input needs to be stable after the active edge of the clock.

This is to avoid corrupting the already present data at node Y that needs to be latched at that edge.

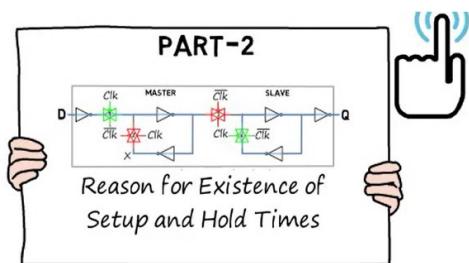
**POSITIVE**      **NEGATIVE**  
ZERO



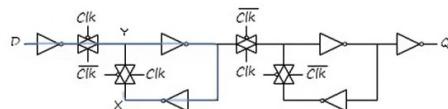
## Summary Of Hold Time

$$\text{Hold Time} = T_g - T_{in}$$

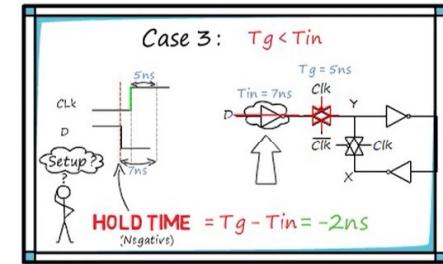
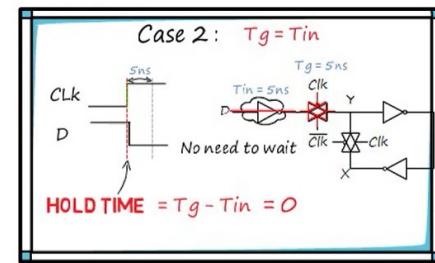
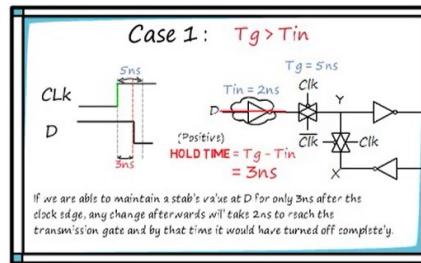
1.  $T_g > T_{in}$ : **POSITIVE**
2.  $T_g = T_{in}$ : **ZERO**
3.  $T_g < T_{in}$ : **NEGATIVE**



Setup Time is always Positive

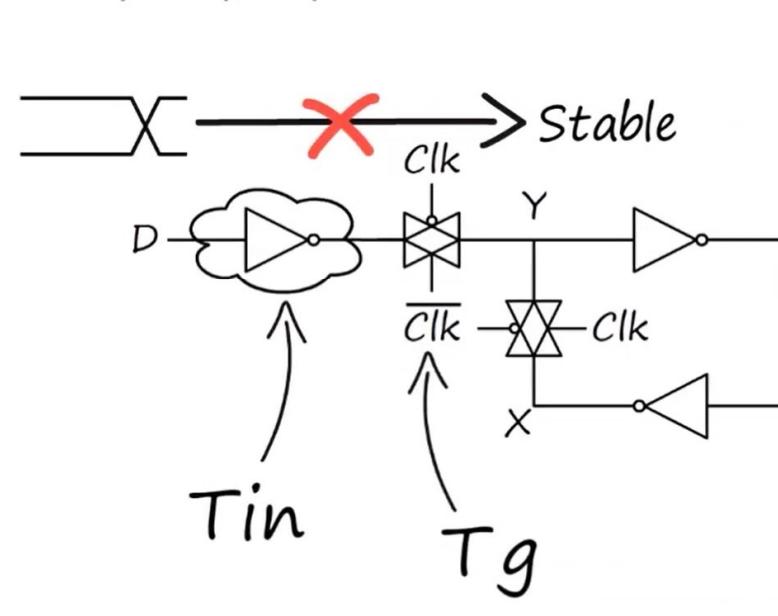
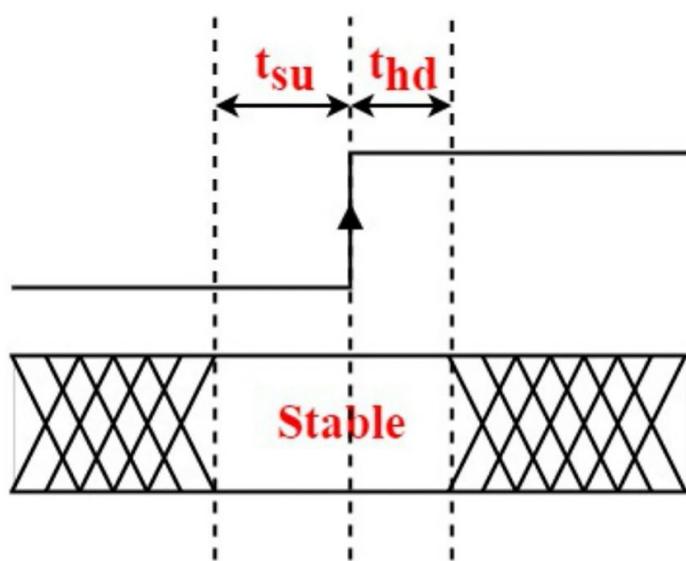
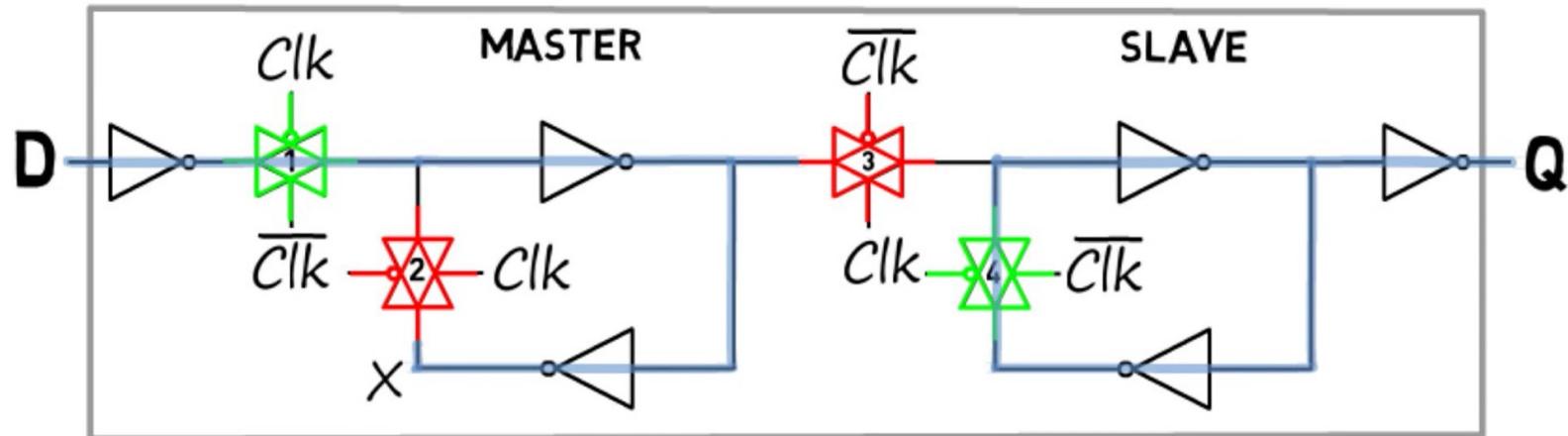


2 Different Delays



# **STATIC TIMING ANALYSIS**

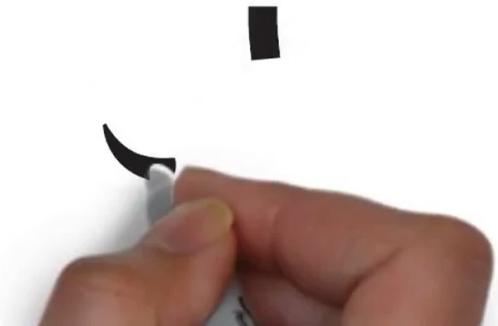
## **PART-4**



# **SETUP ANALYSIS AND MAXIMUM CLOCK FREQUENCY**

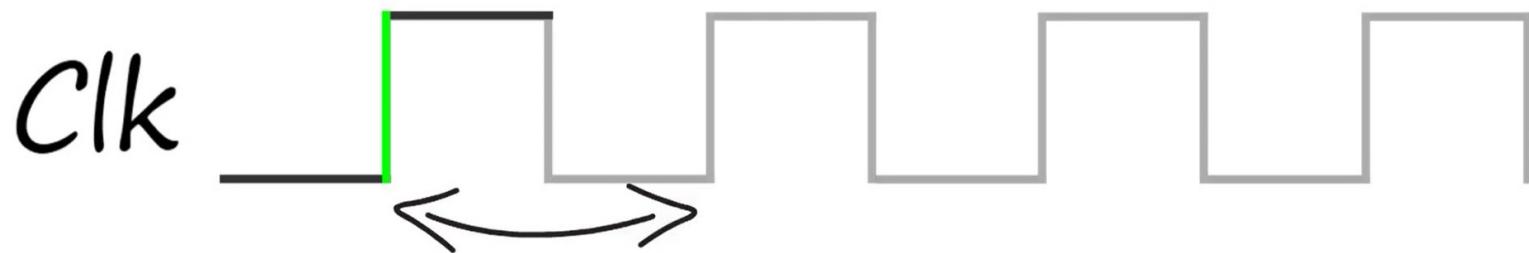
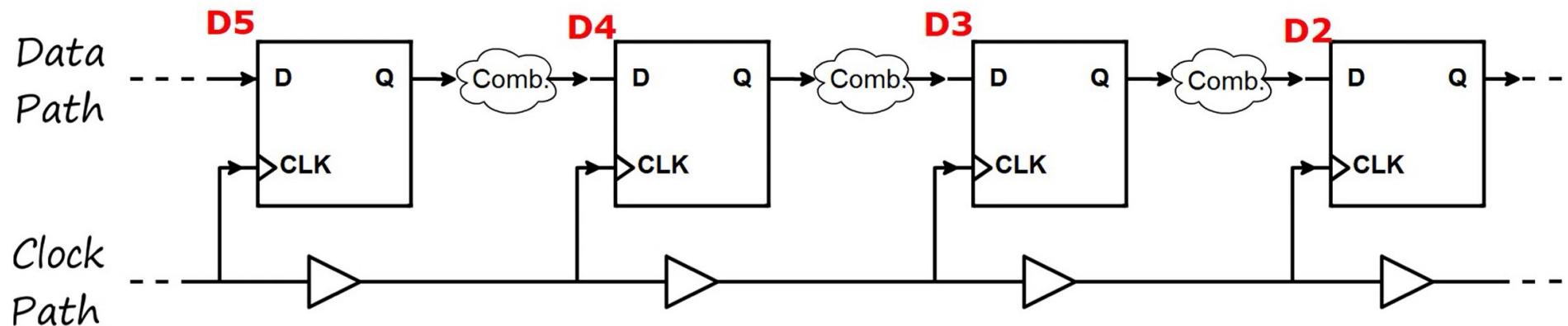
# What is STA ??

It is a method of validating the timing performance of a design by checking all possible paths for timing violations under worst case conditions.



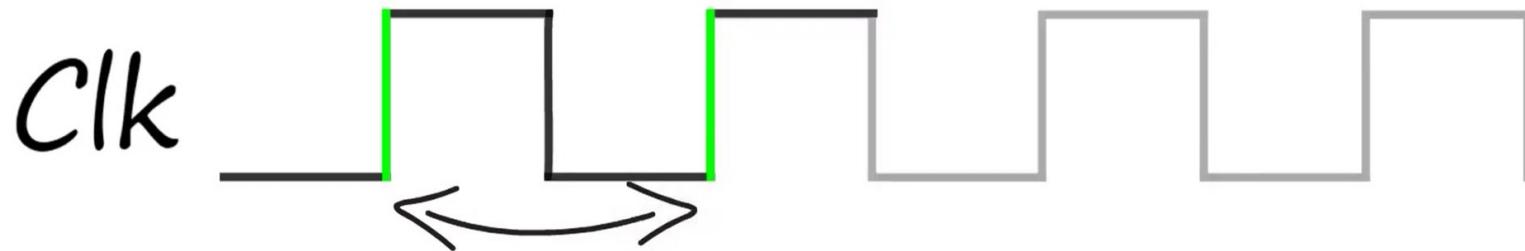
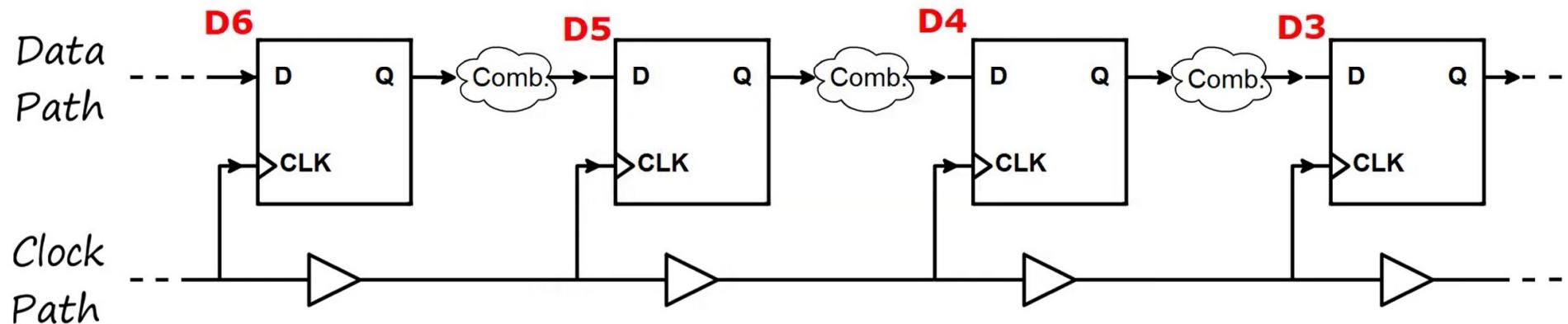
## Current State

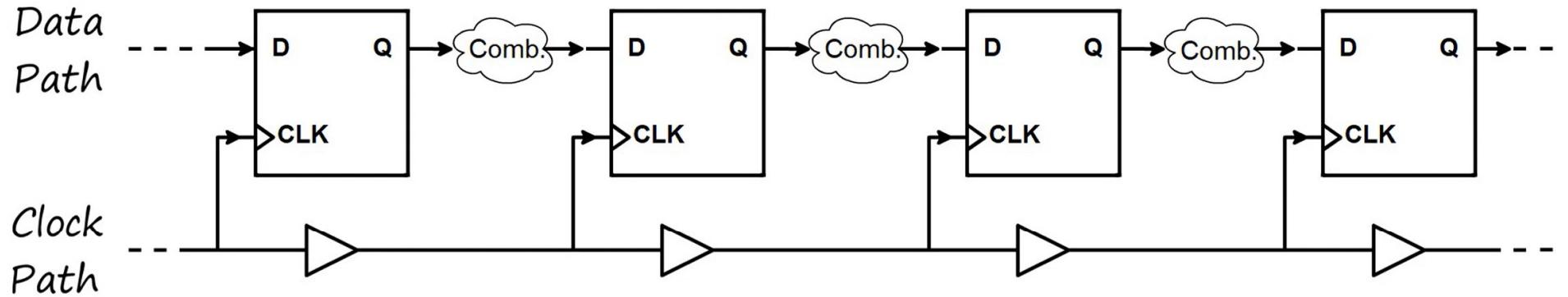
- Positive edge triggered
- Same clock everywhere



## Next State

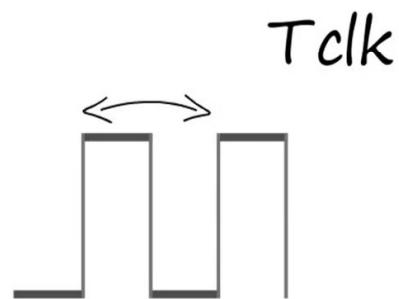
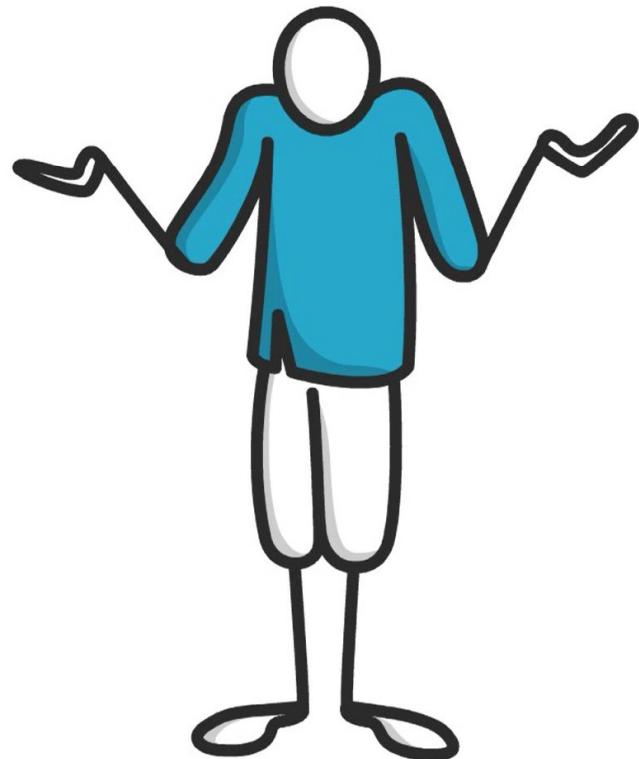
- Positive edge triggered
- Same clock everywhere





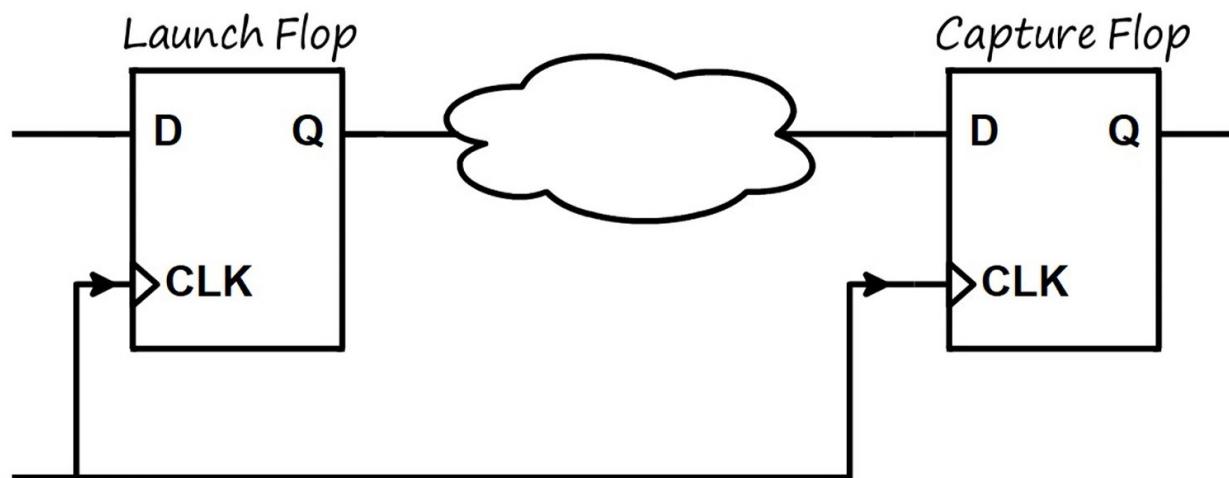
Static Timing Analysis is performed to ensure that the correct data is present at the data input of each synchronous device, when the clock edge arrives, under all possible conditions.

Time Period = 1/Frequency



**MAXIMUM  
OPERATING  
FREQUENCY**

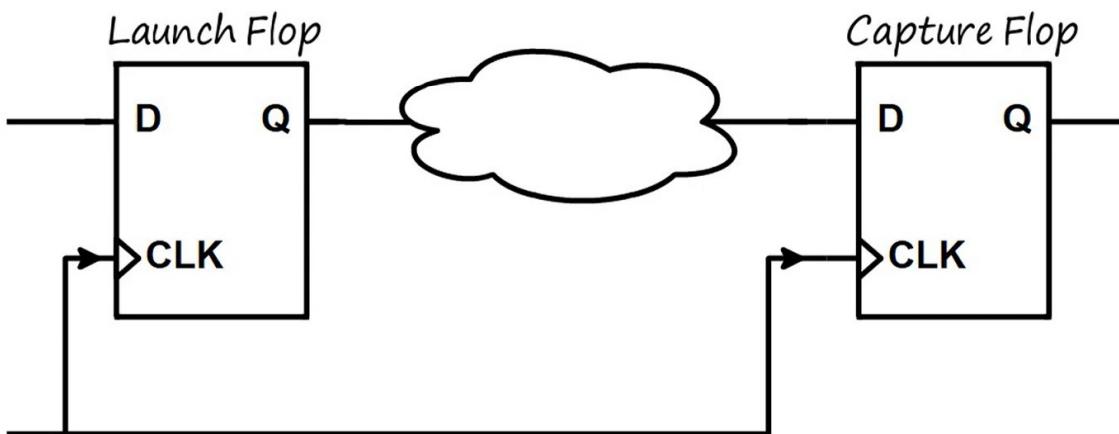
# SETUP ANALYSIS



Equation for Setup analysis

The process is more important than the final result

# SETUP ANALYSIS



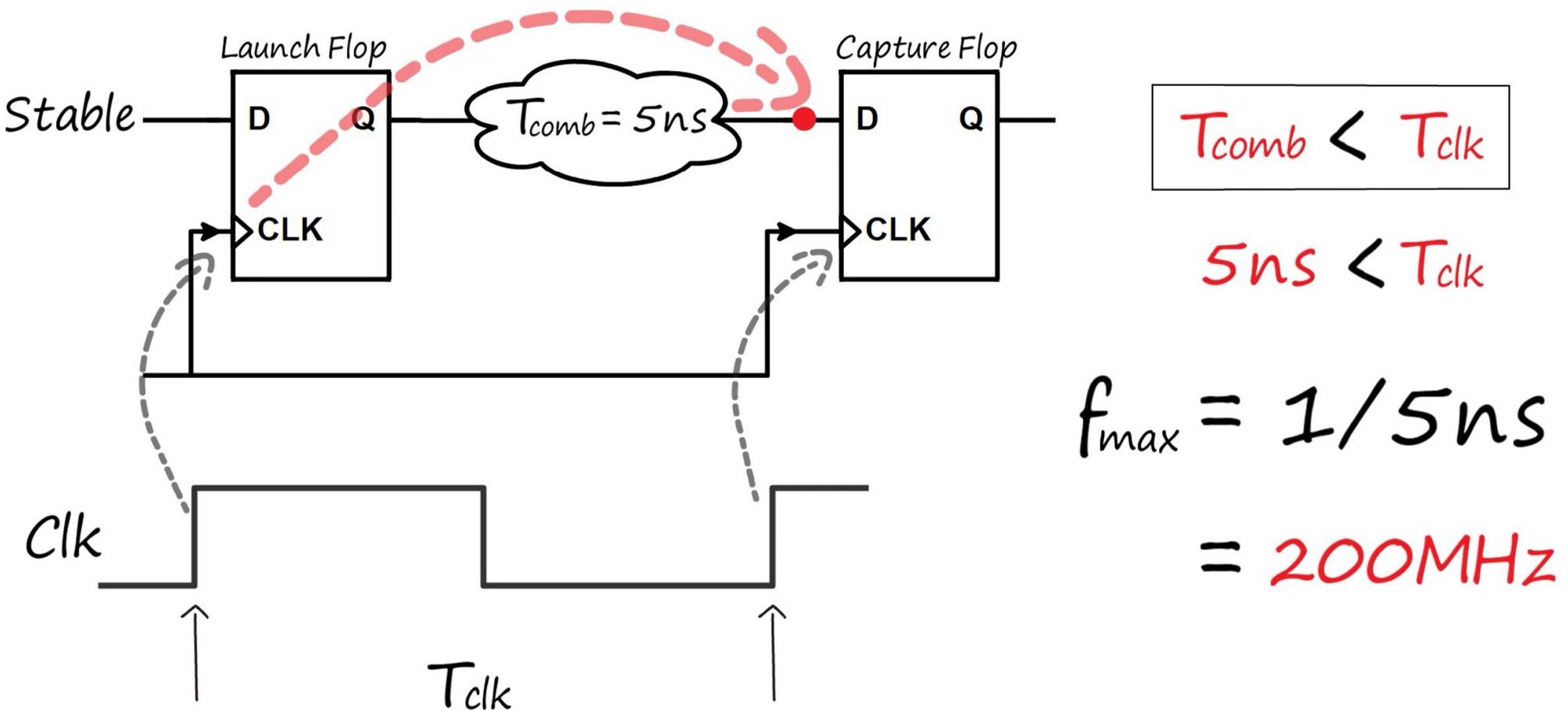
Equation for Setup analysis

## IDEAL CONDITIONS

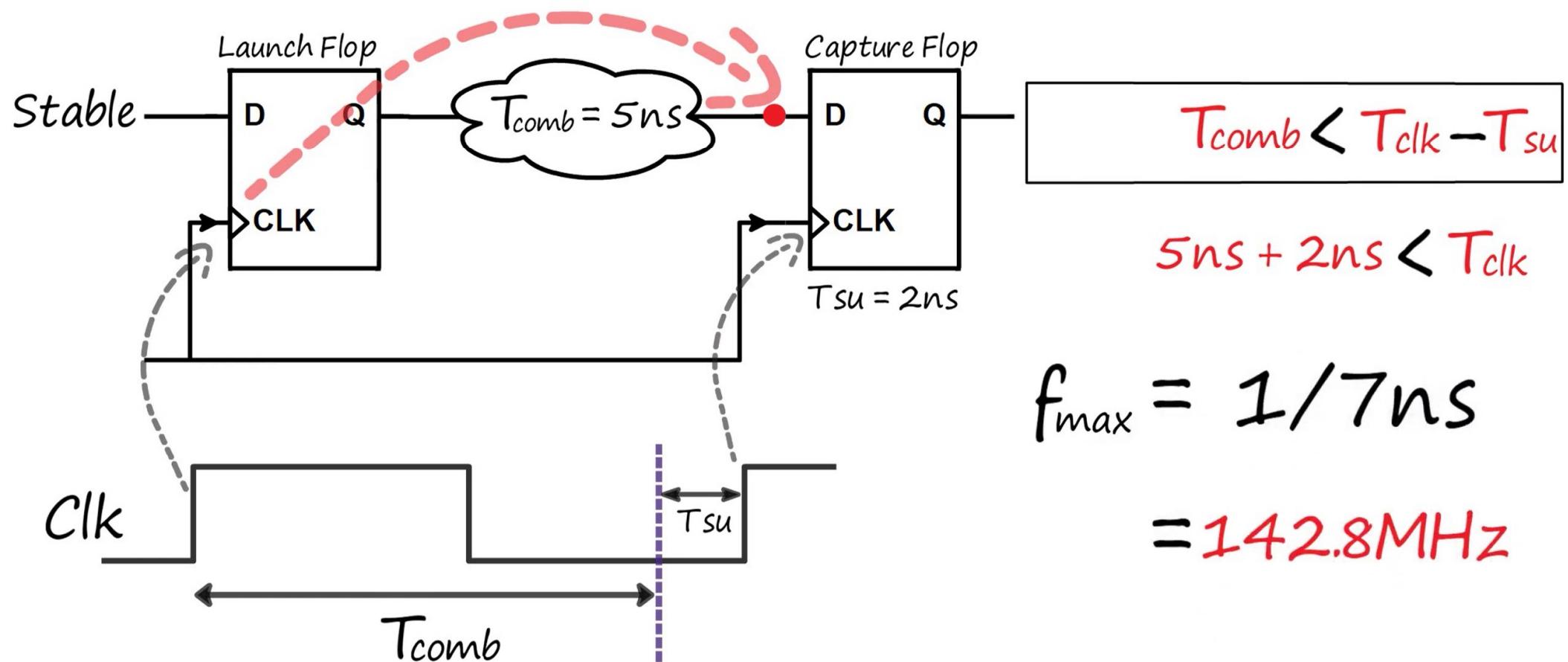
1. Clock is ideal,  
No delays in clock path
2. Zero Clock to Q delay
3. Zero Setup and Hold Times

The process is more important than the final result

# Ideal Conditions

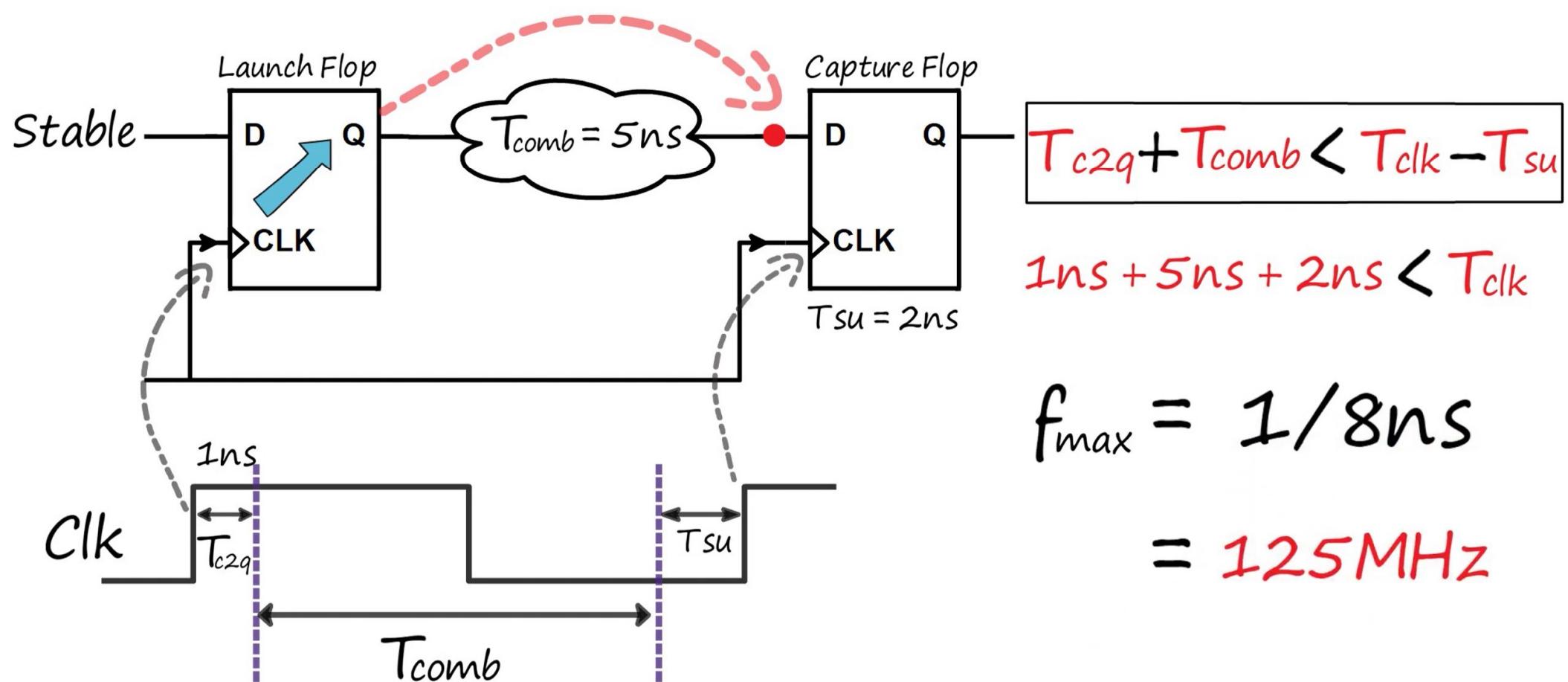


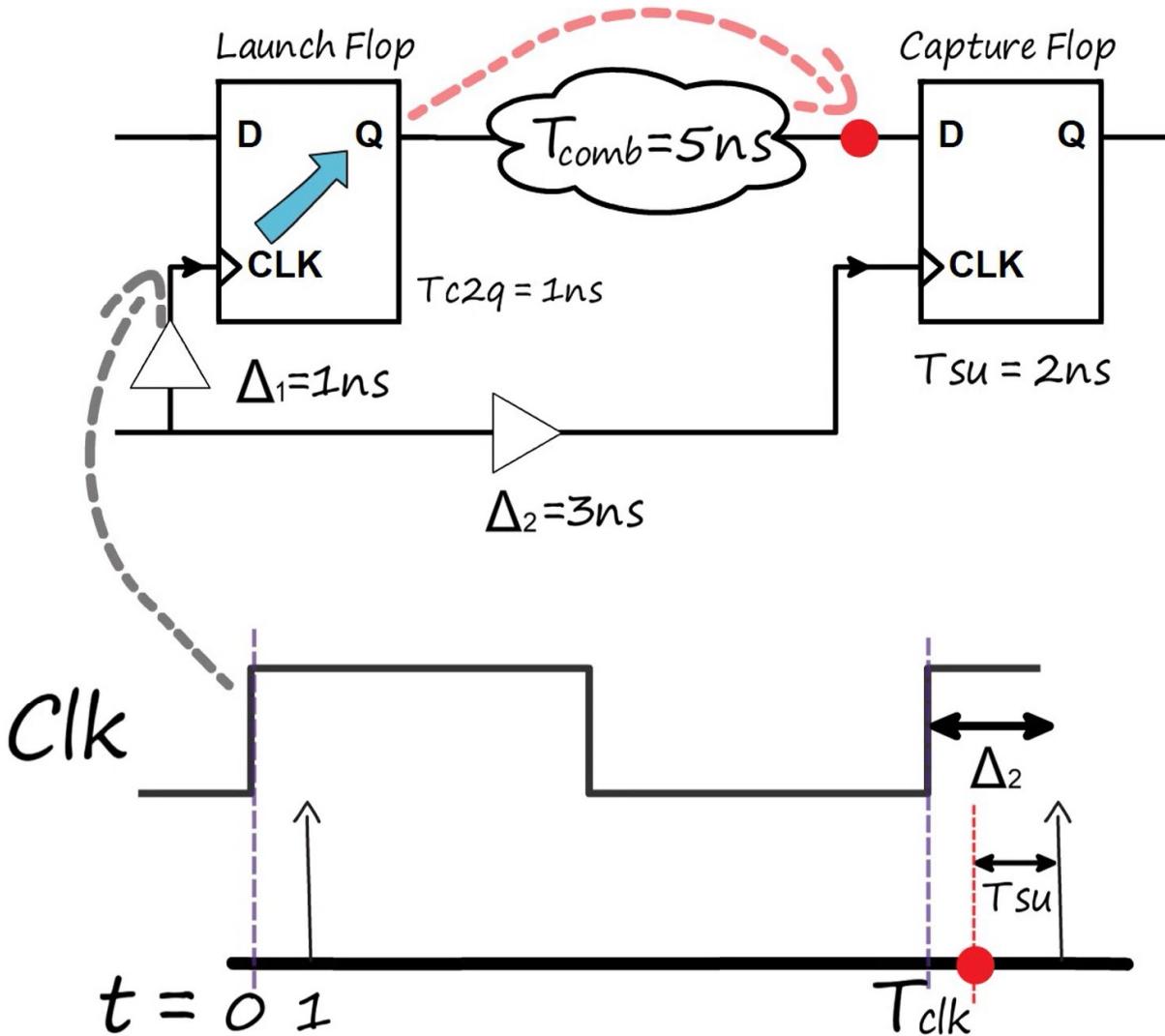
# Finite Setup Time



# Finite Setup Time

# Clock to Q delay





**DATA ARRIVAL TIME** < **DATA REQUIRED TIME**

$$\Delta_1 + T_{c2q} + T_{comb} < T_{clk} + \Delta_2 - T_{su}$$

$$1 + 1 + 5 \\ 7\text{ns}$$

DATA ARRIVAL TIME < DATA REQUIRED TIME

$$\Delta_1 + T_{c2q} + T_{comb} < T_{clk} + \Delta_2 - T_{su}$$

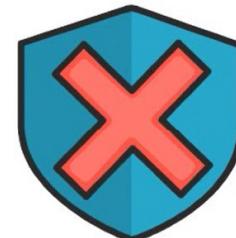
$$1 + 1 + 5 < T_{clk} + 3 - 2$$

$$7\text{ns} - 1 < T_{clk}$$

$$6\text{ns} < T_{clk}$$

$$f = 200\text{MHz}$$

$T_{clk} = 5\text{ns}$



$$\text{Max Clk Frequency} = 1/6\text{ns} = 166.67\text{MHz}$$

# SLACK

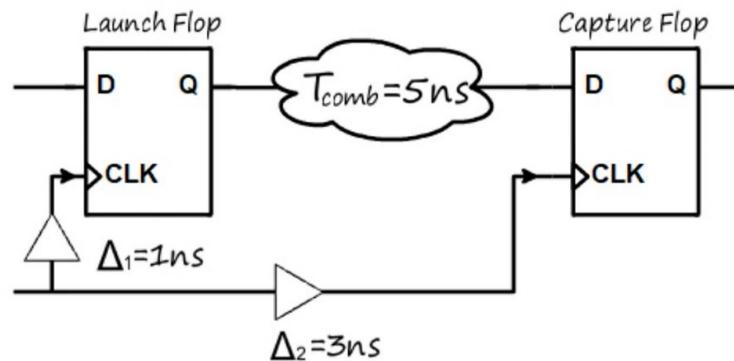
**DATA REQUIRED TIME – DATA ARRIVAL TIME**

(For Setup Analysis)

Data should arrive on or before the required time

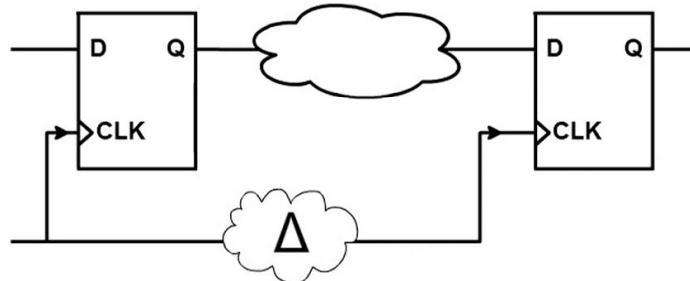
*Setup Slack  $\geq 0$*

# CLOCK SKEW



$$\Delta = \Delta_2 - \Delta_1$$

$$\Delta = 3 - 1 = 2\text{ns}$$



$$T_{\text{c2q}} + T_{\text{comb}} < T_{\text{clk}} + \Delta - T_{\text{su}}$$

# SUMMARY

Why we do Static Timing Analysis

What a sequential system looks like

Why we can't increase the clock frequency beyond a certain limit

How to calculate that maximum value of the clock frequency

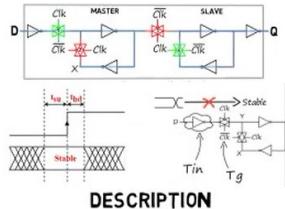
THE SETUP TIMING ANALYSIS

## STATIC TIMING ANALYSIS

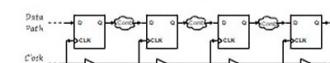
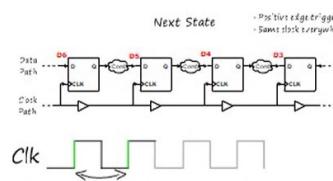
PART-4

### What is STA??

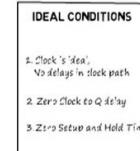
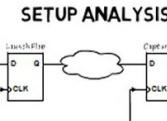
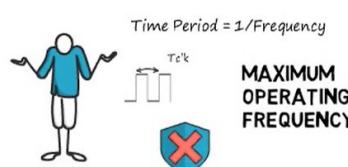
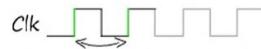
It's a method of validating the timing performance of a design by checking all possible paths for timing violations under worst case conditions.



## SETUP ANALYSIS AND MAXIMUM CLOCK FREQUENCY



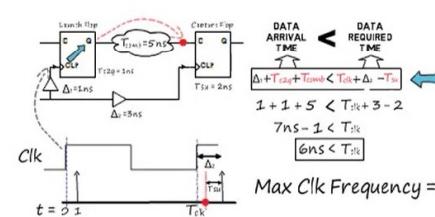
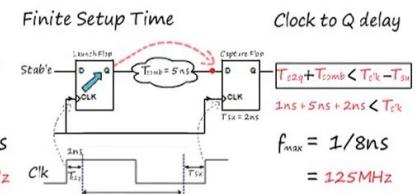
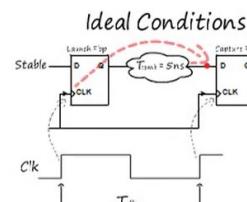
Static Timing Analysis is performed to ensure that the correct data is present at the data input of each synchronous device, when the clock edge arrives, under all possible conditions.



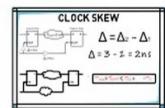
## SUMMARY

Why we do Static Timing Analysis  
What a sequential system looks like  
Why we can't increase the clock frequency beyond a certain limit

How to calculate that maximum value of the clock frequency  
THE SETUP TIMING ANALYSIS



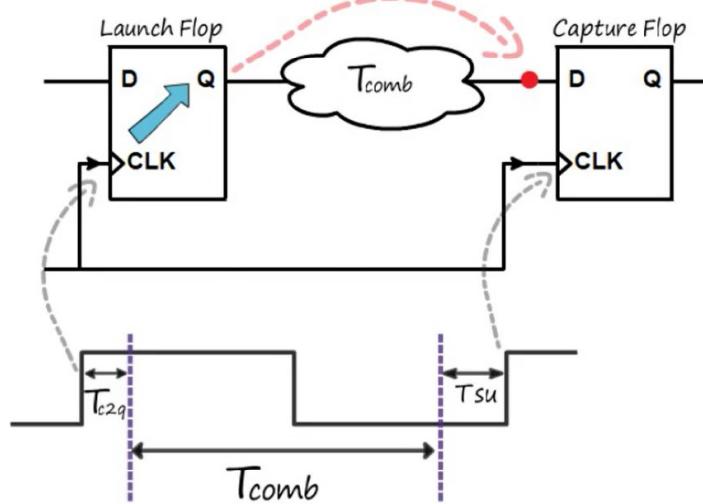
$$\text{Max Clk Frequency} = 1/6\text{ns} = 166.67\text{MHz}$$



# **STATIC TIMING ANALYSIS**

## **PART-5**

## PART-4

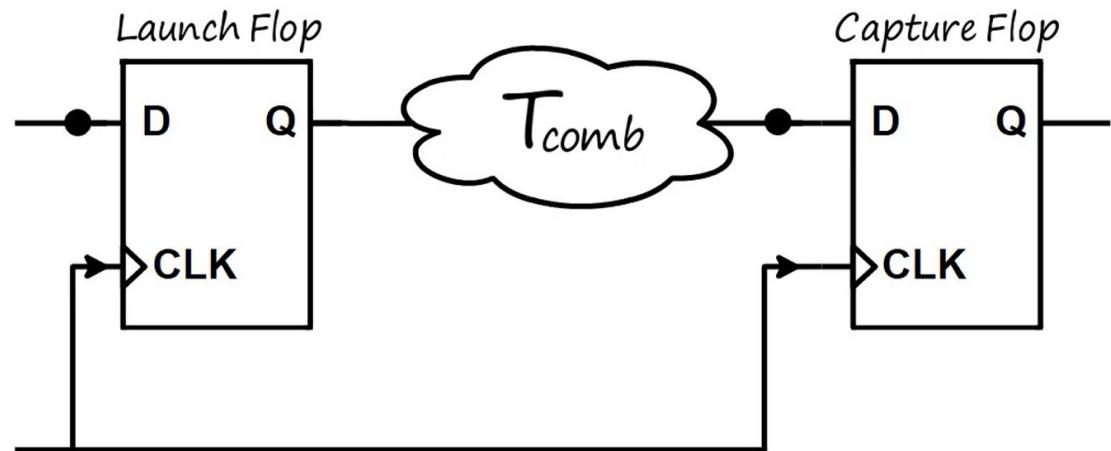
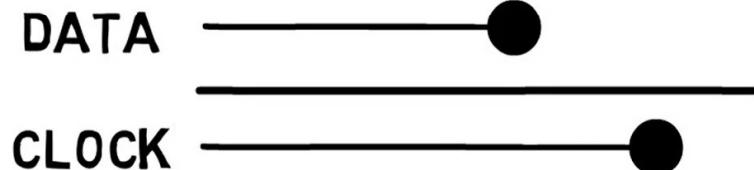
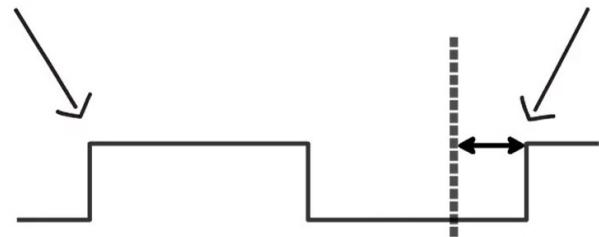


Setup Analysis and Maximum Clock Frequency

# HOLD ANALYSIS

# Setup Analysis

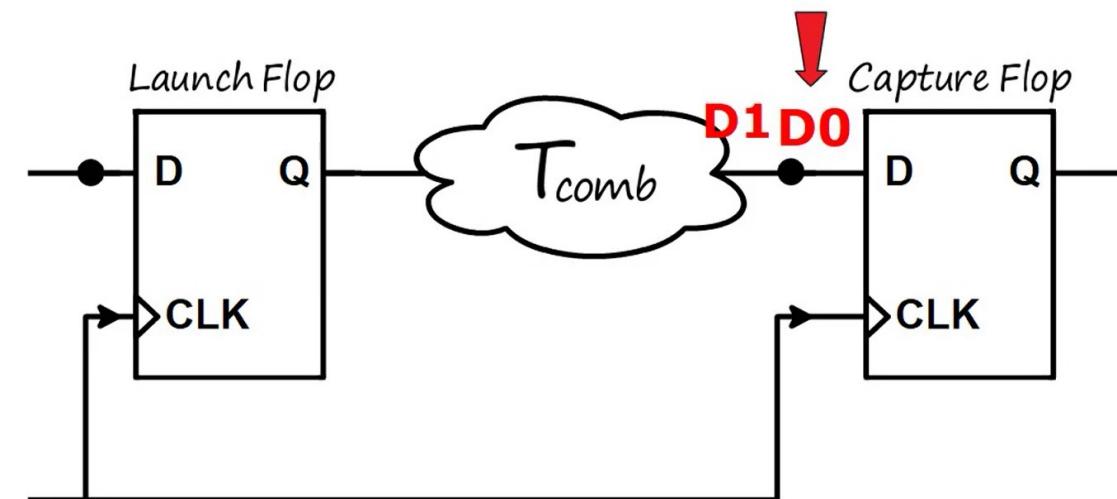
Current Clock edge



DATA  
ARRIVAL  
TIME

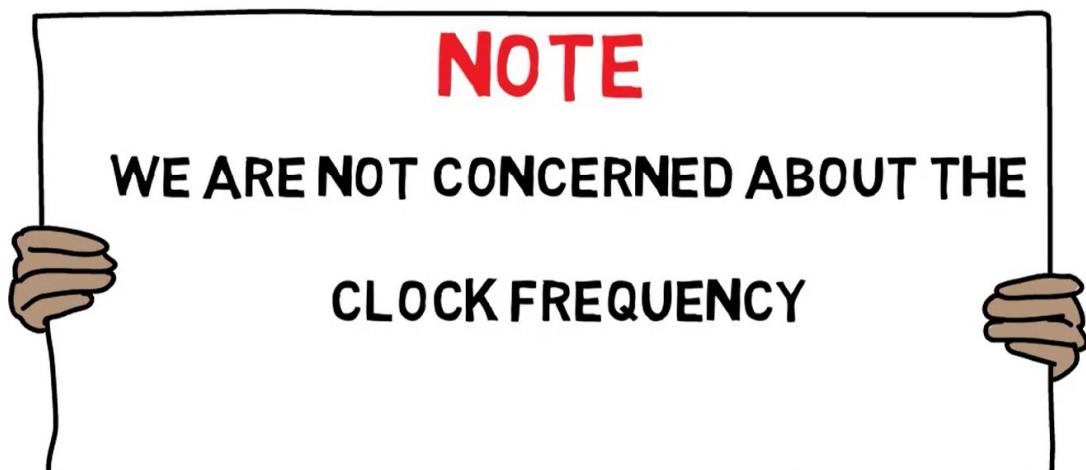
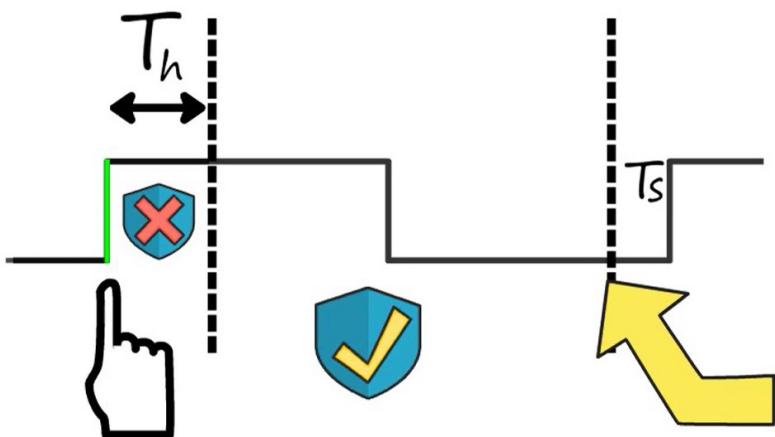


DATA  
REQUIRED  
TIME

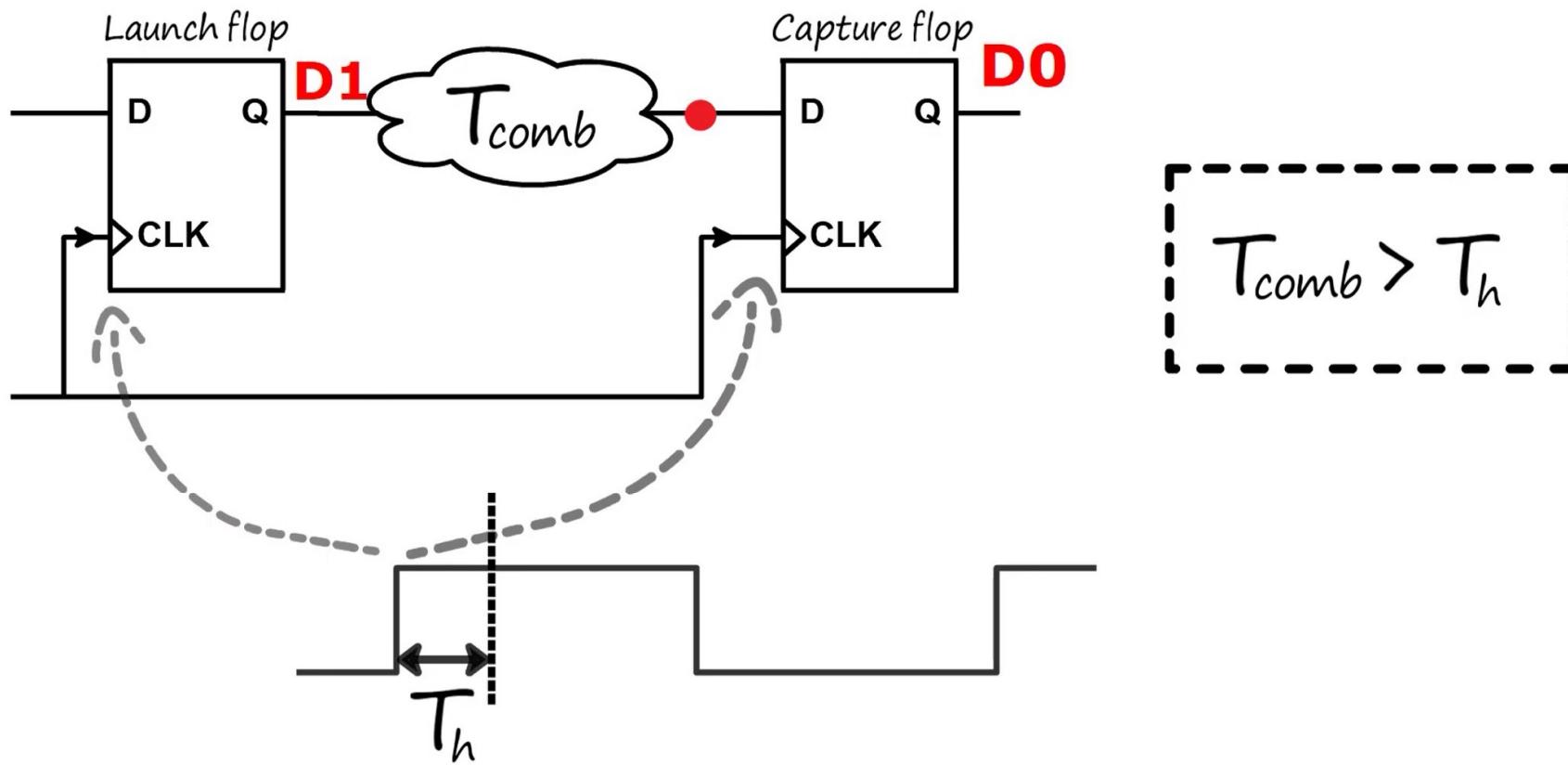


## Hold Analysis

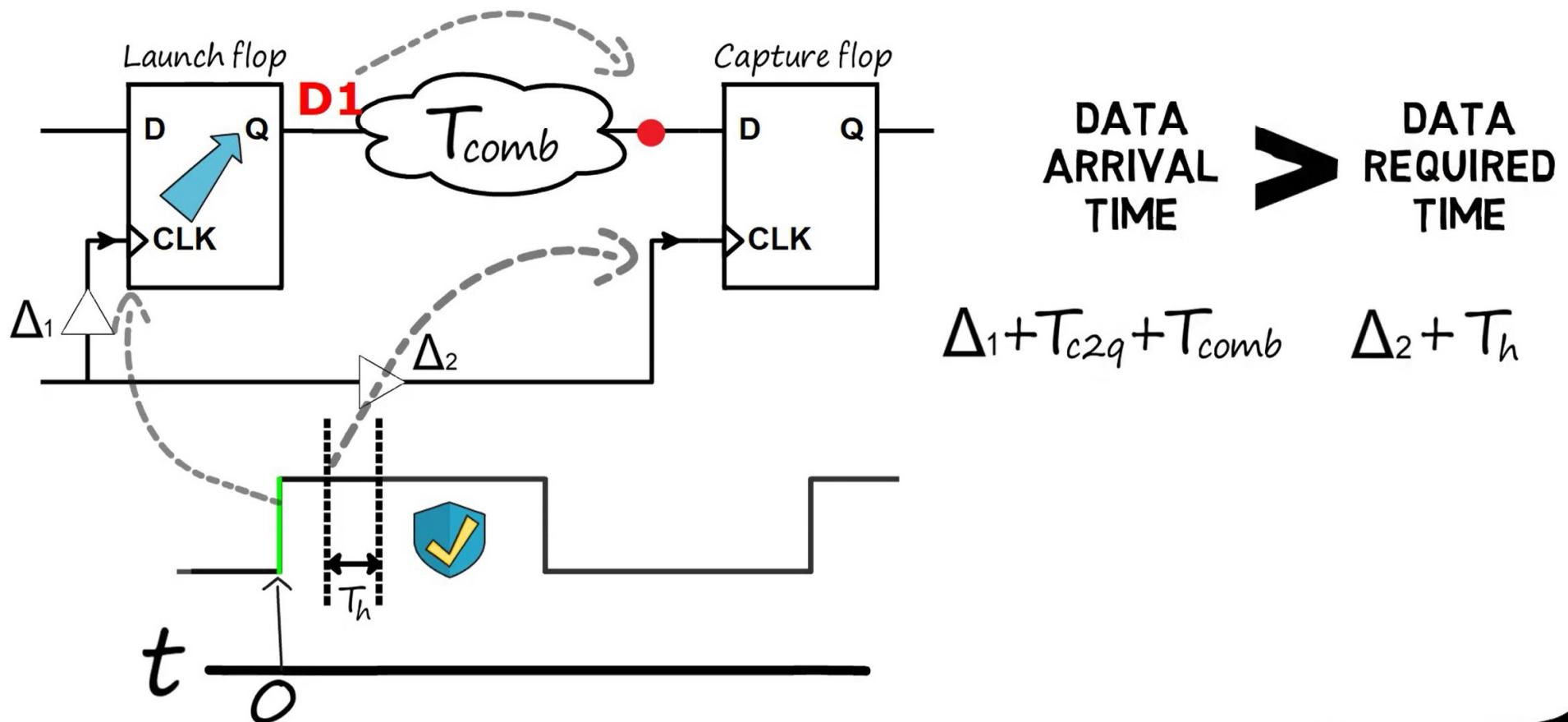
The data that is launched at the current clock edge should not travel to the capture flop before the hold time has passed after the clock edge.



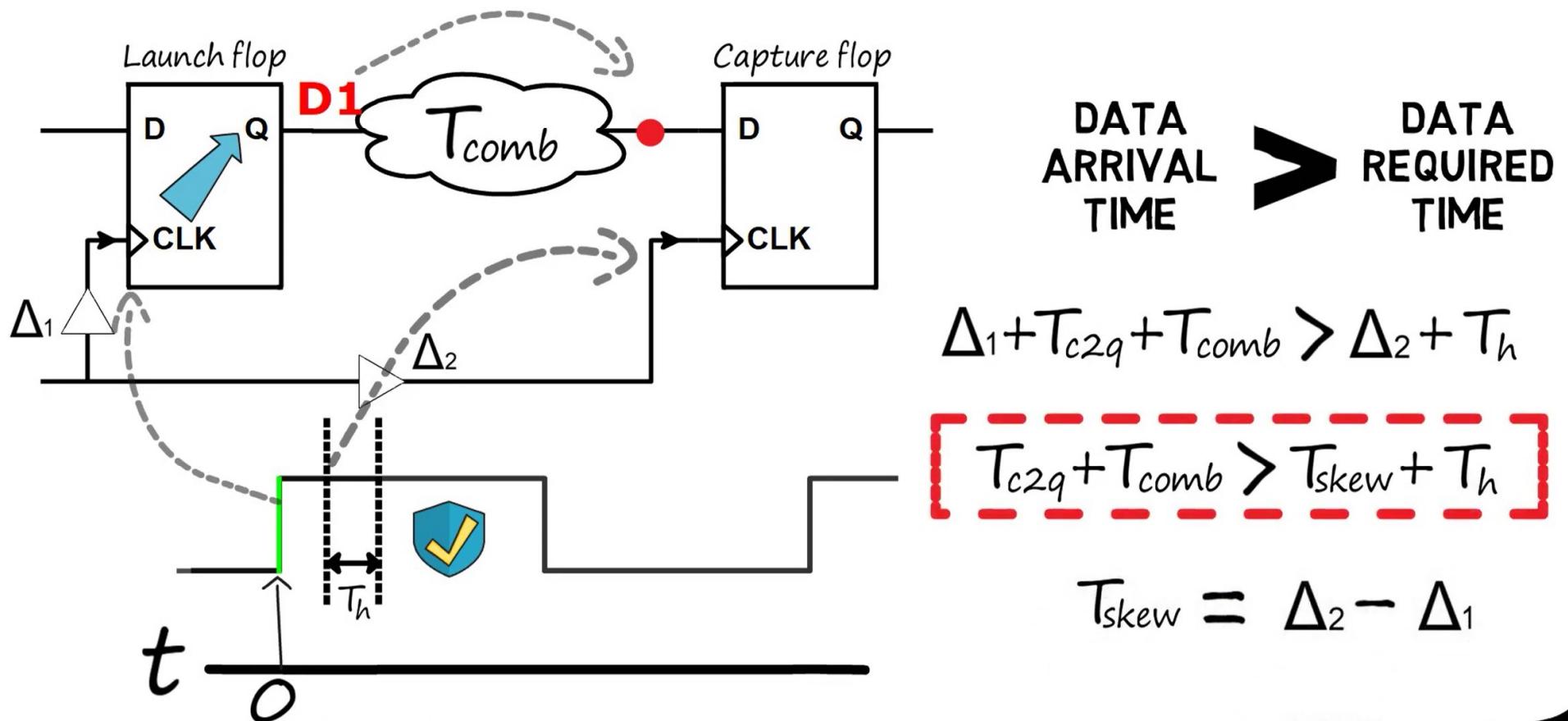
Case-1:  $T_{c2q} = 0$ ,  $\Delta = 0$ ,  $T_h \neq 0$



Case-2:  $T_{c2q} \neq 0$ ,  $\Delta \neq 0$ ,  $T_h \neq 0$



Case-2:  $T_{c2q} \neq 0$ ,  $\Delta \neq 0$ ,  $T_h \neq 0$



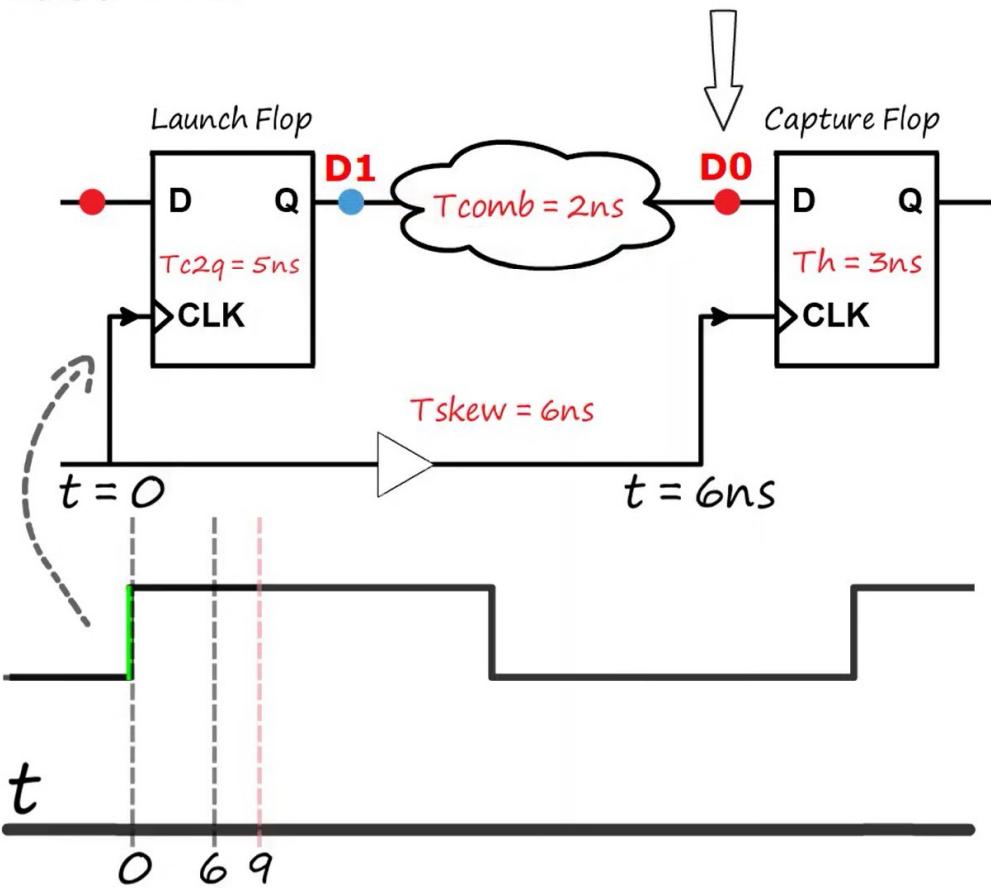
# HOLD SLACK

**DATA ARRIVAL TIME - DATA REQUIRED TIME**

Data should arrive after the required time

*Hold Slack  $\geq 0$*

## EXAMPLE

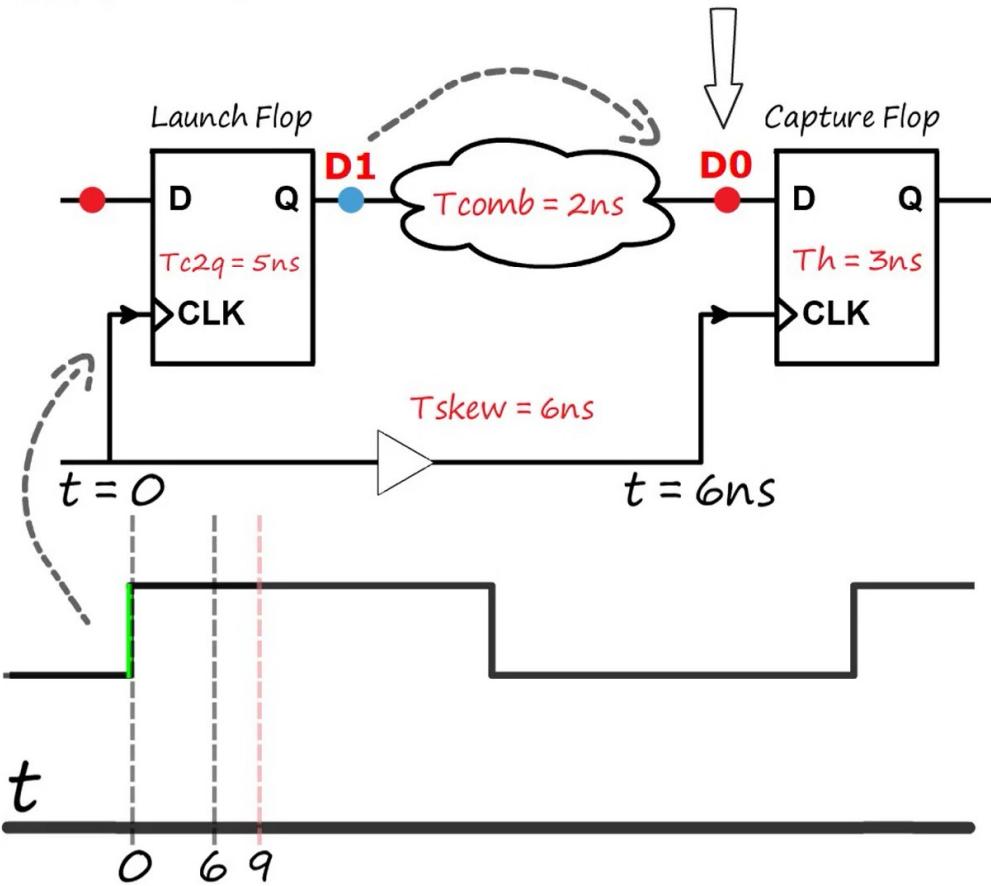


DATA  
ARRIVAL  
TIME

DATA  
REQUIRED  
TIME

$$6 + 3 \\ 9\text{ns}$$

## EXAMPLE



DATA  
ARRIVAL  
TIME

$$5 + 2 \\ 7\text{ns}$$



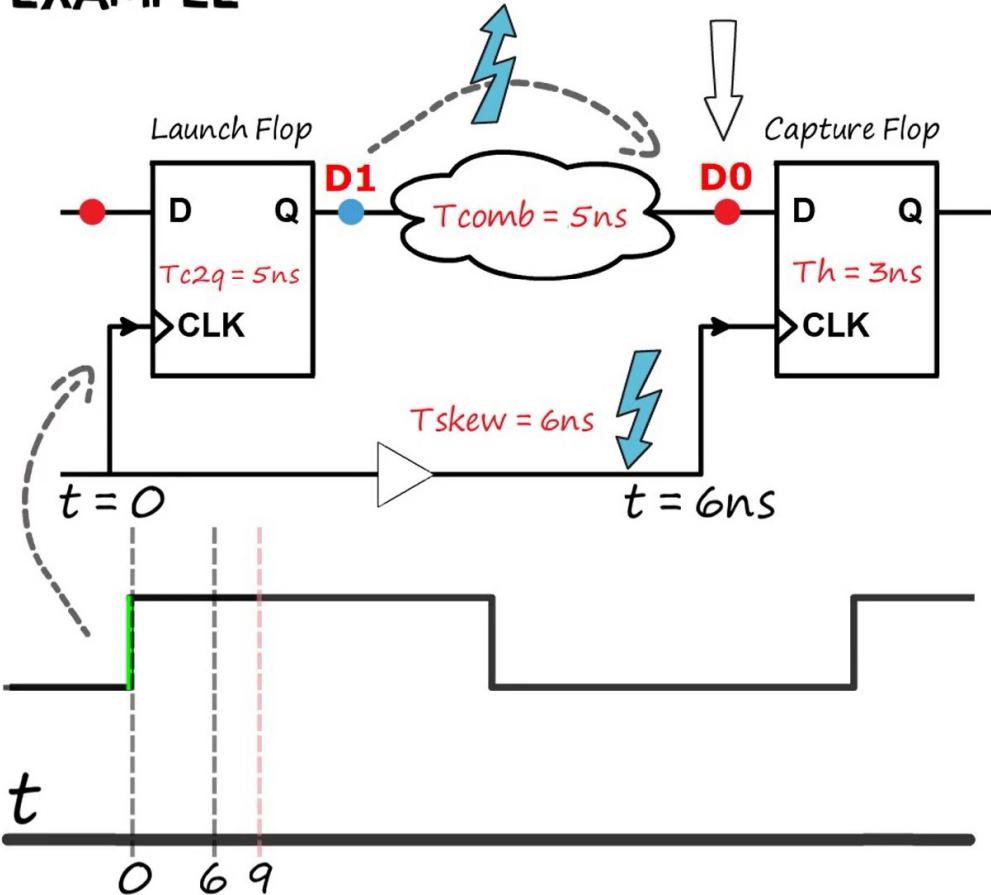
DATA  
REQUIRED  
TIME

$$6 + 3 \\ 9\text{ns}$$



HOLD VIOLATION AT  
THE CAPTURE FLOP

## EXAMPLE



DATA  
ARRIVAL  
TIME

$$5 + 5$$

$$10\text{ns}$$

DATA  
REQUIRED  
TIME

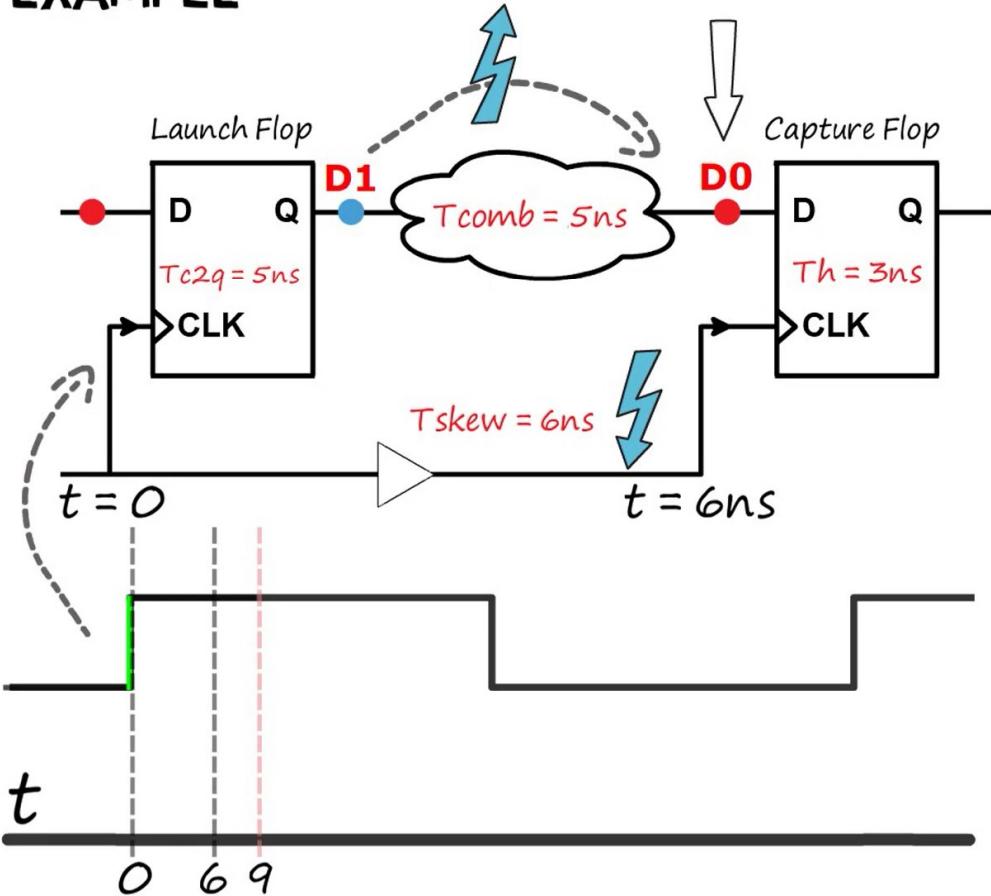
$$6 + 3$$

$$9\text{ns}$$



HOLD VIOLATION AT  
THE CAPTURE FLOP

## EXAMPLE



DATA  
ARRIVAL  
TIME



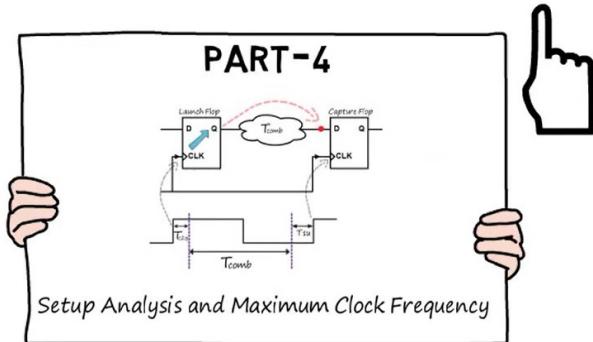
DATA  
REQUIRED  
TIME

$$\begin{array}{ll} 5 + 5 & 6 + 3 \\ 10\text{ns} & > 9\text{ns} \end{array}$$

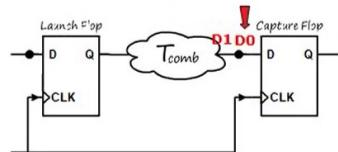
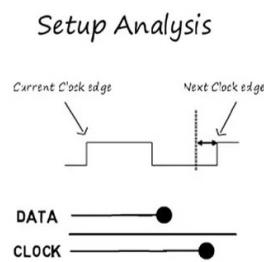


# STATIC TIMING ANALYSIS

## PART-5



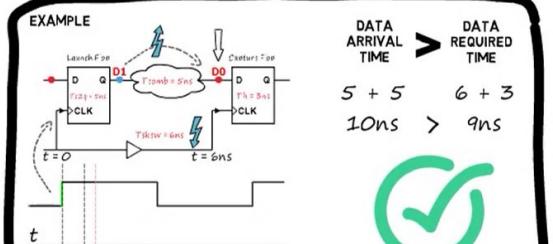
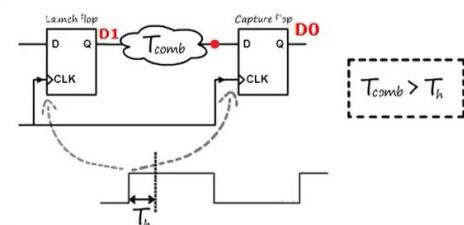
# HOLD ANALYSIS



The data that is launched at the current clock edge should not travel to the capture flop before the hold time has passed after the clock edge.

**NOTE**  
WE ARE NOT CONCERNED ABOUT THE  
CLOCK FREQUENCY

**Case-1:**  $T_{c2q} = 0, \Delta = 0, T_h \neq 0$



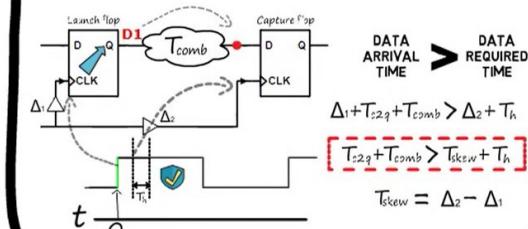
**HOLD SLACK**

DATA ARRIVAL TIME - DATA REQUIRED TIME

Data should arrive after the required time

$\text{Hold Slack} \geq 0$

**Case-2:**  $T_{c2q} \neq 0, \Delta \neq 0, T_h \neq 0$



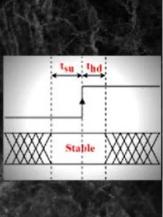
# **STATIC TIMING ANALYSIS**

**PART-6**

# STATIC TIMING ANALYSIS

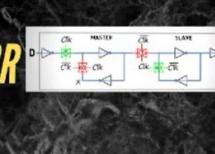
**STA-1**

INTRODUCTION TO  
**SETUP AND HOLD**  
TIMES



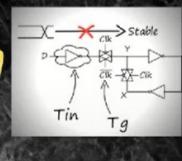
**STA-2**

SETUP AND HOLD  
**REASON FOR**  
EXISTENCE



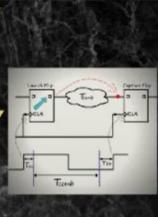
**STA-3**

CONDITION FOR  
**NEGATIVE HOLD**  
TIME



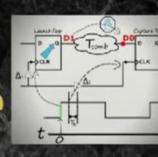
**STA-4**

SETUP ANALYSIS AND  
**MAXIMUM CLOCK**  
FREQUENCY

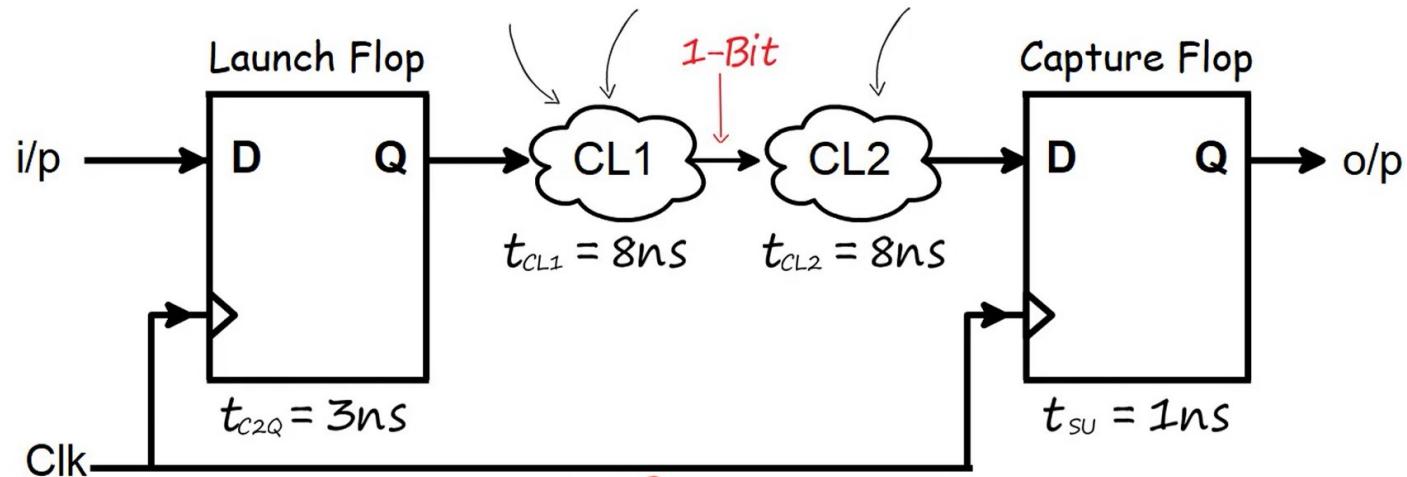


**STA-5**

**HOLD**  
**ANALYSIS**



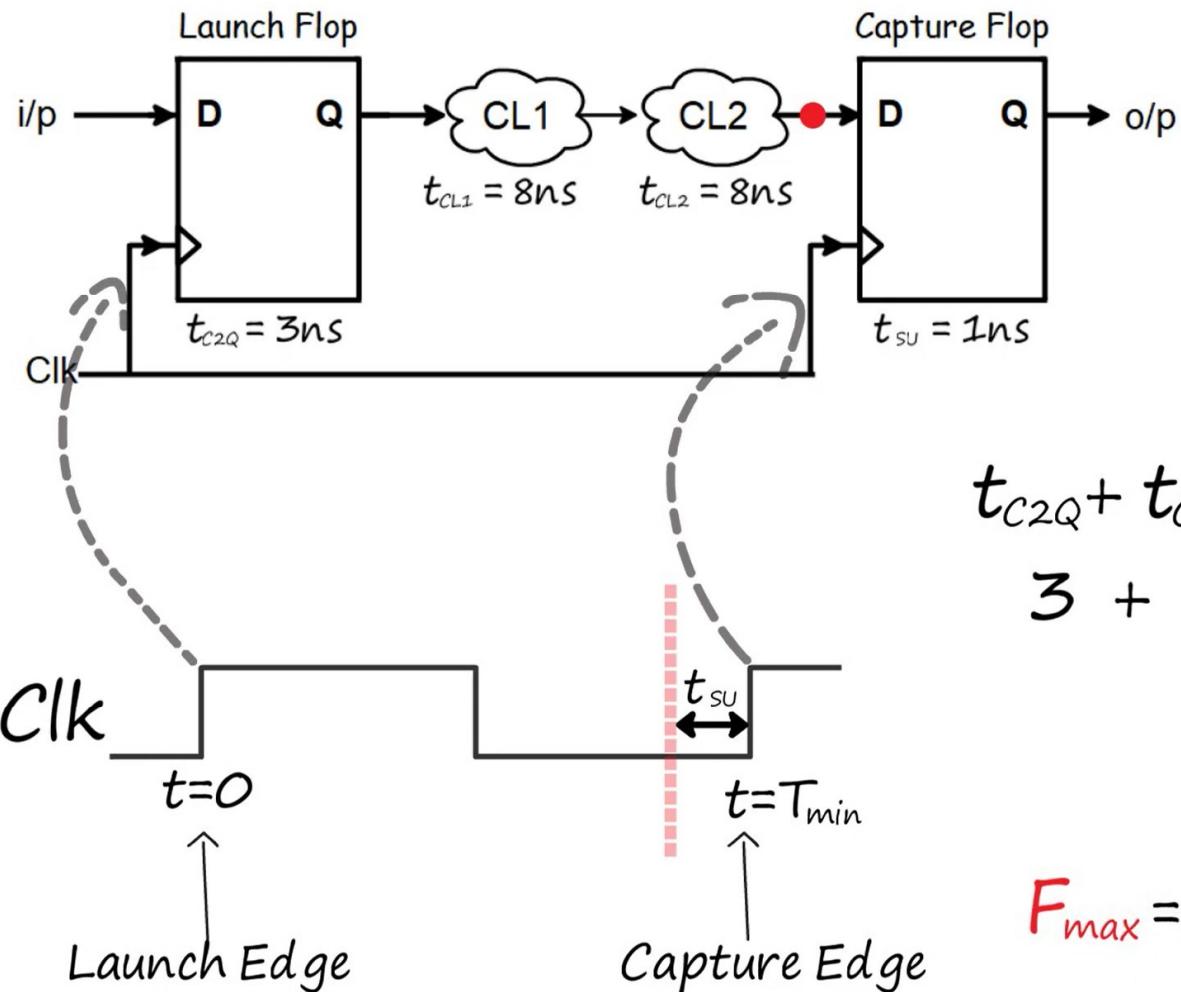
# **STA INTERVIEW PROBLEM**



*Assumptions:* Only timing, not area

Delay of any gates/mux/etc = 1ns

1. Calculate the minimum time period and maximum clock frequency at which the given circuit can operate.
2. Can you operate the given circuit at some frequency higher than the max frequency you've calculated. If yes, then what modifications are required in the design.



$$t_{C2Q} + t_{CL1} + t_{CL2} < T_{min} - t_{SU}$$

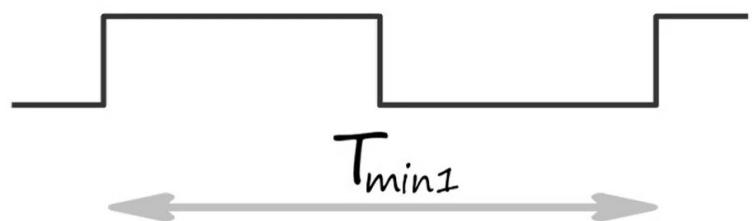
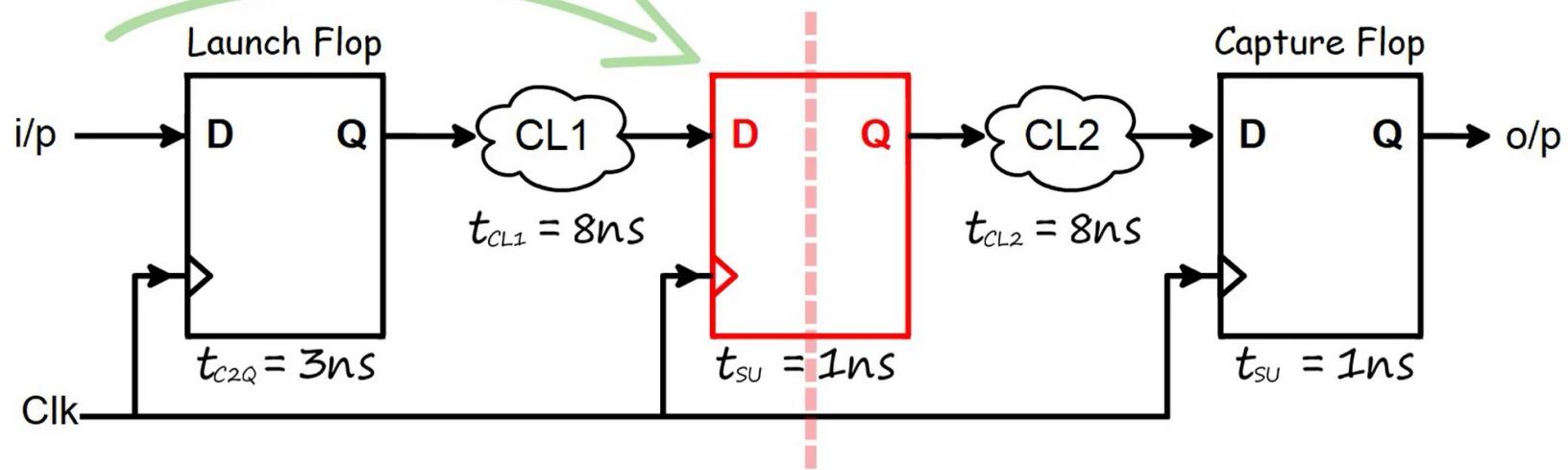
$$3 + 8 + 8$$

$$19\text{ns} < T_{min} - 1\text{ns}$$

$$T_{min} = 20\text{ns}$$

$$F_{max} = 1/20\text{ns} = 50 \text{ MHz}$$

# PIPELINING



$$t_{C2Q} + t_{CL1} < T_{min1} - t_{SU}$$

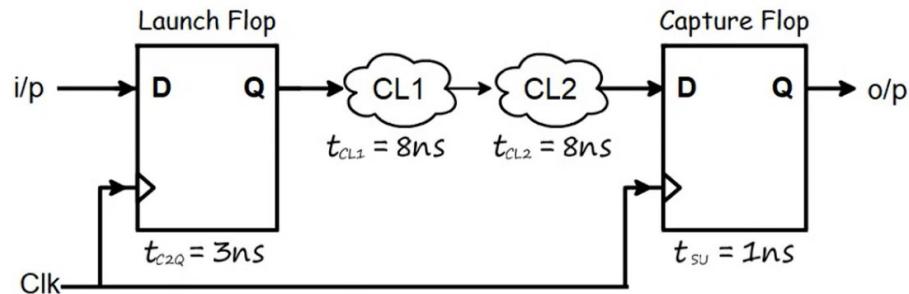
$$3 + 8 < T_{min1} - 1\text{ ns}$$

$$T_{min1} = 12\text{ ns}$$

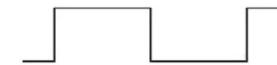
$$F_{max} = 1/12\text{ ns} = 83.33\text{ MHz}$$

## PIPELINING DRAWBACK

# INCREASED LATENCY

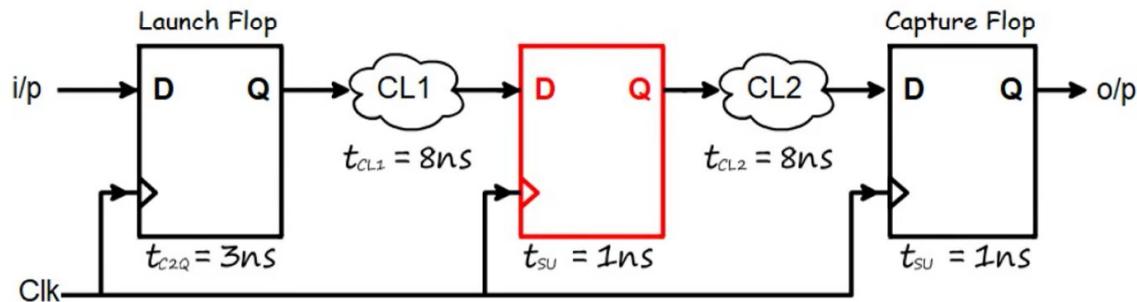


50 MHz



$$T_{\min} + t_{C2Q}$$

$$20 + 3 = \textcircled{23\text{ ns}}$$



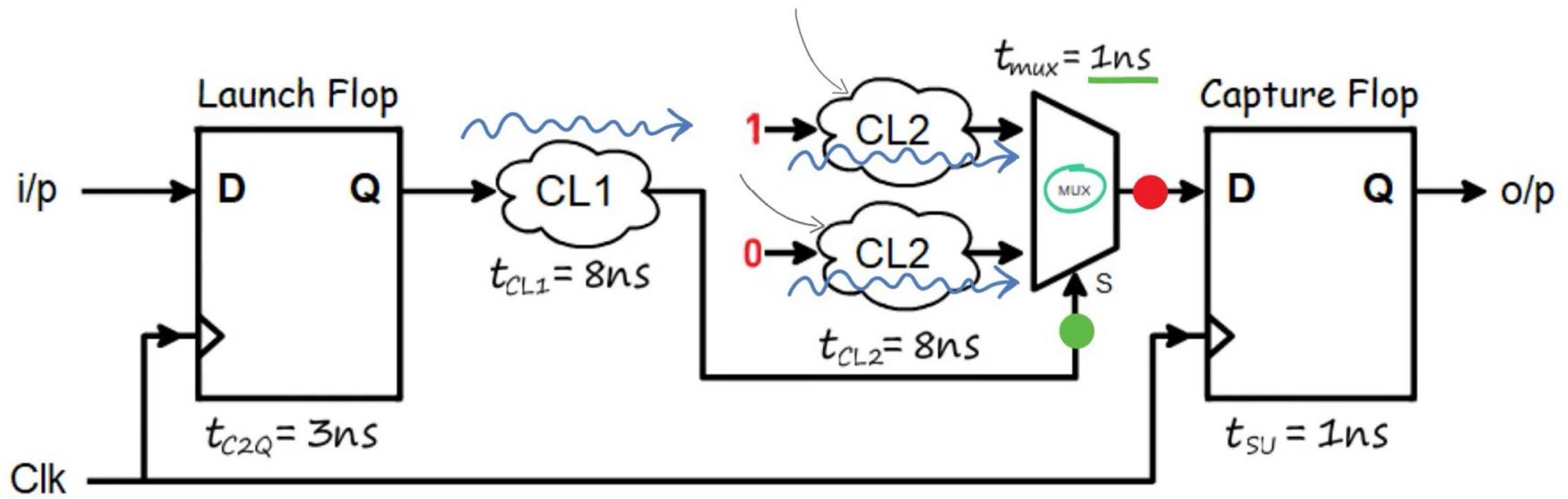
83.33 MHz



$$T_{\min1} + T_{\min1} + t_{C2Q}$$

$$\textcircled{12 + 12 + 3 = 27\text{ ns}}$$

# COMBINATIONAL LOGIC DUPLICATION

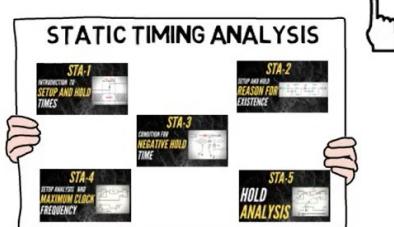
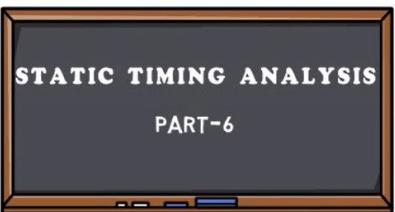


$$\text{Data Arrival Time: } 3 + 8 + 1 = 12 \text{ ns} < T_{min} - T_{su}$$

- No extra latency
- Tradeoff: Increased area

$$T_{min} = 12 + 1 = 13 \text{ ns}$$

$$F_{max} = 1/13\text{ns} = 76.9 \text{ MHz}$$



## STA INTERVIEW PROBLEM

