ECE6025	LOW POWER IC DESIGN	L	T	P	J	C
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Pre-requisite	**ECE5015- Digital IC Design**					**v 1.0**

Course Objective:

The course is aimed to

1. Understand the concepts and techniques of Low power VLSI.
2. Develop a broad insight into the methods used to confront the low power issue from lower level (circuit level) to higher levels (system level) of abstraction.
3. develop a system with multiple supply and threshold voltages used for low power DSP applications.

Expected Course Outcome:

After completion of the course student will be able to:

1. Understand the factors affecting the power in VLSI circuits.
2. Apply algorithmic and architectural level power optimization methods.
3. Apply logic and circuit level power optimization techniques.
4. Apply register transfer level power optimization techniques.
5. Develop an optimum code to reduce the power in the software level.
6. Analyse and explore the usage of sleep transistors for low power.
7. Develop power efficient IPs.

Student Learning Outcomes (SLO):	**1,5,9,17**

Module:1	**Introduction to Low Power Design Methods**	**3 hours**	

Motivation- Context and Objectives-Sources of Power dissipation in Ultra Deep Submicron CMOS Circuits – Static, Dynamic and Short circuit components Effects of scaling on power consumption- Low power design flow- Normalized Figure of Merit – PDP& EDP- Overview of power optimization at various levels.

Module:2	**Algorithmic and Architecture Level Optimization**	**5hours**	

Pipelining and Parallel Processing approaches for low power in DSP filter structures- Multiple supply voltage and Multiple threshold voltage designs for low power- Computer arithmetic techniques for low power- Optimal drivers of high speed low power- software level power optimization.

Module:3	**Logic Level and Circuit Level Optimization**	**5hours**	

Theoretical background – Calculation of Steady state probability- Transition probability - Conditional probability- Transition density- Estimation and optimization of Switching activity- Power cost computation model.

Transistor variable re-ordering for power reduction- Low power library cell design (GDI)- Estimation of glitching power- leakage power optimization-Subthreshold logic design.

Module:4	**Register Transfer Level Optimization**	**4 hours**	

Low power clock-Interconnect and layout designs- Low power memory design and low power

SRAM architectures- Clock gating- Bus Encoding techniques-Deglitching for low power.			
Module:5	**Low Power Design of Sub-Modules**	**5hours**	
Circuit techniques for reducing power consumption in Adders- Multipliers. Synthesis of FSM for low power- Retiming sequential circuits for low power.			
Module:6	**Sleep Transistor Design**	**3hours**	
Design metrics- switch efficiency- area efficiency- IR drop, normal Vs reverse body bias -Layout design of Area efficiency- Single row Vs double row- Inrush current and current latency.			
Module:7	**IP Design for Low Power**	**3hours**	
Architecture and partitioning for power gating- power controller design for the USB OTG- Issues in designing portable power controllers- clocks and resets- Packaging IP for reuse with power intent.			
Module:8	**Contemporary issues:**	**2 hours**	
	Total Lecture hours:	**30hours**	

Text Book(s)

1.	Jan M.Rabaey, MassoudPedram, Low power Design methodologies,SpringerUS, First Edition, 2014.
2.	Kaushik Roy, Sharat Prasad, Low Power CMOS VLSI circuit design, John Wiley and Sons Inc, Second Edition,2010.

Reference Books

1.	Soudris, Dimitrios, ChristrianPignet, Goutis, Costas, Designing CMOS circuits for low power, Springer US, FirstEdition, 2011.
2.	Gary K.Yeap, Practical Low Power Digital VLSI Design, Springer US, First Edition 2010.
3.	AjitPal , Low Power VLSI circuits and Systems, Springer India, First Edition, 2014.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Projects (Indicative)

1. Design of Low Power, High Speed VLSI Adder and Multiplier Subsystems
2. Power Gating Design solutions for Low Power
3. Circuit level power reduction using multi-V_t
4. Non-conventional Low Power Circuits such as Energy Recovery Logic
5. Design of Low Power Clocking Solution for a Sequential System
6. Low power SRAM and CAM design
7. Low Power FFT Design for Wireless Communication Systems
8. Low Power Filter design for SDR systems.

Mode of Evaluation:Review I , II & III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016