ECE5017	DIGITAL DESIGN WITH FPGA	2	0	2	4	4
Pre-requisite	**Nil**					**v 1.0**

Course Objectives :

The course is aimed to

1. understand the various abstraction levels in Verilog HDL and thus model tasks & functions at behavioral level.
2. model the state machines using D and JK Flip Flops and design the complex combinational and sequential logic circuits using various constructs in Verilog.
3. understand the types programmable logic devices and building blocks of FPGA and thus implement the design using Xilinx and ALTERA FPGAs.

Expected Course Outcome :

At the end of the course the student will be able to

1. Understand various abstraction levels in Verilog HDL.
2. design finite state machine using D and JK Flip Flop.
3. model sequential circuit using behavioural modelling.
4. Design the complex combinational and sequential logic circuits using various constructs in Verilog.
5. Understand programmable logic devices and various blocks exist in FPGA.
6. distinguish the architectural and resource difference between ALTERA and Xilinx.
7. use EDA tool to design complex combinational and sequential circuits.
8. develop and prototype digital systems design using FPGA.

Student Learning Outcomes (SLO):	**1,5,17**	
Module:1	**Verilog HDL – Data Flow & Structural Modeling**	**6 hours**

Lexical Conventions - Ports and Modules – Operators - Gate Level Modeling - Data Flow Modeling - System Tasks & Compiler Directives - Test Bench.

Module:2	**State Machine Design**	**4 hours**

Definition of state machines -State machine as a sequential controller- Analysis of state machines using D and JK flip-flops - Design of state machines- State table and State assignment - Transition/excitation table - excitation maps and equations - logic realization- Design examples: Sequence detector, Serial adder, Vending machine.

Module:3	**Verilog HDL – Behavioral Modeling**	**5 hours**

Behavioral level Modeling- Procedural Assignment Statements- Blocking and Non-Blocking Assignments -Tasks & Functions - Useful Modeling Techniques.

Module:4	**Verilog Modeling of Combinational Circuits**	**4 hours**

Behavioral, Data Flow and Structural Realization of Adders and Multipliers

Module:5	**Verilog Modeling of Sequential Circuits**	**4 hours**

Synchronous and Asynchronous FIFO – Single port and Dual port ROM and RAM - FSM Verilog modeling of Sequence detector - Serial adder - Vending machine.

Module:6	**FPGA Architecture**	**3 hours**
Types of Programmable Logic Devices: PLA, PAL, CPLD - FPGA Architecture - Programming Technologies-Chip I/O- Programmable Logic Blocks- Fabric and Architecture of FPGA.		
Module:7	**Xilinx and ALTERA FPGAs**	**2 hours**
Xilinx Virtex 5.0 Architecture - Xilinx Virtex VI Architecture – ALTERA Cyclone II Architecture - ALTERA Stratix IV Architecture.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**30 hours**

Text Book(s)

1.	Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, Create Space Independent Publishing Platform, Second Edition, 2015.
2.	Michael D Ciletti, Advanced Digital Design with the Verilog HDL, Prentice Hall, Second Edition, 2011.

Reference Books

1.	Wayne Wolf, FPGA Based System Design, Prentices Hall Modern Semiconductor Design Series, 2011.
2.	Charles H Roth Jr, Lizy Kurian John and ByeongKil Lee Digital Systems Design using Verilog, Cengage Learning, First Edition, 2016.

Mode of Evaluation: Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Challenging Experiments (Indicative)

1.	Many ink-jet printers have six cartridges for different colored ink: black, cyan, magenta, yellow, light cyan and light magenta. A multibit signal in such a printer indicates selection of one of the colors. Write a data flow Verilog model for a decoder for use in the inkjet printer described above. The decoder has three input bits representing the choice of color cartridge and six output bits, one to select each cartridge. Verify the output of the design using test bench by simulating in Modelsim Simulator. Implement the design in ALTERA DE2-115 Board and verify it's functionality.	**4 hours**
2.	Write a behavioral Verilog code to divide the ALTERA DE2-115 Board clock frequency 50MHz by 40MHZ, 30MHz, 20 MHz, 10MHz. Display each of the output using LEDs available in the board.	**4 hours**
3.	Design and implement a circuit on the DE2-115 board that acts as a time-of-day clock. It should display the hour (from 0 to 23) on the 7-segment displays HEX7−6, the minute (from 0 to 60) on HEX5−4 and the second (from 0 to 60) on HEX3−2. Use the switches SW15−0 to preset the hour and minute parts of the time displayed by the clock.	**4 hours**
4.	We wish to implement a finite state machine (FSM) that recognizes two specific sequences of applied input symbols, namely four consecutive 1s or four consecutive 0s. There is an input w and an output z. Whenever w = 1 or	**8 hours**

	w = 0 for four consecutive clock pulses the value of z has to be 1; otherwise, z = 0. Overlapping sequences are allowed, so that if w = 1 for five consecutive clock pulses the output z will be equal to 1 after the fourth and fifth pulses. Design and Implement the design using DE2-115 Board.	
5.	Write a behavioral Verilog code to design FIFO with the following specification d_in: input data; 8 bit width is considered d_out: output data; 8 bit width is considered · w_en: write enable signal r_en: read enable signal r_next_en: read next enable w_next_en: write next enable w_clk: write clock; 10 MHz for this design r_clk: read clock; 50 MHz for this design w_ptr: write address pointer; 4 bit to address depth of 16 · r_ptr: read address pointer; 4 bit to address depth of 16 · ptr_diff: address pointer difference; 4 bit width f_full_flag: FIFO full flag; asserted when FIFO is full · f_empty_flag: FIFO empty flag; asserted when FIFO is empty Use Dual Port RAM available in ALTERA IP library to realize the FIFO. Implement the design using ALTERA DE2-115 board.	**10 hours**
	Total Laboratory hours:	**30 hours**

Mode of Evaluation: Continuous assessment of challenging experiments / Final Assessment Test (FAT).

List of Projects (Indicative)

1. Design MIPS 32-Bit RISC Processor and implement it using ALTERA Cyclone IV FPGA and study about it's performance.
2. Design a Reconfigurable FIR Filter and verify it's functionality through test bench. Implement the design using ALTERA Cyclone IV FPGA.
3. Design and Implementation of Smart Traffic Light System for congested four way road using ALTERA Cyclone IV FPGA.
4. Design and Implementation of CORDIC Algorithm using ALTERA Cyclone IV FPGA.

Mode of Evaluation: Review I , II & III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016