S.No:	Subject
1	**Digital Electronics**
2	**RTL Design - Verilog (Basics)**
3	**RTL Design Verification** - System Verilog (Basics)
4	**RTL Design Verification: UVM - Universal Verification Methodology (Advance Verification)**
5	**Assignments**

VLSI Training Syllabus

Syllabus
* CMOS VLSI Design Concepts. * FPGA's. * Refreshing all Digital Concepts.
Introduction, DATA TYPES - Value Set, Net, Variable Or Reg, Vectors, Memories, Net Types.OPERATORS - Binary Arithmetic Operators, Unary Arithmetic Operators, Relational Operators, Logical Operators, Bitwise Operators, Unary Reduction Operators,Other Operators, Operator Precedence, ASSIGNMENTS - Blocking Procedural Assignments, The Nonblocking Procedural Assignment, Procedural Continuous Assignments, Assign And Deassign Procedural Statements, Force And Release Procedural Statements, Delays, Inter Assignmnet Delay, Intra-Assignment Delay Control,CONTROL CONSTRUCTS - If And If Else Statements, Case, Forever, Repeat, While, For loop, PROCEDURAL TIMING CONTROLS - Delay Control, Event Control, Named Events.STRUCTURE - Module, Ports, Signals, BLOCK STATEMENTS - Sequential Blocks, Parallel Blocks, STRUCTURED PROCEDURES - Initial, Always, Functions, Task.Introduction to Testbench, Linear Testbench, File IO TB, Self checking Testbench, Verification flow,Process control, Compilation and simulation switches, Debugging, Code coverage, File handling, Finding Test senarious .
PAcked and Unpacked array, Dynamic array, Associative array, Queues, Class and their methods, Procedural Statments and flow control - Blocking and Non Blocking statements, while do while, foreach loop, disable and disable statement, Event control, Process Statement - Fork join_any, fork join_none, wait fork, disable fork, Task and Function - Task, Function, Argument passing, Import and export function. Radomization and Constraints - Randomization disable, methods, Constraint block, Inside operators, Weighted distribution, Implication and if-else, Iterative constraint block, Constraint mode disable, static constraint, In line constraint, function in constraints, soft constraint, unique constraint, Bidirectional constraint, Classes and Methods - This keyword, Constructors, Static class and methods, Class assignments, Shallow copy, Deep copy, Parametrized class, Inheritance, Overriding class members, Super keyword, Casting, Data hiding and encapsulation, Abstract class, SCR operator, Extern methods, Typedef classes.Semaphore - Mailbox, Event , Scheduling semantics, Program block, Interface,Virtual interface, Modport, Clocking block. Assertion - SVA building blocks, SVA sequence, Implication operator, Repetition operator, Ended and disable iff. Coverage - Functional Coverage, Cross coverage, Coverage options.
Copy, Print, Clone, Compare, Pack, Unpack, UVM Sequence - Methods, Macros, Sequence control, UVM Sequencer. UVM Config db - config db, Set Methods, Get Methods, UVM Pahses, UVM Driver, UVM Monitor, UVM Agent. UVM Scoreboard, UVM Environment, UVM Test, UVM Testbench Top, UVM Callback - callback, Callback add methods, UVM Callback in UVM Sequence, UVM Event, UVM TLM, UVM RAL, UVM Barrier and Heartbeat.
2. Design a HDL code for serial in parallel out module with different clock rate and verify the design. 3. Design a APB protocol and verify it. 4. Write a verilog code for Memory module and interface it with APB. verify the memory module through APB. 5. Design a FSM to detect a sequence of bits. 6. Design a verilog code for coin Winding Machine. 6. Verifying the above RTL Design with Verification language.

S.No.	Name of the tool
1	edaplayground (open access tool)