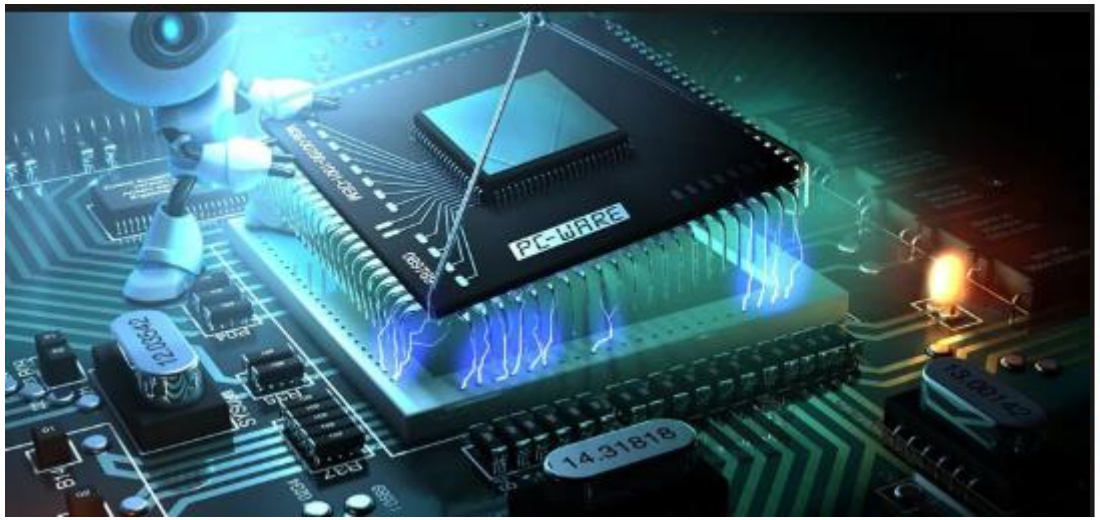


IC Planning and Implementation (Physical Design)

Floorplanning

Presentation topics

- Floorplanning
- Blockages
- Congestion/Reduction techniques
- Tips for better macro placement

Floorplanning

- The netlist is the logical description of the ASIC and the floorplan is the physical description of the ASIC
- Mapping the logical description of the design to the physical description
- The main objectives of floorplanning are to minimize
  – Area
  – Timing (delay)
- During floorplanning, the following are done:
  – The size of the chip is estimated.
  – The various blocks in the design, are arranged on the chip.
  – Pin Assignment is done.
  – The I/O and Power Planning are done.
  – The type of clock distribution is decided

Floorplanning

Floorplanning is a major step in the Physical Implementation process. The final timing, quality of the chip depends on the floorplan design. The three basic elements of chip are:

– **Standard Cells:** The design is made up of standard cells.
– **I/O cells**: These cells are used to help signals interact to and from the chip.
– **Macros** (Memories): Examples of memory cells include 6T SRAM (Static Dynamic Access Memory), DRAM (Dynamic Random Access Memory) etc

Floorplanning

Aspect ratio (AR):

- It is defines as the ratio of the width and length of the chip
- If there are more horizontal layers, then the rectangle should be long and width should be small and vice versa if there are more vertical layers in the design
  - Normally, METAL1 is used up by the standard cells. Usually, odd numbered layers are horizontal layers and even numbered layers are vertical. So for a 5 layer design, AR = 2/2 = 1.
  - Example2: For a 6 layer design, AR = 2/3 = 0.66

Concept of Rows:

- The standard cells in the design are placed in rows. All the rows have equal height and spacing between them. The width of the rows can vary.
- The standard cells in the rows get the power and ground connection from VDD and VSS rails which are placed on either side of the cell rows.
- Sometimes, the technology allows the rows to be flipped or abutted, so that they can share the power and ground rails

Floorplanning

Core:

- Core is defined as the inner block, which contains the standard cells and macros. There is another outer block which covers the inner block.
- The I/O pins are placed on the outer block

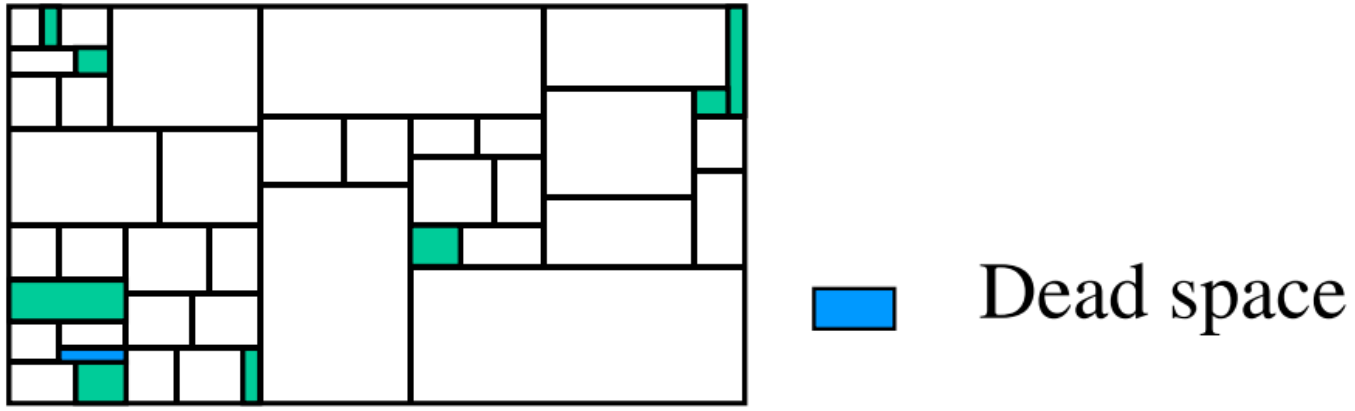
Power Planning:

- Signals flow into and out off the chip
- A power ring is designed around the core. The power ring contains both the VDD and VSS rings. Once the ring is placed, a power mesh is designed such that the power reaches all the cells easily.
- The power mesh is nothing but horizontal and vertical lines on the chip. One needs to assign the metal layers through which you want the power to be routed.
- During power planning, the VDD and VSS rails also have to be defined.

Floorplanning

The floorplanning is to plan the positions and shapes of the modules at the beginning of the design cycle to optimize the circuit performance:

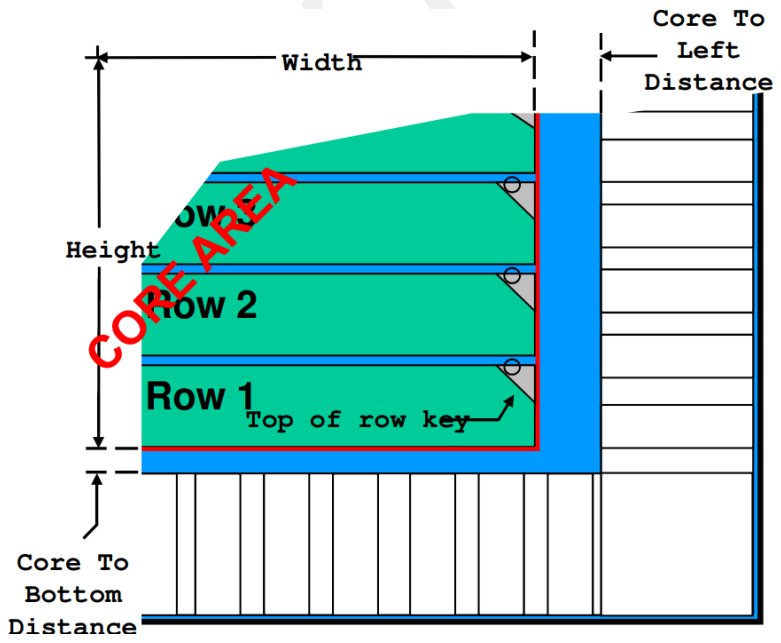
– Chip area
– Total wire length
– Delay of critical path
– Routability
– Others, e.g**., noise, heat** dissipation, etc.



Core area

Control Parameters

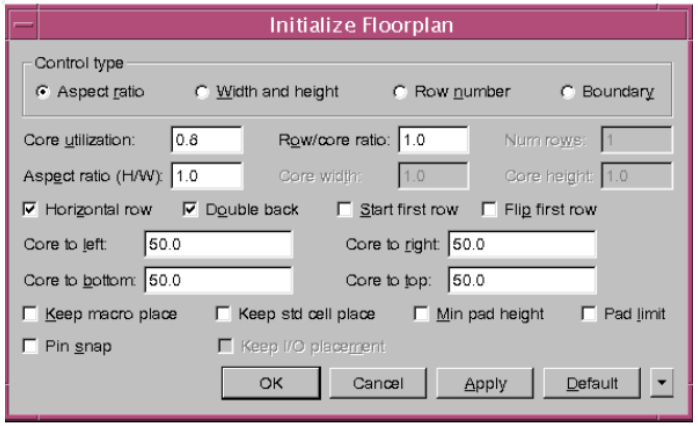
- Aspect Ratio
  - ✓ Utilization
  - ✓ Aspect ratio (H/W)
  - ✓ row/core ratio
- Width & Height
  - ✓ Width
  - ✓ Height
  - ✓ Row/Core ratio



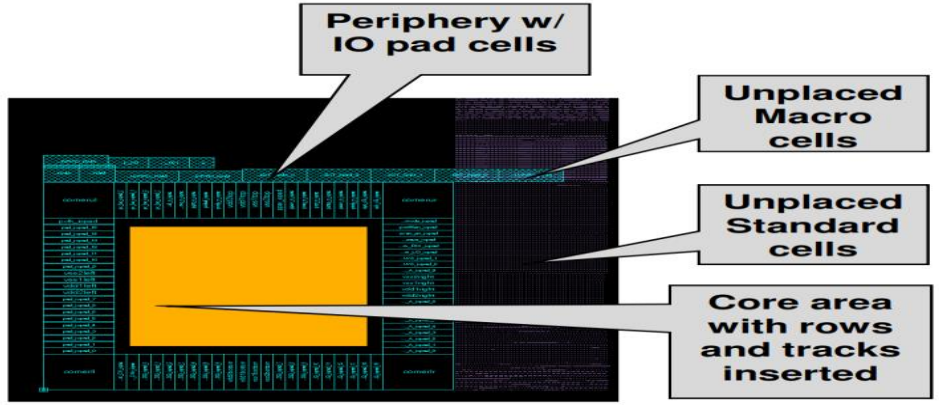
Initialize floorplan

Generates the basic elements of the FP
– Place IO pads/pins, as defined in the TDF file.
– Create chip/core boundary
– Create rows and tracks honoring user defined values
• aspect ratio/width & height/row number boundary
• core utilization
• …

Initialize the Floorplan
“initialize_floorplan” is the command



Floorplan after initialization



Blockages

- Blockages are specified location where placing of the cells are prevented or blocked. This acts a guidelines for placing std cells in the design

- Blockges will guide the placement engine to place the standard cells or/not

Types of blockages

1. Placement blockage

- Soft (Non buffer) Blockage :- Soft blockages specifies the region where only buffer can be placed (Other logic cells can not be placed)
- Hard blockage:- Avoid placing any kind of cells in the specific region
  - Hard blockages mainly added to block placing standard cells in specific region to avoid congestion near macros
  - Congestion near critical modules
- Partial placement blockage :-Reduce the placement density without blocking 100% of the area. You can control how much % would need to be blocked.

2. Routing blockage :- Routing blockage is added to block routing resource on one or more layer at specific region at certain point of the design

Halos/keep out margins

1. HALO is the region around the boundary of fixed macro in the design in which no other macro or std cells can be placed. Halo allows placement of buffers and inverters in its area.
2. Halos of two adjacent macros can be overlap.
3. If the macros are moved from one place to another place, Halos will also be moved. But in the case of blockages if the macros are moved from one place to another place the blockages cannot be moved.

Congestion

Congestion :- If the number of available routing tracks is less than the number of required routing tracks

We need to do congestion analysis at each and every stage of physical design (For better routability)

Congestion are of two types

1. Global congestion
2. Local congestion

Possible reason for congestion

1. High standard cell count near macro edges
2. Lot of standard cells placed in small area
3. High pin count in local region (It may be due to OAI/AOI cells etc)
4. Bad macro placement
5. Bad Aspect ratio
6. Criss cross communication of logic

Congestion reduction techniques

- Before finding out the reduction techniques, need to root cause the reason behind congestion
- Below are the few of the possible ways to fix the congestion problems

  - ✓ After seeing the congestion maps check the congested area having high standard cell density. If you see such case than apply the partial blockages with less than the density in that particular area.

  Eg: if the congestion regions is let say 80% utilization then apply partial blockage with 60%

  - ✓ If you see the congestion near to the macro area then apply 5-10 microns of soft or hard blockage (better is 5 microns hard and 5 is soft is better). Because high critical timing path cell will be seated in the soft blockage area in the optimization phase.

  - ✓ If you see the congestion M2 M3 layers apply cell padding to the high number of pin standard cells (Eg. AOI, OAI,Full adders or other 4 i/p gates)

  - ✓ Congestion is at rectileanior areas apply the partial blockages

  - ✓ Using proper partial placement blockages (Desnity screens)

Floorplaning

I/O Placement: There are two types of I/O's.

- **Chip I/O:** The chip contains I/O pins. The chip consists of the core, which contains all the standard cells, blocks. The chip I/O placement consists of the placement of I/O pins and also the I/O pads.
- **Block I/O:** The core contains several blocks. Each block contains the Block I/O pins which communicate with other blocks, cells in the chip. This placement of pins can be optimized.

Concept of Utilization:

- Utilization is defined as the percentage of the area that has been utilized in the chip.
- In the initial stages of the floorplan design, if the size of the chip is unknown, then the starting point of the floorplan design is utilization. There are three different kinds of utilizations
  – Chip Level utilization
  – Floorplan Utilization
  – Cell Row Utilization

Floorplanning

Chip Level utilization:

It is the ratio of the area of standard cells, macros and the pad cells with respect to area of chip.

[Area(Standard cells) +Area (Macros)+Area(Pad cells)] / Area(Chip)

Floorplan Utilization:

It is defined as the ratio of the area of standard cells, macros, and the pad cells to the area of the chip minus the area of the sub floorplan.

[Area (Standard Cells) + Area (Macros) + Area (Pad Cells)] / [Area(Chip) – Area (Sub floorplan)]

Cell Row Utilization:

It is defined as the ratio of the area of the standard cells to the area of the chip minus the area of the macros and area of blockages
[Area (Standard Cells)] / [Area(chip) - Area (Macros) - Area (Region blockages)]

Top level level Floorplan tasks

1. Placement of Pad cells
2. Placement of macros/Blocks
3. Bump placement
4. Block level shaping (If needed)
5. RDL routing
6. Creation of appropriate blockages b/w the macros (This can be understood through multiple PnR iteration)
7. Addition of physical only cells to make sure to obey the “ Base DRC” manufacturing rules

Block level Floorplan tasks

1. Decision on block level shape (Aspect ratio)
2. Decision on block level utilization
3. Placement of macros
4. Placement of block level pins
5. Creation of appropriate blockages b/w the macros (This can be understood through multiple PnR iteration)
6. Addition of physical only cells to make sure to obey the “ Base DRC” manufacturing rules

Floorplanning

Macro Placement:

- As a part of floor planning, initial placement of the macros in the core is performed. Depending on how the macros are placed, the tool places the standard cells in the core.
- If two macros are close together, it is advisable to put placement blockages in that area. This is done to prevent the tool from putting the standard cells in the small spaces between the macros, to avoid congestion.
- Few of the different kinds of placement blockages are:
  – **Standard Cell Blockage:** The tool does not put any standard cells in the area specified by the standard cell blockage.
  – **Non Buffer Blockage:** The tool can place only buffers in the area specified by the Non Buffer Blockage.
  – **Blockages below power lines:** It is advisable to create blockages under power lines, so that they do not cause congestion problems later. After routing, if you see an area in the design with a lot of DRC violations, place small chunks of placement blockages to ease congestion.

Floorplanning guidelines

- Flylines helps us to understand the communication b/w macro & IO , b/w Macro & Macro, b/w macro and standard cells.
- Place macro's near to core boundary (Otherwise it acts a blockage for standard cells placement & routing)
- More number of connection from macro to macro place them near to each other
- If i/p pin/port is connected to macro, place near to pin or pad which is better
- More connections of macro to standard cells, spread macro inside core area (Careful placement of macros has to be done in this scenario otherwise impact on congestion/timing is very high)
- Avoid criss cross placement of macros in order to save routing resources as well as from routing ,Placement and congestion issues

Tips for macro Placement /Floorplanning

1. **Design data flow and module interaction is needed to create macro location**

2. Place macros around chip periphery:-Avoid creating obstacle in core area by placing them in periphery region (if there is no much communication between macro & standard cells). Another advantage to placing the hard macros around the core periphery is it's easier to supply power to them, and reduces the change of IR drop problems to macros consuming high amounts of power.

3. Consider connections to fixed cells when placing macros :- When you decide macro position, you have to pay attention to connections to fixed elements such as I/O and perplaced macros. Place macros near their associate fixed element. Check connections by displaying flight lines in the GUI.

4. Orient macros to minimize distance between pins (Pins should be towards the core logic) When you decide the orientation of macros, you also have to take account of pins positions and their connections

Tips for macro Placement /Floorplanning

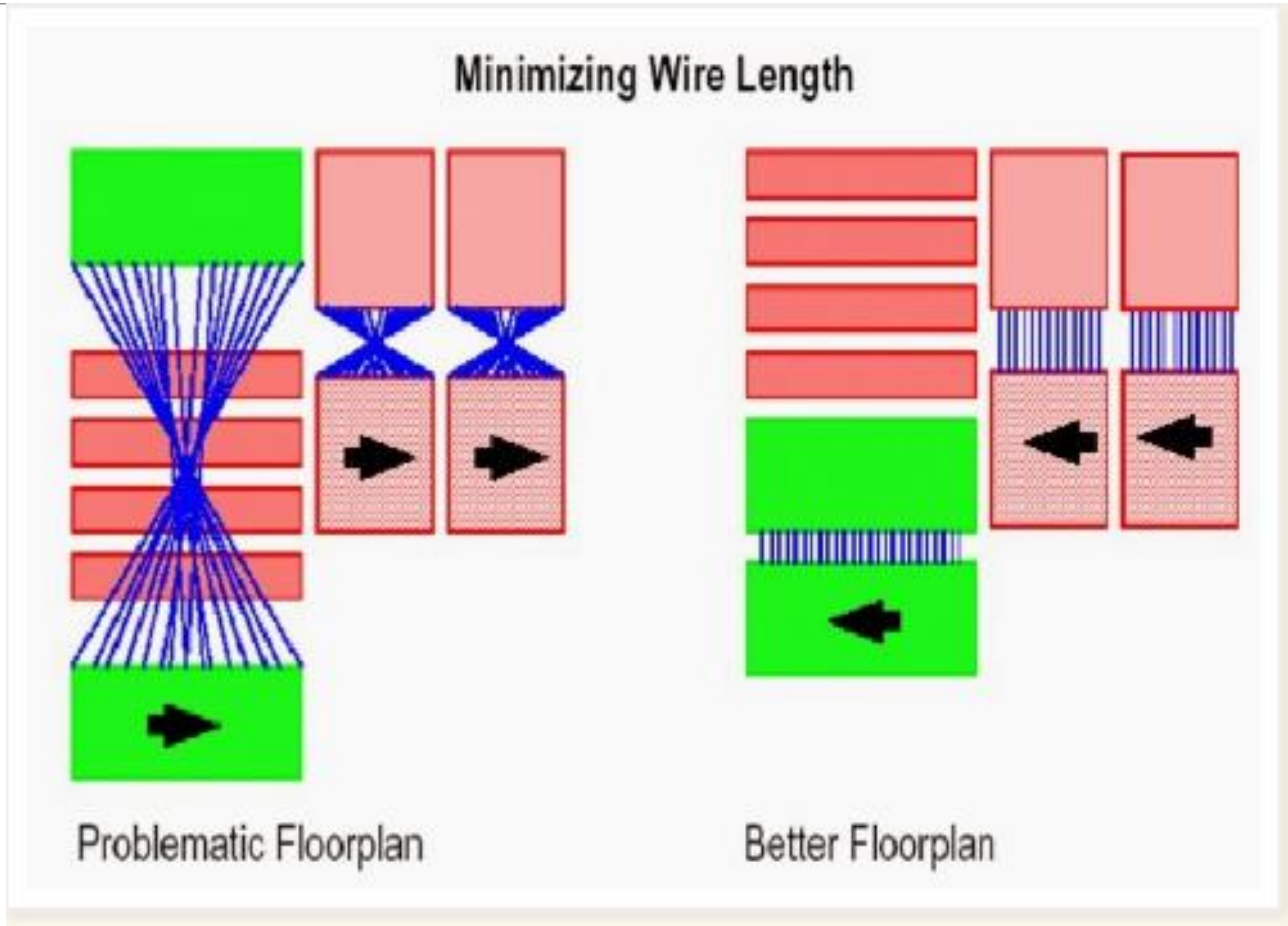
5. Reserve enough room around macros.
For regular net routing and power grid, you have to reserve enough routing space around macros. In this case estimating routing resources with precision is very important. Use the congestion map from trialRoute/Virtual route to identify hot spots between macros and adjust their placement as needed.

6. Reduce open fields as much as possible.
Except for reserved routing resources, remove dead space to increase the area for random logic. Choosing different aspect ratio (if that option is available) can eliminate open fields.

7. Reserve space for power grid.
The number of power routes required can change based on power consumption. You have to estimate the power consumption and reserve enough room for the power grid. If you underestimate the space required for power routing, you can encounter routing problems.

8. **Avoid long and thin long channels**

Fly line comparison b/w problematic and better floorplan



Spacing b/w the macros

- We should estimate the channel spacing b/w the macros
- Below is the general rule of thumb to estimate the channel length

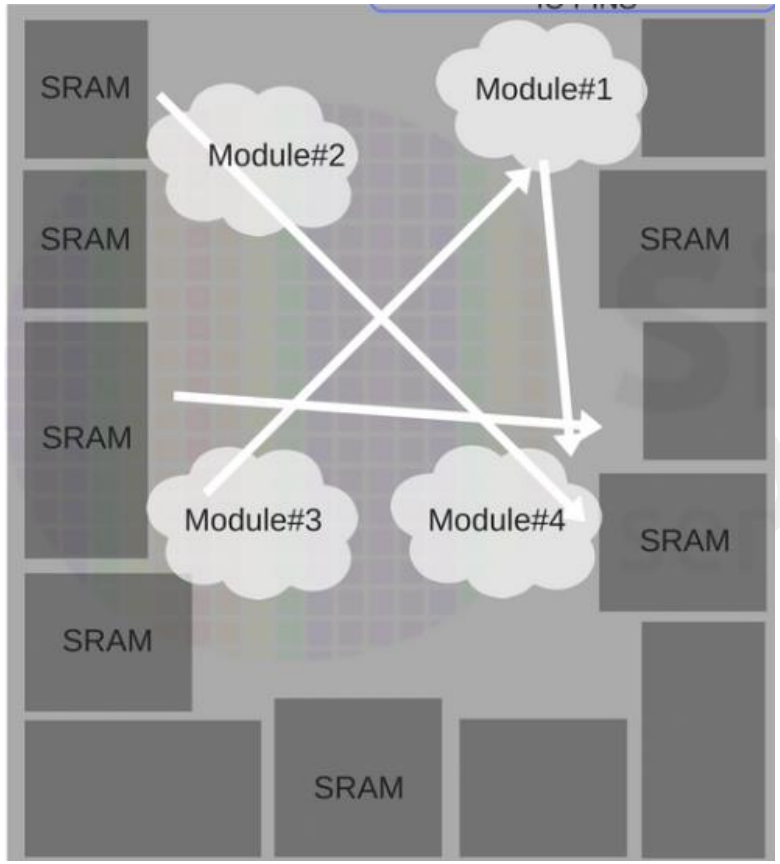
Channel spacing= (number of pins of macros * pitch) / (number of available routing layers * 2)

Divided 2 is because of Horizontal/vertical routing resources

- Example:- We have 2 macros having the pins of 100 each macro and pitch=0.25 and available metals are 6

Spacing b/w the macros = ((100+100)*0.25/(6/2) =16.6 micron spacing is needed b/w the macros

Bad floorplan impacts

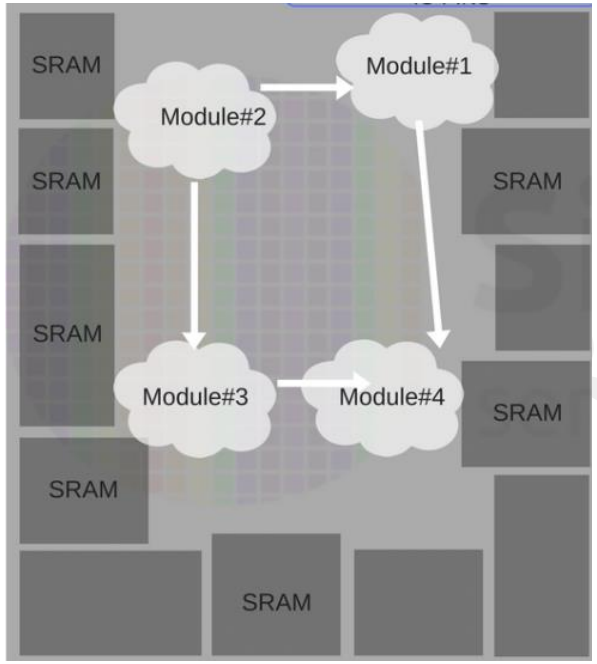


Below are the few of the problems due to bad problem

1. Bad floorplan can create congestion (Leads to physical DRC's)
2. Big timing violations (Due to detouring/Unnecessary buffering)
3. EM violations
4. IR violations
5. Noise violations
6. Completed routing can cause complicated DRC pop up

Good floorplan decisions

- Arriving at good floorplan takes multiple iteration
- It's worth to spend time to come with good floorplan , it will avoid many of the design problems



Good floorplan

1. Minimal crisscrosses
2. Minimal congestion/ Good congestion hotspot
3. Better timing QOR
4. Minimal IR/EM impact

DRC’s

1. Logical DRC’s
2. Physical DRC’s
   - Base DRC’s
   - Metal DRC’s

Checklist after floorplace stage

1. Proper Die to core spacing / Placement of Pads,BUMPS
2. Macro to Macro spacing (Shouldn't be any criss cross connection b/w the macros)
3. Acceptable channel congestion
4. Proper blockage creation b/w the macros to avoid the high cells density issues
5. Base DRC (With proper physical cells addition for manufacturability reasons) should be clean


THANKS