ECE6028	NANOSCALE DEVICES AND CIRCUIT DESIGN	L	T	P	J	C
		2	0	0	4	3
Pre-requisite	**ECE5018 - Physics of VLSI Devices**					**v 1.0**

Course Objective:

The course is aimed to

1. Make student to understand CMOS scaling
2. understand theory and operation of multigate MOSFET and analog design digital, circuits using multigatedevicesaterials and their properties used for designing Microsensors.
3. understand the concepts of Microsystem technologies used for realizing Microsensors and actuators.
4. understand the working principles of Interface Electronic Circuits for resistive, capacitive and temperature sensors.

Expected Course Outcome:

At the end of the course the students will be able to

1. Understand the CMOS scaling
2. explain the need of novel MOSFET.
3. explain the physics of multigateMOS system
4. model nanowire FETs.
5. Design digital and analog circuit using multigate devices.
6. Understand the physics of CNTFET
7. Develop analytical model for novel FETs and validate them by numerical simulations..

Student Learning Outcomes (SLO):	**5,17**		
Module:1	**CMOS Scaling Issues and Solutions**	**2hours**	

MOSFET scaling, short channel effects, quantum effects, volume inversion, threshold voltage, channel engineering, source/drain engineering, high-k dielectric, strain engineering,multigate technology mobility, gate stack.

Module:2	**Introduction to Novel MOSFETs**	**2hours**	

SOI MOSFET, multigate transistors, single gate, double gate, triple gate, surround gate, Silicon Nanowire transistors

Module:3	**Physics of Multi-gate MOS System**	**5hours**	

MOS electrostatics, 1D, 2D MOS electrostatics, ultimate limits, double gate MOS system, gate voltage effect, semiconductor thickness effect, asymmetry effect, oxide thickness effect , electron tunnel current, two dimensional confinement, scattering

Module:4	**Nanowire FETS**	**5hours**	

Silicon nanowire MOSFETs, evaluation of I-V characteristics, I-V characteristics for non-degenerate carrier statistics, I-V characteristics for degenerate carrier statistics, electronic conduction in molecules, general model for ballistic nano transistors, CNT-FETs

Module:5	**Digital Circuit Design using Multi-gate Devices**	**5hours**	

Digital circuits design, impact of device performance on digital circuits, leakage performance trade off, multi VT devices and circuits, SRAM design			
Module:6	**Analog Circuit Design using Multi-gate Devices**	**5hours**	
Analog circuit design, trans-conductance, intrinsic gain, flicker noise, self-heating, band gap voltage reference, operational amplifier, comparator designs, mixed signal, successive approximation DAC, RF circuits			
Module:7	**Carbon Nanotube FET**	**4hours**	
CNT-FET, CNT memories, CNT based switches, logic gates, CNT based RF devices, CNT based RTDs, CNTFET based applications			
Module:8	**Contemporary issues**	**2 hours**	
	Total Lecture hours:	**30hours**	

Text Book(s)	
1.	J P Colinge, FINFETs and other Multi-gate Transistors, Springer, Germany, 2010.
2.	B.G.Park, S.W. Hwang &Y.J.Park, Nanoelectronic Devices, Pan Stanford Publisher, Singapore, 2012.
Reference Books	
1.	N. Collaert, CMOS Nanoelectronics: Innovative Devices, Architectures and Applications, Reprint Pan Stanford publisher, Singapore, 2012.
2.	Niraj K. Jha, Deming Chen, Nanoelectronic Circuit Design, Springer London, First Edition, 2011.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / QUIZ, Final Assessment Test (FAT).

List of Projects

1. Design and Extraction of DC and AC parameters of MOSFET with Source/Drain Extension
2. Performance Analysis of Double/Triple/Surround gate devices
3. Analysis of Gate Work Function Engineering in Multi-gate Devices
4. Single Event Upset/Soft Error Analysis in Multi-gate FETs
5. Comparison of CMOS and Fin FET based SRAM
6. Design of OTA and Comparator in Multi-gate Devices

Mode of Evaluation:Review I, II & III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016