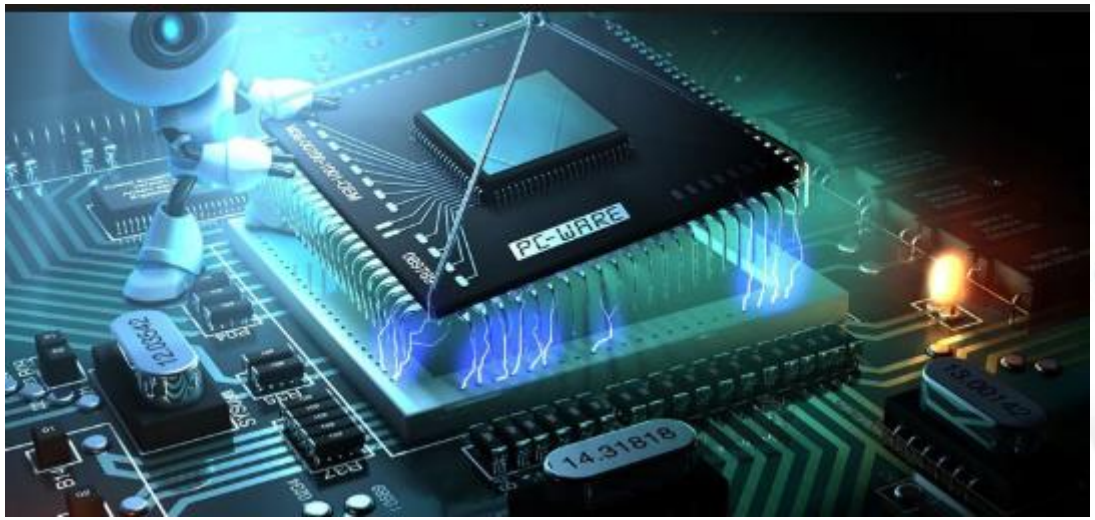


Placement and post placement optimization

Topics covered

- Pre placement setup and checks
- Types of blockages
- What is placement and it’s necessity
- Congestion and reasons for congestion
- Understanding the pre and post placement optimization
- Scan chain reordering

Pre placement checks (placement readiness)

Below are the few preplacement sanity checks to be performed before starting “placement of standard cells”

1. Appropriate MCMM scenarios were created

2. Clean “ZIC”- Zero interconnect timing QOR

3. Good understanding of “check_physical_design –stage pre_place_opt” report – It checks for readiness for placement of floorplan, netlist and Design constraints

4. “check_physical_constraints” checking

   It checks if any cells placed in hard placement blockage area, Metal layer inconsistencies against library, R/Cs for routing layers, Narrow placement regions, legal sites for cell placement and large RC variation b/w metal layers.

5. Macro/Pin placement completion

Pre placement setup

1. Make sure all the macro are having a fixed attribute

Command to check:- get_attribute [all_macro_cells] physical_status

If it's not fixed make sure to fix the macro attribute

set_attribute [all_macro_cells] physical_status fixed **or** set_dont_touch_placement [all_macro_cells]

2. Set the min/max layers to be used for Signal routing, this settings to be applied for preroute metal layer assignment/estimation

set_ignored_layers –max_routing_layer <> -min_routing_layer<>

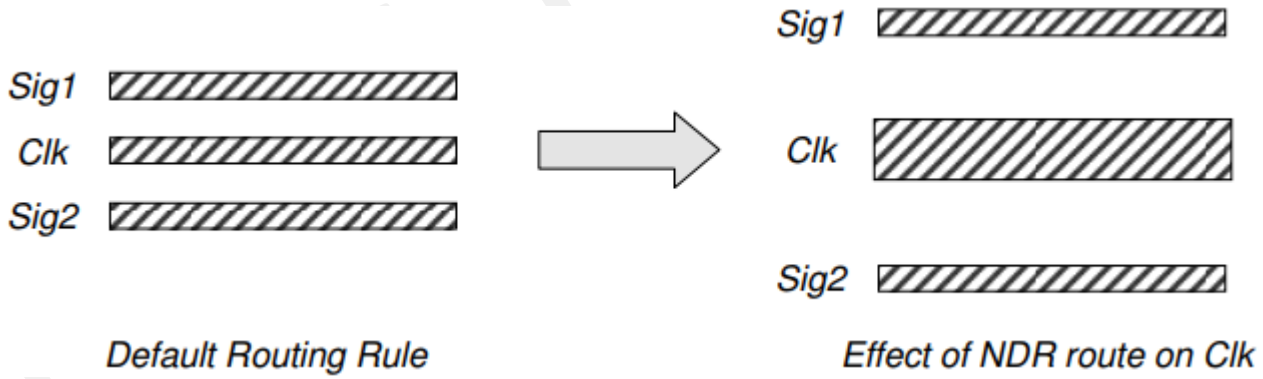
Layer you have set can be reported through "report_ignored_layers" command , it can be removed through "removed_ignored_layers -all"

Pre placement setup

3. Verify whether any keepout margins are applied (report_keepout_margin).

4. - It's good to define the NDR(Non default routing) for clock nets during placement stage for better RC estimation for clock nets .

- RC parasitic are different between NDR and Normal nets.
- NDR rules are applied to clock nets to avoid EM and cross talk effects.



Method to specify the NDR rules

- **Define the NDR rules:**

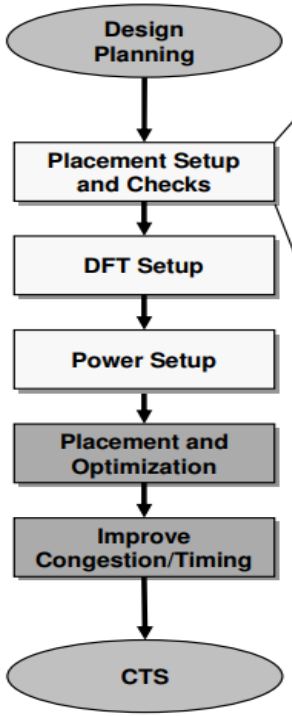
```
define_routing_rule MY_ROUTE_RULES   \
  -widths {METAL3 0.4 METAL4 0.6 METAL5 0.6} \
  -spacings {METAL3 0.5 METAL4 0.65 METAL5 0.65}
```

- **Configure the clock tree routing:**

```
set CLK_NETS [get_nets -of [all_fanout -flat -clock_tree]]
set_net_routing_rule -rule MY_ROUTE_RULES $CLK_NETS
set_net_routing_layer_constraint -min_layer METAL3 \
                                 -max_layer METAL5 $CLK_NETS
```

You may also specify the layers to be used for clock tree routing

Summary- Preplacement setup and checks




```
open_mw_cel DESIGN_floorplanned
link

set_dont_touch_placement [all_macro_cells]

report_ignored_layers
report_pnet_options

printvar physopt_hard_keepout_distance
printvar placer_soft_keepout_channel_width

# Define non-default routing rules, if applicable
define_routing_rule MY_ROUTE_RULES  \
  -widths {METAL3 0.4 METAL4 0.6 METAL5 0.6} \
  -spacings {METAL3 0.5 METAL4 0.65 METAL5 0.65}
set CLK_NETS \
      [get_nets -of [all_fanout -flat -clock_tree]]
set_net_routing_rule -rule MY_ROUTE_RULES $CLK_NETS
set_net_routing_layer_constraint -min_layer METAL3 \
                         -max_layer METAL5 $CLK_NETS

check_physical_design -stage pre_place_opt
check_physical_constraints
```

Types of blockages

1. Placement blockage

- Soft Blockage
- Hard blockage
- Partial placement blockage

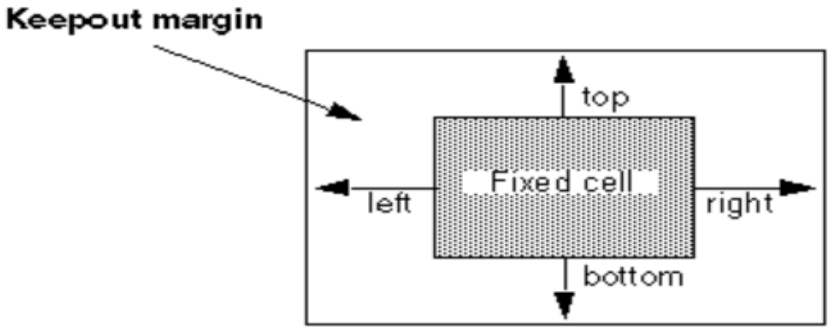
2. Routing blockage :- Routing blockage is added to block routing resource on one or more layer at specific region at certain point of the design

Blockages information

SL NO	Blockage type	Command to create the blockages	Details
1	Hard	create_placement_blockage -bbox {{x1 y1} {x2 y2} } -type hard	A hard blockage prevents the placement of standard cells and hard macros within the specified area during coarse placement, optimization, and legalization.
2	Soft	create_placement_blockage -bbox {{x1 y1} {x2 y2} } -type soft	A soft blockage prevents the placement of standard cells and hard macros within the specified area during coarse placement, but allows optimization and legalization to place cells within the specified area
3	Partial	create_placement_blockage -bbox {{x1 y1} {x2 y2}} \ -type partial -blocked_percentage	A partial blockage limits the cell density in the specified area during coarse placement, but has no effect during optimization and legalization
3.a	Partial-Buffer only	create_placement_blockage -bbox {{x1 y1} {x2 y2}}\ -type partial -blocked_percentage <X%> -buffer_only	Buffer-only blockage is a special type of partial blockage that allows only buffers and inverters to be placed within the blockage. To create a buffer-only blockage, use the -type partial, –blocked_percentage, and -buffer_only options.
3.b	Partial- no register	create_placement_blockage -bbox {{x1,y1} {x2 y2}} \ -type partial -blocked_percentage 50 -no_register	A no-register blockage is a special type of partial blockage that prevents registers from being placed within the blockage. To create a no-register blockage, use the -type partial, –blocked_percentage, and -no_register options.

Halos/keep out margins

1. HALO is the region around the boundary of fixed macro in the design in which no other macro or std cells can be placed. Halo allows placement of buffers and inverters in its area.
2. Halos of two adjacent macros can be overlap.
3. If the macros are moved from one place to another place, Halos will also be moved. But in the case of blockages if the macros are moved from one place to another place the blockages cannot be moved.



Congestion

Congestion :- If the number of available routing tracks is less than the number of required routing tracks

We need to do congestion analysis at each and every stage of physical design (For better routability)

Congestion are of two types

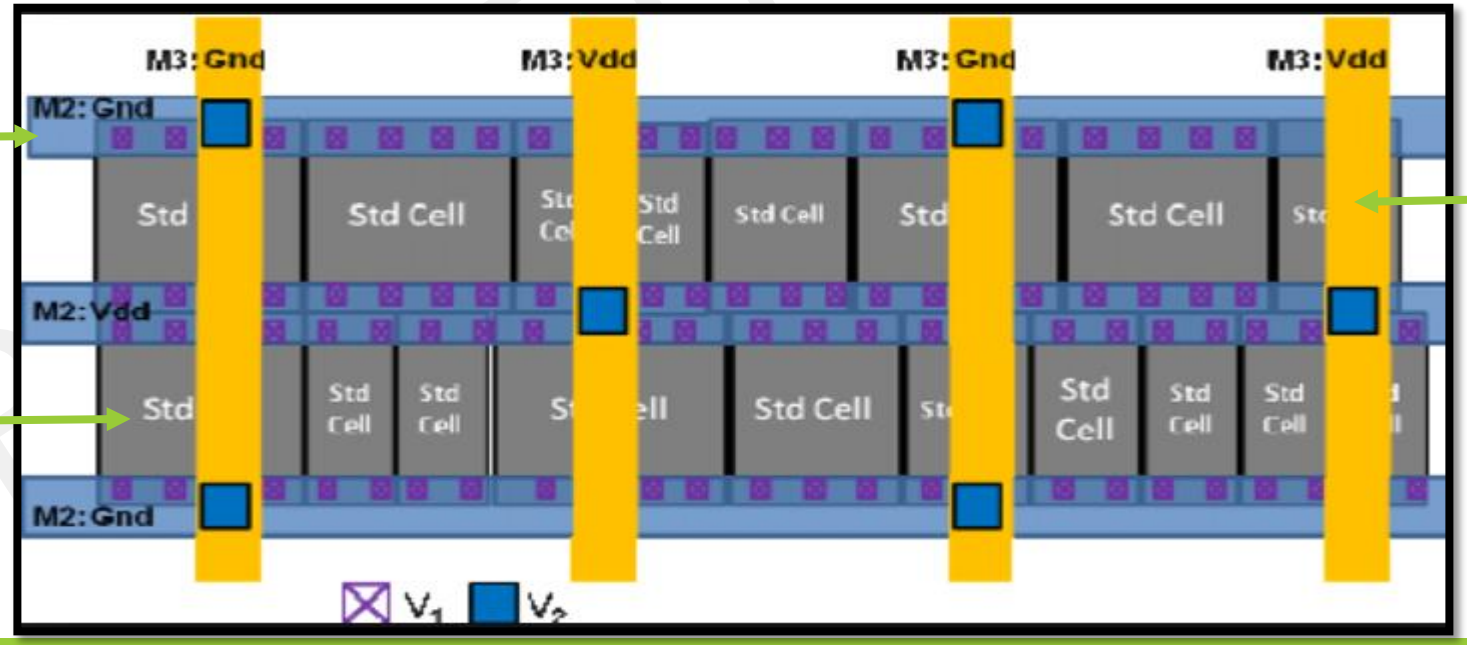
1. Global congestion
2. Local congestion

Possible reason for congestion

1. High standard cell count near macro edges
2. Lot of standard cells placed in small area
3. High pin count in local region (It may be due to OAI/AOI cells etc)
4. Bad macro placement
5. Bad Aspect ratio
6. Criss cross communication of logic

What is placement?

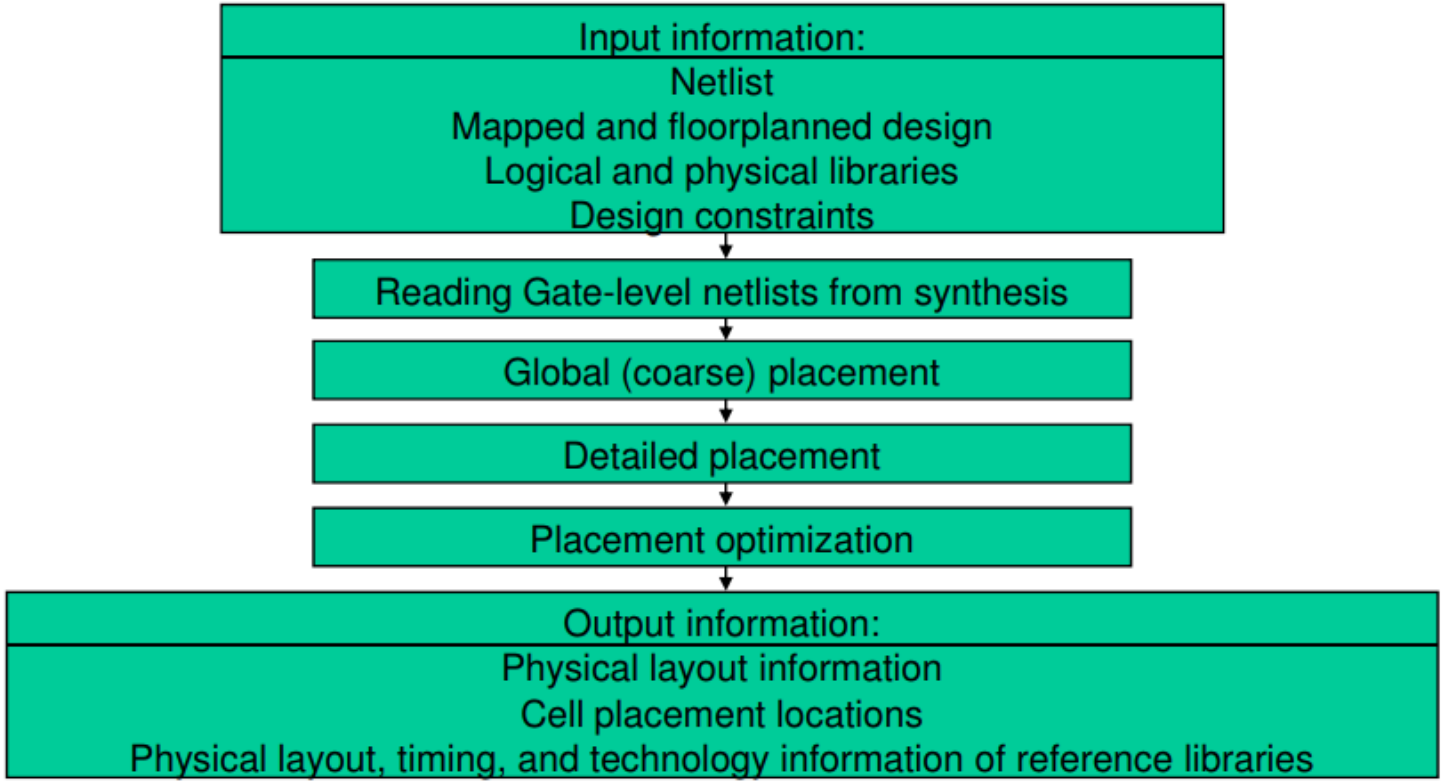
- "Placement" is a method of assigning physical locations for the cells specified in the logical gate level netlist .
- "Placeable" cells will be placed onto "sites" (sitting on site arrays) which were defined in the floorplan



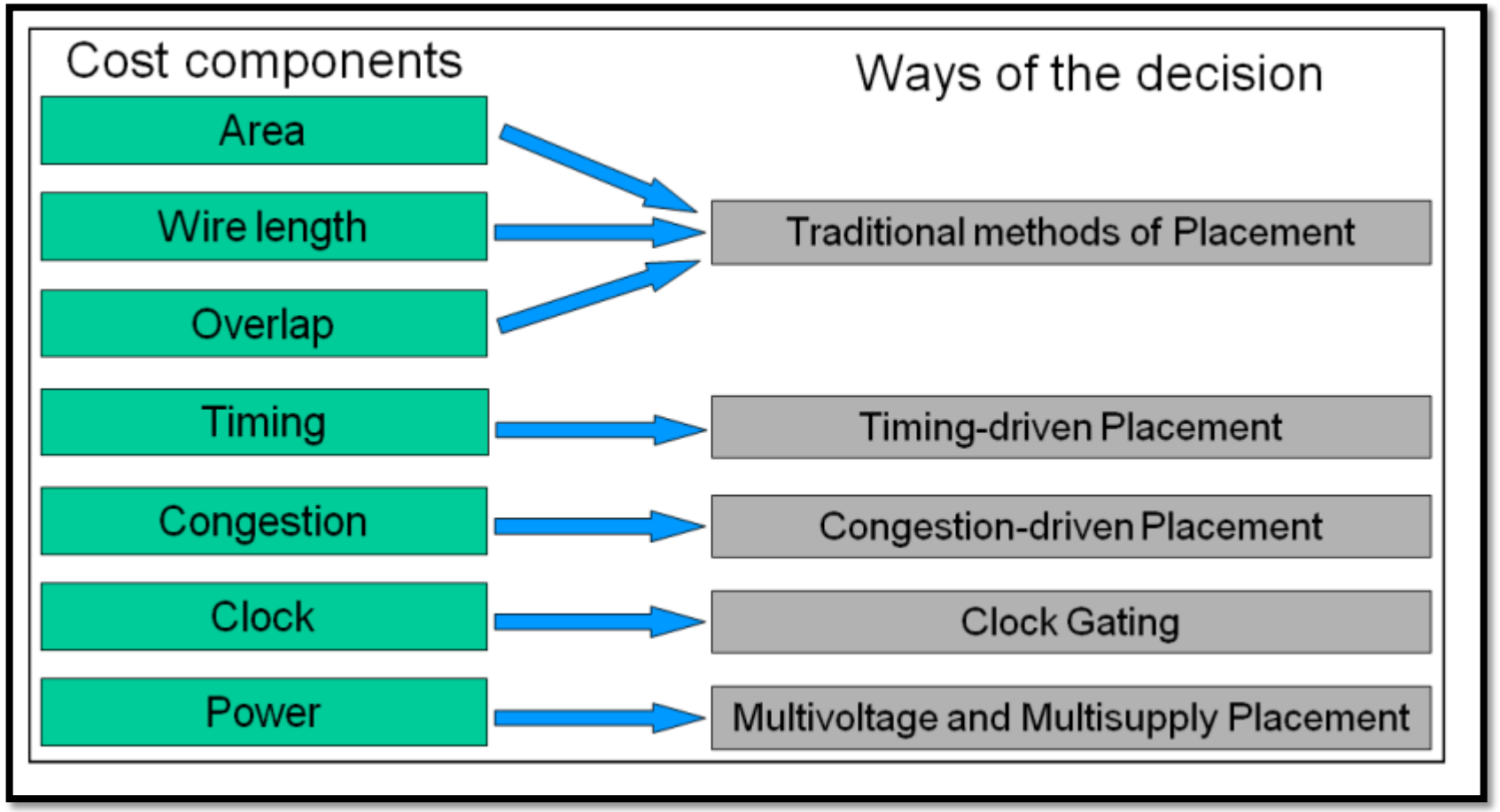
Placement goals

- Place the standard cell in legalized location
- Minimize all the critical net delays in the design
- Make sure router can complete the routing with minimal DRC’s- By reducing the congestion

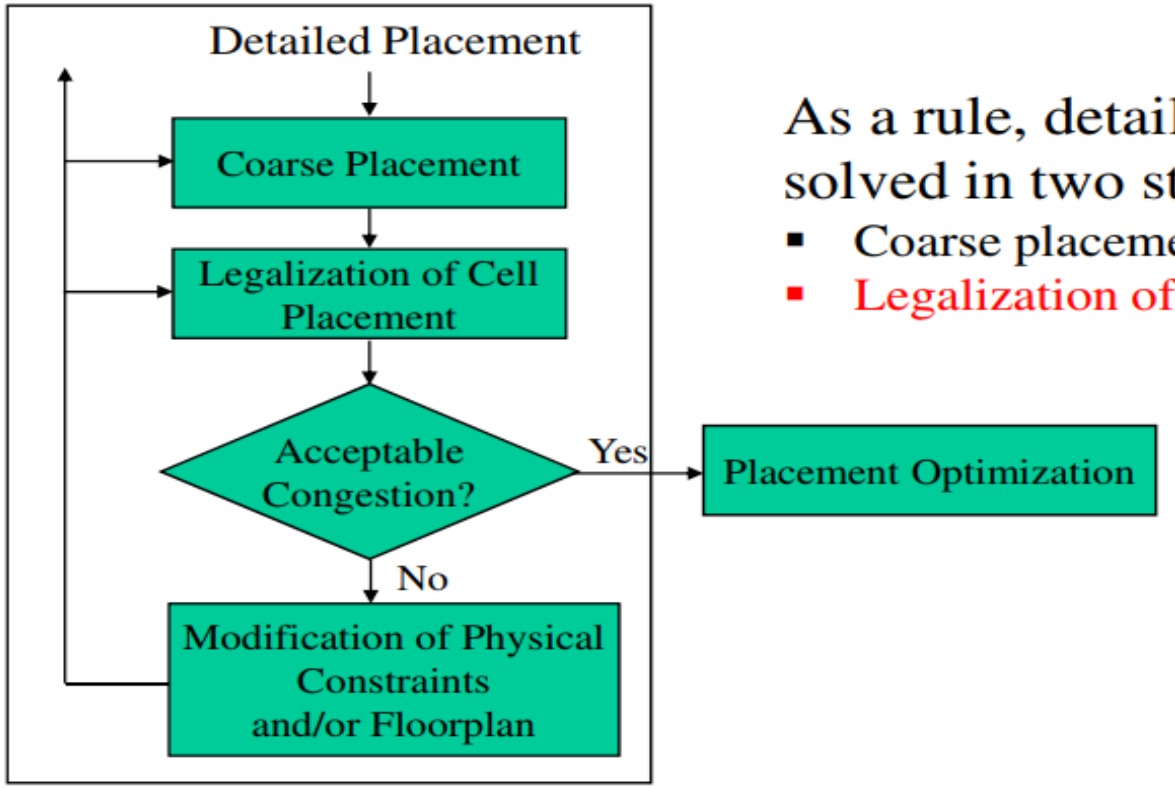
Placement stages



Placement Cost Components



Detailed placement

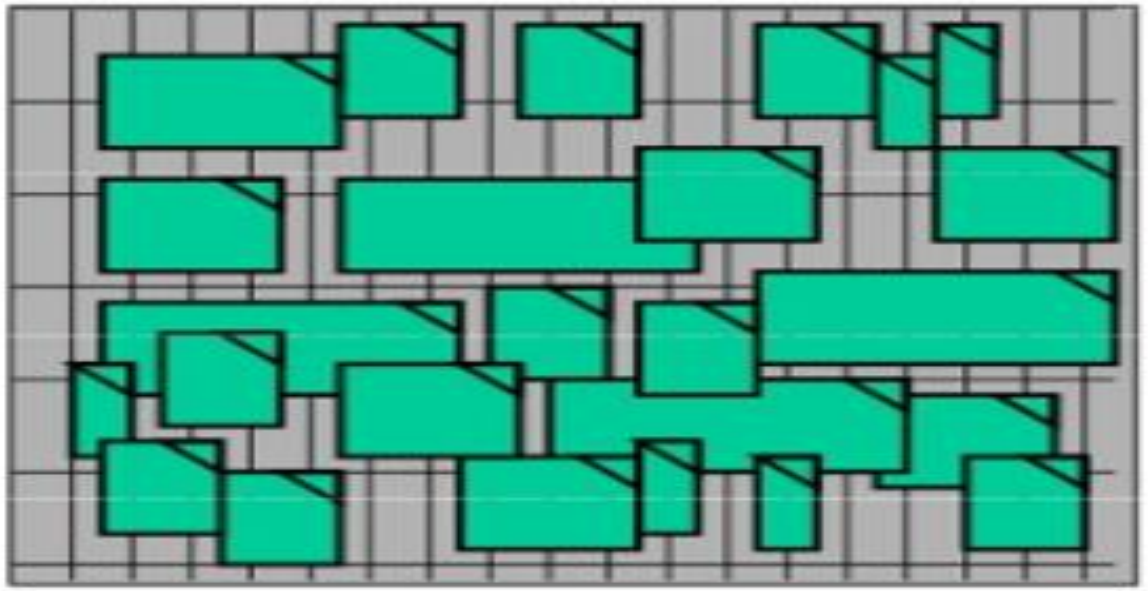


As a rule, detailed placement is solved in two stages:

- Coarse placement
- Legalization of cell placement

Coarse placement

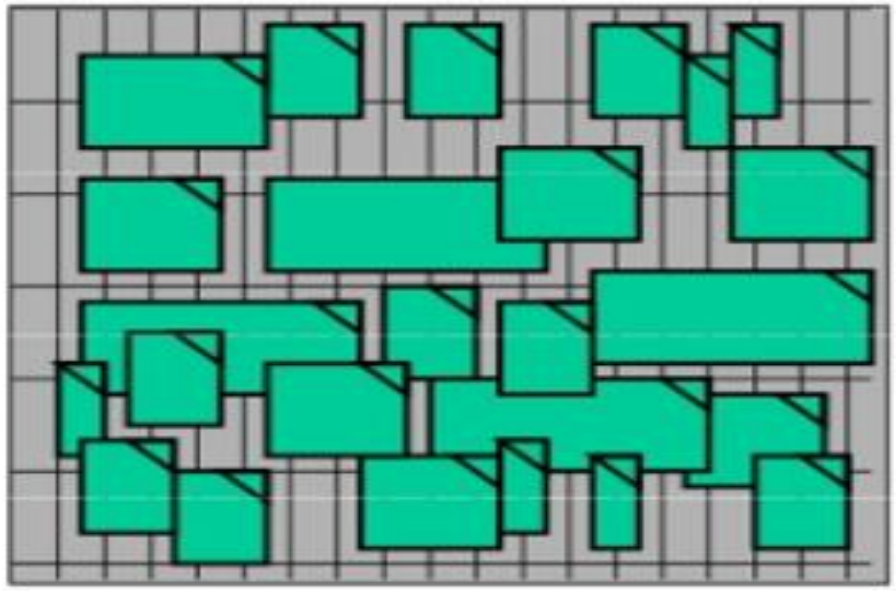
- Depending upon the logical connection in the netlist, standard cells placed in the approximate location in the core area .
- Cell are not placed in the legalized location .
- No logic optimization is done to fix any timing issues.



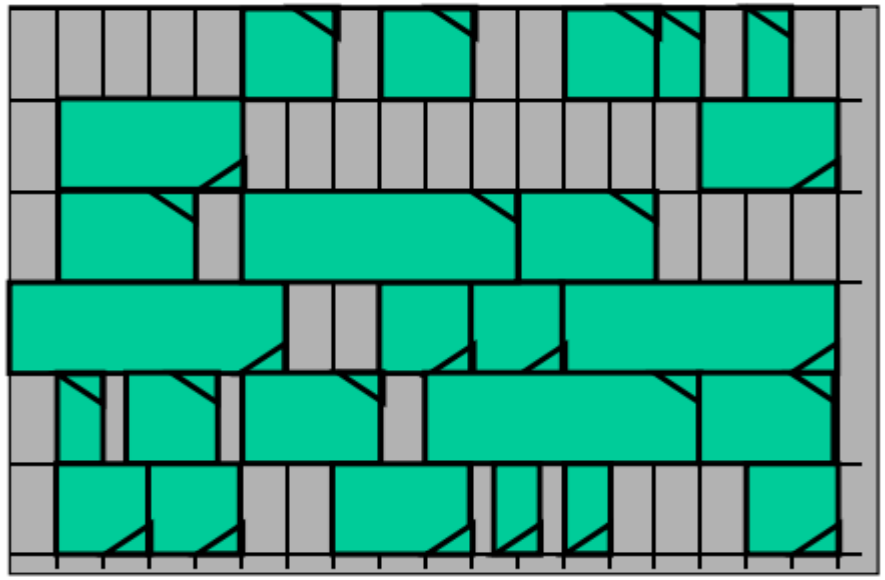
Legalize placement

- Ensure that legal placement is done before saving the design
- Legal placement of cells is not required for analyzing routing congestion at an early stage .

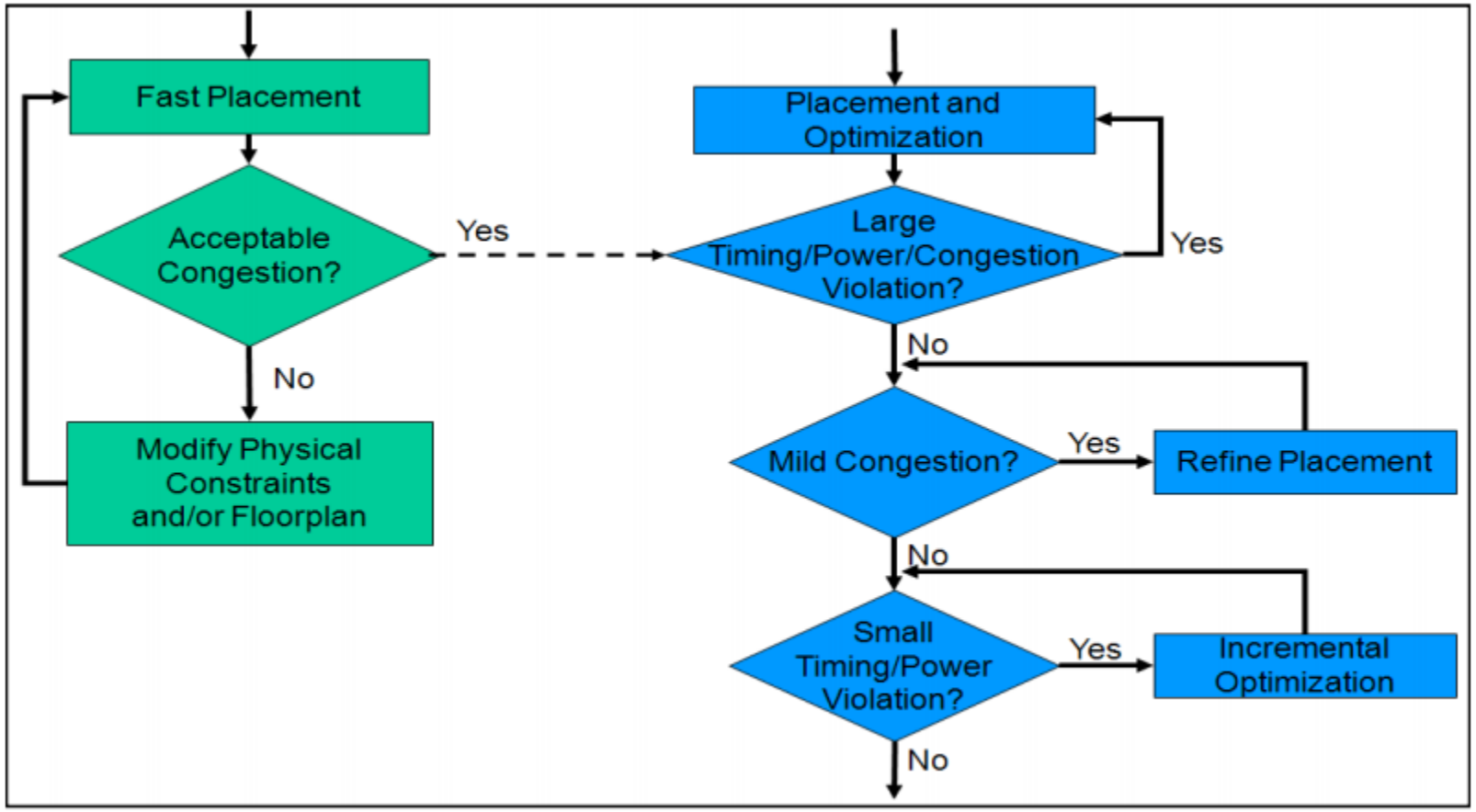
Coarse placement



legalized placement



IC compiler placement methodology

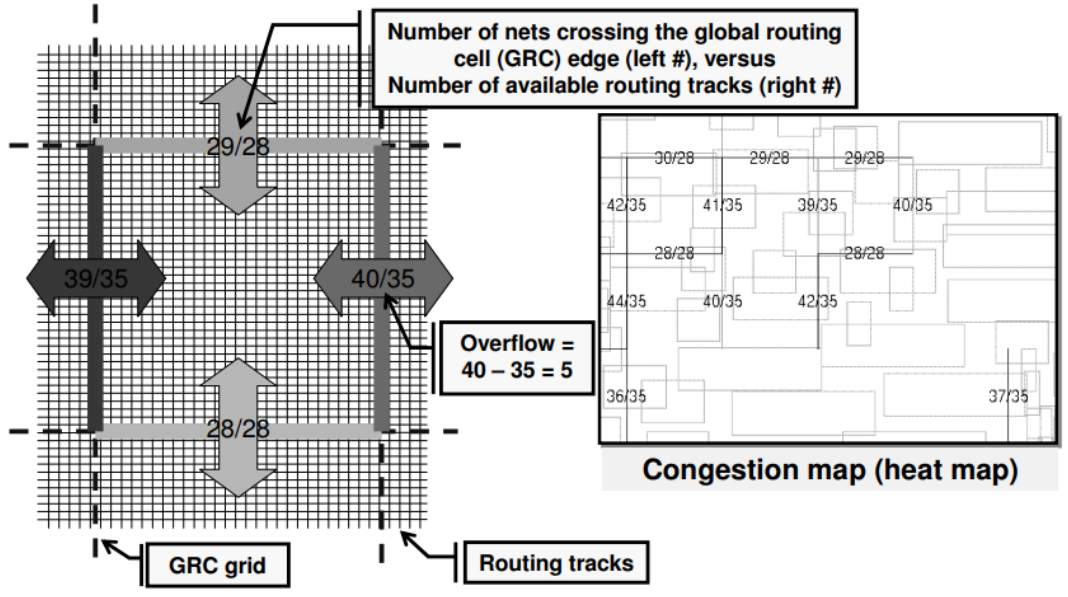


Congestion analysis

- Complete routing area in the design is divided into routing tracks. Routing tracks helps router to laid down the metal and via shapes in the design.

- Routing area is divided into GRC (Global routing cells) to analyze the congestion .

- Each GRC may contain many tracks

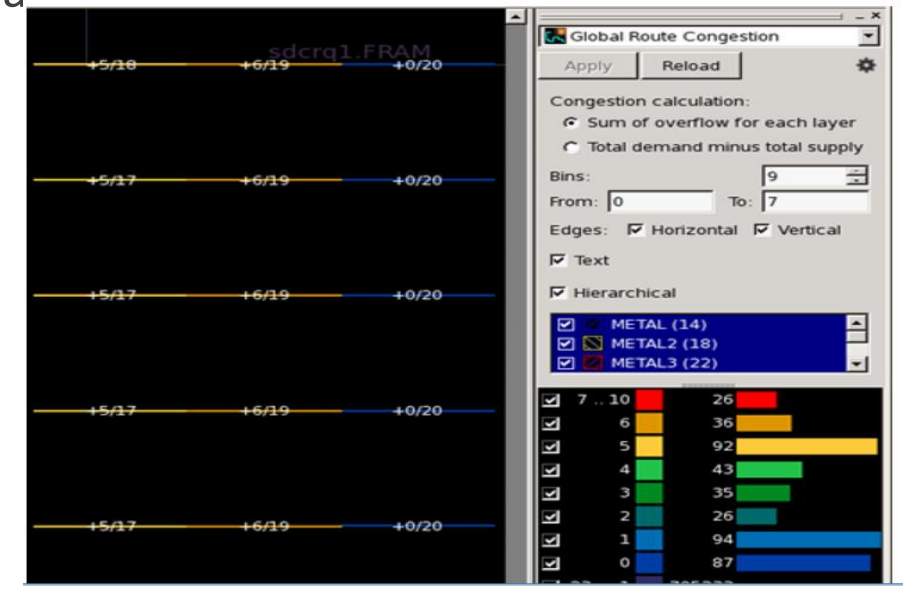


Overflow/underflow= Demand-Supply

Congestion analysis

- After loading the placement database execute “route_global –congestion_map_only” command in ICC shell to generate the congestion map. (In gui you can click on route->Global Route Congestion Map in the GUI and click Reload in the Map Mode dialog box to generate the map).

- There are two methods in GR (global route) congestion analysis
  - Sum of overflow for each layer (the default)
  - Demand minus total supply



Congestion analysis

- **Sum of overflow for each layer (the default)Demand minus total supply :-** In this mode, the tool calculates the congestion value as the sum of the overflow for all selected layers. Underflow is not considered; if a layer has underflow, it contributes zero overflow to the total overflow calculation.

- **Total demand minus total supply :-** In this mode, the tool calculates the congestion value by subtracting the supply for all selected layers from the demand for all selected layers. Note that because this calculation considers the underflow, it produces a more optimistic congestion result in regions that contain both overflow and underflow.

Congestion reduction techniques

- Before finding out the reduction techniques, need to root cause the reason behind congestion
- Below are the few of the possible ways to fix the congestion problems

  - ✓ After seeing the congestion maps check the congested area having high standard cell density. If you see such case than apply the partial blockages with less than the density in that particular area.

    Eg: if the congestion regions is let say 80% utilization then apply partial blockage with 60%

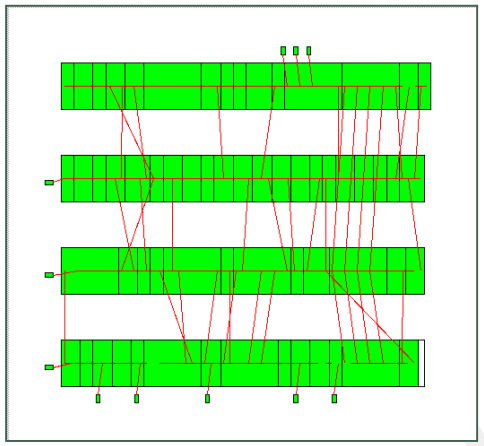
  - ✓ If you see the congestion near to the macro area then apply 5-10 microns of soft or hard blockage (better is 5 microns hard and 5 is soft is better). Because high critical timing path cell will be seated in the soft blockage area in the optimization phase.

  - ✓ If you see the congestion M2 M3 layers apply cell padding to the high number of pin standard cells (Eg. AOI, OAI,Full adders or other 4 i/p gates)

  - ✓ Congestion is at rectileanior areas apply the partial blockages

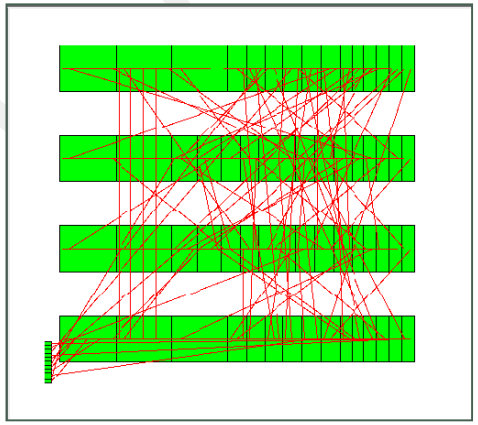
  - ✓ Using proper partial placement blockages (Desnity screens)

Good placement v/s Bad placement



Good placement

- No congestion
- Shorter wires
- Less metal levels
- Smaller delay
- Lower power dissipation



- Bad placement
  - Congestion
  - Longer wire lengths
  - More metal levels
  - Longer delay
  - Higher power dissipation

Bounds

- Bounds are placement constraints that control the placement of groups of leaf cells and hierarchical cells in the design.

- Bounds are of different types
  - ***Move bound***
  - Diamond bound
  - Ground bound

- Move bound are of different types
  - Hard move bound
  - Soft move bound
  - Exclusive bound

Move bound types

1. Hard move bound:- Hard move bounds force placement of the specified cells inside the bounds.

2. Soft move bound:- Soft move bounds specify placement goals, with no guarantee that the cells will be placed inside the bounds.

3. Exclusive bound:- Exclusive move bounds force the placement of the specified cells inside the bounds. All other cells must be placed outside the bounds.

Advantages of using bounds in the design

- Move bound allows you to group cells to minimize wire length
- Place the cells at most appropriate locations to improve timing QOR
- For best results, make the number of cells you place in placement bounds relatively small compared to the total number of cells in the design

Placement and optimization attributes

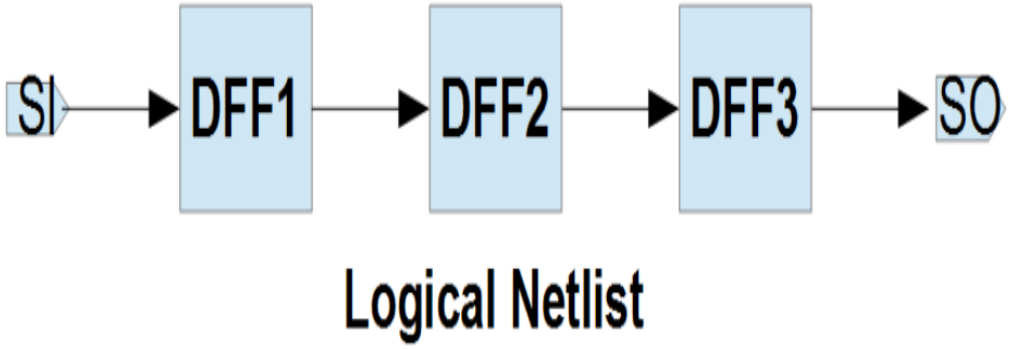
Typical Attributes	Coarse placement	Detailed placement	Optimization
Fixed	Cannot move cells	Cannot move cell	Cannot move, rotate, or resize cells
Imposed on clock buffers	Cannot move cells	Cannot move cells	Cannot move, rotate, or resize cells
Soft fixed	Cannot move cells	No restrictions	No restrictions
Size only	No restrictions	No restrictions	Can only resize cells
In place size only	Cannot move cells	No restrictions	Can resize cells only if there is room
Imposed on clock sinks	No restrictions	No restrictions	Can resize cells only if there is room
Don't touch	No restrictions	No restrictions	Cannot move, rotate, or resize cells

What is scan chain?

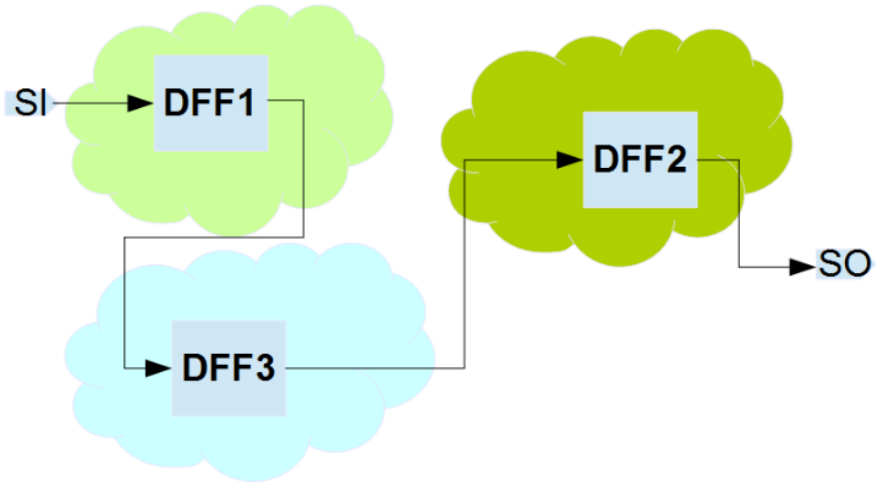
- Scan chains are groups of FFs that are serially connected through SI/SO pins
- Scan chain paths are active only during “test mode”, not during “functional mode”
- Scan chain is a technique used in design for testing. The objective is to make testing easier by providing a simple way to set and observe every flip-flop in an IC. The basic structure of scan include the following set of signals in order to control and observe the scan mechanism.
  - Scan_in and scan_out define the input and output of a scan chain. In a full scan mode usually each input drives only one chain and scan out observe one as well .
  - A scan enable pin is a special signal that is added to a design. When this signal is asserted, every flip-flop in the design is connected into a long shift register.
  - Clock signal which is used for controlling all the FFs in the chain during shift phase and the capture phase. An arbitrary pattern can be entered into the chain of flip-flops, and the state of every flip-flop can be read out.

Why Scan chain reordering done in PnR?

- Scan chains are long shift registers for ATPG purposes. Since these chains are stitched pre-layout, these need not be layout friendly. Because of this reason, we might see huge congestion issue.
- Without re-ordering of chains, scan chains contribute to a long total wire length. From a routability perspective it is important to reduce total wire length. This reduces (limited) metal demand and acts to reduce congestion.
- Implementation(PnR) tools detach the original scan chain , reorders them to improve the congestion problem.



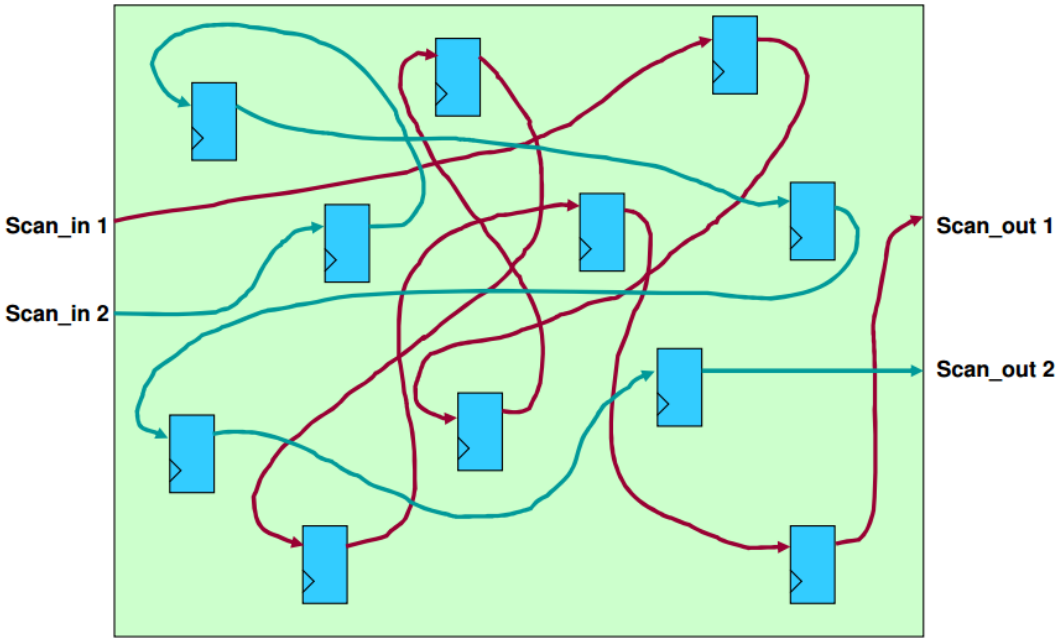
Logical Netlist



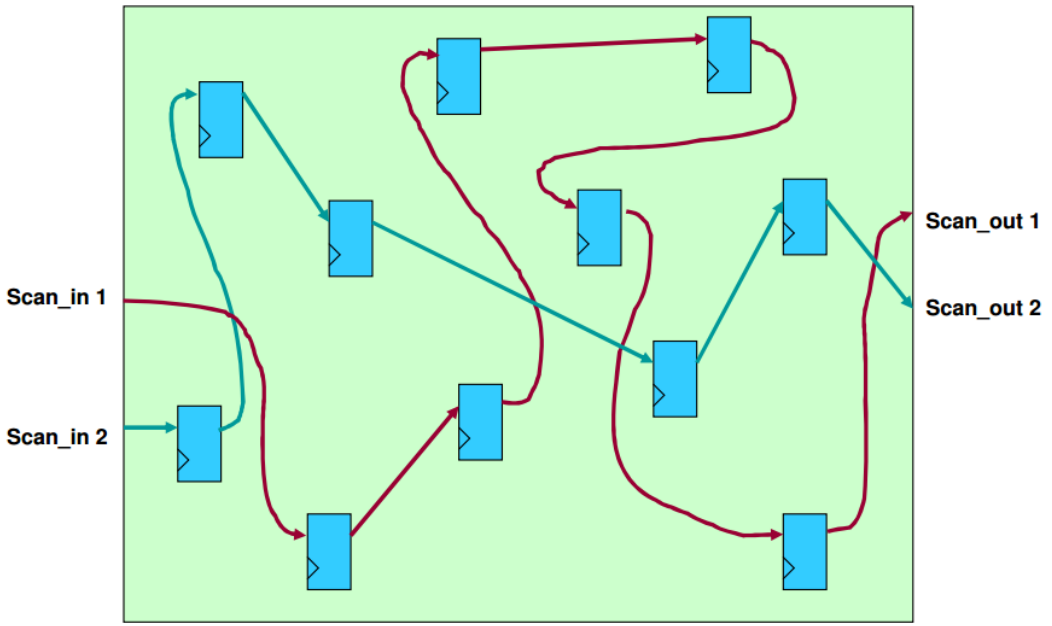
Physical Sythesis Netlist: After Reordering

Classic example of scan chain reordering

Placement unaware scan insertion



Scan chain reordering



Example of SCANDEF from Synthesis

```
DESIGN my_design ;
SCANCHAINS 2 ;
- 1
+ START PIN test_si1
+ FLOATING A ( IN SI ) ( OUT Q )
                B ( IN SI ) ( OUT Q )
                C ( IN SI ) ( OUT Q )
                D ( IN SI ) ( OUT Q )
+ PARTITION CLK_45_45
+ STOP PIN test_so1

- 2
+ START PIN test_si2
+ FLOATING E ( IN SI ) ( OUT Q )
                F ( IN SI ) ( OUT Q )
                G ( IN SI ) ( OUT Q )
                H ( IN SI ) ( OUT Q )
+ PARTITION CLK_45_45
+ STOP PIN test_so2
```

Design name

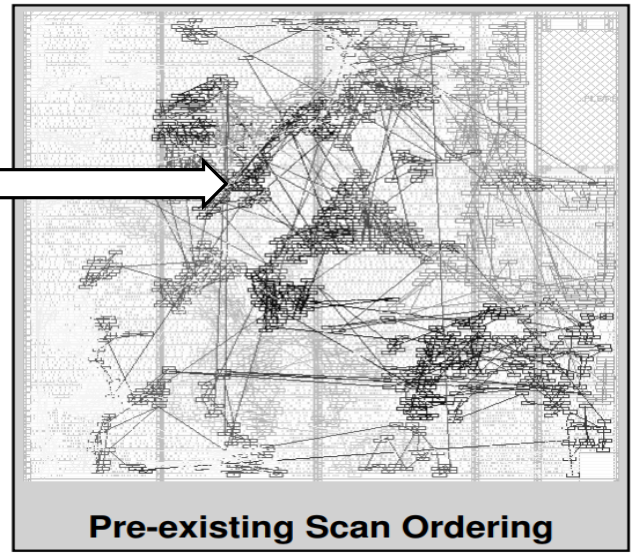
Number of chain stubs in the design

"**FLOATING**" indicates that these flipflops can be reordered

PARTITION keyword in SCANDEF. Flipflops can be swapped between two partitions with the same name

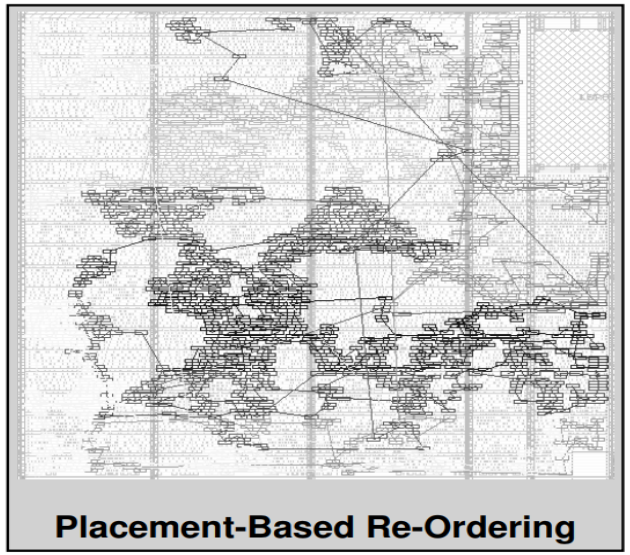
place_opt considered with DFT for optimization (DFT setup)

Congestion due to bad scan chain connections



Pre-existing Scan Ordering

```
place_opt
```

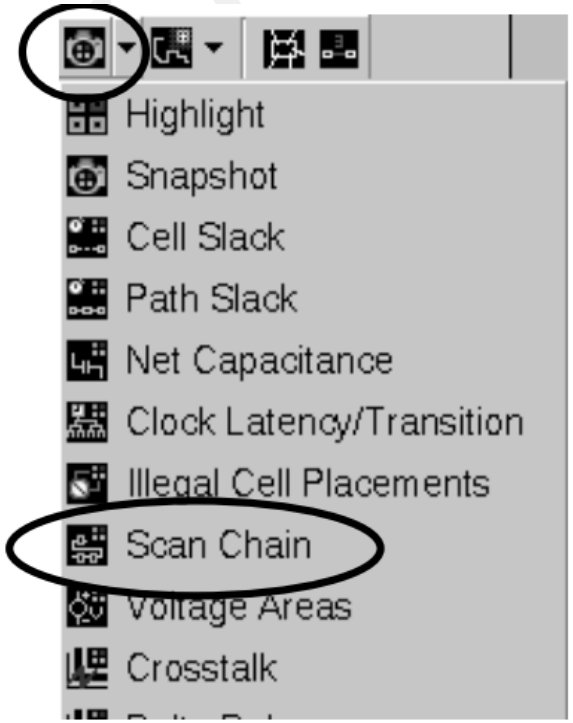


Placement-Based Re-Ordering

```
read_def DESIGN.scandef
report_scan_chain
place_opt -optimize_dft
```

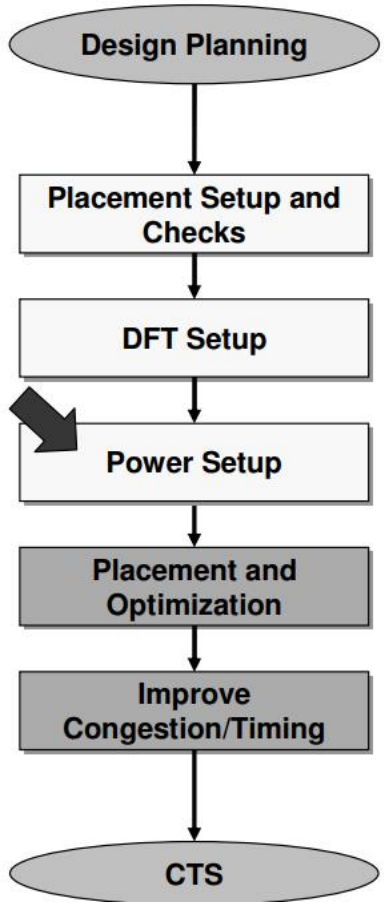
GUI option to report the scan chain

One of the modes available from the “Visual Mode” is to display scan chains. It allows you to highlight each scan chain in a different color.

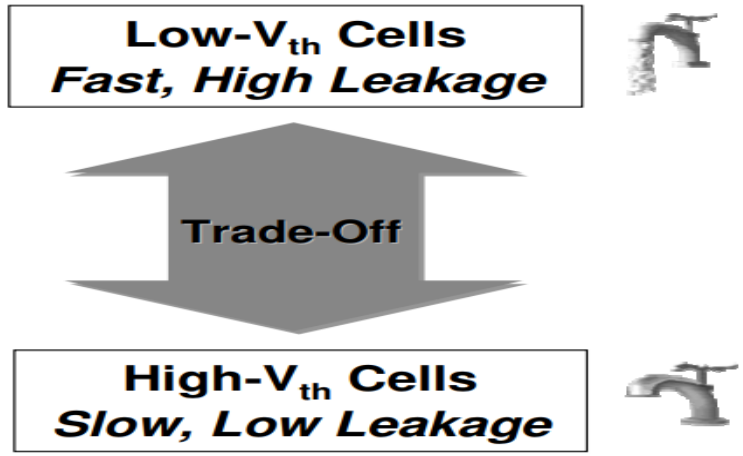


Power setup during place_opt stage

- If power optimization is critical in the design, then it's necessary to do power setup before placement and optimization
- Power optimization generally not impact the critical path
- Enabling the power optimization increases the run time
- Total power consumption = Internal + Switching+ Short circuit power



Leakage power optimization



- A multi-V_{th} library is the key to minimize leakage power
- Low V_{th} cells are used on critical paths to help timing
- High V_{th} cells are used on non-critical paths to save leakage power

```
set target_library  "hvt.db svt.db lvt.db"
create_mw_lib  ... -mw_reference_library \
   "mw/sc_hvt  mw/sc_svt  mw/sc_lvt  mw/io  mw/ram32"
set_power_options -leakage true|false
```

Leakage power optimization is enabled by default with `place_opt -power`, or can be explicitly controlled with `set_power_options -leakage true|false`

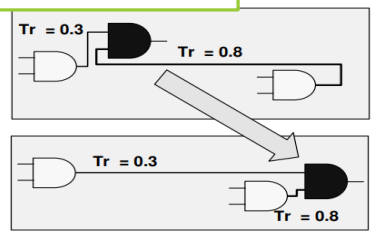
Reducing dynamic power dissipation

- Dynamic power optimization reduces power by identifying high “toggle rate” nets by reducing
  - Wire capacitance
  - Downsizing gates
- Two optimization techniques available during placement

Low power placement

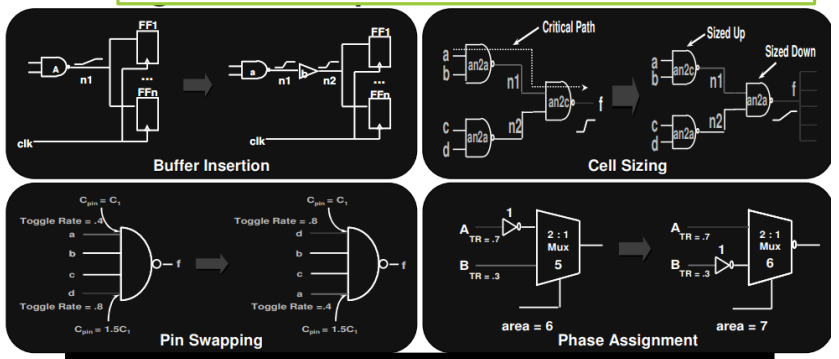
Low Power Placement (LPP):

- **Moves cells closer to shorten <u>non-clock</u> high-activity nets**
  - Clock tree LPP is done later, after `place_opt`, but pre-CTS
- **Must be enabled – OFF by default**



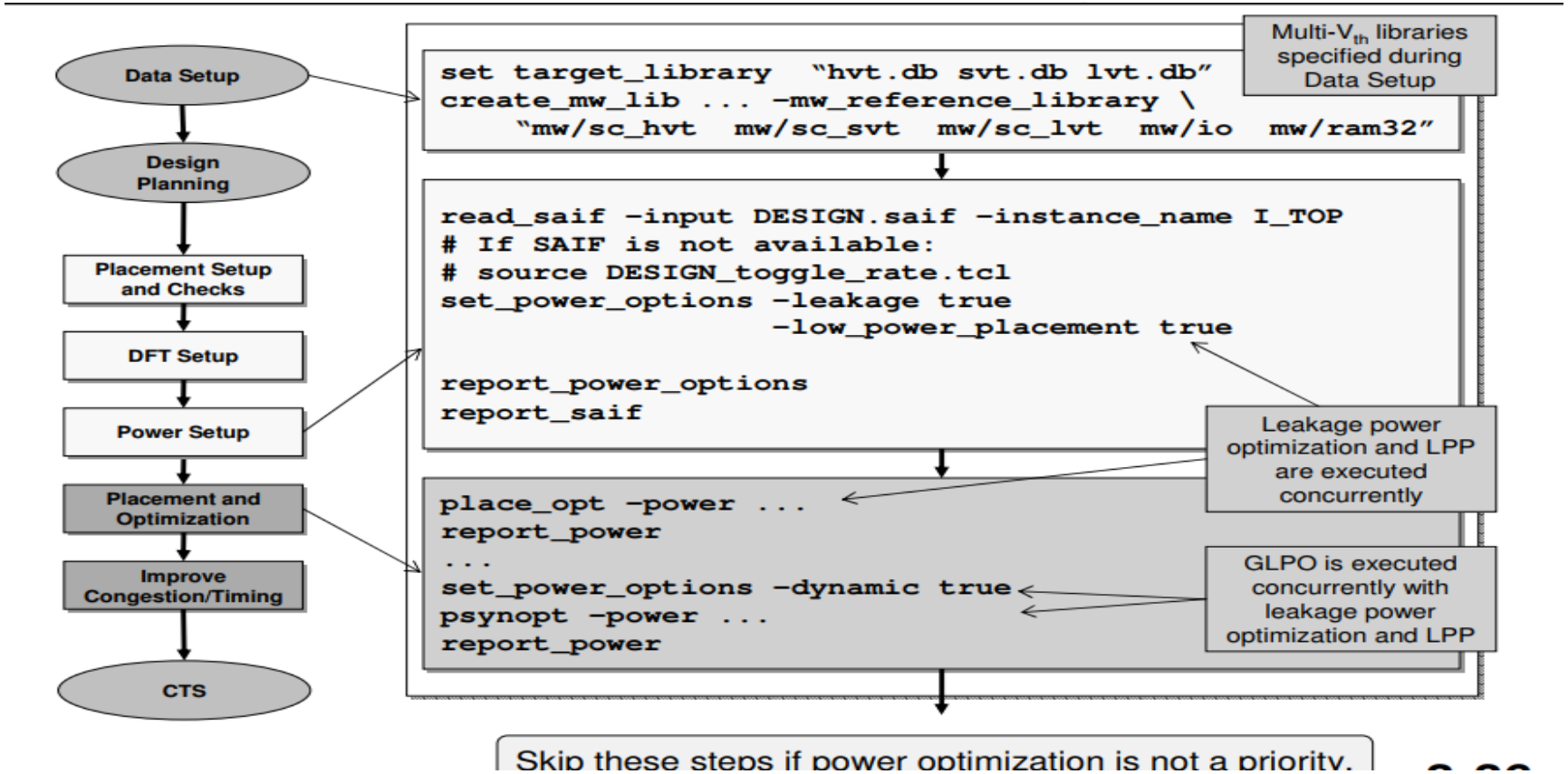

```
read_saif -input DESIGN.saif -instance_name I_TOP
# If SAIF is not available:
# source DESIGN_toggle_rate.tcl
set_power_options -low_power_placement true
report_power_options
...
place_opt -power
```

Gate level power optimization




```
set_power_options -low_power_placement true
place_opt -power
...
set_power_options -dynamic true
psynopt -power
```

Summary – Power optimization flow

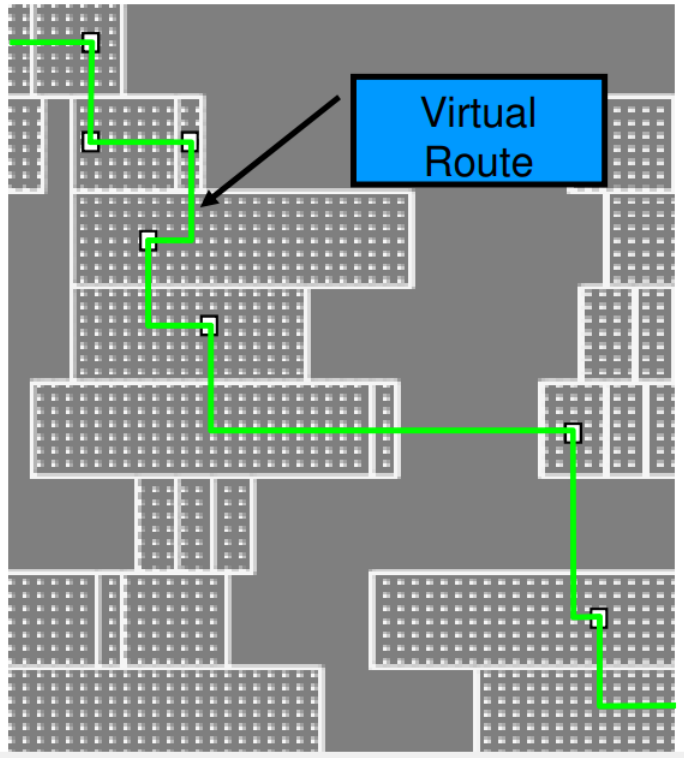


Timing driven placement

- All steps including placement are timing-driven

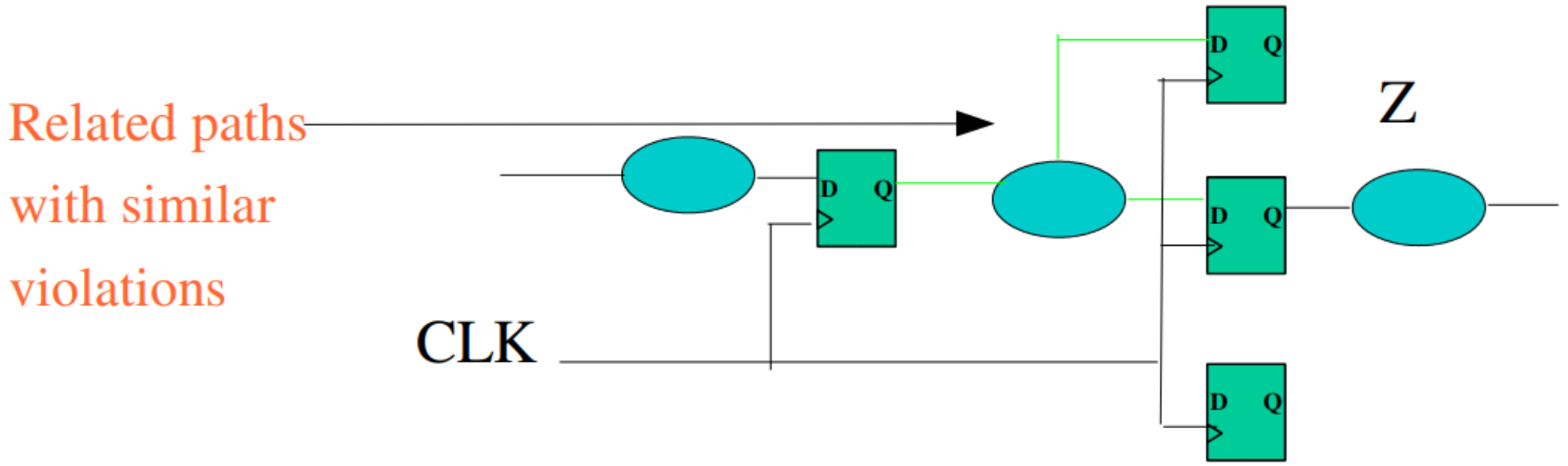
- Timing-driven placement tries to place critical path cells close together to reduce net RCs and to meet setup timing

- RCs are based on Virtual Route (VR)



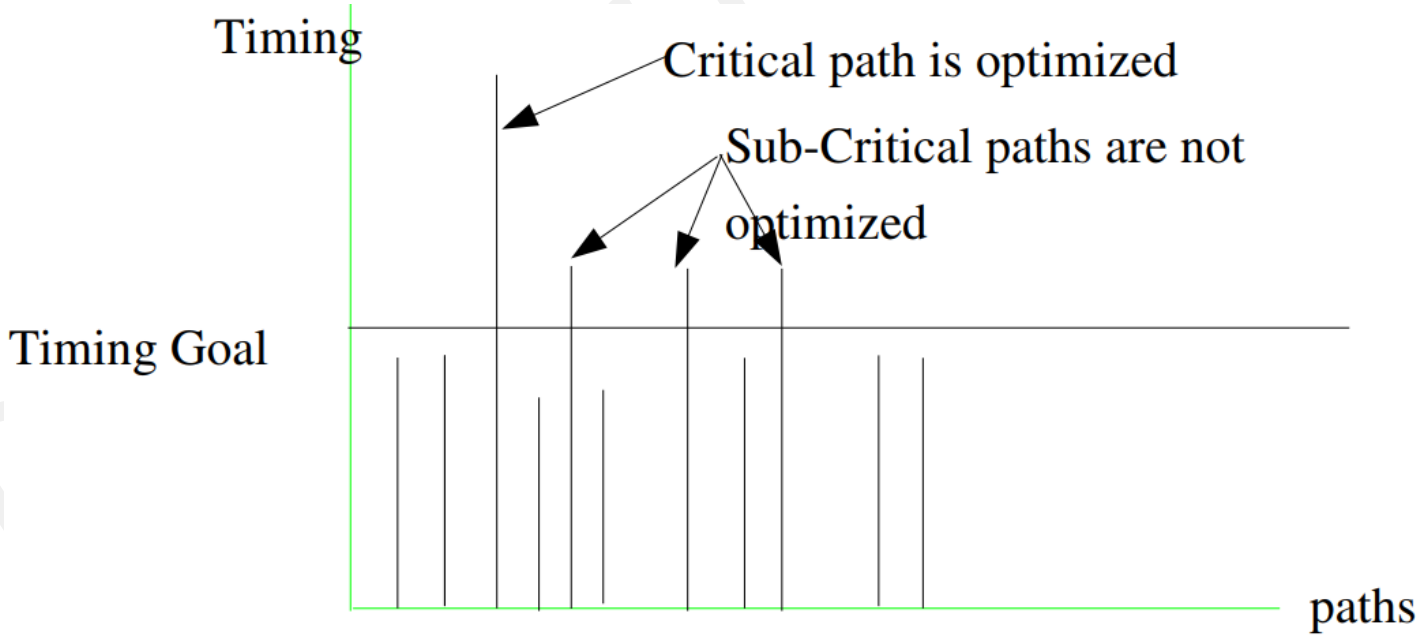
What Does it mean if TNS >> WNS?

- A large TNS implies that there could be many sub-critical violations that are almost as bad as the critical path violation
- It is also possible that these paths are 'related', or share logic.
- We can verify by analyzing the sub-critical paths with detailed timing reports



What does Optimization Do By Default?

- By default, logic optimization during placement works only on the critical path of each clock domain, and stops when it cannot further improve its timing
- Sub-critical paths are not optimized!



If TNS >> WNS Critical Range Optimization

- Critical Range Optimization (CRO) works on the sub critical paths, which reduces the total number of violations paths and the TNS
- CRO may also help to reduce the critical path violations if it is 'related‘ to some of the sub-critical paths

Key metrics to be checked after placement/optimization

1. Legal placement completed – “check_legality”
2. Power and ground nets should be prerouted
3. Acceptable congestion values
4. Acceptable timing values (WNS and TNS for all the path groups in the design)
5. High fanout net synthesis is done (Nets :- reset, scan enable) . Clock network shouldn’t be buffered
6. Acceptable DRV’s

Possible ways to improve the timing QOR in placement stage in ICC

1. Cells are sitting far apart in the hierarchy and wire length is high, timing QOR can be improved by placing them together by creating the bounds

2. Assigning separate path group for the violating hierarchy (command :- group_path)

3. Assigning different weight value to different path groups depending upon the timing QOR degradations (group_path –weight)

4. Try setting the high timing effort app option and execute the “place_opt” command.

5. Incrementally running the logic optimization through (psynopt)

Tools used for placement

1. ICC1 and ICC2 – Synopsys
2. EDI and Innovus – Cadence
3. Aprisa – Avatar integrated systems

Placement related lab exercises

1. Create different blockages and execute “create_placement” & “legalize_placement” and understand the differences in standard cell placement

2. Explore different placement GUI features

3. Create different types of “bounds” and understand the impact on “timinig” QOR and standard cell placement

4. Understand the different congestion methods in ICC

5. Explore different GUI maps need to be analyzed to decide placement quality

6. Understand the placement utilization (“report_placement_utilization”)

7. Understand the timing QOR at placement stage

Placement related lab exercises

8. Compare the timing and power QOR by providing different VT cells in the target_library list before place_opt command execution.

		Power QOR		
VT type	timing QOR	Internal power	leakage	switching power
SLVT				
LVT				
HVT				

9. Tabulate the below results without any optimization techniques
   - Timing (report_qor)
   - Area (report_area)
   - Power (report_power)
   - Placement utilization (report_placement_utilization)


THANKS