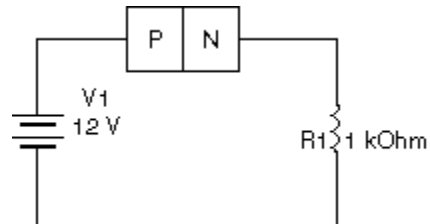


CMOS QUESTIONS

1. Ionization within a P-N junction causes a layer on each side of the barrier called the:
 - a. Junction
 - b. depletion region
 - c. barrier voltage
 - d. forward voltage
2. What causes the depletion region?
 - a. Doping
 - b. Diffusion
 - c. barrier potential
 - d. ions
3. What is an energy gap?
 - a. the space between two orbital shells
 - b. the energy equal to the energy acquired by an electron passing a 1 V electric field
 - c. the energy band in which electrons can move freely
 - d. an energy level at which an electron can exist
4. When an electron jumps from the valence shell to the conduction band, it leaves a gap. What is this gap called?
 - a. energy gap
 - b. hole
 - c. electron-hole pair
 - d. recombination
5. Forward bias of a silicon P-N junction will produce a barrier voltage of approximately how many volts?
 - a. 0.2
 - b. 0.3
 - c. 0.7
 - d. 0.8
6. When is a P-N junction formed?
 - a. in a depletion region
 - b. in a large reverse biased region
 - c. the point at which two opposite doped materials come together

d. whenever there is a forward voltage drop

7. What is the voltage across R1 if the P-N junction is made of silicon?



- a. 12 V
- b. 11.7 V
- c. 11.3 V
- d. 0 V

8. If conductance increases as temperature increases, this is known as a:

- a. positive coefficient
- b. negative current flow
- c. negative coefficient
- d. positive resistance

9. Which of the following cannot actually move?

- a. majority carriers
- b. ions
- c. holes
- d. free electrons

10. What electrical characteristic of intrinsic semiconductor material is controlled by the addition of impurities?

- a. Conductivity
- b. Resistance
- c. Power
- d. all of the above

11. Junction Field Effect Transistors (JFET) contain how many diodes?

- a. 4
- b. 3
- c. 2
- d. 1

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12. In the constant-current region, how will the I_{DS} change in an n-channel JFET?
- a. As V_{GS} decreases I_D decreases.
 - b. As V_{GS} increases I_D increases.
 - c. As V_{GS} decreases I_D remains constant.
 - d. As V_{GS} increases I_D remains constant.
13. A MOSFET has how many terminals?
- a. 2 or 3
 - b. 3
 - c. 4
 - d. 3 or 4
14. I_{DSS} can be defined as:
- a. the minimum possible drain current
 - b. the maximum possible current with V_{GS} held at -4 V
 - c. the maximum possible current with V_{GS} held at 0 V
 - d. the maximum drain current with the source shorted
15. A very simple bias for a D-MOSFET is called:
- a. self-biasing
 - b. gate biasing
 - c. zero biasing
 - d. voltage-divider biasing
16. With the E-MOSFET, when gate input voltage is zero, drain current is:
- a. at saturation
 - b. zero
 - c. I_{DSS}
 - d. widening the channel
17. When an input signal reduces the channel size, the process is called:
- a. Enhancement
 - b. substrate connecting
 - c. gate charge
 - d. depletion
18. Which JFET configuration would connect a high-resistance signal source to a low-resistance load?
- a. source follower

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- b. common-source
 - c. common-drain
 - d. common-gate
19. How will electrons flow through a p-channel JFET?
- a. from source to drain
 - b. from source to gate
 - c. from drain to gate
 - d. from drain to source
20. When $V_{GS} = 0\text{ V}$, a JFET is:
- a. Saturated
 - b. an analog device
 - c. an open switch
 - d. cut off
21. When applied input voltage varies the resistance of a channel, the result is called:
- a. Saturation
 - b. Polarization
 - c. Cutoff
 - d. field effect
22. When is a vertical channel E-MOSFET used?
- a. for high frequencies
 - b. for high voltages
 - c. for high currents
 - d. for high resistances
23. When the JFET is no longer able to control the current, this point is called the:
- a. breakdown region
 - b. depletion region
 - c. saturation point
 - d. pinch-off region
24. With a JFET, a ratio of output current change against an input voltage change is called:
- a. transconductance
 - b. siemens
 - c. resistivity
 - d. gain

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25. Which type of JFET bias requires a negative supply voltage?

- a. Feedback
- b. Source
- c. Gate
- d. voltage divider

26. The type of bias most often used with E-MOSFET circuits is:

- a. constant current
- b. drain-feedback
- c. voltage-divider
- d. zero biasing

27. The transconductance curve of a JFET is a graph of:

- a. I_S versus V_{DS}
- b. I_C versus V_{CE}
- c. I_D versus V_{GS}
- d. $I_D \times R_{DS}$

28. Which component is considered to be an "OFF" device?

- a. Transistor
- b. JFET
- c. D-MOSFET
- d. E-MOSFET

29. In an n-channel JFET, what will happen at the pinch-off voltage?

- a. the value of V_{DS} at which further increases in V_{DS} will cause no further increase in I_D
- b. the value of V_{GS} at which further decreases in V_{GS} will cause no further increases in I_D
- c. the value of V_{DG} at which further decreases in V_{DG} will cause no further increases in I_D
- d. the value of V_{DS} at which further increases in V_{GS} will cause no further increases in I_D

30. The primary function of the bias circuit is to

- a. hold the circuit stable at VCC
- b. hold the circuit stable at v_{in}
- c. ensure proper gain is achieved
- d. hold the circuit stable at the designed Q-point

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31. A JFET

- a. is a current-controlled device
- b. has a low input resistance
- c. is a voltage-controlled device
- d. is always forward-biased

32. The capacitor that produces an ac ground is called a(n)

- a. coupling capacitor
- b. dc open
- c. bypass capacitor
- d. ac open

33. When transistors are used in digital circuits they usually operate in the:

- a. active region
- b. breakdown region
- c. saturation and cutoff regions
- d. linear region

34. A current ratio of I_C/I_E is usually less than one and is called:

- a. beta
- b. theta
- c. alpha
- d. omega

35. In a C-E configuration, an emitter resistor is used for:

- a. Stabilization
- b. ac signal bypass
- c. collector bias
- d. higher gain

36. Voltage-divider bias provides:

- a. an unstable Q point
- b. a stable Q point
- c. a Q point that easily varies with changes in the transistor's current gain
- d. a Q point that is stable and easily varies with changes in the transistor's current gain

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37. The digital logic family which has minimum power dissipation is

- a. TTL
- b. RTL
- c. DTL
- d. **CMOS**

38. CMOS circuits are extensively used for ON-chip computers mainly because of their extremely

- a. low power dissipation.
- b. high noise immunity.
- c. **large packing density.**
- d. low cost.

39. The guard rings are used to reduce

- a. V_t
- b. **latch up**
- c. Width of channel
- d. C_{GS}

40. The rate of oxidation depends on

- a) Supply of oxidation to the surface
- b) The reaction rate constant R_i and C_i
- c) Mobility
- d) **Both a and b.**

41. The layers of MOS technology are isolated from each other by

- a. Dielectric
- b. **Thin oxide**
- c. Polysilicon
- d. Oxide layers

42. Load capacitance effects _____.

- a. **Power Consumption**
- b. Connectivity
- c. Chip Density
- d. None

43. An interconnect line is made from a material with resistivity $4\text{ohm} / \text{cm}$ and thickness of 1200um . Sheet resistance is _____

- a. **1375Ω**
- b. 1200Ω
- c. 500Ω
- d. 2000Ω

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44. For P- transistor channel R_s in $5\mu\text{m}$ technology is
- 10^4
 - 2.5×10^4**
 - 3×10^4
 - 3.5×10^4
45. The source and drain are connected by a conducting channel but the channel may now be cleared by applying a suitable _____ voltage to the gate.
- Positive
 - negative**
 - not possible
 - threshold voltage
46. Guard rings prevent the formation of _____ and contact cuts.
- Parasitic Transistors**
 - Capacitance
 - Resistance
 - None
47. _____ is used to provide a connection between the output and V_{dd} any time the output of the logic gate is meant to be 1.
- Pull Up Network (PUN)**
 - Pull Down Network (PUD)
 - A and b
 - None
48. If a gate is connected to a suitable positive voltage then a _____ is formed between the source and drain.
- Conductive layer.**
 - Transistor
 - Capacitance
 - Resistance
49. The thickness of Silicon dioxide layer (SiO_2) layer is typically _____ thick.
- $10\mu\text{m}$.
 - $5\mu\text{m}$.
 - $1\mu\text{m}$.**
 - $23\mu\text{m}$.
50. The voltage applied between the gate and source of a MOS device, below which the drain -to-source current effectively drops to zero, is _____.
- Threshold voltage**
 - Bulk Voltage
 - Parasitic voltage
 - None

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51. The slope of the voltage transfer characteristics is equal to _____.
a. $-3/4$
b. 3
c. -1
d. 1
52. _____ is used to reduce the number of transistors required to implement a given logic information.

Ans: **Ratioed Logic**

53. Scaling improves the _____ by shrinking the dimensions of transistors and interconnection between them.
a. packing density
b. power dissipation
c. **figure of merit**
d. Channel Length
54. The high noise margin is given by $NM_H =$
a. $2(V_{IH} - V_{OH})$
b. $V_{IH} - V_{OH}$
c. **$V_{OH} - V_{IH}$**
d. $V_{IH} + V_{OH}$
55. The process of transferring patterns of geometric shapes in a mask to a layer of radiation sensitive material for covering surface of semiconductor wafer is called
a. Metallization
b. **Lithography**
c. Diffusion
d. Ion implantation
56. Which of the following is due to the switching transient current and charging and discharging of load capacitance?
a. static power dissipation
b. **dynamic power dissipation**
c. steady state power dissipation
d. none of the above
57. The variation of threshold voltage due to source to substrate voltage is referred as _____.
a. **Body effect**
b. Latch up
c. ESD
d. Antenna Effect
58. A parallel combination of nMOS and pMOS transistor is called as _____.
a. CMOS

- b. **Transmission Gates**
 - c. Dynamic CMOS
 - d. None
59. _____ is an alternate gate circuit that is used as supplement for complementary MOS circuits.
- a. Transmission Gates
 - b. **Pesudo-Nmos**
 - c. Both
 - d. None
60. The technique to increase number of devices per chip is called _____

ANS: Level of Integration