Bindu Prasad C S

Design and Verification Engineer

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CAREER OBJECTIVE

Electrical and Electronics Engineering graduate with a passion for solving challenging problems and a deep interest in VLSI design. Seeking a challenging role in the field of VLSI that leverages my strong work ethic, punctuality, and dedication to achieving organizational goals. Committed to putting forth my best effort to contribute to cutting-edge projects, drive innovation, and excel in a dynamic team environment.

PROFESSIONAL TRAINING

- **Advanced VLSI Design and Verification Course** **(Jan-2023 to Present)**
  Maven Silicon VLSI Training Center, Bangalore.

EXPERIENCE

- **Lead Procurement Engineer** **(Sep-2022 - May 2023)**
  (Tata Power Solar Systems Limited)
  - Accountable for procuring raw materials for Solar PV Modules and cells.
  - Implemented cost-saving strategies using innovative tools such as negotiation and diversifying sourcing options.

- **Graduation Engineer Trainee** **(Sep 2021 – Aug 2022)**
  (Tata Power Solar Systems Limited)
  - Oversaw the procurement of spares for a solar manufacturing plant.
  - Managed purchase order creation and collaborated with OEM's and other industry resource to resolve component-related issue.

ACADEMIC CREDENTIALS

Qualification	College Name	Board/University	Year of Passing	Result
BE in Electrical and Electronics Engineering	R V College of Engineering, Bangalore	Visvesvaraya Technological University, Belagavi	2021	7.75 CGPA
PUC	Sri Swamy Vivekananda PU College, Turuvekere	Department of Pre-University Education, Karnataka	2017	92.33%
SSLC	Sri Someshwara High School, Dombaranahalli	Karnataka Secondary Education Examination Board	2015	91.84%

TOOLS AND TECHNICAL SKILLS

HDL: Verilog
HVL: System Verilog
Verification Methodology: Constraint Random Coverage Driven Verification, Assertion Based Verification
TB Methodology: UVM
Protocols: AXI, AHB, UART, I2C, SPI
EDA Tools: Mentor Graphics – Questasim, Quartus Prime, Xilinx-Vivado, Synopsys VCS
Programming Skills: C [Datatype | Array | Pointers | Memory Allocation | Lists | Queues and Stacks | Data Structure | Functions]
C++ [Good knowledge of OOP's Concepts | Polymorphism | Inheritance]
Operating System: Linux
Script Language: Perl Scripting
Core Skills: RTL Coding using Synthesizable constructs of Verilog, FSM Based Design Simulation, CMOS Fundamentals, Code Coverage, Functional Coverage, Static Timing Analysis, Assertion based verification using System Verilog Assertions.

PROJECTS

- **AHB2APB Bridge IP Core Verification**
  - **HVL:** System Verilog
  - **TB Methodology:** UVM
  - **EDA Tool:** Synopsys VCS
  - **Description:** The AHB to APB bridge is an AHB slave which works as an interface between the high speed AHB and the low performance APB buses.

- **Router 1X3 – RTL Design and Verification**
  - **HDL:** Verilog
  - **HVL:** System Verilog
  - **TB Methodology:** UVM
  - **EDA Tools:** Questasim and ISE
  - **Description:** The router accepts data packets through a single 8-bit port and directs them to one of the three output channels: channel 0, channel 1 and channel 2.

- **Dual Port RAM -RTL Design and Verification**
  - **HDL:** Verilog
  - **HVL:** System Verilog
  - **TB Methodology:** UVM
  - **EDA Tools:** Quartus Prime and Synopsys VCS
  - **Description:** Design and verify a Dual Port RAM module for efficient data read and write operations in embedded systems, enhancing memory access capabilities.

- **Simulation Study of 11KV Composite Insulator**
  - **Tools:** Ansys, Catia and HyperMesh
  - **Methodology:** Finite Element Method
  - **Material:** Silicon Insulator Rubber with Magnesium Oxide nanofiller
  - **Description:** Conducted an in-depth analysis of Electric Potential, Electric Field and Leakage Current of silicon polymer insulators. Utilized 3D simulation technique to investigate the impact of varying nanofiller compositions. The study encompassed air as a surrounding medium, accounting for environmental conditions such as pollution.

ACHIVEMENTS

In 2015, I was received the Kannada Madyama Award from the Government of Karnataka for attaining the highest marks in the SSLC examination at the Taluk Level.

STRENGTHS

- Self-motivated
- Rapid learner
- Forward thinking with a positive attitude
- Collaborative team player
- Adaptable and flexible
- Eager to acquire new knowledge
- Proficient in cooperation and coordination

HOBBIES

- Reading books
- Gardening
- Listening to music

DECLARATION

I affirm that all the information provided above is accurate and factual to the best of my knowledge. I take full responsibility for the accuracy of the aforementioned details.

Date: 23/10/2023
Place: Bangalore

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