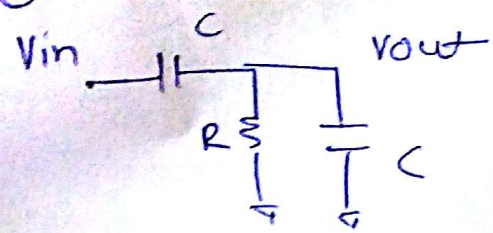
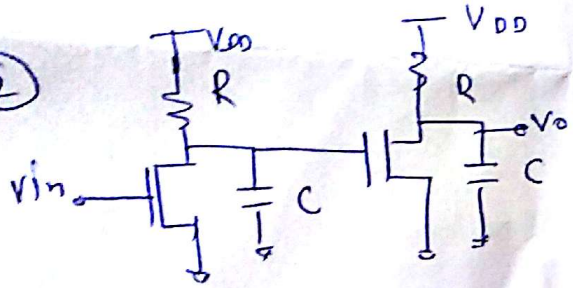
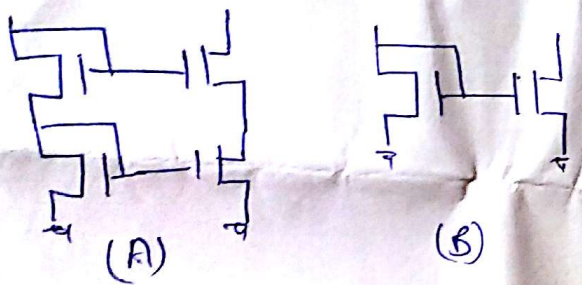
megachips test

① 

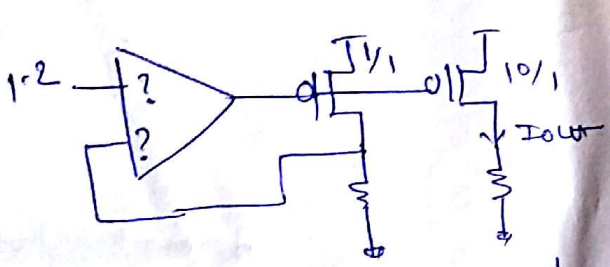
Plot Response

② 

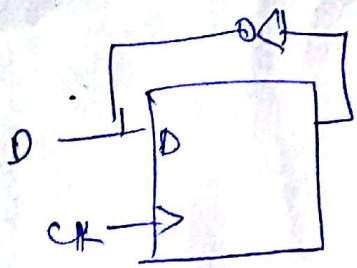
Plot Vo/Vin

③ 

which is better and why

④ 

find Polarity for stability and Iout

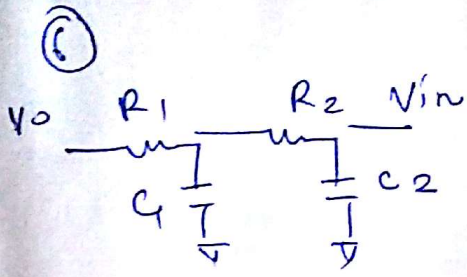
⑤ 

Find fmax ?

~~tout~~ tCLK-Q = 50p

tinv = 10p

tset = 50p thold = 50p

⑥ 

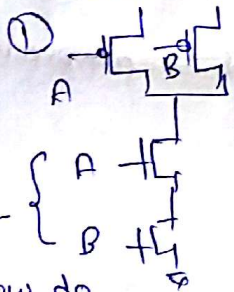
~~find~~ estimate delay

⑦ Stablity margins

$$H(S) = \frac{100\,(S+10)}{(S+0.001)(S+1000)}$$

⑧

interview

① 

how do U order them for min delay

② why cascode is better than Single stage (5 reasons)

③ static comparators

④ folded cascode

⑤ Differential amp

⑥ Diff amp Vs two CS amp

⑦ Dynamic latch comp design & constraints

⑧ inverter as amplifier

⑨ Small signal model of inverter.

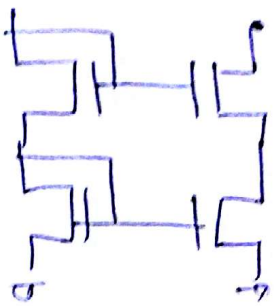
OTI Semi

interview

① ADC explain → (1 hour)

They asked every thing about the ADC

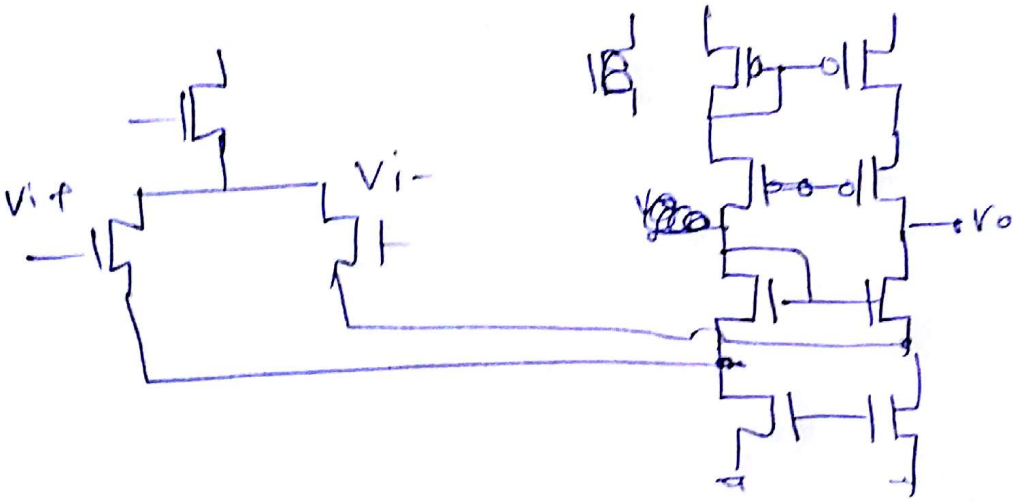
②



Vmin to operate this current mirror

benefits of using this over simple one

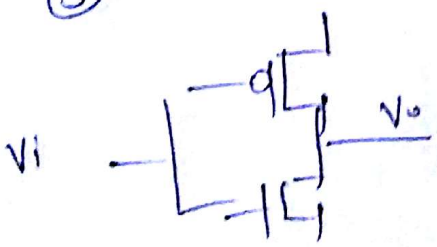
③ draw folded cascode op-amp so I draw

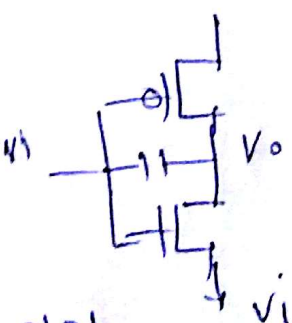


he asked me how will modify the PM and SR.

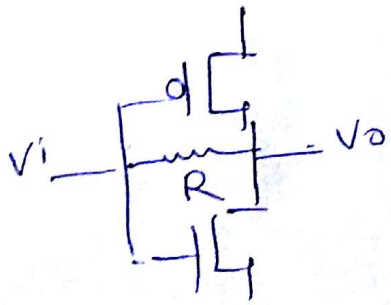
④ o/p Unar of mos and explain. (r_o)

⑤ inverter as an amplifier





plot vi/vo

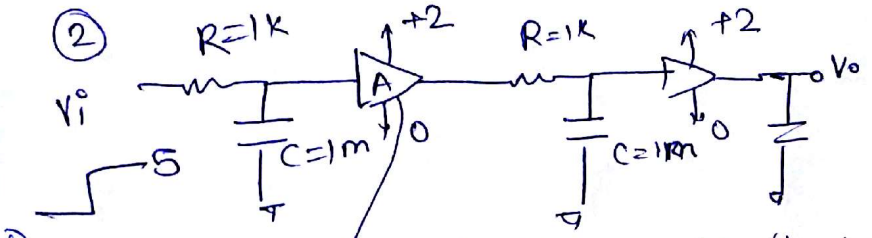


Texas instruments

Written test

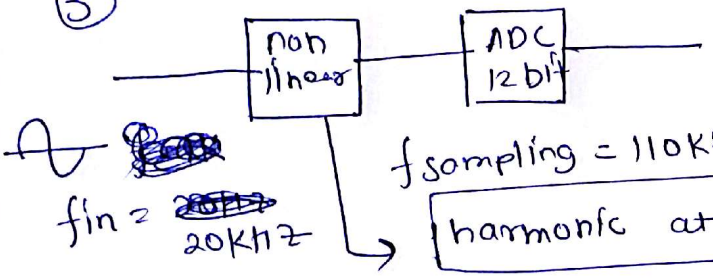
① pm and gm

$$H(S) = \frac{100(S+10)}{(S+0.001)(S+1000)}$$

② 

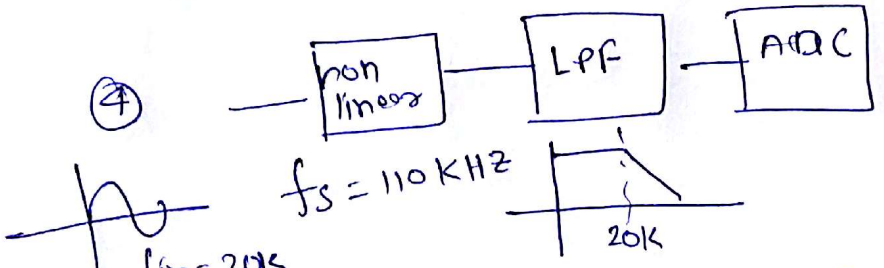
how much time will it take to reach Vo to 2 V

unity gain butter

③ 

harmonic at 30K (60dbm) and 80K (50 dBm)

what is the 2nd largest harmonic at which freqm

④ 

Now calculate 2nd largest harmonic.

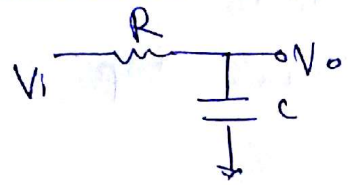
⑤ i don't remember other questions but they were difficult like above.

apptitude was also time consuming (20 question)

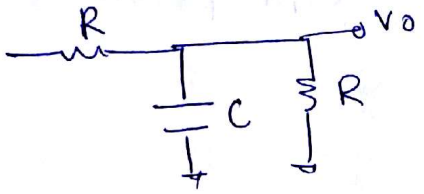
20+20 = 40 in (75 mins) So prepare hard for it.

TI interview

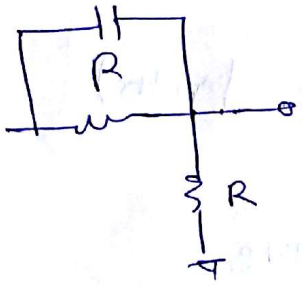
1st round

① 

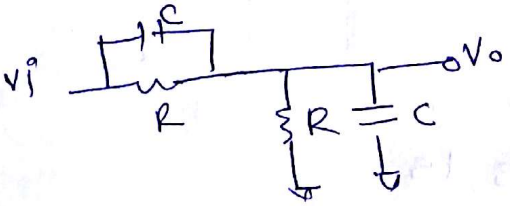
plot $\frac{V_o}{V_i}$

② 

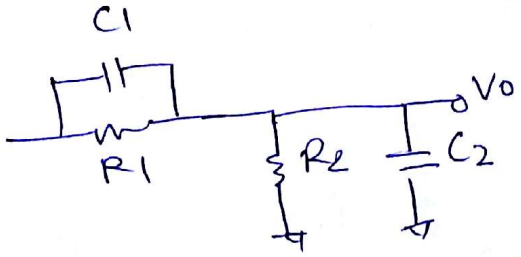
plot $\frac{V_o}{V_i}$ and explain

③ 

$\frac{V_o}{V_i}$

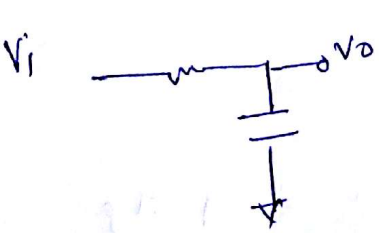
④ 

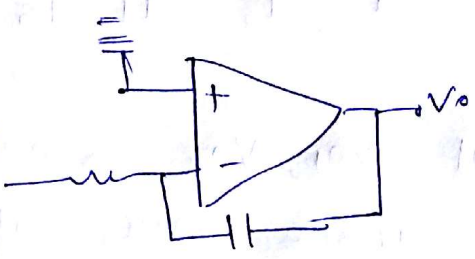
$\frac{V_o}{V_i}$ and explain

⑤ 

$\frac{V_o}{V_i}$ and explain

⑥ what is an integrator



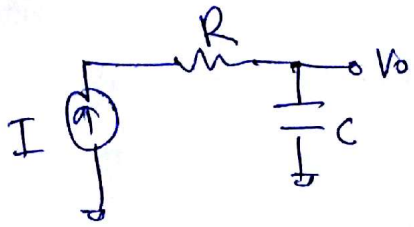


How they are different ?

will they work for every kind of signal ?

(integrate)

TI interview



plot Vo and where it will going to stop and why.

⇒ Repeat all the questions from previous page

2nd round → 1 st person

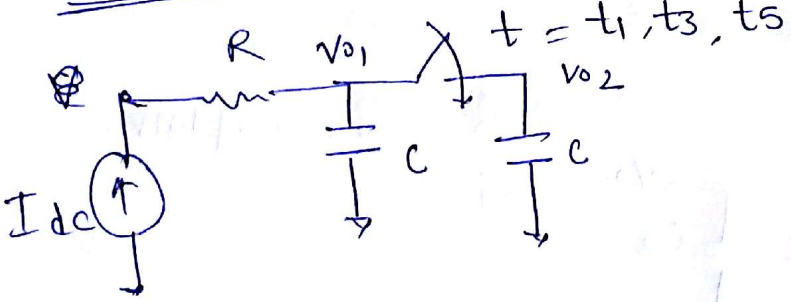
→ About thesis

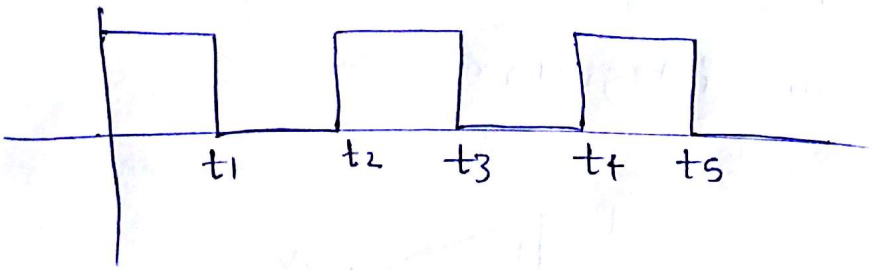
→ ~~plot~~ bottom plate sampling (in depth)
  → advantage & disadvantage

→ Some mwth Capacitor circuit to solve

} 1.5 hours (only thesis)

2nd person

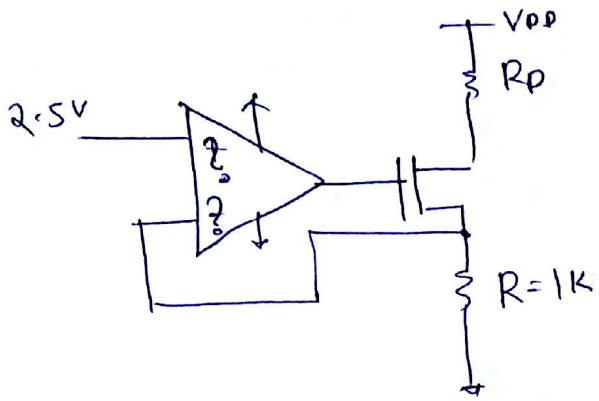




plot V_{o1}, V_{o2} → explain

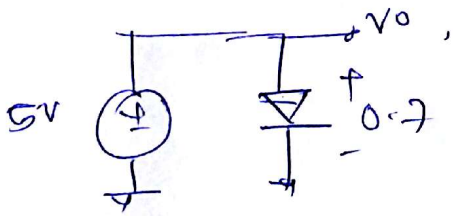
average value of V_{o2} ? and its significance.

TI interview

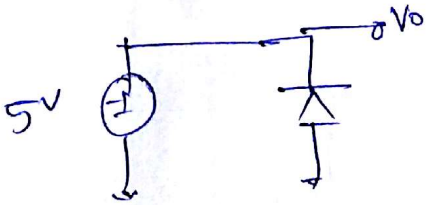


determine polarity for stable system and explain

→ what is op-amp
→ explain virtual short concept at transistor level as well as block level
→ From previous questions they asked lot of questions.



Vo = ?



Vo = ?