

CTS: Clock Tree Synthesis

By → Kianul

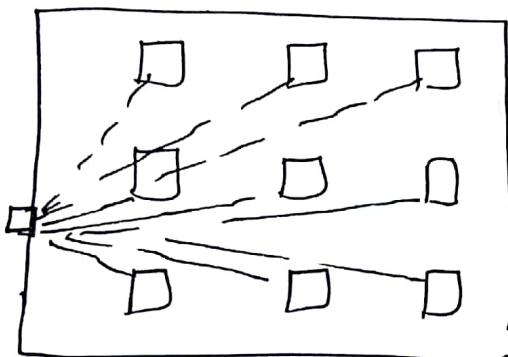
What is CTS?

Clock Tree synthesis is a process of balancing clock skew and minimizing insertion delay in order to meet timing, power requirement and other constraints.

CTS Goals

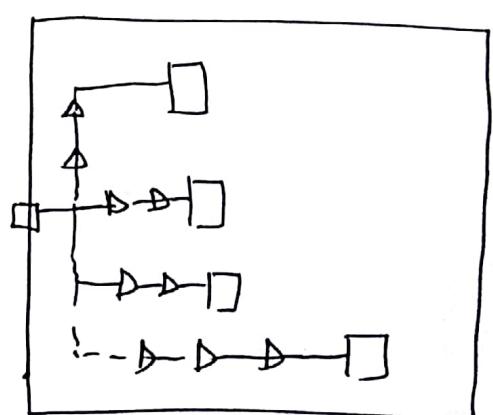
- ① Delivering clock to all seg. elements.
- ② Meet the clock tree Design rule Constraints (DRC) → what are DRCs?
 - ↳ Maximum transition delay
 - ↳ Max load capacitance
 - ↳ Max. fanout!
- ③ Meet the clock tree targets:
 - ↳ Max skew
 - ↳ Min/Max insertion delay.

Before CTS



One clock port driving
a lot of flops.

After CTS



Design rule checking or checks (DRC) is the area of electronic design automation that determines whether the physical layout of a particular chip layout satisfies a series of recommended parameter called design rules.

Design rule checking is a major step during physical verification signoff; which also involves LVS (Layout Schematic) check, XOR checks, ERC (Electrical rule check) and antenna checks.

The three basic DRC checks are

- ① width
- ② space's
- ③ enclosure

A width rule specifies the min. width of any shape of design. A spacing rule specifies the min. space b/w two adjacent object.

→ DRC software takes as a I/p a layout in GDS-II Std. format & a list of rules

Ques: What are DRVs & How to fix?

Ans:

↳ Design Rule Violation in timing closure

One of the most imp. rule that we should obey is "NEVER LEAVE DRV TO BE FIXED AT THE LAST STAGE OF DESIGN CYCLE"

It is g so b/c usually DRVs which directly impact timing are proactively fixed by the designer but the ones which do not impact timing are often left till last phase of design cycle, since timing closure is the topmost priority job. At that time, ~~design~~ conversion could make DRVs fix quite diff.

★ The best approach to fix DRVs is through implementation tool b/c it ensures u need not to do manual work a lot.

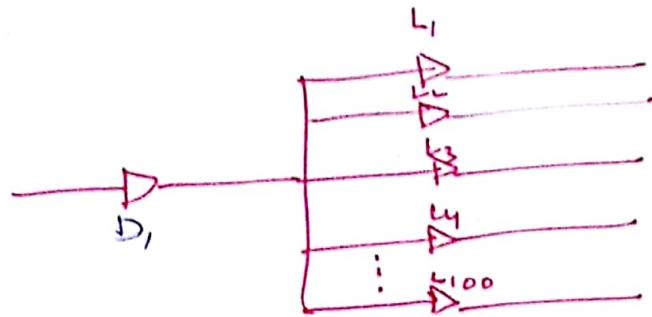
Design Rule Constraints:

1. Max. fanout: This constraint is present only for o/p pin. It is max no. of i/p pins that an o/p pin can drive. i.e. It denotes the load-driving capacity of that pin.

2. Max/ Min capacitance: This is the max/min cap. load that an o/p pin can drive. This comprises of both pin & interconnect net capacitance denotes the min. load value with which the cell in lib. is characterized for.

Cell delay is fn. of i/p transition and o/p load. So when transition \uparrow load delay \uparrow .

3. Max transition: Max time taken by net to charge its logic value. This is directly prop. to cell delay.



- * The o/p of D_1 fans out to 1000 cells. So the o/p net of D_1 sees 1000 fanout capacitances and hence the transition on that net will be bad. Thus the imp trans. for all L^* cell will be bad. So cell delays of L^* cells will be high. Since the transition after the o/p net of D_1 is bad, the net delay is also high. For cell D_1 , since the o/p load is high, cell delay is high here also.
- * These constraints come from the tech. file library. We can fight them through user defined constraints. Out of the design rule constraint; a synthesis tool gives priority to max. transition constraint.
- * Max transition is the most imp. one among these. Usually clock nets should have min. transition values. Trans violations can be fixed by upsizing the drivers; or decreasing the spacing b/w cells, shortening wire length or by buffering.
- * Max cap can be fixed by ↑ the drive strength of the driver cell.
- * Max fanout violation can be fixed by ↑ the drive strength of the driver cell. It can be fixed by buffering.

 If trans & max cap and timing is met, this is not a must fix.

Is the Design Ready for CTS? (Sanity Test) ③

- ① check_physical_design - stage pre_clock_opt.
↳ It will check
 - * Design is placed
 - * Clock have been defined
 - * Clock roots are not on Hierarchical pins. (what it is ??)
- ② Check_clock-tree
↳ It will check & warns if
 - * A clock source pin is on hierarchical pin
 - * A ~~master~~ pin generated clock with improper master & clock.
 - * Multiple clocks per registers.

Where does a clock Tree Begin & End?

Clock Tree begins at SDC-defined clock source:

create_clock

& it ends at "sinks" These are:

- ① Stop pins → (flop pins)
- ② float pins
- ③ Exclude pins (aka ignore pins)
↳ (Don't touch an ignore no timing analysis.)

Specifying clock tree exceptions

To define clock tree exceptions, use the `set_clock_tree_exception` command or choose `Clock > Set Clock Tree Exception` in the GUI. You can set clock tree exceptions on pins or hierarchical pins.

→ If you issue the `set_clock_tree_exceptions` command ~~multiple~~ multiple time on some pin; the pin keeps highest priority.

- ↑ ① Nonstop pin
- ② Exclude pin (if pins of seg. cells which are not int)
- ③ Float pin (input pin of Macros or Cells)
- ④ Stop pin. (stop)

Note:

- ① If your design contains sequential cells with unconnected outputs, the clock pins of these cells are marked as implicit ignore pins. When you run CTS, these unloaded sequential cells are deleted from the design. As a result, at the end of CTS, you no longer see these implicit ignore pins. To prevent the removal of these sequential cells, set the Physical_delete_unloaded_sequential_cells variable to false before running ETS.

② If your design contain dangling nets. The CTS exception report will show false implicit ignore pins on these nets. If this happens, you can remove the false implicit ignore pins by saving your design & reopening it.

Exclude pins

These are clock tree endpoints that are excluded from clock tree timing calculations & optimizations. ICC uses exclude pins only in calculation & optimization for DRC. In addition to exclude pins inferred by ICC (the implicit exclude pins), ICC supports user defined (or explicit) exclude pin.

ClockSpec.tcl (specification)

(4)

- ① Target skew / insertion delays
- ② List of buffers & inverters you are going to use in design.
- ③ DRC constraints (clock trans / cap / fanout)

e.g.

```
{
    AutoCTS Root Pin SH1/I23/Z
    Exclude pin +XPU/CAM/C
    Max Delay 5 ns
    Min Delay 0 ns
    Buffer buf1 buf2 m2 del1
    Max Skew 50 ps
}
End
```

- ④ NDR (Non default rule for f routing)
- Diagram → It is already defined in tf but here we need to define if additional needed. & configure it.

1st define.

```
define_routing_rule my-route-rule
  - width {METAL3 0.4 METAL4 0.6 METAL5 0.8}
  - spacing {METAL3 0.5 METAL4 0.65 METAL5 0.65}
```

→ 2nd Configure

```
set_clock_tree_options -root CLK \
```

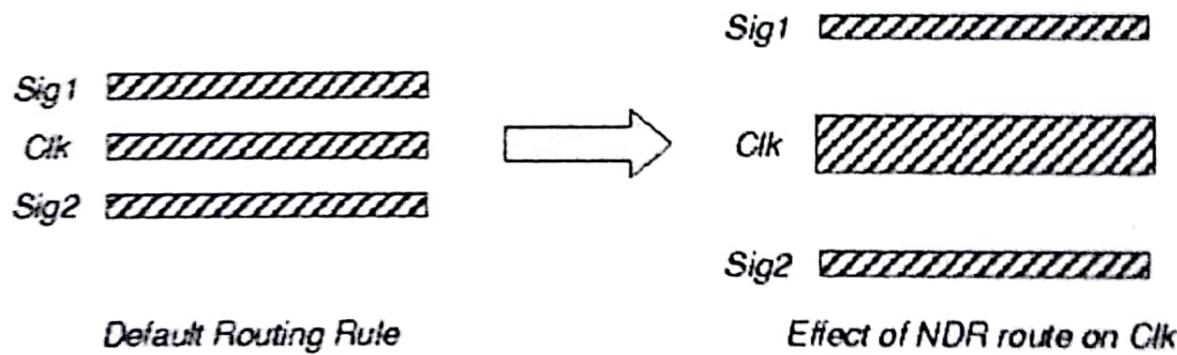
```
  - routing_rule my-route-rule \
```

```
  - layer_list "METAL3 METAL4 METAL5"
```

- ⑤ CTS Exceptions: pins.

- ⑥ Very Imp. type of Tree.

- IC Compiler can route clock nets using non-default routing (NDR) rules, e.g. double-spacing, double-width, shielding
- Non-default rules are often used to “harden” the clock, e.g. to make the clock routes less sensitive to cross-talk or electro-migration (EM) effects
- RC parasitics are different for NDR nets versus default routing nets → Affects timing
- This timing difference can and should be taken into account before actual routing, during placement



3-

Recommended flow

(5)

- ① place-opt
timing OK, congestion OK.
 - ② Set-clock-tree-options
 - ③ Set-clock-tree-exceptions
 - ④ remove-clock-uncertainty [all_clocks]
OR: adjust uncertainty to contain
only jitter, not skew component
 - ⑤ clock-opt —only_cts —no_clock_route
Analyse.
 - ⑥ Set-fix-hold [all_clocks]
 - ⑦ Clock-opt —only-psyn —optimize-dft —no_clocks
- Int. ↗ Analyzing CTS Results

Report-clock-tree

- Summary
- Setting.

* Reports Max global skew, Late/Early insertion delay, Number of levels in clock tree reference(Buffers), Clock DRC violations

↳ Show cts report ??

CTO (Clock tree Optimization)

Clock can be shielded so that noise is not coupled to other signals. But shielding ↑ area so it can be achieved by buffer sizing, gate sizing, buffer relocation, level adjustment & HFN synthesis.

Command:

optimize-clock-tree

- delay_injection [default = on]
- buffer_sizing []
- buffer_relocation []
- gate_sizing [default = off]
- gate_relocation [default_on]
- operating_condition min/max.

Or Please goto GUI, CTS option

Optimize clock tree & you can select Reg. options.

Types of Tree

- ① H-tree
- ② Balance tree
- ③ Spine tree
- ④ Distributed driven buffer tree.

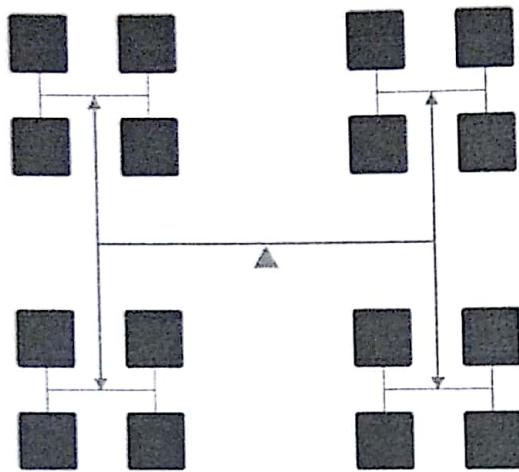


Figure 1 — H-tree, Because of the balanced construction, it is easy to reduce clock skew in the H-tree clock structure. A disadvantage to this approach is that the fixed clock plan makes it difficult to fix register placement. It is rigid in fine-tuning the clock tree.

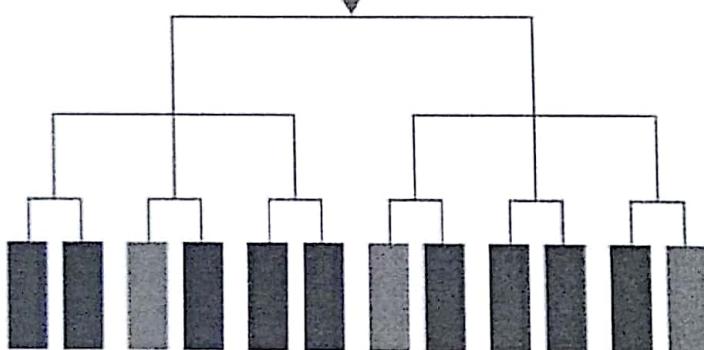


Figure 2 — Balanced tree makes it easy to adjust capacitance of the net to achieve the skew requirements. But the dummy cells used to balance the load increase area and power.

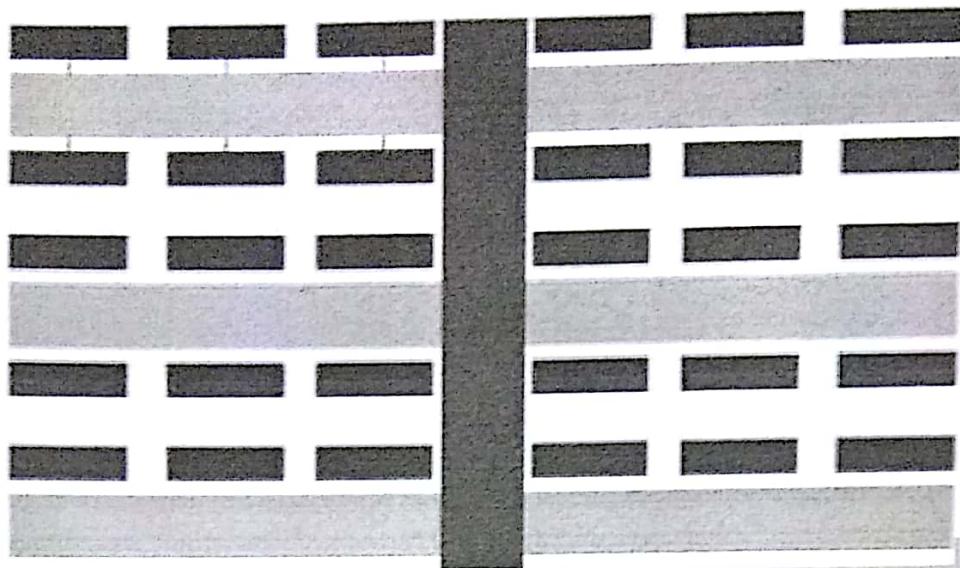


Figure 3 — The spine tree (Fish bone) arrangement makes it easy to reduce the skew. But it is heavily influenced by process parameters, and may have problems with phase delay.

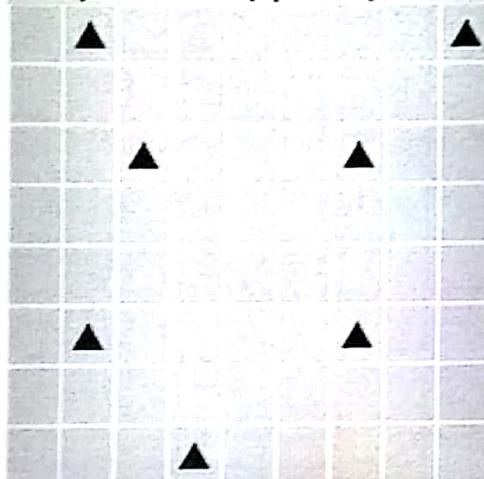


Figure 4 — Distributed driven buffer tree. Distributed buffers make it easy to reduce skew and power. Clock routing may not be an issue. However, since buffering is customized, it may be a less area efficient method.

Design Constraints

Clock constraints

Non-clock constraints

NOTE: Constraints are generally given by SDC file → generated by DC, it can also be generated by PT also.

Input-Output Constraints

Exceptions

- False Path
- Multicycle path

False path

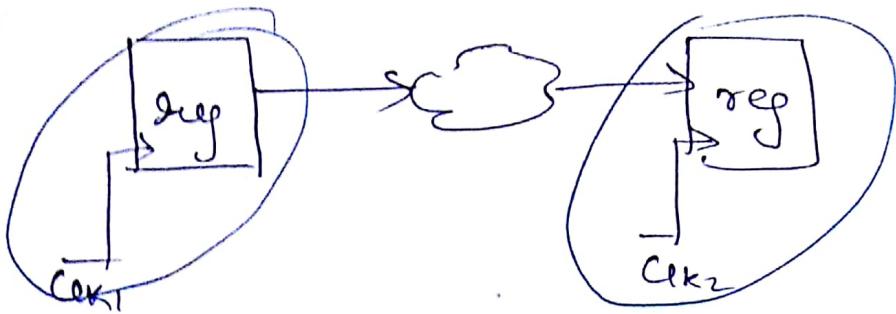
- ⇒ not a valid path for timing.
- ⇒ you need not worry to meet setup and hold constraints for this path.

e.g.

- ① All asynchronous paths.
- ② Static paths. (You need to decide)
- ③ Non-functional paths.

So if you do not mention the false path the tool will try to optimize these paths & may come up with using more area.

①

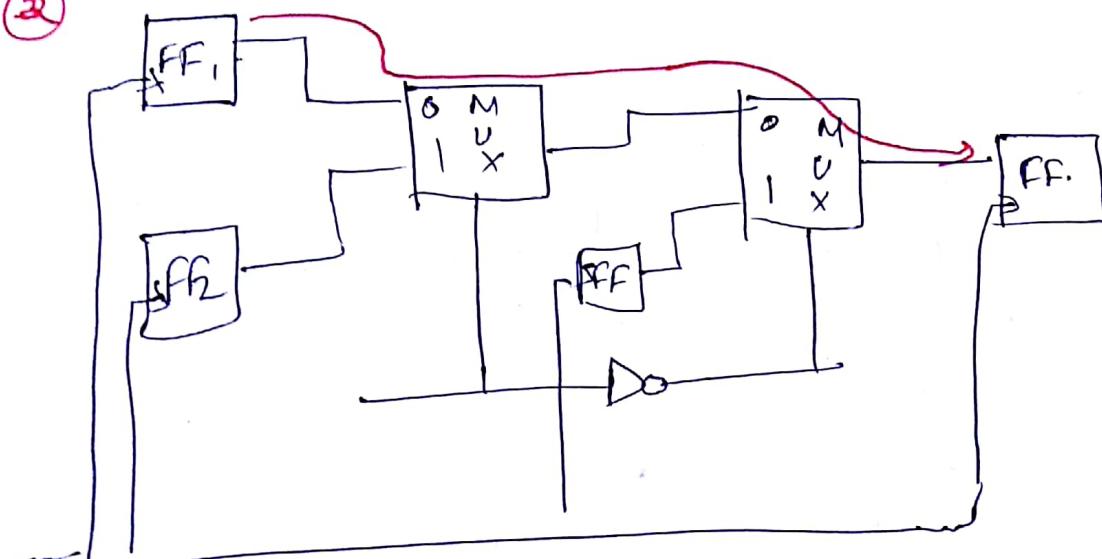


Both are independent of each other & both work in diff clock domain so if data is travelling from ① to ② so we can't say it will meet timing.

★ All asynchronous path you have to specify as false path.

↳ Set-disable-timing

②

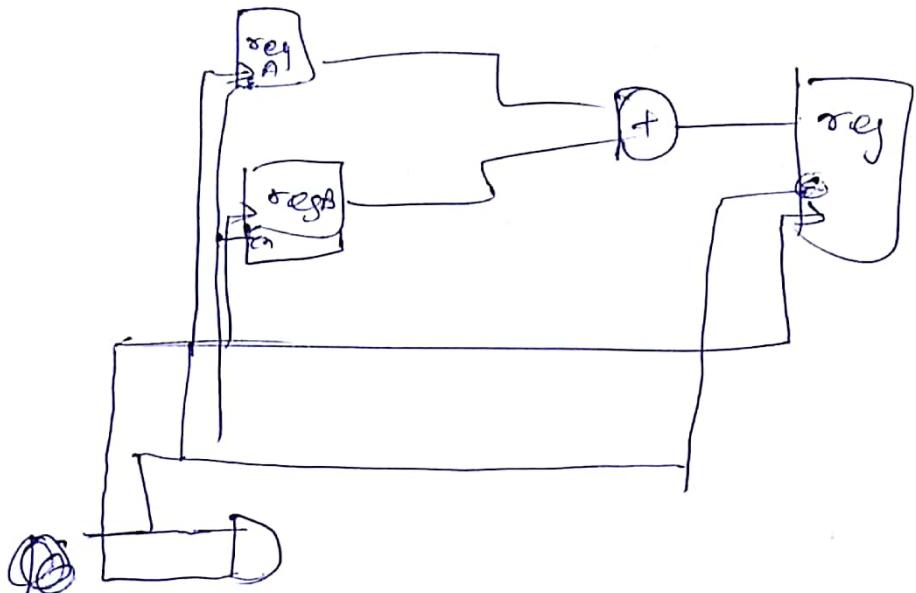


flk.

This path will occur at 00 only so it can never be possible.

↳ Set-false-path.

③ Multicycle Path \Rightarrow



Let say adder need 16ns to complete addition of 64 bit bus.

If you have total clock period of 4ns so you can't meet the requirement. So what you do you can use pipelining i.e. we can break into 4 delay of 4ns.

NDR (Non Default Rules)

NDR are mainly used in place & routing section of design flow. when they actually route the design.

The default routing guidelines for the router would be provided by Techlef or Techfile (ICC)
(concluded
in noisy.)

However when we are routing special nets especially clocks, we would like to provide more width & more spacing for them. Instead of default 1 unit width & 1 unit spacing specified in TechLEF, NDR will have double width, double spacing or triple width double spacing rules coded in them.

NDR's are mainly applied on clock nets. Clock nets are less sensitive than xtalk & EM.

- * NDR rules are
 - ① Double width
 - ② Double spacing
 - ③ Shielding (grounding)
- ① By applying double width we can avoid the EM
- ② By applying double spacing we can avoid xtalk.

adv:

- ① Help to avoid congestion at lower metal layer
- ② Help Pin accessibility of std cells.

DIFFERENT TYPE OF CELLS

DIFFERENT TYPE OF CELLS:

- STDCELLS:
 - Nothing But Base cells(Gates,flops).
- TAP CELLS:
 - Avoids Latch up Problem(Placing these cells with a particular distance).
 - Cells are physical-only cells that have power and ground pins and dont have signal pins.
 - Tap cells are well-tied cells that bias the silicon infrastructure of n-wells or p-wells.
 - They are traditionally used so that Vdd or Gnd are connected to substrate or n-well respectively.
 - This is to Help TIE Vdd and Gnd which results in lesser drift and prevention from latchup.
 - Required by some technology libraries to limit resistance between Power or Ground connections to well of the substrate.
- TIE CELLS :
 - It is used for preventing Damage of cells; Tie High cell(Gate One input is connected to Vdd, another input is connected to signal net);Tie low cells Gate one input is connected to Vss, another input is connected to signal .
 - Tie - high and Tie - low cells are used to connect the gate of the transistor to either Power and Ground.
 - In lower technology nodes, if the gate is connected to Power or Ground. The transistor might be turned "ON/OFF" due to Power or Ground Bounce.
 - These cells are part of the std cell library.
 - The cells which require Vdd(Typically constant signals tied to 1) connect to tie high cells.
 - The cells which require Vss/Vdd (Typically constant signals tied to 0) connect to tie low cells.
- END CAP CELLS:

✓ Jain

- To Know the end of the row, and At the edges endcap cells are placed to avoid the cells damages at the end of the row to avoid wrong laser wavelength for correct manufacturing.
 - You can add Endcap cells at both Ends of a cell row.
 - Endcap cells surrounding the core area features which serve as second poly to cells
 - placed at the edge of row.
 - The library cells do not have cell connectivity as they are only connected to Power and Ground rail,
 - Thus ensure that gaps do not occur between "WELL" and "IMPLANT LAYER" and to prevent the DRC violations by satisfying "WELL TIE - OFF" requirements for core rows we use End cap cells.
 - Usually adding the "Well Extension" for DRC correct designs.
 - End caps are a "POLY EXTENSION" to avoid drain source SHORT
-
- DECAP CELLS:
 - Charge Sharing; To avoid the Dynamic IR drop , charge stores in the cells and release the charge to Nets.
 - Decoupling capacitor cells , or Decap cells, are cells that have a capacitor placed.
 - Between the Power rail and Ground rail to Over come Dynamic voltage drop.
 - Dynamic IR Drop happens at the active edge of the clock at which a High currents is drawn from the Power Grid for a small Duration.
 - If the Power is far from a flop the chances are there that flop can go into Metastable State.
 - To overcome decaps are added , when current requirements is High this Decaps discharges and provide boost to the power grid.

 - FILLER CELLS:
 - Filler cells are used to connect the gaps between the cells after placement.
 - Filler cells are used to establish the continuity of the N-Well and the IMPLANT LAYERS on the standard cells rows, some of the cells also don't have the Bulk Connection (Substrate connection) Because of their small size (thin cells).
 - In those cases, the abutment of cells through inserting filler cells can connect those substrates of small cells to the Power/Ground nets.
 - i.e. those thin cells can use the Bulk connection of the other cells(this is one of the reason why you get stand alone LVS check failed on some cells)

 - ICG CELLS:
 - Clock gating cells ,to avoid Dynamic power Dissipation.
 - Register banks disabled during some clock cycles.

** Biuld*

- During idle modes, the clocks can be gated-off to save Dynamic power dissipation on flipflops.
 - Proper circuit is essential to achieve a gated clock state to prevent false glitches on the clock paths
- POWER GATING CELLS:
 - In Power gating to avoid static power Dissipation.
 - Power Gating Cells:
 - Power switches
 - Level Shifters
 - Retention registers
 - Isolation cells
 - Power controller
- PAD CELLS:
 - To Interface with outside Devices; Input to of Power, Clock, Pins are connected to pad cells and outside also.
- CORNER CELLS:
 - Corner Pads are used for Well Continuity.
 - To lift the chip.
- MACRO CELLS:
 - Memories.
 - The memory cells are called Macros.
 - To store Information using sequential elements takes up lot of area.
 - A single flipflop could take up 15 to 20 transistors to store one bit store the data efficiently and also do not occupy much space on the chip comparatively by using macros.
- SPARE CELLS:
 - Used at the ECO.
 - Spare cells are standard cells in a design that are not used by the netlist.
 - Placing the spare cells in your design provides a margin for correcting logical error that might be detected later in the design flow, or for adjusting the speed of your design.
 - Spare cells are used by the fix ECO command during ECO process.

**Sicaut*

Routing

(1)

Routing creates physical connections to all clock and signal pins through metal interconnects.

- * Routed paths must meet setup & hold timing, max cap/trans & clock skew req.
- * Metal traces must meet physical DRC req.

Pre-Route checks:

There should not be :

- ① Ideal Nets.
- ② High fanouts nets greater than certain limit (e.g. 500)

{ check_physical_design - stage pre-routing
all_ideal_nets
all_high_fanout_nets - threshold 50,
check_routability.
↳ 2t checks cell access pt; pin out of boundary, Pin design rule, blockages .

↳ blocked pins is also checked here.

Routing order :

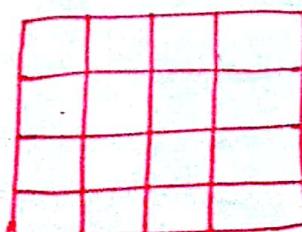
- ① ~~Power~~
- ② Clock
- ③ Signal

Def: It is the process of creating physical connections based on logical connectivity. Signal pins are connected by routing metal interconnects. Routed metal paths must meet timing, clock skew, max trans/cap req. & also physical DRC req.

The four steps of routing operations

- ① Global Routing.
 - ② Track Assignment
 - ③ Detail Routing
 - ④ Search & Repair
- } These all operations
is performed by
single command.
* "route-opt" *

→ GR: The first step of the global routing algorithm is to define routing regions or cells (i.e. a rectangular area with terminals on all side) and calculate their corresponding routing density. These routing regions are commonly known as Global routing Cells or GRC.



Global routing uses a graph to model the interconnection networks. The vertices of the graph denotes the std. cell ports. The edges of the graph corresponds to connections b/w two ports within routing cells and among routing cells themselves. The graph is constructed by means of region assignment.

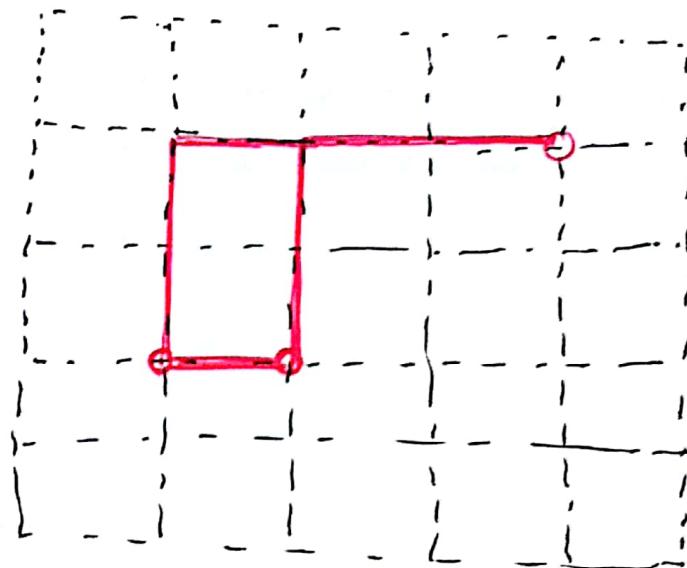


Fig: Complete graph wire length estimation.

Type of wire estimation Methods others are :-

- 1. Complete graph
- 2. Source to sink
- 3. Steiner minimal tree
- 4. Min. spanning tree
- 5. Hull perimeter
- 6. Min. chain.

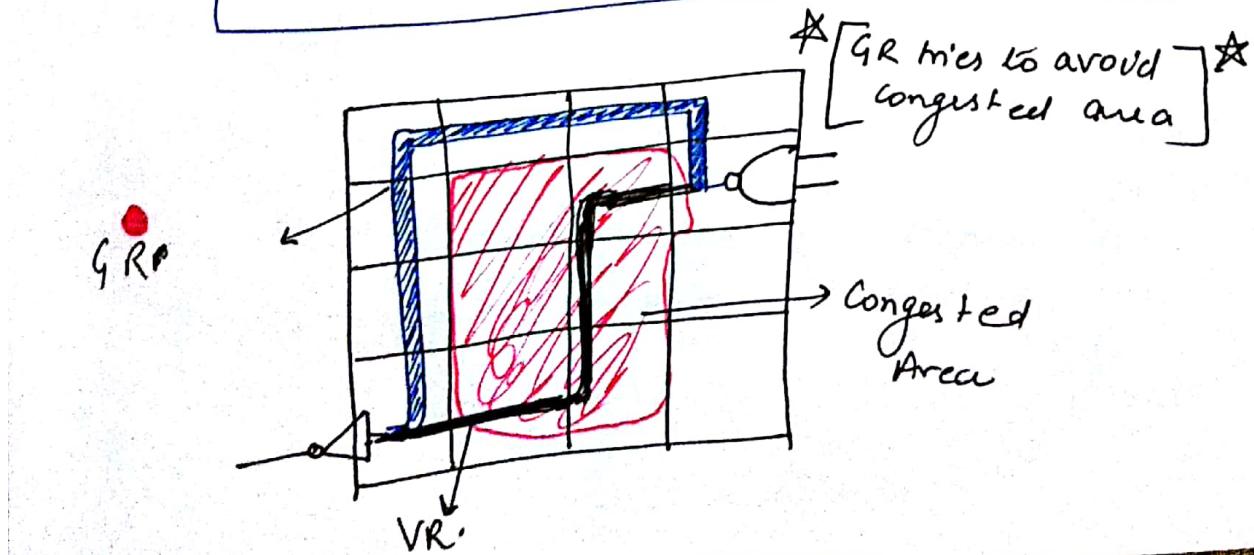
→ GR algorithm generate a non restricted route (i.e. not in detail route) for each net in the design & use some method of estimation of computing wire lengths & extract the polarities.

- The size of GRC is equal to height of avg. standard cell. GR determines whether each assigned GRC along a path has equal wire tracks for assigned nets through the edges of GRC. If there are not enough wire tracks GR assigns metal layers or GRCs a/c.
- Physically they don't exist.
- GR congestion is based on no. of tracks available in each GRC vs the no. of tracks need to assigned. (* For ASIC design to be routed completely without any design rule violation, this Ratio should be less than 1.)

So How does it diff from virtual Route??

→ pure assumption only.

★ VR will not add any via in b/w but GR will do.



(2)

TIA:

Assign each net to a specific track and actual metal traces are laid down by it.

- This is carried out based on GRC
- This is 1st phase of real physical connectivity.

- It tries to make long straight traces to avoid the number of Vias.
- DRC are not followed in TA.
- If track assignment can reduce the number of jumps & jogs in metal layer then this will generally improve timing (since each jump generally req. via), less use of via is generally a plus for reliability bcoz their failure rate is slightly higher than long straight metal trace then why further steps? ??

B/c it works for full chip at once & do not care abt physical DRC like.

- ① min spacing (wire)
- ② width (wire)
- ③ via rule.

* jogs: It uses same metal in horizontal & vertical direction to prevent vias.

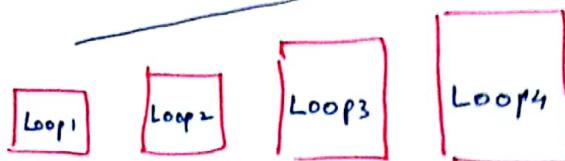
⑥

Detail Routing:

- It tries to fix all DRC violations after TIA using a fixed size small area known as Search box (sbox).
- Detail Routing does not work on entire chip at same time so it works by executing within the confines of a small area called as "Sboxes".
- Due to fixed size sboxes, detail route may not be able to clear all DRC violations.

Search & Repair:

S&R fixes remaining DRC violations through multiple loops using progressively larger sboxes.



NOTE: Even if the design is DRC clean after S&R, you must still run a sign-off DRC checker (Hercules) why??

Routing DRC is only a subset of full DRC & only partinfo is given in fp.

② ICC uses FRAM view, not the detail CEL view. ??

Used during P&R

The CEL view contains cells with full layout view (all layer). This view is used while taping out. i.e. writing complete stream in GDSII database which defines all processing layers & is handled off to fab for wafer implementation.

Few important topic

1] Fixing IR /congestion

- Spread macros → C
- Spread std cells → C
- Increase strap width → IR + C
- Increase Num of straps → IR
- Use proper blockages → C
- Use decap cells. → IR

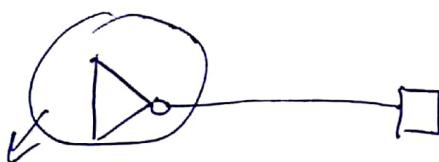
2]

Electron Migration

Due to high current flow in the metal atoms of the metal can displaced from its original place. When it happens in larger amount the metal can open or bulging of metal layer can happen. This effect is known as EM.

[Affects: Either shorts or open of the signal line or power line.]

e.g:-



X_{16}

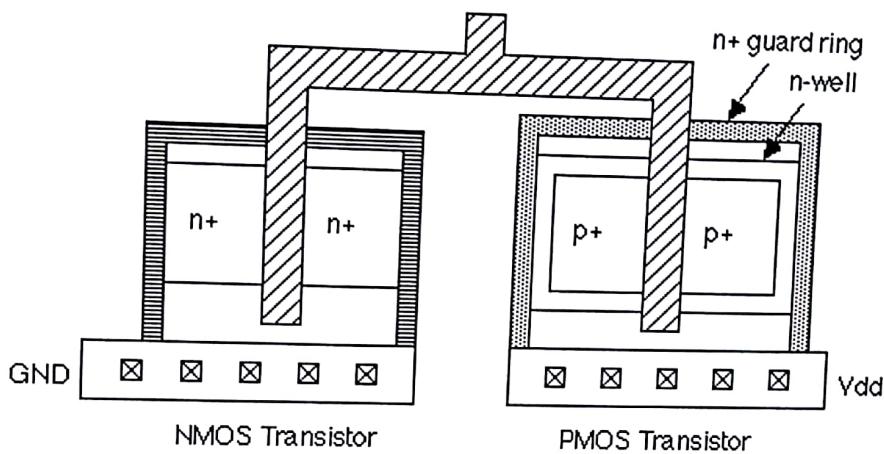
→ (since this cell is very big then it gives very high current density & this may lead to displacement of atom)

Fixes:

- ① Downsize driver ($X_{16} \rightarrow 2 \times X_8$)
- ② ↑ metal width
- ③ Add more vias
- ④ spread cells.

* Guard rings will reduce parasitic resistance. *

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CMOS transistors with guard rings

Systems Approaches

1. Make sure power supplies are off before plugging a board. A "hot plug in" of an unpowered circuit board or module may cause signal pins to see surge voltages greater than 0.7 V higher than Vdd, which rises more slowly to its peak value. When the chip comes up to full power, sections of it could be latched.
2. Carefully protect electrostatic protection devices associated with I/O pads with guard rings. Electrostatic discharge can trigger latchup. ESD enters the circuit through an I/O pad, where it is clamped to one of the rails by the ESD protection circuit. Devices in the protection circuit can inject minority carriers in the substrate or well, potentially triggering latchup.
3. Radiation, including x-rays, cosmic, or alpha rays, can generate electron-hole pairs as they penetrate the chip. These carriers can contribute to well or substrate currents.
4. Sudden transients on the power or ground bus, which may occur if large numbers of transistors switch simultaneously, can drive the circuit into latchup. Whether this is possible should be checked through simulation.

Antenna

Process antenna effect or "plasma induced gate oxide damage" is a manufacturing effect i.e. this is a type of failure that can occur solely at the manufacturing stage. This is a gate damage that can occur due to charge accumulation on metals and discharge to a gate through gate oxide.

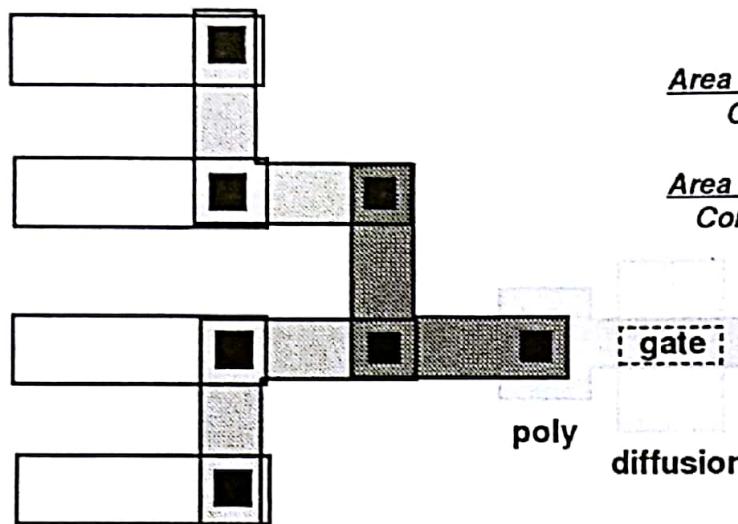
Let us see how this happens. In the manufacturing process, metals are built layer by layer i.e. metal 1 is deposited first, then all unwanted portion are etched away, with plasma etching. The metal geometries when they are ~~stationary~~ exposed to plasma can collect charge from it. Once metal 1 is completed then via 1 is built then metal 2 & so-on. So with each pass, stage metal geometries can build up static electricity. The larger the metal area that is exposed to the plasma, the more charge they can collect. If the charge collected is large enough to cause current to flow to gate, this can cause damage to gate oxide.

Antenna rules are normally expressed as an allowable ratio of metal area to gate area. Each foundry sets a maximum allowable antenna ratio for its processes; of the metal area - which is cumulative i.e. sum of ratios of all lower layer ~~interconnects~~ interconnects in addition to layer in check - is greater than allowable area, the physical verification tool flag error. For example, let's say max allowable antenna ratio for metal is 400. If the gate area is 1 sq. unit & if sum

metal area connecting to the gate is 500 sq.u.
There will be a process antenna violation.

Antenna Rules

- As total area (length) of wire increases during processing, the voltage stressing the gate oxide increases
- Antenna rules define acceptable total area of wires



Antenna Ratios:

Area of Metal Connected to Gate
Combined Area of Gate
Or
Area of Metal Connected to Gate
Combined Perimeter of Gate

7-7

The ASIC vendor will specify antenna design rules in terms of allowable ratios of antenna metal to gate oxide.

Basic Antenna rules are:

$$(\text{antenna-area}) / (\text{gate-area}) < (\text{max-antenna-ratio})$$

Gate-area:

Boolean AND (or intersection) of the 'poly' and the 'diffusion' layers
Recognized as the gate area of the transistors by essentially all foundries

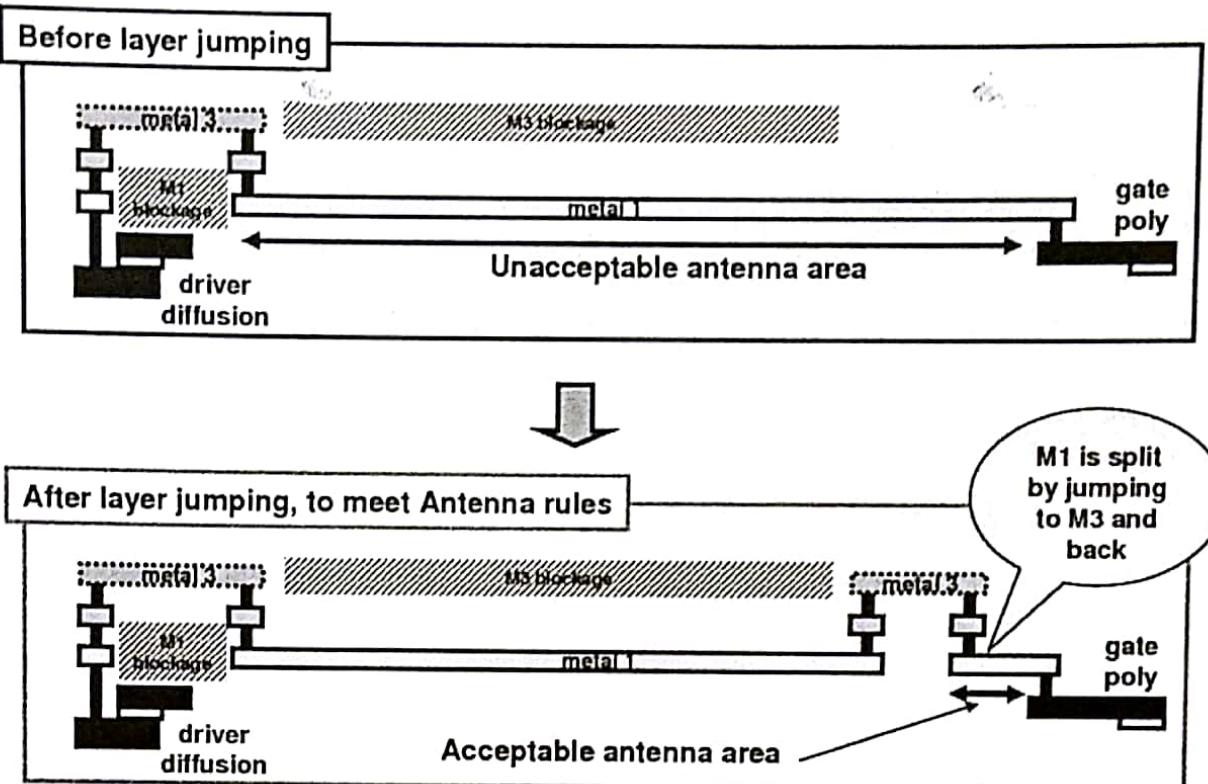
Antenna-area:

Amount of metal area attached to the input pin
Calculation method varies for different processes

Max-antenna-ratio:

Represents max allowed ratio of antenna area to gate area
Calculation method varies for different processes

Solution 1: Splitting Metal or Layer Jumping



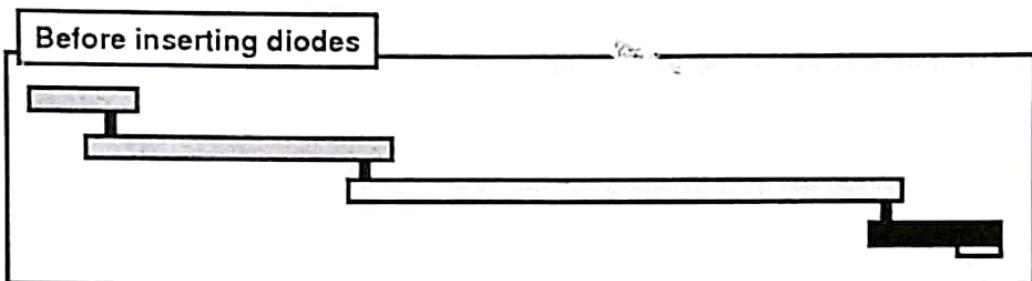
7-8

Until the top metal 3 link is in place, the metal 1 wire can generate large voltage gradients that may damage the gate oxide. This method of fixing antenna rule violations uses jumps in metal layers to keep the total length of lower level metal traces that are directly connected to polysilicon gates below maximum. Once the top metal 'link' is in place and the polysilicon gate is connected to its driver, it is relatively safe. The pn junction of the source/drain of the driver will help shunt large voltage swings – it acts like a reverse-biased diode.

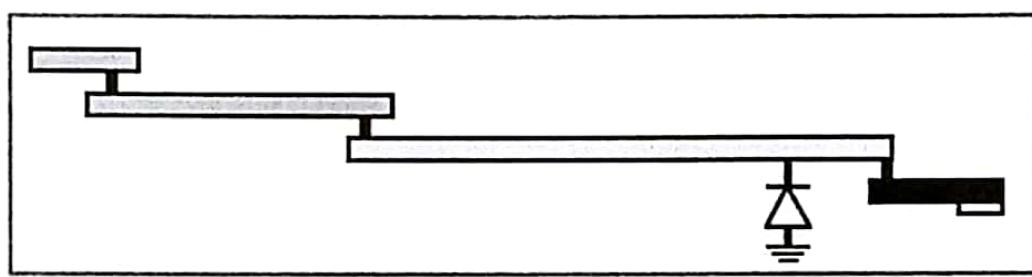
This is the preferred method for fixing antenna problems. Antenna violations that cannot be fixed by this method must be provided with special shunting diodes. These diodes use up additional silicon placement and metal routing resources, which may be challenging – diode insertion is therefore the second choice, over layer jumping, to address antenna violations.

Run an Search and Repair to fix antenna violations. The search & repair engine will reroute antenna violators adding multiple jumps to the long traces.

Solution 2: Inserting Diodes



Diode Inhibits large voltage swings on metal tracks



7-9

If the antenna can not be fixed with metal jumping, add an antenna diode to shunt the voltage. The diode acts like the pn-junction of a driving gate to clamp the voltage swings on the metal. A special antenna diode CEL is usually provided by the fab or ASIC vendor.

During normal operation, these diodes are always reverse biased and have modest effects on signal performance.

~~★ Start~~

Once you are done with Routing your main task is now to generate .spef. So what icc will do it will require (.tlat, .def, .sdc, .v, .lib, .tf, .lef) & internally StarRC session would be triggered & it will dump the spef. This spef will be i/p to sign off tool & you will proceed for STA.

for STA one catch is there any DUA can work in diff modes & diff corners & a PD engineer should fix any timing issue in all modes & all corners.

(MMMC/MCML)

→ what is →

★ **Mode**: A mode is defined by set of clocks, supply voltage, timing constraints and libraries. It can have annotation data, such as SDF or parasitics files.

{ Back annotation
* }

Many chips have multiple modes such as functional mode, testmode, sleep mode etc.

Func	Test
e.g. 1. High speed 2. Slow 3. Sleep 4. debug.	e.g. 1. Scan capture 2. Scan stuff 3. BIST 4. JTAG. * No need for P.D engineer?



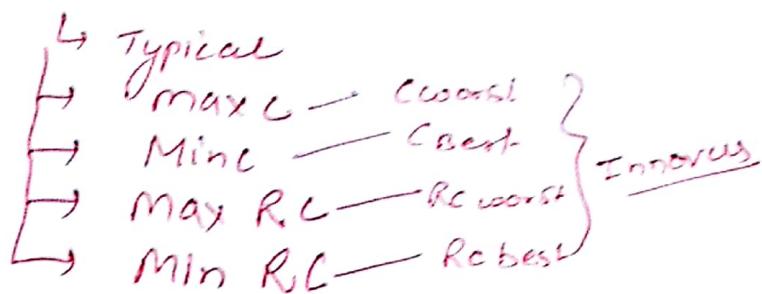
What's a corner?

A corner is defined as a set of libraries characterized for process, voltage and temperature variations.

Corners are not dependent on functional settings; they are meant to capture variations in the manufacturing process, along with expected variations in the voltage & temperature of the environment in which chip will operate.

Some other corners are there which are governed by variation in metal width & metal etching in the manufacturing process & these are called parasitic.

Interconnects Corners .



Now why it is very complicated to choose in all MMMC?

Cornr	{ P → Best, SS, FF, SF, PS, Typical — 5 V → Best, worst, typical —————— 3 T → Beat worst, typical —————— 3
Par Cornr	{ Typical 2 Max C Min C Max RLC Min RLC } 5

$$\text{total} = 5 \times 5 \times 3 \times 3 \\ = 225$$

These are only corners now think abt diff modes. So Ans you got right?



Ques: for (Setup/H₁) which PVT corner & also parasitic interconnect corner we should consider?

- I/O pins delay
- O/I pins delay
- Is there any false path?
- Is there any multi cycle path?

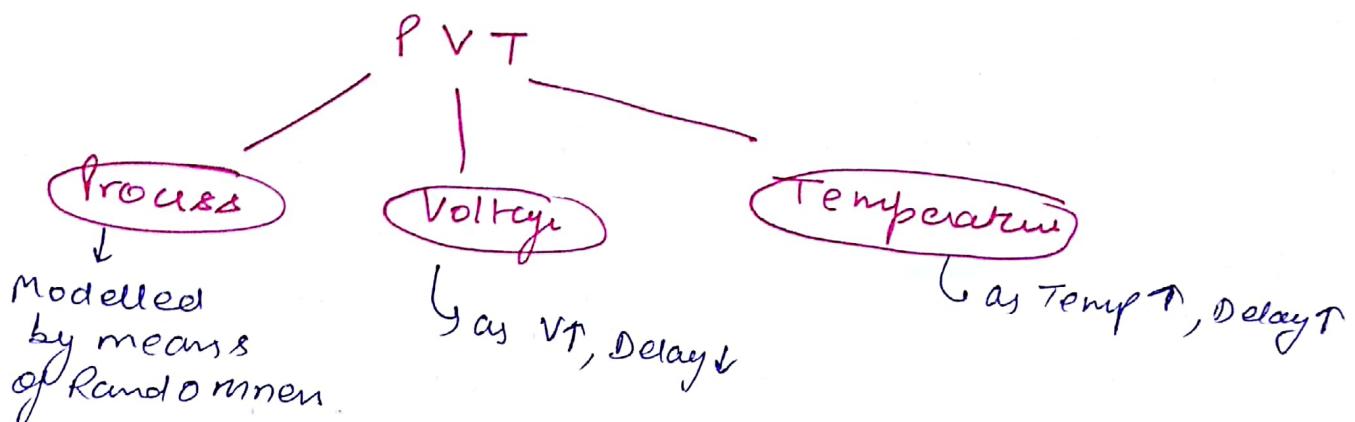
This is called design constraints. Typically mostly you have applied in synthesis itself. You can use write-adc will generate a file called Synopsys Design constraints; then you can use that file and add one more constraint needed.

③ Parasitic, those RC values that info you have to give this is called SPEF (Standard Parasitic Exchange format.)

④ You can close binary by SDF format (Standard delay format) (It is faster than SPEF but SPEF is more accurate).

⑤ O/P is timing report.

Analysis



Slow corner	Typical corner	Fast corner
{ 1.6 V, 125 °C ↳ for delay 70 °C	1.8 V, 27 °C	2 V, 0 °C ↳ ground - 90 °C

* More prone to have Setup violations.

* More prone to have Hold violation.

* Close timing in all corners.

Design Constraints

Clock Constraints

Non-clock constraints

NOTE: Constraints are generally given by SDC file → generated by DC, it can also be generated by PT also.

Input-Output Constraints

Exceptions

- False Path
- Multicycle path

False path

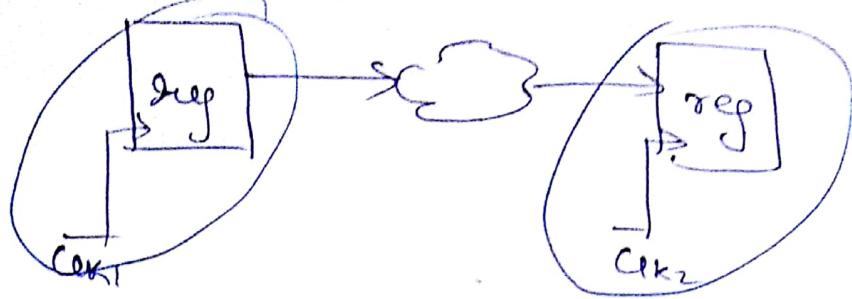
- ⇒ not a valid path for timing.
- ⇒ you need not worry to meet setup and hold constraints for this path.

e.g.

- ① All asynchronous paths.
- ② Static paths. (You need to decide)
- ③ Non-functional paths.

So if you do not mention the false path the tool will try to optimize these paths & may come up with using more area.

①

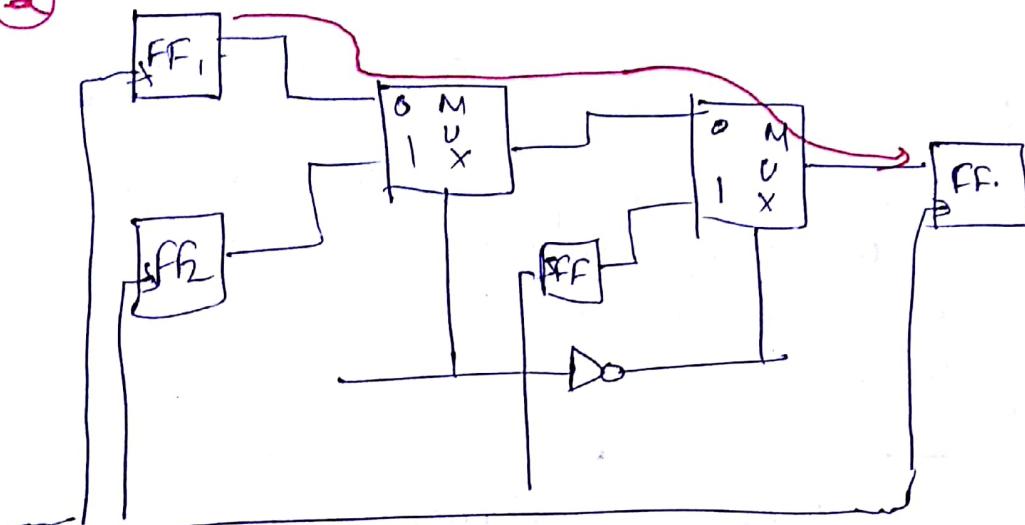


Both are independent of each other & both work in diff clock domain so if data is travelling from ① to ② so we can't say it will meet timing.

★ All asynchronous path you have to specify as false path.

↳ Set-disable-timing

②

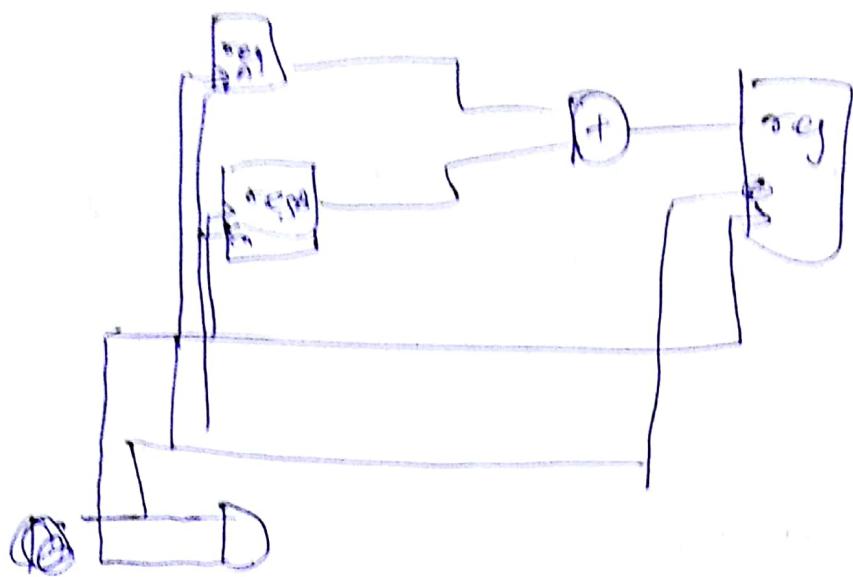


tk.

This path will occur at 00 only so it can never be possible.

↳ Set-false-path.

3) Multiplexer Path



Let say adder need 16ns to complete addition of 64 bit bus.

If you have total clock period of 4ns so you can't meet the req., so what you do you can use pipelining i.e. we can break into 4 delay of 4ns.

Clock Uncertainty

Before CTS

= Clock Skew

+ Clock jitter

+ Margin.

After CTS

= Clock jitter

+ Margin



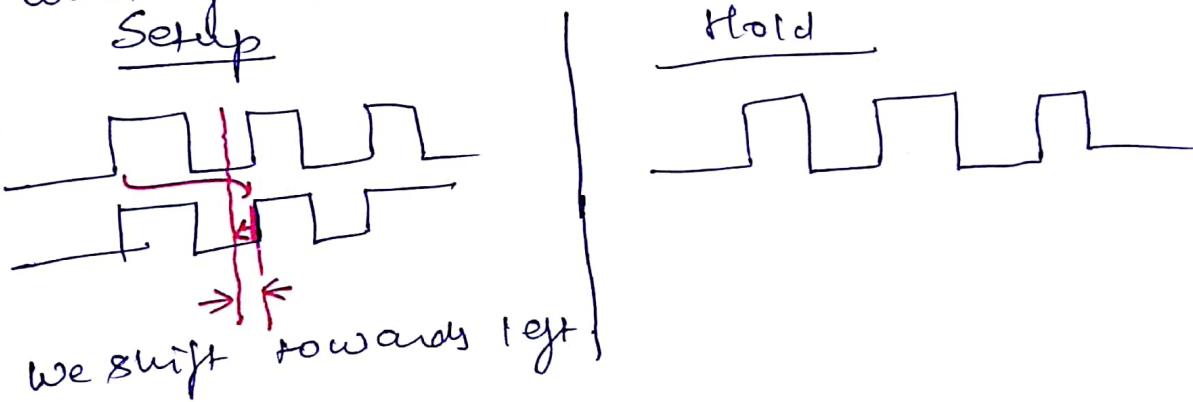
We make clock like that but since there is a

a lot of variations in chip b/c of Randomness
we can give jitter as 10%. And to keep safe we
take some margin.

★ Max analysis - Setup analysis.
[Slowest corner]

★ Min analysis - Hold analysis
[Fast corner]

★ Clock uncertainty has to be used more
worst for each case.



On chip variation

④ temperature across a chip is variable. i.e. if can be off for off path so we will take worst case.

for setup

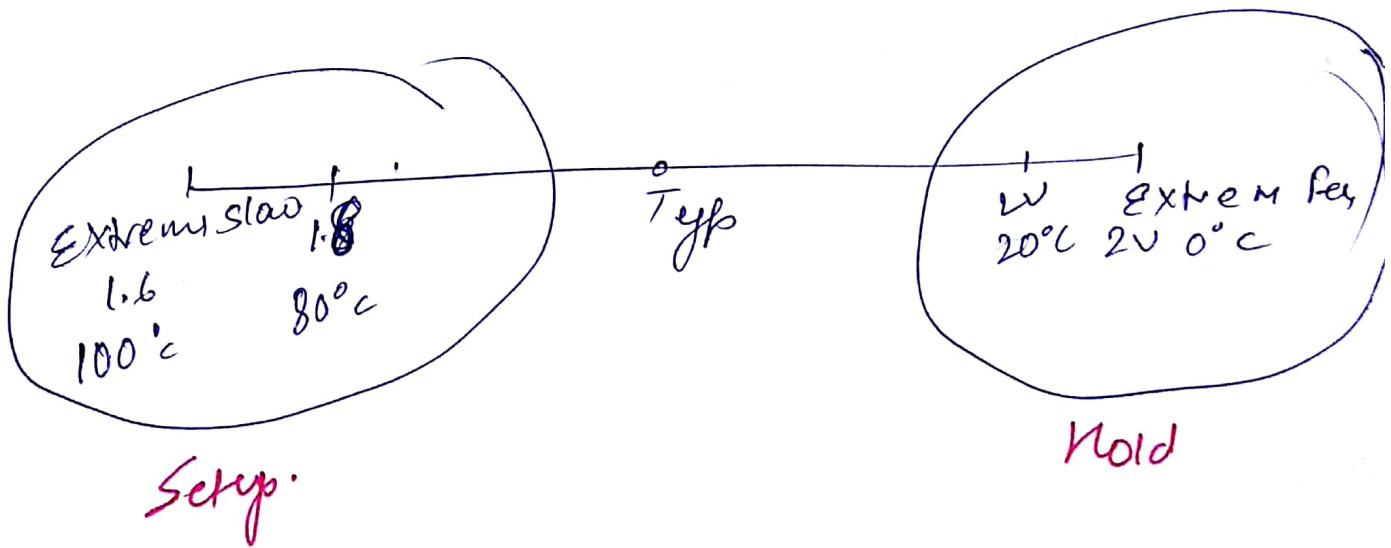
(data path) max
(clock path) min.

for hold

(data) min
(clock) max.

④ Definitely Temp diff Across chip can't be around 100°C , so extreme max & min corners are more pessimistic

④ so library define our specific New corner



[Created By Design Compiler write_sdc]

- ① create_clock - period 48s - waveform {0, 2.425} [get_ports \$clock]
- ② Create - clock - transition - rise 0.04 [get_clocks \$clock]
- ③ ← → - fall ← →
- ④ Set_clock_uncertainty 0.485 - setup [get_clocks \$clock]
- ⑤ ← → - hold ← →
- ⑥ Set_clock_latency 0.4s [get_clocks \$clock]
- ⑦ ← → - source ← →

In PT, the set_operating_conditions command specifies the operating conditions for Analysis.

There are three Analysis mode:-

- ① Single
- ② best_case / worst_case
- ③ on-chip variation

Single

PT uses a single set of delay parameters for the whole ckt; based on PVT conditions

best_case / worst_case

PT simultaneously check the ckt for two extreme operating conditions

For ★ Setup - Max delay in all path
Hold - Min delay in all path

On-chip variation

PT performs a conservative analysis that allows both min and max. delays to apply to diff. paths at the same time.

For, setup = Max delay in launch & data
Min delay in capture clock path.

Hold = Min delay for launch clock path and
data
Max delay for capture clock.

By default, PT performs analysis under one set of operating conditions at a time
(Single operating mode.
Best case commercial.)

You can enable min & max analysis :-
Set-operating-conditions - min BCOM, -max WCON

On Chip Variation Analysis

Set-operating-conditions - analysis-type On-chip-variation - min MIN - max MAX.

Report-timing - delay-type min
Report-timing - delay-type max.

* Derating Factors *

You can have PT adjust min. delays and max delays by specified factors to model the effect of operating conditions. The adjustment of calculated delays is called derating.

The set-timing-derate command specifies the adjustment factors and the scope of the design to be affected by derating. For example;

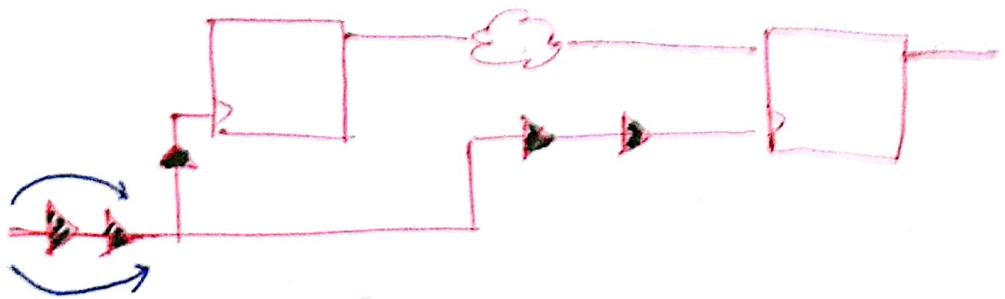
Set-timing-derate - early-cell-delay 0.9
Set-timing-derate - late-cell-delay 1.2

The first of these commands cause all early delays to be decreased by 10%, such as capture clock path in setup check.

The second command causes all late (longest paths) delays to be ↑ by 20%, such as launch clock path and the data path in a setup check.

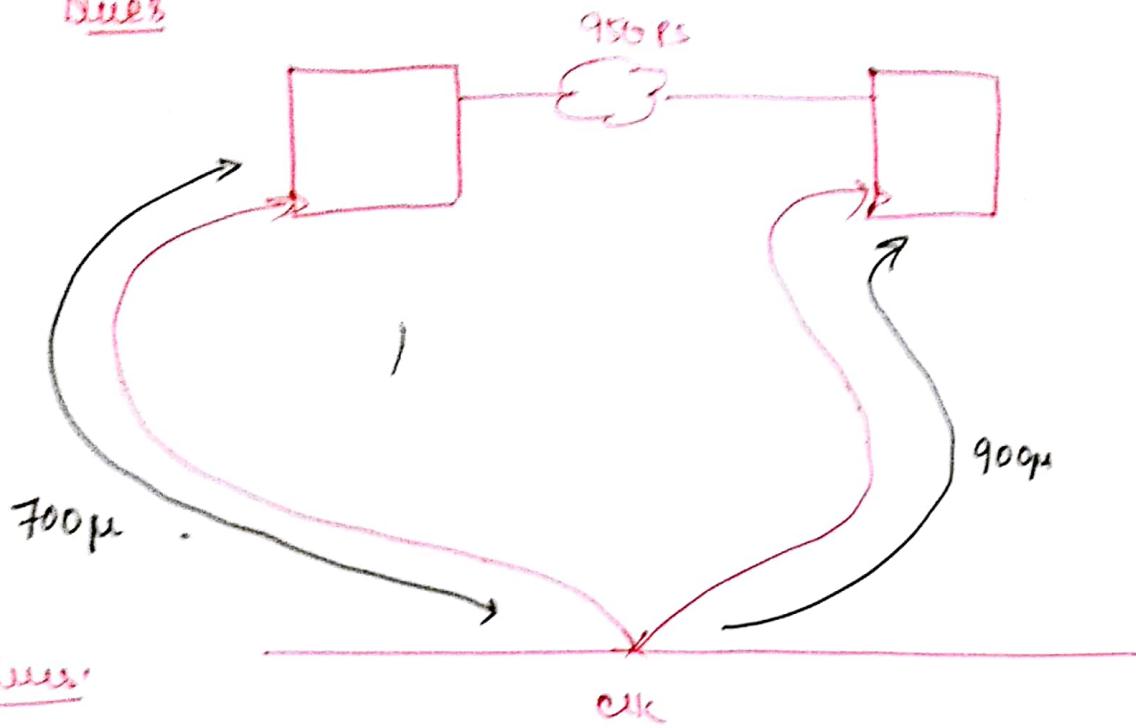
Clock Reconvergence Permission Removal (CRPR)

It is an accuracy limitation that occurs when two different clock paths particularly partially share a common path segment and the shared segment is assumed to have a min. delay of one path and a max. delay of other path. Automated correction of this inaccuracy is called CRPR.



Buffer delay is 10 & duration % is 10%
 Effect seen.
 In SAT →
 { RT →

Buses



Buses

$$V_{k,q} = 5$$

$$\text{Setup} = 3$$

$$\text{Hold} = 2$$

$$\text{Time period} = 1000$$

One buffer can drive 50μ & delay of ~~100ps~~

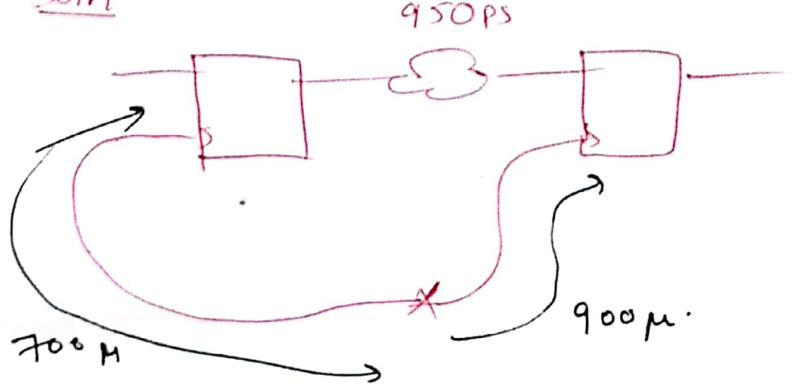
1 buffer is $= 50 \text{ps}$ in $SS_{\text{op}} = qv = 125 \mu$
its 25ps in $FF_{\text{op}} = 10 \mu$

derate % = 10%, 1st part without derate.

Analyse the circuit.



Soln



So, for Setup which corner ??

$$AT = \frac{700}{50} \times 50 + 5 + 950 + 3$$

$$= 700 + 5 + 950 + 3$$

$$= 1658$$

$$RT = \frac{900}{50} \times 50 + 1000$$

$$= 1900$$

If ques is asked
Calculate RT &
AT. Then

$$AT = 700 + 5 + 950$$

$$= 1655$$

$$RT = (900 + 1000) - 3$$

$$= 1897$$

$$\therefore \text{Setup slack} = (RT - AT)$$

$$\therefore \text{Setup slack} = (RT - AT) =$$

for Hold, which corner ??

$$AT = \frac{700}{50} \times 25 + 950 + 5$$

$$= 350 + 950 + 5 = 1305$$

$$RT = \frac{900}{50} \times 25 + (2)$$

$$= 452$$

$$\therefore \text{Hold slack} = (AT - RT) =$$

~~OCV analysis~~

Applying derate for setup \rightarrow

Applying derate for Hold \rightarrow

datapath: $50 + 50 \times 10\%$
capture: $50 - 50 \times 10\%$

data = $25 - 25 \times 10\%$
capt = $25 + 25 \times 10\%$

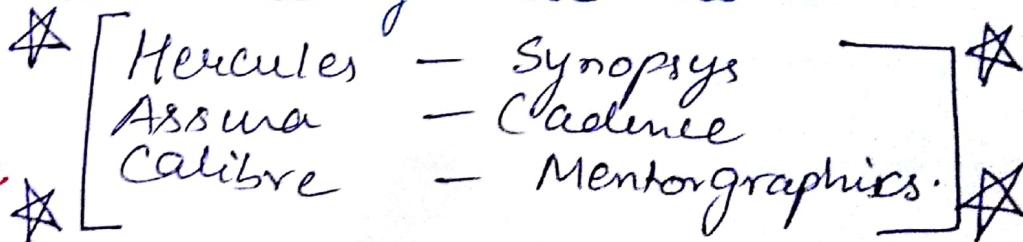
After Routing, your layout is complete. Now a number of checks are performed to verify that the drawn layout works as intended.

- (1) Physical Verification
- (2) equivalence checking
- (3) timing analysis.

④ Equivalence check will compare the netlist we started out with (pre-layout / synthesis netlist) to the netlist written out by the tool after PnR.

Physical Verification will verify that the post-layout netlist and layout are equivalent. i.e. all connection specified in the netlist is present in the layout.

Physical Verification: After routing your PnR tool should give you zero DRC/LVS violations. However PnR tool deals with abstract like FRCM or LEF views. We use dedicated physical verification tools for signoff LVS and DRC checks. Some of these are:



DRC checks determine if the layout satisfies a set of rules required for manufacturing. The most common of these are spacing rules b/w metals, min. width rules, via rules etc.

There will also be specific rules pertaining to your technology. An I/p to the design rule tool is a "design rule file" (called a sunset by Synopsys' Hercules).

The design rule ensures sufficient margins to correctly define the geometries without any connectivity issues due to proximity in semiconductor manufacturing processes, so as to ensure that most of the parts work properly.

The min. width rule exists for all mask layers, Spacing b/w same layers are also specified.

Spacing rule may change depending on the width of one or both of the layers as well.

There can be rules b/w two diff layer, and specific via density rules.

They will take the layout in any format.
e.g GDSII

② LVS (Layout versus schematic):

LVS is another major check in the physical verification stage. Here you are verifying that the layout you have created is functionally the same as the schematic/netlist of the design that you have correctly transferred into geometries your intent while creating the design. So all the connections should be proper and there shouldn't be any missing connections etc.

The LVS tool creates a layout netlist, by extracting the geometries. This layout netlist is compared with the schematic netlist. The tool may require some steps to create either of these netlists (e.g. natrah run in Synopsys).

If the two netlist match, we get an LVS clean result. Else the tool reports the mismatch and the components and location of the mismatch along with formal verification, which verifies if your pre-layout netlist matches the post-layout netlist, LVS verifies the correctness of the layout w.r.t. intended functionality.

Some of LVS errors are:

- ① Shorts: Wires that should not be connected are overlapping.
- ② Opens: Connections are not complete for certain nets.
- ③ Parameter Mismatch: LVS also checks for parameter mismatch. e.g. It may match a resistor in both layout and schematic, but the resistor values may be different. This will be reported.

④ Unbounding: If the pins don't have a geometry but all the connection to the net are made and unbounding is reported.

made
63-116

(3) Antenna

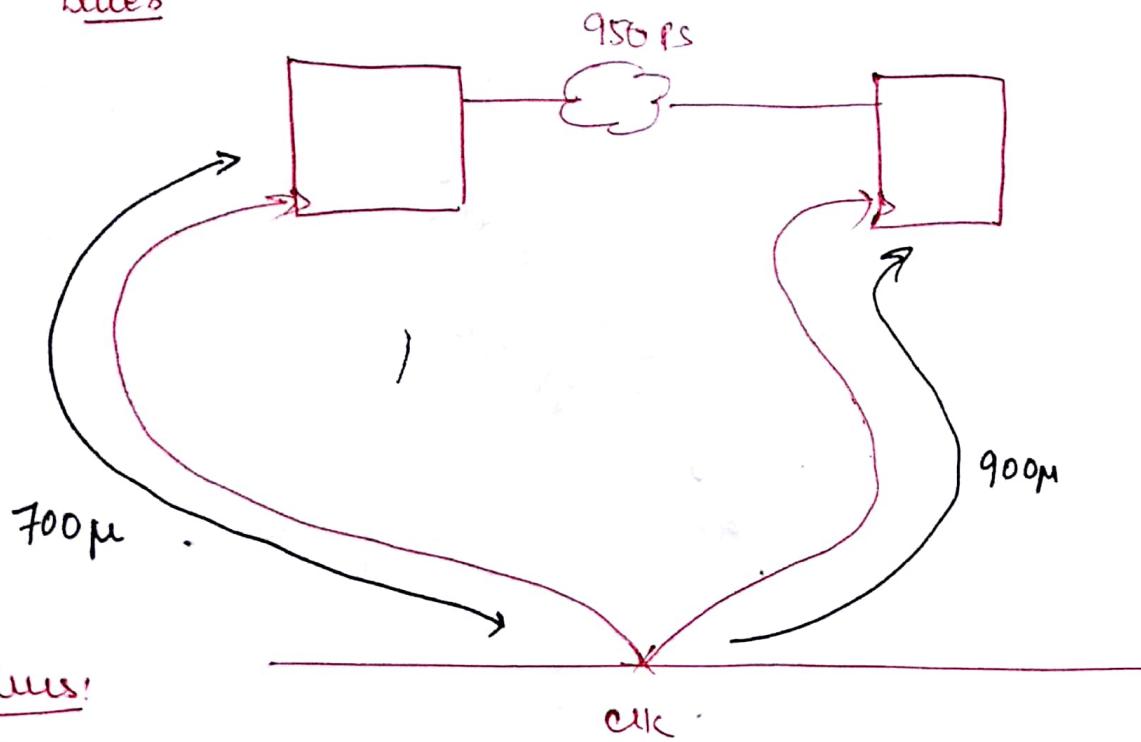
④ ERC (Electrical Rule Check): It involves checking

a design for all electrical connection that are considered dangerous.

* Floating gate error: unconnected gate leads to leakage issue.

VDD/VSS Errors: The well geometry need to be connected to power ground.
"Nwell not connected to VDD"

Ques



Ans:

$$Clk_q = 5$$

$$\text{Setup} = 3$$

$$\text{Hold} = 2$$

$$\text{Time period} = 1000$$

One buffer can drive 50μ & delay of ~~100 ps~~

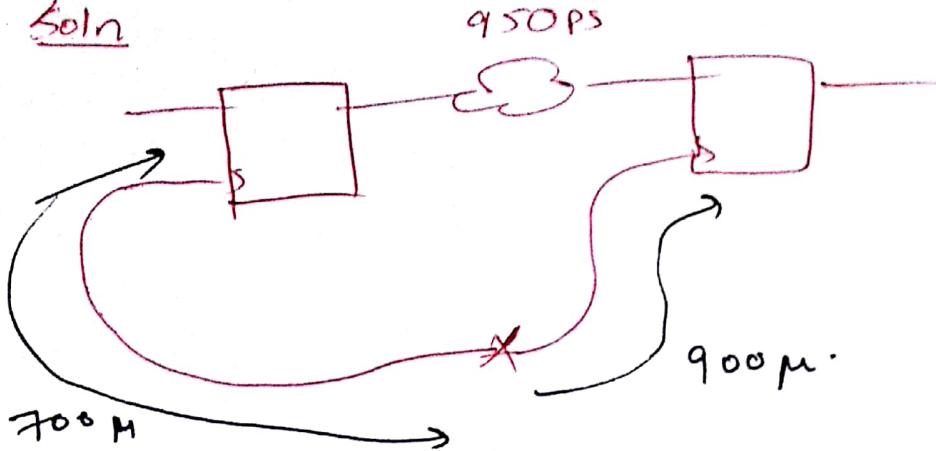
1 buffer is $= 50 \text{ps}$ in $SS_{\text{op}} - q_v - 125 \text{ps}$
its

~~25 ps in $FF_{\text{op}} - 10V_0$~~

~~derate % = 10%.~~ 1st part without derate.

Analyse the circuit.

Soln



So, for setup which corner ??

$$AT = \frac{700}{50} \times 50 + 5 + 950 + 3$$

$$= 700 + 5 + 950 + 3 \\ = 1658$$

$$RT = \frac{900}{50} \times 50 + 1000 \\ = 1900$$

If ques is asked
calculate RT &
AT then.

$$AT = 700 + 5 + 950 \\ = 1655$$

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$$\therefore \text{Setup slack} = (RT - AT)$$

$$\therefore \text{Setup slack} = (RT - AT) =$$

for hold, which corner ??

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$$= 350 + 950 + 5 = 1305$$

$$RT = \frac{900}{50} \times 25 + (2)$$

$$= 452$$

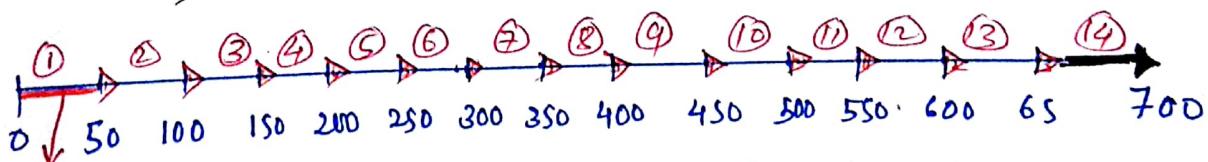
$$\therefore \text{Hold slack} = (AT - RT) =$$

So to drive 50μ if we need 1 buffer
 then to drive 700μ how many buffers
 we need

$$\frac{700\mu}{50\mu} = 14$$

But one ambiguity arises which is like
 why to put buffer at 0μ & finally if
 you don't put buffer at 0μ then number
 of buffer will reduce to $= 14 - 1$
 i.e. = 13

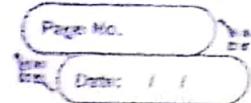
But i feel this is wrong perception



i) this part is driven by buffer 1 so by virtue of explanation
 we can say section ⑬ is driven by buf 13 but
 what abt section 14 so i feel one more buffer
 is needed to drive that. Section represented in
 black.

Basics of Unix By

Ziyauddin Huque



Agenda

- ⇒ Creating Files
- ⇒ Indulging in File Play
- ⇒ Listing Files & Directories
 - * Masking File Permission
 - * Directory Permissions
 - * Removing A File Forcefully
 - * Other Useful ls Variations
- ⇒ Directory Related Commands
 - * mkdir
 - * rmdir
 - * cd

Creating Files: There are two commands to do so: [touch] & [cat]

touch → it will create a file of zero bytes
what is use? {

↳ It is of great use. How abt. creating several empty files quickly

\$ touch s₁ s₂ s₃ s₄ ↵

But what if you want to store few lines in the file; Just type command

\$ [cat > test]

after entering the text ↵; press ctrl+d

ctrl+d indicates End of file character (EOF)
to see the content of file use

\$ cat test.

Now we know two uses of cat command. One is to create new files and another to display contents of existing file. Besides these cat is also used to concatenate the contents of two files and store them in the third file.

```
$ cat sample1 sample2 > newSample
```

This would create newSample which contains contents of sample1 followed by contents of sample2.

★ If newSample already contains something it would be overwritten. If you want that it would remain intact and contents of sample1 and sample2 should get appended to it then you should use the 'append' op/redirectional operator'; >> as shown below

```
$ cat sample1 sample2 >> newSample
```

Indulging in File Play:

Now that we know how to create files & display them let us indulge ourselves in more file related commands. Like those for copying files, renaming files, deleting them, listing them etc.

Copy:

Before understanding this we should have little bit idea of absolute & relative path.

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(3)

Absolute path: It starts with root directory /.
Relative path: It starts from the directory you are in now.

↳ (pwd)

Now, copying

`cp <source file path> <destination file path>`

e.g.

\$ cp /user/xyz/chapter1 /usr/xyz/chapter2

Copy everything to this &
rename as chapter 2.

★ if you want to copy full content of directory as (cp -rf)

Ⓐ If you just want to rename the file name use (mv)
e.g. mv test sample ↲

rm → It deletes the file or files supplied to it.

rm -i → It removes the file interactively i.e. you are asked for confirmation.

rm -r → delete content of directory as well as the directory itself.

Listing Files & Directories

②

[ls]

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(*) It will not enlist the hidden file.

How to create hidden file?

\$ cat > .cricket <

Sahin is the Best Batsman.

Now try ls.

So to see hidden file use [ls -a]

Try → ls, ls -l, ls -a, ls -lxt,
ls -la

(*) Let us get back to possibly the most imp. field
in the o/p of ls -l: the permission field.

r → read
w → write
x → execute.

There are three entries to which any
combination of these permissions are assigned.
These entries are the owner, the group, and
the other (those outside the group)

e.g. rwx r-x -
owner group other.

(*) — means permission is denied.

See the weight

— → it can be 1 or 0

So if rwx that means all are true then 111
= 7

therefore use [chmod 777] to give full permission

Directory Related Commands

(5)

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When the user logs in, he is always brought in his default 'working area' & which can be found by command '`pwd`'.

`mkdir:` It will create directory.

`mkdir -p;` It allows you to create multiple generations of directories, at one go. That means, it creates all the parent directories specified in the given path too.

e.g. `$ mkdir -p works/bpd/unix/ziya`

>Create works, then bpd & next its child directory unix and lastly ziya nested within all these.

* Suppose you want to create a directory which should have permissions 754 irrespective of the umask value you can use the command

`$ mkdir -m 754 newdir`

`rmdir:` It deletes the empty directories.

`$ rmdir -p works/bpd/unix/book.`

Here on removing book directory if unix is empty it will also removed, similarly if removing unix if bpd is empty it is also removed. This will only stop if non empty is found.

`cd:` Change directory.

Essential Unix Commands

(6)

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- ⇒ Password
- ⇒ Cal is for calculator
- ⇒ File Related Commands
 - ↳ wc
 - ↳ sort
 - ↳ cut
 - ↳ grep

Password

\$ passwd.

Calender

\$ cal

\$ cal 2 1997 ↴

↳ It will open calendar of
feb 1997.

wc →

It counts the number of lines, words & characters in the specified file or files. It comes with option -l, -w & -c.

e.g. \$ wc -lc file1 file2

file1 20 571

file2 30 804

* wc is capable of accepting inputs directly from the keyboard & on terminating by Ctrl+d ; the appropriate counts are displayed for the input that you specified.

<sort>

Sorting is done a/c to ASCII collating seq; That is, it sorts the spaces and tab first, then the punctuation marks followed by numbers, uppercase letters and lowercase letters - in that order.

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(7)

- ★ Apart from sorting this command merge multiple sorted files in a single file

e.g.

\$ sort -o result file1 file2 file3

<grep>

↳ globally search a regular expression and point it,

① e.g. \$ grep picture newfile

↳ It will search for word picture in the file newfile.

② \$ grep 'picture' newfile storyfile

↳ It will search 'picture' in the newfile & storyfile & if found line containing word would be displayed.

③ If you are searching more than a single word, single quotes can be used to enclosed the same, as in:-

\$ grep 'the picture taken' -i -n newfile

(Case insensitive)

num of lines pattern
find by side of each line.

I/O Redirection and Piping

(8)

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- > implies redirection of output and symbol
< implies redirection of input. The symbol
> sends the output of a command to
the file or a device, such as printer.
The symbol < takes the input needed
for a command from a file rather than
from keyboard.

★ Symbol >> adds o/p of a command
to the end of a file without deleting
the info already in the file.

Run → ① \$ cat file1 > file2 ??

② \$ cat < current-file > newfile ??

③ \$ cat > newfile < currentfile ??

~~for executing this you will press~~

Pipe: |

cmd1 | cmd2 → makes std o/p of
cmd1 to std i/p of cmd2.

What will following do?

① \$ ls | wc -l

② \$ ls | wc -l > countfile .

Vi, The king of all Editors.

(9)

Modes of operation :-

① Command Mode :

all the keys pressed by the user are interpreted to be editor commands. e.g. if you hit h cursor will move on position left.

② Insert Mode :

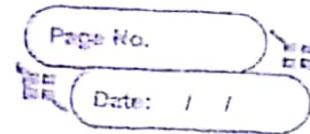
This mode permits insertion of new text, editing of existing text or replacement of existing text. Each of these operations can be performed only after changing over from the command mode to insertion mode using appropriate commands.

③ The ex Command Mode :

This mode permits use to give commands at the command line. The bottom of the vi editor is called command line.

Let's Start

\$ vi filename: ↵



Commands for Positioning Cursor in the Window

N1 Positioning by Character

Command	Function
h	Moves the cursor one character to the left.
Backspace	Moves the cursor one character to the left.
l	Moves the cursor one character to the right.
Space bar	Moves the cursor one character to the right.
0	Moves the cursor to the beginning of the current line.
\$	Moves the cursor to the end of the current line.

N1 Positioning by Line

Command	Function
j	Moves the cursor down one line from it's present position, in the same column.
k	Moves the cursor up one line from it's present position, in the same column.
+	Moves the cursor down to the beginning of next line.
-	Moves the cursor upto the beginning of previous line.
Enter	Moves the cursor down to the beginning of the next line.

N1 Positioning by Word

Command	Function
w	Moves the cursor to the right; to the first character of the next word.
b	Moves the cursor back to the first character of the previous word.
e	Moves the cursor to the end of the current word.

N1 Positioning in the Window

Command	Function
H	Moves the cursor to the first line on the screen, or "home".
M	Moves the cursor to the middle line on the screen.
L	Moves the cursor to the last line on the screen.

Commands for Positioning in the File

N1 Scrolling

Command	Function
Ctrl f	Scrolls the screen forward a full window, revealing the window of text below the current window.
Ctrl b	Scrolls the screen back a full window, revealing the window of text above the current window.

Imp: Positioning on a Numbered Line

Command	Function
G	Moves the cursor to the beginning of the last line in the file.
nG	Moves the cursor to the beginning of the n^{th} line in the file.

Imp:

Commands for Inserting Text

Command	Function
a	Enters text input mode and appends text after the cursor.
i	Enters text input mode and inserts text at the cursor.
A	Enters text input mode and appends text at the end of current line.
I	Enters text input mode and inserts text at the beginning of current line.

O	Enters text input mode by opening a new line immediately below the current line.
O	Enters text input mode by opening a new line immediately above the current line.
R	Enters text input mode and overwrites from current cursor position onwards.

Commands for Deleting Text

Command	Function
X	Deletes the character at current cursor position.
X	Deletes the character to the left of the cursor.
dw	Deletes a word (or part of a word) from the cursor to the next space or to the next punctuation.
dd	Deletes the current line.
nx, ndw, ndd	Deletes n characters, n words or n lines.
d0	Deletes the current line from the cursor to the beginning of the line.
d\$	Deletes the current line from the cursor to the end of the line.

Miscellaneous Commands

Command	Function
Ctrl g	Gives the line number of current cursor position in the buffer and modification status of the file.
.	Repeats the action performed by the last command.
u	Undoes the effects of the last command.
U	Restores all changes to the current line since you moved the cursor to this line.
J	Joins the line immediately below the current line with the current line.
~	Changes character at current cursor position from upper case to lower case or from lower case to upper case.
:sh	Temporarily returns to the shell to perform some shell commands. Type exit to return to vi.
Ctrl l	Clears and redraws the current window.

IMP: Commands for Quitting vi

Command	Function
ZZ	Writes the buffer to the file and quits vi.
:wq	Writes the buffer to the file and quits vi.
:w filename and :q	Writes the buffer to the file filename (new) and quits vi.
:w! filename and :q	Overwrites the existing file filename with the contents of the buffer and quits vi.
:q!	Quits vi whether or not changes made to the buffer were written to a file. Does not incorporate changes made to the buffer since the last write (:w) command.
:q	Quits vi if changes made to the buffer were written to a file.

gmp:

Command	Function
:nd	Deletes n th line.
:m,n d	Deletes lines from m to n .
:n mo p	Moves line n after line p .
:m,n mo p	Moves lines m to n after line p .
:m co p	Copies line m after line p .
:m,n co p	Copies lines m to n after line p .
:m,n w filename	Writes lines m to n to a file.
:m,n w >> filename	Appends lines m to n to a file.
: r filename	Reads the contents of the file filename at current cursor position.
:r !command	Executes shell command and output of the command is read at the current cursor position.

Ans.

Command	Function
/pattern	Searches forward in the buffer for the next occurrence of the pattern of text. Positions the cursor under the first character of the pattern.
?pattern	Searches backward in the buffer for the first occurrence of the pattern of text. Positions the cursor under the first character of the pattern.
n	Repeats the last search command.
N	Repeats the search command in the opposite direction.

grep

Command	Function
: s/str1/str2	Replaces first occurrence of str1 with str2 in current line.
: s/str1/str2/g	Replaces all occurrences of str1 with str2 in current line.
: m,n s/str1/str2/g	Replaces all occurrences of str1 with str2 from lines m to n .
: 1, \$ s/str1/str2/g	Replaces all occurrences of str1 with str2 from 1 st line to end of file.
: 1, . s/str1/str2/g	Replaces all occurrences of str1 with str2 from 1 st line to current line.
: ., \$ s/str1/str2/g	Replaces all occurrences of str1 with str2 from current line to end of file.

Yank

Command	Function
yw	Yanks word from cursor position.
yy	Yanks line from cursor position.
y\$	Yanks line from cursor position to end of line.
y0	Yanks line from cursor position to beginning of line.

Figure 6.9

To paste the matter present in the yank buffers use the following commands.

Yank

Command	Function
1p	Pastes last yanked buffer.
2p	Pastes last but one yanked buffer.

Figure 6.10

no.

Command	Function
:set nu	Set display of line numbers on.
:set nonu	Set display of line numbers off (default).
:set eb	Beep the speaker when an error occurs (default).
:set noeb	Do not beep the speaker when an error occurs.
:set ai	Set auto indent on.
:set noai	Set auto indent off (default).
:set ic	Ignore case while searching a pattern.
:set noic	Do not ignore case while searching a pattern (default).
:set terse	Make messages terse.
:set noterse	Do not make error messages terse (default).
:set mesg	Permit receipt of messages from other terminals.
:set nomesg	Don't receive messages from other terminals (default).
:set show-mode	Display mode in which we are working.
:set noshow-mode	Do not display current working mode (default).
:set aw	Automatically write buffer contents to disk before switching to next file during multiple file editing.
:set noaw	Do not write buffer contents to disk before switching to next file during multiple file editing (default).

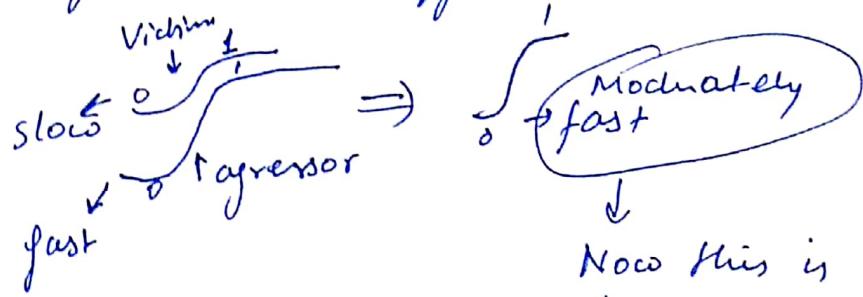
Figure 6.13

Crosstalk:

Switching of the signal in one net can interfere neighbouring net due to cross coupling capacitance. This effect is known as Crosstalk. Crosstalk can be of two types

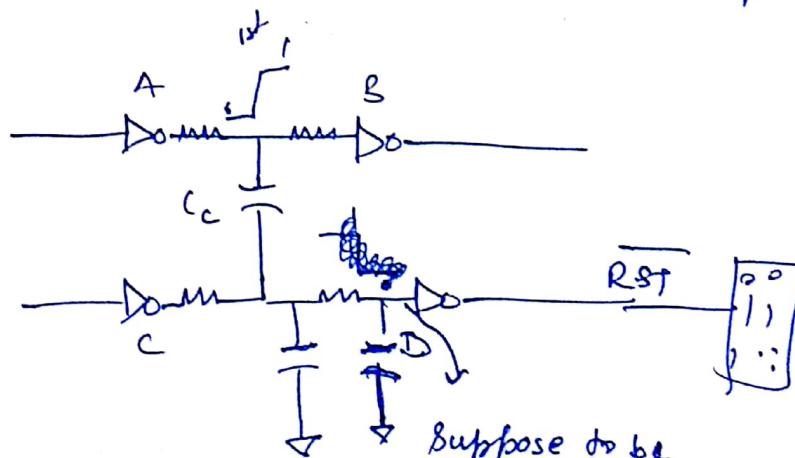
- ① Delay ↗ Setup & Hold violation
- ② Noise ↗ functionality issue

→ let say 1 net is switching from 0-1 slowly & ~~fast~~ during course of switching if any other net affect it like



Now this is good ~~for~~ for Hold
bad ~~for~~ for Setup.

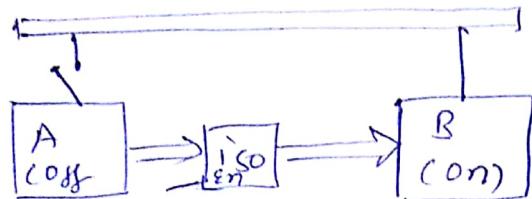
Noise:



Suppose to be 0 but because
if it be 1

Few special Handling for Low Power

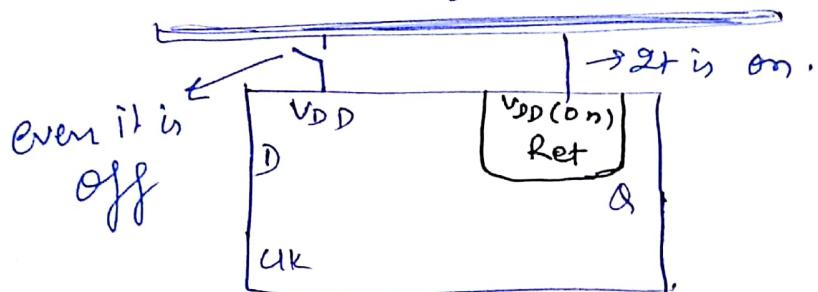
- ① Isolation cell. Inserted b/w two domains to



prevent signals from floating when driving domain is power off.

- ② State Retention DFF

Special FF in a switchable domain that can retain its value when switchable domain's power supply is off. It has secondary power pin to power the retention logic.



- ③ level-shifter cell: It is mainly used when u want to go from one voltage level to other voltage level.

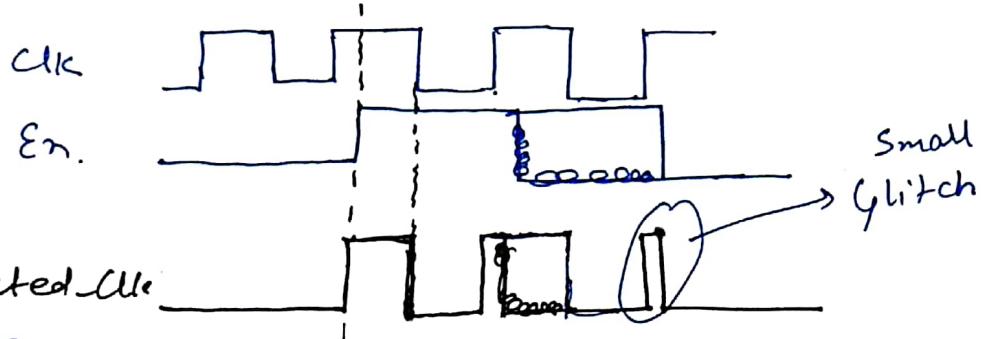
(1)

Clock gating: Clock tree consumes more than 50% of dynamic power. The component of these power are:

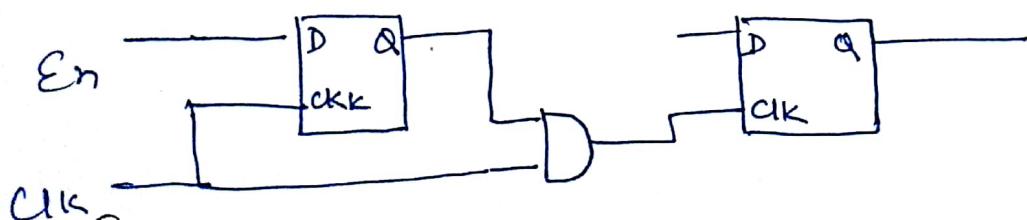
- (1) Power consumed by combinational logic whose values changing on each edge.
 - (2) Power consumed by FF.
 - (3) Power consumed by the clock buffer tree in the design.
- * So it is good design idea to turn off the clock when it is not needed. Automatic clock gating is supported by EDA tools.

There are two types of clock gating styles:-

- (1) Latch free clock gating.
- (2) Latch Based.



(2)



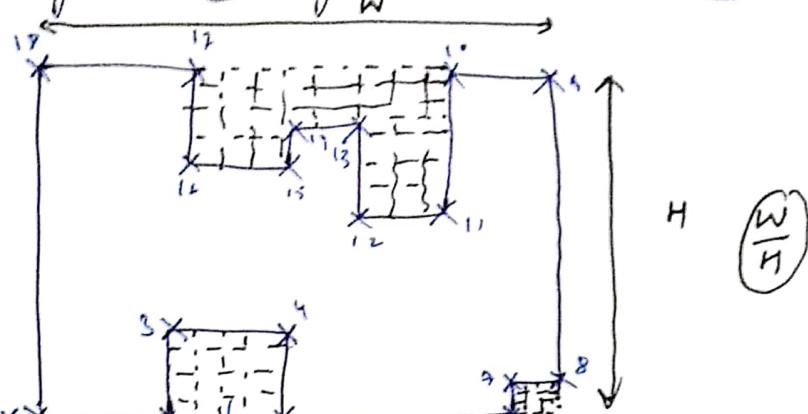
* Enable will only reflect on o/p when CLK is on so no chance of any glitch.

Aspect Ratio:

(2)

$$= \frac{\text{Width of core/Die}}{\text{Height of core/Die}}$$

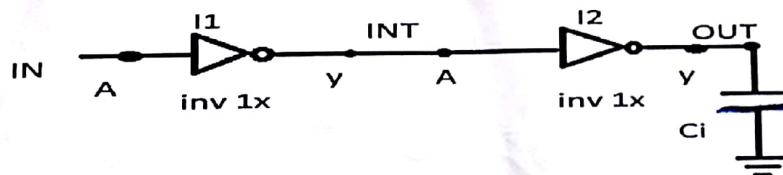
How to give aspect Ratio for Rectangular Block



aspect ratio = W/H
create - diearea - poly { coordinates of all points }

Inter-clock-uncertainty: The uncertainty margin that is given b/w two different clock Domains.

1. With respect to block-level fp arrange the following in right order.
3 {Place macros, creat die & core area, Place ports/pins, creat p/g grid}.
1
2
4
2. On which factors cell delay depends? 2
3. What are the different types delays on which we focus mainly during STA? 2
4. What is virtual clock? How we can say any clock is virtual/ generated/ mastered by looking into sdc. File? 4
5. How prime time will report if you a
 - Set-false path
 - Set-disable time
To you design. 3
6. Explain mmmc. Which parasitic interconnect corners are checked for setup and hold? 3
7. Draw the waveform for following
 - Create_clock -period 1.2 -wavefor{0.30.4 0.81.0} JTAG CLK2
8. Explain OCV, Derate and CRPR. 4 - 2
9. Considering interconnect parasitics are not considered here find path delay b/w IN & OUT. 5 1



Slew at IN = 10ps

Load at OUT (C_i) = 2PF

I/P pin capacitance (I1 & I2) = 1 PF

Delay Table

Slew at A

Load at Y

	1PF	2PF
10ps	40ps	50ps
20ps	50ps	60ps

10. How synthesized netlist i.e. (.v) is in i/p stage of Floorplan is different from RTL
3 -)

11. What is clock latency? Explain source & n/w delay. (5) (E1)
12. What is difference b/w a Halo & a Blockage? (3)
13. What is setup & hold timing? Derive equation to find setup & hold slack. (8) (E2)
14. What are timing exceptions? Why they should be given as constraints? (3)
15. Explain PD flow, i/p & o/p files in each stage. (5)
16. What is uncertainty? Explain inter clock uncertainty. (4)
17. Can there be setup & hold violation for same path? Justify your answer. (5)
18. What is scan chain reordering? (3)
19. Explain following terms and ways to fix them:-
- Congestion
 - Electro migration
 - Crosstalk
 - CMOS Latch-up
- (8)
20. What is crosstalk delay and Crosstalk noise? (4)
21. Explain various kind of preplaced cells. (5)
22. What is NDR? Which stage of PD we apply NDR and why? (5)
23. What are the main goals of CTS? (3)
24. Write Linux commands to perform following operations.
- Make a directory ZIYA
 - Make files x1, x2, and x3.
 - Make a text file x4 and write "I love my India".
 - Make a file with given permission to **read& write** to all but no one should have execute permissions.
- (10) (E2)
25. Write a command to find "Ziya is a good teacher" in a file named XYZ. (2)
26. Create a hidden file & write your favourite actor name. (2)
27. Write a command to find how many times error occurred in your report. (2)

~~Physical Design Questions~~ ~~Predominantly~~

~~Asked in interviews~~

~~By~~

~~Richard~~

Ques: 1 What is multivoltage design? Which extra file is needed when you deal with such a design.

Ques: 2 What is pad limited design and core limited design?

Ans:

PLD: Area of pad limits the size of die. No of IO pads may be larger.

CLD: The area of core will limit the size of die. No. of IO pads may be lesser.

Ques: 3 What is best place to put an HARD macro if it is a power hungry device and dissipate of heat.

Ques: 4 What is diff b/w std cell & IO cells.

Ques: 5 What is TDF format?

Ques: 6 Diff b/w Hierarchical & flat Design?

Ques: 7 If you have both IR drop and Congestion how will you fix it?

Ans: 7

- Spread Macros
- Spread std cells
- Increase strap width
- Increase No. of straps
- Use proper blockages.

Ques: 8 What is tie high and tie low cells and where it used?

Ques:9 Which is Better buffer or inverter?

Ans:? Inverter

① Since transition time is less

② Reduction of duty cycle distortion

Ques:10 What are all the checks to be done before doing CTS?

Ques:11 How to decide pin/pad location.

Ans:11 It is decided in such a way that it meets

① Top level requirement (If it is a block)
Timing

② Timing & congestion

③ Area & power.

* For chip top they have TDF (google?)

Ques:12 How much utilization is used in the design.

Ans:12 There is no hard & fast rule, even though if the following values maintained then the design can be closed without much congestion.

FP Placement	→ 70%
CTS	→ 75%
Routing	→ 80%
During GDSII Generation.	→ 85%
	→ 100%

(Google GDSII)

Ques:13 What is diff b/w std cells and IO cells? Is there any diff in their operating voltage.

Ques:14 What is there in .upf, .cpf & .saif file? (also see vcd)

Ques:15 What is SITE?

Ques:16 How diff is the floorplan if we go for the flip chip approach?

Ques:17 How to decide Core power pad values, Core Ring width calculation, Mesh width, EM Rule Calculation, IR Drop calculation.
Roughly you have to do powerplanning & decide the values. (~~You can expect ans from me just remind me~~)

Ques:18 Why is powerplanning done & How? which metal should we use for power & gnd ring & strips & why?

Ques:19 What is Scan chain Reordering? How will it impact PD?

Ques:20 How to fix setup/Hold during placement stage?

Ques:21 What is HFN^{synthesis} in placement stage?

Ques:22 Explain placement in detail?

Ques:23 B/w floorplanning & placement do we have any other PD floo?

Ques:24 Why we give NDR in placement?

Ques:25 How to limit congestion in Placement here. How to check congestion in Placement stage?

Ques:26 what is CTS. What is main aim of CTS?

Ans:27 What are the SDC constraints associated with clock tree?

Ans:28 Draw waveform and also ckt of divide by 2 generated clock. Why generated clock used.

Ans:29 What is skew. Explain, global skew, useful skew, local skew, target skew.

Ans:30 What is CTO (Clock Tree optimisation)

Ans:31 Deep. (Submicron effect) What are affect of shrink in technology

Ans:32 Explain various kind of clock tree & give adv. and disadv. of each.

Ans:33 What are all checks to be done before doing CTS?

Ans:34 What is clock latency. Explain source & N/w latency?

Ans:35 Should it be create-clock or create-generated-clock for any internal pins in design.

Ans:36 Explain something about Nested Generated clock?

Ques:37 what is clock gating. What is use of Latch Based & Latch-free clock gating.

Ques:38 Difference b/w normal Buffer & Clock Buffer.

Ques:39 Diff b/w HFN synthesis & CTS.

Ques:40 Is it possible to have zero skew in your design.

Ques:41 What kind of optimization done in CTO.

Ques:42 What cells might you put a "don't touch" on before placement?

Ques:43 Diff b/w target & link library.

Ques:44 What are CTS exceptions. Explain float, stop, exclude & ignore pins.

Ques:45 What is fly line analysis. How it will be useful.

Ques:46 Why should we solve hold violation in CTS only.

Ques:47 How to reduce setup / Hold violation?

Ques:48 What is uncertainty. Explain diff types

Ques:49 What is latchup and how to reduce it?

Ques:50 What is trial/ global routing?

Interview Ques
part: 2
~~Arial~~
by:

Ques:51 : What is Routing? Explain in detail.

Ans:52 : What is Congestion? What is overflow.

Ans:53 What is trial route?

Ques:54 What are issues you can face because of congestion as a PD Engineer. How to fix it.

Ques:55 How is Track assignment different from search & repair and detail routing?

Ques:56 What are routing blockages?

Ans:57 What is Overflow; how will you measure the overflow.

Ques:58 If you want to route

- (A) Signal
- (B) Power
- (C) Clock

What would be preferred order.

Ans:59 How to limit Congestion?

Ans:60 Let say you are using 9 metal layer boundary lib, then explain which metal layer can be used for power, clock, macro / std cell placement?

STA

Ques:61 what is WLM? Explain with example.

In which file WLM will be defined & why?

Ans:62 What is there in .sdc?

Ques:63 What is duty cycle distortion?

Ques:64 What are factors on which Cell delay depends. What is NLDM?

Ques: 65 what is there in .lib . Apart from NLDM what types of timing models used now a days.

Ques: 66 what is use of virtual clock?

Ques: 67 Explain setup & hold time with help of waveform?

Ques: 68 Derive equation to satisfy setup & hold analysis.

Ques: 69 what are timing exceptions. Why they should be given as constraint.

Ques: 70 Explain the following terms.

- (a) Skew
- (b) Insertion delay
- (c) Uncertainty.

Ques: 71 How is STA diff from DTA.
Which is good & why?

Ques: 72 If we are fixing timing issues from starting only then what is need of sign off (Timing) ?

Ques: 73 G/P & O/P files to PT?

Ques: 74 What are operating conditions analysis mode of PT?

Ques: 75 How to fix setup & hold violation?

Ques: 76 what is ECO cycle?

Ques: 77 what is min/max analysis?

Ques: 78 what is OCV analysis?

Ques: 79 Can setup & hold analysis be done by using single library from vendors?

Ques: 80 what is derate? Also explain CRRR.

Ques: 81 write PT command to report Setup & hold slack independently?

Ques: 82 can a latch Based design be analyzed using STA? Explain time Borrowing in Latch Based path?

Ques: 83 what are diff kind of delays in STA analysis?

Ques: 84 How delays vary with diff PVT conditions? Show the graph?

Ques: 85 what is the dmax value that can be used?

↳ for setup - 8 to 15% - no derate in clock path.

for Hold - 8 to 15% - no derate in data path.

Ques: 86 what is latency? Give the types?

Ques: 87 What is Unlatency? Explain positive & negative unlatency.

Ques: 88 what is clock jitter?

Ques: 89 what is local skew & global skew?

Ques: 90 Explain target & useful skew?

Ques: 91 Explain MMMC. Which parasitic interconnect is checked for setup & Hold?

Ques: 92 Can I apply dmax on timing check i.e. (lib setup hold time)

Ques: 93 How PT will report

- (a) Set - false - path
- (b) Set - disable - timing

Ques: 94 Can one new clock, that is a master clock be defined at the O/P of ff instead of generated clock?

Ques: 95 What is interclock uncertainty.

Ques: 96 Draw the waveform?

(a) Create_clock - period 1.2 - waveform {0.3 0.4 0.8 1.0} JTAG_CLK.

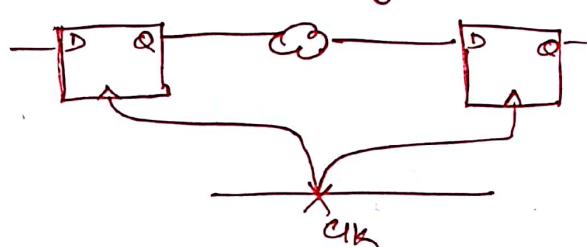
(b) Create_clock - period 1.2 [getports CLK]

Ques: 97 What are timing end points?

Ques: 98 What is Hierarchical pin?

Ques: 99 What are diff Timing paths?

Ques: 100



$$CK_q = 5, T_{setup} = 3; T_{hold} = 2, T.P = 1000$$

One buffer can drive 50pH & delay of 1 buffer is 50ps in SS_OPO_9V_125 & 25ps in FF_OPO_10V_0.

(a) Analyse the ckt.

(b) Considering 10% derate is applied ~~on top~~.

Analyse the ckt.

Interview Questions
Part - III
of miscellaneous Ques
comprises of Random topics
from Linaul Hugue / ~~Final~~

Aus: 101 In a reg to reg path if you have setup problem where will you insert buffer - near to launching flop or capture flop ? Why ?

Aus: 102 Explain physical verification in sign off stage ?

Aus: 103 Which is more complicated when u have 50 MHz and 500 MHz clock design ?

Aus: 104 Explain the working of commands below w.r.t derates.

- a) set-timing-derate - early - cell-delay 0.9
- b) set-timing-derate - late - cell-delay 1.2

Aus: 105 What is Halo ? How is it diff from blockages ?

Aus: 106 calculate channel width b/w two macros if we have 2 macros having 100 pins on each and metal pitch = $0.25 \mu\text{m}$. Out of Nine metal layer only six are allowed for routing ?

Aus: 107 Differentiate b/w Hierarchical & flat design ?

Aus: 108 What is SITE ?

Aus: 109 How to handle hotspot in a chip ?

Aus: 110 How to prevent CMOS latchups ?

Aus: 111 What are Generated clock ? Explain divide by-2 clk by waveform analysis .

Ques: 112 A balanced clock tree can be made by inserting inverters & buffers so which approach is good

- (a) adding more inverters than buffers.
- (b) adding more buffers than inverters.

Explain?

Ans: 113 what will happen if create-clock is defined on a non-physical hierarchical pin?

Ques: 114 What is clock gating? How a latch enable will overcome disadvantage of latch free clock gating?

Ans: 115 what are the vibrations solved in LVS?

Ques: 116 Why filler cells are used?
↳ P-well & N-well connectivity
↳ ↑ yield.

Ans: 117 what is crosstalk? Diff b/w crosstalk delay & crosstalk noise?

Ques: 118 what is power/ground bounce?

Ques: 119 what is Dishing Effect?

Ques: 120 How can we avoid crosstalk?

Ques: 121 what is EM and its effects?

Ques: 122 what is Antenna effect and Antenna Ratio? How to eliminate this? Why it occurs in deep submicron tech.?

Ques: 123 What / why double via insertion?

Ans: 124 Why metal fill insertion?

Ques: 125 Explain (a) Metal Fill (b) Metal Slotting?

Ans: 126 How you can resolve Antenna violation?

Ques: 127 What are power dissipation components? How do you reduce them.

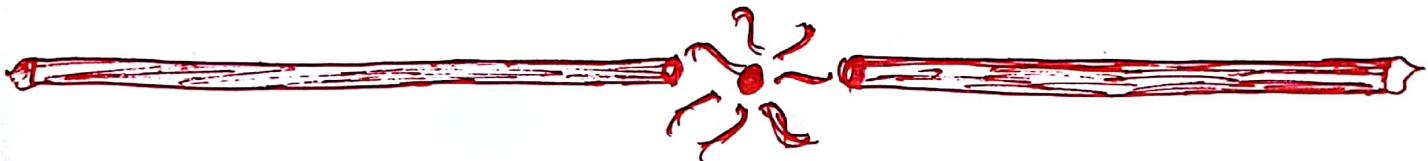
Ans: 128 How can you reduce dynamic power.?

Ans: 129 What is Partitioning?

Ans: 130 What is diff b/w LEF and GDSII file related to a backend lib?

Ans: 131 Design what parameters diff. chip & Block level design?

Ans: 132 What is Recovery & removal time?



STA (Sign off)

①

Sign off engine for timing is Prime time which is predominantly used in Market.

→ We are fixing timing issues in PNR flow then why this Needed?

→ Go to STA NOTES - - - - - >>>

Agenda

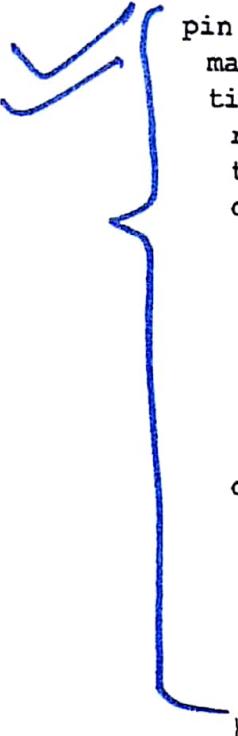
★ Try to understand all Basic terminologies or concepts.

① So, as we know

$$\text{Stage delay} = \underbrace{\text{cell delay}}_{\text{I}} + \underbrace{\text{Net delay}}_{\text{II}}$$

Cell delay: fn (input transition, o/p load)
Where can you find it?

It can be found from the NLDM table present in Std. cell library. This table model captures the delay the cell for various combinations of input transition time at the cell input pin and total o/p capacitance at the cell o/p.



```
pin (OUT) {
    max_transition : 1.0;
    timing() {
        related_pin : "INP1";
        timing_sense : negative_unate;
        cell_rise(delay_template_3x3) {
            index_1 ("0.1, 0.3, 0.7"); /* Input transition */
            index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
            values ( /* 0.16      0.35      1.43 */ \
                     /* 0.1 */    "0.0513,  0.1537,  0.5280", \
                     /* 0.3 */    "0.1018,  0.2327,  0.6476", \
                     /* 0.7 */    "0.1334,  0.2973,  0.7252");
        }
        cell_fall(delay_template_3x3) {
            index_1 ("0.1, 0.3, 0.7"); /* Input transition */
            index_2 ("0.16, 0.35, 1.43"); /* Output capacitance */
            values ( /* 0.16      0.35      1.43 */ \
                     /* 0.1 */    "0.0617,  0.1537,  0.5280", \
                     /* 0.3 */    "0.0918,  0.2027,  0.5676", \
                     /* 0.7 */    "0.1034,  0.2273,  0.6452");
        }
    }
}
```

★ This form of representing delays in a table as a function of two variables transition time and capacitance , is called Non-linear delay Model.

→ ~~Non~~

↓

↓

↓

↓

↓

↓

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Some newer timing libraries for nanometer technologies also provide current source based advanced timing models (such as CCS, ECSV etc.) (2)

The timing models, such as NLDM, represent the delay through the timings arcs based on O/P capacitance and I/P transition. But, in reality the load seen by the cell O/P is composed of capacitance as well as interconnect resistance. The interconnect resistance become an issue since the NLDM approach assumes the O/P loading is purely capacitive. Even with non-zero interconnect resistance, the interconnect resistance is these NLDM models have been utilized when effect of interconnect resistance is very small.

In presence of resistive interconnects the delay calculation methodologies retrofit the NLDM models by obtaining an equivalent effective capacitance at the O/P of the cell. The "effective capacitance" methodologies used here has same delay as RC interconnects.

As the size shrinks, the effect of interconnect resistance can result in large inaccuracy as waveform become highly non-linear. Now new approaches came to provide accuracy by modelling O/P stage of the driver by an equivalent current source. Examples

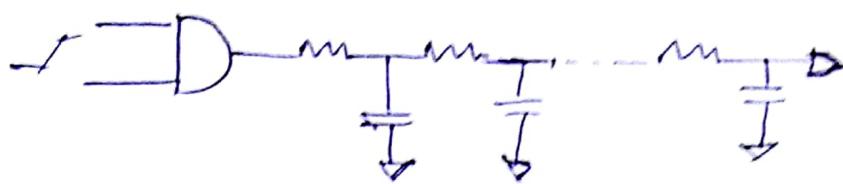
of these approaches are CCS (Composite Current Source) or ECSV (Effective Current Source Model).

*iant

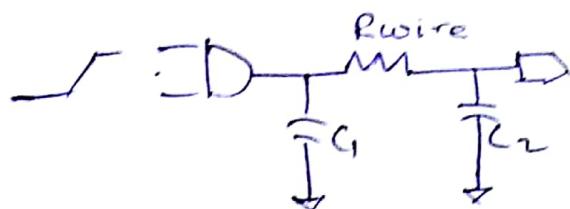
Concept of effective Capacitance

(3)

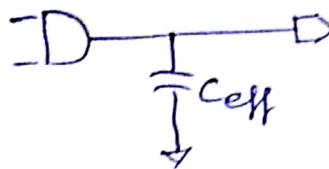
The effective capacitance approach attempts to find a single capacitance that can be utilized as the equivalent load so that the original design as well as design with equivalent capacitance load behave similarly in terms of timing at the I/O of the cell. This equivalent single capacitance is termed as effective capacitance.



① RC Network



② PI model



③ effective capacitance

The effective capacitance is a fn of:

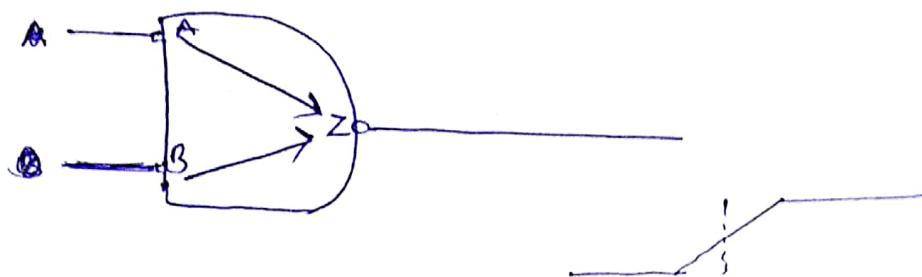
- the driving cell , &
- the characteristics of the load or
Specially the i/p impedance of the load
seen from the driving cell.

*int

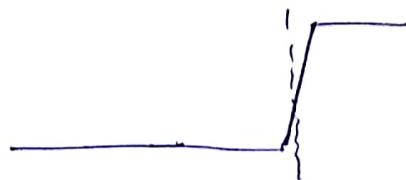
Slew Merging

(4)

what happens when multiple slew arise
at a common pt?



a) Slew at pin Z
due to $A \rightarrow Z$ arc



b) Slew at Pin Z due to
 $B \rightarrow Z$ arc



One thumbs up rule at any node prime time can have only one transition value.

Depending upon the type of timing analysis (max or min) being performed both slew ($A \text{ or } B$) could be selected for further prop.

There is a variable in PT called ~~reset~~

Timing Slew propagation mode; it can be set to one of two values

(a) Max path analysis

(b) Min Path analysis.

Max \rightarrow ?

Min \rightarrow ?

Nicul

Max Path Analysis:

(5)

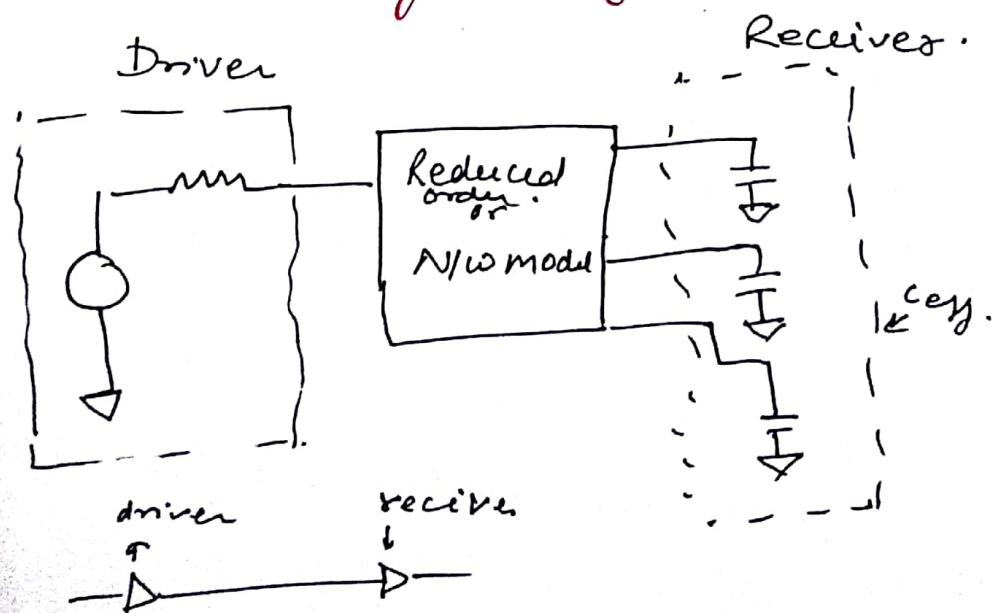
- Worst slew propagation: Selects the worst slew at the merge point to propagate (A)
 - Worst arrival propagation: It means whatever arrives later use that transition. (B)
- 1st one is pessimistic & 2nd one is more accurate, why?

Bcoz since B arrive later most of critical path is through B.

Min Path Analysis:

- Best slew propagation
- Best arrival propagation.

Now we know how Net delay is calculated & how cell delay is calculated then guess here is how PT will calculate delay using SPGF.



*aint

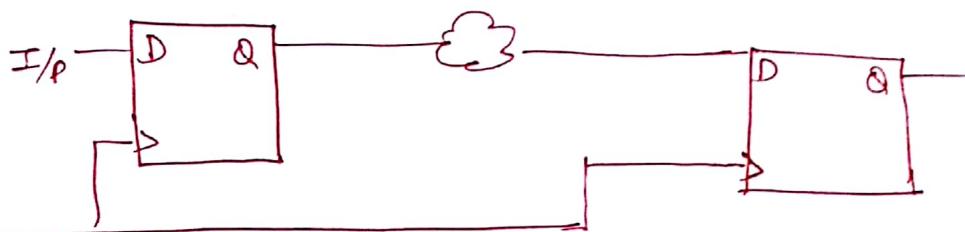
Setup & Hold Time (PD Basic) ⑥

Sep 16

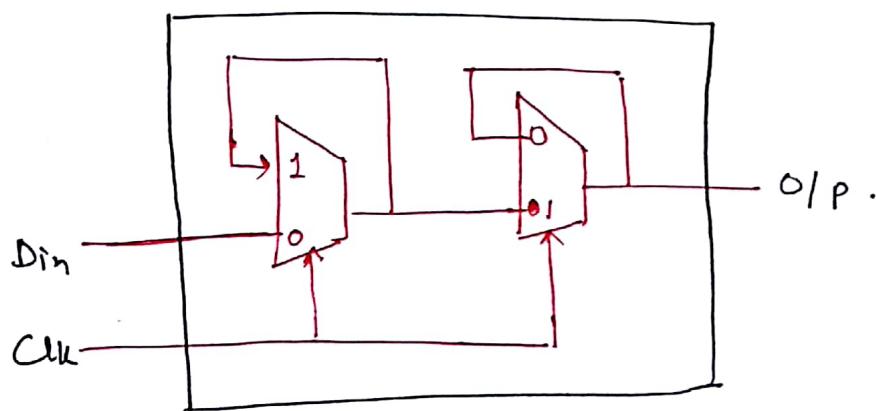
Setup time:

Minimum amount of time data must be stable before clock edge.

Hold time: It is minimum amt of time data stable after clock edge.



How a str of ~~FF~~ look like?

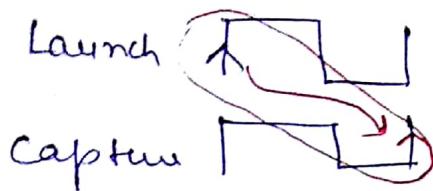


Now you can correlate this with CMOS Str & on basis of charging & discharging of cap. figure out setup & hold time. ☺

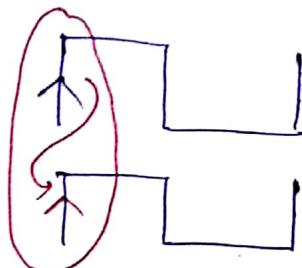
*i am

Setup & Hold check edges

⑦



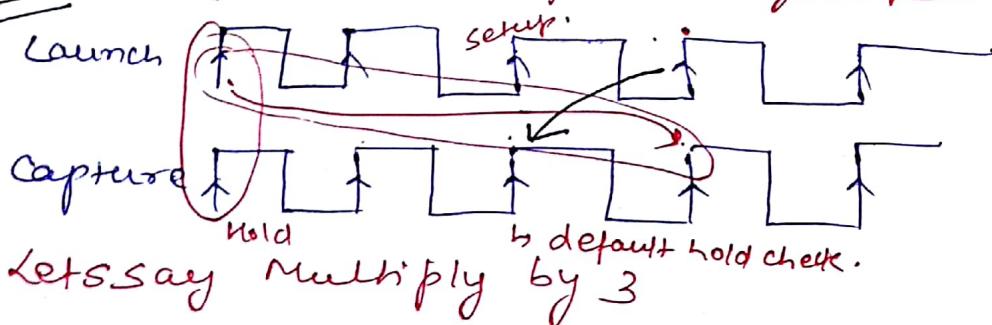
(a) Setup check.



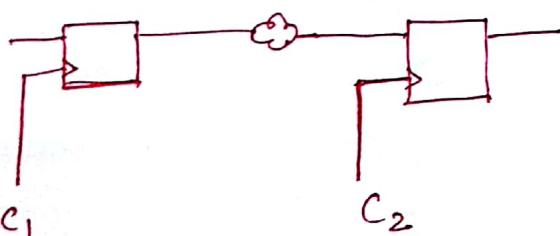
(b) Hold check.

Setup & Hold check for multicycle path

google



Cross clock (CCD)

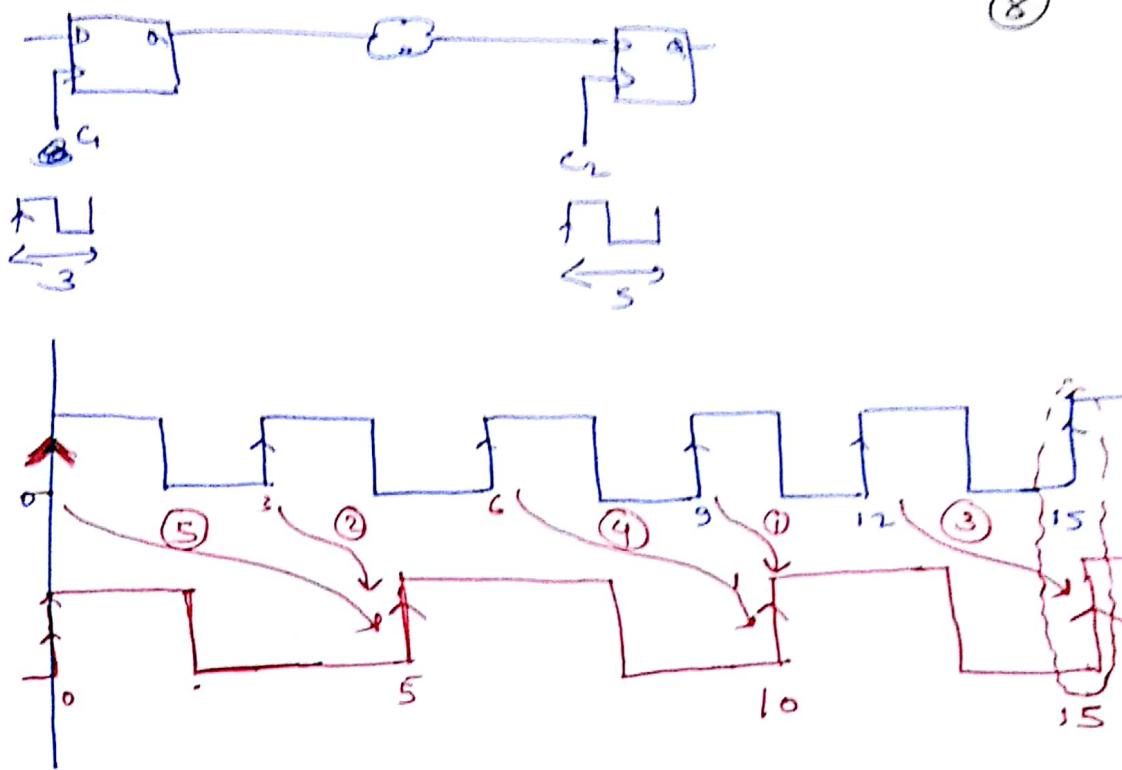


→ Let say clock 1 has period of a & clock 2 has period of b ns so where will common edge comes $\text{LCM}(a, b)$.

→

P.T.O.

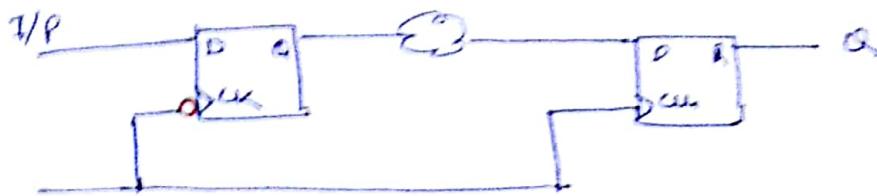
**ians*



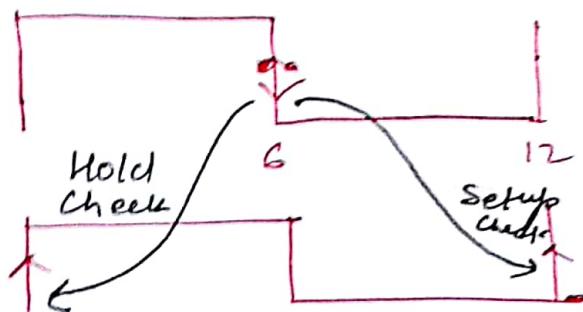
Now if we analyse the ckt we can see
 If launch is at 0 then capture is at 5 &
 Next launch at 3 & capture at 5 (bcz it
 is next edge), Now launch at 6 capture at
 10 similarly launch at 9 capture at 10
 Now at last launch at 12 capture at
 15 so from above analysis we will
 see the window. The most tighter one is
 launch at 9 Capture at 10 so will consider
 this. Now Ques here is is it possible
 to close timing at 1 ps, Ans is No, so
 we only have to give multicycle of
 2 i.e set_multicyclePath 2 from xyz to sab
 It means it will add 1 extra cycle &
 total time period will now become
 $1\text{ ps} + 5\text{ ps} = 6\text{ ps}$. *ps
 Hold analysis will remain same as Multicycle

Half Cycle Paths :-)

⑨



If a design has both negative edge triggered ff (active edge is falling edge) and positive edge triggered flip flops (active edge is rising edge), it is likely that half cycle paths exist in the design. A half cycle path could form from a rising edge FF to falling edge ff, or vice versa.



⑩ Is it good for setup or hold ??

*-out

Setup equation for half cycle:

$$t_{\text{launch}} + t_{\text{cuk_Q}} + T_{\text{comb}} + T_{\text{setup}} = AT$$

$$RT = t_{\text{capture}} + T_{\text{cuk}/2}$$

$$\therefore AT \geq RT$$

$$t_{\text{launch}} + t_{\text{cuk_Q}} + T_{\text{comb}} + t_{\text{setup}} \geq t_{\text{capture}} + T_{\text{cuk}/2}$$

$t_{\text{Skew}} + t_{\text{cuka}} + t_{\text{comb}} + t_{\text{setup}} \leq T_{\text{cuk}/2}$

Hold equation for half cycle:

$$AT \geq RT$$

$$t_{\text{launch}} + t_{\text{cuk_Q}} + T_{\text{comb}} \geq T_{\text{cuk}/2} - t_{\text{hold}} + t_{\text{capture}}$$

$$\Rightarrow t_{\text{cuk_Q}} + T_{\text{comb}} + T_{\text{cuk}/2} \geq t_{\text{hold}} + t_{\text{skew}}$$

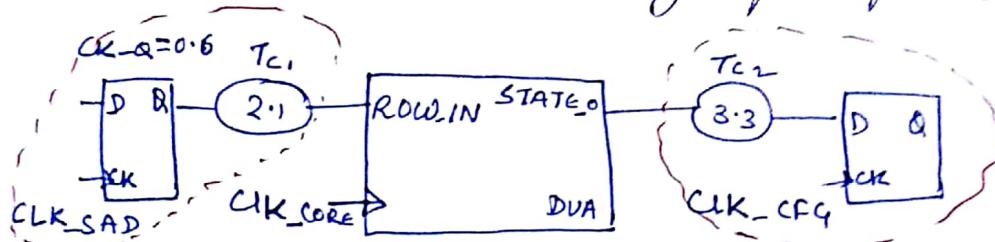
★ So the statement, hold checks is freq. dependent is partially correct. This statement is true only for zero cycle ~~path~~ hold check. By zero cycle hold check means check is performed at same edge at which data is launch.

★ Half cycle paths' hold checks are very relaxed

Virtual Clocks :)

(10)

A virtual clock is a clock that exists but is not associated with any pin or port of the design. It is used as a reference in STA analysis to specify input and o/p delays relative to a clock. An example where virtual clock is applicable is shown below. The design under analysis gets its clock from CLK_CORE, but clock driving input port ROWIN



is unconstrained. How does one apply the IO constraints on i/p port ROW_IN & on O/P port STATE_0 in such cases?

To handle such situation, virtual clock can be defined with no specification of source port or pin. In above fig. virtual clock is defined for CLK_SAD & CLK_CFG.

```
create_clock -name CLK_SAD -period 10
             -waveform {2.8}
```

```
create_clock -name CLK_CFG -period 8
             -waveform {0.4}
```

Having defined these virtual clock, the IO constraints can be specified relative to virtual clock.

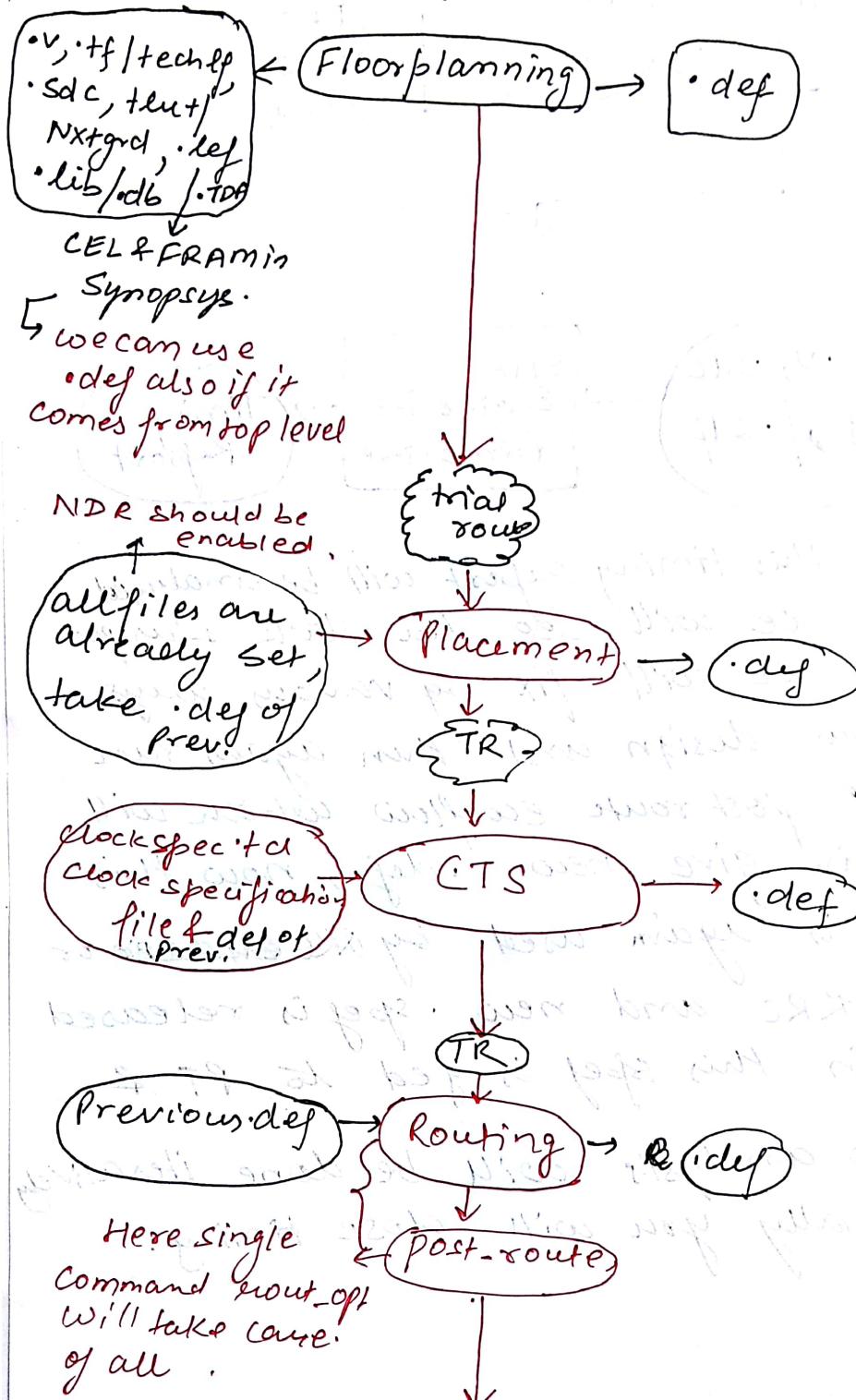
e.g.
~~set_input_delay -clock CLK_SAD -max 2.7~~
~~{getport ROW_IN}~~

*edit



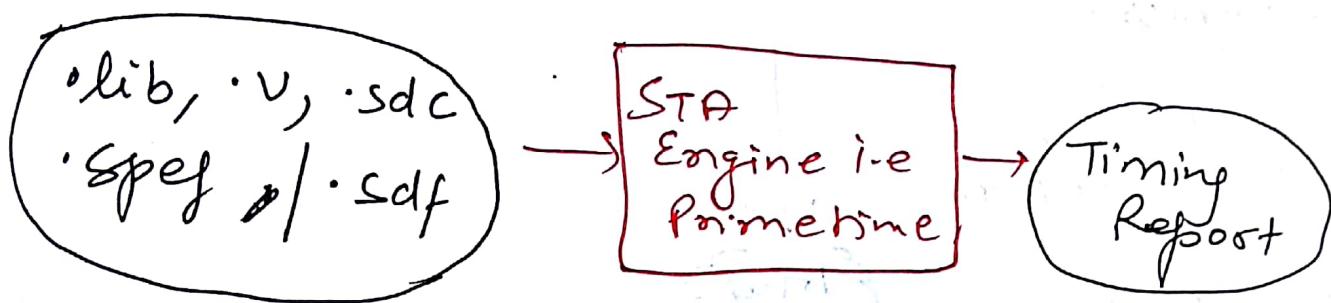
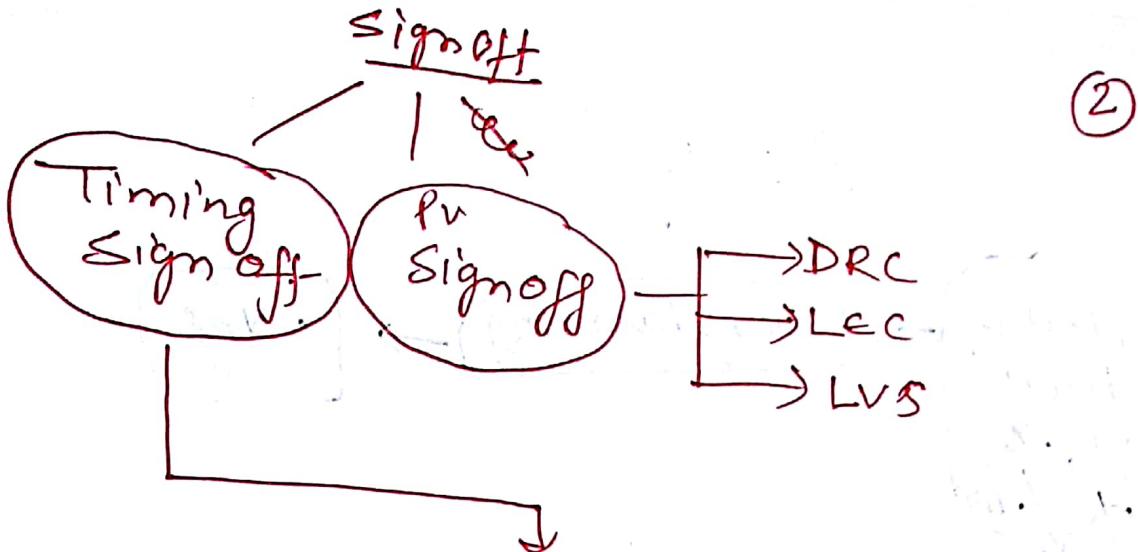
①

PD flow



Now this ·def is fed to routing tool e.g., STARRC or ~~Recong~~ DRC which will do RC extraction & ·spec is o/p.

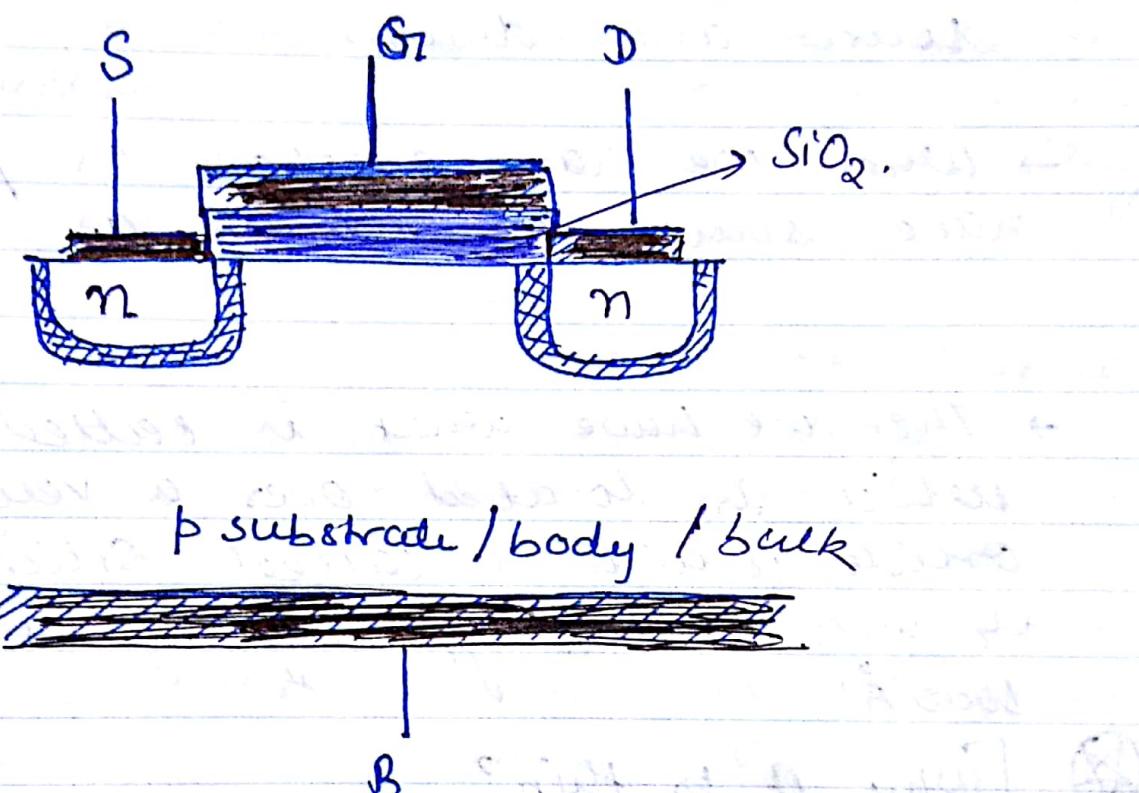
Signoff



Now this timing report will be analysed and we will see the slack & as per that we will fix by various ways in your design and then again run ~~an~~ post route eco flow which will again give new .def, now this .def is again used by DRC ~~extension~~ or STARRC and new .spec is released again this spec is fed to PT & new analysis will be done iteratively & finally you will close timing.

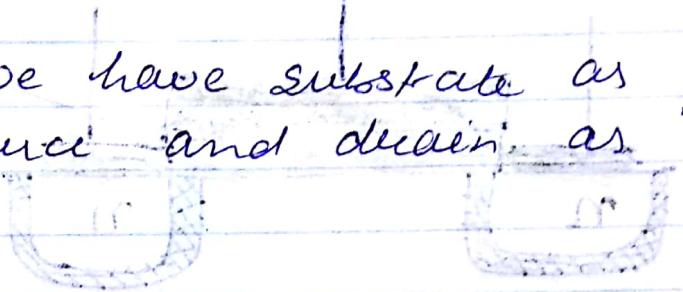
MOSFET

- BJT + MOSFET will together formulate family of active devices, covering almost 99.99% of entire circuitry.
- MOSFET → Metal Oxide semiconductor field effect transistor.



→ Now we will discuss quantitatively all the characteristics of MOSFET i.e. what a MOSFET is.

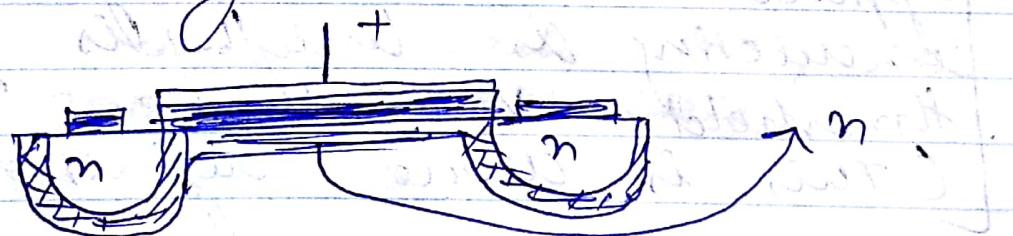
→ Consider, we will take this parent material i.e. wafer a p-type so this particular wafer is called a substrate or body.

- This is the material over which other device is going to be fabricated.
 - Now it would have two n-type wells we can call them source and drain.
 - We have aluminium contacts over source and drain.
 - When we have substrate as p then we have source and drain as n.
- 
- Then we have what is called as gate which is located over a very thin oxide which is called Silicon oxide or gate oxide typically of the order of 1000 \AA .
 - Why it is thin?
 - Bcoz we would like to have control over the surface by gate electrode.

- All the black colour ones are aluminium contacts.

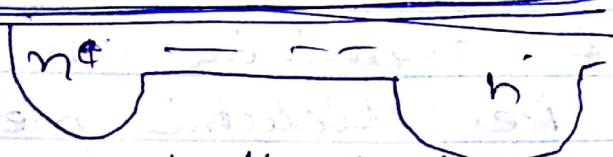
→ we all know p-type have holes in majority & electrons in minority. but overall it would have space charge neutrality. Now let us see what happens if we apply voltage w.r.t. body.

- It is just like a capacitor where b/w two conductive material i.e. aluminium on gate & aluminium on body there is a SiO_2 i.e. dielectric medium.
- If we apply a +ve voltage on gate w.r.t bulk now what happens it will attract electrons and repel holes so a limited number of minority carrier will deposit on surface now if we still ↑ voltage then further -ve charge will induced by immobile ion.



- So on application of +ve voltage it will become less p-type then neutral & then -ve. i.e. n-type.

- this is called inversion.
- This is important action of MOSFET on the surface. There are all surface devices.
- now this is open for conduction since n-well are also -ve so a channel is formed and the depth of channel



can be controlled by gate voltage.

$$\rightarrow V_g \propto W$$

→ The minimum voltage which is applied to make surface as conducting is body/bulk's called threshold voltage i.e. V_T
(This is device definition)

→ Circuit def: The voltage which will permit a certain amount of current to flow from source to drain.

→ The channel is formed by enhancing the conductivity of surface by applying voltage so it is called Enhancement type of MOSFET.

→ Since channel is n-type so it is called n-channel Enhancement type MOS.

→ These devices are initially non-conducting when the gate is not connected to any voltage. all three sources are off.

→ They can become on only after crossing the threshold voltage.

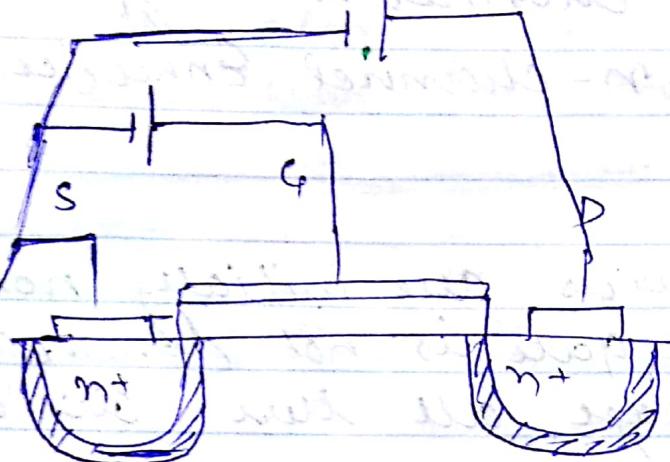
→ So these are very good switches so these are universally adopted in all gates of digital ICs.

→ So we can conclude that the current

$$I_{ds} \propto (V_{ds} - V_T) \quad \text{①}$$

→ Normally for this operation the bulk is connected to source; bcoz we don't want too many independent sources so we would like to minimize it by keeping source & bulk at same potential.

V_{DS}



The p-wells are shaded with just a few short horizontal lines per well.

Now current is going to depend upon $V_{GS} - V_T$ i.e. if $V_{GS} = V_T$ then $I_{DS} = 0$ so no channel formation

→ Drain is more +ve than Source.

When V_{DS} was 0, $V_{GS} = V_{GD}$ i.e. the depletion layer width at all places will be same.

\Rightarrow If we apply V_{DS} more than, $V_{DG} < V_{GS}$
 then the channel width will keep
 On \downarrow until $|V_{DG} = V_{GS}| = V_T$

$$\cancel{V_{DG} = V_{GS} - V_{DS}}$$

$$V_{DG} = V_{DS} - V_{GS}$$

\Rightarrow Let us say $V_{DS} = 0$ then both side
 voltage are same

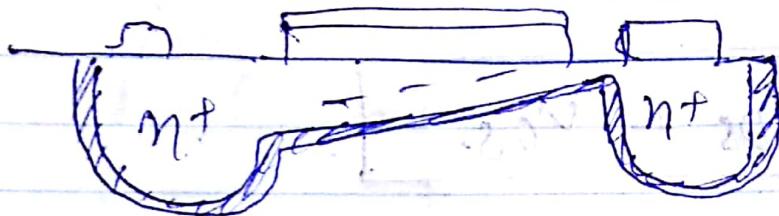
$$\text{i.e. } V_{DG} = V_{GS} - V_{DS}$$

Let us say $V_{DS} \uparrow$. it depends on a
 value ($V_{GS} - V_T$) then

$$|V_{GD} = V_T| \text{ so at that particular p.t}$$

we will have only V_T b/w gate &
 Drain i.e. entire thing will collapse
 block i.e. just channel & facets to
 form.

→ If we ↑ V_{GS} then the channel width will also ↑ but a point will come when channel will be completely closed. This is called pinched off. pt!



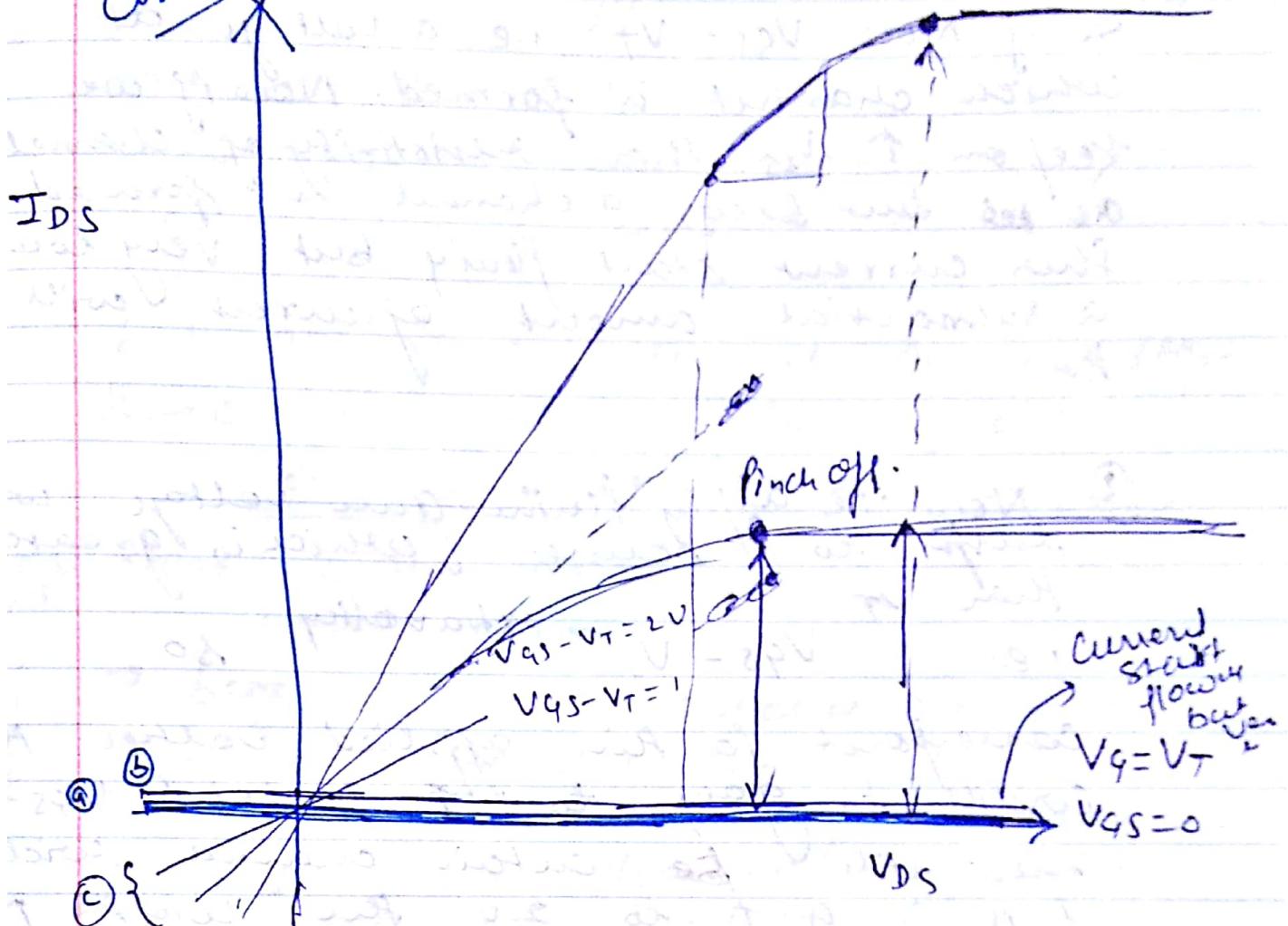
→ When $V_{DS} = 0$, then it will act as a mere resistor b/c the width is constant

I_{DS}

V_{DS}

so if we ↑ V_{DS} then the depletion width will ↑ & so at one side Resistor will also decrease & it act as voltage dependent resistor.

FET Characteristics



- There is no connection b/w source & drain i.e. resistance b/w source & drain is ∞ such i.e. e-type MOS is normally open.

If we plot b/w IDS & VDS , i.e. Resistance is ∞ so (a) is characteristic curve for $VGS = 0$ bcoz voltage current is 0 for whatever voltage you apply.

) Now,

So if Now $V_{GS} = V_T$ i.e a voltage at which channel is formed. Now if we keep on $\uparrow V_{DS}$ then resistivity of channel ~~at~~ ~~is~~ but becos a channel is formed. Then current start flowing but very low a substantial amount of current will flow.

③ Now we apply further gate voltage with respect to source. which is greater than V_T i.e $V_{GS} - V_T \rightarrow$ extra voltage. so

correspond to this applied voltage the width is going to \uparrow & so let $V_{GS} - V_T = 11$ there will be certain channel width & if it is \uparrow to 20 nm width & so on. So if we keep on $\uparrow V_{GS} - V_T$ then channel width is enhanced so it is called as enhancement type of Mosfet.

As long as $V_{DS} \leq 0$ the channel is uniform & it look like a normal resistor.

So if we keep on $\uparrow V_{GS} - V_T$ then width of channel is \uparrow & so we can conclude existence \downarrow Resist.

So this Mosfet can be used as voltage dependent resistor (VDR & VVR)

④ Show what happens when V_G & V_D both

So earlier the scene was

$V_{GS} = V_{GD}$ when $V_{DS} = 0$ i.e. both were shorted.

but now if we current some voltage here then we apply a voltage

$\underline{V_S - V_{GD}}$; Now channel width

pinch off starts ↓ at Drain,

⇒ bcoz this V_{DS} is opposing V_{GS} so that Net V_{DG} is formed. so what is Net V_{DS} that we should apply to make channel 0 at drain is $V_{GS} - V_T$ in opposite direction & this is called pinched off.

channel.

Original

$$\underline{\underline{V_{DS}}}, V_{GS} - V_T$$

Now, this instance is non-linear

Now current is saturated so it is called as saturation region for a lower value of $V_S - V_T$ current is same at lower value of V_{GS} .

A transistor (FET) is operated in Current Saturation Region. Below this region it is called as triode region.

Mathematical eqn

Triode Reg

$$\Rightarrow I_{DS} = K \cancel{V_{GS}} V_{DS}$$

$$\Rightarrow I_{DS} = 2K(V_{GS} - V_T) V_{DS}$$

Now if V_{DS} is $20V$ and said

$$2) \frac{I}{R_{DS}} = \frac{I_{DS}}{V_{DS}} = 2K(V_{GS} - V_T)$$

Square law nonlinear.

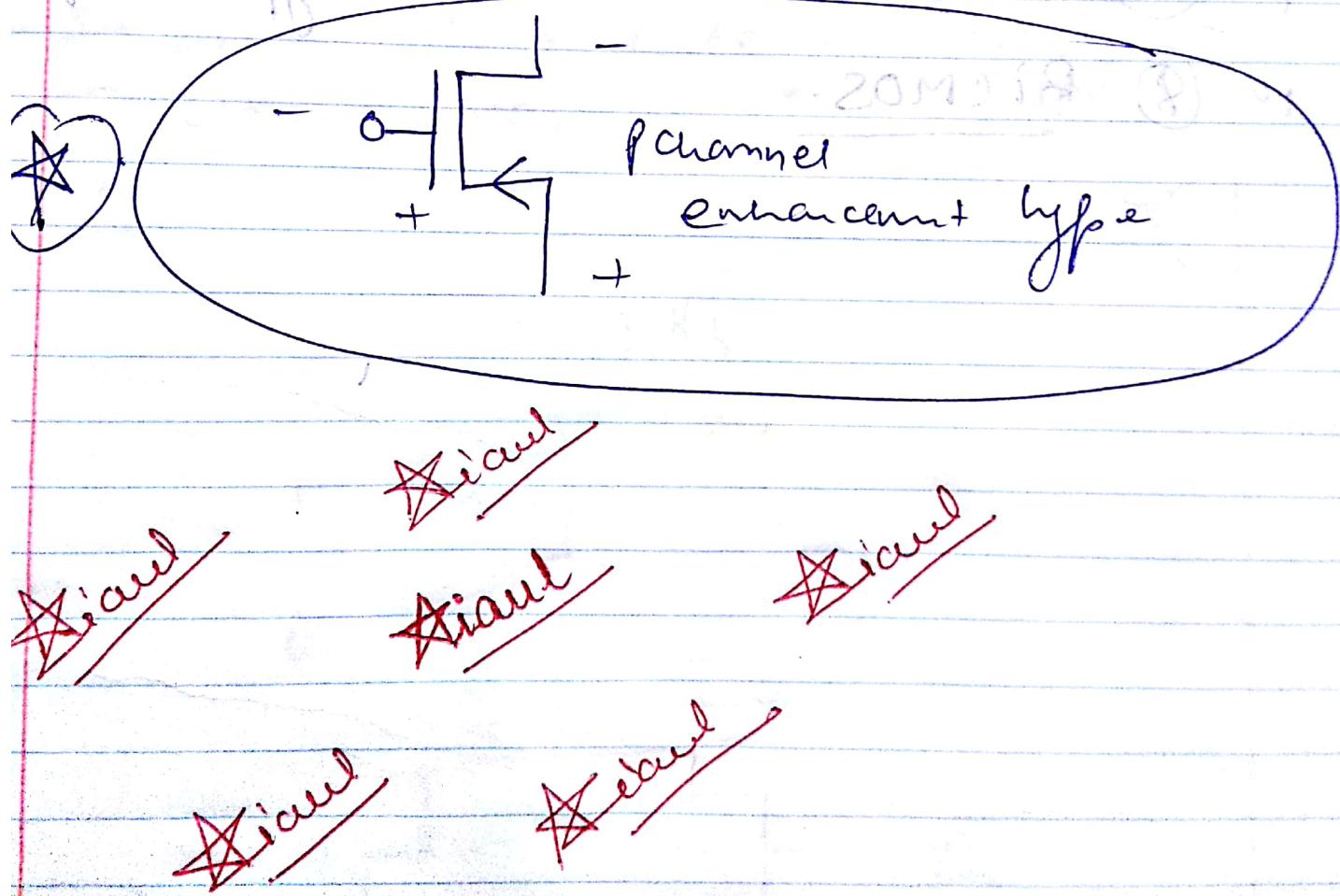
~~eqn~~
$$I_{DS} = 2K[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$$

It keeps on happening until we reach to
 $(V_{DS} = V_{GS} - V_T)$

$I_{DS} = 2K [(V_{GS} - V_T)^2]$



This characteristic is exactly same
as for p-type enhancement type
but only diff is in p-channel
MOS Substrate is n & bias will be -ve i.e. V_T is itself -ve. except this, every thing is same.



~~10th Sept~~

Preplaced Cells /
Special Cells

(4)

- Poe-placae

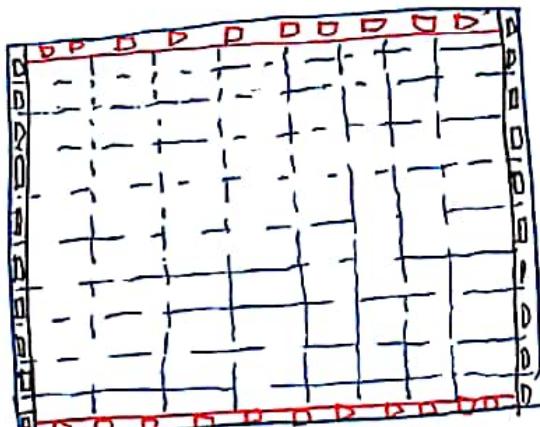
 - ① Endcap cells
 - ② Tap cells
 - ③ De cap cells (~~It is not~~ preplacae)
 - ④ Tie high / Tie low

special cells

 - ⑤ Spare cells
 - ⑥ Filler cells.

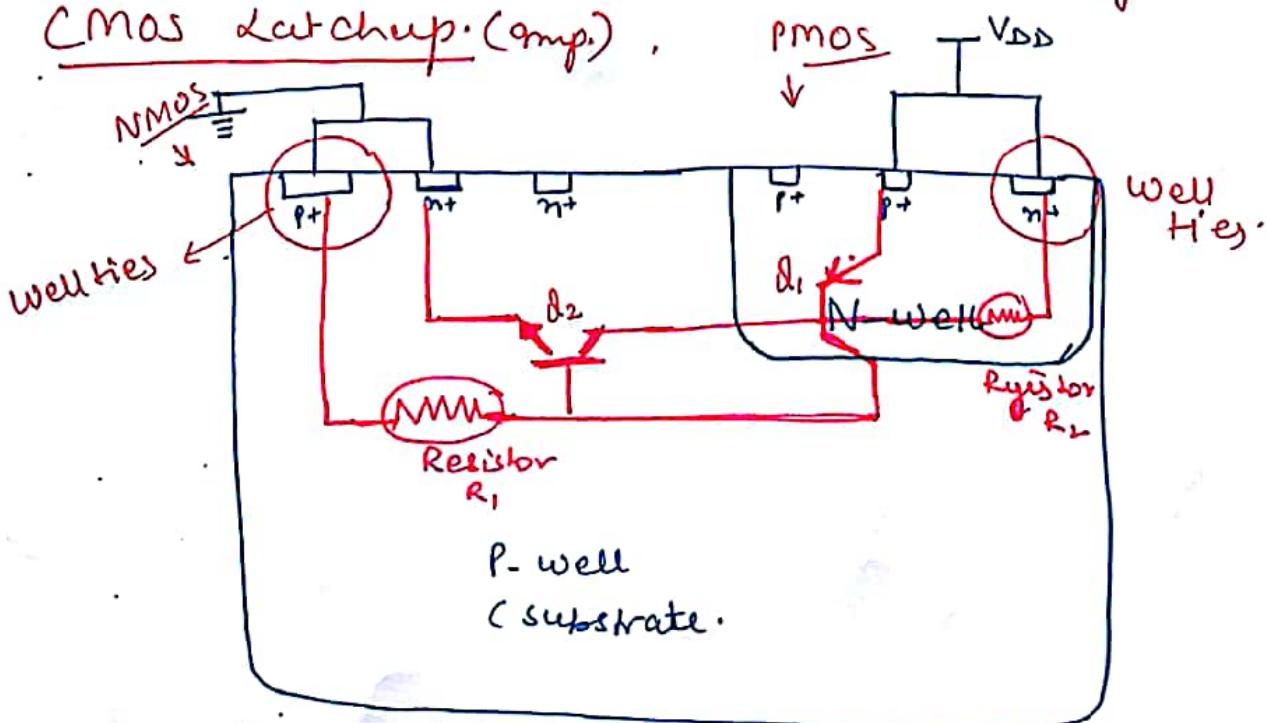
Physical only cells ... why?

1



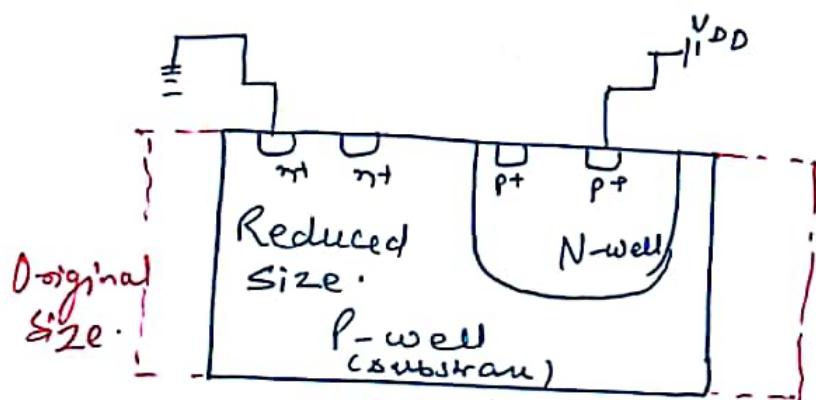
- ① End cap are placed to ensure tool that EOL has done.
 - ② Diff end cap cells are place for vertical & horizontal placement rows.
 - ③ Ensures cells are inserte properly with clean well.

② Now what is tap cells & why we use so before this we will look to a 2nd order effect called CMOS Latchup. (omp.) , PMOS $T^{V_{DD}}$

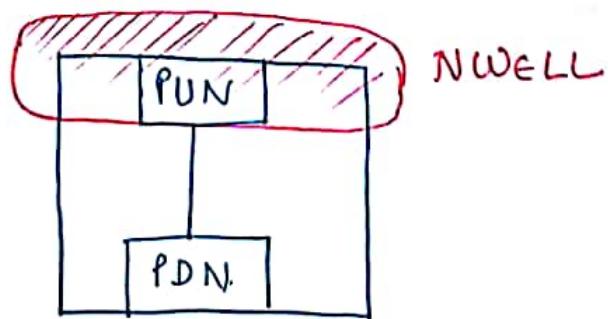


- If any wire is damaged; ---
- ① ~~Reduce the well & substrate resistance, producing lower voltage drops. (Add guard rings)~~
 - ② ~~Make sure power supplies are off before plug in.~~
 - ③ ~~Radiation free env.~~
 - ④ ~~TAP CELLS. (??)~~

SoC to accommodate more std cells. This type of library is called Tap-Less Library. To provide the much required well connection, cells known as well taps are placed at a regular interval.



Symbolic Representation of TAP-Less library



So, once floor planning is done we will take the ⑤ DEF out which will have Macros location, Blockages, pin location & some preplace cells location. Now we go for power planning. (route dep & deposit)

Power planning

{ Power planning is done as a part of floor planning only in which power grid N/W is created to distribute power to each part of design.

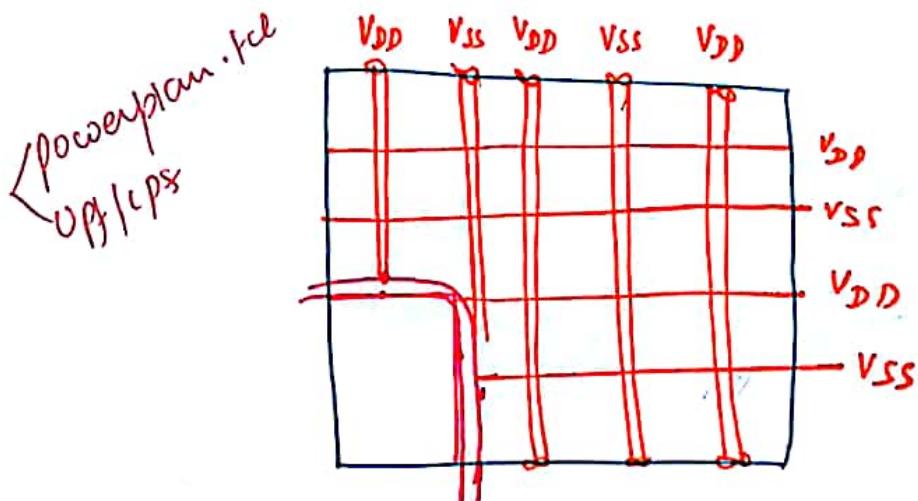
First concept of metal layers

Power planning can be done manually as well as automatically by tool itself. (6)

Terms: Rings: carries V_{DD} & V_{SS} around chip

Strips: carries V_{DD} & V_{SS} from rings across the chip.

Rails: Connect V_{DD} & V_{SS} to std cells.



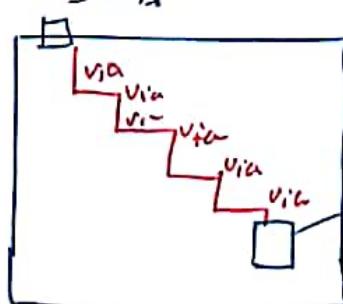
Why Mesh Structure ??

Ans: \downarrow IR drop.

IR Drop(what is ??)

$V = IR$ this this the voltage drop.

$$V_{DD} = 1.8 \text{ V}$$

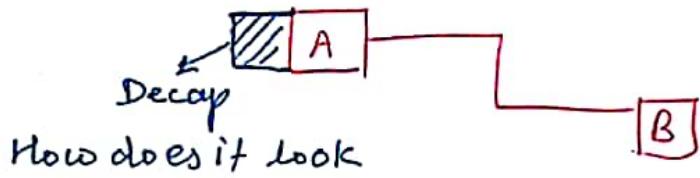


Let say that V_{DD} is in metal 7,8 & you want to connect here at M_2, M_3

So, IR drop will occur
So instead of 1.8 V you will end up with 0.9 V.

So, Here Decap will play a significant role. (Working of Decap here ??)

(7)



How does it look



get charged
& when
need it will discharge &
supply to A that's why it is
decoupling capacitors.

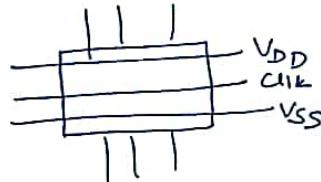
- ★ Once you are done with power planning do an IR analysis & see hotspot If IR drop is there then
- ① increase No. of power straps.
 - ② increase Width of power straps.

Placement

(8)

Placement is the process of automatically assigning correct position to predesigned cells on the chip with no overlapping such that some objective func. is optimized.

Std cell placement. It is designed in such a way



that power & clock connections run horizontally through the cell and other I/O leaves the cell from top or bottom side.

- 3 steps:
- ① Global placement
 - ② Legalization - check - legality
 - ③ Detailed placement - iterative placement & optimization

place-opt →

① HFN Synthesis. — Other than clock all other HFN nets like scan enabled reset etc are synthesized here. HFN are not synthesizable at logic synthesis.

Verify there should not be any

Set_ideal_N/W or set_dont_touch
except clock - why??

② Use Ideal clock.

③ Control congestion : what is congestion?

Scanned by CamScanner

How to remove or control congestion here?

(9)

- * cell padding
- * Max. utilization constraints
- * placement blockages.

↳ Scan chain Reordering is taken care?

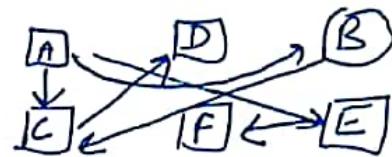
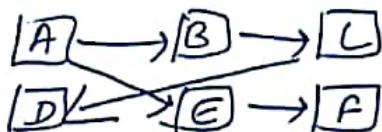


Scanned by CamScanner

How to remove or control congestion here? (9)

- * cell padding
- * Max. utilization constraints
- * placement blockages.

↳ Scan chain Reordering is taken care?



Scanner will have this info so its should be added before placement.

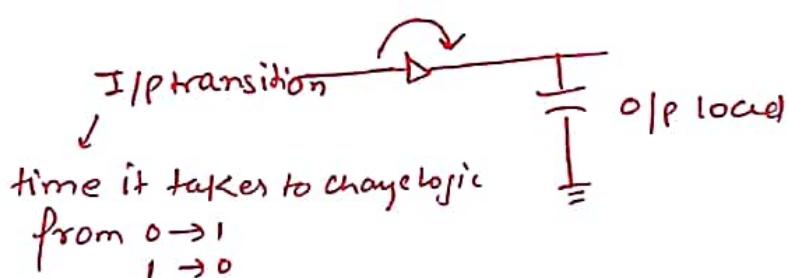
① congestion

② Timing - only setup.

Timing : (Very imp)

1st

Cell delay



Net delay: Net is a wire that connects two cells.



↳ It is calculated by parasitic extraction Methods & dumped in form of

SPEF → Std. Parasitic Exchange fmt.

Stage delay = cell delay + Net delay

Now guess it's there from where you will get this

(10)

Cell delay??
So, the ans. is tool will pick the values from lookup table in .lib.

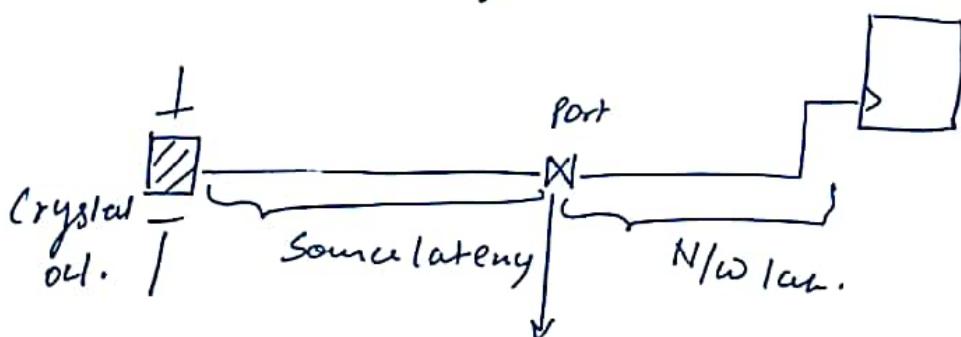
- lib will have different type of timing model like
 - NLDM → Non linear delay Model.
 - CCS → Composite current source
 - ECCS → Effective ..

For time being look into NLDM.

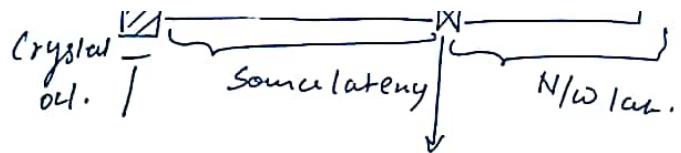
	0.1	0.2	0.3	0.4	MF
0.15	-	-	-	-	
0.25	-	-	-	-	
0.35	-	(○)	-	-	
0.55	-	-	-	-	

Clocks: ❤️ of a chip. (It is defined in SDC)

Create_clock - this is a command to define a clock so before going to this lets understand how clock is actually coming.



You will define clock.



You will define clock.

Scanned by CamScanner

To define a clock you should provide following (ii)
information.

i) clock source:

It can be a part of the design, or be a pin of a cell in-side the design.

ii) period

iii) duty cycle.

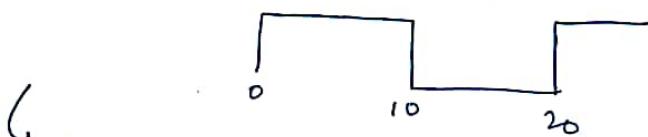
iv) edges.

e.g. Basic clock definition:

```
create-clock
  — name CLK
  — period 20
  — waveform {0,5}
??
  — get_ports SCLK.
```

If waveform is not given what option should it take.

Ans: - waveform {0, period/2}



So we think most of time we will have clock period of what we have defined but in reality it is not so bcoz of variation in P, V, T. & this amount of variation leads to concept of clock uncertainty.

Scanned by CamScanner

Scanned by CamScanner

Now New concept what is this P, V, T? ①

Onchip Variation (OCV)

Process Variation (P) → Variation in manuf. process
Supply Voltage (V) → due to IR drop
Operating Temperature (T) → due to local hotspots.

Relationships

- ① P↑ D↑
- ② V↑ DV
- ③ T↑ D↑

From Here we can see three main PVT corners.

SLOW	TYPICAL	FAST
{ 1.6V, 125°C ↳ mainly defence	1.8V, 27°C	2V, 0°C -90°C
* More prone to setup violation	* Above (Remind during Setup/Hold)	* More prone to Hold violation

So that's the reason for Uncertainty (U)

PreCTS -

$$\text{Skew} + \text{jitter} + (\text{margin}) \xrightarrow{\text{n.}} (\text{Remind during Crosstalk.}) \\ (10\%) + (2\text{ to } 5\%) + (5\%) \approx 20\%$$

PostCTS - jitter + margin

Types of clocks & Few terminology related to it.

① Main clock - create-clock ABC - (source) [get_ports] is given

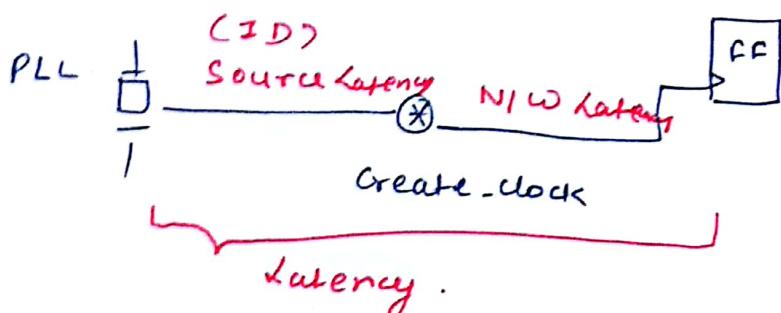
② generated clock - create-generated-clock xyz
- divide by (x)
- source mainclock [get_pins]

③ Virtual clock.

Why we need? discuss later. - create-clock xyz - period.
↳ No source is defined

Terms:

- ① Uncertainty ✓ {① Set-clock-uncertainty - setup
② Clock latency . ② similar 0.2 [get_clocks xyz] for hold.
↳ How it affect in
Setup/Hold??



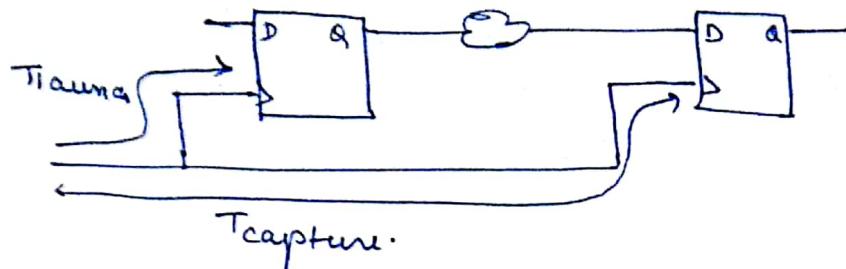
CMD:

① Set-clock-latency 0.8 [get_clocks xyz]
By default N/W latency.

② Set-clock-latency 0.8 - source [get_clocks xyz]

↓
Source latency .

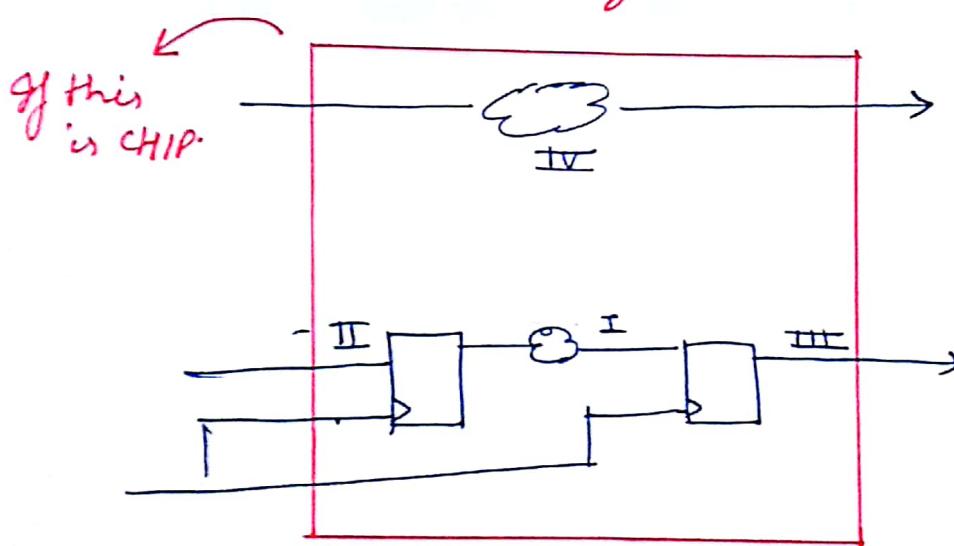
Skew: The difference in the arrival of clock signal at the clock pin of diff flops. (3)



Now why all these discussions ??

B/c in placement stage we are worried about setup violation so we need to understand concept of setup & hold & also Basics of STA.

So, 1st we will see Types of Timing path on which analysis is done.



4 types of timing path.

- ① Reg to Reg.
- ② I/p to Reg
- ③ Reg to O/p
- ④ pure combinational , I/p to O/p.

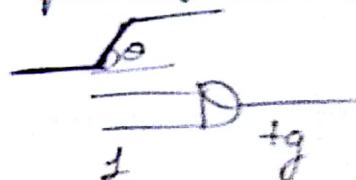
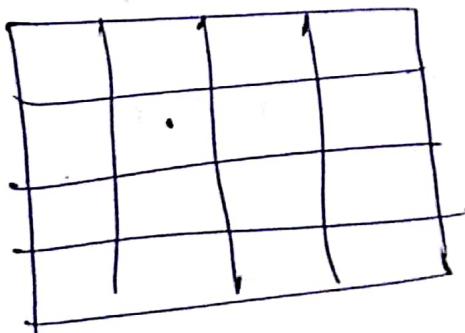
Timing Analysis

Dynamic

- Simulation based (Pspice)
- Highly accurate
- Slow runtime
- Not practical for whole chip.

Static

- formula based
- more pessimistic
- Very fast
- Most popular method for chip sign off.



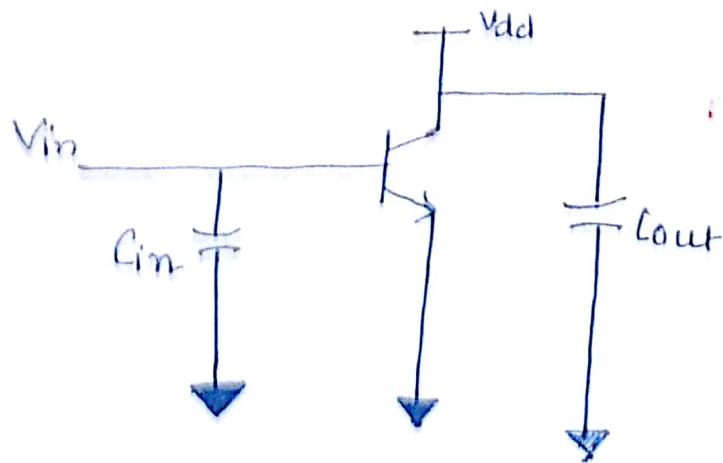
S - is curve i.e. slow

It would be written in table it is characterized by ~~fast~~^{is} guys using some tool, so it is very fast. So if it is SPICE it would have RLC values the tool can calculate using it $I_g = e^{-RC}$. So it's very fast

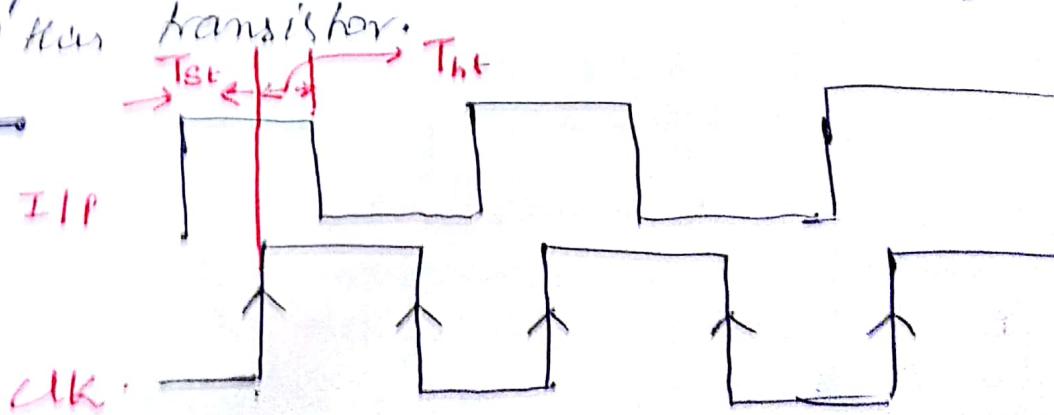
So always we worst case

Setup time: min amt. of time i/p must be stable before clock edge.

Hold time: It is the min. amount of time the i/p must be stable after the clock edge.



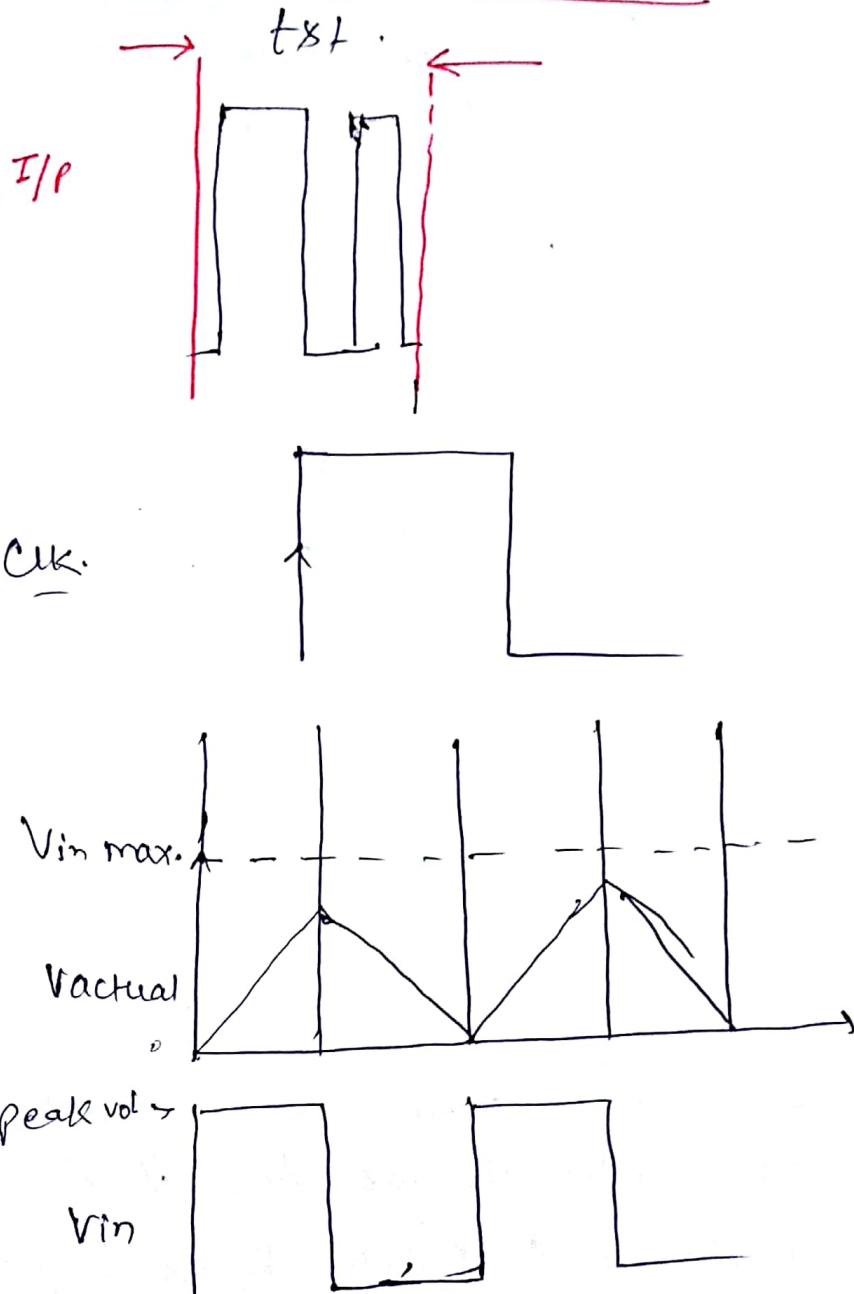
It has i/p capacitance seen from i/p terminal. so whenever any voltage is applied as V_{in} this voltage will charge the i/p capacitance & the charged capacitance will have some voltage now & whatever voltage this capacitor will have will be seen by the gate of the transistor.



So this T_{st} is the min. amount of time the data should be stable so that the transistor clk will see this i/p as it is let say it is 1 then now trans. will consider it as 1.

For my ckt to operate & provide reasonable o/p & charge the o/p capacitor this much amt of time the i/p should be present. So that the valid o/p will appear.

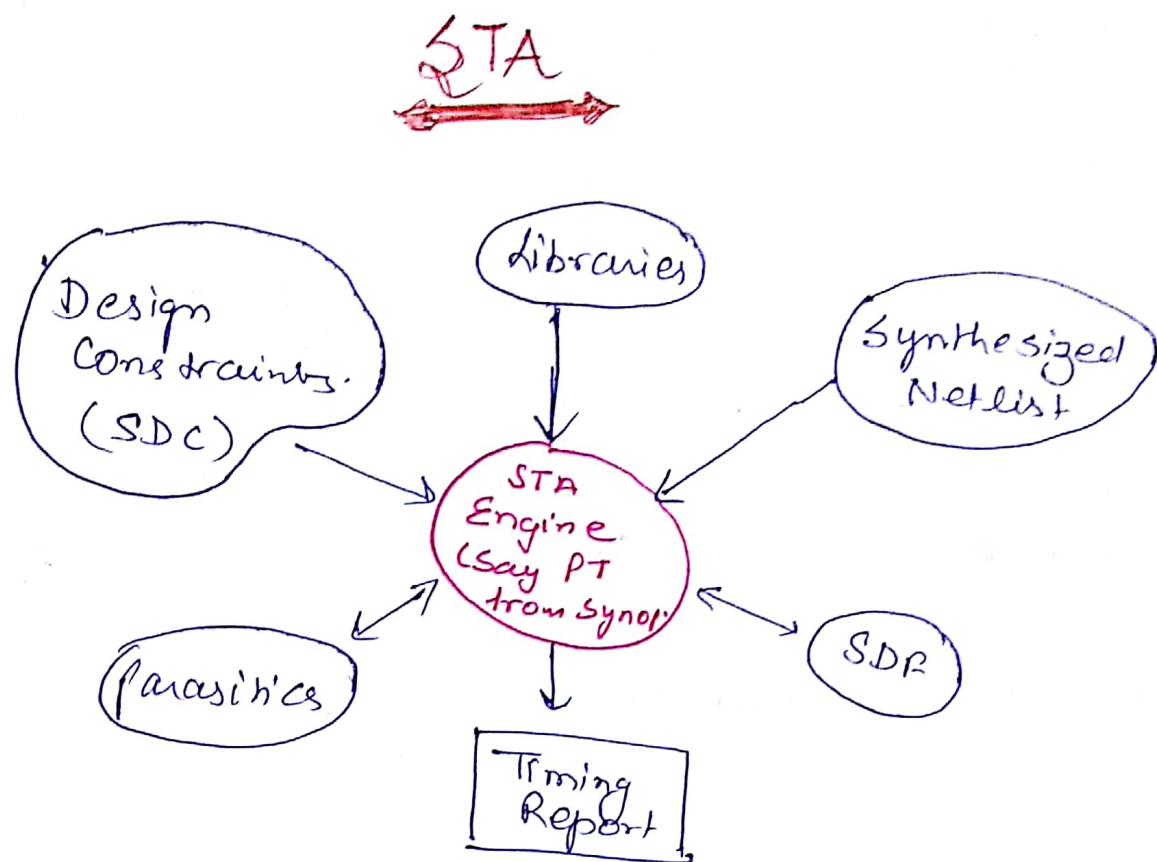
What will happen if we have setup violation?



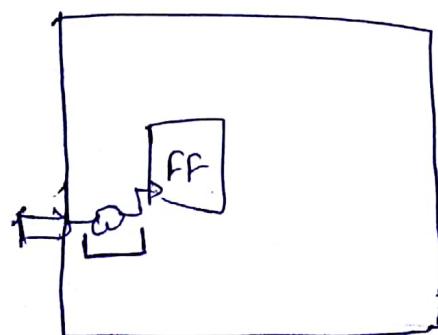
V_{in} - voltage provide by source
 V_{actual} - voltage on i/p capacitor

$T_{st} \rightarrow$ Setup time.

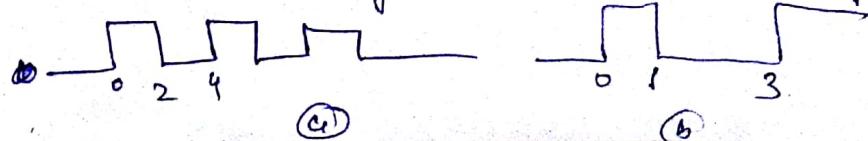
If my i/p is V_{in} & its peak voltage is then so if we apply square wave to the transistor which



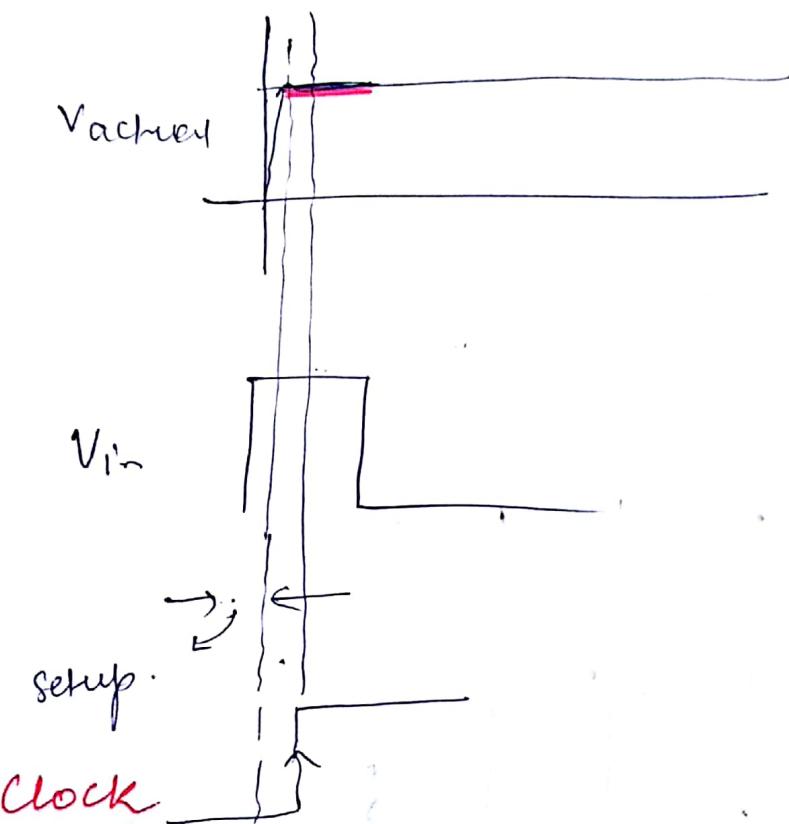
- ① → Synthesized Netlist (Timing closed Netlist); if it is timing closed Netlist then why are you doing STA here;
 Bcoz it is much more accurate.
- ② we can believe the synthesized Netlist.
- ③ There would be Std cell libraries or Macro libraries.
- ④ There is design constraints.



This clock should be constraints properly i.e what is clock period, waveform etc. let say period is 4 ns.



has $1/\mu$ capacitance so then O/P will be ~~exponential~~⁸⁰ waveform. so what will be suff. amt of time that it get charged and before it charge to V_{max} we are changing & discharging it really fast so what will happen the transistor will see the ip as integrated voltage over the period of setup time.



So what happen in general when V_{in} is applied so ideally capacitor will charge but it should req. min amount of time to reach V_{max} & if it ~~does not get charged~~ is fully charged then at clock edge that value can be read accurately.

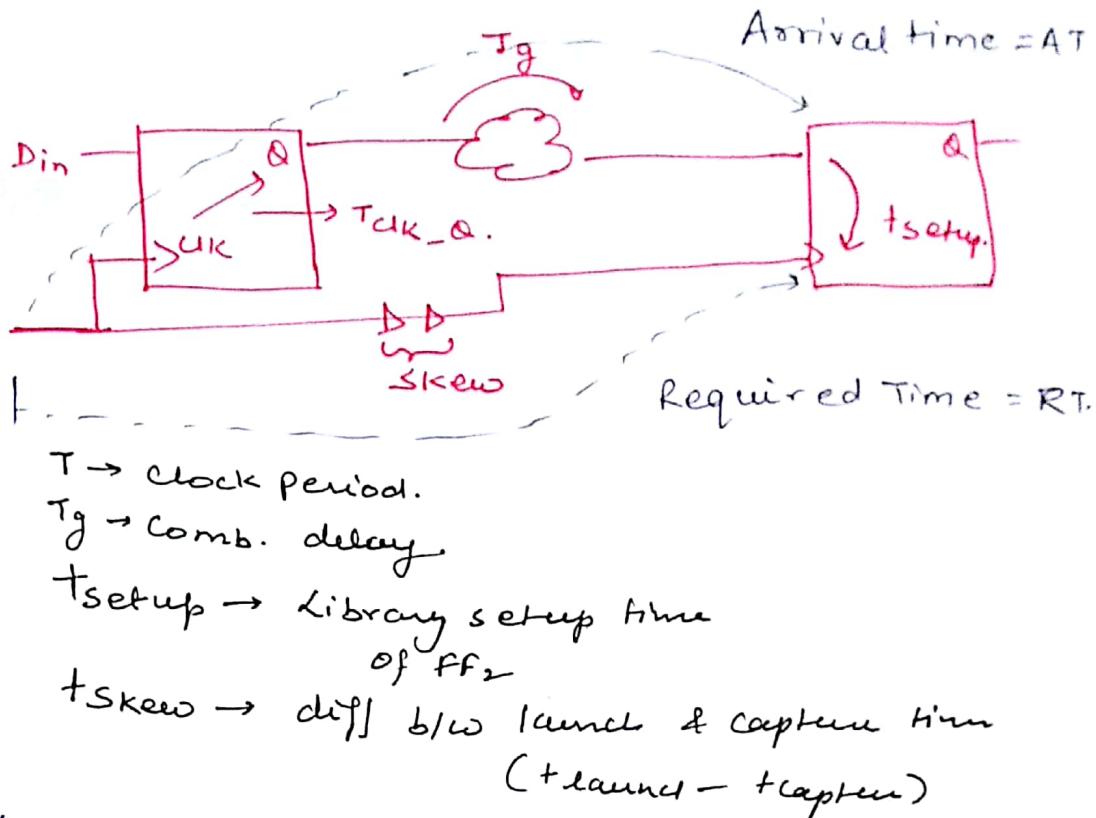
If my clock is in b/w this setup window it will reach an avg. value of over integration period of time.

So, avg value is obtained by $\frac{V_{in} \int t + \text{setup}}{\text{ }}$

so it may lead to metastability for example
it is an n-p-n trans. so it shows 140
& it should work in saturation & cutoff.
but since our logic is switching so high that
it may lead to avg value that is the transistor
will work in b/o saturation & cutoff & so the
o/p value will be linear amplification of i/p
or whatever trampen character is defined.

Equations for Setup & Hold Slack

(4)



So to satisfy setup criteria

$$AT \leq RT. \quad \dots \quad (1)$$

$$AT \rightarrow t_{\text{launch}} + t_{\text{c_q}} + T_g + t_{\text{setup}} \quad \dots \quad (2)$$

$$RT \rightarrow t_{\text{capture}} + \Theta T \text{ (period)} \quad \dots \quad (3)$$

Put (2) & (3) in (1)

$$t_{\text{launch}} + t_{\text{c_q}} + t_{\text{setup}} + T_g \leq t_{\text{capture}} + T$$

$$\Rightarrow \underbrace{(t_{\text{launch}} - t_{\text{capture}})}_{T_{\text{Skew}}} + t_{\text{c_q}} + t_{\text{setup}} + T_g \leq T$$

$$\Rightarrow T \geq T_{\text{Skew}} + t_{\text{c_q}} + t_{\text{setup}} + T_g$$

It can be concluded that setup slack depends upon freq.

$$\text{Setup slack} = RT - AT$$

(5)

It should be +ve to meet setup criteria so if -ve then try to $\downarrow AT$.

How to fix Setup:-

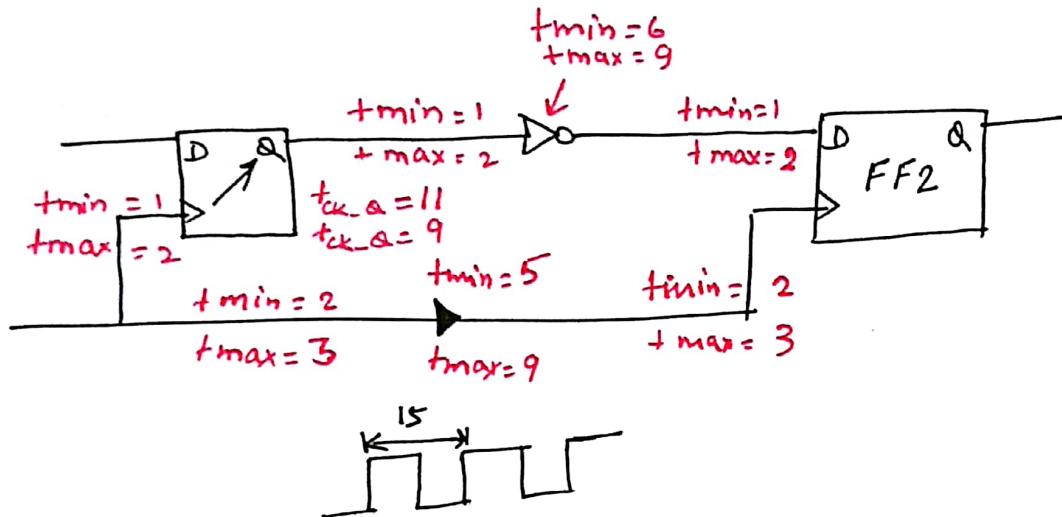
- (1) \uparrow drive strength
- (2) go for cells with less delays
LVT
- (3) \uparrow setup time of capturing ff.

HOLD ANALYSIS (don't bring

Time period in
picture & analysis,

STA Q1 do an analysis of ckt below for
Setup & Hold?

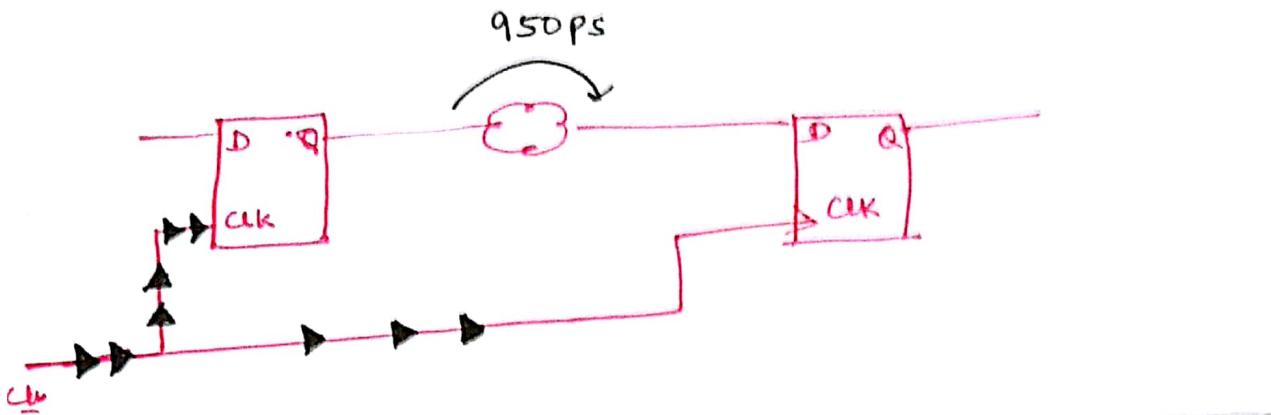
⑥



$$t_{\text{setup}} = 3$$

$$t_{\text{hold}} = 2$$

Rules: 2



(a)

$$T_{Clk-Q} = 5 \text{ ps}$$

$$T_{\text{setup}} = 3 \text{ ps}, T_{\text{hold}} = 2 \text{ ps}$$

$$\text{Time period} = 1000 \text{ ps}$$

$$\boxed{\text{Uncertainty} = 200 \text{ ps}} \rightarrow \text{Ignore for part (a)}$$

$$T_{\text{buffer}} = 10 \text{ ps}$$

$$T_{\text{comp}} = 950 \text{ ps}$$

$$\boxed{\text{derate} = 10\%}$$

\rightarrow Ignore for part (a)
4 (b)

(b) take uncertainty in a/c

(c) take both (derate + uncertainty)

$$\text{Setup Slack} = RT - AT$$

(5)

\$\bullet\$ It should be +ve to meet setup criteria so if -ve then try to $\downarrow AT$.

How to fix Setup:-

- ① \uparrow drive strength
- ② go for cells with less delays
LVT
- ③ \uparrow Setup time of capturing ff.
- ④ Cell padding.

HOLD ANALYSIS (don't bring

Time period in
picture & analy.

$$AT \geq RT$$

$$\Rightarrow \text{RELEASED } AT = t_{\text{launch}} + t_{c-q} + T_g * - T_{\text{hold}}$$
$$RT = t_{\text{capture}}$$

$$\Rightarrow t_{\text{launch}} + t_{c-q} + T_g - T_{\text{hold}} \geq t_{\text{capture}}$$

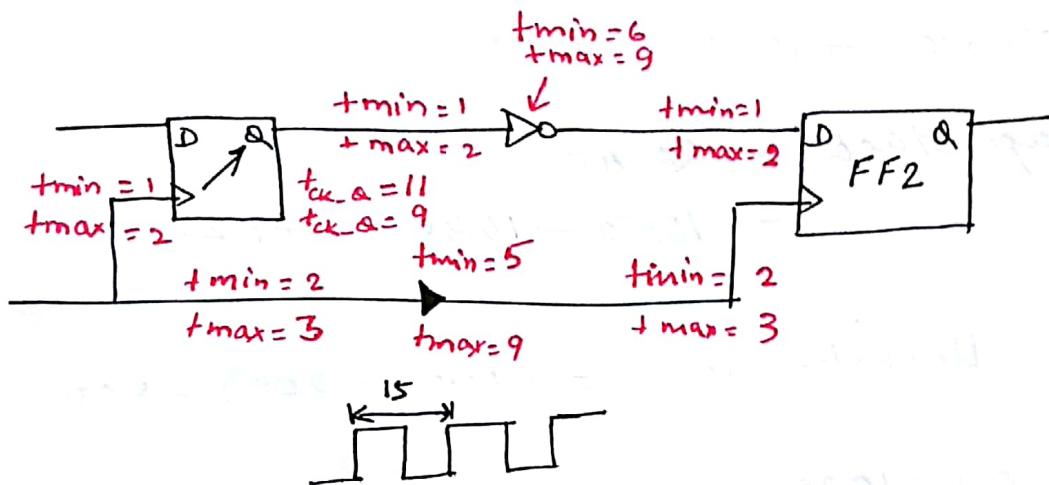
$$\Rightarrow \boxed{T_g + t_{c-q} \geq T_{\text{skew}} + T_{\text{hold}}} \quad \leftarrow (t_{\text{launch}} + t_{\text{capture}})$$

Catch = Hold is not dependent on
freq..

How to fix Hold Hold Slack = $AT - RT$

- ① Add delays (End pt. buffering)
- ② LVT to HVT

STA Q1 Do an analysis of ckt below for setup & hold? ⑥



$$t_{\text{setup}} = 4$$

$$t_{\text{hold}} = 2$$

Setup	Hold
$(AT)_{\text{max}} = 2 + 2 + 11 + 9 + 2 + 4$ $= 24 + 4 + 7 + 8$ $(RT)_{\text{min}} = 30$ $= 2 + 5 + 2 + 15$ $= 24$	$(AT)_{\text{min}} = 1 + 1 + 6 + 1 + 9$ $= 18$ $(RT)_{\text{max}} = 3 + 9 + 3 + 2$ $= 15 + 2 = 17$
$\therefore \text{Setup slack} = -6$	$\text{Hold sh} = 1$

2/a Soln

$$AT = (8 \times 10) + (5) + 950 + 3 \\ = 88 + 950 = 1038$$

$$RT = (5 \times 10) + 1000 = 1050$$

$$\text{Setup slack} = RT - AT$$

$$= 1050 - 1038 = +12$$

(2/b) Uncertainty $= (1000 - 200) = 800$

$$\therefore AT = 1038$$

$$RT = 1050 - 200 = 850$$

$$\therefore \text{Setup slack} = 850 - 1038 = -188.$$

(2/c) due to effect.

$$(AT)_{\max} = 8 \times 11 + 5 + 950 + 3$$

$$= 88 + 8 + 950$$

$$= 96 + 950$$

$$= 1046$$

$$(RT)_{\min} = 8 (5 \times 9) + 5 + 950 + 3$$

~~$$= 53 + 950$$~~

~~$$= 1003$$~~

$$\therefore \text{Setup slack} = -43 \text{ ps}$$

$$(RT)_{\min} = (5 \times 9) + (1000 - 200)$$

$$= 845 \text{ ps}$$

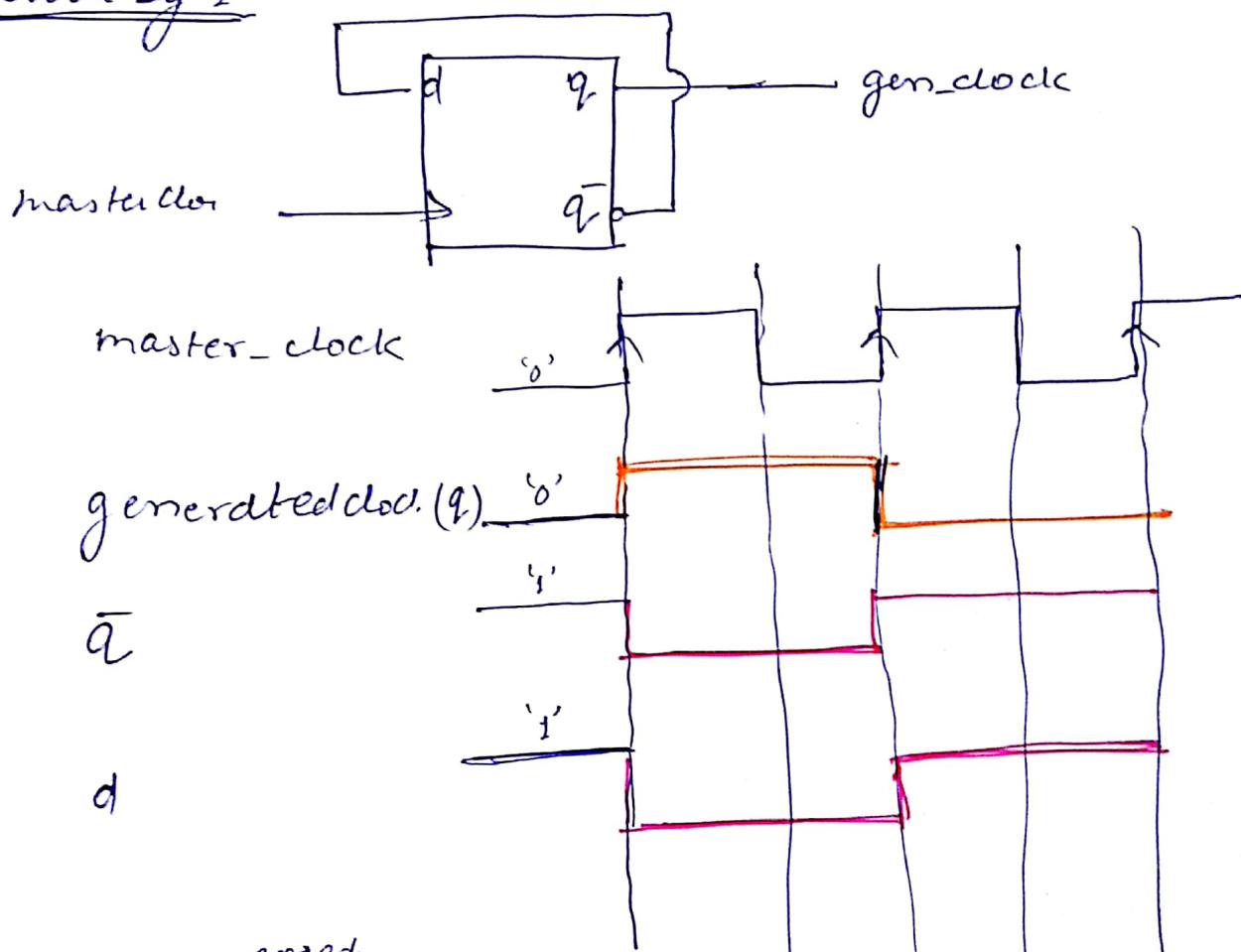
$$\therefore \text{Setup slack} = 845 - 1046 \\ = -201 \text{ ps.}$$

Generated clock

Today's SOCs (System on a chip) contain heterogeneous devices within the same chip. This could include very high speed processors as well as low speed processor. These elements working at diff speed are usually trigger by diff clocks.

⇒ clocks will not propagated beyond ff & port 80 to make sure the other clock get created we use create-generated clock.

divide by 2



⇒ so for 1st posedge of clock $d=1$ is pushed to q & 1st bit

1

⇒ so in 2nd posedge $d=0$

① NAME

Address with phone
numbers & valid
email id

② CAREER OBJECTIVE

③ WORK EXPERIENCE (* if going as fresher then
not needed)

ORGANISATION : - - - - -

POSITION : - - - - -

DURATION : - - - - -

④ PROJECTS : Here you try to mention your
Physical design projects & it should be like

Project 1: Name

Type of services:

Team size:

Title :

Memory & I/O pins:

No. of clock:

Process Technology

Complexity :

Tools used:

Responsibilities:

1.
2.
3.

⑤ Tools AND LANGUAGES SKILLS: Here you can
mention about tool & languages you know.

⑥ Technical skills:

⑦ Academic Details

⑧ Academic Projects

⑨ Soft Skills / Co-curricular Activities

⑩ Personal Info.

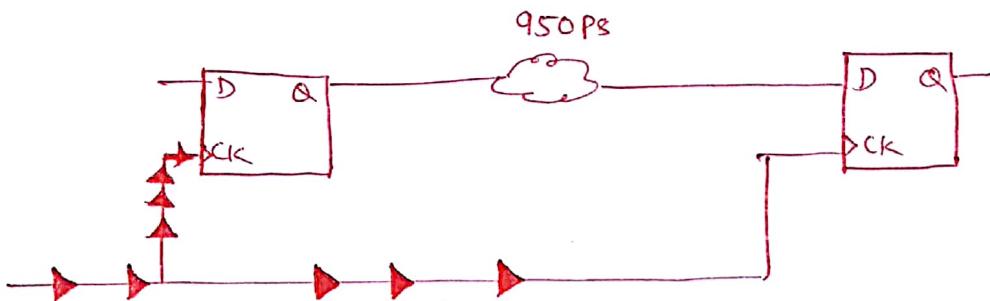
VLSI Guru

PHYSICAL DESIGN EVALUATION

TEST

LEVEL:I (BRAIN WARM UP 😊)

- Ques:1 Explain Physical design flow and also mention the input and output files in each stage.
- Ques:2 Explain the content of .lib, .lef and .def.
- Ques:3 What are guidelines of macro placement? Explain need of flyline analysis.
- Ques:4 What are various sanity checks in P.D.
- Ques:5 What are factors on which cell delay depend? What is NLDM?
- Ques:6



$$T_{\text{comb}} = 950 \text{ ps} ; T_{\text{CK-Q}} = 5 \text{ ps} , T_{\text{setup}} = 3 \text{ ps} , T_{\text{hold}} = 2 \text{ ps}$$

$$\text{Time period} = 1000 ; T_{\text{buffer}} = 10 \text{ ps} ; \text{Uncertainty} = 200 \text{ ps} ;$$

$$T_{\text{comb}} = 950 \text{ ps} \& \text{ derate} = 10\%.$$

Analyse if there is any analysis violation and also mention value of setup and hold slack.

- Ques:7 What is Virtual clock. Write command to generate a V.C of time period 20ps & 50% duty cycle.
- Ques:8 What is difference between Halos and Blockages?
- Ques:9 Explain setup and hold time with help of waveform.

- Ques:10 what are timing Exceptions? why they should be given as a constraint.

LEVEL II (BRAIN BOOST UP) Ques:11 what are preplaced cells . Explain usage of them in detail. (2)

Ques:12 NDR is non default rule for routing . Why we apply these before placement.

Ques:13 Why we can solve hold violation in CTS Stage only.

Ques:14 What is Antenna Violation and what are various reducing techniques.

Ques:15 Explain the terms mention below and also how to reduce them

1. Electro Migration
2. Congestion
3. Crosstalk.
4. CMOS latch up.

Ques:16 What is skew, insertion delay and latency?

Ques:17 What is uncertainty ? Explain inter clock uncertainty in detail.

Ques:18 Explain clock tree optimization . Explain different ways to minimize skew.

Ques:19 Explain crosstalk delay and crosstalk noise.

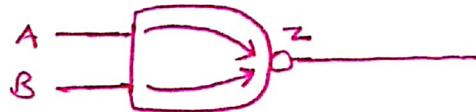
Ques:20 What is scan-chain Reordering.

LEVEL III (BRAIN DRAIN ☹)

Ques:21 Can there be setup and hold violation on same path . Support your ans with explanation.

Ques:22 What is content of clock specification file (clockspec.tcl) . Explain meaning of target skew , global skew and local skew.

Ques: 23 On which factor a cell delay depends. ③
So for following NAND gate there is a transition from $A \rightarrow Z$ and also $B \rightarrow Z$ so which transition should be considered for delay



calculation. Explain.

Ques: 24 Draw waveform for following

- create_clock - period 12 - waveform {0.3 0.4 0.8 1.0} JTAGU
- create_clock - period 10 - waveform {5 10} [get_ports FCLK]

Ques: 25 Can a new clock, that is a master clock, be defined at the output of the flip flop instead of generated clock. Support your answer with valid explanation.

Ques: 26 What is virtual clock?

Ques: 27 What is diff between Retention and Isolation cell.

Ques: 28 How prime time will report if you apply

- set_false_path
- set_disable_timing

to any part of your design.

Ques: 29 Explain mmmc. Which parasitic interconne is checked for setup & hold.

Ques: 30 Explain OCV, Derate and CRPR (CPNR). Can i apply derate on timing checks (i.e. library setup & hold values)

Basics of Physical Design

Parity → Zigzag

①

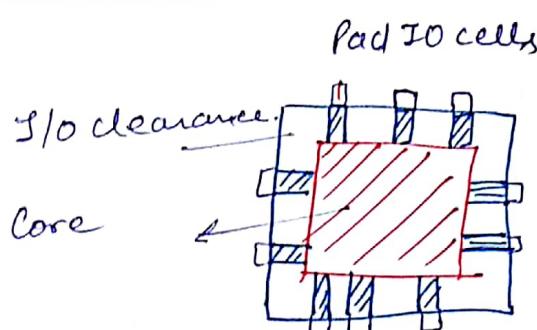
Floorplanning: It is very first step of physical design flow and it take care of placement of macros, pin placement etc. & basically done to use area intelligently.

Now a days power planning is also done as a part of floorplanning only so it can also be taken care during FP.

Implementation of floorplan includes

- Defining **core area**
- Creating & placing power pads
- Placing IO pads/ports & macros
- Modifying orientation of macros
- Implement parameters a P/G grid a/c to given
- Defining placement & routing blockages.

Core & Die



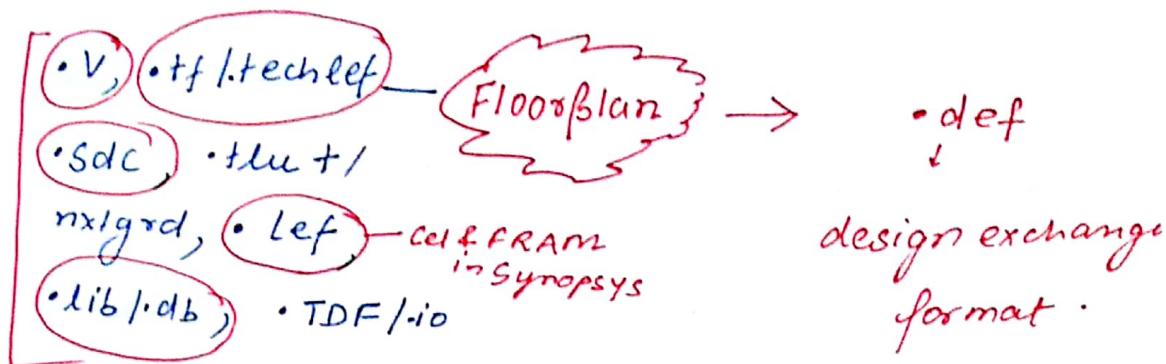
① Core area = Std cell area + (MACROS + HALOS/
KEEPOUTNREGS)
Total utilization
?? Std. cell utilization

② Die area = Core size + I/O core Clearance + Pad Area

③ Std cell Utilization = Netlist Area / Allocated die area.
(Std. cell area)

Data Required for Floor planning.

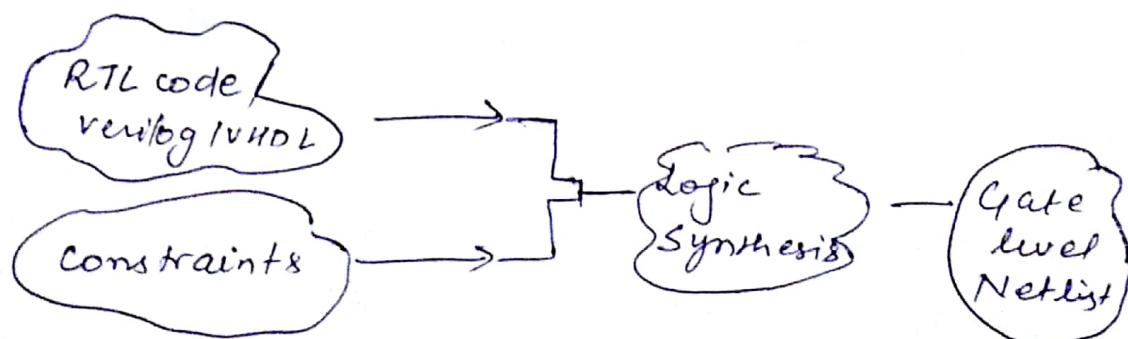
(2)



* Apart from this we can also use "def" if it comes from top level.

Contents of g/p files

V → Synthesized Netlist / Gate level Netlist.



Here what synthesis tool will do it will convert the RTL to ~~gate level~~ Boolean equation and then this Boolean equation to library mapped gate. Here optimization of gates is done to meet setup time [in built algo. will be there to optimize e.g. let us take a not & an and makes a NAND].

Technology file.
.tf / .techlef:

(3)

Technology file defines basic characteristics of cell library pertaining to a particular technology node. They are units used in the design, graphical characteristics like colour pattern, line styles, physical parameters of metal layers, coupling capacitances, dielectrics values, device characteristics, design rules.

Units of power, voltage, current etc are defined in technology section.

The color section defines primary colors that a tool uses to display design in the library. Different layers definition like its current density, width etc are defined in layer section.

Similarly several other specifications like metal density, design rules that apply to design in library, place and route (P&R) rule, slot rule, resistance model are defined in their respective sections.

④

*sic → Synopsys Design constraints:

It will contain all the clock related info to constraint a design. It includes clock freq, rise & fall time, skew & insertion delay etc.

⑤ Timing star

* lib → logical libraries: Timing info of std cell, soft macros, Hard macros ; design rule like max trans, max cap, hold time max fanout etc. & also power info.

⑥ Timing placement)

• lef → layout exchange format.

• lef → Physical libraries.

It contains all the physical info of std cells, macros, pads etc, pin location, height of placement rows, preferred routing direction, pitch of routing track, Antenna rule etc.

⑦ Coming to Synopsys it will have physical info in two views i.e CEL & FRAM

CEL: It has all layout info & it is used at the time of tapeout.

FRAM: It is abstract view & basically used in P&R.

* tlu → It has R_q C_{net} of per unit length & it helps in timing calculation.

* tdf → It has pad location & pin locations generally used by top level guy.

⑤

After setting up all the req. data the very first thing we will do, we will perform a sanity check.

① Check_design:

Syntax

(check_design)

- checks pre-defined stage

placement, clock,
route,

- ↳ It will give warning if you have floating pins
- ↳ PG net is not defined in UPF
- ↳ High fanout nets > (some threshold)

② Check_timing

↳ no-drive, no-input-delay,

Path

★ unconstrained

* Cross clock, gated clock, loops, multiple clock on same pins, no-clock etc.

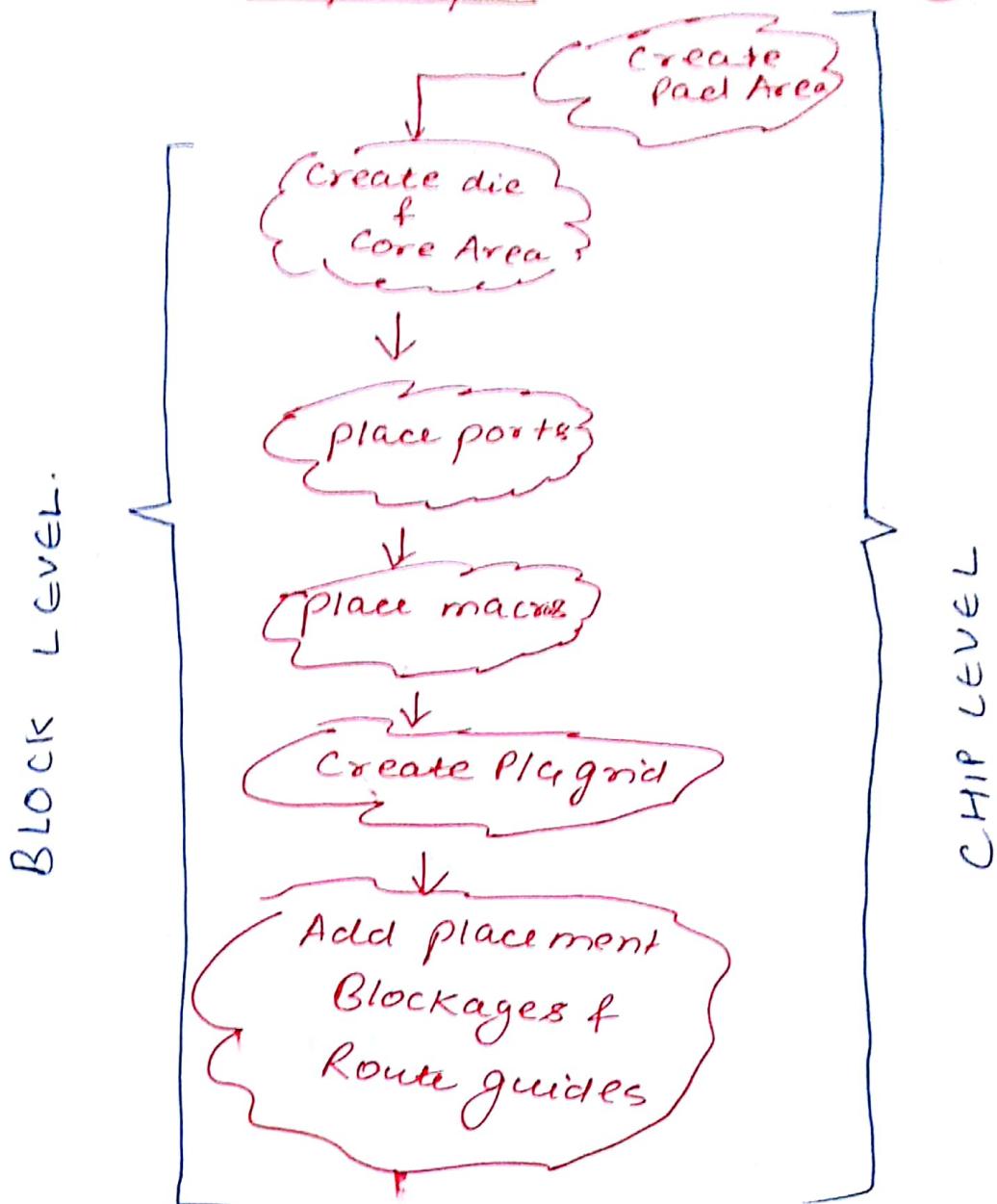
③ Check_netlist

↳ checks the netlist for any connectivity errors or violations & issue warning messages accordingly.

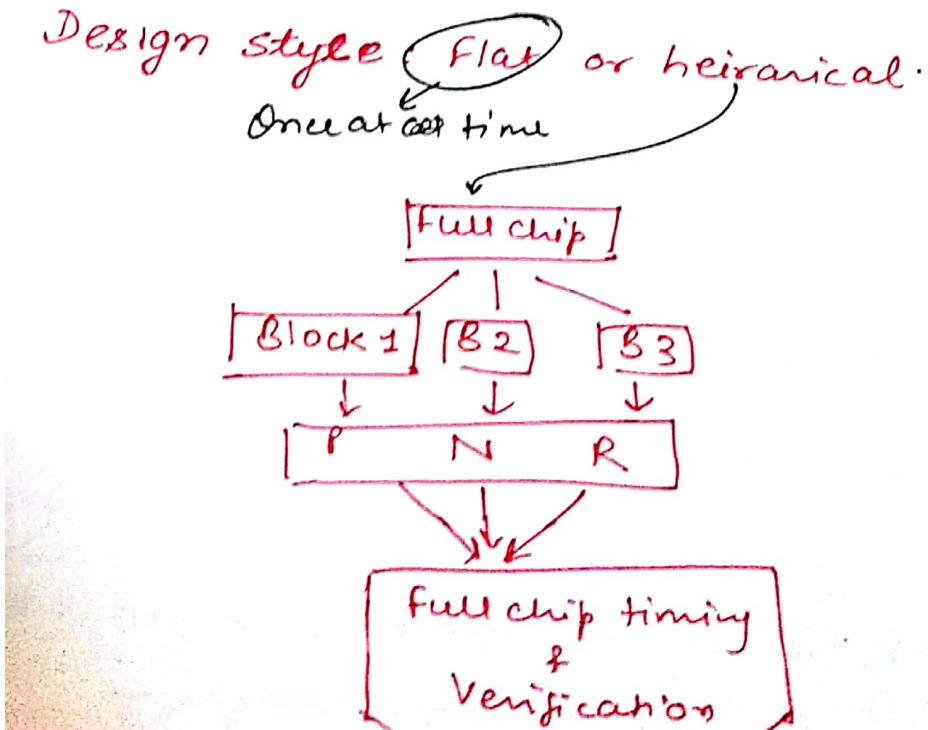
★ Once you get a waver that your sanity test has passed you can move forward otherwise you have to report to synthesis team.

Floorplan flow

(b)



Design style Flat or hierarchical.
Once at a time



Types of floorplan

(7)

① Channeled FP: It contains spacing b/w blocks for the placement of top level Macros. * Spacing enables the tool to place std cell b/w blocks.

② Abutted FP: Block are touching & tool does not allow macro cell placement b/w blocks.

So, now we can start with FP, so if you are using ICC you can use command

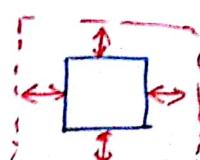
~~icc~~ [create - floorplan - ~~xxxxxx~~] & in ICC2 you can use ??

~~icc~~ [initialize - floorplan ... ~~xxxxxx~~] ??

These stars are Nothing but floorplan switches
 ① core utilization (Let say it is 0.8 which means 80% is use for placement of Macros & other preplaced cells) ??

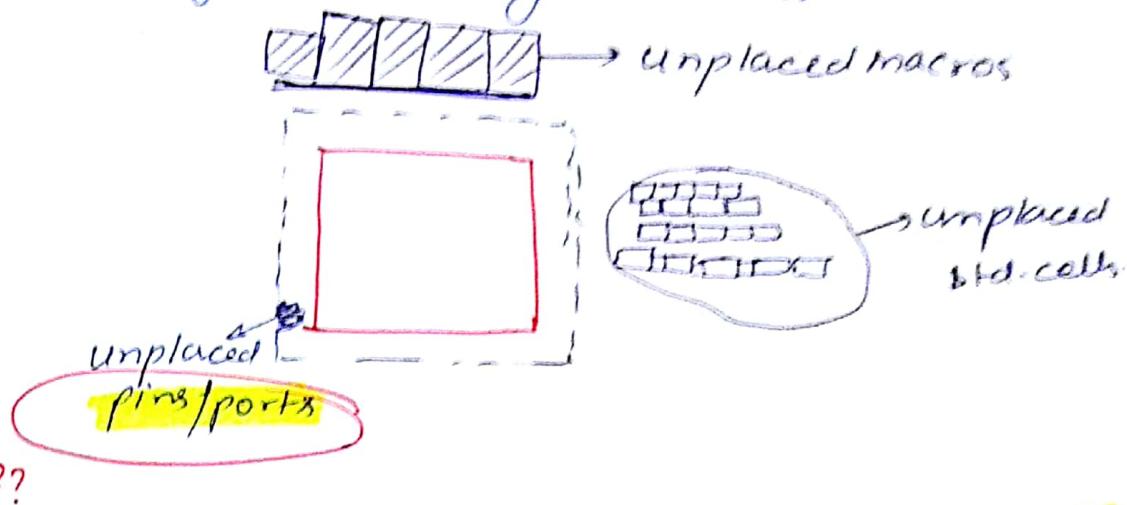
② aspect_ratio: Height / width. (If it is 1 means square shape)

③ I/O clearance core to die distance



e.g. create_floorplan - core_utilization - left_top
 - aspect_ratio .

Once you run above command or else you can do the same using GUI way also you will get something like this.



So, as per flow Now we have to do **pin placement**, again we can do with command or GUI;

Most of the time pin placement can easily be done by writing a small script so it's recommended to answer interview that it was already done from top level guy.

Once done you can do a check on this using command

Check - pin - placement

So once, pin placement is done our main task is to Macro placement. Placement of Macros is very critical task so we need to take care of few things.

(9)

Guidelines

- * do a flyline analysis and see the pin connectivity
- * See the hierarchy of the macros and those belonging to same family should be placed closed.
- * Place the macros nearer to core boundaries. Recommended but why?
- * leave a small spacing around the Macros. called as halos in cadence terminology & keepout margin in synopsys terminology.
- * pins of macros should be accessible.
- * Give proper spacing b/w the macros.

Formula for channel length calculation

$$\text{? ask in routing.} \quad = \frac{\text{No. of pins} \times \text{pitch}}{\text{available } \frac{1}{2} \text{ layer), (Allowed tracking metal}}$$

Once you follow all the above mentioned guidelines you will have your macros placed. Now go to properties of macros & make its fixed attribute == true. ?? why?