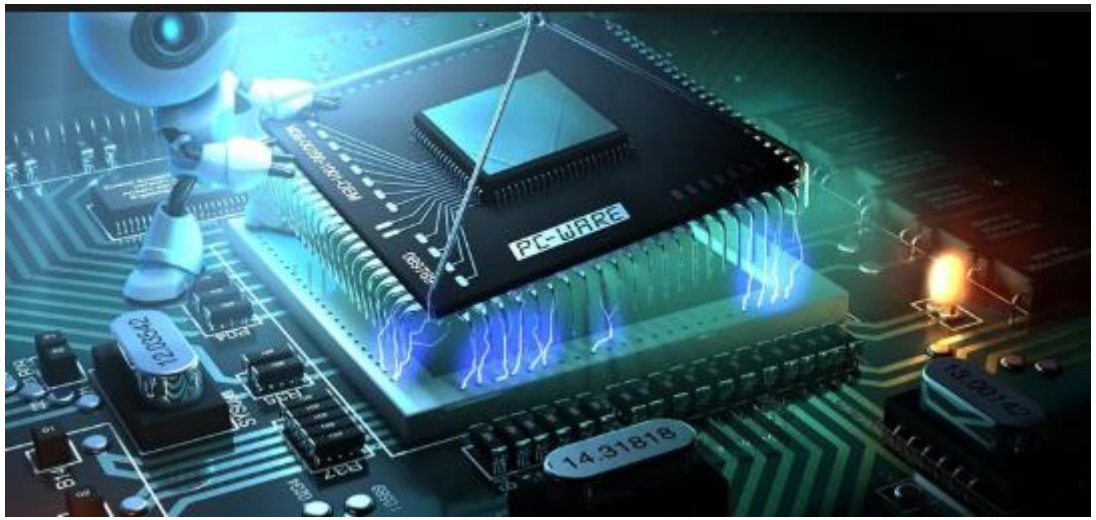
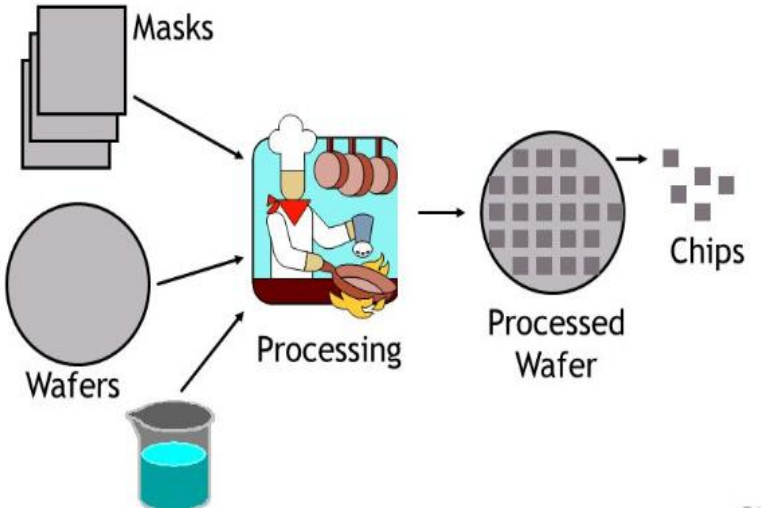
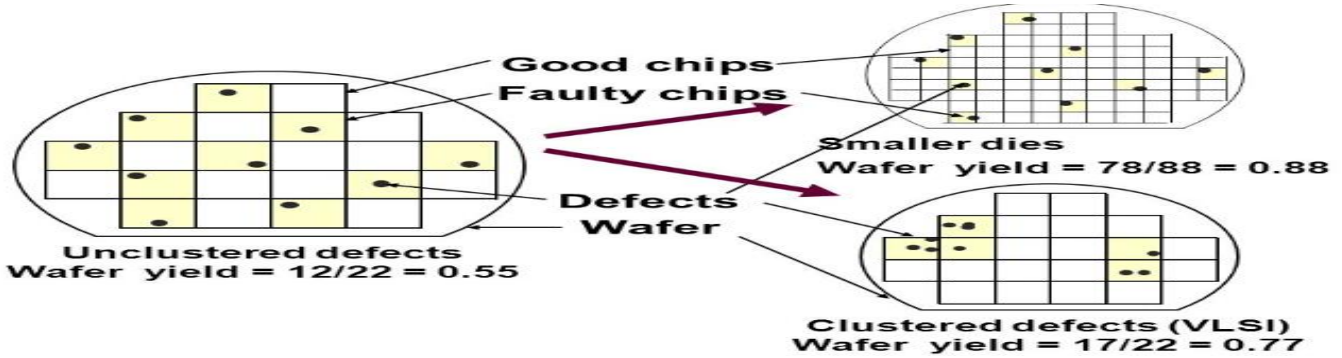


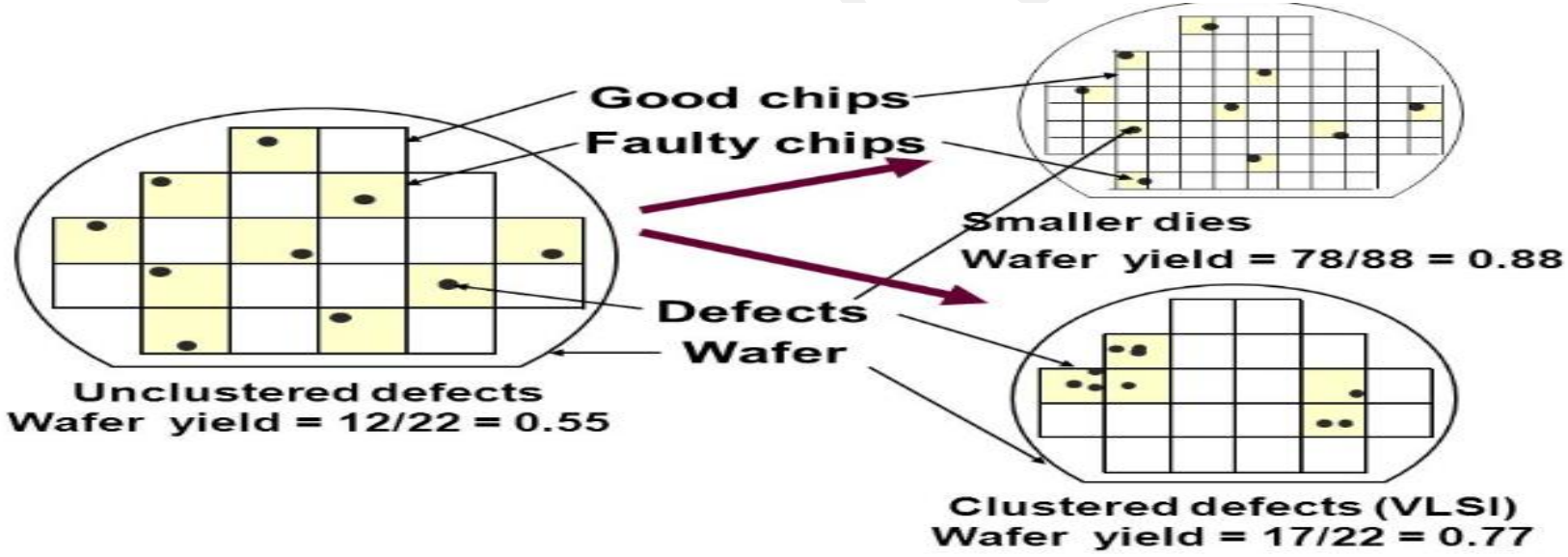


DFM/Chip finishing



What is Yield ?

A manufacturing defect is a finite chip area with electrically malfunctioning circuitry caused by errors in the fabrication process. A chip with no manufacturing defect is called a good chip. Fraction (or percentage) of good chips produced in a manufacturing process is called the **yield**.



Caused for yield dropouts?

1. Random Defects: Due to form of impurities in the silicon itself, or the introduction of a dust particle that lands on the wafer during processing. These defects can cause a metal open or shorts. As feature sizes continue to shrink, random defects have not decreased accordingly making advanced IC's even more susceptible to this type of defect.

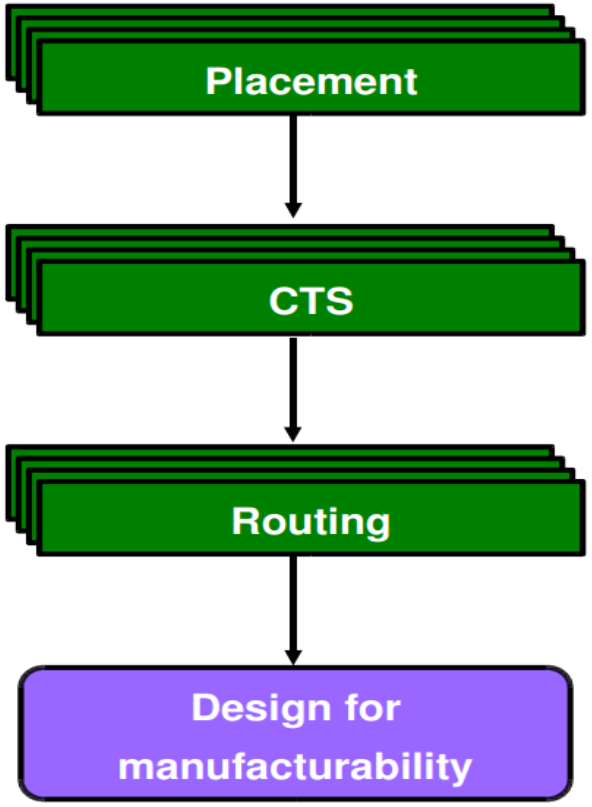
2. Systematic Defects: Again systematic defects are more prominent contributor in yield loss in deep submicron process technologies. Systematic defects are related to process technology due to limitation of lithography process which increased the variation in desired and printed patterns. Another aspects of process related problem is planarity issues make layer density requirements necessary because areas with a low density of a particular layer can cause upper layers to sag, resulting in discontinuous planarity across the chip.

3. Parametric Defects: In deep submicron technology parametric defects is most critical for us. Parametric defects come into the picture due to improper modeling of interconnects parasitic. As a result manufactured device does not match the expected result from design simulation and does not meet the design specification.

DFM and it’s necessity

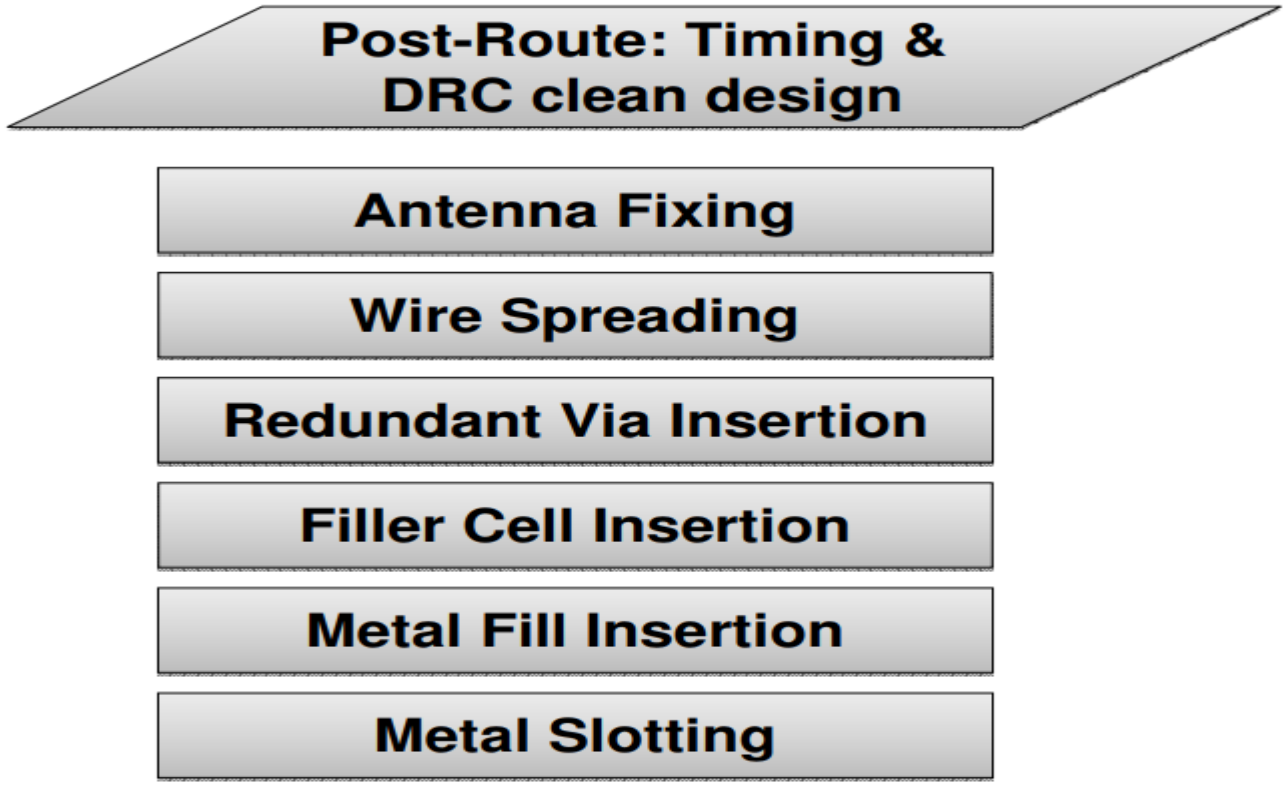
- Design for manufacturability (DFM) is process to overcome Random/Systematic/parametric defects of yield drop out.
- DFM will not be done without collaborations between various technology parties, such as process, design, mask, EDA, and so on.
- Design for Manufacturability is the proactive process which ensures the quality, reliability, cost effective and time to market.
- DFM consist a set of different methodologies trying to enforce some soft (recommended/Mandatory) design rules regarding the shapes and polygons of the physical layout which improve the yield.Given a fixed amount of available space in a given layout area, there are potentially multiple yield enhancing changes that can be made.

Design status at DFM stage



- Standard cells are placed
- Clock tree and HFN buffers are placed
- All clock, signal and P/G nets have been completely routed
- All route related optimizations are completed:
  - Setup and Hold time: met
  - Maximum capacitance limits - met
  - Maximum signal transition times – met
  - Design is DRC clean

DFM/Chip finishing flow



Possible manufacturing issues and fixes

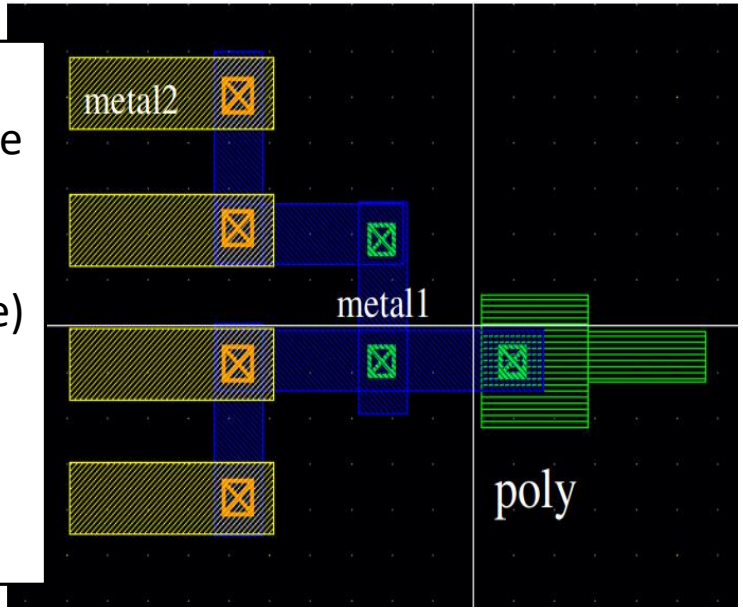
- Gate Oxide integrity → antenna fixing
- Via resistance and reliability → extra contacts
- Random Particle defect → Wire spreading
- Metal erosion → metal slotting
- Metal liftoff → metal slotting
- Metal Over-Etching → metal fill

Gate oxide integrity

- Metal wires (antenna) placed in an EM field to generate voltage gradients
- During the metal each stage . Strong EM fields are used to stimulate the plasma etchant
- Resultant voltage gradients at MOSFET gates can damage thin oxide

Antenna rules

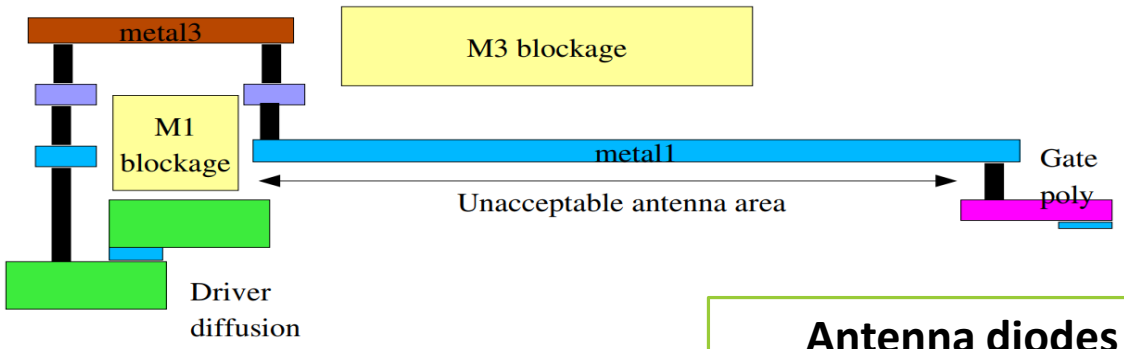
- As length of wire increases during processing , the voltage stressing the gate oxide increases.
- Antenna rules define acceptable length of wires
- Antenna ratio = (Area of metal connected to gate) / (Combined area of gate)
- Ways to fix antenna violations
  - Metal splitting/Layer hopping
  - Antenna cell addition



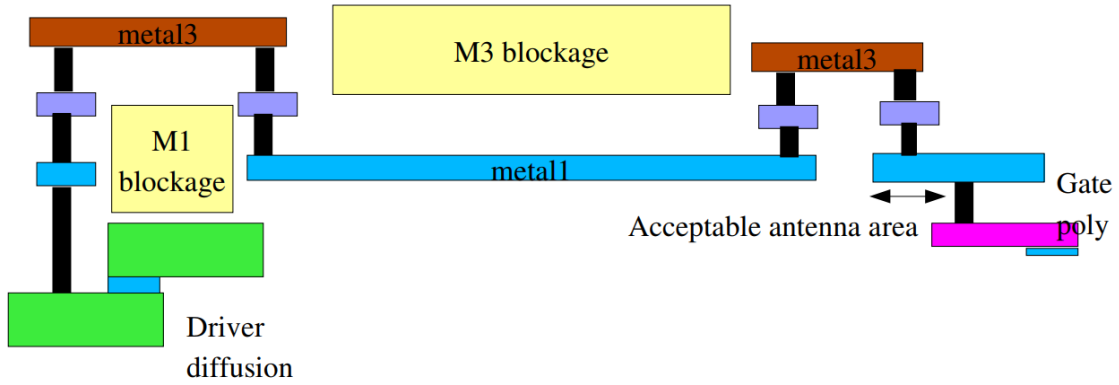
Fixing antenna violations

LAYER JUMPING

Before layer jumping

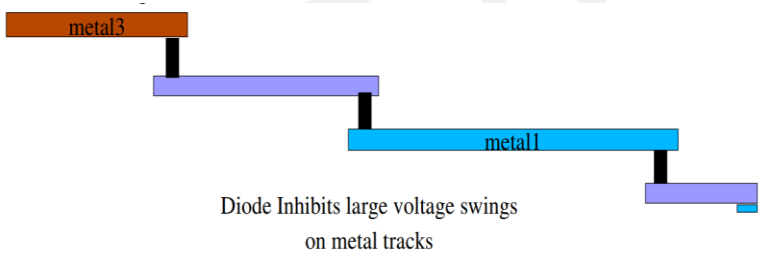


After layer jumping

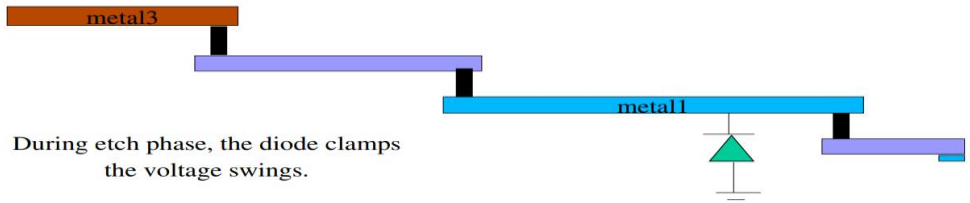


Antenna diodes

Before antenna diode insertion



After antenna diode insertion

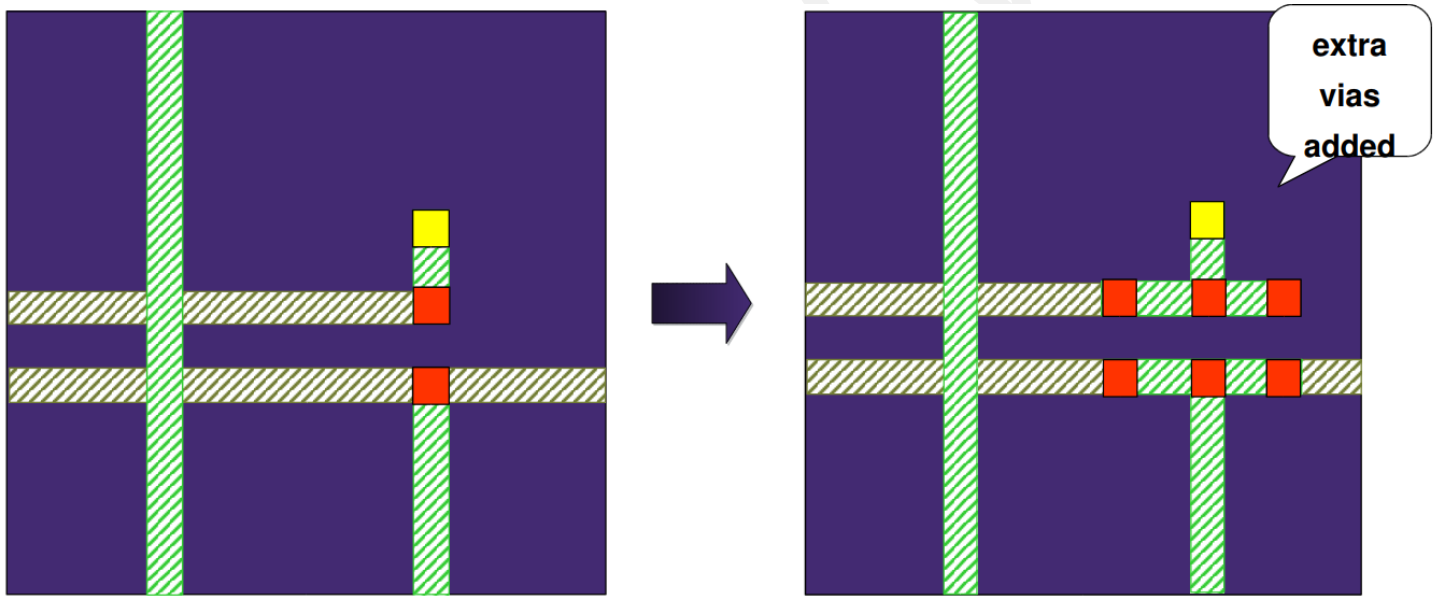


Reliability

- What is reliability ?
- Why do we need fix reliability issues?

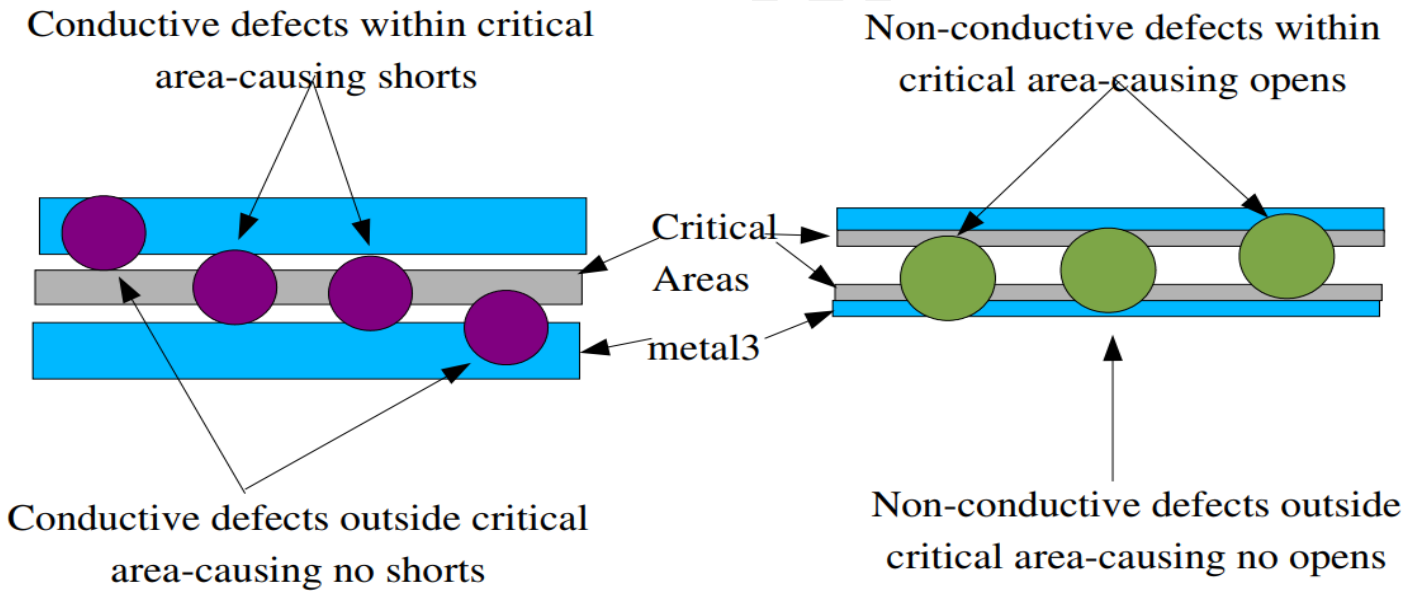
Reliability

- Replacing one via with multiple vias can improve yield & timing (series R reduction)
- Inserts multiple vias without rerouting improve the VIA resistance



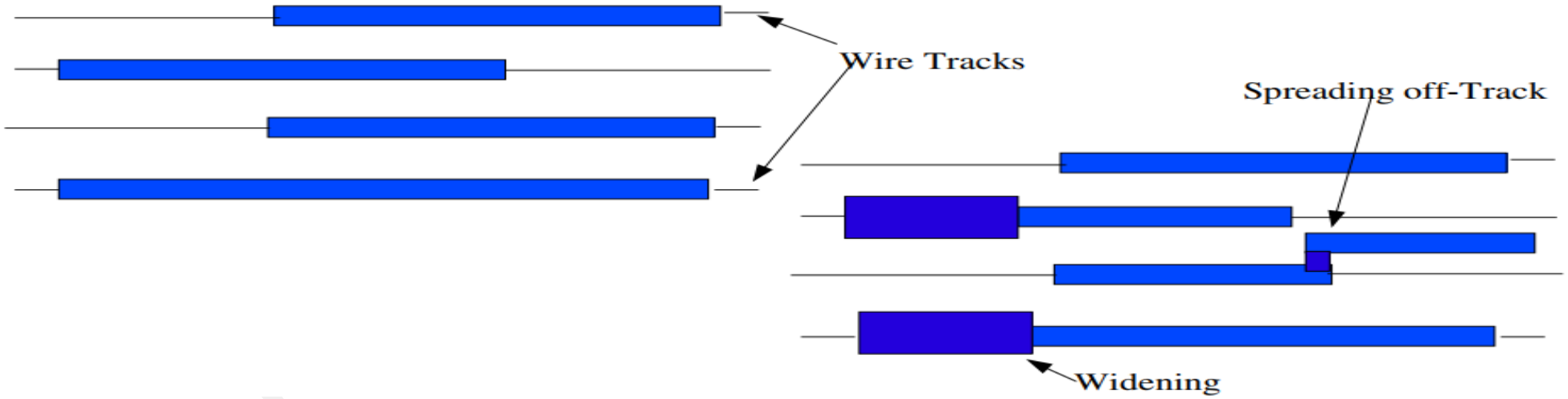
Random particle defects

Random missing or extra material causes opens or shorts during the fabrication process.
* Wires at minimum spacing are most susceptible to shorts
* Minimum width wires are most susceptible to opens

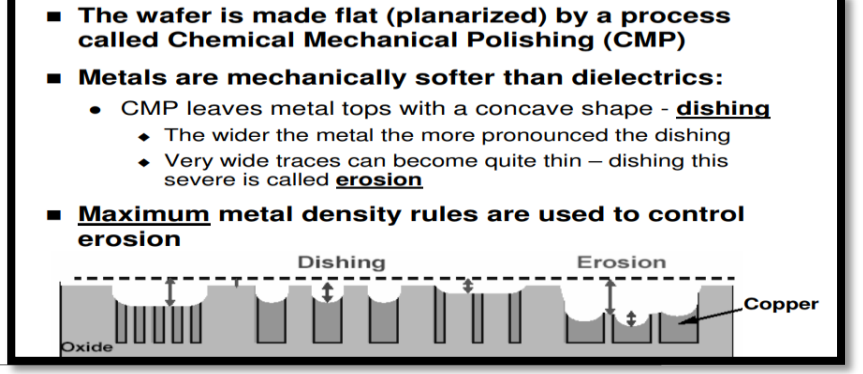


Wire spreading/Wire splitting

- Spread wires to reduce short critical area
  - push routes off-track by half pitch
  - will not push “frozen” nets
- Widens wires to reduce open critical area



Metal erosion



The wafer is made flat (planarized) by a process called Chemical Mechanical Polishing (CMP)

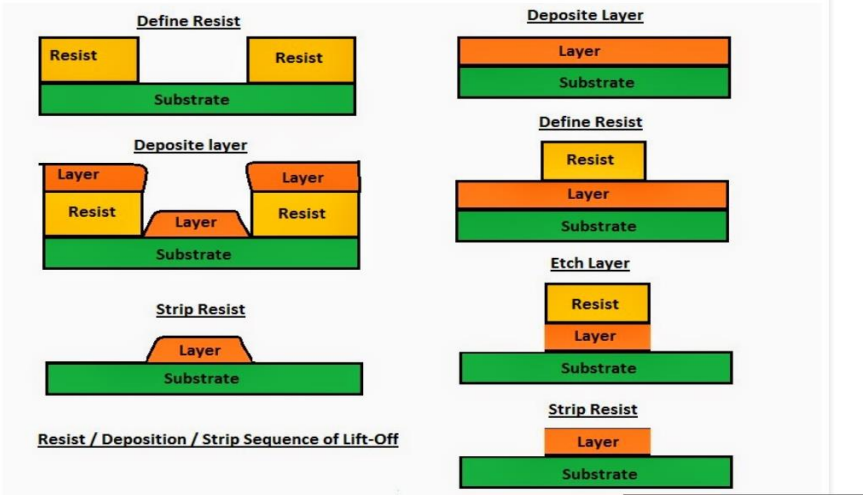
- Metals are mechanically softer than dielectrics:

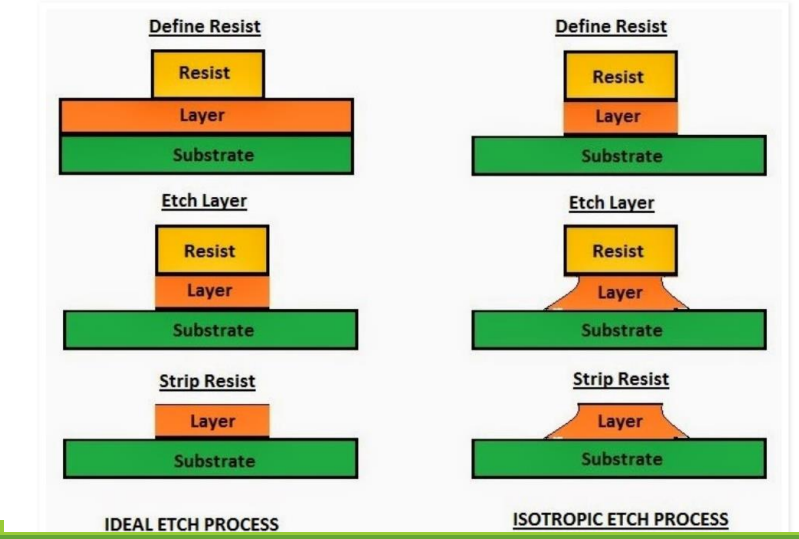
* CMP leaves metal tops with a concave shape dishing

* the wider the metal the more pronounced the dishing

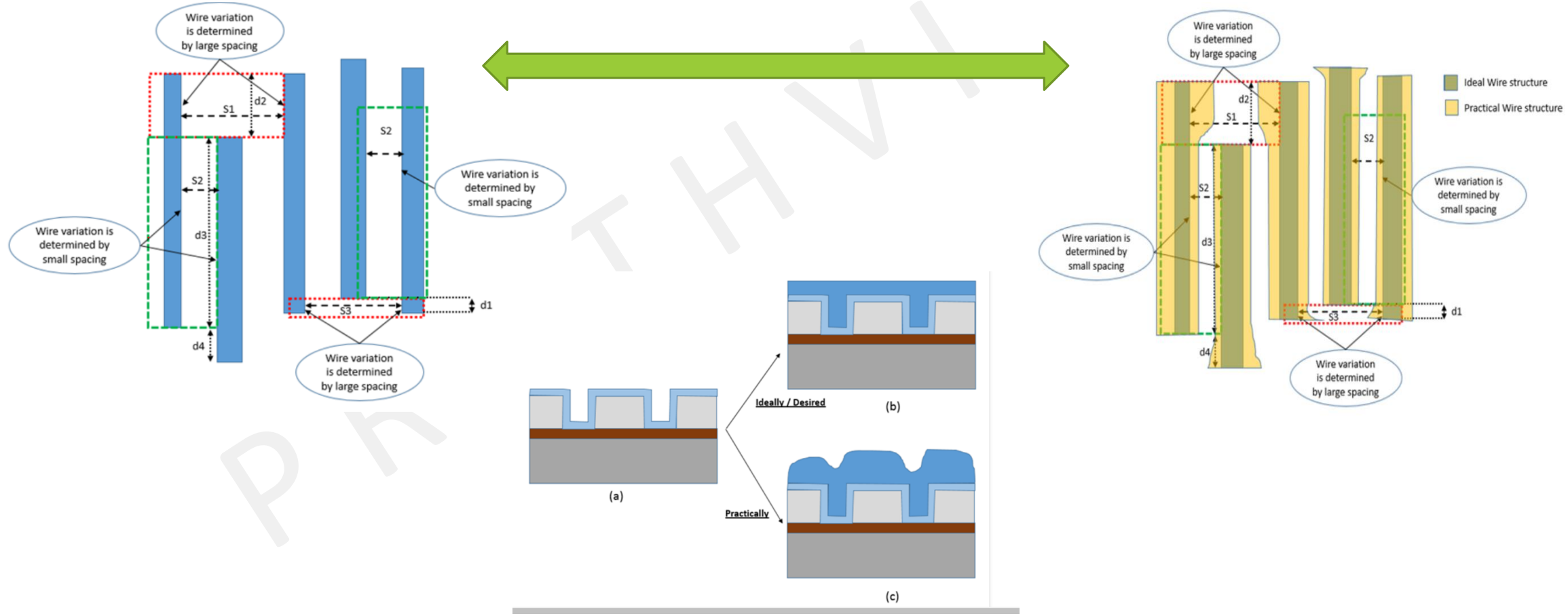
* Wide traces with little intervening dielectric and can become quite thin –dishing this severe is called erosion.

- Process rules specify maximum metal density per layer to minimize erosion



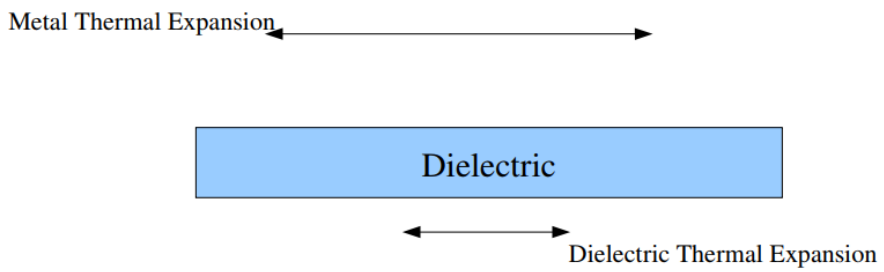


Width variation during etching

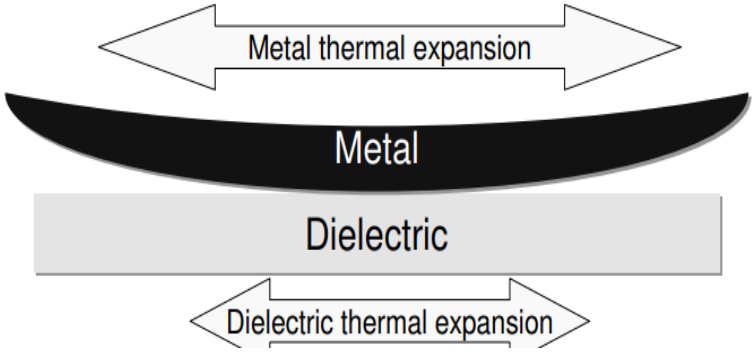


Metal liftoff

- Conductors and dielectrics have different coefficients of thermal expansion:
  - Stress built up with temperature cycling
  - Metals can delaminate (liftoff) with time
  - Wide metal traces are more vulnerable than narrow ones
- Maximum metal density rules also address this issue.



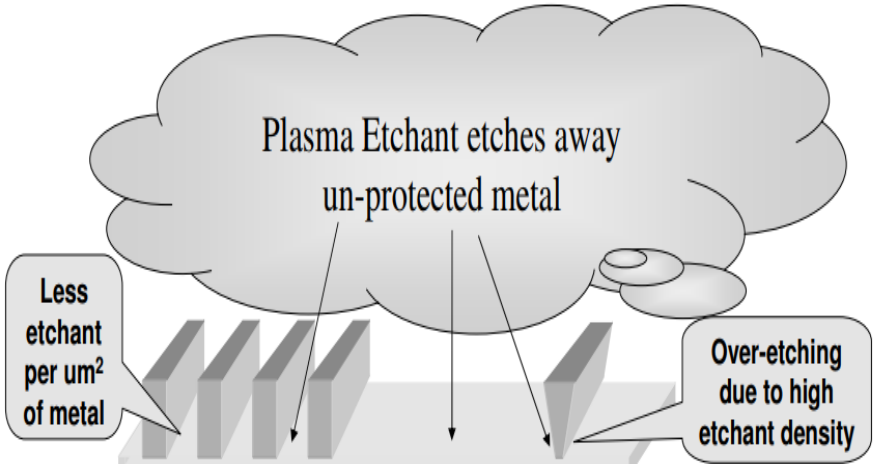
- **Metal conductors and dielectrics have different coefficients of thermal expansion:**
  - Stress builds up with temperature cycling
  - Metals can delaminate (lift off) with time
  - Wide metal traces are more vulnerable than narrow ones
- **Maximum metal density rules also address this issue**



Metal over etching

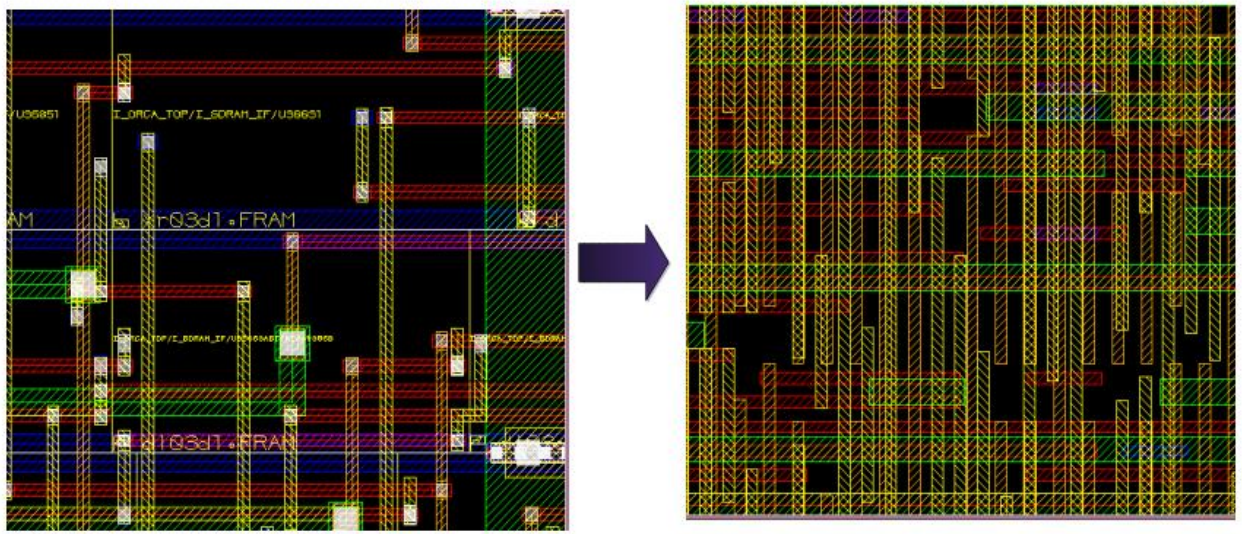
- A narrow metal wire separated from other metal receives a higher density of etchant than closely spaced wires
- The narrow metal can get over etched
- Minimum metal density rules are used to control this.

- **A metal wire in low metal density region receives a higher ratio of etchant can get over-etched**
- **<u>Minimum</u> metal density rules are used to control this**



Metal fill

- Fills empty tracks with metal shapes to meet the minimum metal density rules
- Uses up most of the remaining routing resource:
  - No further routing or antenna fixes can be done



Why filler cell insertion?

* Uniform Nwell connectivity across the core area

What happens if we don’t have filler cells in the design?

General DFM guidelines

1. Filler cell (consisting regular Diffusion and Poly silicon structures) insertion and shielding
Issue Addressed: PO/OD non uniformity
Benefit: Higher parametric yield.

2. Via optimization
Issue Addressed: open Via's, systematic via opening issue
Benefit: Higher yield after manufacturing and qualification.

3. Wire Spreading
Issue Addressed: wire shorts and opening due to defectively.
Benefit: Higher yield, decrease cross talk.

4. Power/ground-connected fill
Issue Addressed: Density gradients, Large IR drop, Layout becomes regular
Benefit: Robustness to IR drop

5. Litho hotspot detection and repair
Issue Addressed: Lithography hotspots
Benefit: Higher yield

6. Dummy Metal/Via/FEOL
Issue Addressed: Large density gradients
Benefit: Higher yield

7. CMP hotspot detection
Issue Addressed: CMP hotspots
Benefit: Higher yield


THANKS