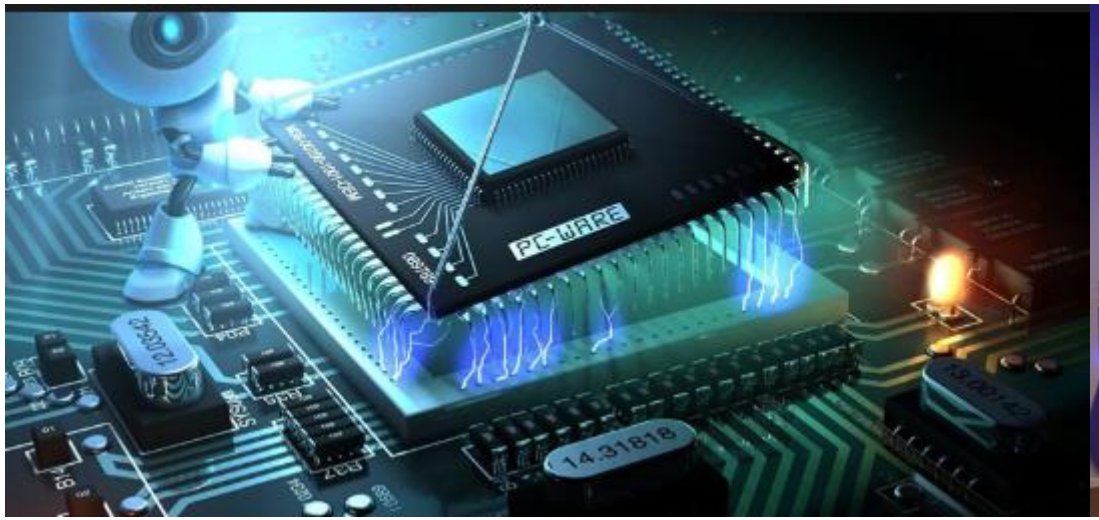
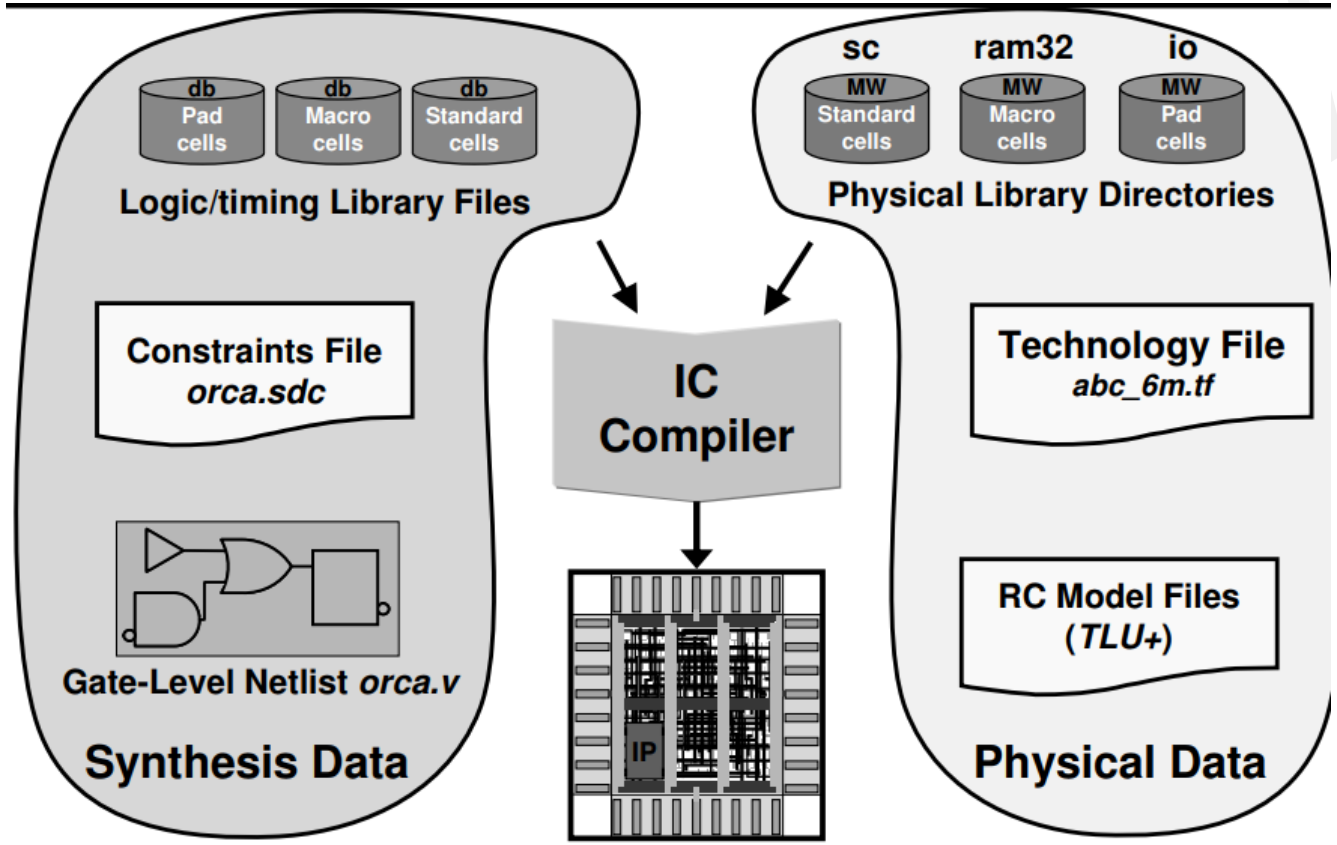


Design setup

Data setup



Inputs required to start PNR

1. Libraries
   - Logical/Timing libraries (.db)
   - Physical libraries (MW or FRAM view)
2. Technology file (.tf)
3. RC model file (TLU plus files)
4. Mapping file (B/w TLU and Tech file)
5. Neltist (.v)
6. Constraints (.SDC)
7. Power intent (.upf)
8. Scan chain information (scan.def)
9. Standard cell placement info (FP.def)

Logical libraries

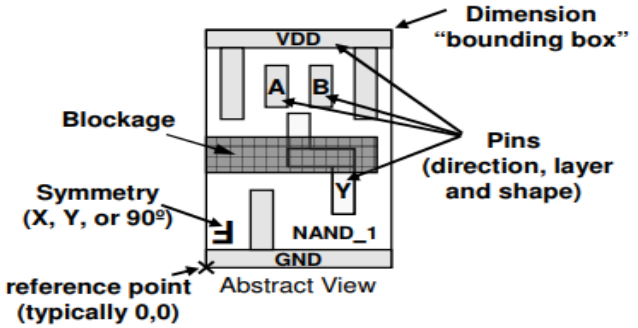
- Provide timing and functionality information for all the standard cells (and or , flipflop)
- Provide timing information for Hard macros
- Define drive/load design rules
  - Max fnaout
  - Max transition
  - Max/min capacitance
- Libraries are specified with below variables

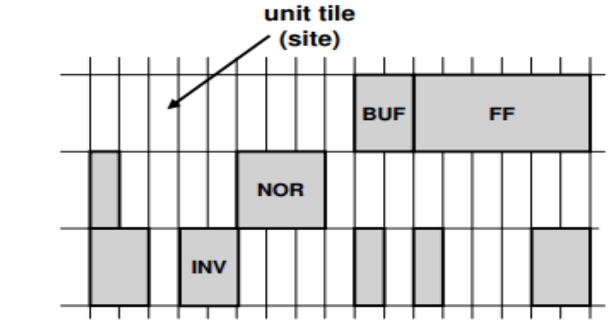
  target_libraries

  link_libraries

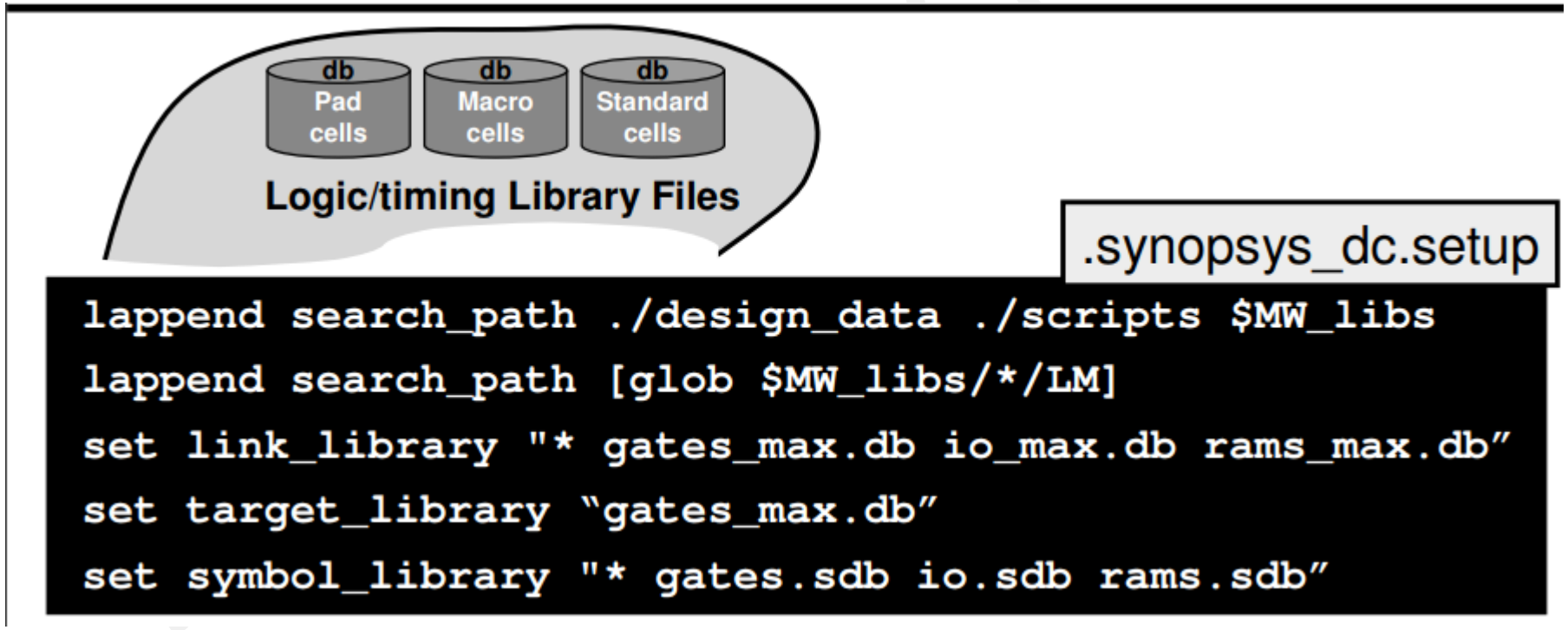
Physical libraries

- Physical libraries contains information about standard cells, macros & pads , necessary for placement and routing
- Contains placement unit tile information
  - Height of placement rows
  - Pitch of routing tracks
  - Preferred routing directions



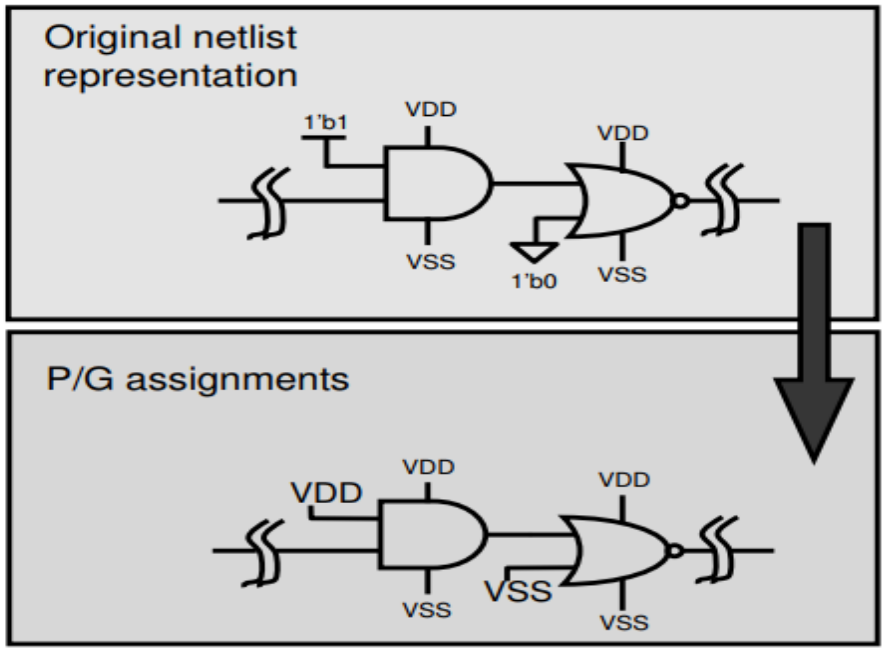


1. Specifying the logical libraries



2. Define logic “0” and logic “1”

- **In the netlist, “tie-high” and “tie-low” inputs may be connected to logical ‘1’ and ‘0’**
- **Define corresponding power and ground signal names**
  - As defined by the names of the P/G pre-routes in your floorplan



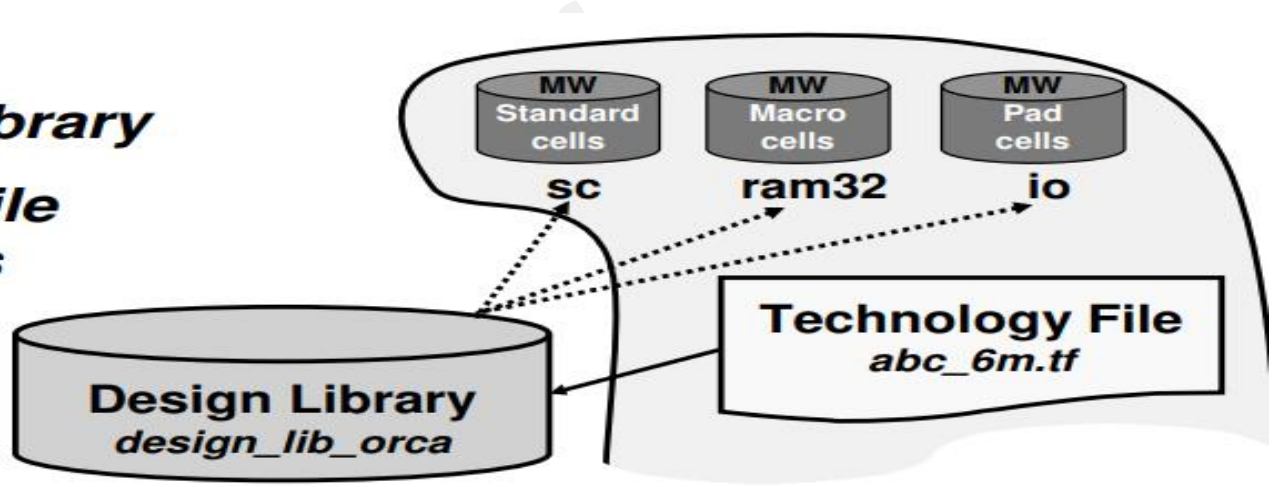
.synopsys_dc.setup

```
set mw_logic0_net "VSS"
set mw_logic1_net "VDD"
```

Set by default in 2008.09-SP2

3. Create a “container” : The design library

- Create a *design library*
- Specify the *tech file* and *reference libs*




```
create_mw_lib   design_lib_orca   -open \
      -technology abc_6m.tf \
      -mw_reference_library “sc ram32 io”
set_check_library_options -all
check_library
```

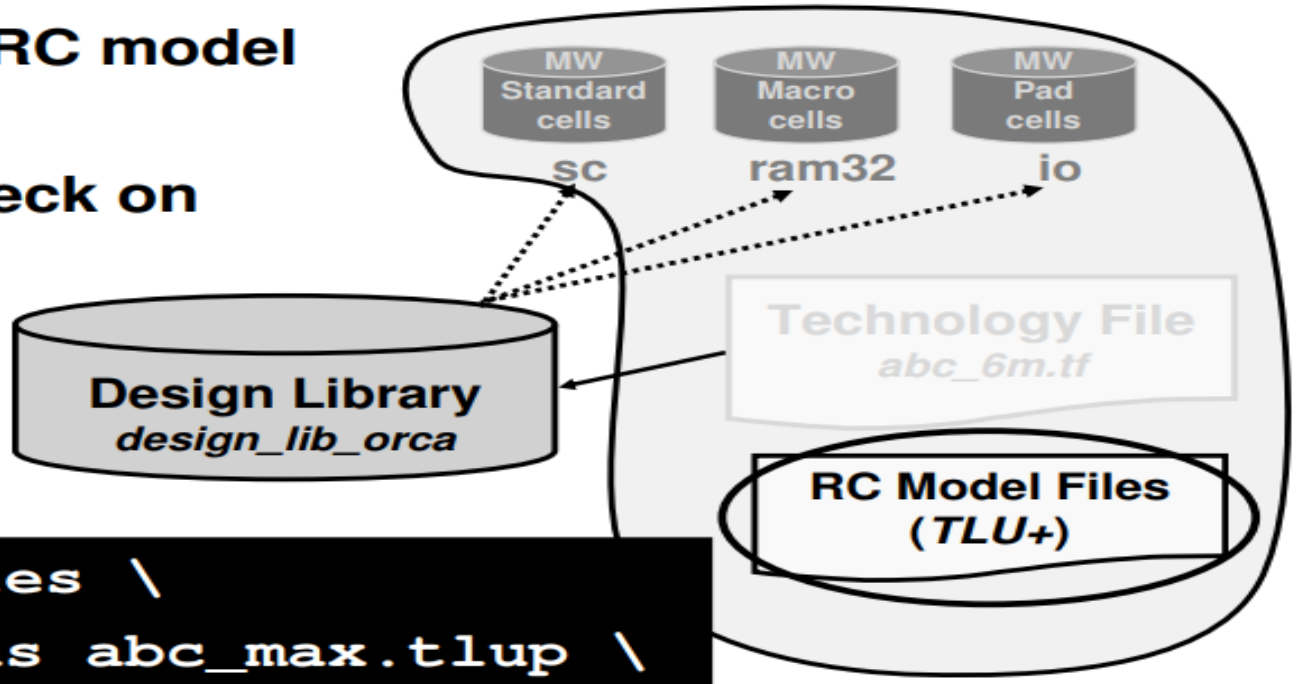
Consistency check b/w logic and physical library (reports missing library)

- **Reports library inconsistencies, for example:**
  - Between logic (`link_library`) and physical libraries:
    - Missing cells
    - Missing or mismatched pins
  - Within physical libraries:
    - Missing CEL (layout) or FRAM (abstract) view cells
    - Duplicate cell name in multiple reference libraries
- **Recommended after creating the design library**

```
create_mw_lib ...
set_check_library_options -all
check_library
```

4. Specify TLU+ parasitic RC model files

- **Specify the *TLU+* RC model files to be used**
- **Perform sanity check on settings and files**



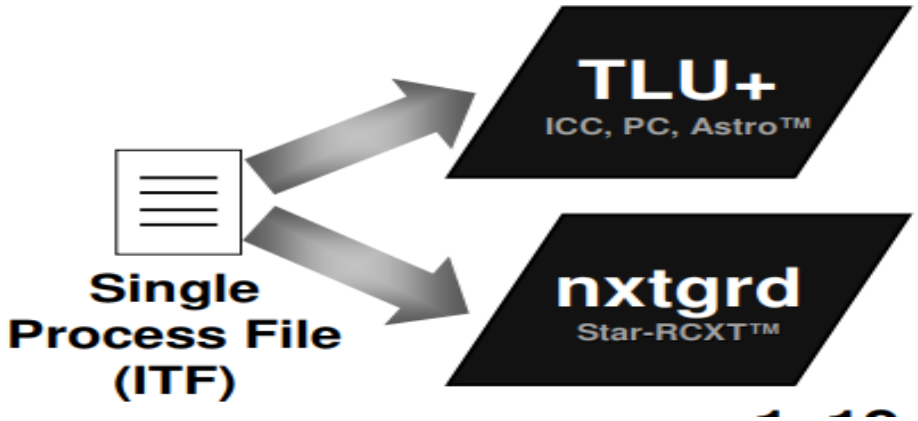

```
set_tlu_plus_files \
      -max_tluplus abc_max.tlup \
      -min_tluplus abc_min.tlup \
      -tech2itf_map  abc.map
check_tlu_plus_files
```

TLU+ models

- **IC Compiler calculates interconnect C and R values using net geometry and the TLU+ look-up tables**
- **Models UDSM process effects**

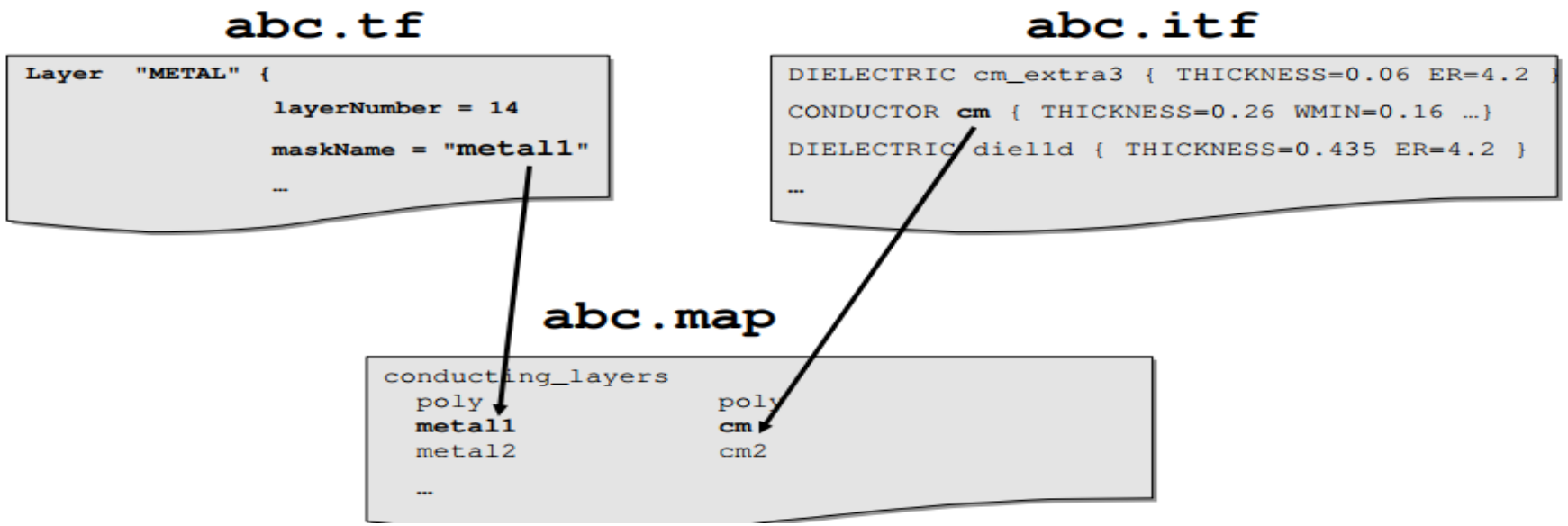
UDSM Process Effects
- Conformal Dielectric
- Metal Fill
- Shallow Trench Isolation
- Copper Dishing:
  - Density Analysis
  - Width/Spacing
- Trapezoid Conductor

- **Some vendors provide only an *ITF* process file**
- **User must then generate *TLU+* from *ITF* (see below)**



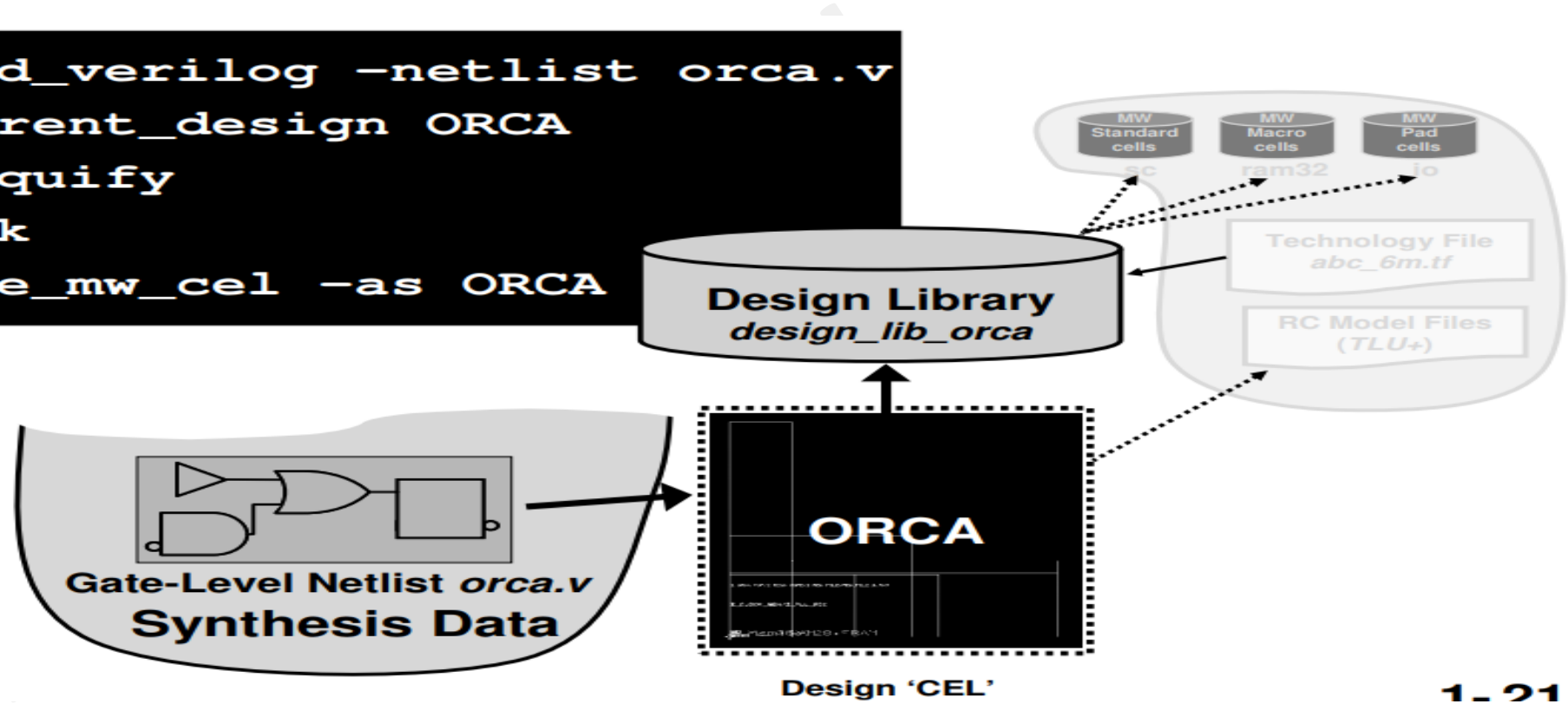
Mapping file

The *Mapping File* maps the technology file (.tf) layer/via names to Star-RCXT (.itf) layer/via names.



5. Read the netlist and create the design view

```
read_verilog -netlist orca.v
current_design ORCA
uniquify
link
save_mw_cel -as ORCA
```



6. Verifying loaded logical libraries

Ensure that all the required logical libraries (specified by `set link_library`) have been loaded

`list_libs`

- Note: This command can be executed only after reading and linking the netlist

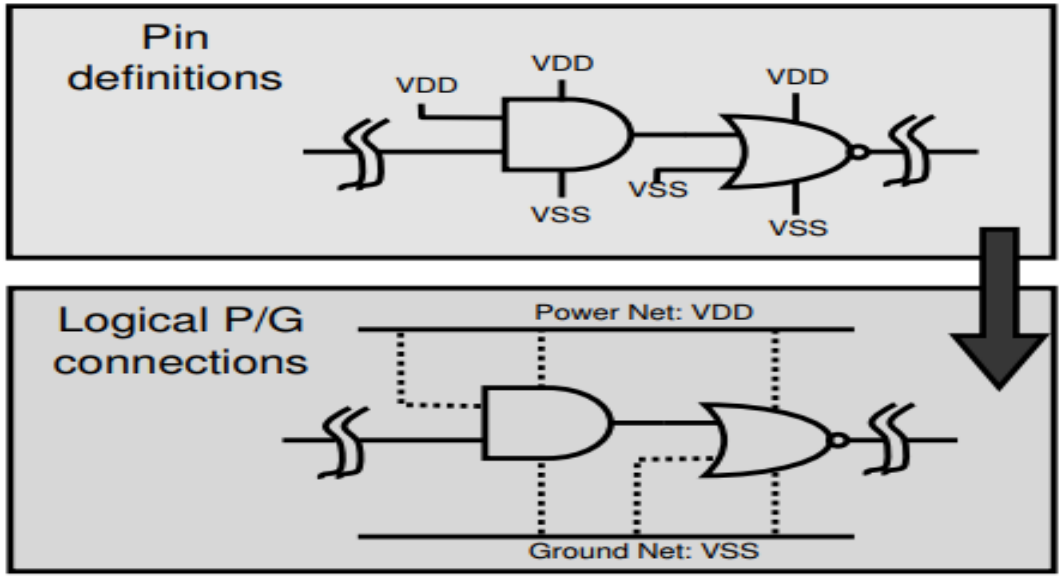
```
Logical Libraries:
------------------------------------------------------------------------
Library                File                          Path
-------                ----                          ----
cb13fs120_tsmc_max     sc_max.db           /projects/XYZ_design/ref/db
cb13io320_tsmc_max     io_max.db           /projects/XYZ_design/ref/db
ram8x64_max            ram8x64_max.db      /projects/XYZ_design/ref/db
ram16x128_max          ram16x128_max.db    /projects/XYZ_design/ref/db
gtech                  gtech.db            /global/apps3/icc_2008.09/libraries/syn
standard.sldb          standard.sldb       /global/apps3/icc_2008.09/libraries/syn
```

The *gtech* and *standard* libraries are generic libraries that are loaded by default – used during synthesis

7. Defining logical power/ground connections

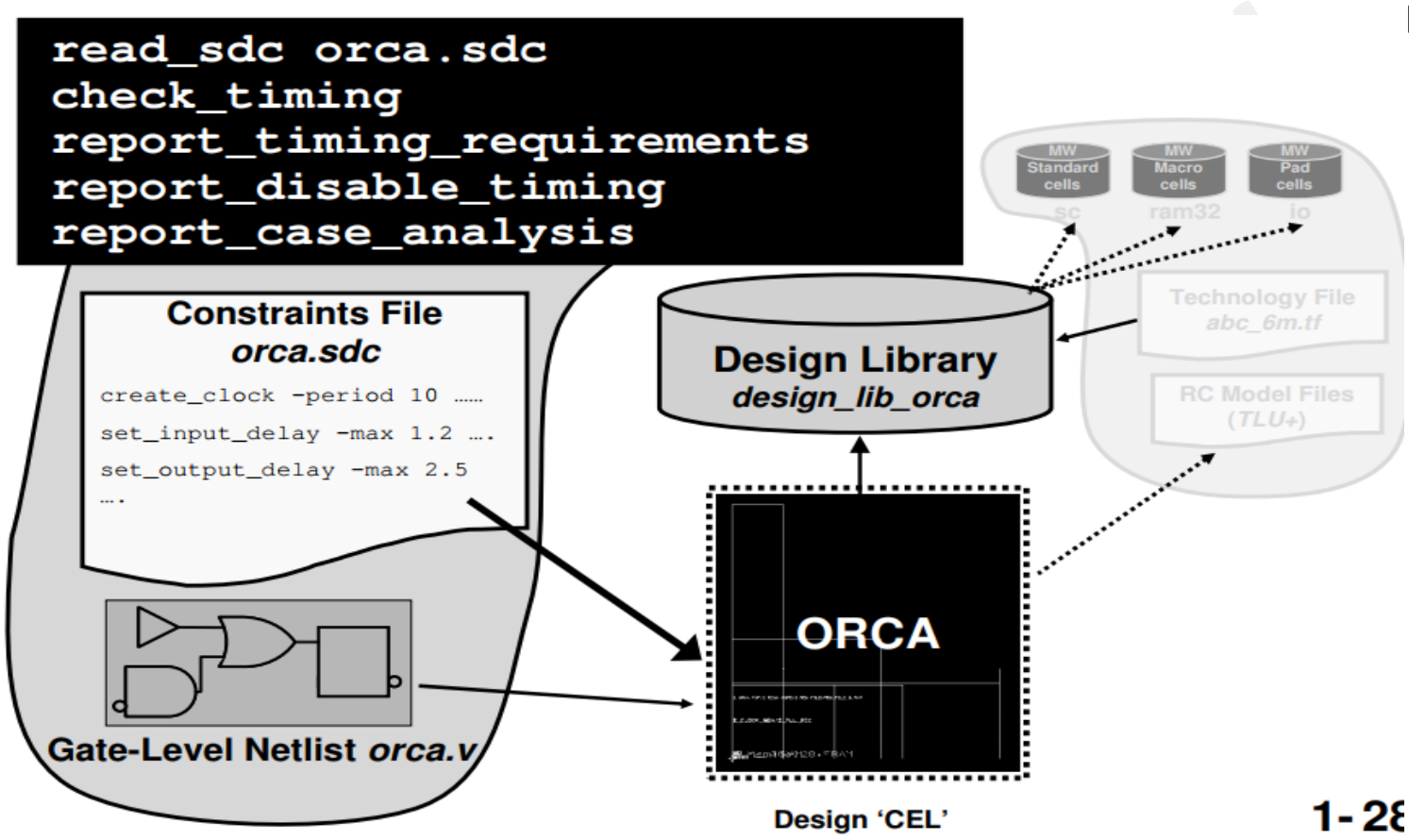
Define "logical connection" between P/G pins and nets

- Does not make any physical connections




```
derive_pg_connection -power_net VDD -power_pin VDD \
                     -ground_net VSS -ground_pin VSS
check_mv_design -power_nets
```

8. Apply and check timing constraints



Need to create MCMM scenario in this stage

9. Ensure proper modelling of clock tree

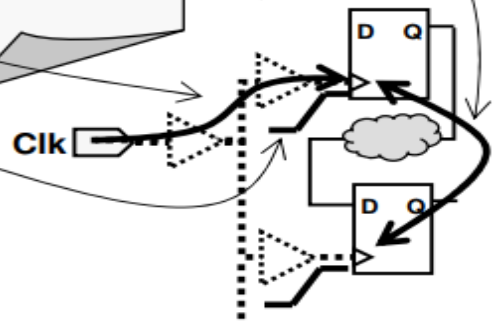
- **Ensure your SDC constraints model estimates of clock skew, latency and transition times for all clocks**

report_clock -skew

Object	Rise Delay	Fall Delay	Min Rise Delay	Min Fall Delay	Uncertainty Plus	Uncertainty Minus
SYS_2x_CLK	0.80	0.80	0.40	0.40	0.10	0.20
SDRAM_CLK	–	–	–	–	0.10	0.15

Object	Max Transition Rise	Max Transition Fall	Min Transition Rise	Min Transition Fall
SYS_2x_CLK	0.07	0.07	–	–
SDRAM_CLK	0.07	0.07	–	–

Pre-CTS clock modeling



- **Ensure no clocks are defined as "propagated" clocks**

report_clock

Clock	Period	Waveform	Attrs	Sources
SDRAM_CLK	7.50	{0 3.75}	p	{sdram_clk}
SYS_2x_CLK	4.00	{0 2}		{sys_2x_clk}

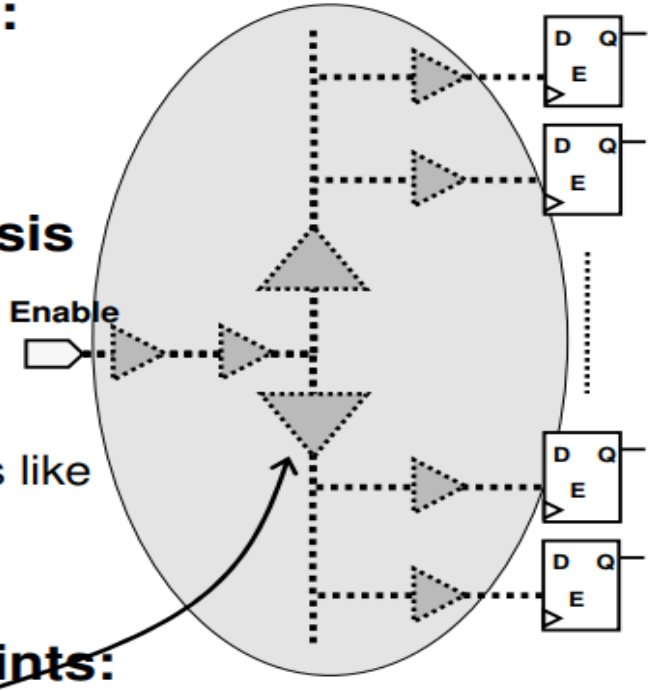
10 . Performing timing sanity check

- **Before starting placement it is important to ensure that the design is not over-constrained**
  - Constraints should match the design's specification
- **Report 'ZIC' timing before placement**
  - Check for unrealistic or incorrect constraints
  - Investigate large zero-interconnect timing violations

```
set_zero_interconnect_delay_mode true
Warning: Timer is in zero interconnect delay mode. (TIM-177)
report_constraint -all
report_timing
set_zero_interconnect_delay_mode false
Information: Timer is not in zero interconnect delay mode. (TIM-176)
```

11. Remove unwated/Ideal nets in the design

- **Your SDC constraints may contain either of the following commands:**
  - `set_ideal_network` **(preferred)**
  - `set_ideal_net` **(obsolete)**
- **These commands prevent synthesis (Design Compiler) from building buffer trees on specified signals, which is deferred to the physical design phase** (typically high fanout nets like *set/reset*, *enable*, *select*, etc.)
  - **To allow buffering during placement remove the constraints:**




```
remove_ideal_network [get_ports Enable Select Reset]
```

12. Save the design

It's good practice to save the design after each key design phase, for example: data setup, design planning, placement, CTS and routing:

```
save_mw_cel -as ORCA_data_setup
```

Design setup (initial db) :- checklist

1. “check_design” should be clean

2. “check_timing” should be clean, all the registers should get the clocks, no unconstrained paths in the design

2. ZIC timing should be acceptable value

4. Loaded with respective Physical/logical, technology file and TLU plus files

5.Correct inputs has to be read inside “design” container

PVT, RC Variation & OCV

PVT:

PVT is abbreviation for Process, Voltage and Temperature. In order to make our chip to work in all possible conditions, like it should work in Siachen Glacier at -40°C and also in Sahara Desert at 60°C, we simulate it at different corners of process, voltage and temperature which IC may face after fabrication. These conditions are called as corners. All these three parameters affect the delay of the cell. We will see each and every parameter and its effect on delay in detail.

Process:

- Process variation is the deviation in attributes of transistor during the fabrication.
- During manufacturing a die, the area at the center and that at the boundary will have different process variation. This happens because layers which will be getting fabricated can not be uniform all over the die. As we go away from the center of the die, layers can differ in their sizes.
- Process variation is gradual . It can not be abrupt.

Process variation

Factors which can cause process variation

1. Wavelength of UV light
2. Manufacturing defects

Affects of process variation

1. Oxide thickness variation
2. Dopant and mobility fluctuation
3. Transistor width, length etc.
4. RC Variation

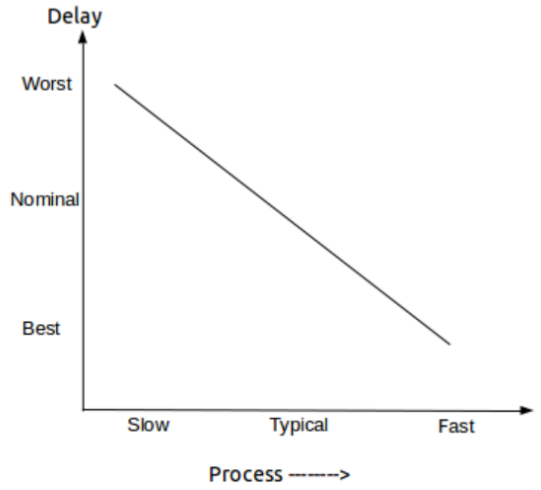
Process variation ctnd..

- Process variations will cause the parameters like threshold voltage to change its value from expected. Threshold voltage depends on oxide thickness, source-to-body voltage and implant impurities. Consider the drain current equation for NMOS.

$$I_D = (1/2)\mu_n C_{ox} (W/L)(V_{GS} - V_{Th})^2$$

- Current flowing through the channel directly depends upon mobility (μ_n), oxide capacitance C_{ox} (and hence thickness of oxide i.e. t_{ox}) and ratio of width to length.

Process V/S Delay



Delay variation with respect to voltage

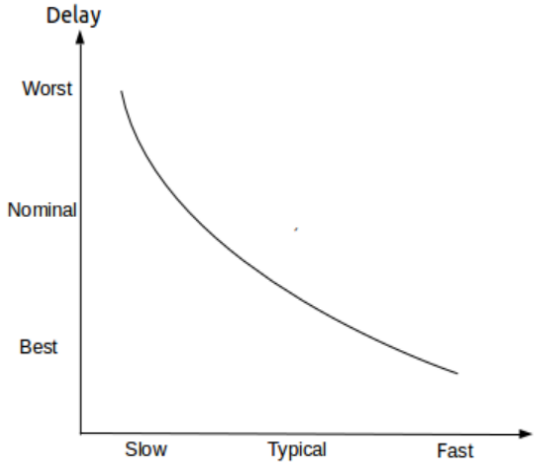
Possible reasons for voltage variation

1. Supply voltage fluctuations :- It's IR drop, IR drop is caused by the current flow over the parasitic resistance of the power grid. IR drop reduces the supply voltage from the required value.

2. Supply noise:- Voltage drop/Overshoot due to fluctuation in inductance, resistance & capacitance

3. Voltage variation across voltage regulators/Power supply ports

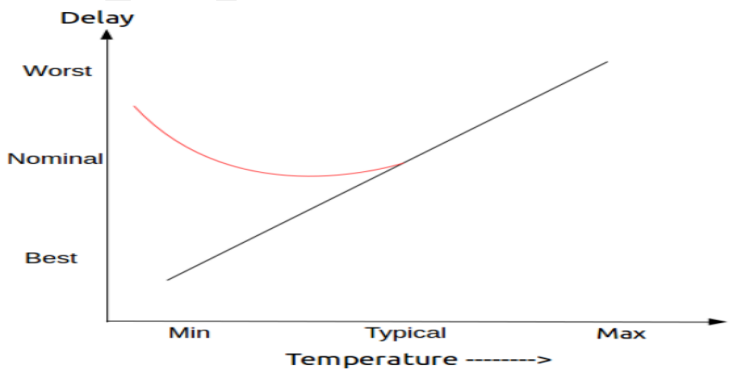
Voltage V/S Delay



Delay variation with respect to temperature

- The temperature at the junction inside the chip can vary within a big range and that's why temperature variation need to be considered.
- Figure shows the variation of delay with respect to temperature. Delay of a cell increases with increase in temperature. But this is not true for all technology nodes. For deep sub-micron technologies this behavior is contrary. This phenomenon is called as temperature inversion.

Voltage V/S Delay



Temperature inversion

- The delay depends on the output capacitance and I_D current (directly proportional to C_{out} and inversely proportional to I_D). When the temperature increases, delay also increases (due to the variation in carrier concentration and mobility).

- But when temperature decreases, delay variation shows different characteristics for submicron technologies. For technology nodes below 65nm, the delay will increase with decrease in temperature and it will be maximum at -40°C. This phenomena is known as “temperature inversion”.

Why temperature inversion happens?

- As temperature increases, mobility and threshold voltage start decreasing. The delay is inversely proportional to the mobility and directly proportional to the threshold voltage. So the resultant effect from both mobility and threshold voltage decides the value of delay.

Consider the current equation of a MOSFET for better understanding

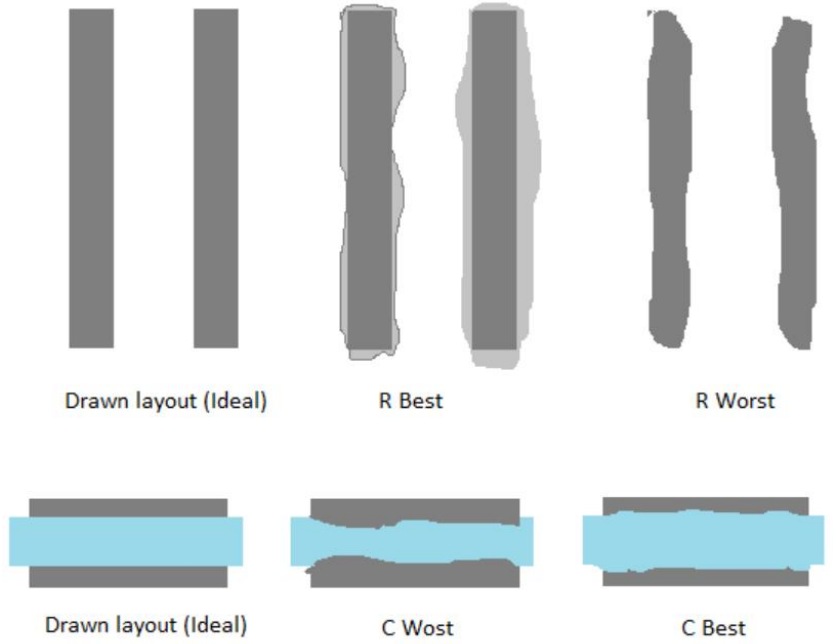
$$I_D = (1/2)\mu_n C_{ox} (W/L)(V_{GS} - V_{Th})^2$$

- In the higher technology node, where the supply voltage is very high, the effect of V_{Th} is very low as ($V_{GS} - V_{Th}$) value is large. Hence mobility plays major role in deciding current. So at higher technology nodes, when the temperature increases mobility decreases and as a result the delay will increase.

- At the lower technology node (specifically, less than 65nm), the supply voltage is very low, so the ($V_{GS} - V_{Th}$) difference is small and the square of this value is very small resulting reduced I_D current, which increases delay at lower temperature. Where at other end above 65nm delay decreases at lower temperature.

RC variations

- RC variation is also considered as corners for the setup and hold checks.
- RC variation can happen because of fabrication process and the width of metal layer can vary from the desired one.
- Parasitic corners
  - Cbest – minimum capacitance, minimum delay (Hold analysis)
  - Cworst – maximum capacitance, maximum delay (Setup analysis)
  - RCbest – minimum RC product (Long interconnects)
  - RCworst – maximum RC product (Long interconnects)
  - Typical – nominal values of RC
-



Different analysis modes in STA

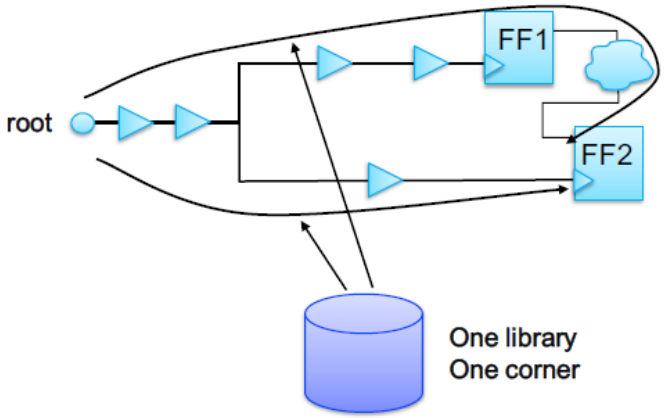
- Semiconductor device parameters can vary with conditions such as fabrication process, operating temperature, and power supply voltage.

- The STA tool supports three analysis modes
  - ✓Single operating condition
  - ✓Min/Max (BC-WC)
  - ✓On chip variation

Single Operating Condition

- Single set of delay parameters for the whole circuit, based on one set of process, temperature, and voltage conditions
- This analysis is the most simplistic type of analysis, because it does not consider any on- or off-chip variation

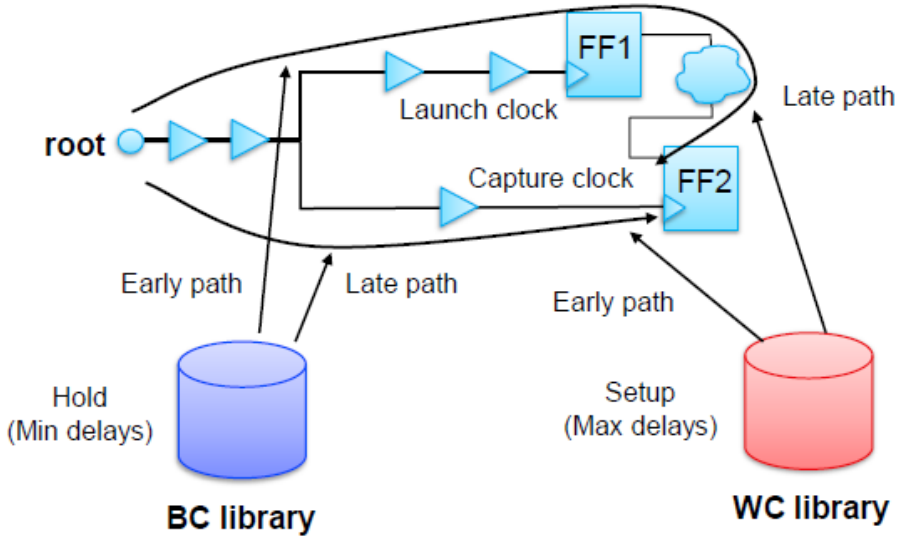
```
read_library maxLib
set_timing_library -max maxLib
set_analysis_mode -analysisType single -checkType setup
```



BC-WC analysis mode

- Using both BC and WC libraries together is one way to model off-chip variation of delays due to external temperature and voltage variations
- Analyzes off-chip variation - Operating conditions are two extremes
- This analysis mode doesn't model the on chip variation

```
read_library -max maxLib -min minLib
set_analysis_mode -analysisType bcWc
```



On chip variation

Variation are of two types

1. Global variation: - These are PVT variations that depend on external factors like Process, Supply Voltage and Temperature. ICs are fabricated in batches and hence exhibit die to die variations. Some exhibit strong process (fast switching) and weak process (slow switching). These are known as inter-chip variations.

2. Local variations:- Local variations are also variations in PVT, but these are intra-chip variations known as OCV.

OCV cntd..

Process:

All the transistors in a chip cannot be expected to have the same process. There can be variations in channel length, oxide thickness, doping concentration, metal thickness etc due to imperfections in manufacturing process like mask print, etching etc.

Voltage:

The supply voltage reaching the power pins will not be the same for all standard cells. The power network has a finite resistance. Consider two cells, one which is placed closer, and other placed far. As the interconnect length for the farther cell is more, it has more resistance and results in a higher IR drop, thereby reducing the supply voltage reaching the cell. As the voltage is less, this cell has more delay than the cell which is placed closer.

Temperature:

The transistor density within a chip is not uniform. Some regions of the chip have higher density and higher switching, resulting in a higher power dissipation. Hence the junction temperature at these regions are higher, forming localized hot spots. This variation in temperature across the chip can result in different delays.

How do we account OCV variations?

- As a result of OCV, some cells may be fast or slow than expected. If these variations are not accounted, results may be pessimistic and can lead to setup or hold violations.
- In order to model these, we introduce derates. Timing derates are multiplied with the net delay and cell delay for the launch and capture clock paths.
- Let us consider a timing derate of 8% and how it is accounted in setup and hold analysis.

Setup analysis:

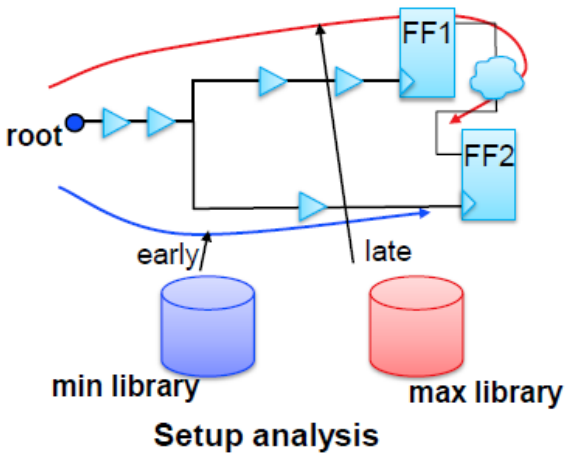
Setup check is done in worst case. The setup check is more pessimistic when the launch clock reaches late than the capture clock. Here we multiply the launch path delays with late derate of 1.08 and the capture path delays with an early derate of 0.92.

Hold analysis:

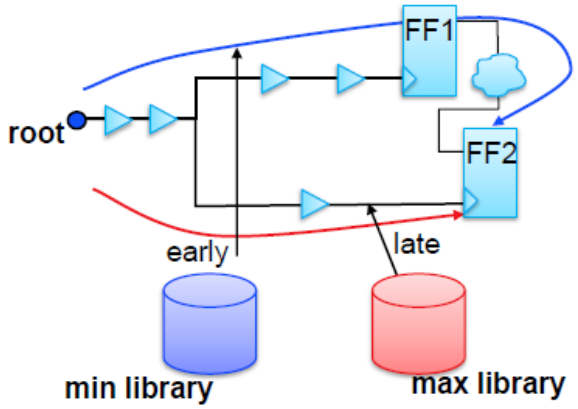
Hold check is done in best case. Hold check is more pessimistic when the launch clock reaches early than the capture clock. Here we multiply the launch path delays with an early derate of 0.92, and capture path delays with a late derate of 1.08.

On chip variation (OCV) solutions

```
read_library -max slow -min fast
set_analysis_mode -analysisType onChipVariation
```



Setup analysis



Hold analysis

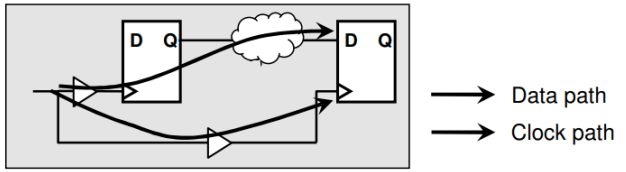
Global variation:- Global variation can be fixed by using different libraries in arrival path and required path

Local variation: - Local variation can be fixed by using different derates for arrival and required path

Example

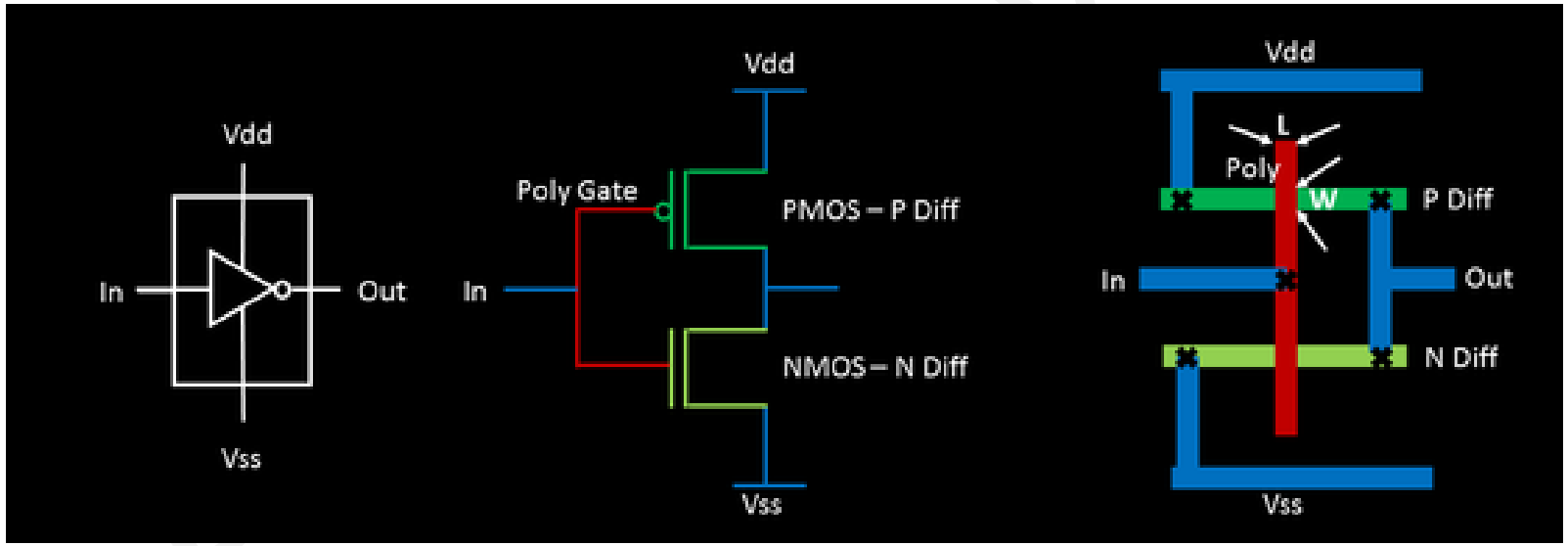
```
set_timing_derate -max -early 0.95
```

This example speeds up the clock path by 5% during setup analysis under maximum PVT operating conditions



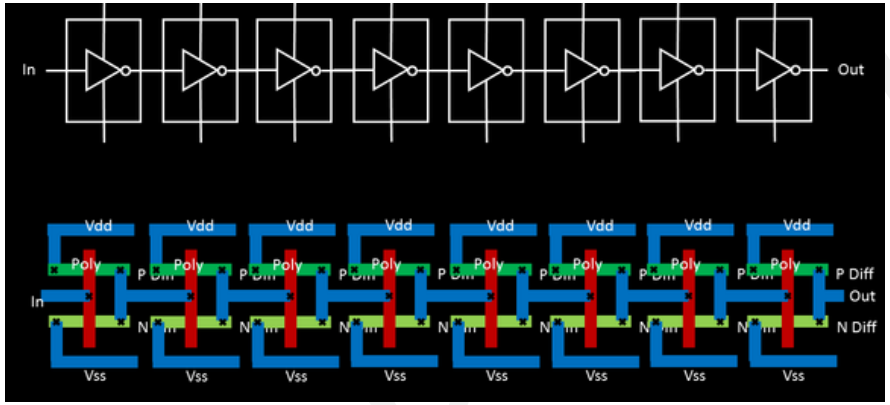
OCV - Sources of variation :- Etching

Sample example of inverter layout and it's also showing the "W" and "L" parameter

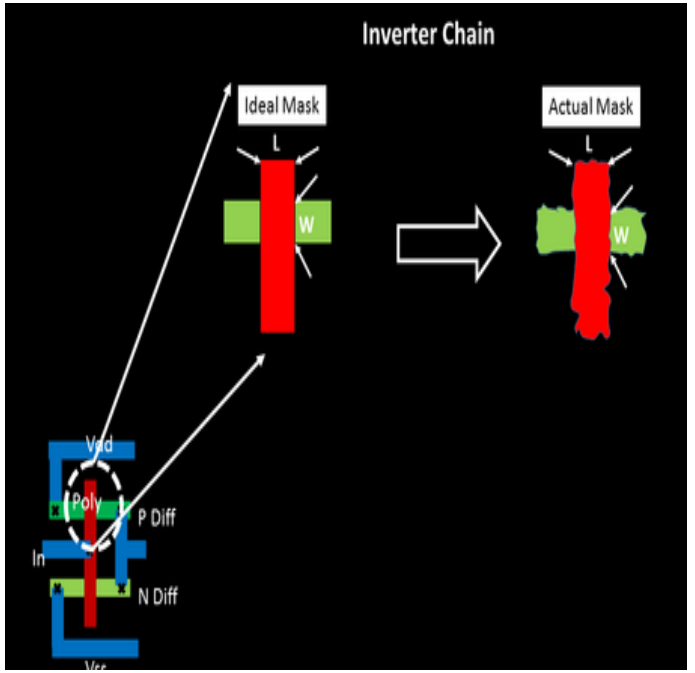


OCV - Sources of variation :- Etching cntd..

- Lets look at the chain of inverters to understand the impact of etching

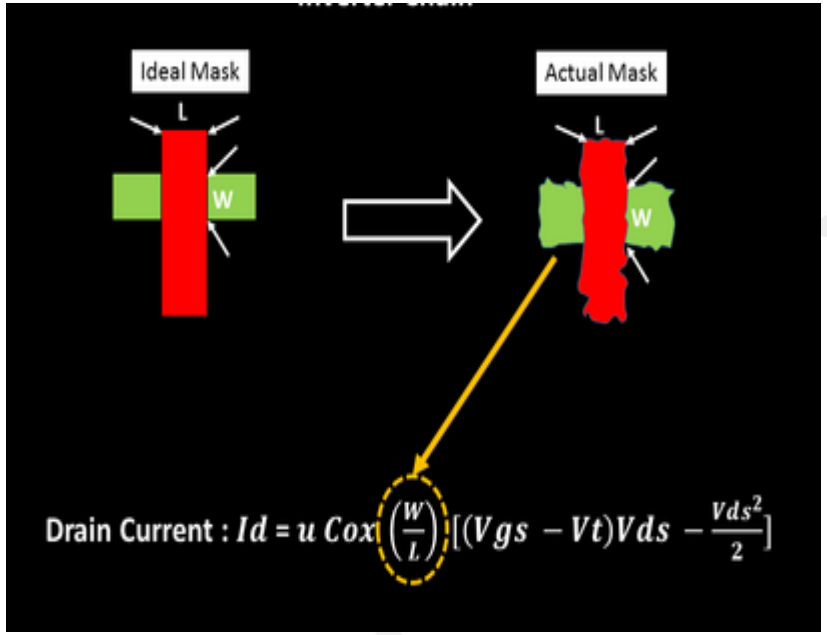


Ideal scenario



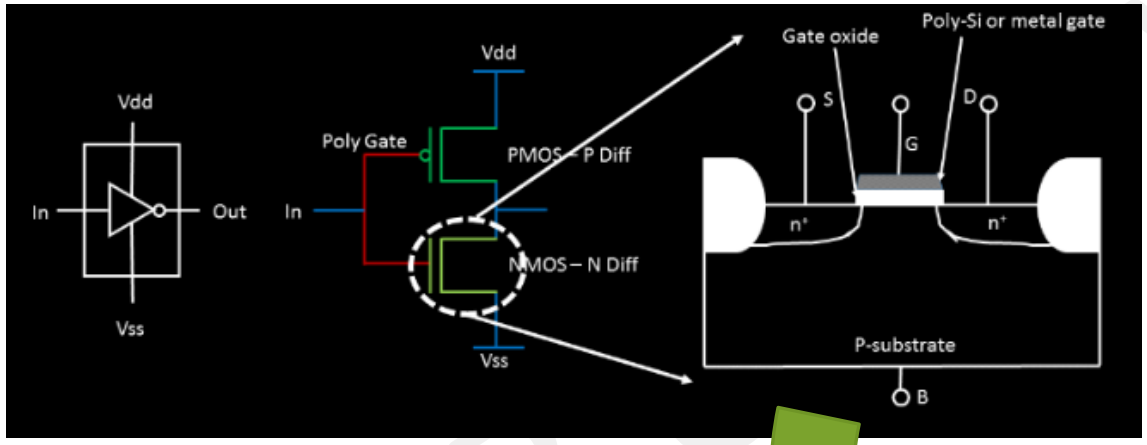
- Photo lithography fabrication technique to build the inverters on silicon wafer and it's the non ideal process , where edges will not exactly be straight lines but there will be disturbances,

Etching impact on transistors

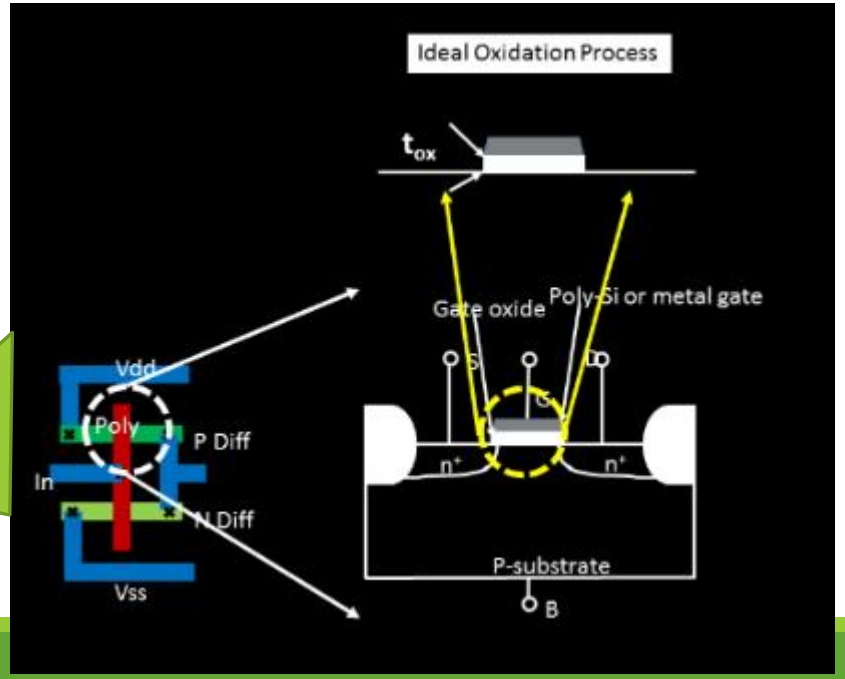


- This variation also dependent on what kind of logic cell which is present on the either sides of this inverter
- if its surrounded by chain of inverters on either sides, the variation on the sides will be less as the process parameters to build mask for a chain of similar size inverter, is almost the same
- But, ***if the inverters are surrounded by other gates, like flip-flops, then the variation will be more***
- *W/L changes it changes on drain current*

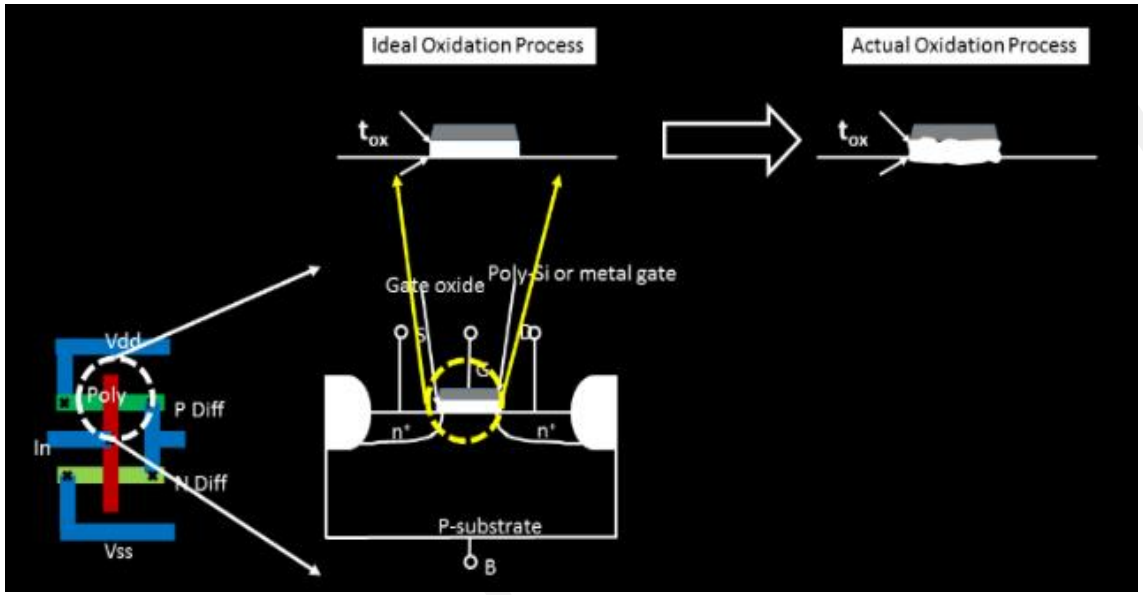
OCV - Sources of variation :-oxide thickness (gate oxide variation)



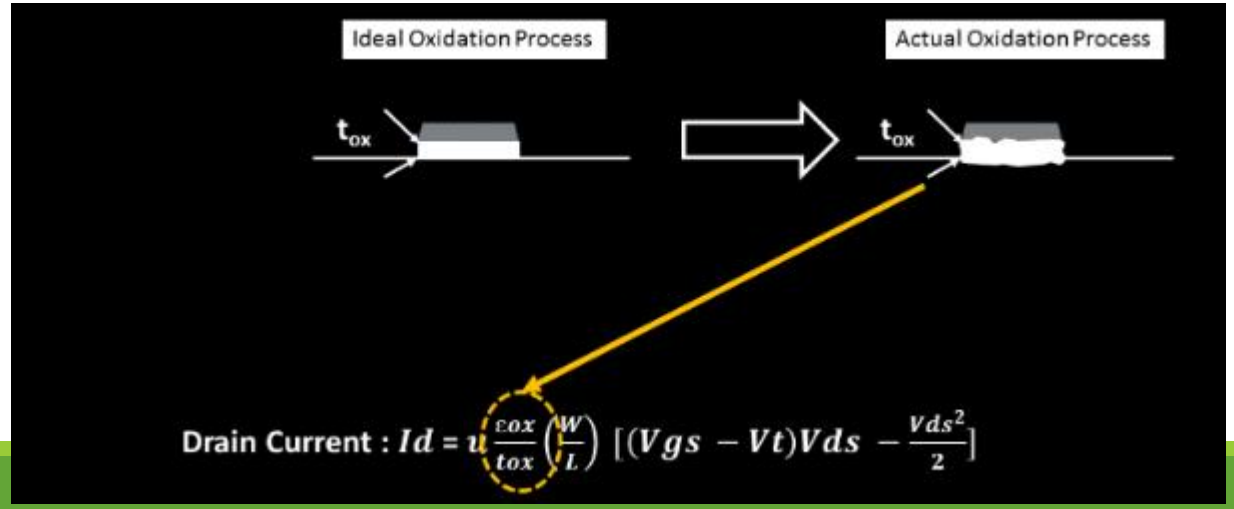
Ideal deposition of oxide layer



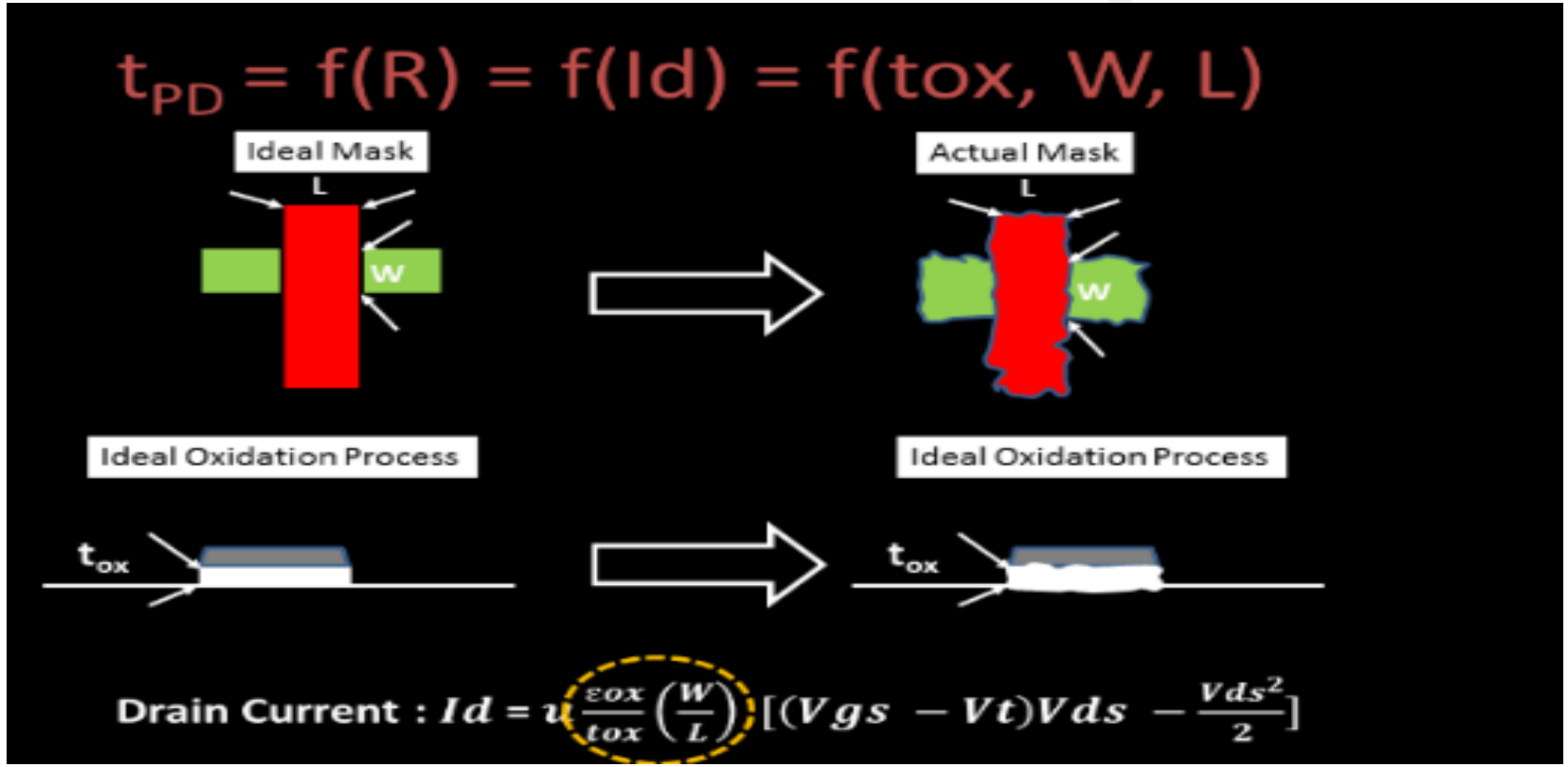
Gate oxide variation



Oxide thickness impacting on your drain current in turn it impact on the cell delay characterization



Process variation on propagation delay



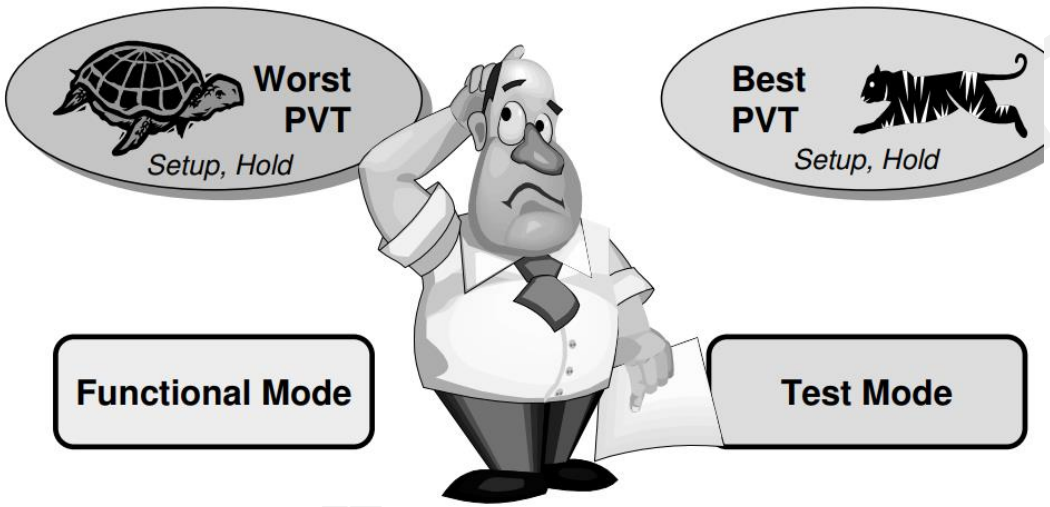
Critical corner for setup and hold cntd….

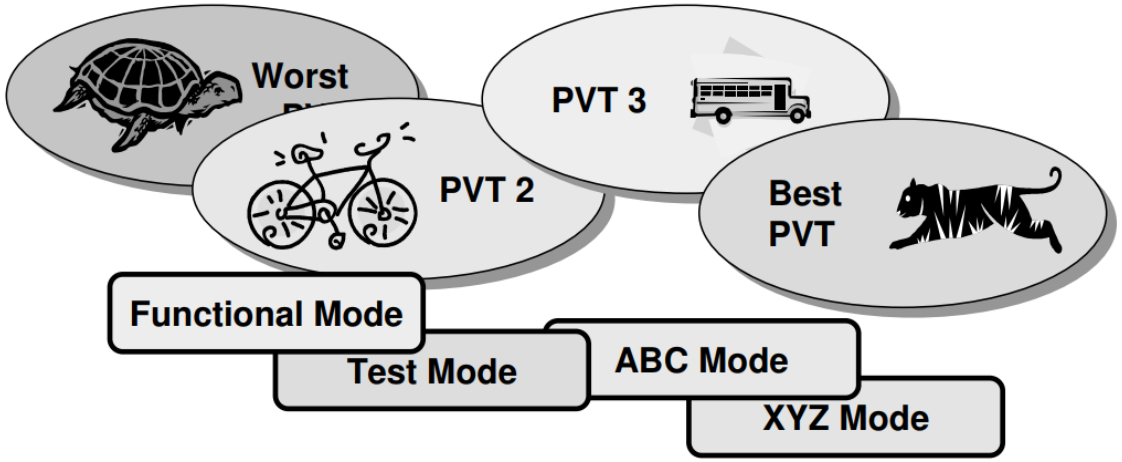
- Now if setup and hold are checked in worst corners, then the chip should work in every scenario. Still we check them in typical corners because we need to analyze power consumption. Refer following table for the worst case scenarios for setup and hold.

	Mode	Process	Voltage(V)	Temperature(°C)	RC/C
Setup	Functional	SS	0.9	125	RC worst/Cworst
	Functional	SS	0.9	-40	RC worst/Cworst
Hold	Functional	FF	1.1	-40	RC best/Cbest

MCMM scenario (Multi corner Multi mode)

- Corners represent a different delay different operating condition
- Modes :- Represents different design timing constraints (Func/Scan)





How many scenarios ?

Problem in having too many scenarios?

1. Memory overhead
2. CPU overhead
3. Run time overhead

Sanity checks on Synthesis netlist

1. check_library :- It checks consistency between logical V/S physical library

2. check_timing: - Implementation tool doesn't optimize timing path if it's not constraints. With the help of this command we can check for any unconstrained paths

3. report_constraints:- it reports WNS/TNS and logical DRC violation

4. report_timing:- It reports timing information about design and it reports single critical paths. WNS should be acceptable value.

5. report_qor :- Displays complete QOR information. Timing numbers should be acceptable value.

6. check_design :- check_design checks the current design for consistency. The check_design command checks the internal representation of the current design for consistency, and issues error and warning messages as appropriate.

7. Understanding physical design MCMM (Multi mode and multi corner) scenarios :- This feedback you can get it from Signoff timing team

“check_design” checks

1. Undriven outputs
2. Unloaded inputs
3. Shorted outputs
4. Multidriven nets
5. Constant outputs
6. Cells do not drive
7. Pins connected to PG
8. Unloaded nets

LAB TIME…!

LAB exercise

1. Sanity checks on the Synthesis Outputs/PNR inputs
2. ZIC timing checking to ensure check on high fanout/unconstrained paths in the design
3. Creation of design setup MW library
4. Practice design setup GUI options


THANKS