STA INTERVIEW QUESTIONS AND ANSWERS

By

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SYNOPSYS

ROUND 1:

1. How to fix setup?

Setup fixes are:

- Upsizing the cell
- Vt swapping from HVT to LVT cells
- Pulling the launch clock
- Pushing the capture clock
- Insert Buffer when the net is dominant
- Metal width is increased
- Metal jogging from lower metals to higher metals
- Use of spare cells after BTO.
- We can use metal buffer's after BTO when net is dominant
- Frequency can be reduced.

2. How to fix DRV?

- **Max Tran**:
  - Upsize the cell
  - Insert a buffer when the net is dominant
  - Buffer can be replaced with Inverter pair.
  - Move the cells nearer
  - Vt Swapping from HVT to LVT
  - Metal width increases
  - Metal jogging from lower to higher metals.
- **Max Cap/ Fanout**:
  - Upsize the cell
  - Load splitting
  - Cloning
  - Swapping

3. How many Corners you worked?

I worked on 24 corners.

Setup Dominant Corners:

Modes	PVT Corners(Slow Corner)	RC Corners
Func Mode	0.72V,1Process,-30C	Cworst-CCworst
Func Mode	0.72V,1Process,125C	Cworst-CCworst

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Test Mode	0.72V,1Process,-30C	Cworst-CCworst
Test Mode	0.72V,1Process,125C	Cworst-CCworst
Func Mode	0.72V,1Process,-30C	RCworst-CCworst
Test Mode	0.72V,1Process,-30C	RCworst-CCworst
Func Mode	0.72V,1Process,125C	RCworst-CCworst
Test Mode	0.72V,1Process,125C	RCworst-CCworst

Hold Dominant Corners:

Modes	PVT Corners(Fast Corner)	RC Corners
Func Mode	1.05V,1Process,-30C	Cbest-CCbest
Test Mode	1.05V,1Process,-30C	Cbest-CCbest
Func Mode	1.05V,1Process,125C	Cbest-CCbest
Test Mode	1.05V,1Process,125C	Cbest-CCbest
Func Mode	1.05V,1Process,-30C	RCbest-CCbest
Test Mode	1.05V,1Process,-30C	RCbest-CCbest
Func Mode	1.05V,1Process,125C	RCbest-CCbest
Test Mode	1.05V,1Process,125C	RCbest-CCbest

Eg:

Corner Name	**Interconnect Wire**
0.720V_0.720V_ssg_-30C_CW_CCW	CWorst_CCWorst
0.720V_0.720V_ssg_125C_CW_CCW	CWorst_CCWorst
0.720V_0.720V_ssg_-30C_RCW_CCW	RCWorst_CCWorst
0.720V_0.720V_ssg_125C_RCW_CCW	RCWorst_CCWorst
1.05V_1.05V_ff_-30C_Cb_CCb	Cbest_CCbest
1.05V_1.05V_ff_125C_Cb_CCb	Cbest_CCbest
1.05V_1.05V_ffg_-30C_RCb_CCb	RCbest_CCbest
1.05V_1.05V_ffg_125C_RCb_CCb	RCbest_CCbest

4. Why that much Corners?

In order to work the chip in all atmospheric conditions.

5. What is the reason for unclocked Flops?

Reasons for unclocked flops are:

- Missing Clock Definitions

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- Missing Timing Arcs in the library
- When case analysis is set
- When set_disabeling_timing is set
- When Mux selection is not proper
- When the clock i/p is tied High/Low

6. What are all the sanity checks you have done?

- **Linking Checks** :

  We need to check, is there are any missing modules or missing pins in library. This is done by link_command.

- **Constraint Checks**:

  In Constarint Checks we need to check the SDC, i.e if there are any no-clock, no-input delay, unconstrained endpoints. This is done by check_timing

- **Parasitic Checks**:

  In Parasitic Checks we need to check for not annotated nets. This is done by Report_annotated_parasitics.

7. What check_timing will give?

Check_timing will give

- No clock
- No Input_Delay
- No driving cell
- Unconstarined_endpoints
- Generated_clock
- Generic
- Latch_fanout

8. What is not annotated nets?

The nets which do not contain RC values are called as not annotated nets.

9. How many not annotated violations you got?

90

10. For 10nm what is the Tran limit?

250ps

11. What is the limit for Fanout?

35

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12. Do you see any Max Capacitance violations?

Yes, it's around 60

13. What type of reasons for Max Tran violations?

The reasons for Max Tran violations

- When long nets are present
- When the driver cell load capacitance is high
- When driver cell drive strength is less

14. How to fix Crosstalk?

Fixes of crosstalk are:

- Upsize the Victim driver cell
- Downsize the aggressor driver cell
- Spacing between the two nets
- Shielding
- Inserting Buffer at the victim net
- Net deteriorate

15. What are the Reasons for 2w 2s in clock network?

The reason for double width is to avoid the EM violations and double spacing is to avoid crosstalk.

ROUND 2:

16. What is your Project Names?

- Nepali
- Starhawk
- Starlord

17. What is Multicycle Path?

The path which takes more than one cycle to capture the data is called Multicycle path.

18. What is Asynchronous Clocks?

The clocks from different sources are called Asynchronous Clocks.

19. Do you consider Crosstalk for asynchronous clocks?

Yes, by considering the infinite timing window.

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20. What is crosstalk?

Crosstalk is the undesirable voltage transitions between two or more adjacent nets through a coupling capacitance.

21. What is Crosstalk Delay?

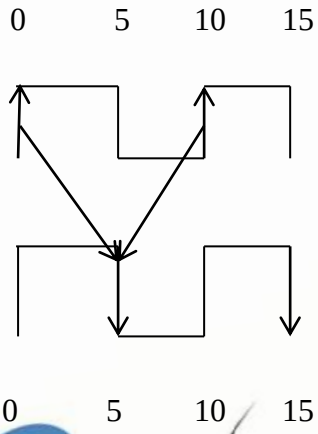
When two nets are switching in same or different directions we get crosstalk delay. Due to crosstalk delay timing is affected.

22. What are Half Cycle paths?

The path which takes only half cycle to capture the data is called Half Cycle Path.

23. Draw some Half Cycle path scenarios?

Launch Clock +ve edge triggered & Capture Clock –ve edge triggered



Setup Check: Hold Check:

Launch at 0 Launch at 10

Capture at 5 Capture at 5

24. How timing will effect with crosstalk delay?

When both the nets are switching in the same direction due to crosstalk the delay in the victim is reduced due to this we get hold violations in data path and setup violations in clock path.

When both the nets are switching in the opposite direction due to crosstalk the delay increases in the victim due to this we get setup violations in the data path and hold violations in clock path.

25. Which one is better is inverter pair or buffer?

In hold perspective Buffer is better, in setup perspective inverter pair is better.

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26. What are GBA and PBA?

- **Graph Based Analysis:**
  In GBA the delays are calculated based on the worst slews. It is more pessimistic analysis. It takes less run time compared to PBA.
- **Path Based Analysis:**
  In PBA the delays are calculated based on the actual slews. It is less pessimistic compared to GBA. It takes more run time.

27. What is the difference between Static and Simulation?

STATIC	SIMULATION
1. In static, without considering the input vectors the timing analysis is performed. 2. It is pessimistic analysis. 3. It takes less run time.	1. In simulation, the timing analysis is performed by considering the input vectors. 2. It is accurate analysis. 3. It takes more run time.

ROUND1:

28. How many blocks u handled? Explain about project issues?

I handled 8 blocks and Top.

Project Issues:

- For a path multicycle contraint is applied for setup and didn't applied for hold, there I faced issues.
- A block contains multiple entry points due to that I faced more skew issues
- Faced issues in fixing setup
- Also, faced issues in fixing crosstalk.

29. Why CSS block is difficult?

Because that block contains multiple clock entry points due to that closing CSS block is difficult.

30. How to fix those violations?

I fixed those violations in the top by finding the hierarchical pin in report_timing –include hierarchical_pins and pushed at that pin without effecting the other paths.

31. Setup and hold fixes with waveforms?

Hold Fixes:

Hold fixes are

- Downsizing the cell

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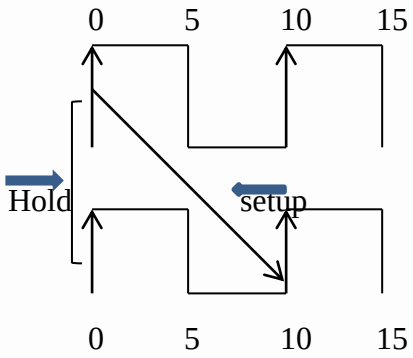
- Vt swapping from LVT to HVT cell
- Pushing the launch clock
- Pulling the capture clock
- Inserting Buffer at D pin
- Metal width decreases
- Net deteriorate
- Using spare cells after BTO
- Inserting metal buf's after BTO
- Voltage can be reduced.



Setup Check: **Hold Check**:

Launch at 0 Launch at 0

Capture at 10 Capture at 0

32. To run Tweaker how many violations u got?

800 violations for hold and 300 for setup

33. How u fix violations in test mode? Did u run tweaker for this?

Mostly in the test mode we see hold violations, fixes of hold violations:

- Inserting Buffer
- Inserting lockup latch

Yes, we can run tweaker for this but I didn't used tweaker for fixing hold in test mode.

34. Explain lockup latch with waveforms?

A lockup latch is a sequential circuit which is used to address hold violations, and skew problems when multiple clock domains are used in a chip. From a DFT perspective it holds the previous scan data, and delays output transition so that the scan data can be effectively captured.

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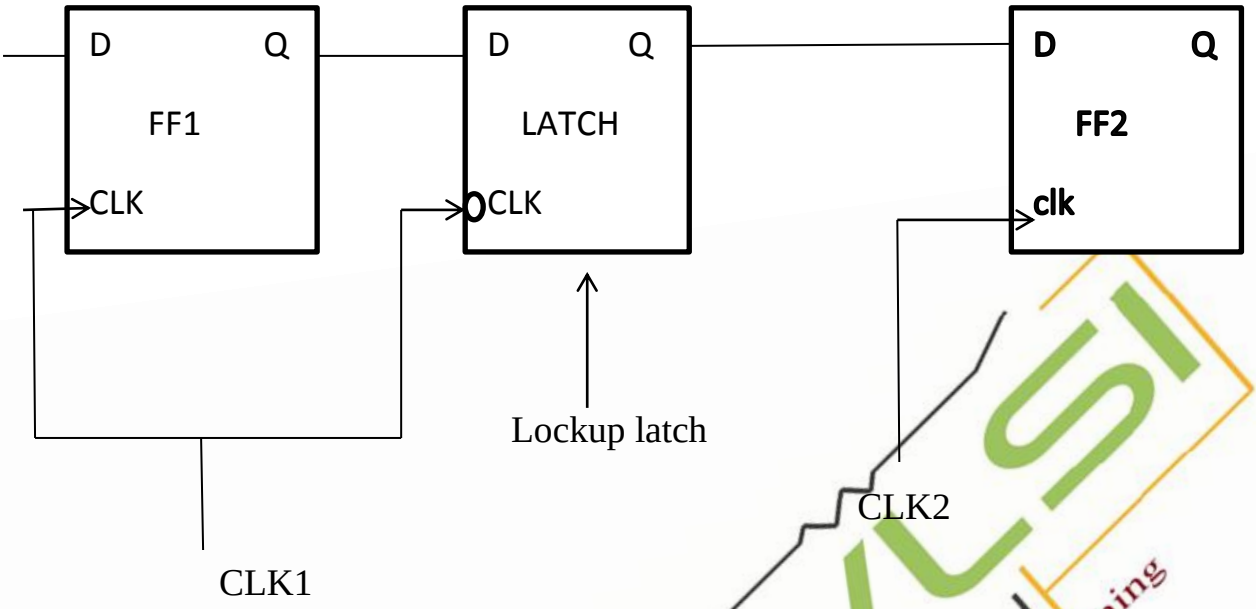
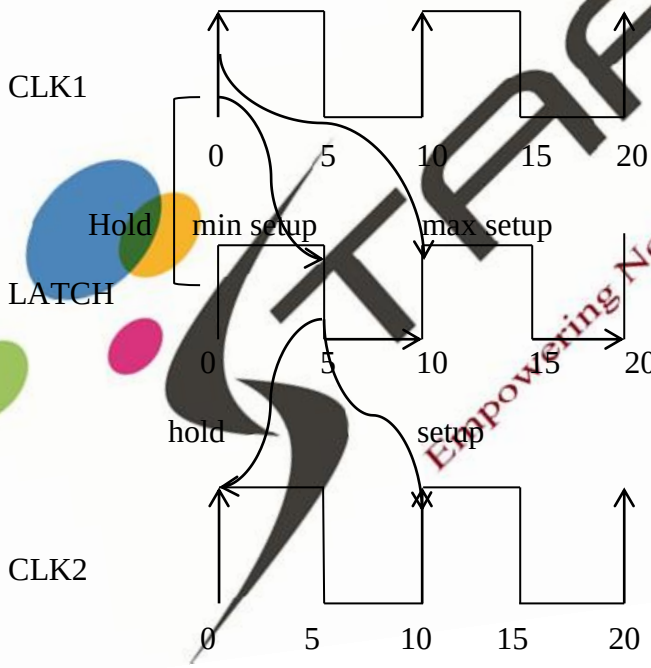


WAVEFORMS:



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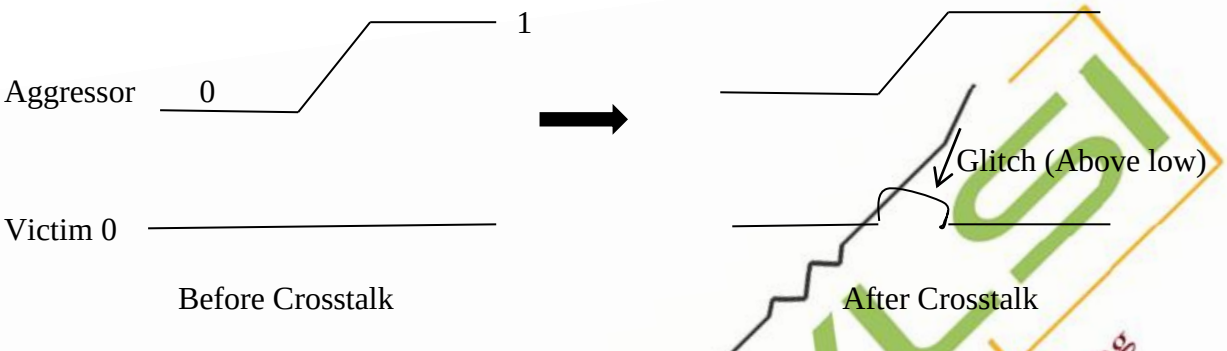
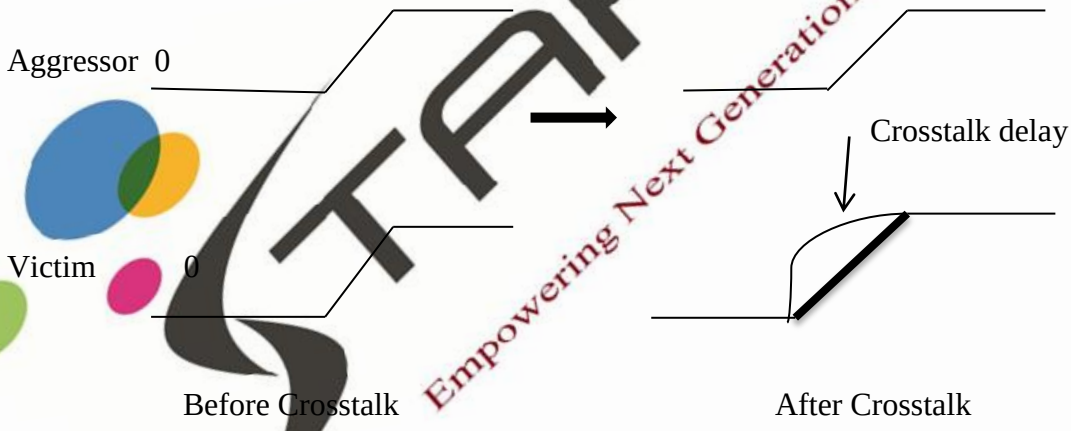
35. What is crosstalk? Explain with Waveforms?

Waveforms:

- Crosstalk Noise:



- Crosstalk Delay:



36. What are the differences between 28nm and 10nm?

28nm	10nm
1. Corners are less 2. Doesn't have more crosstalk issues compared to below technologies.	1. Should work on more corners 2. More crosstalk issues

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XILINX

ROUND1

37. Tell me about your project?

My project name is Nepali. It is 10nm technology. It contains 8 sub HM's, my role in this project is to perform sanity checks and close the timing of all the 8 sub HM's and HM top.

38. What is your role in that?

My role is to perform sanity checks and close the timing of all the sub HM's and HM top.

39. Tell me Tweaker Flow?

To start the Tweaker we need the inputs

- PT sessions
- LEF
- DEF
- Fix Type
- Fix Corners
- Check Corners

First Tweaker invokes the PT Shell and source the tweaker.tcl, then dumps the slack reports from fix corners and TWF from check corners, these are before ECO Reports, then tweaker exit the PT Shell and the load all the inputs

  - Libin
  - Lefin
  - Defin
  - Verilogin
  - Spefin

After loading all these inputs Tweaker generates the ECO's and Incremental files (Verilog, Def, Spef) using the slack reports and TWF using commands Defout, Spefout, Verilogout, and ECOout.tcl. Then Tweaker exit the Tweaker shell and invoke the PT Shell we need to load all the incremental files and generate the reports, these are after ECO Reports.

Then we need to perform what if analysis by observing the before ECO's and After ECO's and we should check the summary reports for how many cells sized or swapped or inserted, if these are valid for that particular violation then we can provide these ECO's to PNR team.

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40. What are the inputs for Tweaker and explain?

Inputs for Tweaker are

- PT sessions
- LEF
- DEF

➢ PT sessions:

PT sessions contains Lib, Verilog, SDC, SPEF

- Liberty File:

It is also called as logical library, it contains the following

- ✓ Cell Functionality
- ✓ Delay Information
- ✓ Timing Information
- ✓ PVT Information
- ✓ DRV's
- ✓ Power Information

- Verilog:

It contains the following

- ✓ Name of the Module
- ✓ Module information
- ✓ Logical connectivity of cells
- ✓ Pin Information
- ✓ Port Information
- ✓ Wire Information
- ✓ Instance Information

- Synopsis Design Constraints:

It contains the following

- ✓ Clock Definitions
  - Create_Clock
  - Create_Generated_Clock
  - Virtual clock
- ✓ I/O Delays
  - Input Delays
  - Output Delays
- ✓ Path Exceptions
  - False path
  - Multicycle path
  - Max Delay / Min Delay
- ✓ Design Rule Violation's
  - Max Transition
  - Max Capacitance

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- Max Fanout

- Standard Parasitic Exchange Format:

It contains the RC values of all the nets.

- Library Exchange Format:

It contains all the physical information, so it is also called as physical library. There are two LEF's

- Tech LEF
- Cell LEF

- Tech LEF:

It contains metal and via information

- ✓ Metal name
- ✓ Metal Direction
- ✓ Pitch Information
- ✓ Area
- ✓ Minimum Width
- ✓ Minimum spacing
- ✓ Resistivity
- ✓ Max Density
- ✓ Min Density
- ✓ Via Name
- ✓ Type of Via

- Cell LEF:

It contains the cell physical Information

- ✓ Cell name
- ✓ Area
- ✓ Site Information
- ✓ Pin Information
- ✓ Port Information
- ✓ Obstruction

- Design Exchange Format:

It contains all the physical information if the design

- Design name
- Die Information
- Core area Information
- Pin Information
- Row Information
- Grid Information
- Components Information
- Metal Information
- Blockage Information
- Halo Information
- Via Information

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- Wire Information
- Special nets Information

41. How many blocks you worked?

8 blocks

42. Did you give all the corners for Tweaker and Why?

No, we will give only the dominant corners for setup and hold, if we analyse the violations in these corners there may be a chance of fixing the violations in the remaining corners i.e, which are not dominant for setup and hold.

ROUND2:

43. Frequency of your block?

500MHZ

44. What are Setup corners? Why?

Setup Worst Corner: 0.720V,-30C, 1Process CWorst

Because the delays are more in those corners, so we see more setup violations in those corners.

45. What is TWF?

TWF is a Timing Window File it contains the Margins to fix violations.

46. What are Tweaker Commands? How the Tweaker fix those violations?

<u>Tweaker Commands</u>:

- **Commands to read inputs**:
  - ✓ Libin
  - ✓ Lefin
  - ✓ Verilogin
  - ✓ Spefin
  - ✓ Defin
- **Commands to fix violations**
  - ✓ Slkfix -all_max_transition
  - ✓ Slkfix -setup –all
  - ✓ Slkfix –hold –all
  - ✓ Slkfix –noise -all
  - ✓ Slkfix –area_recovery
  - ✓ Slkfix –power_eco
  - ✓ Slkfix –dynamic_power_eco

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- **Commands to set fixes**
  - ✓ Set slk_fix_hold_by_sizing true
  - ✓ Set slk_fix_hold_by_delay_insertion true
  - ✓ Set slk_fix_setup_by_sizing true

- **Commands to extract Reports**
  - ✓ Slk_report –summary
  - ✓ Slk_report –timing_summary
  - ✓ Slk_report –leakage_power
- **Commands to dump outputs**
  - ✓ Ecotclout –pt/icc
  - ✓ Verilogout
  - ✓ Defout
  - ✓ Spefout

47. What is the command for upsize and write the full command?

Size_cell instance_name cell_name

ROUND3

48. What is Setup, Hold, and DRV's?

Setup:

It is the amount of time the data must be stable before the arrival of the clock edge.

Hold:

It is the amount of time the data must be stable after the arrival of clock edge.

DRV's:

DRV's are the design rule violations those are Max Tran, Max Cap, and Max Fanout

49. While you fixing Max Tran my setup is violating? What is your approach to fix setup? There is no scope to optimize datapath and clock path (fully optimized)

My approach to fix setup is to optimize common path. But, while fixing max Tran setup will improve but it will not violate.

50. How many corners you worked in 2 projects?

24 corners in both projects

51. What is corner? Why we consider?

CORNER:

Corner is defined as a set of libs characterized for process, voltage and temperature.

To work the chip in all conditions corners are considered.

52. Why only that much of corners?

These corners covered all the possible PVT conditions that a chip can work in any condition.

53. Why list of corners increased in recent project?

In my projects I worked on 24 corners only but with different voltages.

But, as we move towards the below technology the net delays are dominant than the cell delay so we need to work in more corners.

54. Who told you to run? (Corners)

My lead

55. How he can know (lead) to run that much corners only? Who told him?

Based upon the project application the corners are decided, there will be a page of corners may be he took from that.

56. Where is your native place and why you want to change location?

My native place is Vizag, to explore more on the design side I want to change the location.

ROUND1

57. What is Tweaker?

Tweaker is an ECO generation tool.

58. What is Setup?

It is the amount of time the data must be stable before the arrival of clock edge.

59. Is there any other option other than DRV, Setup, and Hold?

Yes, there is power recovery, and Area recovery.

60. How many iterations for ECO?

5 iterations

61. How many projects you done for timing?

2

62. How Tweaker will do upsize?

By setting slk_fix_setup_by_sizing true

Slk_fix_hold_by_sizing true

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ROUND2

63. How upsize will help for fixing the setup violations?

Upsizing means increasing the drive strength, if drive strength increases the width of the gate increases, if width increases the resistance reduces, as resistance and delay are directly proportional to each other if resistance reduces the delay also reduces in this way upsizing will help in fixing setup violations.

64. How to extract Spef?

The inputs to extract Spef are

- Lef
- Def
- QRC tech file

All these inputs are given to the StraRC Extraction tool to get the RC values

65. What type of data you give in Tweaker setup file?

We need to give the following data in Tweaker setup file:

- PT Sessions
- LEF
- DEF
- Fix Type
- Fix Corners and
- Check Corners

66. PT flow?

In order to start PT we need the inputs

- Lib
- Verilog
- SDC
- SPEF

Then we should perform sanity checks

- Linking Checks
- Constraint Checks and
- Parasitic Checks

Then we should analyse the reports using

- Update_timing
- Report_Qor
- Report_timing
- Report_Constraint –all_violators

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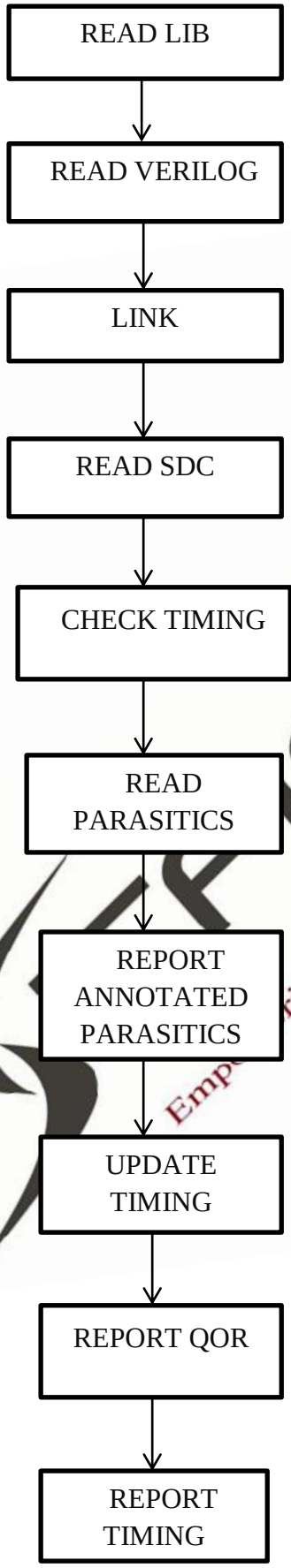
FLOW:


READ LIB
READ VERILOG
LINK
READ SDC
CHECK TIMING
READ PARASITICS
REPORT ANNOTATED PARASITICS
UPDATE TIMING
REPORT QOR
REPORT TIMING

67. What are all the inputs to PT?

Inputs for PT are

- Lib
- Verilog
- SDC
- SPEF

ROUND1:

68. What is your gate count?

2.3 Million

69. What is the WNS of the design?

-100ps

70. How many approximate setup and hold violations?

Setup - 300 violations

Hold - 800 violations

71. What is STA execution and extraction?

STA Execution means loading all the inputs generate the timing reports and analyse the reports.

STA Extraction means extracting the SPEF by StarRC extraction tool by loading the inputs.

72. What are the information present in Extraction and Execution?

Extraction contains R and C values

Execution contains timing reports.

73. What is the voltage and temperature of design?

Slow Corner:

Voltage 0.720V, Temperature -30C

Fast Corner:

Voltage 1.05V, Temperature -30C

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74. What are the best corners and worst corners in your design?

Setup:

- **Worst Corners:**

PVT Corners	RC Corners
0.720V, -30C, 1Process	CWorst
0.720V, 125C, 1Process	CWorst
0.720V, -30C, 1Process	RCWorst
0.720V, 125C, 1Process	RCWorst

- **Best Corners:**

PVT Corners	RC Corners
1.05V, -30C, 1Process	CBest
1.05V, 125C, 1Process	CBest
1.05V, -30C, 1Process	RCBest
1.05V, 125C, 1Process	RCBest

Hold:

- **Worst Corners:**

PVT Corners	RC Corners
1.05V, -30C, 1Process	CBest
1.05V, 125C, 1Process	CBest
1.05V, -30C, 1Process	RCBest
1.05V, 125C, 1Process	RCBest

- **Best Corners:**

PVT Corners	RC Corners
0.720V, -30C, 1Process	CWorst
0.720V, 125C, 1Process	CWorst
0.720V, -30C, 1Process	RCWorst
0.720V, 125C, 1Process	RCWorst

75. Don't you check FF for Setup? Why we have to check FF for Setup?

No we doesn't check FF for Setup because in Fast -Fast the delays are less, there is no chance of getting setup violations.

76. What we have to give in Tweaker data?

- PT Sessions
- Lef
- Def
- Fix Type
- Fix Corners
- Check Corners

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77. What are the methods you gave for your Design?

- ✓ Set slk_fix_hold_by_sizing true
- ✓ Set slk_fix_hold_by_delay_insertion true
- ✓ Set slk_fix_setup_by_sizing true

ROUND2:

78. From which company you are from?

Qualcomm

79. Why you are leaving that company?

Since starting of my career I'm working on the same type of designs, I want to explore on more designs.

80. In General what you will do as a STA Engineer?

As a STA Engineer we need to close the timing in all the corners.

81. What is the information present in SDF and TWF?

Timing Window File:

TWF contains all the margins

Standard Delay Format:

It contains

- Cell Delays
- Timing Checks
- Interconnect Delays

82. How you generate Tweaker in tool?

Tweaker_shell

83. First what you will analyse after getting PNR Database?

First we need to perform the sanity checks, then we should analyse the timing reports.

84. From report how you will get to know where you have to use the types of fixes for setup and hold?

First we should see the slack and then we should check the datapath, for setup we should see which cell is contributing more delay, we should analyse the reason for more delay, is this delay is due to transition or capacitance or fanout or delta delay, then we should check whether there are any HVT cell or less drive strength cell, if there is a less drive strength cell we can go with upsizing option, or if there is any HVT cell we can go with swapping, then whether there is net dominant if there is net dominant we need to insert the buffer.

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For hold first we need to check the skew, if the skew is balanced then we should see the setup margin, if there is enough setup margin then we can go with insert buffer, if there is no setup margin then we should analyse the datapath, we should see for LVT cells and high drive strength cells, if there are any LVT cells we can go with swapping by checking the setup, in the same way if we have any high drive strength cells then we can go with downsizing by checking setup margin, if there is no setup margin then we should get setup margin and then fix hold.

85. Do you know scripting?

Yes, I know scripting.

86. In general how to see the reports in prime time?

By using report_timing we can see the reports.

87. From report what u has to see? How it will helpful to reduce violations?

First we need to check the Slack and then Startpoint and Endpoint for the clock, then we should check margins of uncertainty, if it is different clock we should check the skew, else if it is of same clock then we should check datapath is optimised properly or not, we should analyse the path and fix the violation with appropriate fixes.

88. What are the reports you will see after ECO? How you will see the observations?

- **Manual ECO:**

  We should see the Report_Qor, Report_Constraint –all_violators, Report_timing.

  - ✓ Report_Qor gives the summarised report i.e; for each path group it gives total negative slack, wost negative slack, number of violating paths, cell count, area, and drv's.
  - ✓ Report_costraint –all_violators gives all the violations i.e; Drv's, setup, hold failing endpoints and slack.
  - ✓ Report_timing gives the worst setup slack in the design

From these reports we need to check the WNS, TNS and number of failing endpoints, if we are fixing hold we should check there are any setup violations are pop upped due to the hold fixes.

- **Tweaker ECO:**

After Tweaker ECO we should do what if analysis between the before ECO and after ECO, we should check the WNS, TNS, number failing endpoints, and then we should check the summarised reports for number of cells inserted, sized, and swapped, check if these number cells are valid for that particular violation or not.

89. Do you saw any blocking codes?

Yes, blocking code summary can be seen by using slkreport –blocking_code –summary filename

Blocking codes occur when don't use cells or don't touch nets are used

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Some general blocking codes are:

- B004 – Doesn't have enough setup margin at TWF after insertion
- B034 – Blocked by DRV fail
  - ✓ Don't allow tran/cap value of each pin connected to eco nets.
- B084 – Blocked by inout pin
  - ✓ Don't allow repeater insertion on inout port nets.
- B083 – Blocked by multi-driven net
  - ✓ Don't allow repeater insertion if the net has multiple drivers.

90. Gave one reg to reg path there is no scope of optimisation in datapath and what you will do know?

If there is no scope of optimisation in data path we need to optimise the common path.

91. Did you done clock skewing in your experience?

Yes, I have done clock skewing using pushing and pulling the clock.

ROUND3:

92. Which team you are from?

WLAN Team

93. Did your team is responsible for one PNR block?

No, our team is responsible for 8 sub HM's and HM top.

94. What are the responsibilities in your design?

Our responsibility is to close the timing in all sub HM's and HM top

95. Tell me the errors you saw in your design?

- **Linking Errors:**
  - ✓ LNK -001: Cannot read link_path file.
  - ✓ LNK -049: Main library is not specified.
- **Constraint Errors:**
  - ✓ PTE -014: No net timing arc from pin to pin.
  - ✓ PTE -025: The master of generated clock is not connected to any clock source.
  - ✓ PTE -075: Generated clock has no path to its master clock.

96. Can you explain how to calculate R and C values?

- Resistance:

$$R = \frac{\rho L}{A}$$

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- Capacitance:

$$C = \frac{\in A}{D}$$

97. Which scripting your learning?

TCL and PERL Scripting.

98. What you have seen in Tweaker log file?

I have seen the summarised reports, errors and warnings.

99. How you will say to PNR team to insert Buffer?

If it is endpoint buffering we give as insert_buffer pin cell_name

If it is net breaking then we should collect those nets and provide those to PNR.

100. How you are getting to know this the most violating path in your design?

By using Report_timing, by default report_timing gives the Worst setup slack in the design.

101. How you fix Noise violations?

Fixes of noise are:

- Upsize the Victim driver cell
- Downsize the aggressor driver cell
- Spacing between the two nets
- Shielding
- Inserting Buffer at the victim net
- Net deteriorate

102. How will you give double spacing in your design by tool?

In Prime Time we cannot do double spacing.

103. How you will downsize the aggressor?

By using Size-Cell, size_cell instance_name(driver which is to be downsized) cell_name

104. How you get to know the noise is violated?

Using Report_Noise command.

105. Did you done any buffer insertion by using Tweaker tool?

Yes, by setting slkfix –hold_by_delay_insertion true.

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106. Tweaker completely avoid the violations know?

No there are some violations

107. What is your approach to fix the remaining vioaltions?

I fixed the remaining violations manually.

108. Did you fixed manually?

Yes, I fixed manually.

109. Are you convenient to relocate?

Yes

ALTRAN

NANDINI

ROUND1

110. Where is LeadSoc?

It is located in HSR Layout.

111. Who is the founder of LeadSoc?

Yaseen

112. How many members in LeadSoc?

Around 150 members.

113. Issues in every project?

Project Issues:

- For a path multicycle contraint is applied for setup and didn't applied for hold, there I faced issues.
- A block contains multiple entry points due to that I faced more skew issues
- Faced issues in fixing setup
- Also, faced issues in fixing crosstalk.

114. What information you give to PD as well as Synthesis team?

- **Synthesis:**
  - If there are any missing constraints in SDC, we will analyse and give the constraints which are not proper.
  - If there are any LVT cells present in the design, we will give feedback to replace these cells with HVT.

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- If all the DRV's and Setup violations are met with margins and all the cells used are of HVT then we will give signoff.

➢ **Physical Design:**

- Placement:
  - ✓ If some paths are not meeting the timing due to over buffering and under buffering, we will give feedback to optimise those paths.
  - ✓ If all the Data DRV's and setup is met with margins or if that violation can be met by sizing or swapping then we will give signoff.
- Clock Tree Synthesis:
  - ✓ If the skew is not balanced, we will give feedback to balance the skew
  - ✓ If there is no minimum insertion delay, we will give feedback to reduce the insertion delay.
  - ✓ If the Clock DRV's, Setup and Hold are met with margins then we will give signoff.
- Routing:
  - ✓ If there are any not annotated nets, we will collect those nets and give them to analyse and provide the RC values for those nets.
  - ✓ If there is any crosstalk issue we will tell them to increase spacing or net deteriorate.
  - ✓ If all the DRV's, Setup, Hold and Crosstalk is met then we will give signoff.

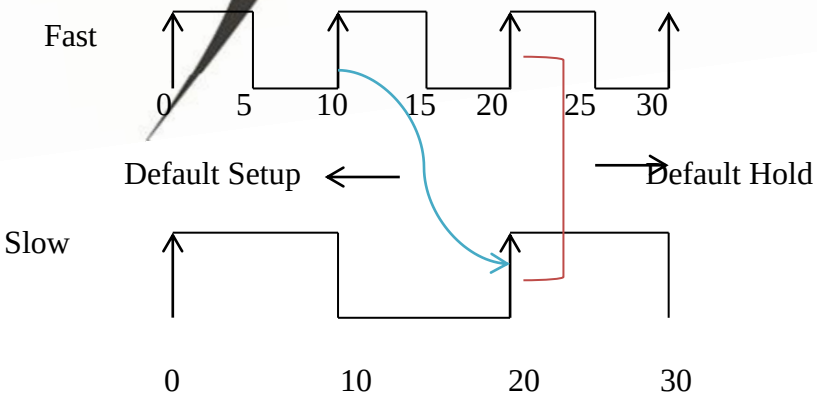
115. How you will see multicycle path issues in PT?

Using Report_timing –exceptions_all

116. Fast to slow, slow to fast how you will apply in PT?

Fast to slow:

Fast to slow means launch clock period is 10 and capture clock period is 20



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Default:

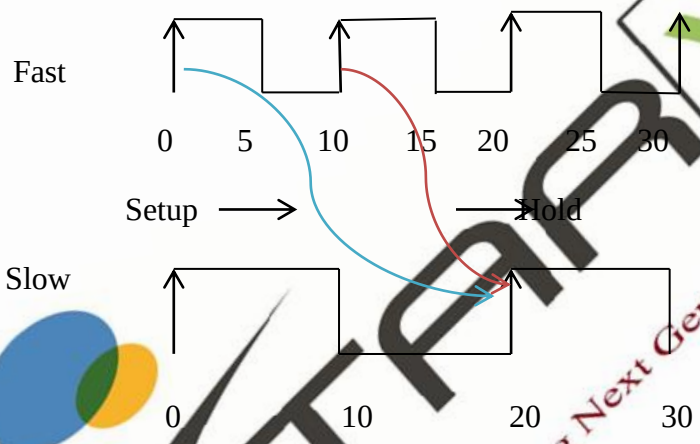
Setup:	**Hold:**
Launch at 10	Launch at 20
Capture at 20	Capture at 20

By default the setup will move in end, hold will move in start. After applying the multicycle path constarints then the directions of setup and hold in start and end are

Start/End	**Setup**	**Hold**
Start	←	→
End	→	←

- **Multicycle path for setup:**

Set_multicycle_path 2 –from [get_clocks Lclk] –to [get_clocks Cclk] –setup -start



After applying multicycle path for setup:

Setup:	**Hold:**
Launch at 0	Launch at 10
Capture at 20	Capture at 20

After applying the setup multicycle the hold is violating due to this we should apply multicycle path for hold.

- **Multicycle path for Hold:**

Set_multicycle_path 1 –from [get_clocks Lclk] –to [get_clocks Cclk] –hold - start

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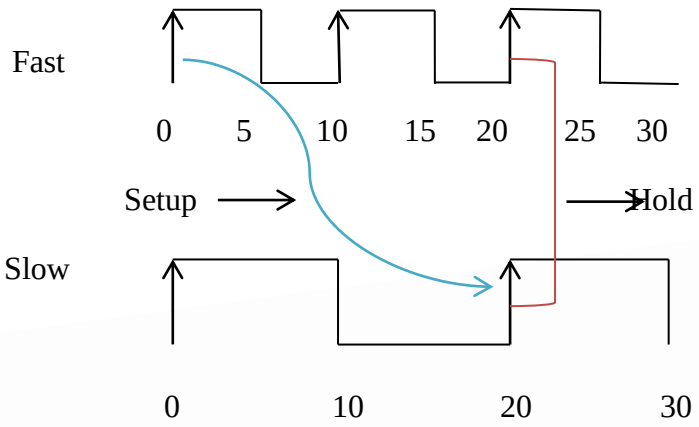
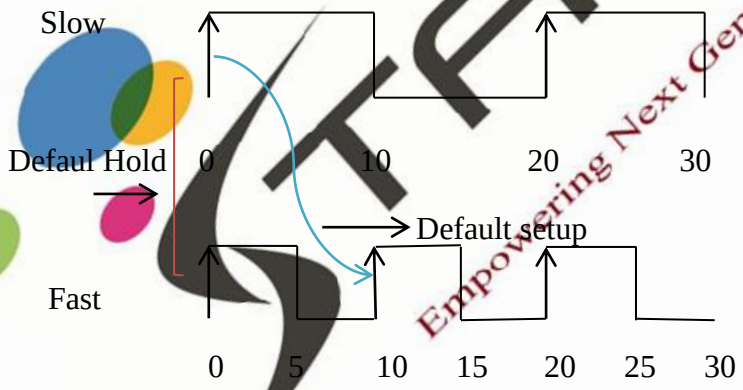


After applying multicycle path for hold:

Setup:	**Hold:**
Launch at 0	Launch at 20
Capture at 20	Capture at 20

Slow to fast:

Slow to fast means launch clock period is 20 and capture clock period is 10



Default:

Setup:	**Hold:**
Launch at 0	Launch at 0
Capture at 10	Capture at 0

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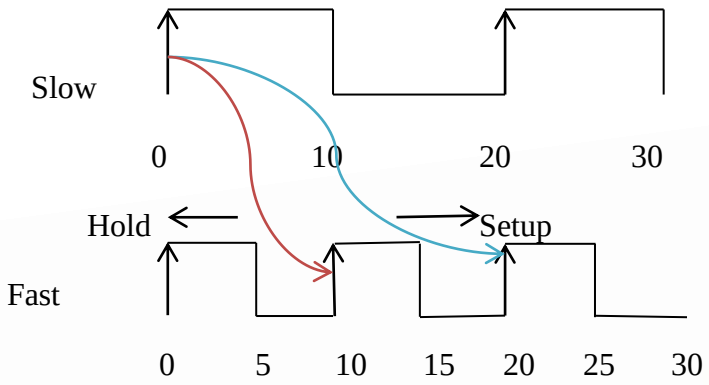
- **Multicycle path for setup:**

Set_multicycle_path 2 –from [get_clocks Lclk] –to [get_clocks Cclk] –setup –end



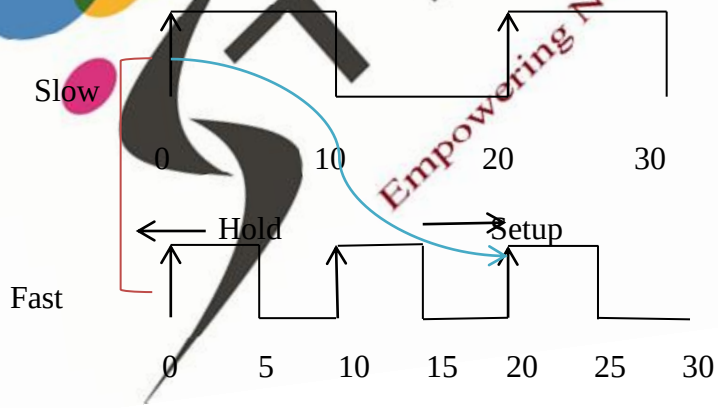
After applying multicycle path for setup:

Setup:	**Hold:**
Launch at 0	Launch at 0
Capture at 20	Capture at 10

After applying the setup multicycle the hold is violating due to this we should apply multicycle path for hold.

- **Multicycle path for Hold:**

Set_multicycle_path 1 –from [get_clocks Lclk] –to [get_clocks Cclk] –hold – end



After applying multicycle path for hold:

Setup:	**Hold:**
Launch at 0	Launch at 0
Capture at 0	Capture at 20

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117. Will you apply clock gating for half cycle paths or full cycle paths?

We can apply clock gating for both half cycle and full cycle paths based upon the requirement.

118. What are the crosstalk issues?

Due to the crosstalk we get the timing and noise violations

- When both the nets are in switching condition then we get setup or hold based upon the direction.
- When one net is static and other net is switching then we get noise violation, due to noise the functionality will be affected.

119. Can u say about func mode and capture mode?

- **Func Mode:**

Func mode is to test the functionality, the frequency of the func mode is 10 times more than the test mode.

- **Capture Mode:**

  Capture mode is also called as At Speed Mode, Capture mode is one type of mode in Test mode, test mode is to test the manufacturing defects, Capture mode works with the frequency of func mode.

120. What are the challenges you faced?

Challenges:

- For a path multicycle constraint is applied for setup and didn't apply for hold, there I faced issues.
- A block contains multiple entry points due to that I faced more skew issues
- Faced issues in fixing setup
- Also, faced issues in fixing crosstalk.

121. What are the approaches to fix those violations?

- For a path multicycle constraint is applied for setup and didn't apply for hold, there I faced issues.
  - ✓ I resolved that by applying the multicycle constraint for hold only for analysis purpose, I given feedback to the Constraint team.
- A block contains multiple entry points due to that I faced more skew issues.
  - ✓ I fixed those violations in the top by finding the hierarchical pin in report_timing –include hierarchical_pins and pushed at that pin without affecting the other paths.

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- Faced issues in fixing setup
  - ✓ I resolved those by analysing the paths and fixed with appropriate fixes.
- Also, faced issues in fixing crosstalk.
  - ✓ I resolved those by analysing those paths and fixed those violations with appropriate fixes.

122. How you will give to ECO tool to fix setup?

➢ **Tweaker Tool:**
- In the fix type we should give setup.
- In fix corner, worst corners of the setup are given.
- In check corner, hold corners are given.
- We can set the methods for upsizing and inserting.
- The command to fix setup is slkfix –setup –all

➢ **PT:**
- Fix_eco_timing –type setup –method inserting/sizing –cell_list

123. Did you write any manual Eco's?

Yes, I wrote manual Eco's.

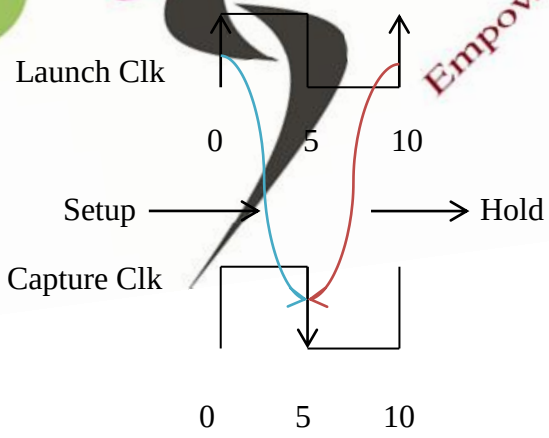
124. In any scenario hold depends on clock?

Yes, during half cycle paths hold is depended on frequency.

Half cycle path:

When launch clock is positive edge and capture clock is negative edge (and vice versa) those paths are called half cycle paths.

Launch Clk – positive edge Captured Clk – negative edge



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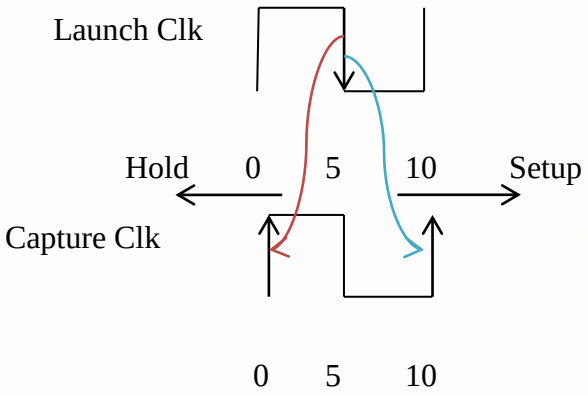
Setup: **Hold:**

Launch at 0 Launch at 10

Capture at 5 Capture at 5

Launch Clk – negative edge Captured Clk – positive edge



Setup: **Hold:**

Launch at 5 Launch at 5

Capture at 10 Capture at 0

125. What is the command to see all the violations?

Report_constraint –all_violators

126. How to fix 2 setup violations? How many sessions u load in PT (only setup Corners or both setup and hold corners)?

First we should see the WNS then we should analyse the paths, is it a same start point or different start points, If it is single start point then we should forward trace and fix with appropriate fixes.

If it is multiple start points then we should analyse the paths individually, first we should analyse which cell is contributing more delay is it due to tran, cap, and crosstalk delta then we should fix that violation using sizing or swapping.

We should give both setup and hold corners.

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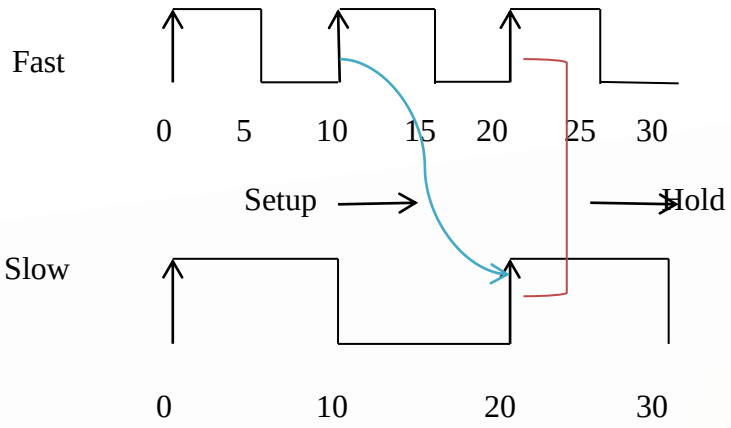
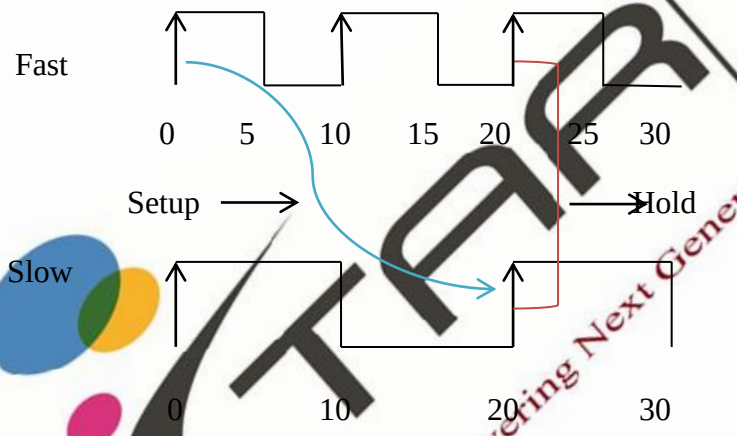
127. In MultiCycle path which constraints having START and why?

When the launch clock is fast and capture clock is slow then those constraints will have START option, because the changes should be made in the START only.

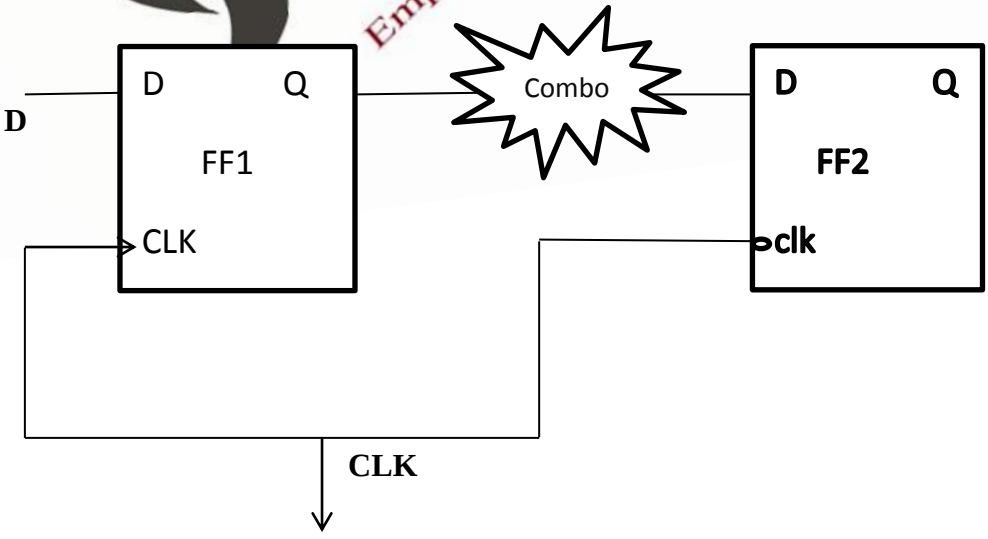


Set_multicycle_path 2 –from [get_clocks Lclk] –to [get_clocks Cclk] –setup -start

Set_multicycle_path 1 –from [get_clocks Lclk] –to [get_clocks Cclk] -hold - start



128. Setup and hold calculations for Halfcycle paths?



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- **Setup:**

Setup Time = Required Time – Arrival Time

Arrival Time = Launch Clk + Launch Clk Latency + TCQ + Tcombo

Required Time = Capture Clk + Capture Clk Latency – Tsetup –Tuncertainty + CRPR

- **Hold:**

Hold Time = Arrival Time – Required Time

Arrival Time = Launch Clk + Launch Clk Latency + TCQ + Tcombo

Required Time = Capture Clk + Capture Clk Latency +Thold +Tuncertainty – CRPR

129. How skew helps to fix setup?

To fix setup we pull the launch clock and push the capture clock.

- Pulling the launch clock means reducing the delays in the arrival time by using the sizing or swapping or removing the buffers without violating the tran, by reducing the arrival time the setup slack improves.
- Pushing the capture clock means adding the delays in the required time by using the sizing or swapping or inserting the buffers, by increasing the required time the setup slack also improves.

130. Is setup and hold will fail in same path? How?

Yes, when there are more variations in the data path and when there is crosstalk in common path both setup and hold fail in the same path. The CRPR is removed for hold and it does not remove for setup when the crosstalk is present because the setup is considered at different edges due to this the setup and hold will fail in same path.

131. Do you know synthesis flow?

The inputs of synthesis are

- Lib
- RTL
- SDC

Then we should perform the sanity checks

- Linking checks/ Elaboration
- Design checks
- Constraint checks

Then compile ultra should be done and then analyse the reports using

- Report_timing

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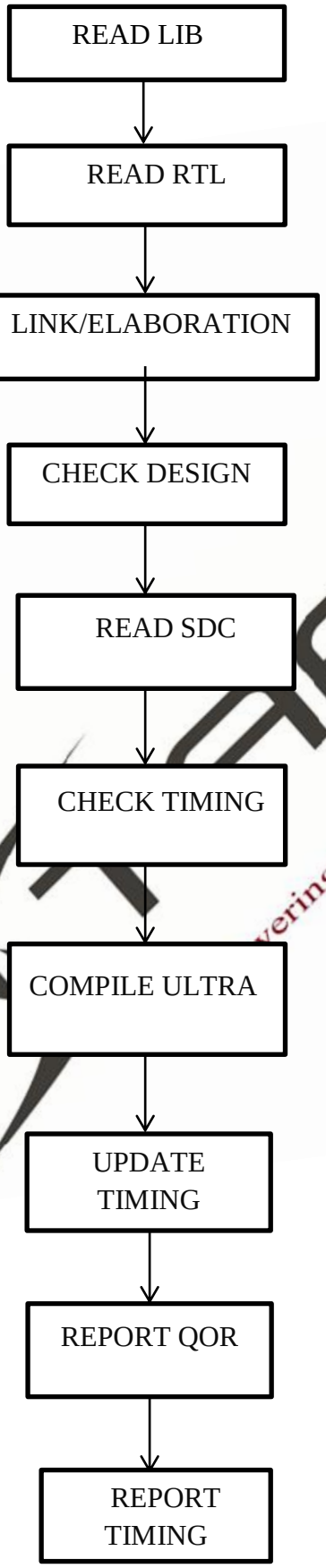
- Report_qor
- Report_constraint –all_violators

Synthesis Flow:



132. What you will do in elaboration in synthesis flow?

Elaboration:

It is the process of expanding HDL description to represent all instances of module into unique objects (GTECH Cells).

133. What is pipelining?

Pipelining is the method of inserting the intermediate stages to reduce the combinational delay.

134. Do you write any manual ECO's? How?

Yes, I wrote manual ECO's, analysed the violations and fixed using size_cell and insert_buffer commands.

135. What is OCV?

On Chip Variation:

OCV is the intra chip variation, all the portions of the chip varies due to Process, Voltage, and Temperature, in order to model these variations different derating factors are applied to the launch path and capture path.

136. How you can say the setup is violated because of constraint issue?

If there is a multicycle path in the design, and the constraint is not applied to that path then we get setup violation.

137. If you add buffer how timing will effect?

If the buffer is added in the launch path there may be a chance of getting setup violations and reduce the hold violations.

If the buffer is added in the capture path there may be a chance of getting hold violations and reduce the setup violations.

138. Instead of buffer why can't u use pair of inverters? Is there any difference in terms of delays?

When there are long nets we use inverter pairs, if we use inverter pairs for short nets more area will be utilised so buffers are preferred for short nets.

But buffers consume more delay compared to the inverter pairs, inverter pairs improves the tran than the buffer.

139. In long Data path, Net delay is dominating cell delay, Will u use pair of inverters?

Where u insert those two?

Yes, we can use pair of inverters in long path but the cell delay must be less than the net delay. Based upon the distance we should add the inverter pair.

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140. Tell me inputs and outputs of Synthesis?

Inputs:

The inputs of synthesis are

- Lib
- RTL and
- SDC

Outputs:

- Gate level Netlist and
- Reports
- Updated SDC

MOCK INTERVIEW QUESTIONS

141. What is the difference between the 14nm and 10nm?

14nm	10nm
1. Corners are less 2. Doesn't have more crosstalk issues compared to below technologies.	1. Should work on more corners 2. More crosstalk issues

142. How many corners you worked in Placement, CTS, Routing?

- **Placement:**

In Placement I worked on 2 worst setup corners.

PVT Corners	RC Corners
0.720V, -30C, 1Process	CWorst
0.720V, 125C, 1Process	CWorst

- **Clock Tree Synthesis:**

In CTS I worked on 4 corners, 2 setup worst corners and 2 hold worst corners.

✓ **Setup:**

PVT Corners	RC Corners
0.720V, -30C, 1Process	CWorst
0.720V, 125C, 1Process	CWorst

✓ **Hold:**

PVT Corners	RC Corners
1.05V, -30C, 1Process	CBest
1.05V, 125C, 1Process	CBest

- **Routing:**

  In Routing stage I worked on the 4 corners, 2 setup worst corners and 2 hold worst corners.

  ✓ **Setup:**

PVT Corners	RC Corners
0.720V, -30C, 1Process	CWorst
0.720V, 125C, 1Process	CWorst

  ✓ **Hold:**

PVT Corners	RC Corners
1.05V, -30C, 1Process	CBest
1.05V, 125C, 1Process	CBest

143. Difference between function mode and test mode?

- **Func Mode:**

Func mode is used to test the functionality, the frequency of the func mode is 10 times more than the test mode.

- **Test Mode:**

  Test mode is to test the manufacturing defects, the frequency of test mode is 10 times less than func mode.

144. Difference between pre layout STA and post layout STA?

Pre Layout STA	Post Layout STA
1. In Pre Layout STA ideal clocks are present. 2. Clock Uncertainty will be more because skew is not balanced. 3. Both source and network latencies are constrained from SDC.	1. In Post Layout STA propagated clocks are present. 2. Clock Uncertainty will be less because skew is balanced. 3. Only source latency is constrained from SDC, network latency is considered from the real values.

145. What is CRPR?

Clock Reconvergence Pessimism Removal:

During OCV analysis, different derates are applied to the launch path and capture path, the cells present in the common path cannot drive both max and min delay at a time in order to reduce this pessimism the CRPR is introduced, the pessimism is taken by subtracting the min delay from max delay.

146. Who is your manager?

Basha

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147. How many clocks are there in your design?

4 clocks, 3 synchronous and 1 asynchronous clocks.

148. Difference between master clock and generated clock?

- **Master Clock:**

  It is the clock defined from the clock source i.e; PLL

- **Generated Clock:**

  It is the clock generated internally in the design using master clock.

149. What are flat SPEF and SPEF Stich?

- **Flat SPEF:**
  In Flat SPEF, LEF and every block DEF is considered and a single SPEF is generated for each corner.
- **SPEF Stich:**
  In SPEF stich, every block SPEF is considered and then integrated to top as a single SPEF for each corner.

150. Did u face any issues in Multicycle path and Halfcycle path?

I faced issues in Multicycle path, multicycle constraint is applied for the setup and the constraint for hold is missed due to that I faced issues in those paths.

151. If u has linking issues what u did?

If there are any linking issues, first we should check the path which is given properly or not, if the path is proper then we should inform to the library team.

152. If u has 1ns setup violation what is your approach?

First we should check is this is a real issue or constraint issue, if it is a constraint issue we should analyse and inform to the constraint team.

If it is a real issue then we should check whether the violation is due to over buffering or under buffering.

Then, we should check the startpoint and endpoint for the clock if it is different clock then check the number of failing endpoints, if the number of failing endpoints is more then we address the violation by using pushing and pulling. If it is a single startpoint and multiple endpoints then we should forward trace and address the violation till the divergent point.

If it is multiple startpoint and single endpoint then we should back trace and address the violation till the divergent point.

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If it is multiple startpoints and multiple endpoints we should analyse the paths individually. We should check the datapath, and analyse which cell is contributing more violation is it is due to tran, cap, fanout, crosstalk delta or due to net dominant.

If any net dominant is there we can insert buffer when the cell delay is less than the net delay, then we should check is there are any low drive strength cells in the path, if there are any low drive strength cells then we should check hold margin and can upsize the cell, if there are any HVT cells we can swap from HVT to LVT.

153. What is no clock and unconstrained endpoints?

No clock means the flops does not contain clock.

Output port, D pin/ SI pin are the unconstrained endpoints, Output port will come when the port does not contain output delay and D pin/ SI pin when the clock is missing to the flop.

154. If u has 5ps hold violation and insert buffer option is not there what is your approach?

We can fix that by downsizing or Vt swapping from LVT to HVT by seeing the setup margin.

155. How u will apply derates for both setup and hold?

- **Setup:**
  For setup derates are added to the launch path i.e; late path and reduced in the capture path i.e; early path.
  Command for applying derates are:
  By default the value will be 1 for both late path and early path, if we apply 10% derate the values changes as below
  Set_timing_derate – late 1.1 –data
  Set_timing_derate – early 0.9 – clock
- **Hold:**
  For hold derates are added to the capture path i.e; late path and reduced in the launch path i.e; early path.
  Command for applying derates are:
  By default the value will be 1 for both late path and early path, if we apply 10% derate the values changes as below
  Set_timing_derate – late 1.1 – clock
  Set_timing_derate – early 0.9 – data

156. If your hold is violating with 100ps and there is no option of fixes and your setup margin is 100ps what is your approach?

First we should get the setup margin by reducing the common path and replace the cells with less variation cells i.e; variation between max and min

delay will be less. After getting the setup margin we can fix hold using inserting buffer or sizing.

157. After Performing sanity checks what u did?

After performing the sanity checks, generated the timing reports, analysed the reports and fixed the violations.

158. In a path if u has 10 cells and both setup and hold are violating what is your approach (Divergence, Through Path)?

We should reduce the common path, and replace those cells with less variation cells and fix setup and then hold.

159. For every corner did u use same SPEF?

No, we use different SPEF for every corner, for every corner the delays will vary so we have different SPEF's.

160. Difference between hierarchical and flat level?

- **Hierarchical:**
  In hierarchical each n every block is closed and without integrating to the top, top level timing is closed.
- **Flat level:**
  In flat each block is closed and then integrated to top and then the top level timing is closed.

161. Tell me blocks names?

There are 8 blocks

- ADR80
- ADR40
- CSS
- RFA Control
- MAC-1
- MAC-2
- Debug
- Always On

162. Which team you worked?

WLAN Team

163. Frequency of func mode and test mode?

- Func Mode:
  1000MHZ

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- Test Mode:
  100MHZ

164. All blocks met timing will you give signoff?

No, if the top level timing is met then only we will give signoff.

165. How you generated ECO's?

Using the Tweaker tool and manually.

166. What can you do if the linking issues have no problem in a path?

If the linking issues have no problem in path, then we should inform to the lib team.

167. What information contain in generated clocks?

Generated clocks contains

- Clock name
- Divide by logic
- Master clock
- Clock Port
- Edges information
- Edge shift information

168. What are the violations you check in your design?

The violations we check in the design are:

- Design Rule Violations
- Setup
- Hold
- Minimum Pulse Width
- Recovery
- Removal
- Clock Gating Setup and
- Clock Gating Hold

169. If 10k hold violations what is your approach to fix those violations, those are real violations?

First we should see the WNS, and if it is of same clock or different clock, if it is of different clock we can fix those violations using pushing and pulling. If it is of same clock then we should see it is single start point or multiple start points, if it is single start point then we can forward trace till the divergent point and fix the violations by observing the setup margin, if it is multiple start points then we should analyse the paths individually and fix the

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violations by observing the setup margin, if there is no setup margin then we should get the setup margin and then fix the hold violation.

170. Pushing and pulling down by Tweaker ECO's?

Yes we can provide clock ECO's with Tweaker i.e; pulling and pushing, but I gave clock ECO's manually, didn't used Tweaker for that.

171. What is Minimum Pulse Width?

Minimum Pulse Width is defined as the amount of on period in total time period, if it is not maintained we get violations.

172. What are the fixes of Minimum Pulse Width?

Fixes of Minimum Pulse Width:

- If there are any normal buffers and normal inverters in the clock path we need to replace those with clock buffers and clock inverters.
- If more number of clock buffers is there we can replace with clock inverters.
- We can replace the cells with less variation cells i.e; equal rise and fall.
- We can swap the flip flops from HVT to LVT.

173. What did u mean by less variation of cells?

The cells with equal rise and fall are called as less variation cells.

174. What are the Setup fixes after Base Tapeout?

Fixes of Setup after Base Tapeout are:

- Metal width is increased.
- Metal jogging from lower metals to higher metals.
- Use of spare cells when net is dominating.
- We can use metal buffers when net is dominant.
- Frequency can be reduced.

175. What are the Hold fixes after Base Tapeout:

Fixes of Hold after Base Tapeout are:

- Metal width decreases.
- Net deteriorate.
- Using spare cells.
- Inserting metal buffers.
- Voltage can be reduced.

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176. What are the Max Transition fixes afte Base Tapeout?

Fixes of Max Tran after Base Tapeout are:

- Metal width increases
- Metal jogging from lower to higher metals.

177. In which way it is useful to Tran if we increase metal width?

If width increases the resistance reduces, due to that delay reduces, as the delay and resistance are directly proportional to each other, due to this the Tran will be improved.

178. Max tran violations are there and if signoff is given is there any problem?

The expected results will not obtain and it will mask some Hold violations i.e; max tran is violated when the delay is more due to that some hold violations may fix, they may pop up after the fabrication, then the functionality will be effected due to that.

179. What are Exceptions?

Timing exceptions are:

- False path
- Multicycle path
- Max Delay/Min Delay

180. What is False path, Multicycle path?

- **False Path:**
  The path which does not exist functionally is called False path.
  All Asynchronous Clocks, Static Paths, and Non-functional paths are false paths.
- **MultiCycle Path:**
  The path which takes more than one clock cycle to capture the data is called MultiCycle Path.

181. If crosstalk in false path what u do?

Then we should fixe those paths, because due to that other paths may violate.

182. How did u gave to PNR team (cross questions)?

Collected all the violated nets and given to the PD team to fix it by using appropriate fixes.

183. What is Noise Analysis?

When one net is switching and other is in static condition then we get Noise violation, due to noise the functionality will be affected. Analysing these paths to fix those noise violations is called Noise Analysis.

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184. If we have functionality effect what is the problem?

If there is functionality effect, the design functionality will not obtain.

185. Derates in OCV and AOCV?

- **OCV:**
  In OCV flat derates are applied.
- **AOCV:**
  In AOCV the derates are applied based on the cell depth and physical distance.

186. How will u apply derates for setup and hold in 10nm and 14nm?

In 14nm derates are applied from AOCV, in 10nm derates are applied from POCV.

187. What is Cross Sectional Area?

Cross-sectional area is the minimum area occupied by metal.

188. How the Resistance and Delays changes?

The Resistance and delay are directly proportional to each other, so as the resistance increases delay increases, and if resistance decreases the delay decreases.

189. What you mean by Crosstalk it comes from?

Crosstalk:

Crosstalk is the undesirable voltage transitions between two or more adjacent nets through a coupling capacitor.

It comes through coupling capacitor.

190. How the Crosstalk effect the delays?

- **When Both the nets are Switching in same direction:**

In the data path if the nets are switching in same direction, due to this the logic is pulled and the delay will be reduced, due to this we get hold violations.

In the clock path if the nets are switching in the same direction due to this the logic is pulled and the delay will be reduced, due to this we get setup violations.

- **When Both the nets are Switching in different direction:**

In the data path if the nets are switching in different direction, due to this the logic is pushed and the delay is increased, due to this we get setup violations.

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In the clock path if the nets are switching in the different direction due to this the logic is pushed and the delay will be increased, due to this we get hold violations.

191. Aggressor and victim both are in same direction it helpful to Setup?

No, it is not helpful to setup.

192. How it is helpful setup what happen in Setup slack?

No, it is not helpful to setup, the setup slack may degrade but it will not improve.

193. Aggressor and victim both are in opposite directions it will helpful to hold?

No, it is not helpful to hold.

194. How it helpful what happen in hold slack?

No, it is not helpful to hold, the hold slack may degrade but it will not improve.

195. In all cases Crosstalk helpful to setup and hold?

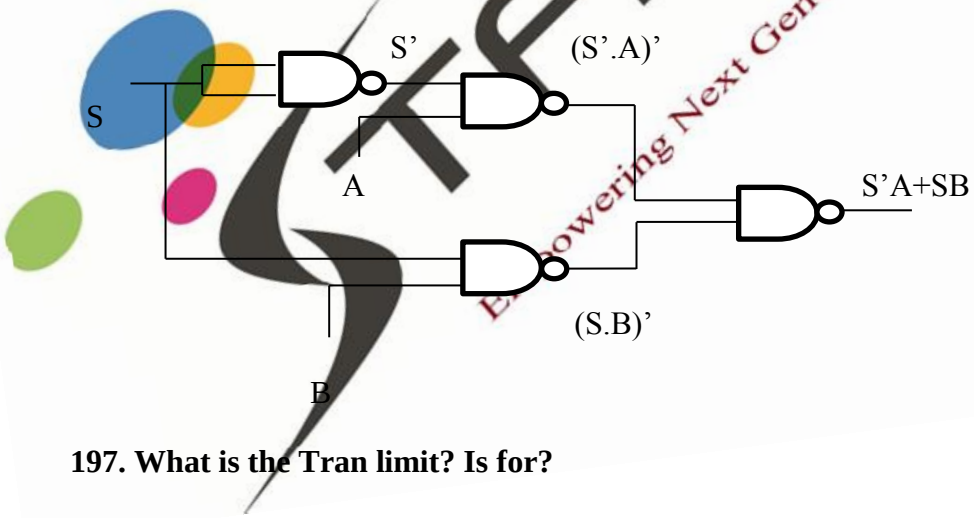
No, in any case Crosstalk is not helpful to setup and hold.

196. Draw Mux functionality by using NAND gates?

Mux:

$$Y = S'A + SB$$

Mux using NAND Gates:



197. What is the Tran limit? Is for?

250ps. It is for setup.

198. What is Tran limit for hold, from where you get Tran value?

100ps, from lib and SDC.

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199. Why different Tran limit?

Because the delays of setup and hold are different, so different Tran limits.

200. What analysis you did before going to eco?

I analysed the timing reports based on WNS, TNS and number of failing endpoints, if number of failing endpoints is more I did clock skewing, if there are less failing endpoints, I analysed the data path for which cells are contributing more violations is it due to tran, cap, fanout, or crosstalk delta based on that I fixed those violations with appropriate fixes.

201. What is Power Recovery?

Power Recovery is a technique to reduce the power dissipation.

202. Types of Powers?

There are two types of Power

- Static Power and
- Dynamic Power

➢ **Static Power**:

Static power is nothing but leakage power. Leakage power is due to sub threshold currents, and when the circuit is in static condition due to rise in temperature the charge carriers get doubled then the PMOS and NMOS will on partially then there will be a leakage from VDD to VSS.

➢ **Dynamic Power:**

Dynamic Power is of two types

- Switching Power and
- Internal Power

✓ **Switching Power:**

Switching power is the power dissipated due to the charging and discharging of load.

✓ **Internal Power:**

Internal Power is again divided into two types

- Short Circuit Power and
- Internal Power

▪ **Short Circuit Power:**

During the transitions from 1 to 0 and 0 to 1, when the tran reaches to its 50% value then both PMOS and NMOS will on due to that we get Short Circuit Power.

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- **Internal Power:**

It is the power dissipated due to switching of internal capacitance of a cell.

203. Types of VT Cells?

There are four types of VT flavours

- HVT Cells
- RVT Cells
- LVT Cells
- Ultra LVT cells

204. VT Cells Percentage?

Initial Stage:

HVT Cells – 97%

RVT Cells – 3%

Signoff Stage:

RVT Cells – 98%

LVT Cells – 2%

205. Hold is violated there is no setup margin what is your approach to fix those violations?

By reducing the common path, and replacing less variation cells, by using this we get setup margin and then we can fix hold violations.

206. How the CRPR helpful to fix those violations?

CRPR value is added to the required time in setup due to that the setup slack improves and we get certain margin.

207. Tell me CRPR with Crosstalk and without Crosstalk to fix the violations, CRPR value zero in any case?

Without crosstalk CRPR is removed for both setup and hold, with crosstalk CRPR is removed for hold, it is not removed for setup.

When there is no common path the CRPR value can be zero.

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208. Tell me Crosstalk effect at same edges and different edges?

Crosstalk is affected in different edges.

209. In a Half cycle path hold is effect by Crosstalk, How?

In half cycle path hold is also effected by crosstalk.

210. From scripting you can trace the margin or not?

Yes, from scripting we can trace the margin.

211. How many corners in 10nm & 14nm?

In both there are 24 corners.

212. What are Cworst and Cbest?

- **CWorst:**
  In CWorst the capacitance is dominant i.e; maximum capacitance, and Interconnect Resistance is smaller, it is also known as Cmax Corner.
- **CBest:**
  In CBest the capacitance is minimum, and interconnect resistance is larger , it is also called as Cmin Corner.

213. Pay roll company?

Mirafra

214. 100ps hold violations are there what is your approach?

First we should check the number of failing endpoints, if there are less failing endpoints then we should see the setup margin and can go with insert buffer option.

Else if there are more failing endpoints then we can go with clock skewing.

215. If u have 10000 violations what is your approach?

First we should check is this is a real issue or constraint issue, if it is a constraint issue we should analyse and inform to the constraint team.

If it is a real issue then we should check whether the violation is due to over buffering or under buffering.

Then, we should check the startpoint and endpoint for the clock if it is different clock then check the number of failing endpoints, if the number of failing endpoints is more then we address the violation by using pushing and pulling. If it is a single startpoint and multiple endpoints then we should forward trace and address the violation till the divergent point.

If it is multiple startpoint and single endpoint then we should back trace and address the violation till the divergent point.

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If it is multiple startpoint and multiple endpoints we should analyse the paths individually. We should check the datapath, and analyse which cell is contributing more violation is it is due to tran, cap, fanout, crosstalk delta or due to net dominant.

For setup If any net dominant is there we can insert buffer when the cell delay is less than the net delay, then we should check is there are any low drive strength cells in the path, if there any low drive strength cells then we should check hold margin and can upsize the cell, if there are any HVT cells we can swap from HVT to LVT.

For hold, if there are less number of failing endpoints then we can check the setup margin and go with endpoint buffering. If there are more failing endpoints we should analyse the paths and fix the violations using downsizing or VT swapping from LVT to HVT by checking the setup margin.

216. How much time u took to analyse the issues?

Based upon the scenario and issue the time depends, if there is sufficient margins analysis will not take that much time but if there is no margin we should analyse the paths in detail and then fix so it takes some time to fix.

217. What is the preference for Tran, Cap, Fanout?

First preference is given to Tran and then Cap at last fanout.

218. What are all the Tcl scripts you have done?

I written some procedures to get the ports based on the direction, to get all the clock gating cells, to get particular clock attributes, if there is cell names collecting the instance names, if instance names are there collecting the cell names, if net is given collecting the pins connected to that net, if a pin is there collecting the nets connected to that pin.

219. Are you doing insert buffer?

Yes, I have done endpoint buffering to fix the hold by checking the setup margin.

220. Are you applied any constraints?

I applied for analysis purpose only, but I didn't modify the SDC.

221. Tell me Uncertainty value in your design for Setup and Hold?

- **Setup:** 120
  Skew – 80
  Jitter – 20
  Margin – 20
- **Hold:** 100
  Skew – 80
  Margin – 20

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There is no jitter for hold because the hold is independent of frequency.

222. What is Inter Clock Uncertainty?

Uncertainty between two different clock domains is called Inter Clock Uncertainty.