



Lecture 17

Parasitic Extraction and Packaging

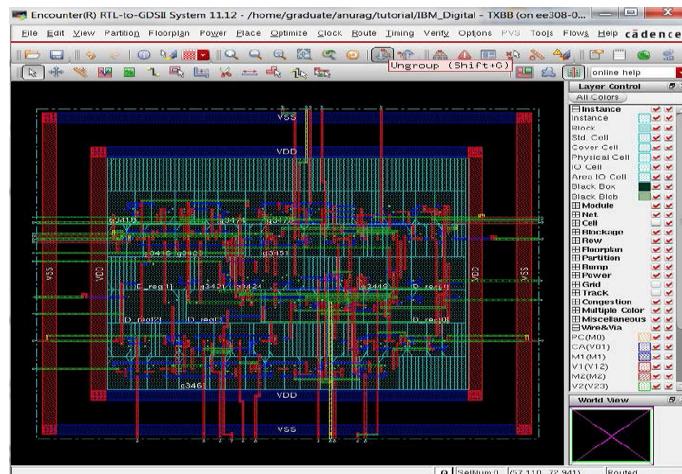
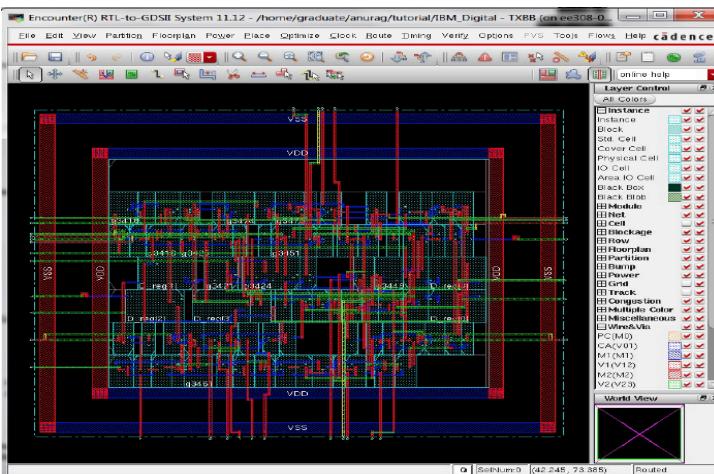
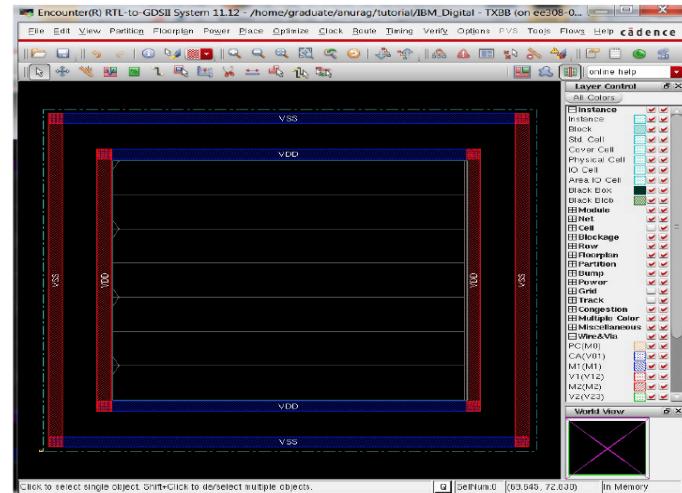
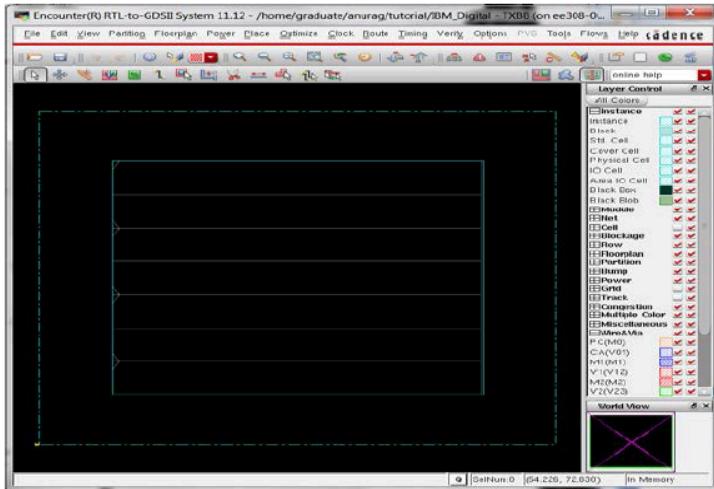
Xuan ‘Silvia’ Zhang
Washington University in St. Louis

<http://classes.engineering.wustl.edu/ese461/>

Cadence Encounter Tutorial



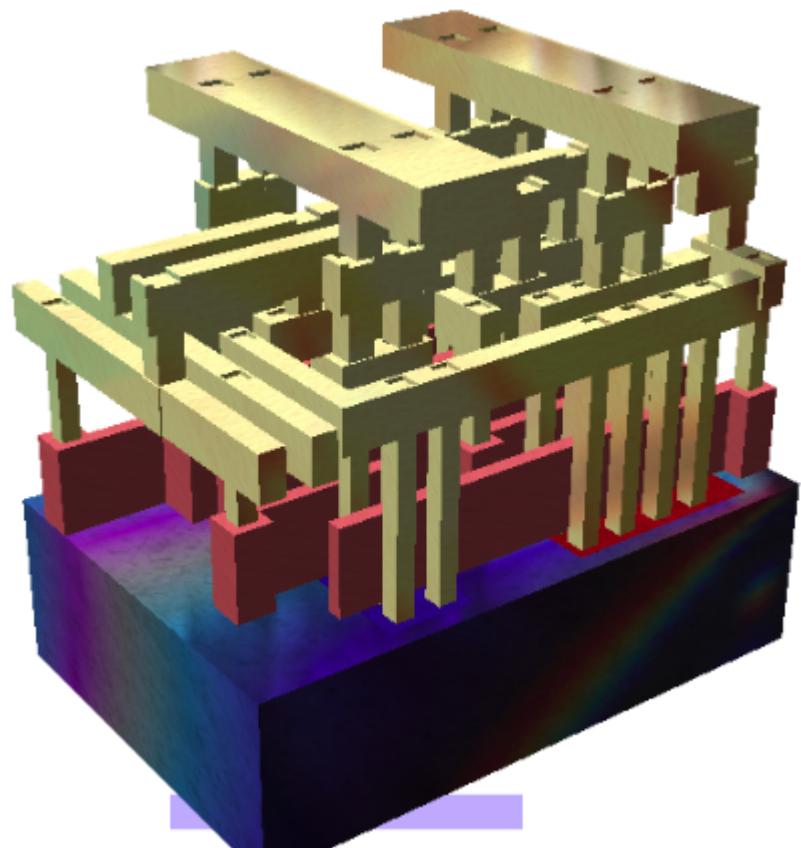
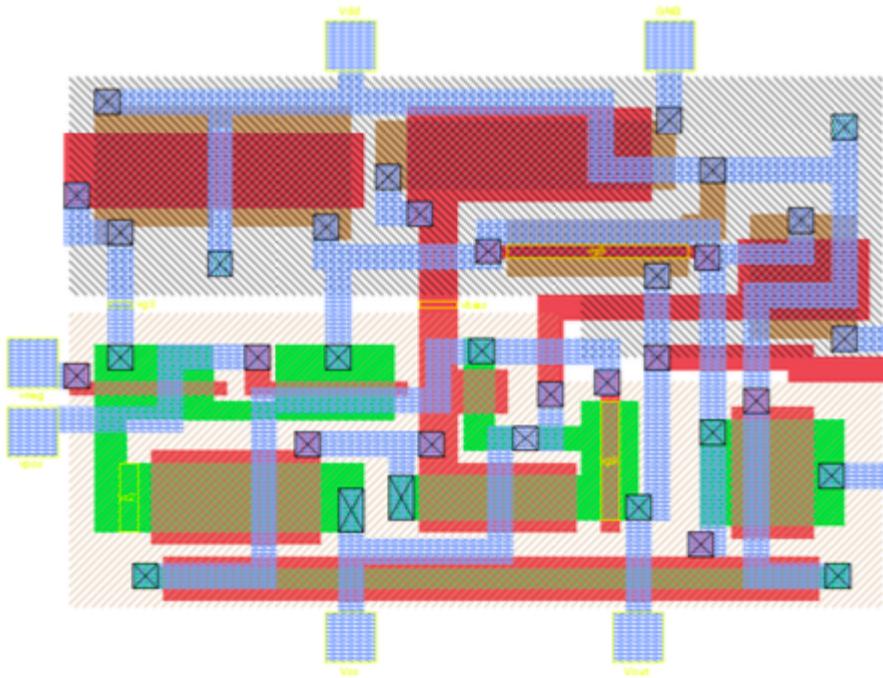
- .syn.v, LEF, clock.ctstch, clock.tcl



Post-Place-and-Route Design

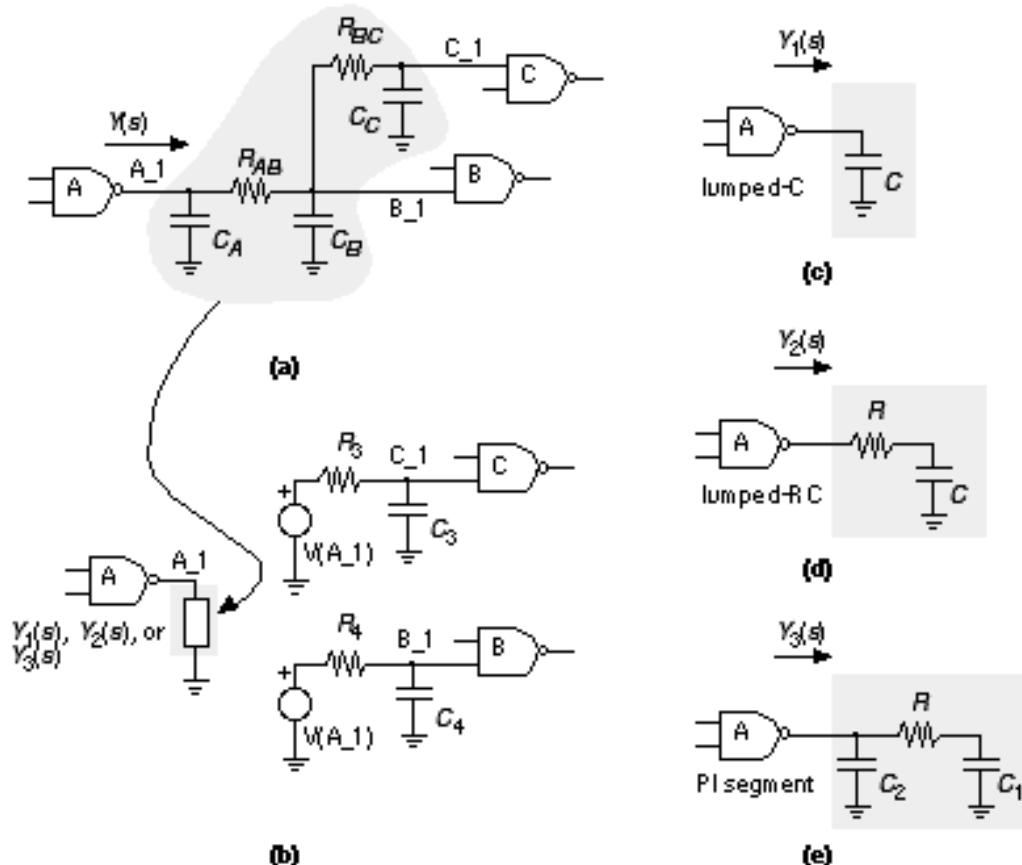


- GDS
 - Graphic Database System



Parasitic Extraction

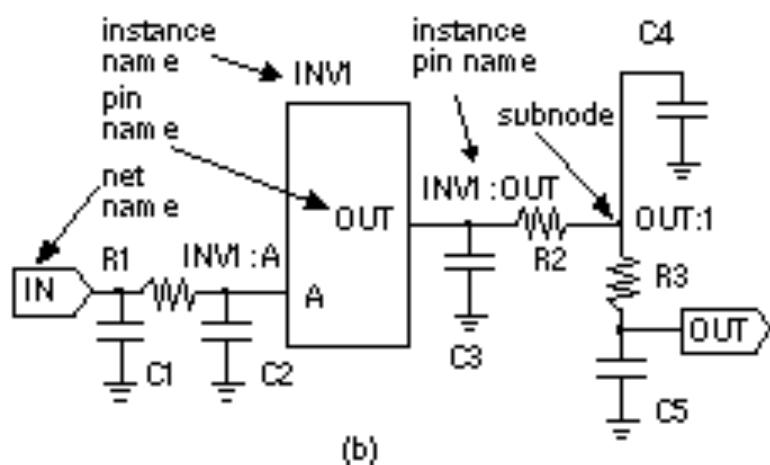
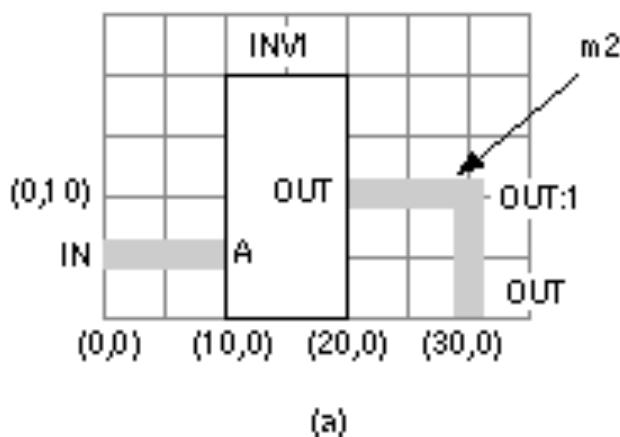
- Parasitic capacitance and resistance
 - exact length and position of interconnect is known



Standard Parasitic Format (SPF)

- SPF

- standard (SPF), reduced (RSPF), detailed (DSPF)
- loading effect represented by RC network
- 3 models: lumped-C, lumped-RC, Pi-segment

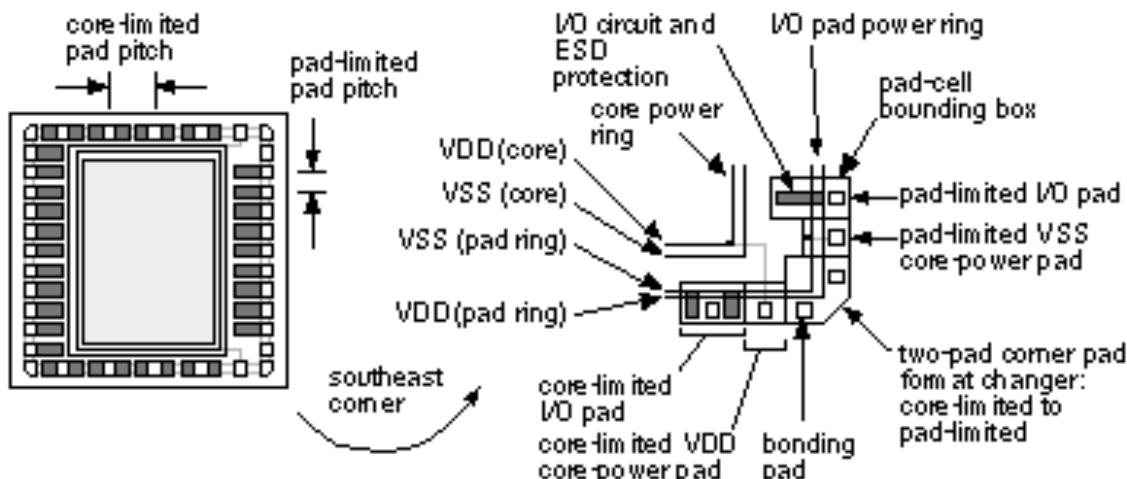


Last-Stage Rule Check



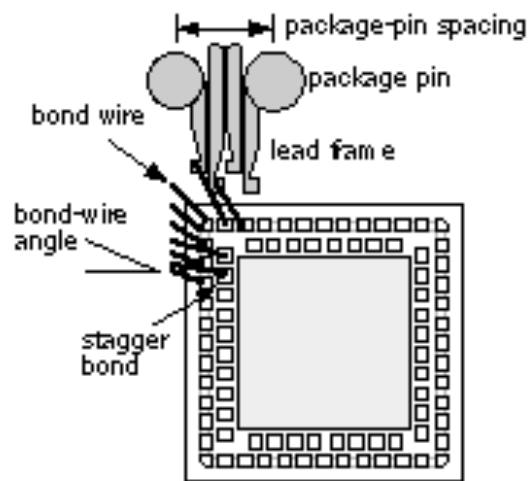
- Design-rule check (DRC)
 - at detailed routing level, using phantom cell view
 - at transistor level, using real library-cell layout
- Layout versus Schematic (LVS)
 - electrical schematic extracted from physical layout
 - compare with the netlist
 - challenge: transistor-level netlist is huge!
- Tools
 - Cadence Dracula/Assura, MentorGraphic Calibre

Bonding Pads

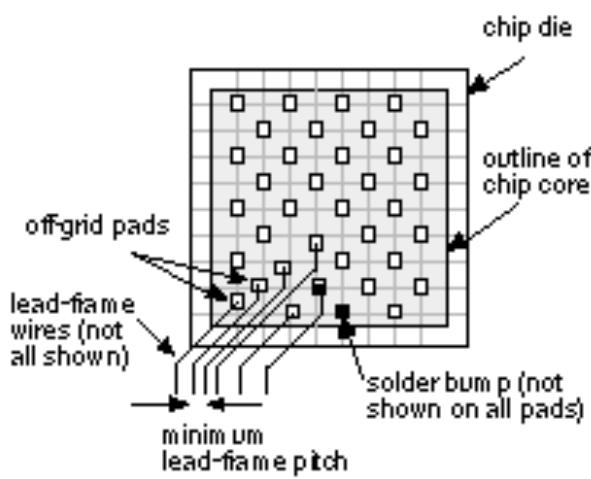


(a)

(b)



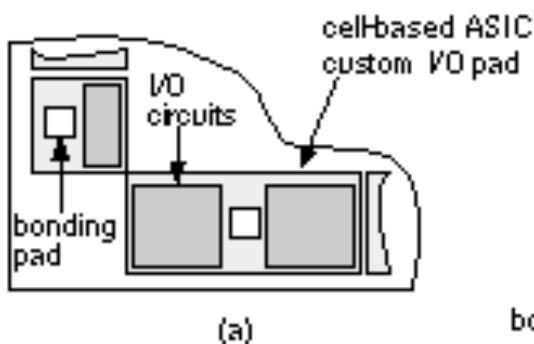
(c)



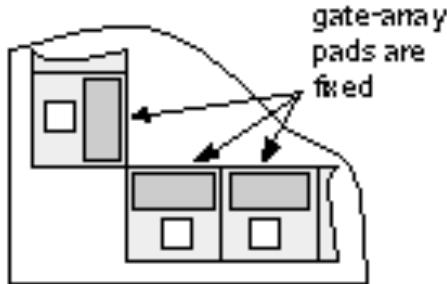
(d)

I/O Pad Cells

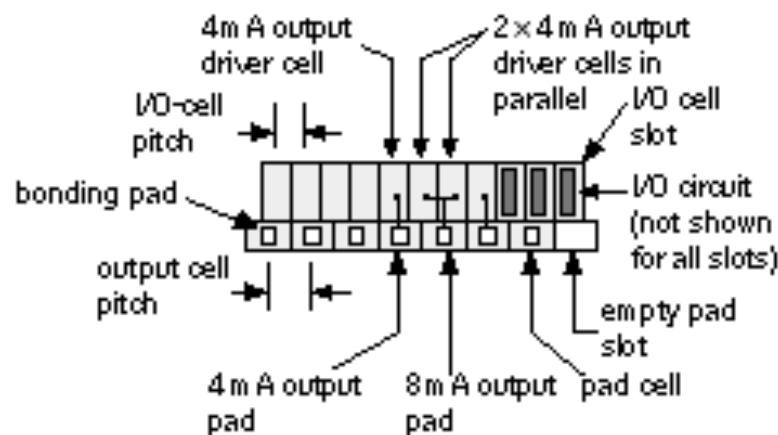
- I/O buffers
- ESD protection
 - electrostatic discharge (ESD)



(a)



(b)

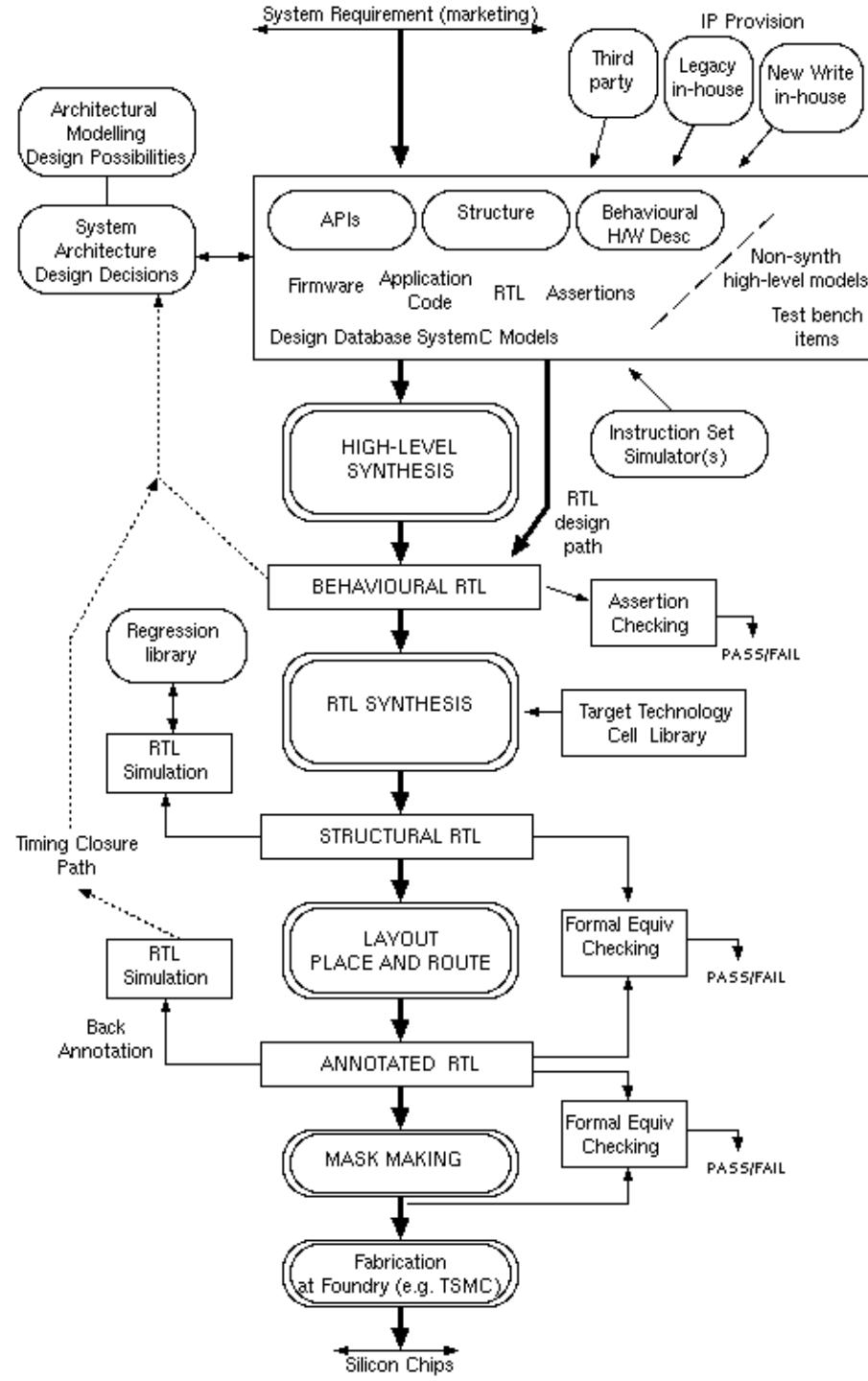


(c)

Mask Preparation



- Final additions before tapeout
 - ASIC artwork: logos, secret messages, etc
 - kerf: alignment markers, mask identification, artifacts
 - scribe lines: die to be separated by diamond saw
 - hermetic edge-seal
- Final export
 - GDSII stream file (binary format)
- Foundry check
 - active layers: n/p diffusion, thin-oxide, implant layer
 - e-beam: generate metal on glass masks
 - optical system: scale to deep-submicron process
 - optical proximity correction (OPC)

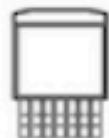


Packaging



- Wafer thinning, dicing/saw
- Die attach, chip bonding
- Wire bonding
- Transfer molding, trim, marking

ASIC Packages



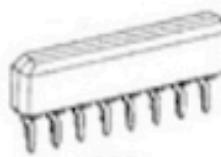
DDPAK



DPAK



DIP



SQP



SW



T7-TO220



FDIP



PDIP



PENTAWATT



TO220



TO2205



TO220ISO



PLCC



QDIP



QFP



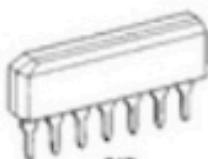
TO252



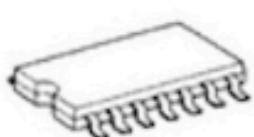
TO263



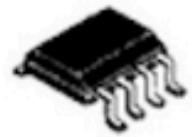
TO268



SIP



SO



SOS



TO3



TO52



TO99



SOT223



SOT23



SQL



TSOP



ZIP

ASIC Packages



- SIP: single in-line package
- DIP: dual in-line package
- QFP: quad flat pack
- LLC: leaded chip carrier
- LLCC: leadless chip carrier
- SOP: small-outline package
- TSOP: thin small-outline package
- PGA: pin grid array
- BGA: ball grid array
- Material: metal, ceramic, plastic

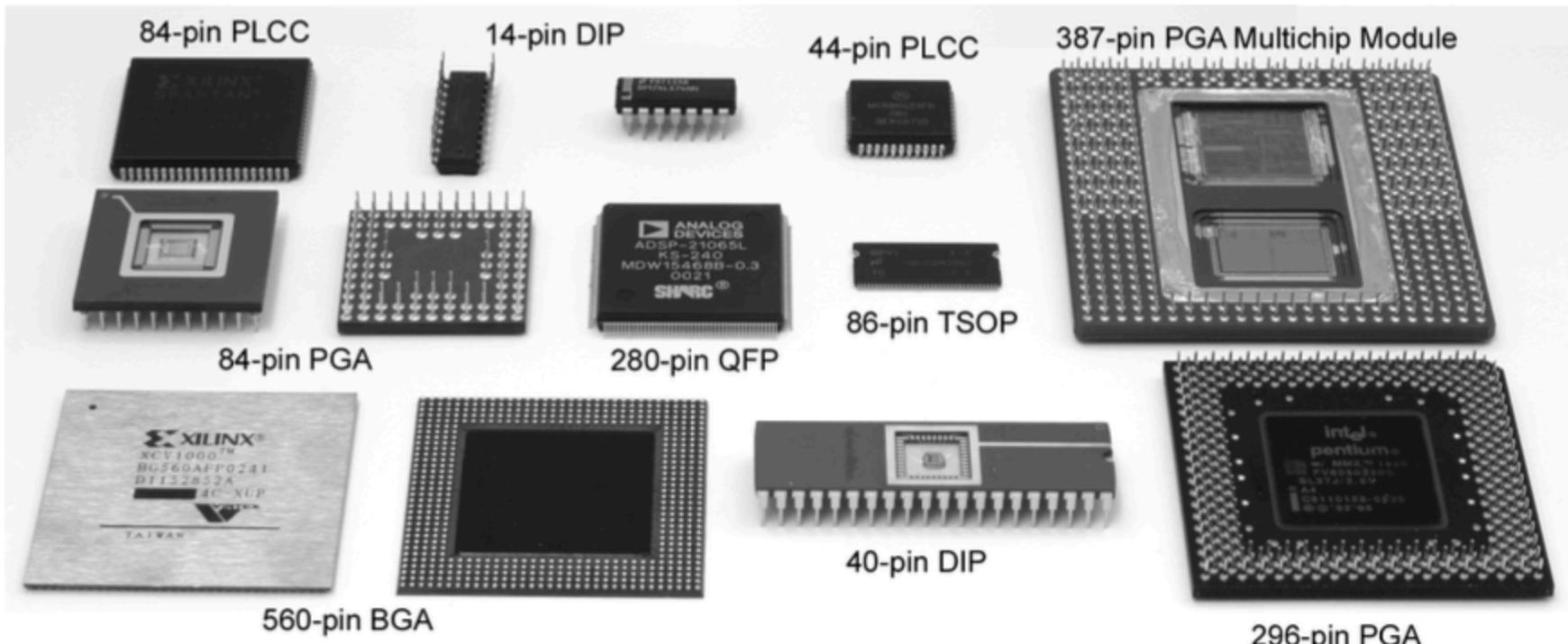
Package Functions



- Electrical connections: signals, power, ground
- Little delay or distortion
- Mechanical connection
- Heat removal
- Protection against mechanical damages
- Compatible thermal expansion
- Inexpensive to manufacture and test

Through-Hole vs Surface Mount

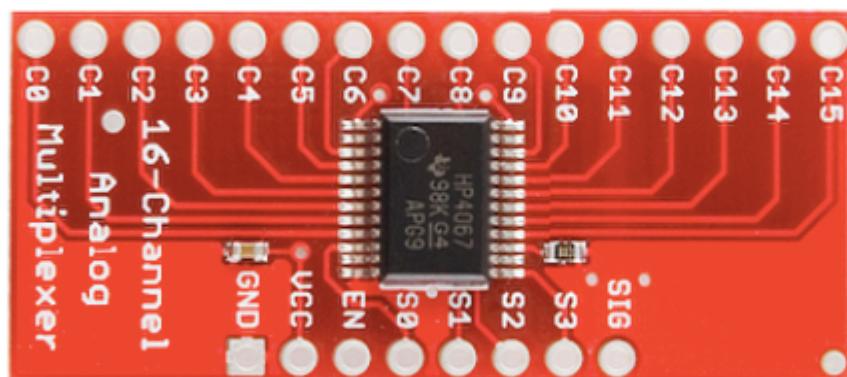
W
SL



Surface Mount (SMT/SMD)



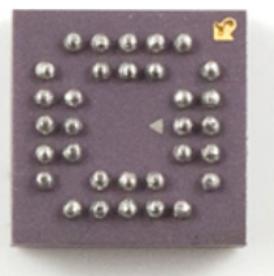
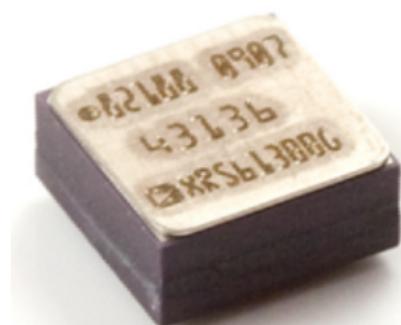
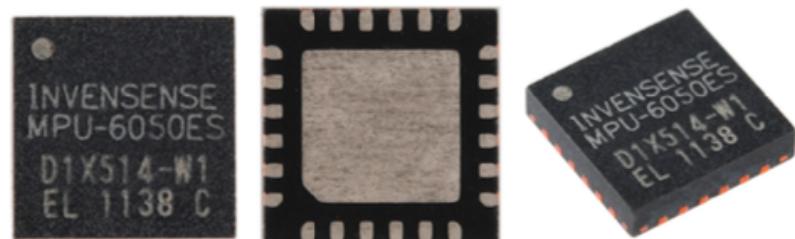
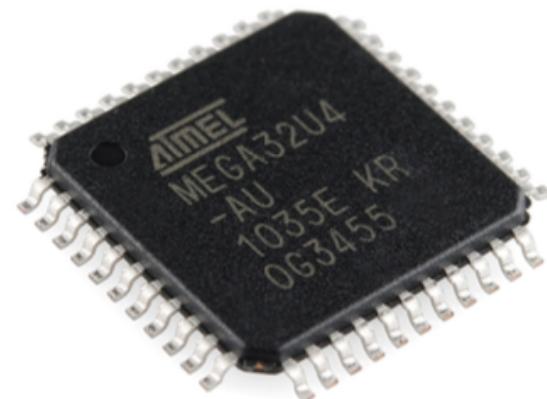
- SOP/SOIC
 - pin pitch 0.05" (1.27mm)
- S(Shrink)SOP, T(Thin)SOP
 - pin pitch 0.635mm



High-Pin-Count Package

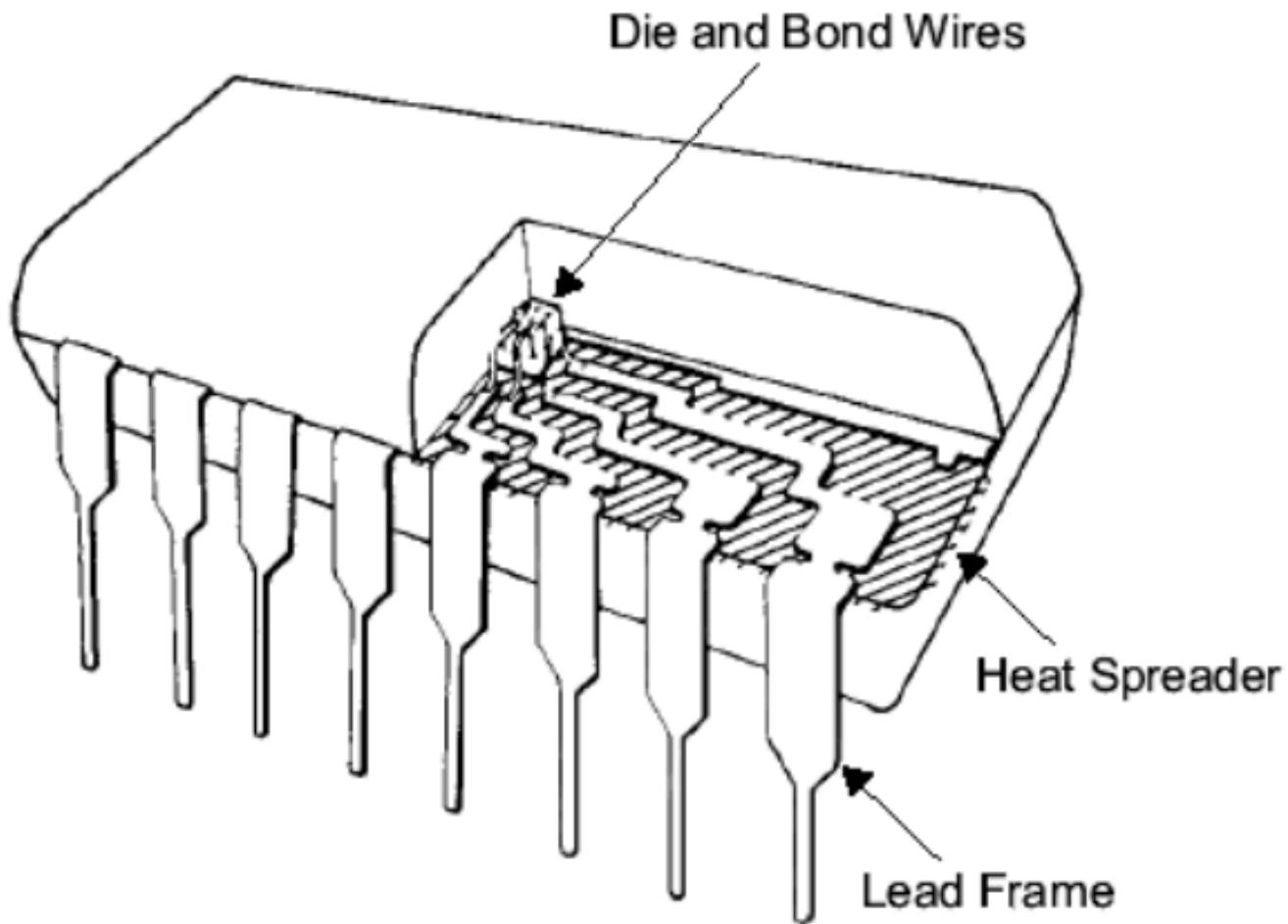


- Quad Flat Package (QFP)
 - pin pitch 0.4mm to 1mm
 - T(Thin)QFP
 - V(Very)QFP
 - L(Low-profile)QFP
- Quad Flat No Leads (QFN)
 - TQFN
 - VQFN
- Ball Grid Arrays (BGA)
 - microprocessors: ~100 pins



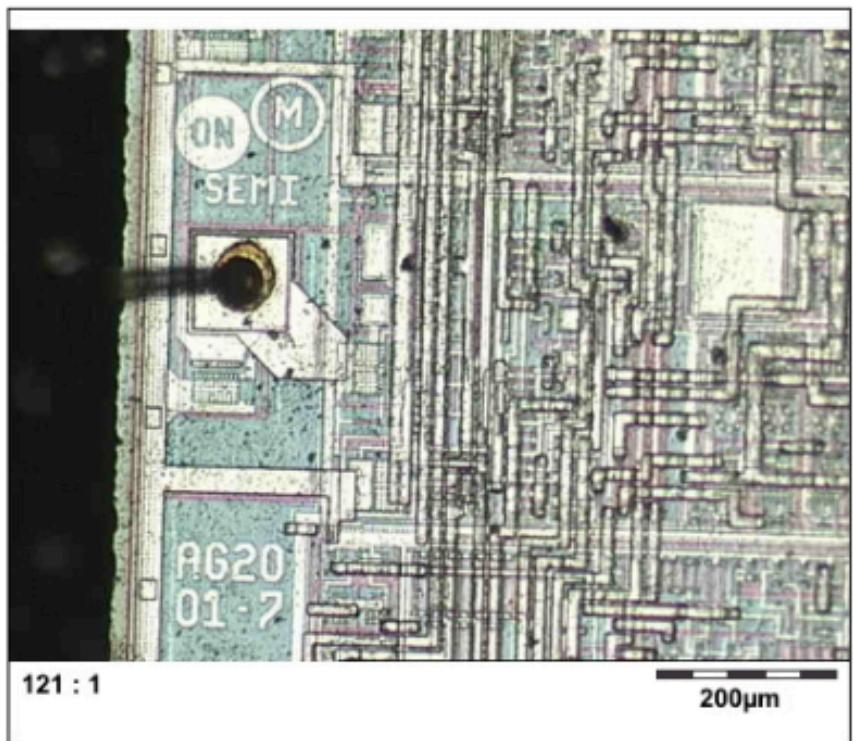
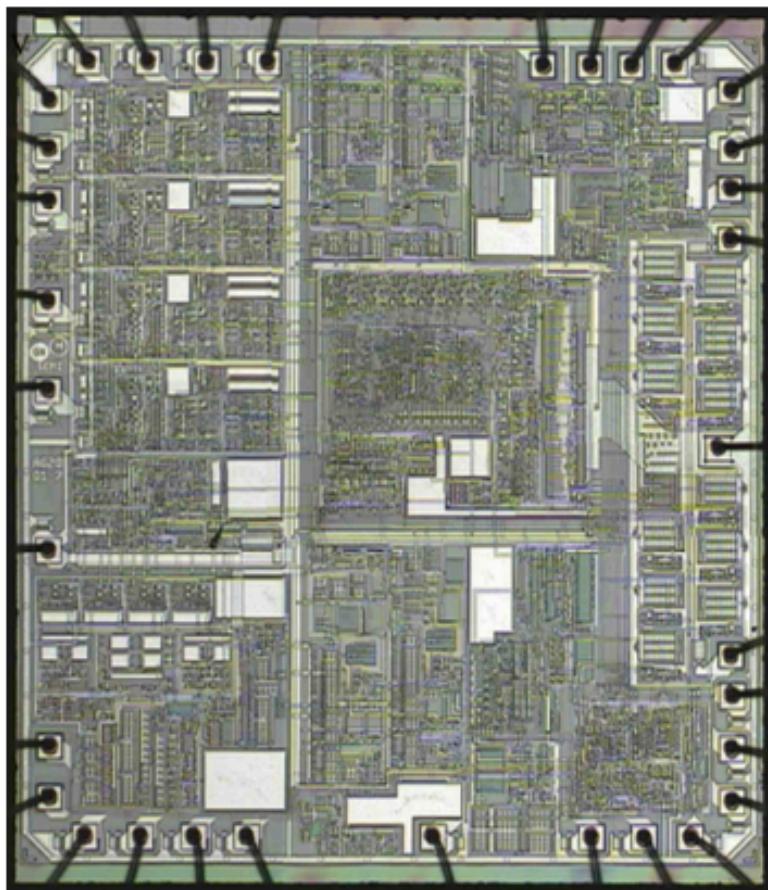
Wire Bonding

W
SL



Wire Bonding

W
SL



Wire Bonding

- Ball bonding and wedge bonding
- Material: gold, copper, aluminum



Flip Chip

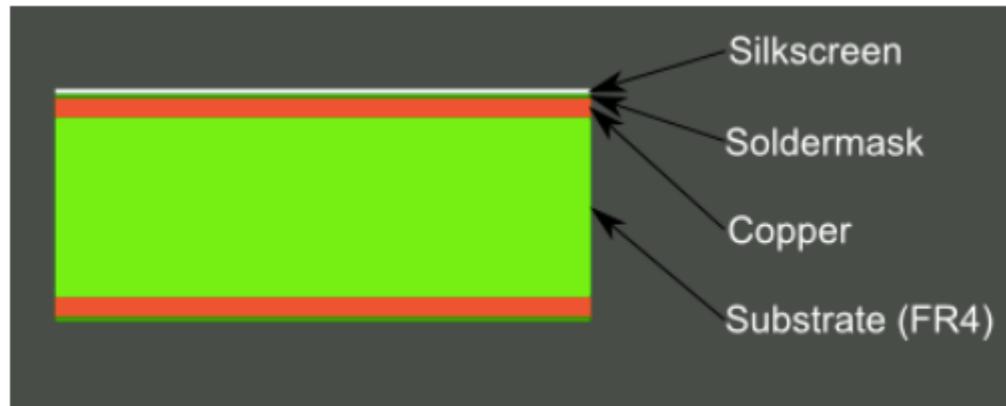


- Pads placed across surface of the die
 - instead of around periphery
 - top level metal covered with solder balls
 - chip flips upside down, aligned to package
 - heated to melt solder balls for bonding
 - aka. C4 (controlled collapse chip connection)

Printed Circuit Board (PCB)



- PCB layers
 - soldermask
 - pad
 - via
 - silkscreen
 - trace
 - v-score
 - footprint



- Reference
 - <https://learn.sparkfun.com/tutorials/pcb-basics>

Questions?

Comments?

Discussion?