Hello
I am Adnan Aslam. I got an AIR 279 in GATE ECE 2021 and took admission in MTech specializing in Telecommunication Technology and Management at IIT Delhi. Being from a non-VLSI specialized branch, and being interested in a VLSI domain job, I can understand the struggles students go through. Fortunately, I got placed in one of the biggest semiconductor companies (Intel and Qualcomm). So, through this document, I would like to share my placement experience and what all I prepared for it. It doesn't matter which college or specialization you're from, I believe that this would be helpful.

CHOOSING PROFILE:

Being from a non-VLSI specialization, you must prepare a little extra so that you can stand out. Firstly, you must decide which domain is more suitable for you (Digital, Analog, or Embedded/Firmware side). As I had digital domain in mind even before the start of my MTech, I stood by it throughout. Improve your networking by connecting with people who are in the domain in which you're interested. Gather and collect all info/material/experiences that you can, by interacting with your seniors and people from the industry. It helps a lot! Trust me, I did the same. I found some amazing seniors and the entire community is very helpful. There is a lot of material available on LinkedIn. What's important is to explore the content according to your need and start saving it for future use.

WHAT ALL I PREPARED:

There is no perfect time to start your preparation. But starting sooner will give you a lot of time to go through multiple concepts. I started my preparation in Dec 2021 after my first sem got over. I started with Verilog and Physical Design course in Dec. Because maintaining a good CGPA is a tough task and takes a lot of your time, I started a bit early. As everyone knows their own capability, I started in Dec because I knew after the second sem I'll have to revisit these concepts. So why not utilize the winter vacation with a head start. The Full proper preparation started in May 2022, after the Second sem finished. Following are the topics that I studied (and their sources):

1) Verilog HDL Programming:
    i. Went through a course by Prof Indranil Sengupta (IIT KGP)
    https://www.youtube.com/playlist?list=PLUtfVcb-iqn-EkuBs3arreilxa2UKIChl
    ii. Practiced a lot of questions on HDLbits. (**Extremely Helpful**)
    https://hdlbits.01xz.net/wiki/Problem_sets#Getting_Started
    iii. Also, go through the Verilog book by Samir Palnitkar. Very Helpful
    many questions for the company tests can be practiced from here.
    Extremely Important for tests and interviews

2) Digital IC design:
    i. Study this course by Prof Janakiraman (IITM) extensively
    https://www.youtube.com/playlist?list=PLHO2NKv71TvsSqYwVvUCZwNkY-jUyUHdS
    Go through the lectures again and again if you're stuck somewhere!
    Especially types of power dissipation and CMOS Inverter related topics (asked in Interviews and tests as well)
    make short notes and keep revising. ***Highly Recommended for Interviews***
    ii. Refer Digital IC design book by Jan M. Rabaey (ch 5-10)
    or CMOS Digital Integrated Circuits by Sung-Mo Kang

3) FIFO:
    i. What is FIFO? Why is it used and FIFO Depth calculation.
    EXTREMELY IMPORTANT for company Tests and Interviews.
    https://hardwaregeeksblog.files.wordpress.com/2016/12/fifodepthcalculationmadeeasy2.pdf

4) Synchronizers and Clock Domain Crossing:
    i. Get a rough idea and basic understanding of them.
    Very Important for Interviews
    https://www.youtube.com/playlist?list=PLdcY8Cf-O1Zon-8c9NDhgY2F8r_O7oeC4
        ii. Other Helpful Links:
        https://youtu.be/Fy9wOF2M-oE , https://youtu.be/TRH89_Hw988

5) Physical Design Flow:
    i. You can find an ample number of useful links on Google or playlists on YouTube. But I did a course on Udemy by Kunal Ghosh which I found particularly helpful. Link: https://www.udemy.com/share/101tpW/
    ii. Get a thorough understanding of the entire flow at a physical level.
    iii. There are concepts like noise margin, **metastability**, voltage droop, and ground bounce which you should know an idea of. ***VERY HELPFUL in Interviews***

6) ASIC Design Flow:
    i. Almost all interviews start with explaining this only. The same happened to me. There are many resources that you can find on Google or YouTube or LinkedIn. Learn from wherever you feel the most comfortable. One useful link I found is: https://www.einfochips.com/blog/asic-design-flow-in-vlsi-engineering-services-a-quick-guide/
    ii. Feel free to use any other resource as well. I went through multiple resources, but the crux of the concept remains the same. ***EXTREMELY IMP FOR INTERVIEWS.*** From design specs to tape out, everything should be covered.

7) Static Timing Analysis:
    i. One of the ***MOST IMPORTANT TOPICS for TEST AND INTERVIEW***
    ii. What is **setup time, hold time, clock skew**, and jitters? Their origin and numerical questions based on setup and hold time where max frequency is asked. Practice these types of questions from Digi_QS.pdf
    iii. Link: https://www.vlsi-expert.com/2011/03/static-timing-analysis-sta-basic-timing.html

8) Digi_QS.pdf question bank:
    i. ***EXTREMELY EXTREMELY IMPORTANT FOR TESTS AND INTERVIEWS***
    ii. Practice this at least three times. Many times, it happens that direct questions are asked from this file, be it in tests or interviews.

iii. Do all the chapters! Cannot emphasize it more. This pdf is available online. https://studylib.net/doc/25245792/digi-qs-full

9) Computer Architecture:
   i. RISC vs CISC. An idea of the overall architecture for a type of processor. Interrupts
   ii. Concepts of pipelining and Related numerical on efficiency, exec time calculation, etc.
   iii. Types of Memories and cache memory. Related numerical on tag size, memory size, etc. ***VERY IMPT FOR INTERVIEWS and sometimes in TESTS***.

10) Basics of Design for Testability (DFT)
   i. A rough idea of Controllability and observability, different types of SCAN techniques, ***types of faults, hazards, and glitches***.
   IMPORTANT FOR TESTS BUT SOMETIMES ASKED IN INTERVIEWS
   ii. Link: https://www.youtube.com/playlist?list=PLyWAP9QBe16qiSMkBcAnUMxFagLIJzmv1

11) Programming Languages:
   i. Apart from C/C++, a scripting language is an added benefit. Like the basics of Python, TCL would certainly help your resume.
   ii. For **TESTS:** practice output based, identify errors-based questions. Know sorting algo time complexity. Usually 95% of the time, questions are objective based i.e., MCQs. But some companies ask you to write the code snippet or some function as well. So, it's better to know how to code as well.
   iii. Sometimes, the interviewer might ask you to write a function using your choice of language so it's ***important for BOTH TEST AND INTERVIEWS.***
   https://www.geeksforgeeks.org/c-multiple-choice-questions/

12) Some Miscellaneous topics:
   i. For Interview:
      1. Have a write-up prepared for your projects and thesis so that you can speak about it thoroughly, explaining all the relevant details.
      2. FPGA design flow
      3. Short channel effect
      4. Basics of UVM (Universal Verification Methodology)
      5. Interrupts in processors. Diff types of addressing modes.
      6. Clock divider problems: https://www.youtube.com/playlist?list=PLPmSCnkkX4qtFcm8FZpwHEawvq5eULxwf
      7. and clock domain crossing basics: http://www.sunburst-design.com/papers/CummingsSNUG2008Boston_CDC.pdf

ii. For both tests and interviews:
    1. ***Prepare Digital electronics (all GATE topics) thoroughly!!***
    2. Go through Network theory and basics of Analog electronics (amplifiers, OpAmp base, MOSFET-based questions). RC circuits are asked directly in interviews. Draw the response without using pen and paper so conceptual understanding is required.
    3. Questions based on Implementing a circuit with only a single component. Like implementing an encoder/decoder using only 2x1 MUX. Draw all fundamental logic gates using only MUX.
    4. FSM-based questions. To program in Verilog, create state diagram. Anything can be asked. FSMs are quite a favorite topic in interviews. Do search on YouTube and practice from Digi_QS.pdf
    5. **PUZZLES**: I practiced from GeeksforGeeks. Link: https://www.geeksforgeeks.org/puzzles/

RESUME, CERTIFICATES, and CGPA:

My resume started with my educational background, followed by my MTech thesis. My thesis was based on High-Level Synthesis where I had to use Pipelining to improve throughput when it runs on an FPGA. This project was a mix of communication with HW implementation. After this section, I added a total of 7 projects. The first 2 were purely based on digital design. The next 3 were Verilog based. And the last 2 were communication oriented. Followed by this, there was a scholastic achievement section. After this, technical skills, industrial training, and extra-curricular activities were there.

I did not add any certificates. It totally depends on you whether you want to add or not. I believe if you add something and you're not able to defend it, it'll certainly leave a bad impression. And the certificate doesn't hold any value if you're not able to justify it. I did watch a few lecture series from NPTEL, and I was able to explain my learnings from it when it came to that. So, it's your wish ultimately. If you want to add then go ahead but if you don't, that's also completely fine. Just be confident about all the data you add to your resume.

Another important part of your Resume is your CGPA. Usually, companies set the eligibility criteria as 7 or 7.5. Very few companies keep it at 8. So **DON'T COMPROMISE** on your CGPA**.** If the eligibility is not met, you might not be able to apply for that company only. At the time of our placement, I had an 8.8 CGPA, which I'll consider decent. However, having a low CGPA doesn't mean that you don't get placed. My classmate had an overall CG of less than 8 but he got placed at TSMC. But don't take risks. Work hard for your grades. A CGPA of 8.5+ is more than safe. ***The more, the better.***

Placement Test:

The pattern for almost all companies was the same only. There are 3 sections. Aptitude, Programming, and Technical section. It's an objective type of paper. All sections are in MCQ format. Aptitude consists of the type we study for GATE. Programming section I've already explained above. There were a few companies like Mathworks and Tenstorrent, that took MCQ as well as subjective-based tests for programming. For example, one question was to write a function for a sorting algo of your choice in your choice of language. The technical section contains questions from

Digital electronics (ADC/DAC, K map, Comb + Seq crkts). Do EVERYTHINGGG from GATE syllabus!!
Analog electronics (opamp, diode applications, mosfet-based amplifiers)
Network Theory (RLC combination crkts, KCL, KVL-based questions, Capacitor-based numericals especially for analog domain). Basics of 8085 and microprocessors are also asked.
A few questions from **FIFO DEPTH** are always there. Sometimes Control system-based block diag reduction or plotting poles and zeros for filters are there. So that can be revised. **Setup and Hold time-based numerical questions**. Delay-based Verilog questions. Semantical errors and syntax-based ques. Also keep revising the stuff you're preparing for interviews, that will certainly help.

We applied for almost all HW companies that opened for us, like Intel, Qualcomm, Nvidia, Texas Instruments, AMD, Samsung Semiconductor, STmicro, Mathworks, Tenstorrent, TSMC, Leapfrog, Quasistatics, Rivos, MaxLinear, Silicon Labs, Infineon Tech. Some other names are also there which I'm not able to recall. But these many companies don't just open to you when they come for VLSI-related profiles. You must have a particularly strong placement coordinator to get these companies to open eligibility for your branch. This scenario varies from college to college. There were some companies like Analog Devices and MediaTek which didn't open for us. It is highly recommended to apply to all companies which are open for you.

Interview Experience:

QUALCOMM (Physical mode): This Interview call came out of the blue as Qualcomm HW profile was not scheduled for that day. The time slot for me was from 9-10 AM. The interview started with me introducing a little about myself. I went on to explain my thesis and all this took 12-15 minutes. After that, the interviewer (only a single person took my interview) went on to explain the type of role they have a vacancy for and how their tasks will be carried out. It was more of a back-end design-related profile, so he got a little skeptical about me because of my communication-related branch.

That's where I convinced him about my interest and passion for digital vlsi. I asked him to give me a chance by interviewing me and based on my responses, he can judge me better if at all I would be a right fit for this job or not. Moreover, I told him that the major project that I had chosen, was also connected to VLSI and the courses that I've studied on my own and the projects that I've added in this resume are also purely out of my own interest and passion which shows my commitment for this profile. He asked me about Physical design flow. I explained it to him and went on a little extra only. He then went on to ask me about my processor-related project. An overview only. Next, he wanted to know the functionality of a 2-bit comparator. How is the decision taken? He then asked me about FIFO. What is it? Why is it used? And explain with an example. I explained all that he had asked and even explained some RD/WR functions using Verilog as I had done a project on FIFO. In the end, he asked me if I had any questions for him. This was all for the first round. Based on his look, I'd say that he was satisfied with all the answers that I gave him.

We were then waiting in the common room where all the other students waited. Many people got called for their 2nd and even 3rd rounds followed by some rounds of HR interviews. So there I got a little panicked as I still had no news. After lunch, I got a call for an Interview. On my way in the lift only, I coincidentally met with my technical recruiter, who took my first interview. He then recognized me and conveyed to me that I was selected, and the one that I'm going for will be my HR interview. He congratulated me and wished me luck. After this, I got really confident, and the HR interview went very smoothly. It was as if two friends were talking. We spoke about the FIFA world cup and

who are my favorites (Argentina, of course!), and how Bangalore is a nice place to work in. The HR then congratulated me and then that was it. Selected!

Intel (Online mode): Although this interview was in online mode, we were required to be on campus. So, we went to vacant designated classrooms for this online meeting. Early morning, I got info that I was slotted for 10-11 AM (Coincidentally, I got called for Qualcomm interview the same day for 9-10 AM which was right before the Intel slot). As far as I remember, the meeting started at 10:20 AM and went on till 11:10 AM. Again, there was only one panelist. He started the interview by asking me to introduce myself briefly. After the introduction, I started explaining my thesis and whenever he had any doubts about it, he would stop me and ask the same. This went on for about 15-20 mins. He then explained the job role that he's recruiting for and why telecom/communication side students might find it a little hard to relate.

He was getting a little skeptical about me because of my branch/specialization. I convinced him to give me a chance just like I did in Qualcomm. He then asked me if I'd ever heard of ASIC design flow and if yes, to explain it. I started off with it and when it came to floor planning, I even included the physical-design flow-related info into it to cover everything about it. There, I mentioned the word "metastability". So, the interviewer took the discussion in that direction. After that, he asked me to draw two D flip flops, one connected to the other, and asked me some questions related to that diagram. He was proposing an issue in this setup, and I kept on discussing the solution. For instance, he asked if the first FF is turned off then what will be the output at the second FF?

Another modification was made to this question and based on your previous response, come up with a better solution. At some point, an inverter, A 2x1 MUX was also integrated into this setup. The major objective of these slight modifications in the question was to know the approach of your solution. He did not want a binary 1 or 0 answer. Rather, he wanted to know the thought process. And whenever I got stuck, he gave me hints to push me in the right direction. He also asked me to identify a type of power dissipation while he was explaining a problem. He also asked me about FIFO and its usage. Toward the end, he asked me if I had any questions for him, and after that, he suggested that I investigate analog concepts as well as that would help in my understanding of Digital circuits. This was my one and only round at Intel, unlike many other students who went for their 3rd or 4th round of tech interviews and had multiple HR interviews. In the evening, I got the result.

Closing Note:

Towards the end, the technical recruiter from Qualcomm did say that all the skills and knowledge toh you can develop later as well, but the striking quality that you have right now is your communication skills. So, it's important to convey your information with the right confidence and in a clear and concise manner.

Don't try to act smart with the panelist. They were students once, so they'll know when you're stalling or when you're trying to evade the question. They are there to help you only and they keep pushing you by giving hints as well. Give them the respect they deserve.

Prepare thoroughly and confidence will come. Stay in touch with your batchmates and friends from other colleges to get their experiences as well. Be honest in your preparation and I'm sure you'll ace it.

Best of luck!