FIFO Depth Calculation

Introduction

FIFO is a distinct kind of buffer. First in, first out, or FIFO, refers to the order in which data is written to and read from a buffer. A FIFO (First-In-First-Out) is a memory queue, which controls the data flow between two modules.

Why do we use FIFO in VLSI?

FIFOs are used in designs to safely pass multi-bit data words from one clock domain to another, or to control the flow of data between source and destination sides sitting in the same clock domain.

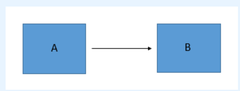
What are the different types of FIFO?

Three kinds of FIFO are Shift Register, Exclusive read/write FIFO, Concurrent read/write FIFO.

- **Shift register:** A type of digital circuit using a cascade of flip-flops where the output of one flip-flop is connected to the input of the next.
- **Exclusive Read/Write FIFOs:** In exclusive read/write FIFOs, the writing of data is not independent of how the data are read. There are timing relationships between the write clock and the read clock. For instance, overlapping of the read and the write clocks could be prohibited. To permit use of such FIFOs between two systems that work asynchronously to one another, an external circuit is required for synchronization. But this synchronization circuit usually considerably reduces the data rate.
- **Concurrent Read/Write FIFOs:** In concurrent read/write FIFOs, there is no dependence between the writing and reading of data. Simultaneous writing and reading are possible in overlapping fashion or successively. This means that two systems with different frequencies can be connected to the FIFO. The designer need not worry about synchronizing the two systems because this is taken care of in the FIFO. Concurrent read/write FIFOs, depending on the control signals for writing and reading, fall into two groups Synchronous FIFOs and Asynchronous FIFOs.
  - **Synchronous FIFOs:**In a Synchronous FIFO, the write and read to the FIFO happen on a single clock. This means in Synchronous FIFO, either write or read can happen at a single time (on single clock).In Synchronous FIFO the read and write operations are performed at the same rate.
  - **Asynchronous FIFO:**In asynchronous FIFO, data read and write operations use different clock frequencies. Since write and read clocks are not synchronized, it is referred to as asynchronous FIFO. Usually, these are used in systems where data need to pass from one clock domain to another which is generally termed as 'clock domain crossing'. Thus, asynchronous FIFO helps to synchronize data flow between two systems working on different clocks.

FIFO Depth Calculation

The following examples describe the different possible scenarios in which Asynchronous FIFO is required. In the following examples, considered that, the module 'A' wants to send some data to the module 'B'.



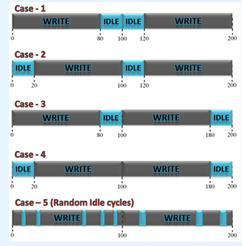
- **Case – 1 : fA > fB with no idle cycles in both write and read.**
- frequency = fA = 80MHz.
- Reading Frequency = fB = 50MHz.
- Burst Length = No. of data items to be transferred = 120.
- There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles.
- **Sol:**
- Time required to write one data item = 1/80MHz = 12.5 nSec.
- Time required to write all the data in the burst = 120 * 12.5 nSec. = 1500 nSec.
- Time required to read one data item =1/50MHz= 20 nSec.
- So, for every 20 nSec, the module B is going to read one data in the burst.
- So, in a period of 1500 nSec, 120 no. of data items can be written.
- And the no. of data items can be read in a duration of 1500 nSec =1500nSec/20nSec=75
- The remaining no. of bytes to be stored in the FIFO = 120 – 75 = 45.
- So, the FIFO which has to be in this scenario must be capable of storing 45 data items.**So, the minimum depth of the FIFO should be 45.**
- **Case – 2 : fA > fB with one clk cycle delay between two successive reads and writes.**
- **Sol:**
- This is just, to create some sort of confusion. This scenario is no way different from the previous scenario (case -1), because, always, there will be one clock cycle delay between two successive reads and writes. So, the approach is same as the earlier one.
- **Case – 3 : fA > fB with idle cycles in both write and read.**
- Writing frequency = fA = 80MHz.
- Reading Frequency = fB = 50MHz.
- Burst Length = No. of data items to be transferred = 120.
- No. of idle cycles between two successive writes is = 1.
- No. of idle cycles between two successive reads is = 3.
- The no. of idle cycles between two successive writes is 1 clock cycle.

FIFO Depth Calculation Cont...

- **Sol:**
- It means that, after writing one data, module A is waiting for one clock cycle, to initiate the next write. So, it can be understood that for every two clock cycles, one data is written.
- The no. of idle cycles between two successive reads is 3 clock cycles. It means that, after reading one data, module B is waiting for 3 clock cycles, to initiate the next read. So, it can be understood that for every four clock cycles, one data is read.
- Time required to write one data item = 2 * 1/ 80Mhz = 25 nSec.
- Time required to write all the data in the burst = 120 * 25 nSec. = 3000 nSec.
- Time required to read one data item = 4 * 1/ 50MHz = 80 nSec.
- So, for every 80 nSec, the module B is going to read one data in the burst.
- So, in a period of 3000 nSec, 120 no. of data items can be written.
- The no. of data items can be read in a period of 3000 nSec = 3000nSec/80nSec =37.5 ≈37
- The remaining no. of bytes to be stored in the FIFO = 120 – 37 = 83.
- So, the FIFO which has to be in this scenario must be capable of storing 83 data items. **So, the minimum depth of the FIFO should be 83.**
- **Case – 4 : fA > fB with duty cycles given for wr_enb and rd_enb.**
- **Sol:**
- This scenario is no way different from the previous scenario (case - 3), because, in this case also, one data item will be written in 2 clock cycles and one data item will be read in 4 clock cycles.
- **Case – 5 : fA < fB with no idle cycles in both write and read (i.e., the delay between two consecutive writes and reads is one clock cycle).**
- Writing frequency = fA = 30MHz.
- Reading Frequency = fB = 50MHz.
- Burst Length = No. of data items to be transferred = 120.
- There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles.
- **Sol:**In this case, a FIFO of depth '1' will be sufficient because, there will not be any data loss since the reading is faster than writing.
- **Case – 6 : fA < fB with idle cycles in both write and read (duty cycles of wr_enb and rd_enb can also be given in these type of questions).**
- Writing frequency = fA = 30MHz.
- Reading Frequency = fB = 50MHz.
- Burst Length = No. of data items to be transferred = 120.
- There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles.
- **Sol:**
- The no. of idle cycles between two successive writes is 1 clock cycle. It means that, after writing one data, module A is waiting for one clock cycle, to initiate the next write. So, it can be understood that for every two clock cycles, one data is written.
- The no. of idle cycles between two successive reads is 3 clock cycles. It means that, after reading one data, module B is waiting for 3 clock cycles, to initiate the next read. So, it can be understood that for every four clock cycles, one data is read.
- Time required to write one data item = 2 * 1 /30MHz = 66.667 nSec.
- Time required to write all the data in the burst = 120 * 66.667 nSec.= 8000 nSec.
- Time required to read one data item = 4 * 1 /50MHz = 80 nSec.
- So, for every 80 nSec, the module B is going to read one data item in the burst.
- So, in a period of 8000 nSec, 120 no. of data items can be written.
- The no. of data items can be read in a period of 8000 nSec = =100
- The remaining no. of bytes to be stored in the FIFO = 120 – 100 = 20.
- So, the FIFO which has to be in this scenario must be capable of storing 20 data items. **So, the minimum depth of the FIFO should be 20.**
- **Case – 7 : fA = fB with no idle cycles in both write and read (i.e., the delay between two consecutive writes and reads is one clock cycle).**
- Writing frequency = fA = fB = 30MHz.
- Burst Length = No. of data items to be transferred = 120.
- There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles.
- **Sol:**
- FIFO is not required if there is no phase difference between clkA and clkB.
- A FIFO of depth '1' will be sufficient if there is some phase difference between clkA and clkB.
- **Case – 8 : fA = fB with idle cycles in both write and read (duty cycles of wr_enb and rd_enb can also be given in these type of questions).**
- Writing frequency = fA = 50MHz.
- Reading Frequency = fB = 50MHz.
- Burst Length = No. of data items to be transferred = 120.
- No. of idle cycles between two successive writes is = 1.
- No. of idle cycles between two successive reads is = 3.
- **Sol:**
- The no. of idle cycles between two successive writes is 1 clock cycle. It means that, after writing one data, module A is waiting for one clock cycle, to initiate the next write. So, it can be understood that for every two clock cycles, one data is written.
- The no. of idle cycles between two successive reads is 3 clock cycles.

FIFO Depth Calculation Cont...

- It means that, after reading one data, module B is waiting for 3 clock cycles, to initiate the next read. So, it can be understood that for every four clock cycles, one data is read.
- Time required to write one data item = 2 * 1/ 50MHz = 40 nSec.
- Time required to write all the data in the burst = 120 * 40 nSec. = 4800 nSec.
- Time required to read one data item = 4 * 1/ 50MHz = 80 nSec.
- So, for every 80 nSec, the module B is going to read one data item in the burst.
- So, in a period of 4800 nSec, 120 no. of data items can be written.
- The no. of data items can be read in a period of 4800 nSec =4800nSec/80nSec =60
- The remaining no. of bytes to be stored in the FIFO = 120 – 60 = 60.
- So, the FIFO which has to be in this scenario must be capable of storing 60 data items.**So, the minimum depth of the FIFO should be 60.**
- **Case – 9 : If the data rates are given as follows.**
- Writing Data = 80 DATA/100 Clock (Randomization of 20 Data's)
- Outgoing Data= 8 DATA/10 Clock.
- Burst size = 160
- **Sol:**
- The given specifications indicate that the Writing Frequency is equal to reading frequency.
- But, both reading and writing can happen at any random instants with the constraints that "writing of 80 data items will be completed in 100 cycles" and "reading of 8 data items will be completed in 10 cycles".
- The following are possibilities.



- The following are the observations from the above diagram.

Case	No. of cycles taken to complete write
1	200
2	200
3	180
4	160
5	200

- To obtain safer FIFO size, we need to consider the worst case scenario for the data transfer across the FIFO under consideration to avoid the data loss.
- For worst case scenario, the difference between the data rate between write and read should be maximum. Hence, for write operation, maximum data rate should be considered and for read operation, minimum data rate should be considered.
- The maximum data rate for the write is in case – 4. (Write operation is completed in minimum no. of cycles in this case). So, consider the case - 4 for further calculations.
- So, in a period of 160 clock cycles, 160 no. of data items can be written.
- The data rate for the read is 8 data / 10 clock cycles.
- The no. of data items can be read in a period of 160 clock cycles = (160 * 8)/10=128
- The remaining no. of bytes to be stored in the FIFO = 160 – 128 = 32.
- So, the FIFO which has to be in this scenario must be capable of storing 32 data items.**So, the minimum depth of the FIFO should be 32.**
- **Case – 10 : Specifications can be given in a different way. (Understanding the specifications is important here)**
- Given the following FIFO rules, how deep does the FIFO need to be to prevent underflow or overflow?
- Frequency (clk A) = frequency (clk B)/4
- Period en_B = period clk_A*100
- Duty cycle (en_B) = 25%
- **Sol:**
- Assume some numerical values, if the specifications are in this way.
- Assume frequency of clk_B = 100MHz
- So, the frequency of clk_A = 100MHz /4 = 25MHz.
- In the specifications given, the burst length is specified indirectly. The burst length is 100.
- Time required to write one data item = 1/25Mhz = 40 nSec.
- Time required to write all the data in the burst = 100 * 40 nSec. = 4000 nSec.
- And the duty cycle of en_B is 25 % means that, out of 4000 nSec in which the writing process is completed, reading is done only in a period of 1000 nSec (25% of 4000 nSec.)
- So, the FIFO should be capable of holding the data which is being written in the remaining 3000 nSec.
- The no. of data items can be read in a period of 3000 nSec =3000nSec/40nSec =75**So, the minimum depth of the FIFO should be 75.**

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