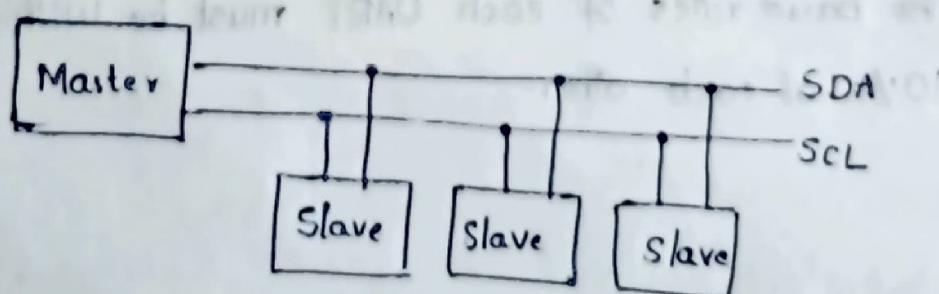


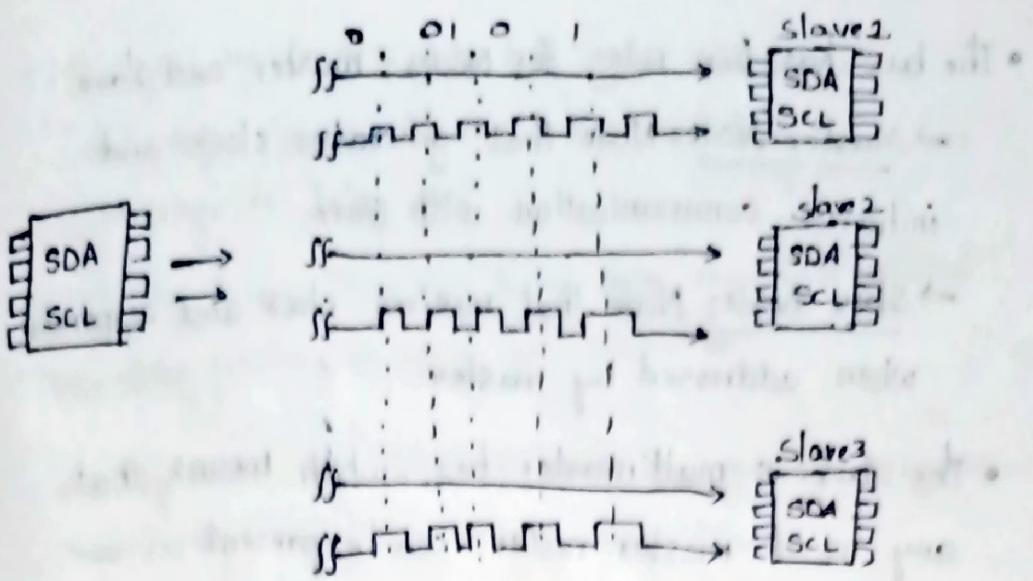
I²C (inter integrated circuit).

- introduced by phillips company & NXP Semiconductor in 1972.
- Synchronous protocol [we use clock]
- it is multiple master & multi Slave
- it is packet switched.
- Single ended.
- I²C is widely used for attaching lower-speed peripheral IC's to processors and microcontrollers in short distance, intraboard communication.
- A particular strength of I²C is the capability of microcontroller to control a network of device chips with just two general purpose I/O pins & software.
- Many other bus technologies used in similar application, such as SPI bus, require more pins & S/I's to connect multiple devices.

Design:

- I²C uses only two bidirectional open-drain lines, Serial data line (SDA) and serial clock line (SCL) pulled up with Resistors.



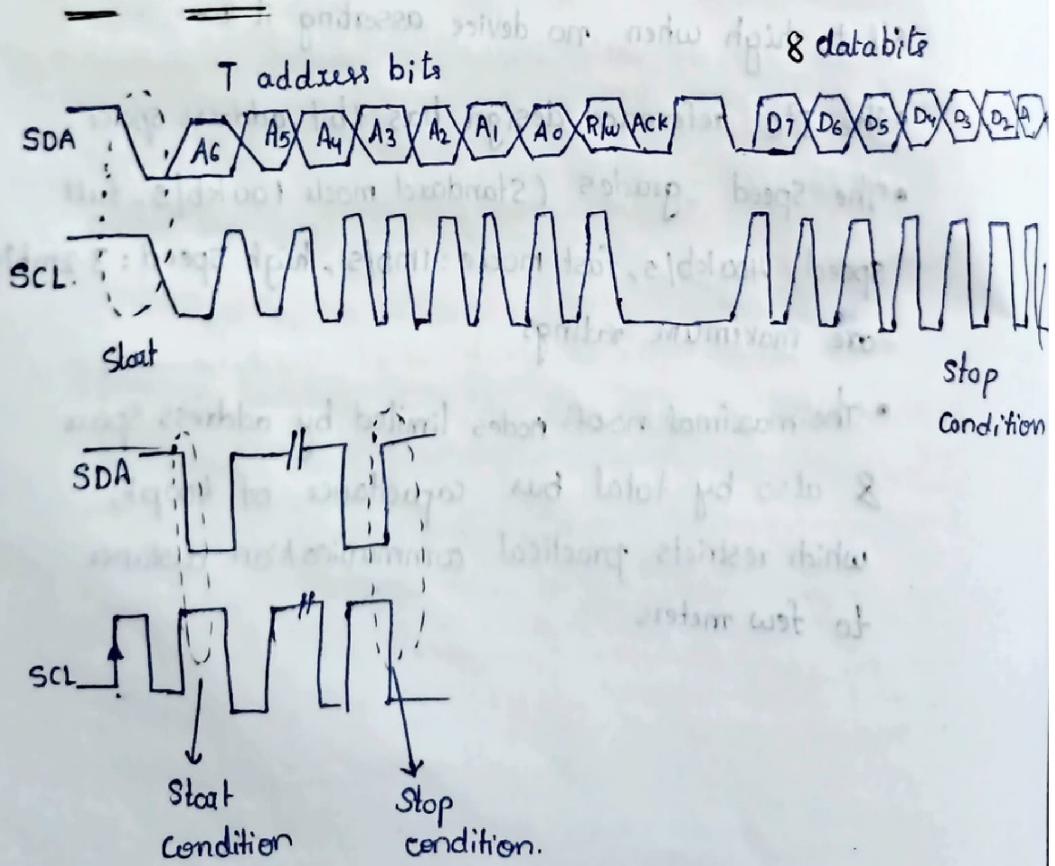


- The I²C bus drivers are "Open drain", means that they can pull corresponding s/l line low, but can't drive it high.
- Thus, there can be no bus contention where one device is trying to drive the line high while another tries to pull it low, eliminating the potential for damage to the drivers or excessive power dissipation in system.
- Each s/l line has a pull-up resistor on it, to restore s/l to high when no device asserting it low.
- The I²C reference design has 7bit address space.
- The Speed grades (Standard mode : 100 kb/s, full speed : 400 kb/s, fast mode : 1mb/s, high speed : 3.2mb/s) are maximum ratings.
- The maximal no.of. nodes limited by address space & also by total bus capacitance of 400pF, which restricts practical communication distance to few meters.

- The bus has two roles for Nodes: master and slave.
 - Master Node: Node that generates clock and initiates communication with slave.
 - Slave Node: Node that receives clock and responds when addressed by master.

- The bus is multimaster bus, which means that any no. of master nodes can be present.
- Additionally, master & slave roles may be changed b/w messages (after STOP sent).
- There are 4 modes:
 - Master Transmit: Master Node sending data to slave
 - Master Receive: Master node receiving data from slave
 - Slave Transmit: slave node sending data to master
 - Slave Receive: Slave node receiving data from master.

Frame Format:



- Messages are broken into two types of frame:

→ Address frame: Master indicates slave to which message is being sent

→ Data frame: There are 8 bit data messages passed from master to slave or viceversa.

- Data placed on SDA line after SCL goes low, & is sampled after SCL line goes high.

- Start condition:

→ To initiate address frame, master device leaves SCL high and pulls SDA low.

→ This puts all slave devices on notice that a transmission is about to start.

→ If two master devices wish to take ownership of bus at one time, whichever pulls SDA low 1st wins race & gains control of bus.

- Address frame:

→ Address frame is always first in any new communication sequence.

→ For 7 bit address, address clocked out most significant bit first, followed by R/W bit indicating whether it is read (1) or write operation.

- NACK/Ack bit:

→ 9th bit of frame.

→ This is case for all frames (data or address)

→ Once, 1st 8 bits of frame are sent, receiving device is given control over SDA.

→ If receiving device does not pull SDA line low before 9th clock pulse, it is inferred that receiving device

- In that case, the exchange halts, and it's up to the master of the system to decide how to proceed.

- Data frame:

- After Address frame has been sent, data can begin being transmitted.
- the master will simply continue generating clock pulses at a regular interval, and data will be placed on SDA by either master or slave, depending on whether R/W bit indicated read/write operation.

- Stop Condition:

- Once all data frames have been sent, master will generate stop.
- Stop condition defined by $0 \rightarrow 1$ (low to high) transition on SDA after $0 \rightarrow 1$ transition on SCL, with SCL remaining high.

I₂C protocol:

1. The master initially in master transmit mode by sending START followed by 7-bit address of slave, it wishes to communicate with.
2. This is finally followed by single bit representing whether it wishes to write (0) to or read (1) from slave.
3. if slave exists on bus then it will respond with an Ack bit (active low for acknowledged) for that address.

4. the master then continues in either transmit or receive mode (according to read/write bit it sent), & slave continues in complementary mode (receive or transmit respectively).
5. the address and data bytes are sent most significant bit 1st.
6. The master terminates a message with STOP condition if this is end of transaction or it may send another START condition to retain control of bus for another message.

Applications:

- Describing connectable devices via small ROM configuration tables to enable "plug and play" operation such as
 - Accessing real-time clocks and NVRAM chips that keep user settings.
 - Accessing low-speed DACs and ADCs.
 - Controlling LCD displays.

Master: who will initiate transfer & gen. clk s/l to transfer
Slave: it will respond to master.

Two wired Communication: SDA, SCL
SDA, SCL