ECE5023	MEMORY DESIGN AND TESTING	L	T	P	J	C
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Pre-requisite	**Nil**					**v 1.1**

Course Objectives:

The course is aimed at

1. Expounding the basics and detailed architecture of SRAMs and DRAMs.
2. model the memory fault and introduce the basic and advanced memory testing patterns.
3. Elaborate the reliability and radiation effect issues of semiconductor memories and present methods for radiation hardening.
4. Review and discuss high performance memory subsystems, advanced memory technologies and contemporary issues

Expected Course Outcome :

At the end of the course the student should be able to

1. Design SRAMs and DRAMs.
2. Design NVRAMs and Flash Memories.
3. Model memory faults, select suitable testing patterns and develop testing patterns.
4. Incorporate DFT and BIST techniques for semiconductor memory testing.
5. Improve the reliability of semiconductor memories, simulate and model radiation effects and, perform radiation hardening.
6. Contribute to the development of high performance memory subsystems and use advanced memory technologies.

Student Learning Outcomes (SLO): **1,6**

Module:1	**Volatile memories**	**5 hours**

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, SOI technology, Advanced SRAM architectures and technologies, soft error failure in SRAM, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

Module:2	**Non-volatile memories**	**5hours**

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

Module:3	**Memory Testing and Patterns**	**7hours**

General Fault Modeling – Read Disturb Fault Model – Precharge Faults – False Write Through Data Retention Faults – Decoder Faults. Megabit DRAM Testing Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing Application Specific Memory Testing – Zero/one Pattern – Exhaustive Test Patterns – Walking, Matching and Galloping – Pseudo Random Pattern – CAM pattern.

Module:4	**Design For Test and BIST**	**4hours**

RAM Built-In Self – Test (BIST)-Weak Write Test mode – Bit Line Contact Resistance – PFET Test – Shadow Write and Shadow Read.		
Module:5	**Reliability and Radiation Effects**	**7hours**
General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Design for Reliability Radiation Effects-Single Event Phenomenon (SEP)- Radiation Hardening Techniques Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics.		
Module:6	**High-Performance Subsystem Memories**	**7hours**
Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories.		
Module:7	**Advanced Memory Technologies**	**8hours**
High-Density Memory Packaging Technologies, Ferroelectric Random Access Memories (FRAMs)- Analog Memories-Magneto-resistive Random Access Memories (MRAMs)-Experimental Memory Devices Memory Hybrids and MCMs (2D)- Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45hours**

Text Book(s)

1.	A. K.Sharma, Advanced Semiconductor Memories: Architecture, Design and Applications, John Wiley, 2014.
2.	Roberto Gastaldi and Giovanni Campardo In Search of the Next Memory: Inside the Circuitry from the Oldest to the Emerging Non-Volatile Memories, Springer, 2017.

Reference Books

1.	Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel, Advanced Test Methods for SRAMs: Effective Solutions for Dynamic Fault Detection in Nanoscaled Technologies, Springer, 2010.
2.	Hao Yu and YuhaoWang,Design Exploration of Emerging Nano-scale Non-volatile Memory, Springer, 2014.
3.	Takayuki Kawahara (Editor), Hiroyuki Mizuno (Editor), Green Computing with Emerging Memory: Low-Power Computation for Social Innovation, Springer, 2012.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

Recommended by Board of Studies	28/02/2017		
Approved by Academic Council	47th AC	Date	05/10/2017