ECE5020	DSP ARCHITECTURES	L	T	P	J	C
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Pre-requisite	**Nil**			**v 1.0**		

Course Objective:

The course is aimed to

1. Explore different Digital Signal Processor (DSP) architectures and to design systems using programmable DSPs.
2. Improve system performance using different pipelining techniques, processor array and systolic array.
3. Interface of memory and peripherals to a DSP; and acquire knowledge on different codec implemented on DSP.

Expected Course Outcome:

The students will be able to

1. Identify and use specific Digital Signal Processor for various applications.
2. Design a system using programmable DSP.
3. Implement pipelining techniques to improve system performance.
4. Implement applications using processor array and systolic arrays to enhance the performance.
5. Design involving memory and other interfaces to DSP.
6. Design of various codecs on target DSPs.

Student Learning Outcomes (SLO): 1,17

Module:1	**DSP Integrated Circuits and VLSI Technologies**	**2hours**

Standard digital signal processors - Application specific IC's for DSP - DSP systems - DSP system design - Integrated circuit design.

Module:2	**Architectures for programmable DSP**	**4 hours**

Basic Architectural Features - DSP Computational Building Blocks - Bus Architecture and Memory - Data Addressing Capabilities - Address Generation Unit - Programmability and Program Execution - Features for External Interfacing.

Module:3	**Execution Control and Pipelining**	**4 hours**

Hardware looping – Interrupts – Stacks - Relative Branch support - Pipelining and Performance - Pipeline Depth – Interlocking - Branching effects - Interrupt effects - Pipeline Programming models.

Module:4	**Synthesis of DSP Architectures**	**6hours**

Top Down approach to DSP LSI - Circuit Synthesis - High Performance Data conversion Techniques - LSI Algorithms and Architectures - Hierarchical Design of Processor Arrays - Systolic Arrays - Stack Filters - Wave-front Array Processors.

Module:5	**Interfacing Memory and I/O to DSP Processors**	**5hours**

External bus interfacing signals - Memory interface - Parallel I/O interface - Programmed I/O -

Interrupts and I/O -Direct memory access (DMA) A Multichannel buffered serial port (McBSP) - McBSP Programming.		
Module:6	**Interfacing CODEC**	**3hours**
CODEC interface circuit - CODEC programming - A CODEC-DSP interface example.		
Module:7	**Multiprocessor Systems**	**4hours**
Architectures of Multiprocessors-Performance comparison of -Multiprocessor Structures.		
Module:8	**Contemporary issues:**	**2hours**
	Total Lecture hours:	**30hours**

Text Book(s)	
1.	Lars Wanhammer, DSP Integrated Circuits,Academic press, New York, 2011.
2.	Avtar Singh and S. Srinivasan, Digital Signal Processing, Thomson Publications, 2012.
Reference Books	
1.	Phil Lapsley, Jeff Bier, AmitShoham, Edward A. Lee, DSP Processor Fundamentals, Architectures & Features,Wiley-IEEE Press, First Edition,2011.
2.	Peter Pirsch, Architectures for Digital signal processing, Wiley India, 2010.

Mode of Evaluation: Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Projects (Indicative)

1. Image Compression algorithm implementation in Programmable DSP.
2. Image processing algorithm implementations on FPGA.
3. Turbo Decoder implementation.
4. CORDIC Algorithm implementation in PDSP/FPGA/ASIC flow.
5. Improved Adaptive filters.
6. Improved Median filters.

Mode of Evaluation:Review I, II and III

Recommended by Board of Studies	13-12-2015		
Approved by Academic Council	No. 40	Date	18-03-2016