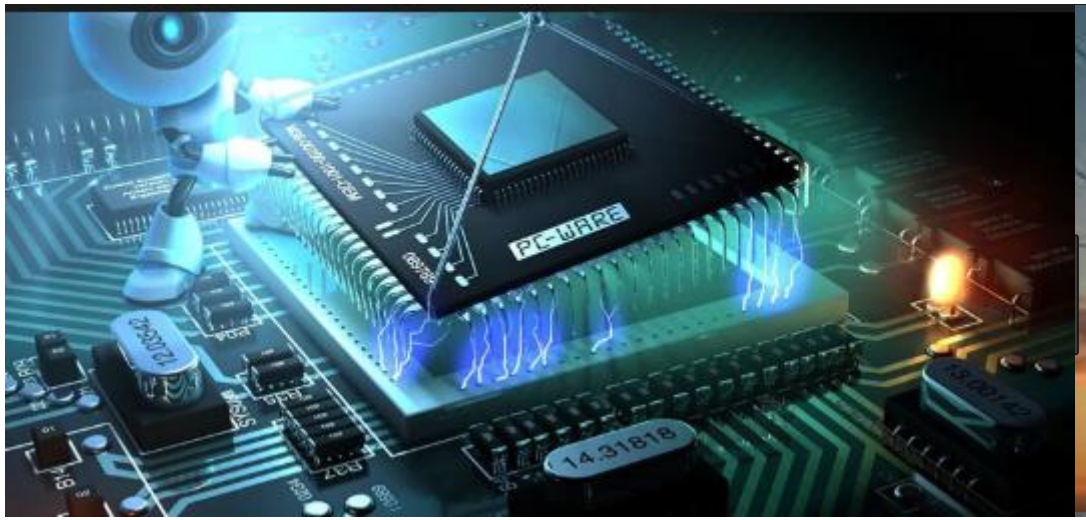


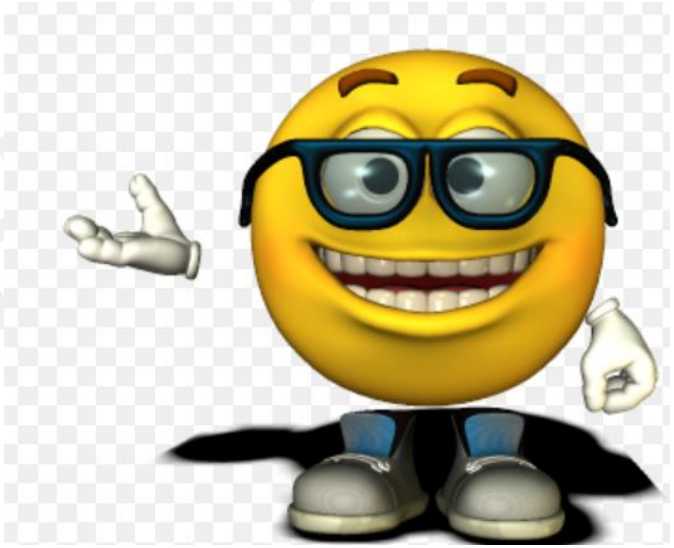
IC Planning and Implementation (Physical Design)

Power planning/Power network synthesis -PNS

Session objective

To understand

- What is power plan
- Why do we need power plan
- PNS key terminologies
- Traditional PG creation flow



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What is Power planning/PNS?

- Power planning is stage typically part of the FP stage , in which PG grid network is created to distribute the power to each part of the chip .
- Power planning can be done manually as well as automatically through tool
- Power planning involves placement of
  - Core power ring
  - Vertical and Horizontal power straps in the core
  - Standard cells power hook up
  - Block power hook up
  - IO power hook up

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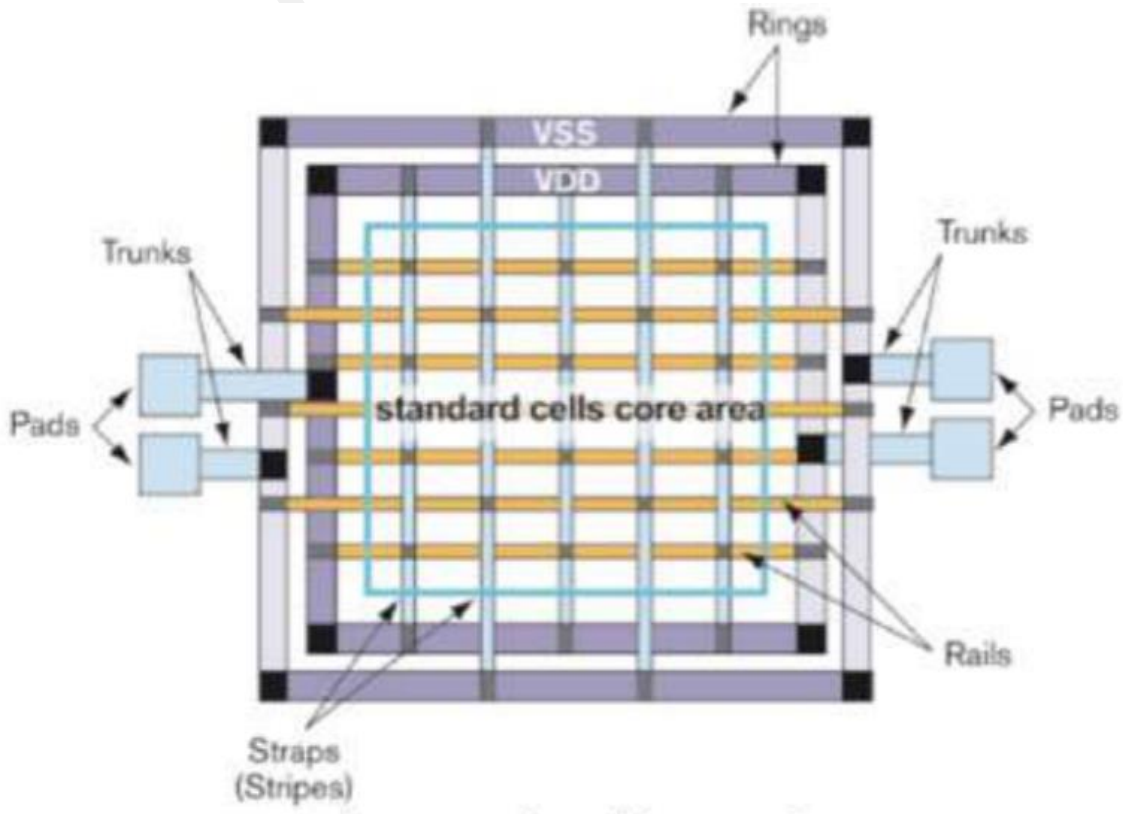
Why do we need power planning?

PNS key terminologies

Below are the key terminologies in PNS

1. Power pads
2. Power trunks
3. Power rings
4. Power rails



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Inputs required for power planning

1. Floorplan database (ICC Floorplan MW design library)

2. Logical PG connectivity of standard/macro cells or Power domain information (Voltage area has to be created according to power domain defined inside UPF)

3. Power rings and power strap width

4. Spacing b/w the VDD and VSS straps

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Outputs after power planning

1. Physical PG connection done for all the cells in the design (Design with power structure)

2. PG DRC count

3. Estimation of possible PG DRC fixes (Early estimation should be done before fixing to ease out the pressure at end ☺)

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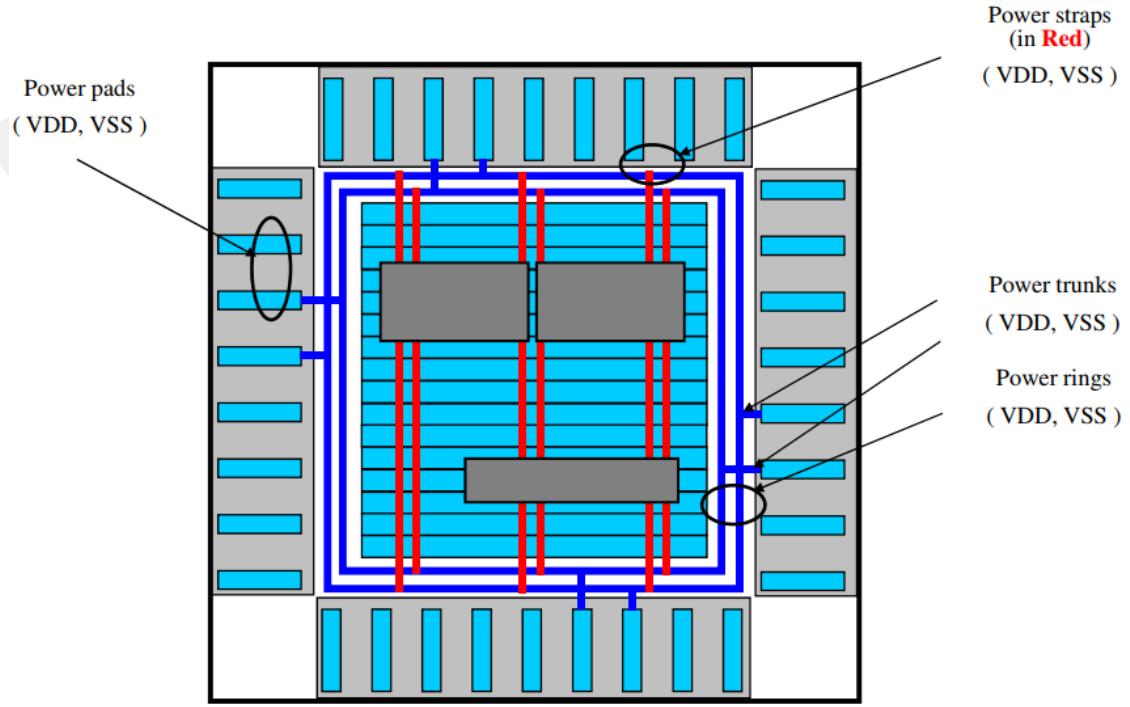
Chip level power management

Chip-level power management can be treated as two parts

- Core cell power management
- I/O cell power management



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Traditional PG creation flow

Steps to manually create PG mesh

- Establish Logical PG Connectivity(Global logical net connection)
- Create core rings
- Create Straps and block rings
- Preroute Cells
- Verify PG net connectivity

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Power plan calculation - Number of Core and IO Power Pads

Input data to required for calculating number of core and IO power pads

– Number of sides (on chip)
– Total Dynamic core power (mW)
– Core voltage (TYPICAL, vdc)
– Power PAD library name
– Maximum allowable current (mA)
– Ground PAD library name
– Maximum Allowable Current (mA)

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Power plan calculation - Number of Core and IO Power Pads

Total number of core power pad's required

Total number of core power pad's required for each side of the chip = Total core power / [number of side*core voltage*maximum allowable current for a I/O pad]

Example calculation

- Total core power - 37.25mW
- Number of sides - 4
- Core voltage – 1.8V
- Maximum allowable current 29mA

$$\frac{37.25\text{mW}}{4\,\text{X}\,1.8\text{V}\,\text{X}\,29\text{mA}} \Rightarrow 0.178 \approx 1$$

Total number of power pads required is "1"

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Power plan calculation - Core Ring Calculations

Input data required to calculate the

- Power Net (layer metal) = choose metal X
- Ground Net (layer metal) = choose metal Y
- Jmax (layer metal, mA/um) - 1mA/um
- Via max current (mA) - 0.403mA
- Total core power (mW) - 37.25mW
- Core voltage (Typical, vdc) - 1.8V
- Number of sides (on chip) - 4

✓ Total Dynamic core current (mA):

$$\frac{\text{Total Dynamic Core Power}}{\text{Typical Core Voltage}} \Rightarrow \frac{37.25\text{mW}}{1.8\text{V}} \Rightarrow 20.694\text{mA}$$

Power plan calculation - Core Ring Calculations

- ✓ PAD to CORE trunk width (um):

$$\frac{\text{Total Dynamic core current}}{(\text{Number of sides} * \text{Jmax})} \Rightarrow \frac{(20.694\text{mA})}{(4*1)} \Rightarrow 5.1735$$

- ✓ Via count for PAD to CORE trunk

$$\frac{(\text{Total Dynamic core current})}{(\text{Via Max current} * \text{Number of sides})} \Rightarrow \frac{(20.694\text{mA})}{(0.403*4)} \Rightarrow 12.875 \approx 12$$

Management of block level power meshes

- ✓ Calculate the current consumption for each sub-block:
  - $I_{block} = P_{block} / V_{ddcore}$
- ✓ Assuming that the current was supplied evenly from the boundary of the block, calculate the current supply from each side of the block in proportion to the block width or height:
  - $I_{top} = I_{bottom} = \{I_{block} \times [W_{block} / (W_{block}+H_{block})]\} / 2$
  - $I_{left} = I_{right} = \{I_{block} \times [H_{block} / (W_{block}+H_{block})]\} / 2$
  - $W_{strap\_vertical} (= W_{strap\_top} = W_{strap\_bottom}) = I_{top} / J_{metal}$
  - $W_{strap\_horizontal} (= W_{strap\_left} = W_{strap\_right}) = I_{left} / J_{metal}$

Power planning is done after PG grid creation ?

No….!

What is next? ?

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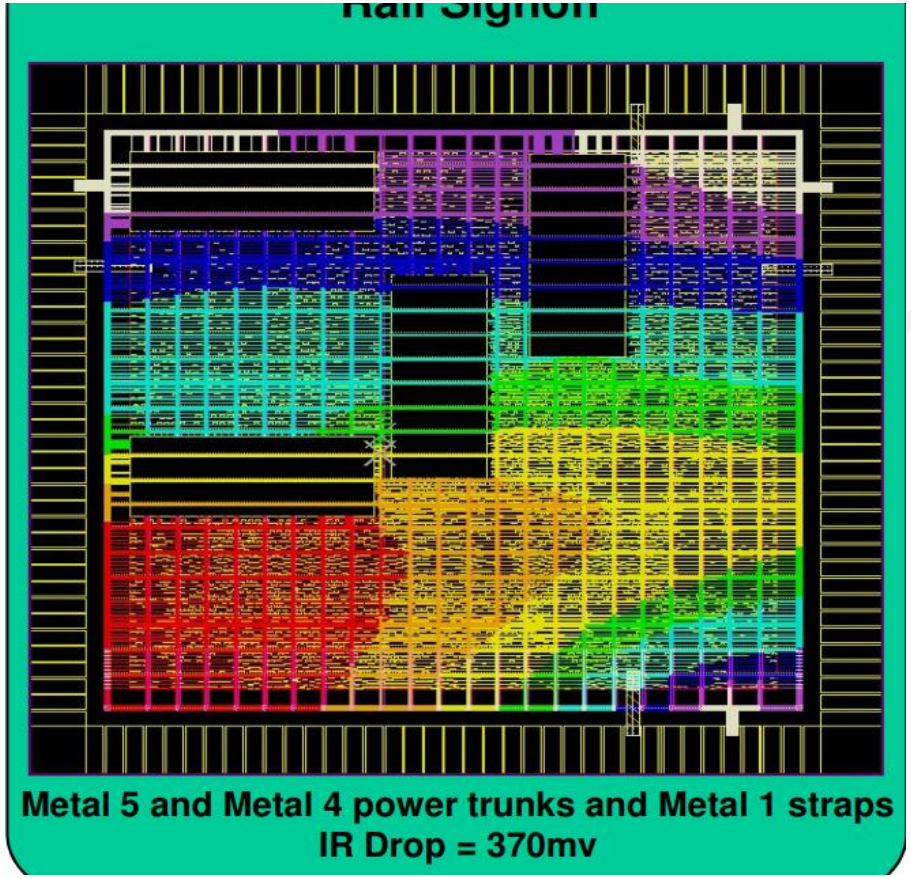
IR Drop analysis

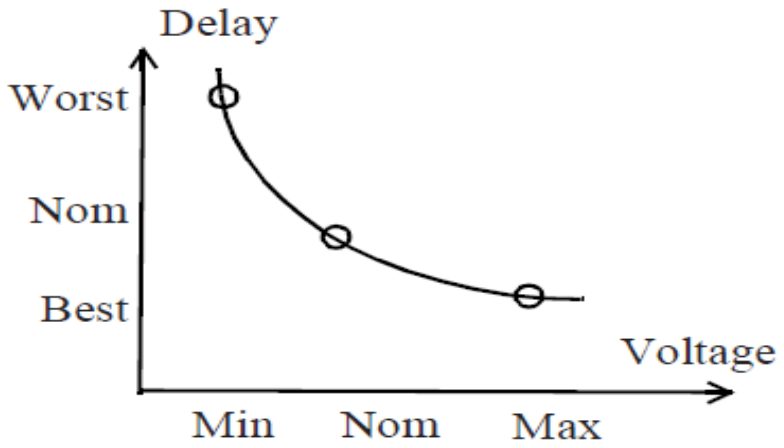


- IR drop is a reduction in voltage that occurs on both power and ground networks in integrated circuits.
- Narrower metal line widths cause an increase in the metal resistance and therefore in the amount of the voltage drop in the chip
- The amount of the voltage drop depends on the effective resistance from the power pads to the logic gates.
- The voltage drop is calculated by the following formula

$$V = Iavg * Reff$$

How does IR drop impact timing?

- As the voltage at gate decreased due to unacceptable voltage drop in supply voltage, the gate delays are increased non-linearly. This may lead to setup time and hold time violations
- Increase in delay , how does impact Setup/Hold timing?



(b) Delay vs voltage.

Type of IR analysis

Below are the types of IR analysis

1. Static IR drop analysis :- Static IR drop is the voltage drop, when a constant current draws through the power network with varying resistance. this IR drop occurs when the circuit is in steady state. To reduce static IR issues, you should increase width of the power network, or a robust power grid has to be designed

Static IR drop (Vstatic) = Iavg * Rwire

2. Dynamic IR drop analysis :- Dynamic IR drop is the drop when the high current draws the power network due to the high switching of the cell. To reduce Dynamic IR drop, reduce the toggle rate or place decap cells near high switching cells

Dynamic IR drop (Vdynamic) = L(dI/dt)

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Method to reduce the voltage IR drop

- Reducing the current consumption (*I*avg) of logic gates. Therefore, any low power design techniques on the circuit will help. Process scaling or capacitance reduction will also help.

- Another alternative is to increase the number of *Vdd* and *Vss* pads in the chip to reduce the current consumption for each pair of *Vdd* and *Vss* pads.

- If the gates along the metal line switch together, the IR drop can be larger due to the increased *I*avg. Therefore, some alternative switching order for large current gates helps to reduce the IR drop.

-Reducing the wire resistance. In this category, the widening of the metal lines for power lines, or adding more power lines in the layout are obviously preferred in the power grid floor plan

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Method to reduce the voltage IR drop

- In addition, multiple power layers with extremely dense power lines in the layout are used for high-performance microprocessors. The wire resistance is also proportional to the metal line length from the power pads to the logic gates.

- The C4 package (Flipchip) technology provides the area I/O pads, which can provide short power lines. Therefore, most high performance chips currently use the C4 technology instead of the wire-bonding technology for this reason.

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If you have both IR drop and congestion how will you fix it?

- Spread macros

- Spread standard cells

- Increase strap width

- Increase number of straps

- Use proper blockage

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Sanity checks after power planning

1. Design with PG structure:- All the cells should get a power
2. Understand & Fix if any PG pins open exists
3. Fix if any PG shorts exists in the design
4. Understand the PG DRC’s
5. Understand the IR drop impact for design PG grid and improve the grid to provide acceptable IR drop
6. Power EM checks

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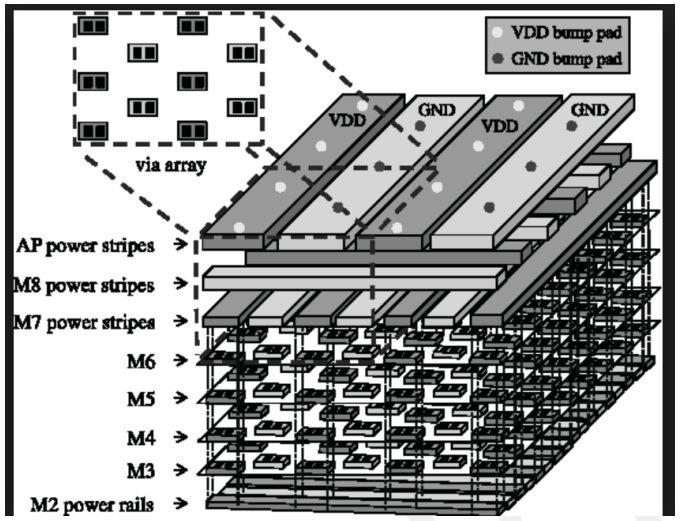
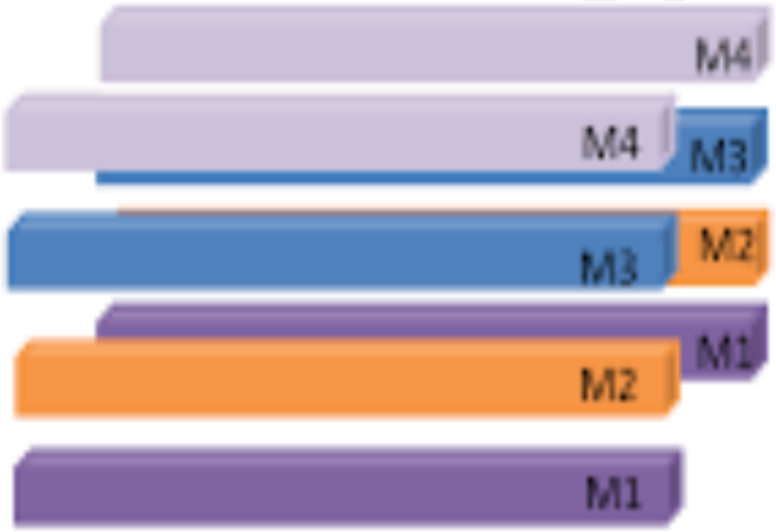
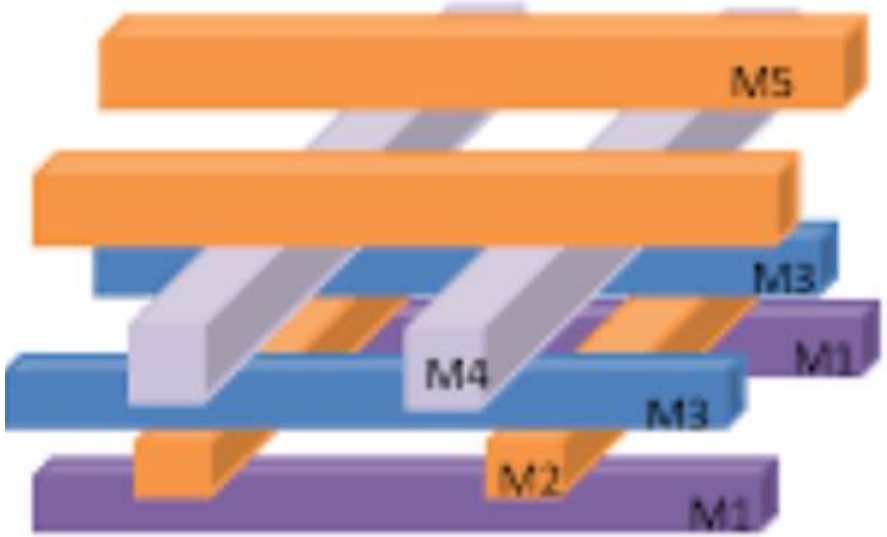
Different metal layer orientation



parallel metal layer orientation



Cross metal layer orientation



Tools used in IR analysis

1. Voltus from Cadence
2. Red hawk from Apache

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Helpful links

1. https://www.apache-da.com/system/files/Dynamic_Voltage_drop.pdf
2. http://www.serc.iisc.ernet.in/graduation-theses/thesis/ks_mar07.pdf
3. http://chipdesignmag.com/display.php?articleId=966
4. http://www.vlsi-basics.com/2013/09/floorplaning-interview-questions.html

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PG planning ICC command info

set_fp_rail_constraints :- This command sets the power network synthesis (PNS) constraints for power planning, including power strap layer constraints, power ring constraints, and global constraints. Multiple core rings and sandwich core rings can also be generated

set_fp_block_ring_constraints : - Defines the power and ground rings that are automatically created around the macros when power network straps are synthesized by power network synthesis (PNS)

synthesize_fp_rail :- Synthesizes power networks or power switch arrays based on user-specified constraints. In a single run, you can synthesize either a power network for a single-voltage design, power networks for a multivoltage design, or a power switch array

create_power_straps :- Command to create the power straps in the design

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THANKS