1. reportGateCount :
2. all_inputs:
3. all_outputs:
4. all_clocks:
5. sizeof_collections [all_outputs]
6. dbget  top.insts.cell.name  -u
7. dbget  top.insts.cell.name  BUF*
8. dbget  top.inst.cell.name  BUF*
9. dbget [dbget    −P2    top.insts.cell.baseclass        block].name//Macro Insts
10. dbget [dbget    −P      top.insts.cell.baseclass        block].name//Macro cells
11. dbget [dbget    −P2    top.insts.cell.baseclass        block].orient//Macro orientation
12. dbget [dbget    −P2    top.insts.cell.baseclass        block].box//Macro coordinates
13. dbget [dbget    −P2    top.insts.cell.baseclass        core].name//std cells
14. dbget [dbget    −P2    top.insts.cell.baseclass        pad].name//pads
15. dbget   top.fplan.pBlkge.type  //gives blockage type (soft ,hard,partial)
16. dbgettop.fplan.pblkge.boxes  //blockage coordinateswith out cell view
17. dbgettop.fplan.pblkge.box  //blockage coordinates with cell view
18. createPlaceBlockage  -type hard  -box {x1,y1,x2,y2}
19. setEndcapMode   -help
20. addEndCap  -preCap<filler_name>        -postcap<filler_name> -prefix  name
21. addWellTap    -cell   FILL2 -cellInterval   20 -checkerBoard
22. cutRow  // is used for cut the row
23. dbQury  //
24. PlaceInstance   inst_name       coordinates
25. setObjFplanBox          Instance   <Ins_name>    coordinates //used to place Inst
26. AddInst    -cell <cell_name> -inst<Inst_name>   -loc  X1,Y1
27. deleteFiller    -inst<instname>
28. deleteFiller      -cell    FILL2
29. checkNetlist    //usd to netlist checks (floating i/p,multidrivenets ,Inst pin check : o/p pins
   connected to PG net……..)
30. checkDesign     -all
31. dbget -regexp [dbget -p2      top.insts.cell.baseClass   core].name    WELLTAP
32. dbget   [dbget  top.fplan.rows].box  //row coordinates
33. dbget   top.fplan.coreBox
34. dbget   top.fplan.coresite.size
35. dbget   top.fplan.pblkgs.type  hard
36. dbget   [dbget  -p top.fplan.pBlkgs  type  hard].boxes
37. editDelete   -shapes  {RING  STRIPE} -status {ROUTED FIXED}
38. deleteAllPowerPrerouts   // it delete all power plane
39. dbget   top.insts.name END*
40. dbget   [dbget  -p       top.inst.name  END*].box  //it gives endCap coordinates]
41. setEdit   {specify metal and spaceing}

42. editAddRoute<X         Y>
43. editCommitRoute<X     Y>
44. dbget   top.fplan.ioBox    //It gives IO boundary coordinates
45. dbget   top.fplan.ios   //it give IO pads
46. dbget    top.fplan.core2left //it give dist b/w core pads
47. specifyCellPad<cell_name><factor>
48. refinePlace
49. trialRoute     -maxRouteLayer 6
50. setPlaceMode -modulePadding<inst_name>facter
51. attachIOBuffer   -basename  new1  -out  BUFX3
52. SelectInst  New1*
53. Dbget top.insts.cell.name    *FF* //gives all flip flops
54. Dbget [dbget -p2 top.insts.cell.isSequential   1].name  //all registers
55. All_registers  (or)  all_registers  -flops
56. Sizeof_collection [all_registers  -flops]  // it give flop count
57. QueryDensityInBox    x1 y1 x2 y2
58. CreateDensityArea   x1 y2  x2  y2  50%
59. addTieHilo  -cell  TIELO  -prefix  TIE
60. dbget [dbget -p2 top.insta.instTerms.isTieLo 1].cell.name
61. setPlaceMode  -congEffort  medium
62. addNetnewName
63. AttachTerm<Inst_name><Pin_name><net_name>
64. queryPlaceDensity

## CTS-COMMANDS

1. get_clocks
2. get_property   [all_clocks]      period
3. get_property   [all_clocks]      sources
4. get_property   [get_clocks]    clock_network_pins
5. ChangeClockStatus     -nofixedBuffers      -all
6. deleteClockTree      -all
7. cleanUpSpecifyClockTree
8. dbget  -regexp   [dbgettop.nets].name  clk  //to get clock net names
9. dbget [dbget -p     top.nets.isCTSclock    1].name // to get clock net names
10. report_clock_timing    -type   skew/latency
11. set_interactive_constraint_modes     [all_constraints] // for Update SDC
12. set_timing_derate    -delay_corner dtmf_corner_max/min -data  10  -clock  5
13. reportTranViolation
14. report_constraints   -AllViolaters   //it reports all DRV violations
15. add_ndr        -width  {Metal1 0.46 . . . . . . . . . . . . . . . . .}
                          -spacing  {Metal1  0.3 . . . . . . . .. … . . . .} -name    NDR2W2S

16. exoprtNdr        NDR2W2S       -leffilename.lef
17. SetCTSMode      -routeLeafNonDefaultRule   NDR2W2S
18. setCTSMode      -routeShielding      VSS
19. setCTSmode      -specmultimode      true
20. createClockTreeSpec     -file       name.ctstch  -bufferlist {CLKINVX2  CLKINVX4 …… }
21. SpecifyClockTree          -file       name.ctstch
22. ClockDesign      -specfilename.ctstch
23. Dbget   [dbget  -p1       top.nets.shildNets.Name   VSS].name
24. Dbget   head.rules.name   // it gives extra rules from lef
25. Dbget  [dbget –p top.nets.isCTSclock 1].name
26. Dbget  top.nets.rule.name 2w2s (it give NDR(2w2s)rules)
27. editDelete  -type Signal –status {ROUTED  FIXED}  (it delet fixed nets)
28. dbget [dbget –p1 top.insts.cell.terms.type clockTerm].name   ….to get sink pins

## Routing:

1. getAttribute  -net  net_name
2. getNetWireLengthnet_name
3. describeCongestion
4. dumpCongestArea –all  file_name
5. dbget  [dbget  –p head.LibCell.isInverter 1].name
6. dbget   [dbget  –p2 [dbget-p2  top.instcell.isSequential  1]
   .instTerms.cellTerm.typeclockTerm].net.name  (it  give sequential clk nets)
7. dbget [dbquery  -area {_  _  _  _} ].box
8. get_metric       (give all detales)
9. set_analysismode  -analysisTypeonChipVariation
10. get_property  [get _property [get_clocks]  clock_network_pins]
    actual_latency_late_fall_max
11. all_fanout –from  pin_name _endpoint_only
12. report_clock_timing  -type skew
13. report_clocks –unsertainty_table
14. reOut  –speffile_name.spef   -reg_cornercorner_name
15. creatInstGroupgroup_name   -guid  box (give co-ordinats)
16. setDoAssign –buffer buf_name on
17. ecoChangeCell   -inst name  -upsize
18. report_timing  –net -from  beginingpoint  -to  endpoint  -path_typefull_clock –through
    instname
19. group_path
20. setEcoMode          -updatetiming   false/true
21. setCheckMode        -Netlist     true  -true    //default getCheckMode
22. CreateInstGroup     group_Name    -fence  x1  y1  x2  y2

23. addInstToInstGroup      group_name     instName
24. SetInstGroupPhyttier      group_Name
25. EcoAddRepeater   -cell    DLY2X1   -net   Net_Name      -relativeDisttosink     0.1 // (It place Near to sink)
26. SpecifyNetWeight<net_name><net_weight   value>
27. editSelect   -layer   {metal1   metal2}
28.

# SCAN CHAIN

specifyScanChainchain_name<chain_name>-start   i/p pin    -stop   o/p pin \\creates chain

ScanTrace //It reports start & end points & elements

ScanReorder

displayScanChain

Set_analysis_view    -setup   view_name   -hold   view_Name   -update_timing

All_constraint_modes   //get_constraint_mode

All_constrint_modes    -active

## TIMING

Report_timing   [all_registers] –to [all_registers]

Group_path    -name r2r   -from   [all_reg]   to   [all_reg]

Report_timing   -path_group   r2r

Report_timing   -path_group   r2r   -max_paths   100

Report_timing   -path_group   r2r   -max_paths   100 –nworst 10 //it gives no of worst paths

Report_timing    -path_group r2r -max_paths   10 –nWorst   10   -through    <inst_name>

Set_propagated_clock

Report_timing   -path_typefull_clock

Report_timing   -path_type   summary

Report_timing    -machine_readable

Report   -from   [all_registers] –to [all_registers]   -machine_readable> a

Report_timing  -early  //for hold

Report_timing   -collection //

Set  x  [report_timing  -from  [all_reg]  -to  [all_reg]  -collection]

Get_property   $x  path

Get_property   $x   slack  /startpoint/endpoint/arrival/setup

List_property    $x

Get_property  [all_clocks]  source

Get_property  [all_clocks]  period

Get_property  [all_clocks]  waveform

TimeDesign  -reportsonly   -help //gives all reports

First  DO:

    Report_timing   -machine_readable>file_name

    Load_timing_debug_report  filename

DRV Checks:

    Analyze_paths_by_drv      -generate_tran_file<file_name>

                              -generate_cap_file<file_name>

                              -generate_fanout_file<file_name>

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- setEndCapMode -leftTopCorner FILL4 -leftTopEdge FILL4 -leftBottomEdge FILL4 -  leftBottomCorner FILL4 -prefix end_left
- setEndCapMode -rightEdge FILL2 -leftEdge FILL2 -topEdge {FILL2 FILL32} - bottomEdge {FILL2 FILL32}
- addEndCap