ECE5014	ASIC DESIGN	L	T	P	J	C
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Pre-requisite	Nil				v 1.1	

Course Objective:

The course is aimed to

1. explain the types of ASIC and typical ASIC design Flow.
2. give the students an understanding of HDL coding guidelines and synthesizable HDL constructs.
3. explain the RTL synthesis Flow with respect to different cost function.
4. teach the various timing parameter and how to perform Static Timing Analysis for ASIC chips.
5. discuss the various abstraction levels in physical design and guidelines at each abstraction level.
6. provide detailed insight on importance of physical design verification

Expected Course Outcome :

At the end of the course the student will be able to

1. Understand different types of ASICs and design flows.
2. Design digital systems by adhering to synthesizable HDL constructs.
3. Synthesize the given design by considering various constraints and to optimize the same.
4. Understand various timing parameters and compute computation time for a givendesign using static timing analysis.
5. Perform physical design by adhering to guidelines.
6. Apprehend the importance of physical design verification.
7. Design ASIC based systems using industry standard tools.

Student Learning Outcomes (SLO): 1,17,18

Module:1	ASIC Design Methodology & Design Flow	4 hours

Implementation Strategies for Digital ICs: Custom IC Design- Cell-based Design Methodology - Array based implementation approaches - Traditional and Physical Compiler based ASIC Flow.

Module:2	Verilog HDL Coding Style for Synthesis	6 hours

HDL Coding style – Guidelines and Recommendation - FSM Coding Guideline and Coding Style for Synthesis.

Module:3	RTL Synthesis	8 hours

RTL synthesis Flow – Synthesis Design Environment & Constraints – Architecture of Logic Synthesizer - Technology Library Basics– Components of Technology Library –Synthesis Optimization- Technology independent and Technology dependent synthesis- Data path Synthesis – Low Power Synthesis – Timing driven synthesis- Formal Verification.

Module:4	Timing Parameters	5 hours

Timing Parameter Definition – Setup Timing Check- Hold Timing Check- Multicycle Paths- False Paths - Clocking of Synchronous Circuits.

Module:5	Static Timing Analysis	7 hours

Timing Analysis - Clock skew optimization – Clock Tree Synthesis.

Module:6	**Physical Design**	**8 hours**
Detailed step in Physical Design Flow- Guidelines for Floor plan, Placement and routing. Conducting layers and their characteristics - Cell-based back-end design –ECO – Packaging- Layout Issues-Preventing electrical overstress.		
Module:7	**Physical Design Verification**	**5 hours**
Static verification techniques-Post-layout design verification.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)		
1.	HimanshuBhatnagar, Advanced ASIC Chip Synthesis, Kluwer Academic Publisher, Second Edition, 2012.	
Reference Books		
1.	Erik Brunvand, Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Addison Wesley, First Edition, 2010.	
2.	J. Bhasker and RakeshChadha, Static Timing Analysis for Nanometer Designs, Springer US, First Edition, 2010.	
Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).		
List of Challenging Experiments (Indicative)		
1.	**Phase- I Design of digital architecture** Design Specification: Starting with the soda machine dispenser design described in lecture, create a block diagram and high-level state machine for a soda machine dispenser that has a choice of two soda types, and that also provides change to the consumer. A coin detector provides the circuit with a 1-bit input c that becomes 1 for one clock cycle when a coin is detected, and an 8-bit input a indicating the coin's value in cents. Two 8-bit input s1 and s2 indicate the cost of the two soda choices. The user's soda selection is controlled by two buttons b1 and b2 that when pushed will output 1 for one clock cycle. If the user has inserted enough change for their selection, the circuit should set either output bit d1 or d2 to 1 for one clock cycle, causing the selected soda to be dispensed. The soda dispenser circuit should also set an output bit cr to 1for one clock cycle if change is required, and should output the amount of change required using on an 8-bit output ca. Use the RTL design method to convert the high-level state machine to a controller and a data path. Design the data path to structure, but design the controller to the point of an FSM only.	12 hours
2.	**Phase-II Logical Synthesis of digital architecture** Apply design and timing constraints : Timing constraints: set_clock ,set_clock_uncertainty, set_clock_latency, set_clock_transition, set_input_delay, set_output_delay, set_false_path and set_multicycle_path. DRC constraints are: set_max_fanout, set_max_transition and	6 hours

	set_max_capacitance. Optimization constraints :set_max_area, set_min_area, set_max_leakegeandset_max_dynamic.	
3.	**Phase-III Netlist Optimization and Formal Verification** Apply power optimization constraints, Gate Level Simulation and Formal verification of digital architecture.	4 hours
4.	**Phase-IV Physical Synthesis of digital architecture** create_floorplan, set_propgated_clock,preroute_standard_cells, set_route_zrt.	4 hours
5.	**Phase - VPhysical Verification of digital architecture** set_fix_multiple_port_nets, write_physical_constraints and write_parasitics	4 hours
	Total Laboratory hours:	30 hours

Mode of Evaluation:Continuous assessment of challenging experiments /Final Assessment Test (FAT).			
Recommended by Board of Studies	28/02/2017		
Approved by Academic Council	47th AC	Date	05/10/2017