ECE5029	VLSI TESTING AND TESTABILITY	L	T	P	J	C
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Pre-requisite	**Nil**					**v 1.1**

Course Objective:

The course is aimed to

1. Model and simulate different types of faults in digital circuits at the gate level.
2. Establish equivalence and dominance relationships of faults in a circuit.
3. compare automatic test pattern generation algorithms with respect to search space, speed, fault coverage and other criteria.
4. Handle design complexity, ensure reliable operation, and achieve short time-to-market using various testing methodologies.

Expected Course Outcome:

After completion of the course students will be able to:

1. Model different fault models.
2. Simulate faults and generate test patterns for combinational circuits.
3. Apply scan based testing.
4. Recognize the BIST techniques for improving testability.
5. Understand boundary scan based test architectures.
6. Analyse and apply the test vector compression techniques for memory reduction and fault diagnosis.

Student Learning Outcomes (SLO): **1,17**

Module:1	**Fault Modelling**	**6hours**

Importance of Testing - Testing during the VLSI Lifecycle - Challenges in the VLSI Testing: Test Generation - Fault Models - Levels of Abstraction in VLSI Testing - Historical Review of VLSI Test Technology - Functional Versus Structural Testing - Levels of Fault Models - Fault Equivalence - Fault Dominance - Fault Collapsing - Check point Theorem - Delay Fault.

Module:2	**Fault Simulation and Test Generation**	**7hours**

Fault Simulation: Serial, Parallel, Deductive, Concurrent - Combinational Test Generations - ATPG for Combinational Circuits - D-Algorithm - Testability Analysis - SCOAP measures for Combinational Circuits

Module:3	**Scan based Testing**	**7hours**

Design for Testability Basics - Ad Hoc Approach - Structured Approach - Scan Cell Designs - Scan Architectures - Scan Design Rules - Scan Design Flow – Special Purpose Scan Designs - RTL Design for Testability.

Module:4	**Built-in Self-Test**	**7hours**

BIST Design Rules - Test Pattern Generation - Exhaustive Testing - Pseudo-Random Testing - Pseudo-Exhaustive Testing - Delay Fault Testing - Output Response Analysis - Logic BIST Architectures - BIST Architectures for Circuits with and without Scan Chains

Module:5	**Boundary scan and Core based Testing**	**5hours**
Digital Boundary Scan (IEEE Std. 1149.1): Test Architecture and Operations - On-Chip Test Support with Boundary Scan - Board and System-Level Boundary-Scan Control Architectures.		
Module:6	**Test Compression and Compaction**	**6hours**
Test Stimulus Compression: Code-Based Schemes, Linear-Decompression-Based Schemes - Test Response Compaction.		
Module:7	**Fault Diagnosis**	**5hours**
Dictionary Based and Adaptive fault diagnosis.		
Module:8	**Contemporary issues:**	**2hours**
	Total Lecture hours:	**45hours**

Text Book(s)

1.	Z.Navabi, Digital System Test and Testable Design, Springer, 2011.

1.	Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, VLSI Test Principles and Architectures, The Morgan Kaufmann, 2013.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

Recommended by Board of Studies	28/02/2017		
Approved by Academic Council	47th AC	Date	05/10/2017