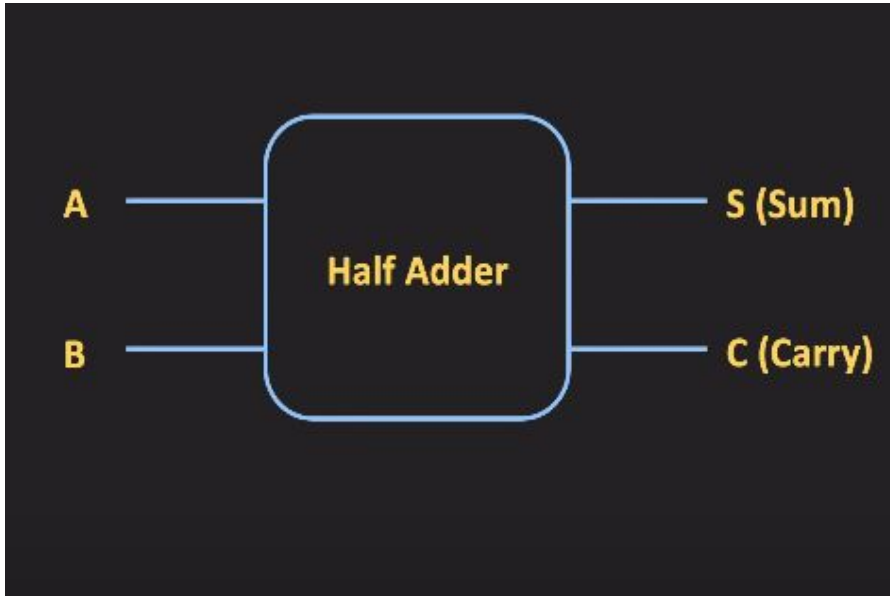
Half Adder, Full Adder, Ripple Carry adder

Silicon Community - Varun Kouda

Half Adder - Truth table



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

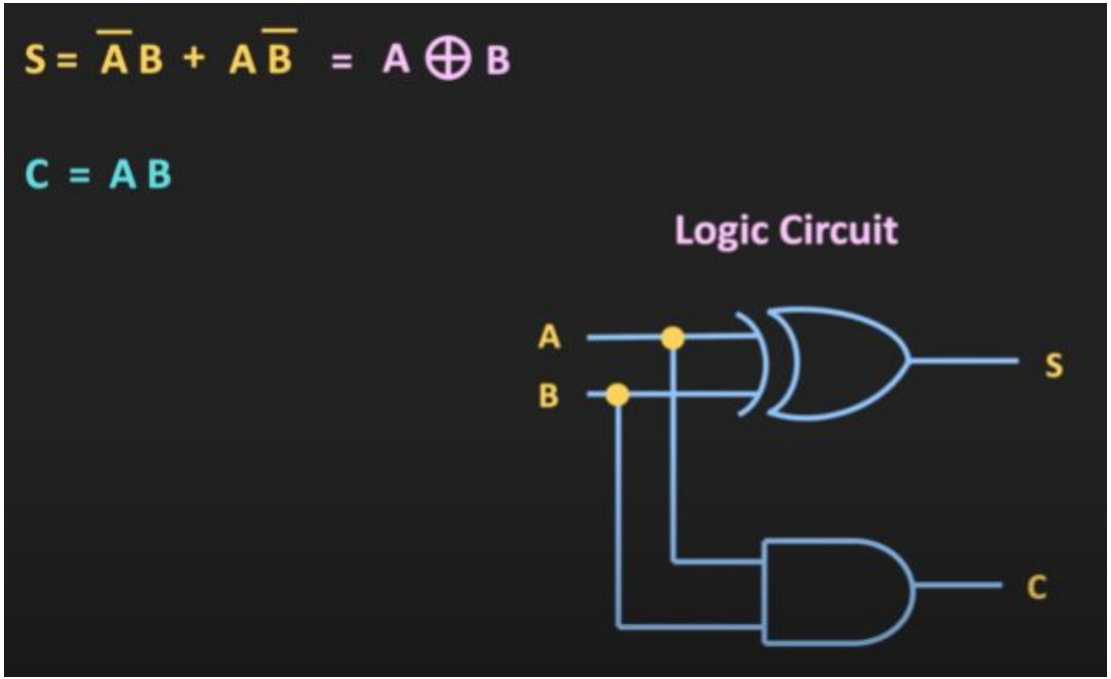
Half Adder - Boolean expression

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

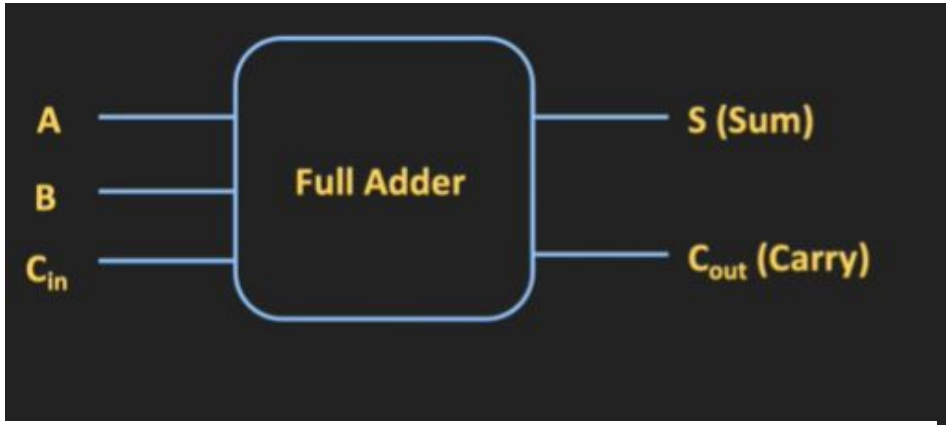
$$S = \overline{A}B + A\overline{B} = A \oplus B$$

$$C = AB$$

Half Adder - Digital Circuit Diagram



Full Adder - Truth Table

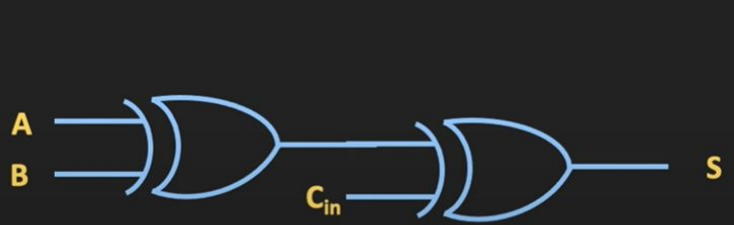


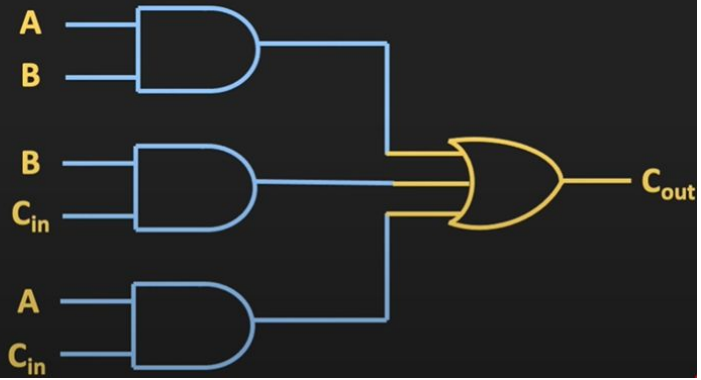
A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder - Boolean expression

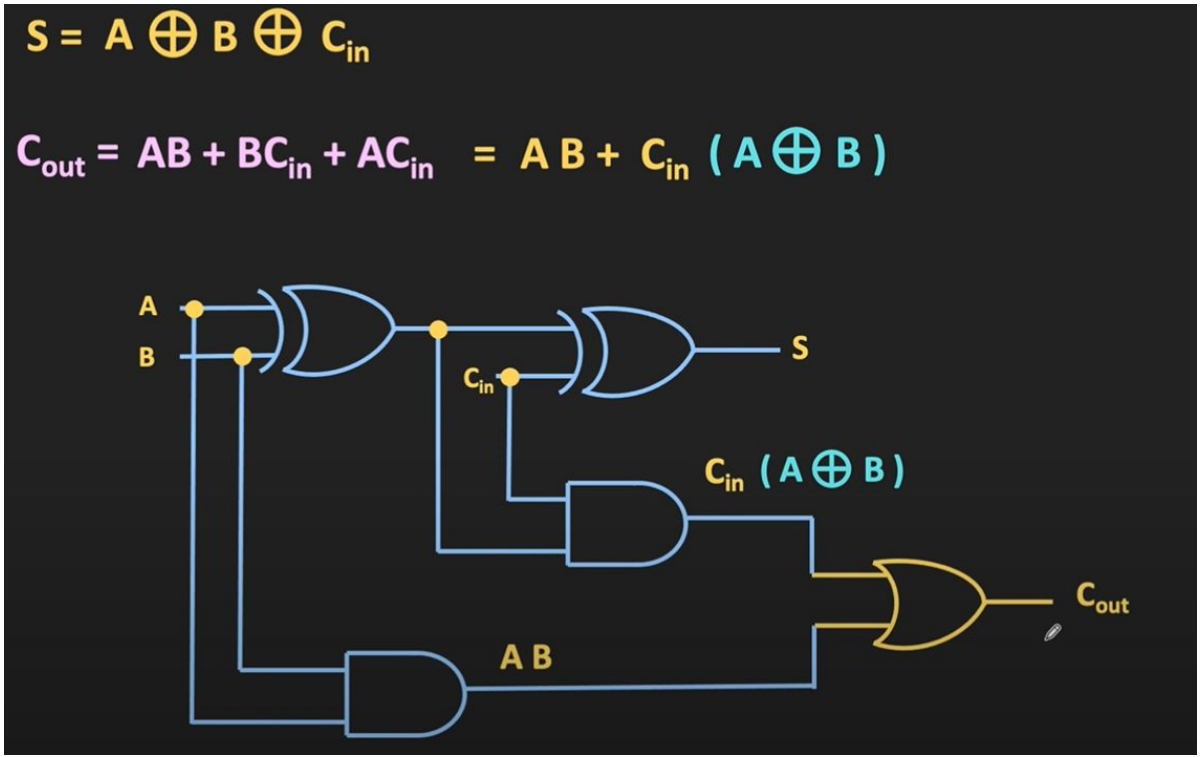
$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = AB + BC_{in} + AC_{in} = AB + C_{in}(A \oplus B)$$

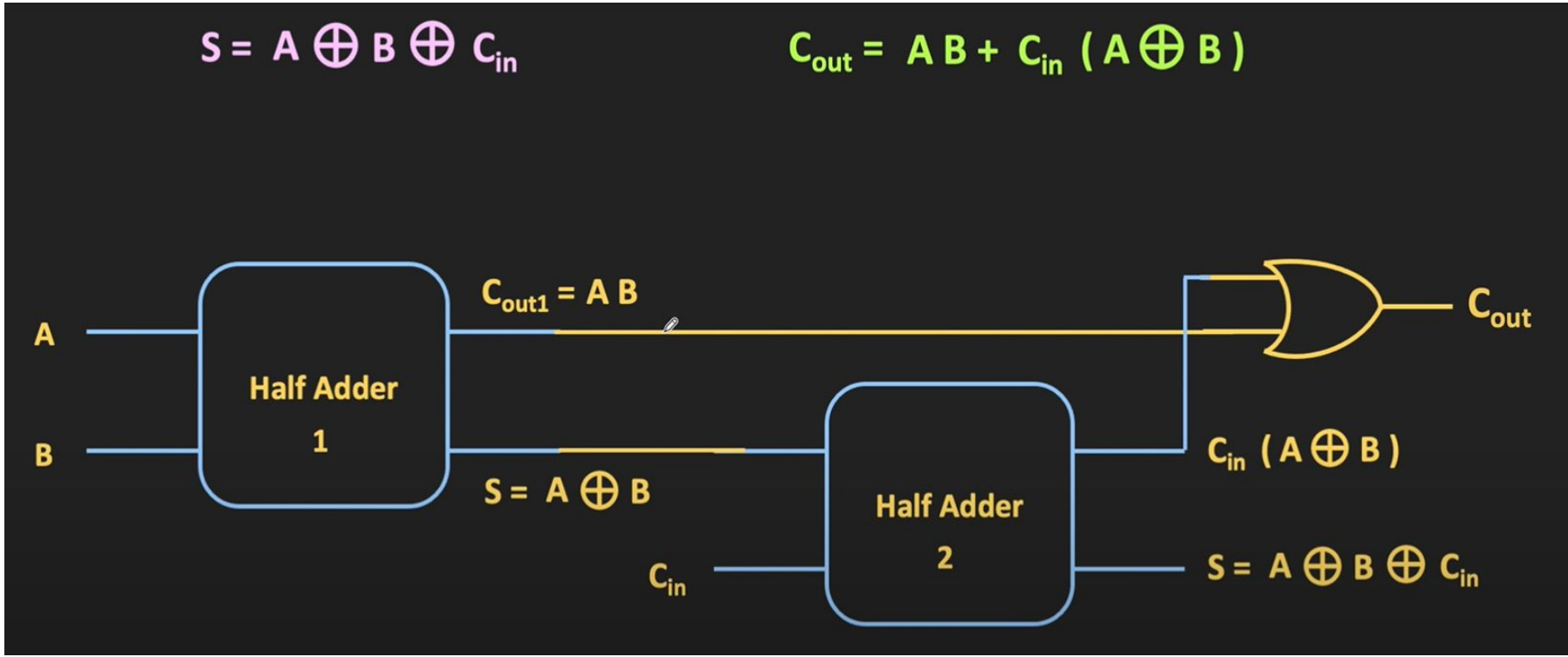




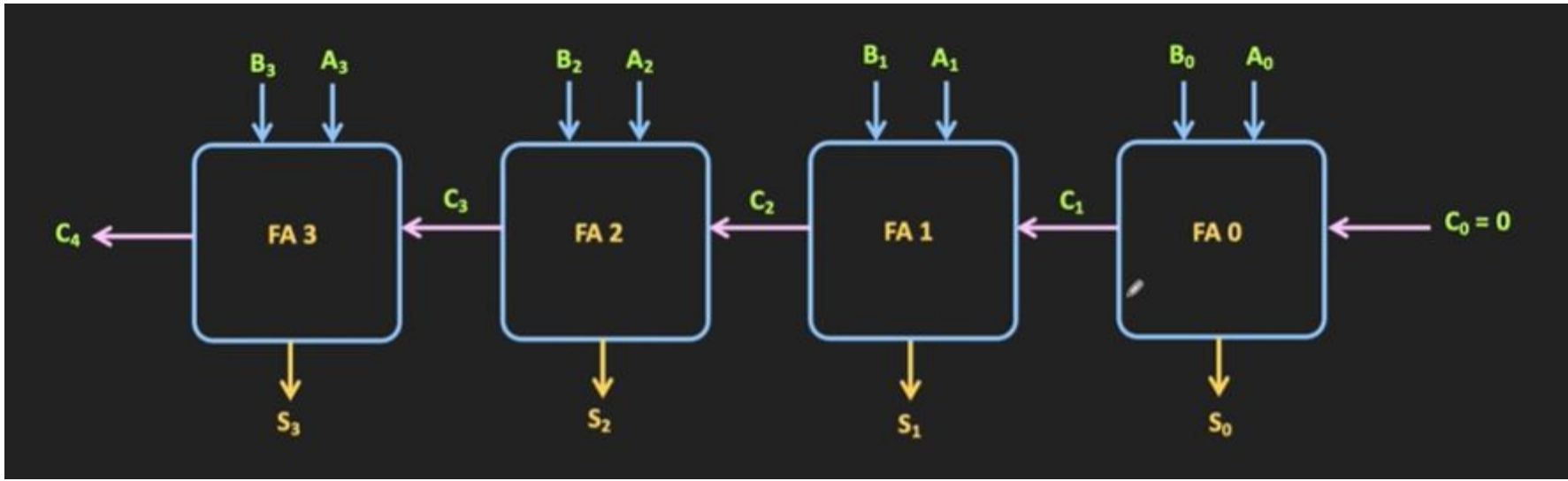
Full Adder - Digital Circuit diagram



Full Adder using Half Adder



Ripple Carry Adder (4 - bit)

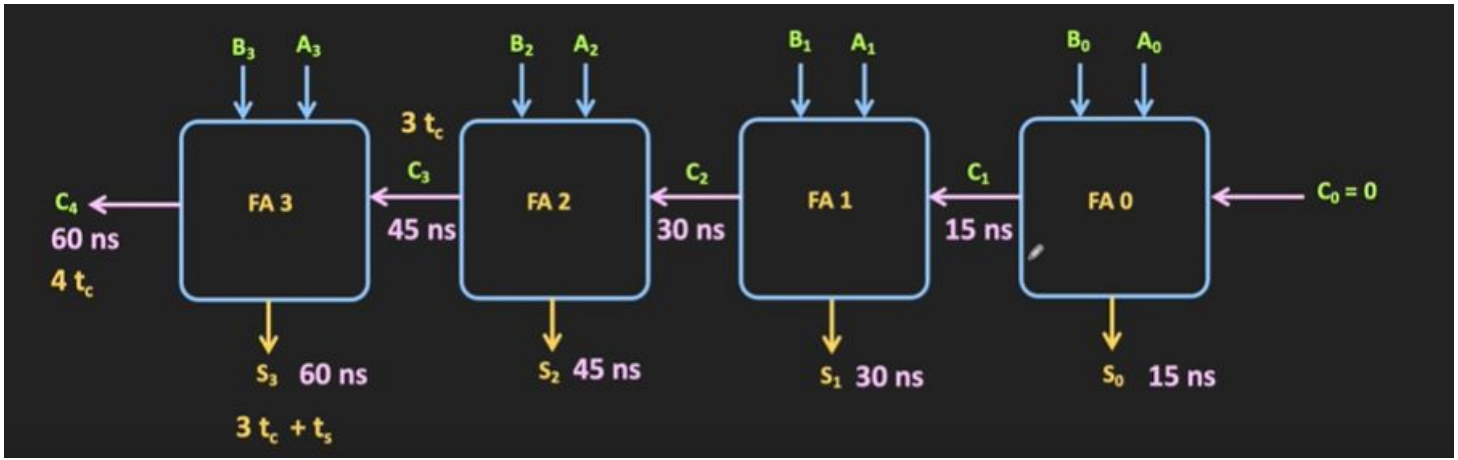


S0, S1, S2 and S3 are the Sums of 4 bit adder
C1, C2, C3 and C4 are carry forwards of 4 bit adder

Ripple Carry Adder - disadvantage

Let us suppose propagation delay for sum is T(s)
And propagation delay of Carry is T(c)

Let T(s) = 15ns and T(c) = 15ns



Ripple Carry Adder - Disadvantage

For 4 bit adder
Delay for sum = 3T(s) + 4T(c)
Delay for carry = 4T(c)

For n bit adder
Delay for sum = (n-1)T(s) + nT(c)
Delay for carry = nT(c)

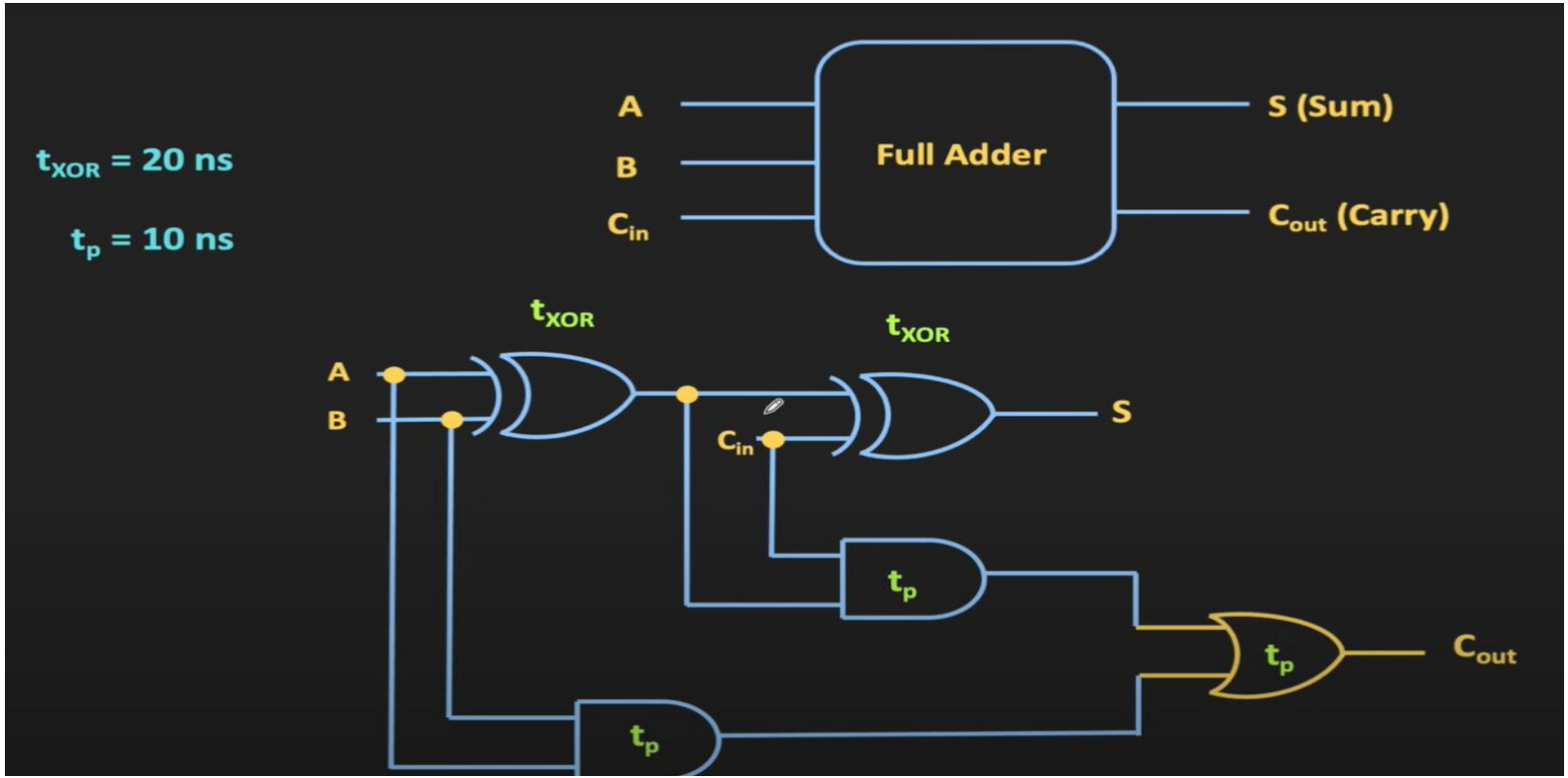
So, ripple carry adder has this delay for giving the results out

Ripple Carry Adder - Example

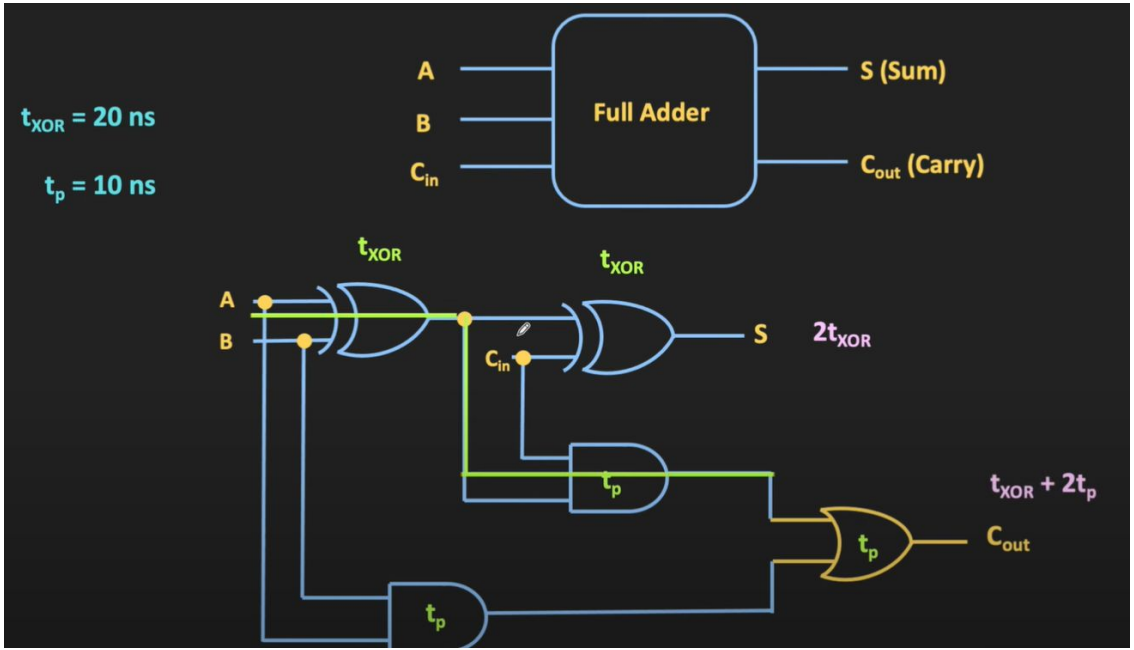
In the Previous slide, we have seen total propagation delay for sum and carry of ripple carry adder when given propagation delay of sum and carry of each full adder

Now, here we will see the propagation delay for sum and carry of n bit ripple carry adder if propagation delay of XOR gate is T(xor) and propagation delay of AND and OR gate is T(p)

Prop delay of Ripple Carry Adder with gate delays (1)



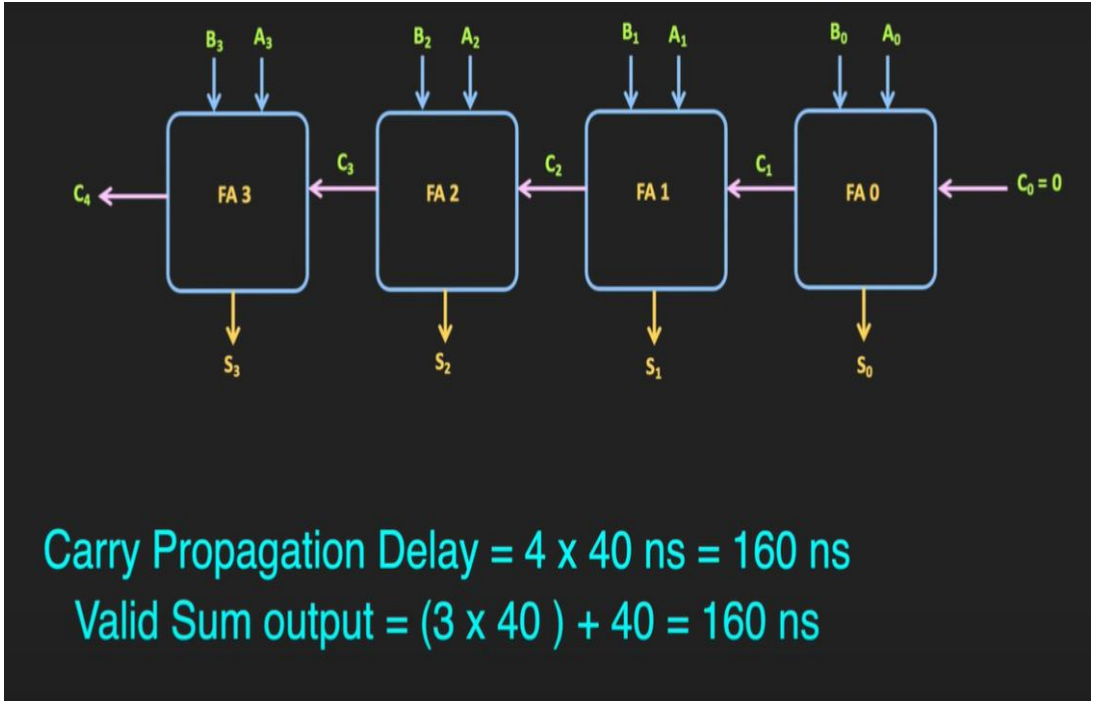
Prop delay of Ripple Carry Adder with gate delays (2)



Propagation delay for sum given T(xor) and T(p) is **2T(xor)**

Propagation delay for Carry given T(xor) and T(p) is **T(xor) + 2T(p)**

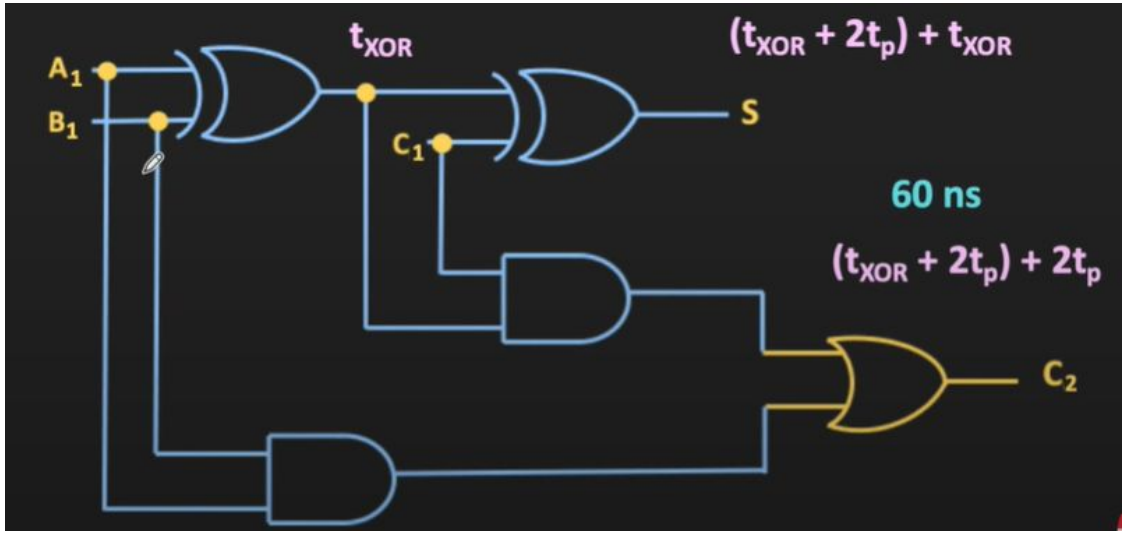
Prop delay of Ripple Carry Adder with gate delays (3)



By applying the formula we derived earlier, the worst case delay for sum and carry is 160ns

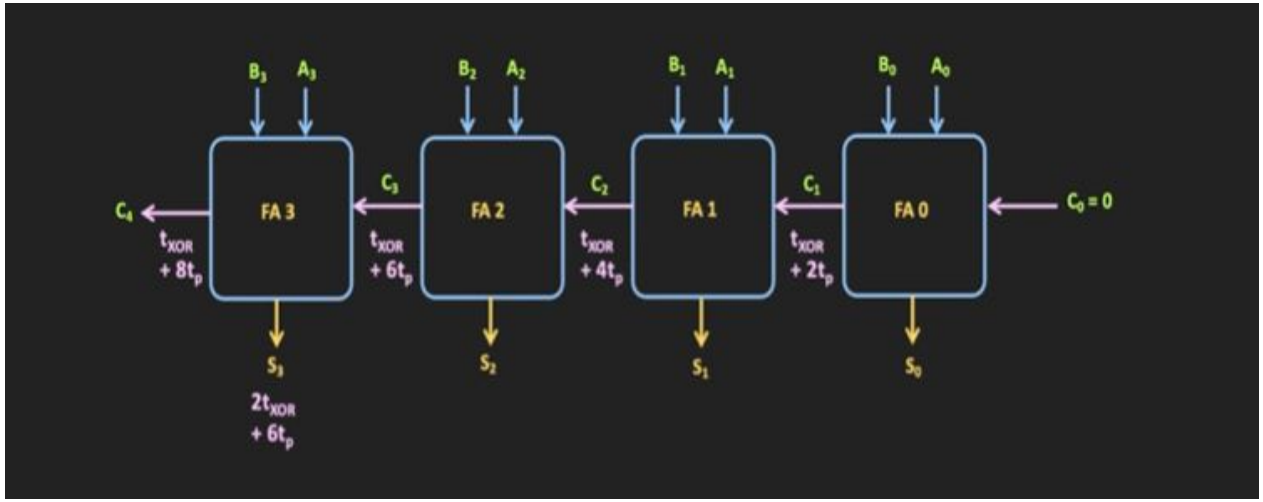
But as we know the internal circuitry now and propagation delay of the logic gates, we can find the propagation delay of sum and carry even more accurately

Prop delay of Ripple Carry Adder with gate delays(4)



Calculation of S1:
Delay for 1st XOR gate is T(xor)
For the second XOR gate, It needs C1 as input and it takes T(xor) + 2T(P)
Hence total time taken for S1 is (2T(xor) + 2T(p))
Calculation of C1:
T(xor) + 4T(p)

Prop delay of Ripple Carry Adder with gate delays(4)



So, applying the same to all the Sums and Carry of Ripple carry adder

S3 = 2T(XOR) + 6T(P)

C4 = T(xor) + 8T(P)

For n bit Ripple Carry adder

Stable Carry output C_{n+1} is available after $t_{XOR} + 2n\ t_p$

Stable Sum output S_n is available after $2t_{XOR} + 2\ (n-1)$