

DIGITAL CIRCUIT

Objective Paper –“Topic wise Updated up to GATE-2019 & IES-2015”

(VERSION : 24|05|19)

GATE / IES

For “Electrical”, “Elect. & Comm.” And "Instrumentation" Engg.



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SYLLABUS: ENGG. DIGITAL ELEX

GATE-2019

ELECTRONICS AND COMMUNICATION ENGINEERING (EC)

Number systems; Combinatorial circuits: Boolean algebra, minimization of functions using Boolean identities and Karnaugh map, logic gates and their static CMOS implementations, arithmetic circuits, code converters, multiplexers, decoders and PLAs; Sequential circuits: latches and flip-flops, counters, shift registers and finite state machines; Data converters: sample and hold circuits, ADCs and DACs; Semiconductor memories: ROM, SRAM, DRAM; 8-bit microprocessor (8085): architecture, programming, memory and I/O interfacing.

ELECTRICAL ENGINEERING (EE)

Combinational and Sequential logic circuits, Multiplexer, Demultiplexer, Schmitt trigger, Sample and hold circuits, A/D and D/A converters, 8085Microprocessor: Architecture, Programming and Interfacing.

IES-2019

ELECTRONICS AND TELECOMMUNICATION ENGINEERING

Transistor as a switching element; Boolean algebra, simplification of Boolean functions, Karnaguh map and applications; IC Logic gates and their characteristics; IC logic families : DTL, TTL, ECL, NMOS, PMOS and CMOS gates and their comparison; Combinational logic Circuits; Half adder, Full adder; Digital comparator; Multiplexer Demulti-plexer; ROM an their applications. Flip flops. R-S, J-K, D and T flip-flops; Different types of counters and registers Waveform generators. A/D and D/A converters. Semiconductor memories.

ELECTRICAL ENGINEERING

Digital logic gate families, universal gates-combination circuits for arithmetic and logic operational, equential logic circuits. Counters, registers, RAM and ROMs.

Table of Contents

1. Number System	1
1.1 (r)'s and (r-1)'s Comp.	1
1.2 Miscellaneous	4
2. Boolean Algebra	9
3. Logic GATES	24
4. Combinational Digital Circuits	40
4.1 Multiplexer	40
4.2 Adder	49
4.3 Decoder	53
4.4 Miscellaneous	55
5. Sequential Digital Circuits	59
5.1 Counter	59
5.2 Miscellaneous	74
6. Semiconductor Memories	90
7. Logic Gate Families	95
8. A/D & D/A Converters	111
9. MICROPROCESSOR 8085 PROGRAMMING & BASICS	122
10. MEMORIES & INTERFACING	134
Answers :	138

01

Number System

1.1 (r)'s and (r-1)'s Comp.

[IES - EC - 1992]

- (1) Which of the following number systems has two 0's?

 - (A) Sign plus magnitude
 - (B) 1's complement
 - (C) 2's complement
 - (D) None of the above

[IES – EC – 1993]

- (2) When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero?

 - (A) Sign- magnitude
 - (B) 1's complements
 - (C) 2's complements
 - (D) 9's complements

[IES - EC - 1995]

- (3) Two's complement of a given 3 or more bit binary number of non-zero magnitude is the same as the original number if :

 - (A) MSB is zero
 - (B) LSB is zero
 - (C) MSB is one
 - (D) LSB is one

[IES - EE - 2005]

- (4) Which of the following notations have two representations of zero ?

 1. 1's complement with radix of number being 2
 2. 7's complement with radix of number being 8
 3. 9's complement with radix of number being 10
 4. 10's complement with radix of number being 10

Select the correct answer using the code given below.

- (A)** 1, 2 and 4 **(B)** 1 and 3
(C) 2, 3 and 4 **(D)** 1, 2 and 3

[GATE -EC - 1987]

- (5) The subtraction of a binary number Y from another binary number X, done by adding the 2's complement of Y to X, results in a binary number without overflow. This implies that the result is:

 - (A) negative and is in normal form.
 - (B) negative and is in 2's complement form.
 - (C) positive and is in normal form.
 - (D) positive and is in 2's complement form.

[GATE - IN - 2003]

- (6)** Two 4-bit 2's complement numbers 1011 and 0110 are added. The result expressed in 4-bit 2's complement notation is

(A) 0001
(B) 0010
(C) 1101
(D) cannot be expressed in 4-bit 2's complement

[GATE -EC - 2004]

- (7) 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following gets of number?

(A) 25, 9 and 57 respectively

(B) -6, -6 and -6 respectively

(C) -7, -7 and -7 respectively

(D) -25, -9 and -57 respectively

[GATE -EC - 1998]

- (8) An equivalent 2's complement representation of the 2's complement number 1101 is

(A) 110100 (B) 001101
(C) 110111 (D) 111101

[GATE -EC - 2002]

[GATE-EC-2008]

- (22) The two numbers represented in signed 2's complement form are

P = 11101101 and Q = 11100110. If Q is subtracted from P, the value obtained in signed 2's complement form is

- (A) 100000111
- (B) 00000111
- (C) 11111001
- (D) 111111001

[GATE-EC-2001]

- (23) The 2's complements representation of -17 is

- (A) 101110
- (B) 101111
- (C) 111110
- (D) 110001

[GATE – IN – 2018]

- (24) The representation of the decimal number $(27.625)_{10}$ in base-2 number system is

- (A) 11011.110
- (B) 11101.101
- (C) 11011.101
- (D) 10111.110



1.2 Miscellaneous

[GATE-EE-2014]

- (1) Which of the following is an invalid state in an 8-4-2-1 Binary Coded Decimal counter
 (A) 1 0 0 0 (B) 1 0 0 1
 (C) 0 0 1 1 (D) 1 1 0 0
- [GATE-EC-2006]
- (2) A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example, the base-5 number 24 will be represented by its BCP code 010100. In this numbering system, the BCP code 100010011001 corresponds to the following number in base-5 system
 (A) 423 (B) 1324
 (C) 2201 (D) 4231

[GATE-IN-2004]

- (3) 7EH and 5FH are XORed. The output is multiplied by 10H. The result is :
 (A) 0210H (B) 7E5FH
 (C) 5F7EH (D) 2100H
- [GATE-EC-2004]
- (4) A digital system is required to amplify a binary-enclosed audio signal. The user should be able to control the gain of the amplifier from a minimum to a maximum in 100 increments. The minimum number of bits required to encode, in straight binary, is
 (A) 8 (B) 6
 (C) 5 (D) 7

[GATE - EC - 2014]

- (5) The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary coded decimal) form is ----- --.

[IES - EE - 1992]

- (6) Match List-I with List-II and select the correct answer by using the Codes given below the lists:

List - I	List - II
(Hexadecimal)	(Octal)
A. 68	1. 150
B. 8C	2. 214
C. 4F	3. 117
D. 5D	4. 135

Codes:

	A	B	C	D
(A)	3	2	4	1
(B)	2	3	1	4
(C)	1	2	3	4
(D)	3	1	2	4

[IES - EE - 1992]

- (7) Which of the following hexagonal sum is equivalent to hexadecimal A8H?
 (A) 2CH + 4FH
 (B) 5EH + 1AH
 (C) 3BH + 6DH
 (D) 5AH + 2CH

[IES - EE - 1992]

- (8) Match List - I with List - II and select the correct answer by using the codes given below the lists:

List-I	List-II
(Octal)	(Binary)
A. 75	1. 010110
B. 65	2. 110101
C. 37	3. 111101
D. 26	4. 011111

Codes:

	A	B	C	D
(A)	3	1	4	2
(B)	3	2	4	1
(C)	1	2	3	4
(D)	4	1	2	3

[IES - EE - 1995]

- (9) Match List I with List II and select the correct answer using the codes given below the lists:

List I	List II
(Binary)	(Decimal)
A. 10101010	1. 128
B. 11110000	2. 240
C. 10001000	3. 170
D. 10000000	4. 136

Codes:

	A	B	C	D
(A)	3	2	4	1
(B)	2	3	1	4

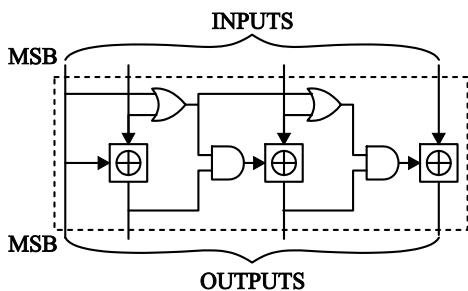
- (C) 2 4 1 3
 (D) 3 1 2 4

[IES – EE – 1995]

- (10) The decimal equivalent of the hexadecimal number $(BAD)_{16}$ is
 (A) 111013 (B) 5929
 (C) 3416 (D) 2989

[GATE -EC -2003]

- (11) The circuit shown in the figure converts



- (A) BCD to Binary code
 (B) Binary to excess-3code
 (C) Excess-3 to Gray code
 (D) Gray to Binary code.

[IES – EE – 1998]

- (12) Which one of the following is a non-valid BCD code?
 (A) 0111 1001 (B) 0101 1011
 (C) 0100 1000 (D) 0100 1001

[IES – EE – 1999]

- (13) A four-bit BCD (DCBA) for numeral 9 can be decoded most economically by the logic operation
 (A) AD (B) $A\bar{B}D$
 (C) $A\bar{C}D$ (D) $A\bar{B}\bar{C}D$

[GATE -EC - 1990]

- (14) The minimal function that can detect a “divisible by 3” 8421 BCD code digit (representation is $D_8 D_4 D_2 D_1$) is given by:
 (A) $D_8 D_1 + D_4 D_2 + \overline{D_8} D_2 D_1$
 (B) $D_8 D_1 + D_4 D_2 \overline{D_1} + \overline{D_4} D_2 D_1$
 $+ \overline{D_8} \overline{D_4} D_2 \overline{D_1}$
 (C) $D_8 D_1 + D_4 D_2 + \overline{D_8} \overline{D_4} D_2 D_1$
 (D) $D_4 D_2 \overline{D}_1 + D_4 D_2 D_1 + D_8 \overline{D_4} D_2 D_1$

[IES – EE – 2002]

- (15) The decimal equivalent of hexadecimal number 2 A 0 F is :
 (A) 17670 (B) 17607
 (C) 17067 (D) 10767

[IES – EE – 2003]

- (16) The binary representation 100110 is numerically equivalent to the
 1. Decimal representation 46
 2. Octal representation 46
 3. Hexadecimal representation 26
 4. Excess-3 representation 13

Select the correct answer using the codes given below:

- (A) 1 and 2 (B) 2 and 3
 (C) 1 and 3 (D) 2 and 4

[IES – EE – 2004]

- (17) What are the values respectively of R_1 and R_2 in the expression

$$(235)_{R1} = (565)_{10} = (1065)_{R2}$$

- (A) 8, 16 (B) 16, 8
 (C) 6, 16 (D) 12, 8

[IES – EC – 1991]

- (18) Which of the following is incorrect?

- (A) $(11100)_2 - (10001)_2 = -(00101)_2$
 (B) $(15E)_{16} = (350)_{10}$
 (C) $(81)_{10} = (1010001)_2$
 (D) $(37.4)_8 = (011111.100)_2$

[IES – EC – 1991]

- (19) Consider the bit pattern 01010001. Which of the following has Hamming distance of exactly 2 from these patterns?

- (A) 01010000 (B) 01010010
 (C) 01010011 (D) 01010110

[IES – EC – 1992]

- (20) If two numbers in excess – 3 code are added and the result is less than 9, then to get equivalent binary

- (A) 0011 is subtracted
 (B) 0011 is added
 (C) 0110 is subtracted
 (D) 0110 is added

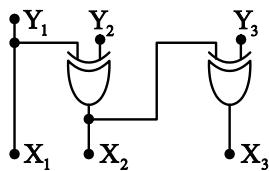
[IES – EC – 1992]

- (21) A 7 bit Hamming code (Even parity checker) 0001001 for a BCD digit is known to have error. The BCD encoded digit is

- (A) 9 (B) 5
 (C) 3 (D) 0

[IES – EC – 1993]

- (22) The logic circuit given below converts a Gray code $Y_1 Y_2 Y_3$ into



- (A) Excess – 3 code
- (B) Binary code
- (C) BCD code
- (D) Hamming code

[IES – EC – 1995]

- (23) In hexadecimal system, $7716 - 3B16$ is equal to

- (A) 3C00
- (B) 6016
- (C) 3C16
- (D) 7316

[IES – EC – 1998]

- (24) Match List – I with List – II and select the correct answer using the codes given below the Lists

List – I

- (A) 45
- (B) 90
- (C) 180
- (D) 210

List – II

1. 1 0 1 1 0 1 0 0
2. 1 1 0 1 0 0 1 0
3. 0 1 0 1 1 0 1 0
4. 0 0 1 0 1 1 0 1
5. 1 0 1 0 1 0 0 0

Codes :

A	B	C	D
(A) 3	4	5	2
(B) 4	3	1	2
(C) 4	3	5	2
(D) 3	4	2	1

[IES – EC – 2000]

- (25) The decimal equivalent of the number $(11C)_{17}$ is

- (A) 183
- (B) 318
- (C) 268
- (D) 269

[IES – EC – 2001]

- (26) The number of digit 1 present in the binary representation of

$3 \times 512 + 7 \times 64 + 5 \times 8 + 3$ is

- (A) 8
- (B) 9
- (C) 10
- (D) 12

[IES – EC – 2005]

- (27) A Gray code is a/an
- (A) Binary weighted Code
 - (B) Arithmetic code
 - (C) Code which exhibits a single bit change between two successive codes
 - (D) Alphanumeric code

[IES – EC – 2005/2014]

- (28) Given $(135)_{\text{base}_x} + (144)_{\text{base}_x} = (323)_{\text{base}_x}$. What is the value of base x ?
- (A) 5
 - (B) 3
 - (C) 12
 - (D) 6

[IES – EC – 2006]

- (29) What is the Gray code word for the binary 101011 ?
- (A) 101011
 - (B) 110101
 - (C) 011111
 - (D) 111110

[IES – EC – 2006]

- (30) Which of the following subtraction operations results in F_{16} ?
1. $(BA)_{16} - (AB)_{16}$
 2. $(BA)_{16} - (CB)_{16}$
 3. $(CB)_{16} - (BC)_{16}$
- Select the correct answer using the code given below:

- (A) Only 1 and 2
- (B) Only 1 and 3
- (C) Only 2 and 3
- (D) 1, 2 and 3

[IES – EC – 2008]

- (31) $(24)_8$ is expressed in Gray code as which one of the following ?
- (A) 11000
 - (B) 10100
 - (C) 11110
 - (D) 11111

[IES – EC – 2010]

- (32) The hexadecimal representation of 657_8 is :
- (A) 1 AF H
 - (B) D 78 H
 - (C) D 71 H
 - (D) 32 F H

[IES – EC – 2011]

- (33) If 73_x (in base x number system) is equal to 54_y (in base y number system), the possible values of x and y are :

- | | |
|---|---|
| <p>(A) 8 and 16 (B) 10 and 12
 (C) 9 and 13 (D) 8 and 11</p> <p style="text-align: center;">[IES – EC – 2012]</p> <p>(34) If $(11X1Y)_8 = (12C9)_{16}$ then the value X and Y are
 (A) 3 and 1 (B) 5 and 7
 (C) 7 and 5 (D) 1 and 5</p> <p style="text-align: center;">[GATE - IN - 1999]</p> <p>(35) For a shaft encoder, the most appropriate 2 – bit code is
 (A) 11,10,01,00 (B) 11,10,00,01
 (C) 01,10,11,00 (D) 01,00,11,10</p> <p style="text-align: center;">[GATE - IN - 2011]</p> <p>(36) The base of the number system for the addition operation $24 + 14 = 41$ to be true is
 (A) 8 (B) 7
 (C) 6 (D) 5</p> <p style="text-align: center;">[GATE - IN - 1992]</p> <p>(37) The most suitable coding scheme for coding the successive positions in an 8 position digital shaft encoder is
 (A) 00,001,010,011,100,101,110,111
 (B) 00,010,100,110,001,011,101,111
 (C) 00,001,011,010,110,111,101,111
 (D) 00,001,100,101,010,011,110,111</p> <p style="text-align: center;">[GATE - EE - 2007]</p> <p>(38) The octal equivalent of the HEX number AB.CD is
 (A) 253.314 (B) 253.632
 (C) 526.314 (D) 526.632</p> <p style="text-align: center;">[IES – EC – 2015]</p> <p>(39) Given $(125)_R = (203)_5$ the value of radix R will be
 (A) 16 (B) 10
 (C) 8 (D) 6</p> <p style="text-align: center;">[IES – EC – 1992]</p> <p>(40) Which of the following is error correcting code?
 (A) EBCDIC (B) GRAY
 (C) Hamming (D) ASCII</p> <p style="text-align: center;">[GATE -EC - 2000]</p> <p>(41) $(FE35)_{16}$ XOR $(CB15)_{16}$ is equal to
 (A) $(3320)_{16}$ (B) $(FE35)_{16}$
 (C) $(FE50)_{16}$ (D) $(3520)_{16}$</p> | <p style="text-align: right;">[GATE -EC - 2002]</p> <p>(42) Which of the following represent '$E3_{16}$'?
 (A) $(CE)_{16} + (A2)_{16}$
 (B) $(1BC)_{16} - (DE)_{16}$
 (C) $(2BC)_{16} - (1DE)_{16}$
 (D) $(200)_{16} - (11D)_{16}$</p> <p style="text-align: right;">[GATE - EC - 2007]</p> <p>(43) What is the addition of $(-64)_{10}$ and $(80)_{16}$?
 (A) $(-16)_{10}$
 (B) $(16)_{10}$
 (C) $(1100000)_2$
 (D) $(01000000)_2$</p> <p style="text-align: right;">[GATE -EC - 2005]</p> <p>(44) If $(2.3)_{\text{base}4} + (1.2)_{\text{base}4} = (Y)_{\text{base}4}$; What is the value of Y ?
 (A) 10.1 (B) 10.01
 (C) 10.2 (D) 1.02</p> <p style="text-align: right;">[IES – EC – 2012]</p> <p>(45) Binary data is being represented in size of byte and in 2's complement form. The number of 0's present in representation of (-127) DECIMAL IS
 (A) 8 (B) 7
 (C) 6 (D) 5</p> <p style="text-align: right;">[GATE - IN - 2006]</p> <p>(46) The binary representation of the decimal number 1.375 is
 (A) 1.111 (B) 1.010
 (C) 1.011 (D) 1.001</p> <p style="text-align: right;">[GATE – EC – 1993]</p> <p>(47) 2's complement representation of a 16-bit number (one sign bit and 15 magnitude bits) if FFFF. Its magnitude in decimal representation is :
 (A) 0 (B) 1
 (C) 32,767 (D) 65,535</p> <p style="text-align: right;">[IES -EC - 2006]</p> <p>(48) The greatest negative number which can be stored in a computer that has 8 – bit word length and uses 2 complement arithmetic is
 (A) -256 (B) -255
 (C) -128 (D) -127</p> |
|---|---|

[GATE -EC - 2002]

- (49) In signed magnitude representation, the binary equivalent of 22.5625 is (the bit before comma represents the sign)
- (A) 0, 10110.1011
(B) 0, 10110.1001
(C) 1, 10101.1001
(D) 1, 10110.1001

[GATE -EC - 2007]

- (50) Which one of the following is the correct sequence of the numbers represented in the series given below ?
- $(2)_3, (10)_4, (11)_5, (14)_6, (22)_7, \dots$
- (A) 2, 3, 4, 5, 6 ...
(B) 2, 4, 6, 8, 10,
(C) 2, 4, 6, 10, 12, ...
(D) 2, 4, 6, 10, 16,

[GATE – EC – 2005]

- (51) Decimal 43 in Hexadecimal and BCD number system is respectively.
- (A) B2, 0100 0011
(B) 2B, 0100 0011
(C) 2B, 0011 0100
(D) B2, 0100 0100

-----0000-----

T A R G A T E

02

Boolean Algebra

[GATE - EC - 2014]

- (1) For an n-variable Boolean function the maximum number of prime implicants is
 (A) $2(n-1)$ (B) n^2
 (C) 2^n (D) $2^{(n-1)}$

[IES - EC - 2007]

- (2) Consider the following statements :
 1. Minimization using Karnaugh map may not provide unique solution.
 2. Redundant grouping in Karnaugh map may result in non-minimized solution.
 3. Don't care states if used in Karnaugh map for minimization, the minimal solution is not obtained.

Which of the statements given above are correct ?

- (A) 1, 2 and 3
 (B) 2 and 3 only
 (C) 1 and 3 only
 (D) 1 and 2 only

[GATE-IN-2003]

- (3) The Karnaugh map for a four variable Boolean function is given in below figure. The correct Boolean sum of product is

		PQ	00	01	11	10
		RS	00	0	0	0
		01	1	0	0	1
		11	1	0	0	1
		10	0	1	0	0

- (A) $PQRS + \bar{Q}S$
 (B) $\bar{P}Q\bar{R}\bar{S} + \bar{Q}S$
 (C) $PQR + Q\bar{S}$
 (D) $PQRS + \bar{Q}$

[GATE-IN-1994]

- (4) Any Boolean function can be realized using only NAND gates. (True/False)

[GATE - EC - 2007]

- (5) The Boolean expression

$$Y = \overline{ABC}D + \overline{AB}\overline{CD} + A\overline{BC}\overline{D} + AB\overline{CD}$$

can be minimized to

- (A) $Y = \overline{ABC}D + \overline{ABC} + A\overline{CD}$
 (B) $Y = \overline{ABC}D + BC\overline{D} + A\overline{BC}\overline{D}$
 (C) $Y = \overline{ABC}\overline{D} + \overline{BC}\overline{D} + A\overline{BC}\overline{D}$
 (D) $Y = \overline{ABC}\overline{D} + \overline{BC}\overline{D} + AB\overline{CD}$

[GATE-EC-2015]

- (6) The Boolean expression

$$F(X, Y, Z) = \bar{X}\bar{Y}\bar{Z} + X\bar{Y}\bar{Z} + X\bar{Y}\bar{Z} + XY\bar{Z}$$

Converted into canonical product of sum (POS) form is :

- (A) $(X+Y+Z)(X+Y+\bar{Z})$
 $(X+\bar{Y}+\bar{Z})(\bar{X}+Y+\bar{Z})$
 (B) $(X+\bar{Y}+Z)(\bar{X}+Y+\bar{Z})$
 $(\bar{X}+\bar{Y}+Z)(\bar{X}+\bar{Y}+\bar{Z})$
 (C) $(X+Y+Z)(\bar{X}+Y+\bar{Z})$
 $(X+\bar{Y}+Z)(\bar{X}+\bar{Y}+\bar{Z})$
 (D) $(X+\bar{Y}+\bar{Z})(\bar{X}+Y+Z)$
 $(\bar{X}+\bar{Y}+Z)(X+Y+Z)$

[GATE-EC-2015]

- (7) A function of Boolean variables, X, Y and Z is expressed in terms of the main-terms as $F(X, Y, Z) = \Sigma(1, 2, 5, 6, 7)$

Which one of the product of sums given below is equal to the function $F(X, Y, Z)$?

- (A) $(\bar{X}+\bar{Y}+\bar{Z}) \cdot (\bar{X}+Y+Z) \cdot (X+\bar{Y}+\bar{Z})$
 (B) $(X+Y+Z) \cdot (X+\bar{Y}+\bar{Z}) \cdot (\bar{X}+Y+Z)$

- (C) $(\bar{X} + \bar{Y} + Z) \cdot (\bar{X} + Y + \bar{Z}) \cdot (X + \bar{Y} + Z) \cdot (X + Y + \bar{Z}) \cdot (X + Y + Z)$

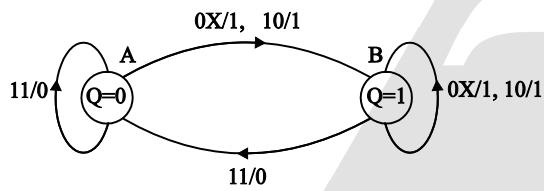
(D) $(X + Y + \bar{Z}) \cdot (\bar{X} + Y + Z) \cdot (\bar{X} + Y + \bar{Z}) \cdot (\bar{X} + \bar{Y} + Z) \cdot (\bar{X} + \bar{Y} + \bar{Z})$

[GATE -EC - 2003]

[GATE -EC - 1990]

[GATE-EE-2014]

- (10) A state diagram of a logic gate which exhibits a delay in the output is shown in the figure, where X is the don't care condition, and Q is the output representing the state.



The logic gate represented by the state diagram is

[IES – EC – 1998]

- (11) While obtaining minimal sum of products expression

 - (A) All don't cares are ignored
 - (B) All don't cares are treated as logic ones
 - (C) All don't cares are treated as logic zeros
 - (D) Only such don't cares that aid minimization are treated as logic ones

[IES – EC – 2009]

- (12)** What are the ultimate purposes of minimizing logic expressions?

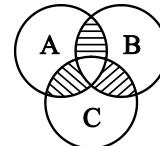
 1. To get a small size expression.
 2. To reduce the number of variables in the given expression.
 3. To implement the function of the logic expression with least hardware.

4. To reduce the expression for making it feasible for hardware implementation.

Select the correct answer from the codes given below:

[IES – EC – 1992]

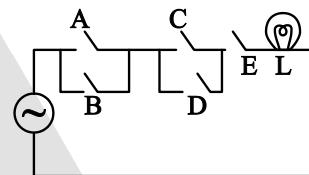
- (13) The expression for shaded area shown below is :



- (A) $A B + B C$
(B) $\overline{ABC} + A\overline{BC}$
(C) $AB\overline{C} + \overline{ABC} + A\overline{BC}$
(D) None of the above

[IES – EE – 1995]

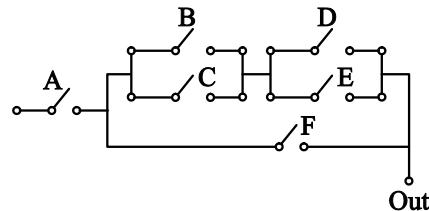
- (14) The switching circuit given in the figure can be expressed in binary logic notation as



- (A) $L = (A + B)(C + D)E$
 - (B) $L = AB + CD + E$
 - (C) $L = E + (A + B)(C + D)$
 - (D) $L = (AB + CD)E$

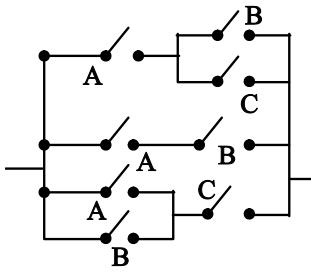
[IES – EC – 1995]

- (15) What Boolean function does the following circuit represent?



- (A) $A[F + (B + C).(D + E)]$
 - (B) $A[F + (B + C).DE]$
 - (C) $A[F + (BC + DE)]$
 - (D) $A[F(B + C) + (D + E)]$

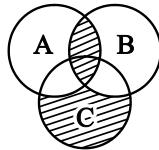
- (16) The minimum Boolean for the following circuit is



- (A) $AB + AC + BC$
 (B) $A + BC$
 (C) $A + B$
 (D) $A + B + C$

[IES – EE – 2011]

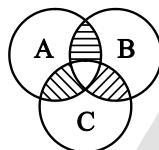
- (17) The Boolean expression for the shaded area in the Venn diagram shown is:



- (A) $A + \bar{B} + C$
 (B) $AB + \bar{A}BC$
 (C) $\bar{ABC} + \bar{ABC}$
 (D) $AB + \bar{ABC}$

[IES – EC – 1996]

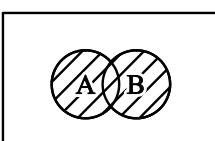
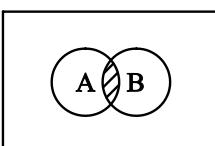
- (18) The Boolean expression for the shaded area in the given Venn diagram is :

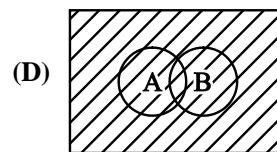
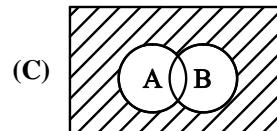


- (A) $AB + BC + CA$
 (B) $AB\bar{C} + \bar{A}BC + A\bar{B}C$
 (C) $ABC + \bar{A}\bar{B}\bar{C}$
 (D) $\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$

[IES – EC – 1998]

- (19) The Venn diagram representing the Boolean expression $A + (\bar{A} \cdot B)$ is

- (A) 
 (B) 



- [GATE - IN - 2011]
 (20) For the Boolean expression $f = \bar{abc} + \bar{ab}\bar{c} + \bar{a}\bar{bc} + abc + ab\bar{c}$, the minimized product of Sum (POS) expression is

- (A) $f = (b + \bar{c}).(a + \bar{c})$
 (B) $f = (\bar{b} + c).(\bar{a} + c)$
 (C) $f = (\bar{b} + c).(a + \bar{c})$
 (D) $f = \bar{c} + abc$

- [GATE - IN - 2008]
 (21) The minimum sum of product form of the Boolean expression

$$Y = \bar{P}\bar{Q}\bar{R}\bar{S} + P\bar{Q}\bar{R}\bar{S} + P\bar{Q}\bar{R}\bar{S} + P\bar{Q}R\bar{S} + P\bar{Q}RS + \bar{P}\bar{Q}RS$$

- (A) $Y = P\bar{Q} + \bar{Q}\bar{S}$
 (B) $Y = P\bar{Q} + \bar{Q}RS$
 (C) $Y = P\bar{Q} + \bar{Q}RS$
 (D) $Y = \bar{Q}\bar{S} + P\bar{Q}R$

- [IES – EC – 2010]
 (22) The standard SOP expression for Boolean expression $AB + AC + BC$ is

- (A) $A\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + ABC$
 (B) $AB\bar{C} + \bar{A}BC + ABC$
 (C) $A\bar{B}C + AB\bar{C} + ABC$
 (D) $\bar{A}\bar{B}C + AB\bar{C} + A\bar{B}\bar{C}$

- [IES – EC – 1999]
 (23) $Y = f(A, B) = \prod M(0, 1, 2, 3)$ represent (M is Max terms)

- (A) NOR gate
 (B) NAND gate
 (C) OR gate
 (D) A situation where output is independent of input.

[IES – EE – 1994]

- (24) There are four Boolean variables x_1, x_2, x_3 and x_4 . The following functions are defined on sets of them :

$$f(x_3, x_2, x_1) = \sum(3, 4, 5)$$

$$g(x_4, x_3, x_2) = \sum(1, 6, 7)$$

$$h(x_4, x_3, x_2, x_1) = fg.$$

Then $h((x_4, x_3, x_2, x_1))$ is

- (A) Zero
- (B) $\sum(3, 12, 13)$
- (C) $\sum(3, 4, 5, 1, 6, 7)$
- (D) $\sum(3, 12, 15)$

[GATE – EC/ EE - 2012]

- (25) In the sum of products function $f(X, Y, Z) = \sum(2, 3, 4, 5)$, the prime implicants are

- (A) $\bar{X}Y + X\bar{Y}$
- (B) $\bar{X}Y + X\bar{Y}\bar{Z} + X\bar{Y}Z$
- (C) $\bar{X}Y\bar{Z} + \bar{X}YZ + X\bar{Y}$
- (D) $\bar{X}Y\bar{Z} + \bar{X}YZ + X\bar{Y}\bar{Z} + X\bar{Y}Z$

[GATE - EE - 2014]

- (26) The SOP (sum of products) form of a Boolean function is $\Sigma(0, 1, 3, 7, 11)$, where inputs are A, B, C, D (A is MSB, and D is LSB). The equivalent minimized expression of the function is

- (A) $(\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{B})(\bar{C} + D)$
- (B) $(\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{C})(\bar{C} + D)$
- (C) $(\bar{B} + C)(\bar{A} + C)(\bar{A} + \bar{C})(\bar{C} + \bar{D})$
- (D) $(\bar{B} + C)(A + \bar{B})(\bar{A} + \bar{B})(\bar{C} + D)$

[GATE - EC - 2008]

- (27) The Boolean functions can be expressed in canonical SOP (sum of products) and POS (product of sums) form. For the function, $Y = A + \bar{B}C$, which are such two forms?

(A) $Y = \sum(1, 2, 6, 7)$ and $Y = \prod(0, 2, 4)$

(B) $Y = \sum(1, 4, 5, 6, 7)$ and

$$Y = \prod(0, 2, 3)$$

(C) $Y = \sum(1, 2, 5, 6, 7)$ and $Y = \prod(0, 1, 3)$

(D) $Y = \sum(1, 2, 4, 5, 6, 7)$ and

$$Y = \prod(0, 2, 3, 4)$$

[GATE – EE – 2015]

- (28) $f(A, B, C, D) = \prod M(0, 1, 3, 4, 5, 7, 9, 11, 12, 13, 14, 15)$ is an maxterm representation of a Boolean function $f(A, B, C, D)$ where A is the MSB and D is the LSB. The equivalent minimized representation of this function is

- (A) $(A + \bar{C} + D)(\bar{A} + B + D)$
- (B) $A\bar{C}D + \bar{A}BD$
- (C) $\bar{A}C\bar{D} + A\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D}$
- (D) $(B + \bar{C} + D)(A + \bar{B} + \bar{C} + D)$
 $(\bar{A} + B + C + D)$

[IES – EC – 2007]

- (29) When the Boolean function

$$F(X_1, X_2, X_3) = \sum(0, 1, 2, 3)$$

$$+ \sum \Phi(4, 5, 6, 7)$$

is minimized, what does one get?

- (A) 1
- (B) 0
- (C) X_1
- (D) X_3

[GATE - IN - 2006]

- (30) Min – term(sum of products) expression for a Boolean function is given as follows.

$$F(A, B, C) = \sum m(0, 1, 2, 3, 5, 6) b$$

Where A is the MSB and C is the LSB. The minimized expression for the function is

- (A) $A + (B \oplus C)$
- (B) $(A \oplus B) + C$
- (C) $\bar{A} + (B \oplus C)$
- (D) \overline{ABC}

[GATE –EE/IN - 2012]

- (31) The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1, is :

- (A) 4
- (B) 6
- (C) 8
- (D) 10

- (32) According to De Morgan's second thermo

- (A) A NAND gate is always complimentary to an AND gate
- (B) A NAND gate equivalent to a bubbled NAND gate

[IES – EC – 1991]

[GATE – EE/EC - 2013]

- (45) A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by anyone of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles
- (A) An AND gate
 (B) An OR gate
 (C) An XOR gate
 (D) A NAND gate

[GATE -EC - 2011]

- (46) Match List-I with List-II and select the correct answer using the code given below the lists :

List I		List II	
A.	AND gate	1.	Boolean complementation
B.	OR gate	2.	Boolean addition
C.	Not gate	3.	Boolean multiplication

Codes:

- | A | B | C |
|-------|---|---|
| (A) 3 | 1 | 2 |
| (B) 1 | 2 | 3 |
| (C) 3 | 2 | 1 |
| (D) 1 | 3 | 2 |

[GATE - EE - 2015]

- (47) Consider the following Sum of products expression, F.

$$F = ABC + \overline{AB}C + A\overline{B}C + \overline{A}\overline{B}C + \overline{ABC}$$

The equivalent Product of Sums expression is

- (A) $F = (A + \overline{B} + C)(\overline{A} + B + C)$
 $(\overline{A} + \overline{B} + C)$
- (B) $F = (A + \overline{B} + \overline{C})(A + B + C)$
 $(\overline{A} + \overline{B} + \overline{C})$
- (C) $F = (\overline{A} + B + \overline{C})(A + \overline{B} + \overline{C})$
 $(A + B + C)$
- (D) $F = (\overline{A} + \overline{B} + C)(A + B + \overline{C})$
 $(A + B + C)$

[GATE – EC – 2014]

- (48) The simplified Boolean expression from the K-MAP

Consider the Boolean function $F(w, x, y, z) = wy + xy + \overline{wxyz} + \overline{wx}y + xz + \overline{x}yz$ which one of the following is the complete set of essential prime implicants?

- (A) w, y, xz, \overline{xz} (B) w, y, xz
 (C) $y, \overline{xy}, \overline{z}$ (D) y, xz, \overline{xz}

- (49) Four logical expressions are given below :

1. $\overline{A}\overline{B}\overline{C}\overline{D}\overline{E}\overline{F}\overline{G}\overline{H}$
 2. $\overline{AB}\overline{CD}\overline{EF}\overline{GH}$
 3. $\overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$
 4. $(\overline{A} + \overline{B})(\overline{C} + \overline{D})(\overline{E} + \overline{F})(\overline{G} + \overline{H})$

Two of these expressions are equal. They are

- (A) 1 and 2 (B) 3 and 4
 (C) 1 and 3 (D) 2 and 4

- (50) What is the simplified form of the Boolean expression

$$T = (X + Y)(X + \overline{Y})(\overline{X} + Y) ?$$

- (A) $\overline{X} Y$ (B) $\overline{X} Y$
 (C) XY (D) $X \overline{Y}$

[IES – EC – 1991]

- (51) The terms $AB + AC + B\overline{C}$ reduce to
 (A) $AB + CA$ (B) $AC + BC$
 (C) $AC + B\overline{C}$ (D) $AB + \overline{B}\overline{C}$

[GATE -EC - 2005]

- (52) Which one of the following is the dual form of the Boolean Identity?

$$\overline{AB} + \overline{A} C = (A + C)(\overline{A} + B) ?$$

(A) $AB + \overline{AC} = AC + \overline{AB}$
 (B) $(A + B) + (A + C) = (A + C)(A + B)$
 (C) $(\overline{A} + B)(\overline{A} + C) = AC + \overline{AB}$
 (D) $AB + \overline{AC} = AB + \overline{AC} + BC$

[GATE -EC - 2006]

- (53) If A and B are Boolean variables, then what is $(A + B) \cdot (A + \overline{B})$ equal to ?
 (A) B (B) A
 (C) A+B (D) AB

[IES -EC - 2008]

- (54) Which one of the following statements is not correct?
- $X + \overline{XY} = X$
 - $X(\overline{X} + Y) = XY$
 - $XY + X\overline{Y} = X$
 - $ZX + Z\overline{XY} = ZX + ZY$

[IES -EC - 2012]

- (55) The Boolean equation $X + [(A + \overline{B})(B + C)]B$ can be simplified to
- $X = \overline{AB}$
 - $X = A\overline{B}$
 - $X + AB$
 - $X + \overline{A}\overline{B}$

Common Data for the Next Two Questions

The following Karnaugh map represents a function F,

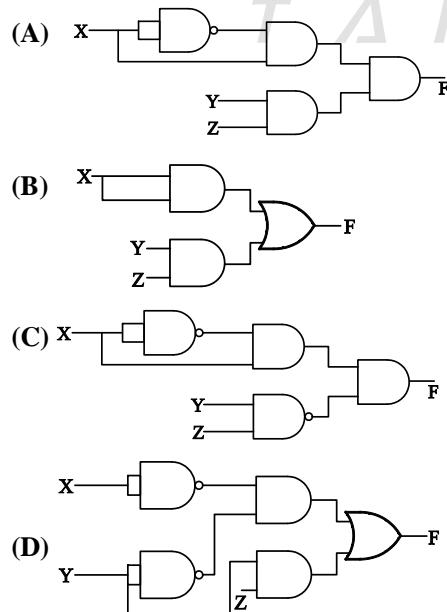
		YZ			
		00	01	11	10
X	0	1	1	1	0
	1	0	0	1	0

[GATE - EE - 2010]

- (56) A minimized form of the function F is
- $F = \overline{XY} + YZ$
 - $F = \overline{XY} + Y\overline{Z}$
 - $F = \overline{XY} + Y\overline{Z}$
 - $F = \overline{XY} + \overline{Y}Z$

[GATE - EE - 2010]

- (57) Which of the following circuits is a realization of the above function F?



[GATE - EC - 2004]

- (58) A Boolean function f of two variables x and y is defined as follows :
 $f(0, 0) = f(0, 1) = f(1, 1) = 1; f(1, 0) = 0$
 Assuming complements of x and y are not available, a minimum cost solution for realizing f using only 2-input NOR gates and 2-input OR gates (each having unit cost) would have a total cost of
- 1 unit
 - 4 unit
 - 3 unit
 - 2 unit

[IES - EC - 2006]

- (59) The Boolean expression for the truth table shown is :

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

$$(A) B(A + C)(\overline{A} + \overline{C})$$

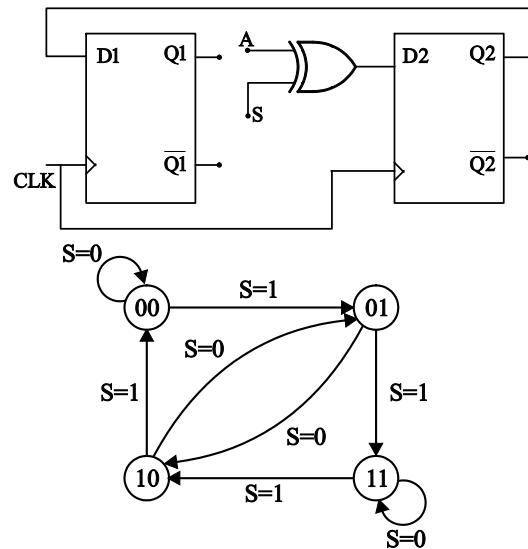
$$(B) B(A + \overline{C})(\overline{A} + C)$$

$$(C) \overline{B}(A + C)(\overline{A} + C)$$

$$(D) \overline{B}(A + C)(\overline{A} + \overline{C})$$

[GATE – EC – 2014]

- (60) The digital logic shown in the figure satisfies the given state diagram when Q1 is connected to input A of the XOR gate. Suppose the XOR gate is replaced an by an XNOR gate. Which one of the following options preserves the state diagram?



Suppose the XOR gate is replaced by an XNOR gate. Which one of the following options preserves the state diagram?

- (A) Input A is connected to \bar{Q}_2
- (B) Input A is connected to Q_2
- (C) Input A is connected to \bar{Q}_1 and S is complemented
- (D) Input A is connected to \bar{Q}_1

[GATE – EC – 2015]

- (61) A 3 input majority gate is defined by the logic function $M(a, b, c) = ab + bc + ca$. Which one of the following gates is represented by the function

$$M(\overline{M(a,b,c)}M(a,b,\bar{c}),c)?$$

- (A) 3-Input NAND gate
- (B) 3-Input XOR gate
- (C) 3-Input NOR gate
- (D) 3-Input XNOR gate

[IES – EC – 2006]

- (62) What is the Boolean expression $A \oplus B$ equivalent to ?

- (A) $AB + \bar{A} \bar{B}$
- (B) $\bar{A}B + A \bar{B}$
- (C) B
- (D) \bar{A}

[GATE – EC – 2014]

- (63) The Boolean expression $(X + Y)(X + \bar{Y}) + (\bar{XY}) + \bar{X}$ simplifies to
- (A) X
 - (B) Y
 - (C) XY
 - (D) $X + Y$

[IES – EE – 1995]

- (64) Match List I with List II and select the correct answer using the codes given below the lists :

List I

List II

- | | |
|--------------------|---------------------------|
| (Boolean identity) | (Boolean expression) |
| A. $Y.(Y + Z)$ | 1. Y |
| B. $Y + \bar{X}.Z$ | 2. $(Y + \bar{X})(Y + Z)$ |
| C. $Y \oplus Z$ | 3. $\bar{Y}Z + \bar{Z}Y$ |
| D. $X + Y.Z$ | 4. $(X+Y)(X+Z)$ |

Codes:

	A	B	C	D
(A)	1	2	3	4
(B)	2	3	1	4

(C) 2 3 4 1

(D) 3 2 1 4

[IES – EE – 2001]

- (65) In Boolean Algebra, if $F = (A + B)(\bar{A} + C)$, then

$$(A) F = AB + \bar{AC}$$

$$(B) F = AB + \bar{A}\bar{B}$$

$$(C) F = AC + \bar{A}\bar{B}$$

$$(D) F = AA + \bar{A}\bar{B}$$

[IES – EE – 2003]

- (66) The simplified form of a logic function

$$Y = \overline{\overline{(AB)}(\overline{AB})}$$
 is :

$$(A) A + B \quad (B) A \cdot B$$

$$(C) \bar{A} + \bar{B} \quad (D) \bar{A} \cdot B + A \bar{B}$$

[IES – EE – 2003]

- (67) The reduced form of the Boolean expression $A[B + C(\bar{AB} + AC)]$ is :

$$(A) \bar{A}B \quad (B) A\bar{B}$$

$$(C) AB \quad (D) AB + B\bar{C}$$

[IES – EE – 2005]

- (68) Which of the following statements is correct?

$$(A) X + \bar{X}Y = X$$

$$(B) X + (\bar{X} + Y) = XY$$

$$(C) X + X + \bar{Y} = XY$$

$$(D) ZX + Z\bar{X}Y = ZX + ZY$$

[IES – EE – 2005]

- (69) The Boolean expression $\bar{YZ} + \bar{X}\bar{Z} + \bar{X}\bar{Y}$ is logically equivalent to

$$(A) YZ + \bar{X}$$

$$(B) YZX + \bar{X}\bar{Y}\bar{Z}$$

$$(C) YZ + XZ + XY$$

$$(D) X\bar{Y}\bar{Z} + \bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y}\bar{Z}$$

[IES – EE – 2008]

- (70) Match List-I with List-II and select the correct answer using the code given the Lists:

List – I

(Expression-I)

$$A. ABC + AB\bar{C} + A\bar{B}C$$

$$B. \bar{A}B\bar{C} + A\bar{B}\bar{C} + B\bar{C}$$

C. $\bar{A}BC + A\bar{B}C + A\bar{B}\bar{C} + ABC$

D. $\bar{A}\bar{B} + \bar{A}B + ABC$

List-II

(Expression-II)

1. $\bar{A} + BC$

2. $A(B + C)$

3. $B\bar{C}$

4. $AB + BC + AC$

Codes:

	A	B	C	D
(A)	2	1	4	3
(B)	4	3	2	1
(C)	2	3	4	1
(D)	4	1	2	3

[IES – EE – 2008]

- (71) The Boolean expression $A.B + \bar{A}\bar{B}$ is logically equivalent to which of the following?

1. $(A + \bar{B})(\bar{A} + B)$

2. $\overline{(A + \bar{B})(A + B)}$

3. $\overline{(A + \bar{B})(\bar{A} + B)}$

4. $\overline{(A.B)(\bar{A}.B)}$

Select the correct answer using the code given below :

(A) 1 and 2 only

(B) 2 and 3 only

(C) 1 and 3 only

(D) None of these

[IES – EC – 1991]

- (72) If X, Y and Z are Boolean variables, then the expression

$X(X+XY)Z(X+Y+Z)$ is equal to

(A) $X + \bar{X}Y$

(B) $X + Y + Z$

(C) XYZ

(D) XZ

[IES – EC – 1992]

- (73) What is dual of $A + [B + (AC)] + D$

(A) $A + [B(A+C)] + D$

(B) $A[B+AC]D$

(C) $A + [B(A+C)]D$

(D) $A[B(A+C)]D$

[IES – EC – 1992]

- (74) The product – of – sum expression for given truth table is

X Y Z

0 0 1

0 1 0

1 0 1

1 1 0

(A) $(\bar{X} + \bar{Y})(X + Y)$

(B) $(X + \bar{Y})(\bar{X} + \bar{Y})$

(C) $(X)(\bar{X} + \bar{Y})$

(D) None of the above

[IES – EC – 1992]

- (75) What is dual of $X + \bar{X}Y = X + Y$

(A) $X+Y=XY$

(B) $\bar{X} + XY = XY$

(C) $X(\bar{X}+Y)=XY$

(D) $X + (\bar{X} + Y) = X + Y$

[IES – EC – 1993]

- (76) The number of switching functions of 3 variables is

(A) 8

(B) 64

(C) 128

(D) 256

[IES – EC – 1997]

- (77) In a digital system, there are three inputs A, B and C. The output should be high when at least two inputs are high. The Boolean expression for the output is :

(A) $AB+BC+AC$

(B) $ABC + AB\bar{C} + \bar{A}CB + A\bar{B}C$

(C) $AB\bar{C} + A\bar{B}C + \bar{A}CB$

(D) $A\bar{B} + B\bar{C} + \bar{A}C$

[IES – EC – 1998]

- (78) The complements of the Boolean expression $AB(\bar{B}C + AC)$ is :

(A) $(\bar{A} + \bar{B}) + (B + \bar{C})(\bar{A} + \bar{C})$

(B) $(\bar{A}\bar{B}) + (B\bar{C})(\bar{A}\bar{C})$

(C) $(\bar{A} + \bar{B})(B + \bar{C})(\bar{A} + \bar{C})$

(D) $(A + B)(\bar{B} + C)(A + C)$

[IES – EC – 1999]

- (79) The Boolean theorem $AB + \bar{A}C + BC = AB + \bar{A}C$ corresponds to

(A) $(A+B)(\bar{A}+C)(B+C) =$

$(A+B)(\bar{A}+C)$

(B) $AB + \bar{A}C + BC = AB + BC$

(C) $AB + \bar{A}C + BC = AB + BC$

(D) $(A+B).(\bar{A}+C).(B+C) = AB + \bar{A}C$

[IES – EC – 2002]

- (80) Consider the Boolean expression

$$X = ABCD + A\bar{B}CD + \bar{A}BCD + \bar{A}C\bar{B}D$$

The simplified form of X is

(A) $\bar{C} + \bar{D}$

(B) BC

(C) CD

(D) $\bar{B}\bar{C}$

[IES – EC – 2003]

- (81) Match List I with List II and select the correct answer using the codes given below the Lists :

List I		List II	
A.	$A \oplus B = 0$	1.	$A \neq B$
B.	$\overline{A + B} = 0$	2.	$A = B$
C.	$\bar{A}.B = 0$	3.	$A = 1$ OR $B = 1$
D.	$A \oplus B = 1$	4.	$A = 1$ OR $B = 0$

Codes:

A B C D

(A) 3 2 1 4

(B) 2 3 4 1

(C) 3 2 4 1

(D) 2 3 1 4

[IES – EC – 2003]

- (82) The Boolean expression

$$(\bar{A}+B)(A+\bar{C})(\bar{B}+\bar{C})$$
 simplifies to

(A) $(A+B)\bar{C}$ (B) $(A+\bar{B})\bar{C}$

(C) $(\bar{A}+B)\bar{C}$ (D) $(\bar{A}+\bar{B})\bar{C}$

[IES – EC – 2003]

- (83) The minimum number of NAND gates required to implement the Boolean junction $A + A\bar{B} + A\bar{B}C$ is equal to

(A) Zero (B) 1

(C) 4 (D) 7

[IES – EC – 2004]

- (84) A, B and C are three Boolean variables. Which one of the following Boolean expressions cannot be minimized any further?

(A) $Z = A.\bar{B}.\bar{C} + A.B.\bar{C} + A.B.C$

$$+ \bar{A}.B.\bar{C}$$

(B) $Z = A.\bar{B}.C + A.B.\bar{C} + A.B.C + \bar{A}.\bar{B}.\bar{C}$

(C) $Z = A.\bar{B}.\bar{C} + \bar{A}.\bar{B}.C + A.B.C$

$$+ \bar{A}.B.\bar{C}$$

(D) $Z = \bar{A}.B.\bar{C} + A.B.\bar{C} + A.B.C$

$$+ \bar{A}.\bar{B}.C$$

[IES – EC – 2005]

(85) $AB + \bar{A}C = (A+C)(\bar{A}+B)$

Which one of the following is the dual form of the Boolean identity given above.

(A) $AB + \bar{AC} = AC + \bar{AB}$

(B) $(A+B)(\bar{A}+C) = (A+C)(\bar{A}+B)$

(C) $(A+B)(\bar{A}+C) = AC + \bar{AB}$

(D) $AB + \bar{AC} = AB + \bar{AC} + BC$

[IES – EC – 2006]

- (86) What does the Boolean expression $AD + ABCD + ACD + \bar{A}B + \bar{A}B$ on minimization result into ?

(A) $A + D$

(B) $AD + \bar{A}$

(C) AD

(D) $\bar{A} + D$

[IES – EC – 2008]

- (87) The Boolean function $A + BC$ is a reduced form of which one of the following?

(A) $AB + BC$

(B) $\bar{A}B + A\bar{B}C$

(C) $(A+B).(A+C)$

(D) None of these

[IES – EC – 2010]

- (88) The Boolean expression

$$\overline{A+\bar{B}+C} + \overline{\bar{A}+\bar{B}+C} + \overline{A+\bar{B}+\bar{C}} + ABC$$

reduces to :

(A) A

(B) B

(C) C

(D) $A+B+C$

[IES – EC – 2010]

- (89) The complement of the expression

$$Y = ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC$$

(A) $(A+\bar{B})(A+\bar{C})$

(B) $(\bar{A}+B)(A+C)$

(C) $(A+\bar{B})(\bar{A}+C)$

(D) $(\bar{A}+\bar{B})(A+\bar{C})$

[IES - EC - 2011]

- (90) If the Boolean expression $\overline{PQ} + QR + PR$ is minimized, the expression becomes
 (A) $\overline{P}Q + QR$ (B) $\overline{P}Q + PR$
 (C) $QR + PR$ (D) $\overline{P}Q + QR + PR$

[IES - EC - 2012]

- (91) Simplified form of the logic expression $(A + \overline{B} + C)(A + \overline{B} + \overline{C})(A + B + C)$
 (A) $\overline{AB} + \overline{C}$ (B) $A + \overline{BC}$
 (C) A (D) $AB + \overline{C}$

[GATE - IN - 1994]

- (92) The Boolean expression $\overline{A + B + C}$ is equal to
 (A) $\overline{A} + \overline{B} + \overline{C}$ (B) $\overline{A}\overline{B}\overline{C}$
 (C) $\overline{A + B + C}$ (D) $A.(B + C)$

[GATE - IN - 2000]

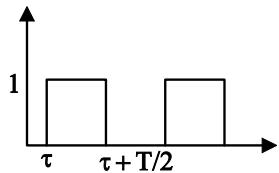
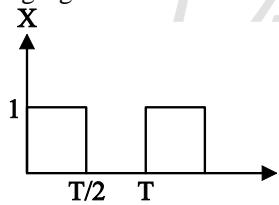
- (93) The expression $X = \overline{AB}$ is equivalent to
 (A) $\overline{A} + \overline{B}$ (B) $AB + A$
 (C) $A + B$ (D) AB

[GATE - IN - 2004]

- (94) The simplest form of the Boolean expression $ABC\overline{D} + ABC\overline{D} + AB\overline{C}\overline{D} + ABCD$ is
 (A) AD (B) BC
 (C) $\overline{A}B$ (D) AB

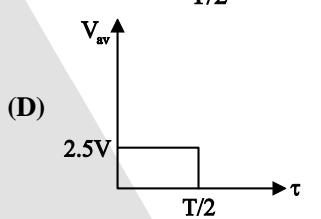
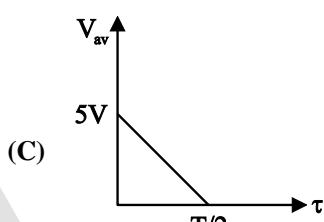
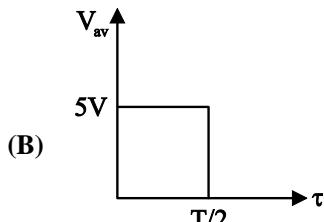
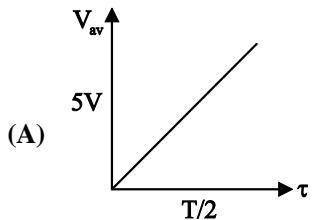
[GATE - IN - 2007]

- (95) Two square waves of equal period T, but with a time delay τ are applied to a digital circuit whose truth table is shown in the following figure.



X	Y	Output
0	0	1
0	1	0
1	0	0
1	1	1

The high and the low levels of the output of the digital circuit are 5V and 0V, respectively. Which one of the following figures shows the correct variation of the average value of the output voltage of τ for $0 \leq t \leq (T/2)$?



[GATE - EE - 2003]

- (96) The Boolean expression $\overline{XYZ} + \overline{XYZ} + XY\overline{Z} + X\overline{YZ} + XYZ$ can be simplified to
 (A) $X\overline{Z} + \overline{X}Z + YZ$
 (B) $XZ + \overline{Y}Z + Y\overline{Z}$
 (C) $\overline{XY} + YZ + XZ$
 (D) $\overline{XY} + Y\overline{Z} + \overline{X}Z$

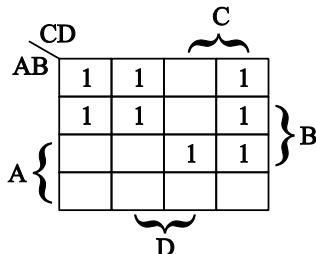
[GATE - EE - 2004]

- (97) The simplified form of the Boolean expression $Y = (\overline{A}BC + D)(\overline{A}D + \overline{B}\overline{C})$ can be written as
 (A) $\overline{A}D + \overline{B}\overline{C}D$
 (B) $AD + B\overline{C}D$
 (C) $(\overline{A} + D)(\overline{B}C + \overline{D})$
 (D) $A\overline{D} + BC\overline{D}$.

- [GATE -EC - 1999]**
- (98) The Logical expression $y = A + \overline{AB}$ is equivalent to
 (A) $y = AB$ (B) $y = \overline{AB}$
 (C) $y = \overline{A} + B$ (D) $y = A + B$
- [GATE -EC - 2007]**
- (99) The Boolean function $Y = AB + CD$ is to be realized using only 2-input NAND gates. The minimum number of gates required is
 (A) 2 (B) 3
 (C) 4 (D) 5
- [GATE -EC - 1999]**
- (100) The minimized form of the logical expression $(\overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + AB\overline{C})$ is
 (A) $\overline{A}\overline{C} + B\overline{C} + \overline{A}B$
 (B) $A\overline{C} + \overline{B}C + \overline{A}B$
 (C) $\overline{A}C + \overline{B}C + \overline{A}B$
 (D) $A\overline{C} + \overline{B}C + A\overline{B}$
- [GATE -EC - 2003]**
- (101) If the functions W, X, Y and Z are as follows
- $$W = R + \overline{P}Q + \overline{R}S$$
- $$X = P\overline{Q}\overline{R}\overline{S} + \overline{P}\overline{Q}\overline{R}\overline{S} + P\overline{Q}\overline{R}\overline{S}$$
- $$Y = RS + PR + \overline{P}\overline{Q} + \overline{P}\overline{Q}$$
- $$Z = R + S + \overline{P}Q + \overline{P}\overline{Q}R + P\overline{Q}S$$
- (A) $W = Z, X = \overline{Z}$
 (B) $W = Z, X = Y$
 (C) $W = Y$
 (D) $W = Y = \overline{Z}$
- [GATE -EC - 2004]**
- (102) The Boolean expression $AC + B\overline{C}$ is equivalent to
 (A) $\overline{A}C + B\overline{C} + AC$
 (B) $\overline{B}C + AC + B\overline{C} + \overline{A}C\overline{B}$
 (C) $AC + B\overline{C} + \overline{B}C + ABC$
 (D) $ABC + \overline{ABC} + ABC + A\overline{B}C$
- [GATE -EC -2007]**
- (103) The Boolean expression
- $Y = \overline{ABCD} + \overline{ABC}\overline{D} + A\overline{BCD} + A\overline{B}\overline{CD}$
- (A) $Y = \overline{ABCD} + \overline{ABC} + A\overline{CD}$
 (B) $Y = \overline{ABCD} + B\overline{C}\overline{D} + A\overline{B}\overline{CD}$
 (C) $Y = \overline{ABC}\overline{D} + \overline{BCD} + A\overline{BCD}$
 (D) $Y = \overline{ABC}\overline{D} + \overline{BCD} + A\overline{B}\overline{CD}$
- [GATE -EC - 2009]**
- (104) If $X = 1$ in the logic equation $[X + Z\{\overline{Y} + (\overline{Z} + XY)\}]\{\overline{X} + \overline{Z}(X + Y)\} = 1$, then
 (A) $Y = Z$ (B) $Y = \overline{Z}$
 (C) $Z = 1$ (D) $Z = 0$
- [GATE -EC - 2000]**
- (105) Karnaugh map is used to
 (A) Minimize the number of flip flops in a digital circuit.
 (B) Minimize the number of gates only in a digital circuit
 (C) Minimize the number of gates and fan in of a digital circuit
 (D) Design gates
- [GATE – EC – 2005]**
- (106) The number of product terms in the minimized sum-of-product expression obtained through the following k-map is (where, “d” denotes don’t care states)
- | | | | |
|---|---|---|---|
| 1 | 0 | 0 | 1 |
| 0 | d | 0 | 0 |
| 0 | 0 | d | 1 |
| 1 | 0 | 0 | 1 |
- (A) 2 (B) 3
 (C) 4 (D) 5
- [IES – EC – 1997]**
- (107) Consider the Karnaugh Map given below
 The function represented by this map can be simplified to the minimal form as
- | | | | | | |
|----------|----|-------------|---|---|---|
| | | X_1X_2 | | | |
| | | 00 01 11 10 | | | |
| X_3X_4 | 00 | 1 | | d | d |
| | 01 | | 1 | d | 1 |
| | 11 | | d | 1 | |
| | 10 | 1 | d | | d |
- (A) $X_1\overline{X}_2\overline{X}_4 + X_2X_4 + X_1\overline{X}_3$
 (B) $X_1X_2X_4 + X_2X_4 + X_1\overline{X}_2\overline{X}_3\overline{X}_4$
 (C) $X_2X_4 + \overline{X}_2\overline{X}_4 + X_1\overline{X}_3$
 (D) $X_1\overline{X}_2\overline{X}_4 + \overline{X}_1X_2\overline{X}_3\overline{X}_4$
 $+ X_1X_2$

[IES – EE – 2010]

(108) map given in the figure is



- (A) $\overline{AC} + \overline{AD} + ABC$
- (B) $\overline{AB} + \overline{AD} + ABC$
- (C) $AC + ACD + ABC + BCD$
- (D) $\overline{AB} + \overline{CD} + AD$

[IES – EC – 2007]

(109) By inspecting the Karnaugh map plot of the switching function

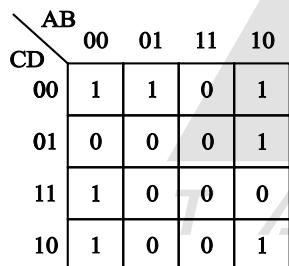
$$F(X_1 X_2 X_3) = \sum(1, 3, 6, 7)$$

One can say that the redundant prime implicant is

- (A) $\overline{X_1} \cdot X_3$
- (B) $X_2 \cdot X_3$
- (C) $X_1 \cdot X_2$
- (D) X_3

[GATE -EC - 1998]

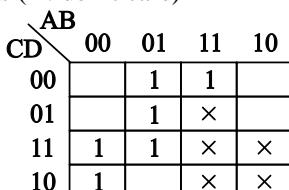
(110) The K-map for a Boolean function is shown in figure. The number of essential prime implicants for this function is :



- (A) 4
- (B) 5
- (C) 6
- (D) 8

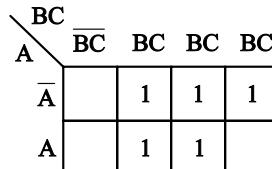
[IES – EC – 1996]

(111) The Minimized expression for the given K-Map is (X: don't care)



- (A) $CB + BD + CD$
- (B) $AB + C \bar{B} + B \bar{C}$
- (C) $C \bar{B} + AC + B \bar{C}$
- (D) $\bar{C}B + BD + C \bar{B}$

(112)

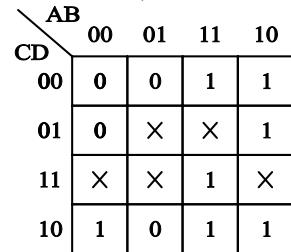


For a function F, the Karnaugh map is shown above. Then minimal representation of F is

- (A) $AB + \overline{C}$
- (B) $C + \overline{AB}$
- (C) $A + B + C$
- (D) $A + \overline{BC}$

[IES – EC – 2002]

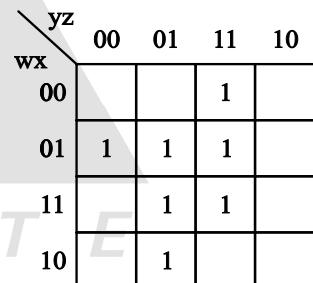
(113) The minimized expression for the given K-map (A: don't care) is :



- (A) $A + \overline{BC}$
- (B) $B + AC$
- (C) $C + AB$
- (D) $A \cdot B \cdot C$

[IES – EC – 2005]

(114) What is the minimized logic expression corresponding to the given Karnaugh Map?



- (A) xz
- (B) $\overline{w} x \overline{y} + \overline{w} y z + w \overline{y} z + w x y$
- (C) $\overline{w} x \overline{y} + \overline{w} y z + w \overline{y} z + w x \overline{y}$
- (D) $xz + \overline{w} y z + \overline{w} x \overline{y} + w x y + w \overline{y} z$

[GATE-IN-2007]

(115) A logic circuit implements the Boolean function $F = \bar{X} \cdot Y + X \cdot \bar{Y} \cdot \bar{Z}$. It is found that the input combination $X = Y = 1$ can never occur. Taking this into account, a simplified expression for F is given by

- (A) $\bar{X} + \bar{Y} \cdot \bar{Z}$
- (B) $X + Z$
- (C) $X - Z$
- (D) $Y + X \cdot \bar{Z}$

[GATE – IN – 2018]

- (125) The product of sum expression of a Boolean function $F(A, B, C)$ of three variables is given by

$$F(A, B, C) = (A + B + \bar{C}) \cdot (A + \bar{B} + \bar{C}) \cdot$$

$$(\bar{A} + B + C) \cdot (\bar{A} + \bar{B} + \bar{C})$$

The canonical sum of product expression of $F(A, B, C)$ is given by

- (A) $\bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + ABC$
 (B) $\bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C}$
 (C) $A\bar{B}\bar{C} + A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}\bar{C}$
 (D) $\bar{A}\bar{B}\bar{C} + \bar{A}BC + AB\bar{C} + ABC$

[GATE-EE-2019]

- (126) The output expression for the Karnaugh map shown below is :

		PQ	00	01	11	10
		RS	00	01	11	10
00	00	0	1	1	0	
	01	1	1	1	1	
11	11	1	1	1	1	
	10	0	0	0	0	

- (A) $QR + \bar{S}$ (B) $Q\bar{R} + S$
 (C) $QR + S$ (D) $Q\bar{R} + \bar{S}$

[GATE-IN-2019]

- (127) The total number of Boolean functions with distinct truth-tables that can be defined over 3 Boolean variables is _____.
T A R G A T E
-----0000-----

03

Logic GATES

[IES – EE – 1992]

- (1) Which of the following statement is true?
- IC's area always linear
 - Digital circuits are linear circuits
 - AND gate is a logic circuit whose output is equal to its highest input
 - In a four - input AND circuit, all input must be UP for the output to be UP.

[GATE - IN - 1995]

- (2) This question contains 4 sub-sections of matching the pairs. Indicate the answer as follows :

If A and B are the inputs to a logic gate, then match the logic with its output

(a)	NAND	(i)	$\bar{A} + \bar{B}$
(b)	NOR	(ii)	$\bar{A} + B$
(c)	XNOR	(iii)	$\overline{AB} + AB$
(d)	AND	(iv)	$\bar{A} \cdot \bar{B}$

[IES – EE – 2012]

- (3) **Statement (I) :** XOR gate is not a universal gate

Statement (II) : It is not possible to realize any Boolean function using XOR gates only

- Both (I) and (II) is true and R is the correct explanation of A
- Both (I) and (II) is true but R is NOT the correct explanation of A
- (I) is true but (II) is false
- (I) is false but (II) is true

[IES – EC – 1995]

- (4) Which one of the following sets of gates are best suited for parity checking and party generation?

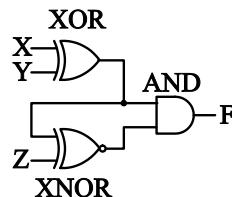
- AND, OR, NOT gates
- X – OR, X – NOR gates
- NAND gates
- NOR gates

[IES – EC – 2001]

- (5) In the negative logic system,
- The more negative of the two logic levels represents a logic '1' state.
 - The more negative of the two logic levels represents a logic '0' state.
 - All input and output voltage levels are negative.
 - The output is always complement of the intended logic function.

[GATE – EC – 2014]

- (6) The output F in the digital logic circuit shown in the figure is



$$(A) F = \overline{XYZ} + X\overline{YZ}$$

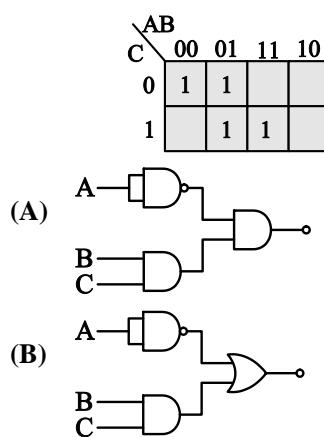
$$(B) F = \overline{XY}\overline{Z} + XY\overline{Z}$$

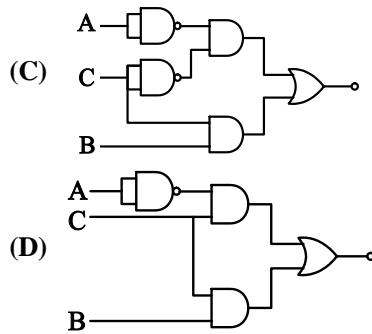
$$(C) F = \overline{XYZ} + XYZ$$

$$(D) F = \overline{XYZ} + XYZ$$

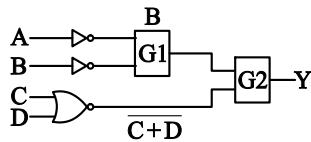
[GATE-EE-2014]

- (7) Which of the following logic circuits is a realization of the function F whose Karnaugh map is shown in figure



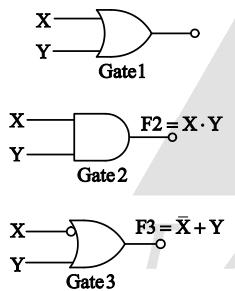


- [GATE – EC – 2015]
- (8) In the figure shown, the output Y is required to be $Y = AB + \overline{CD}$. The gates G1 and G2 must be, respectively,



- (A) NOR, OR
 (B) OR, NAND
 (C) NAND, OR
 (D) AND, NAND

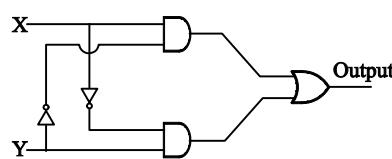
- [GATE – EC – 2015]
- (9) A universal logic gate can implement any Boolean function by connecting sufficient number of them appropriately. Three gates are shown.



Which one of the following statements is TRUE?

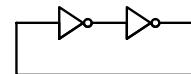
- (A) Gate 1 is a universal gate.
 (B) Gate 2 is a universal gate.
 (C) Gate 3 is a universal gate.
 (D) None of the gates shown is a universal gate

- [GATE – IN – 2015]
- (10) The logic evaluated by the circuit at the output is



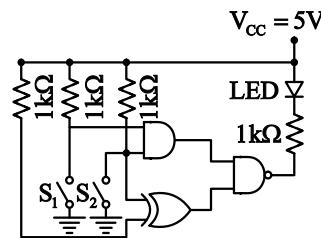
- (A) $X\bar{Y} + Y\bar{X}$
 (B) $(\overline{X+Y})XY$
 (C) $(\overline{XY})XY$
 (D) $\overline{XY} + X\bar{Y} + X + Y$

- [GATE • EE – 2004/IES – EE – 2010]
- (11) The digital circuit using two inverters shown in Fig. will act as



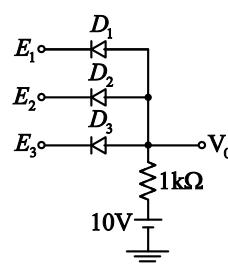
- (A) A bistable multi-vibrator
 (B) An astable multi-vibrator
 (C) A Monostable multi-vibrator
 (D) An oscillator

- [GATE-EC-2001]
- (12) In the figure, the LED



- (A) emits light when both S_1 and S_2 are closed.
 (B) emits light when both S_1 and S_2 are open.
 (C) emits light when only of S_1 and S_2 is closed.
 (D) does not emit light, irrespective of the switch positions.

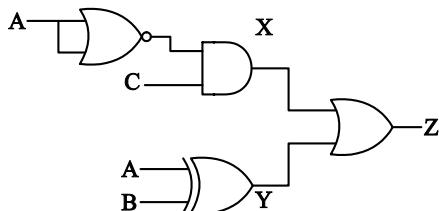
- [GATE-EC-2015]
- (13) In the circuit shown, diodes D_1 , D_2 and D_3 are ideal, and the inputs E_1 , E_2 and E_3 are '0 V' for logic '0' and '10V' for logic '1'. What logic gate does the circuit represent?



- (A) 3 input OR gate
 (B) 3 input NOR gate
 (C) 3 input AND gate
 (D) 3 input XOR gate

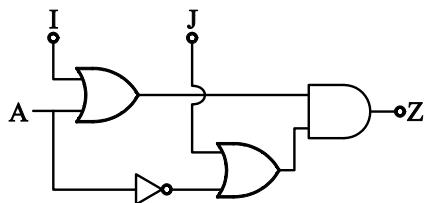
[GATE-IN-1998]

- (14) For the logic circuit shown in figure write the expression for X, Y and Z.



[IES - EC - 2006/2010]

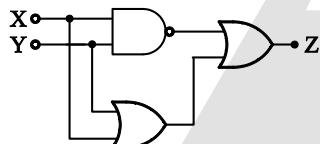
- (15) The circuit given in the figure is to be used to implement the function $Z = f(A,B) = \overline{A} + B$. What values should be selected for I and J?



- (A) $I = 0, J = B$
 (B) $I = 1, J = B$
 (C) $I = B, J = 1$
 (D) $I = \overline{B}, J = 0$

[IES - EE - 1996]

- (16) Which of the following is the truth table of the given logic circuit?



(A)

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	1

(B)

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

(C)

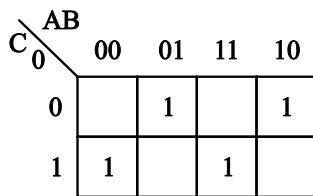
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

(D)

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

[GATE - IN - 1995]

- (17) A combinational circuit has input A, B and C and its Karnaugh Map is as shown. The output of the circuit is given by



- (A) $(\overline{A}\overline{B} + A\overline{B})C$

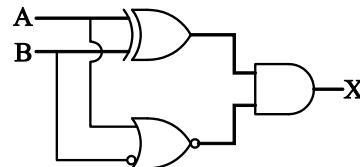
- (B) $(\overline{A}\overline{B} + A\overline{B})\overline{C}$

- (C) \overline{ABC}

- (D) $A \oplus B \oplus C$

[IES - EE - 1998]

- (18) The output X of the circuit shown in the figure will be



- (A) AB

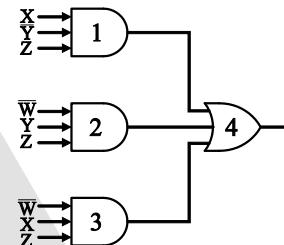
- (B) \overline{AB}

- (C) $A\overline{B}$

- (D) $\overline{A}\overline{B}$

[IES - EE - 1999]

- (19) Which one of the gate labelled 1, 2, 3 and 4 in the network shown in the figure is redundant?



- (A) 1

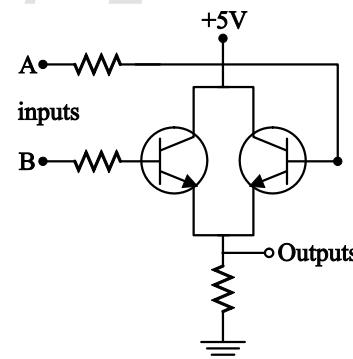
- (B) 2

- (C) 3

- (D) 4

[IES - EE - 2000]

- (20) The circuit shown in the given figure is



- (A) an AND gate

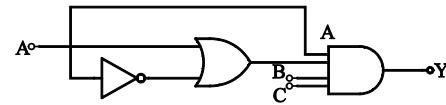
- (B) an OR gate

- (C) a XOR gate

- (D) a NAND gate

[IES - EE - 2002]

- (21) The Boolean expression for the output Y in the logic circuit is



(A) $A \bar{B} C$

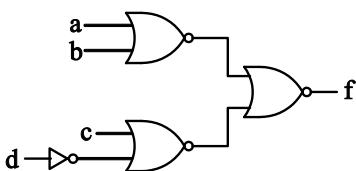
(C) $\bar{A} B C$

(B) $A B C$

(D) $\bar{A} \bar{B} \bar{C}$

[IES – EE – 2009]

- (22) Which one of the following is the correct output (f) of the below circuit?



(A) $(a+b)(c+d)$

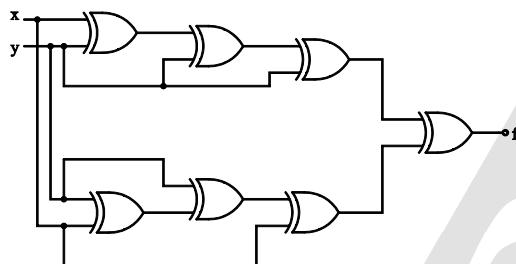
(B) $(\bar{a}+\bar{b})(c+d)$

(C) $(a+\bar{b})(c+\bar{d})$

(D) $(a+b)(\bar{a}+\bar{d})$

[IES – EE – 2010]

- (23) The circuit shown below generates the function of



(A) $x \oplus y$

(B) 0

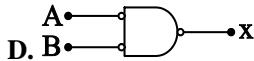
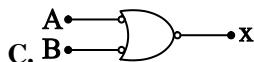
(C) $x\bar{y} + yx + \bar{y}x$

(D) $x.\bar{y}$

[IES – EE – 2010]

- (24) Match List I with List II and select the correct answer using the code given below the lists :

List-I



List-II

1. AB

2. \overline{AB}

3. $A + B$

4. $\overline{A + B}$

Codes :

A	B	C	D
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(A) 3	1	4	2
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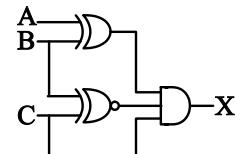
(B) 2	1	4	3
-------	---	---	---

(C) 3	4	1	3
-------	---	---	---

(D) 2	4	1	3
-------	---	---	---

[IES – EE – 2011]

- (25) For logic circuit shown, the required inputs A, B and C to make the output X = 1 are, respectively,



(A) 1, 0 and 1

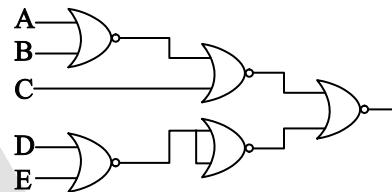
(B) 0, 0 and 1

(C) 1, 1 and 1

(D) 0, 1 and 1

[IES – EC – 2000]

- (26) The circuit shown in figure realizes the function



(A) $(A+B+C)(D\bar{E})$

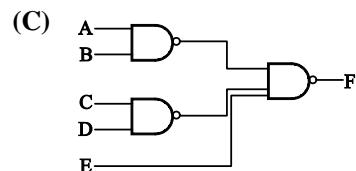
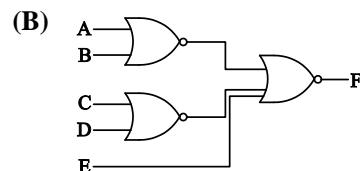
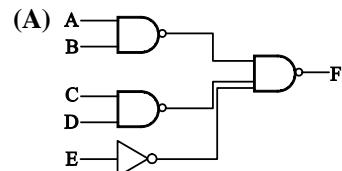
(B) $(A+(\overline{B+C}))(\bar{D}E)$

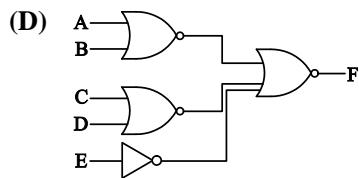
(C) $(A+B+C)(\bar{D}\bar{E})$

(D) $(\overline{A+B}+C)(\bar{D}\bar{E})$

[IES – EC – 1991]

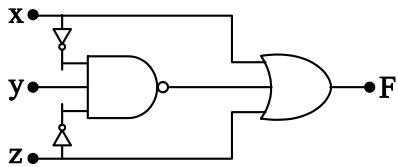
- (27) The Boolean function $F=AB+CD+E$ can be realized as





[IES - EC - 1992]

- (28) The minimized version for the logic circuit shown in the figure is:



- (A)
- (B)
- (C)
- (D)

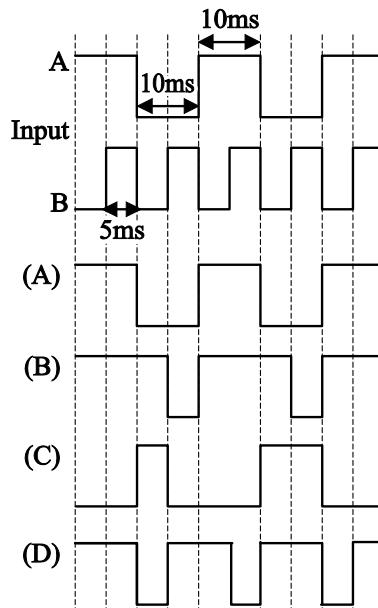
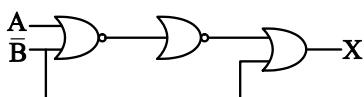
[IES - EC - 1992/1993/1996/2000]

- (29) Which of the following is a coincidence logic circuit?

- (A)
- (B)
- (C)
- (D)

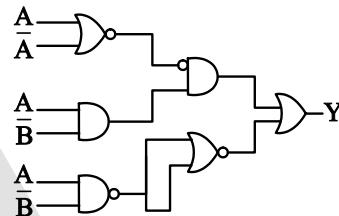
[IES - EC - 1994]

- (30) The output (X) wave form for the below combination circuit for the inputs at A and B (waveform shown in the figure) will be.



[IES - EC - 1995]

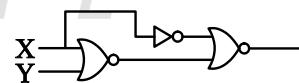
- (31) The output Y for the logic circuit shown in the given figure is



- (A) $A\bar{B}$
- (B) $\bar{A} + \bar{B}$
- (C) $\bar{A}B$
- (D) $A + \bar{B}$

[IES - EC - 1995]

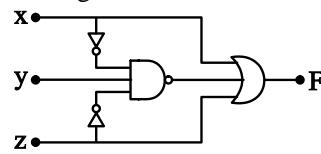
- (32) The logic circuit shown in the given figure can be minimized to

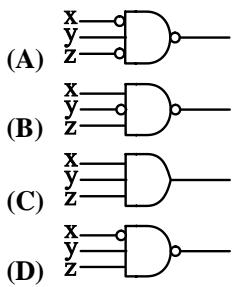


- (A) $X \rightarrow \text{---}$
- (B) $X \rightarrow \text{---}$
- (C) $X \rightarrow \text{---}$
- (D) $X \rightarrow \text{---}$

[IES - EC - 1996]

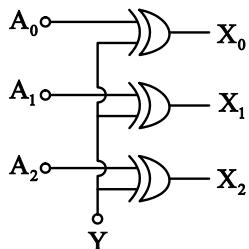
- (33) The minimized logic circuit for the circuit shown in fig. is





[IES – EC – 1996]

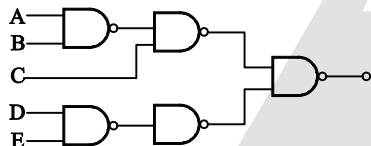
- (34) In the figure shown X_2 , X_1 , X_0 will be 1's complement of $A_2 A_1 A_0$ if



- (A) $Y = 0$
 (B) $Y = 1$
 (C) $Y = \bar{A}_0 = \bar{A}_1 = \bar{A}_2$
 (D) $Y = A_0 = A_1 = A_2$

[IES – EC – 1996]

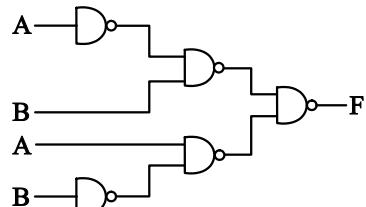
- (35) The circuit shown in the following figure realizes the function



- (A) $(\bar{A} + \bar{B})C + \bar{D}\bar{E}$
 (B) $(A + B)C + D + E$
 (C) $AB + C = DE$
 (D) $AB + C(D + E)$

[IES – EC – 2003/2007]

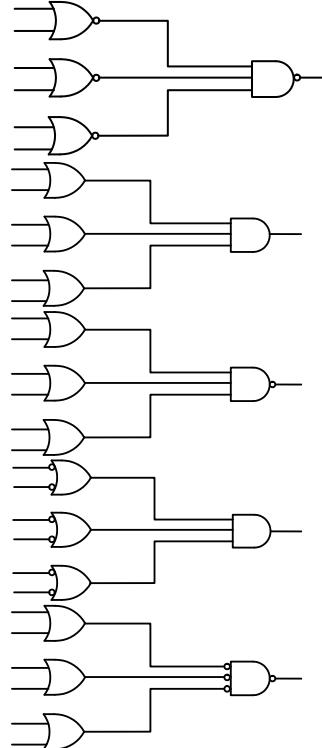
- (36) The circuit shown in the figure is functionally equivalent to



- (A) NOR gate
 (B) OR gate
 (C) EX-OR gate
 (D) NAND gate

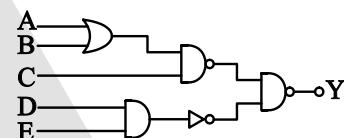
[IES – EC – 1998]

- (37) The circuit shown in Fig. is equivalent to



[IES – EC – 1998]

- (38) The output Y of the circuit shown in the figure is

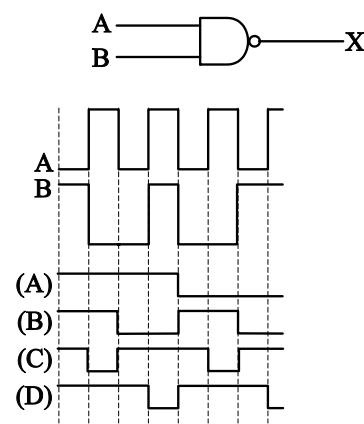


- (A) $(A+B)C+DE$
 (B) $AB+C(D+E)$
 (C) $(A+B)C+D+E$
 (D) $(AB+C)DE$

[IES – EC – 1999]

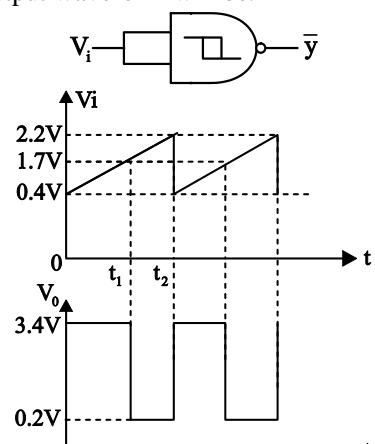
- (39) The given figure shows a NAND gate with input waveforms A and B.

The correct output waveform X of the gate is :



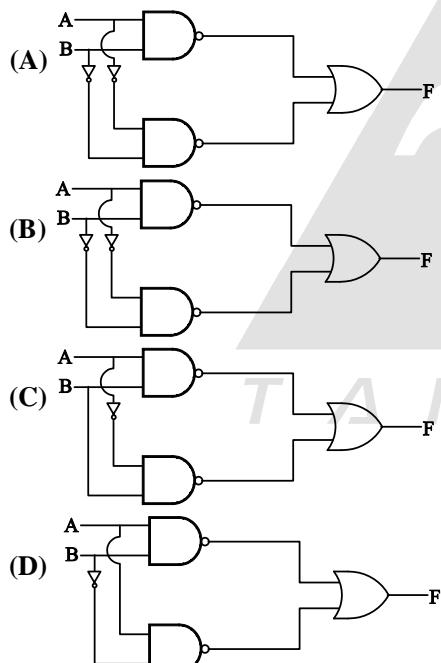
[IES – EC – 1999]

- (40) The input waveform V_i and the output waveform V_o of a Schmitt NAND are shown in the given figures. The duty cycle of the output waveform will be.



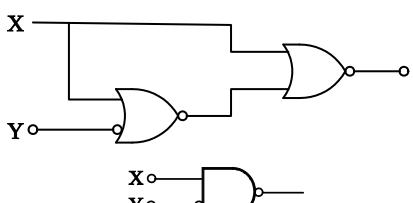
[IES – EC – 2000]

- (41) Which one of the following figures represents the coincidence logic?



[IES = EC = 2000]

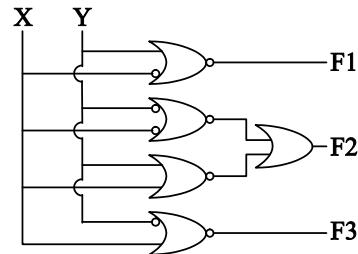
- (42) The logic operations of two combinational circuits given in figure - I and figure - II are



- (A) Entirely different (B) identical
(C) Complementary (D) Dual

[IES – EC – 2001]

- (43)** The circuit shown in the given figure is :

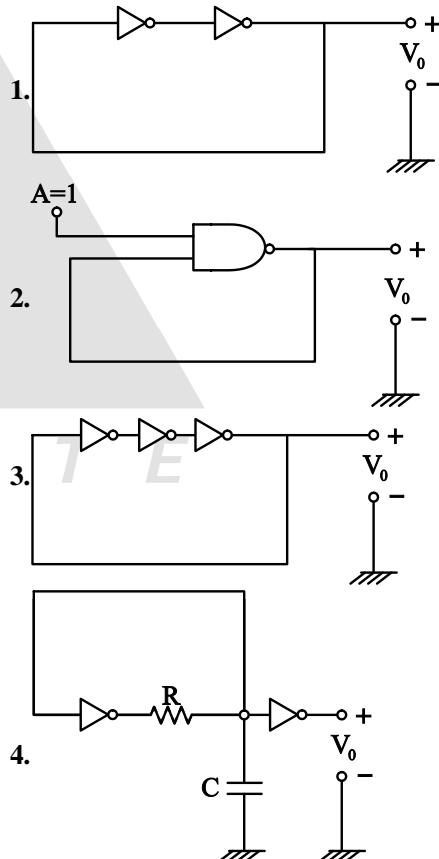


- (A) An adder circuit
 - (B) A subtractor circuit
 - (C) A comparator circuit
 - (D) A parity generator circuit

[IES – EC – 2002]

- (44) Consider the following circuits (Assume all gates to have a finite propagation delay)

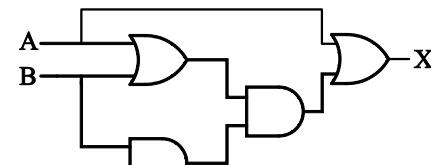
Which of these circuits generate a periodic square wave output?



- (A) 1 and 2
 - (B) 3 and 4
 - (C) 2, 3 and 4
 - (D) 1, 2, 3 and 4

[IES – EC – 2007]

- (45) For the logic circuit given below, what is the simplified Boolean function?



- (A) $X = AB + C$
 (B) $X = BC + A$
 (C) $X = AB + AC$
 (D) $X = AC + B$

[IES - EC - 2007]

- (46) The black box in the figure below, consists of a minimum complexity circuit that uses only AND, OR and NOT gates.



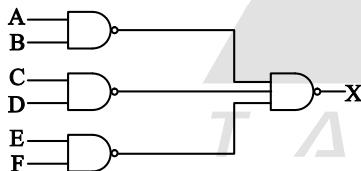
The function $f(X, Y, Z) = 1$ whenever X, Y are different and 0 otherwise. In addition the 3 inputs X, Y, Z are never all the same value.

Which one of the following equations leads to the correct design for the minimum complexity circuit?

- (A) $X'Y + XY'$
 (B) $X + YZ'$
 (C) $X'Y'Z + XY'Z$
 (D) $XY + Y'Z + Z'$

[IES - EC - 2010]

- (47) The output X of the below logic circuit is



- (A) $AB + CD + EF$
 (B) $\overline{AB} + \overline{CD} + \overline{EF}$
 (C) $(A + B).(C + D).(E + F)$
 (D) $(\overline{A + B}).(\overline{C + D}).(\overline{E + F})$

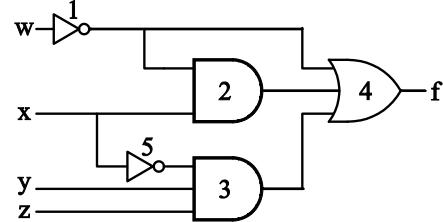
[IES - EC - 2011]

- (48) Which of the following are universal gates ?
 1. AND
 2. NAND
 3. OR
 4. NOR
 5. NOT
 (A) 1, 2, 3, 4 and 5
 (B) 1, 3 and 4 only

- (C) 2, 3 and 5 only
 (D) 2 and 4 only

[IES - EC - 2011]

- (49) Consider the following gate network:

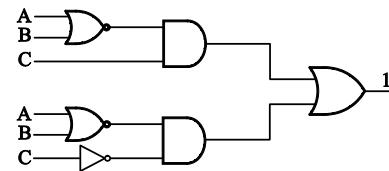


Which one of the following gates is redundant?

- (A) Gate No. 1 (B) Gate No. 2
 (C) Gate No. 3 (D) Gate No. 4

[GATE - IN - 1992]

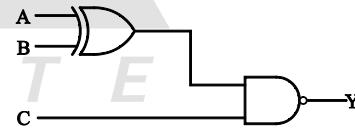
- (50) In the digital circuit shown below, the output f is found to be logic 1 when A is logic '0'. The values of B and C are



- (A) $B = 1, C = 0$
 (B) $B = 0, C = 0$ or 1
 (C) $B = 1, C = 1$
 (D) Indeterminate

[GATE - EE - 1996]

- (51) The Boolean expression for the output of the logic circuit shown in figure is



- (A) $Y = \overline{A} \overline{B} + AB + \overline{C}$
 (B) $Y = \overline{A} \overline{B} + AB + C$
 (C) $Y = \overline{A} B + \overline{A} \overline{B} + C$
 (D) $Y = \overline{A} B + \overline{A} \overline{B} + \overline{C}$

[GATE - EE - 1999]

- (52) The logic function $f = \overline{(x.y)} + \overline{(\bar{x}.y)}$ is the same as

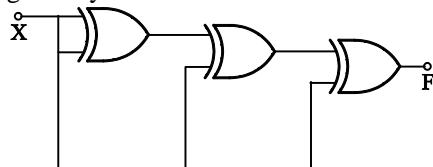
- (A) $f = (x + y)(\overline{x} + \overline{y})$
 (B) $f = \overline{(\overline{x} + \overline{y})} + (x + y)$
 (C) $f = (\overline{x.y}) \cdot (\overline{x}\overline{y})$
 (D) None of (A), (B), (C)

- (A) 10 MHZ
(C) 1 GHZ

- (B) 100 MHZ
(D) 2GHZ.

[GATE -EC - 1988]

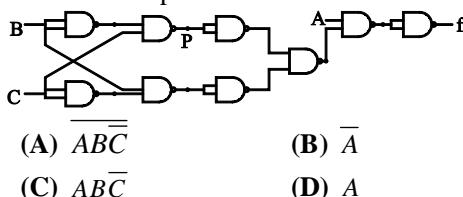
- (62) For the circuit shown below the output F is given by



- (A) $F = 1$
(C) $F = X$
(B) $F = 0$
(D) $F = \bar{X}$

[GATE -EC - 2006]

- (63) The point p in the following figure is stuck – at 1. The output f will be



- (A) \overline{ABC}
(C) ABC
(B) \bar{A}
(D) A

[GATE -EC - 1988]

- (64) Minimum number of 2-input NAND gates required to implement he function.

$$F = (\bar{X} + \bar{Y})(Z + W)$$

- (A) 3
(C) 5
(B) 4
(D) 6

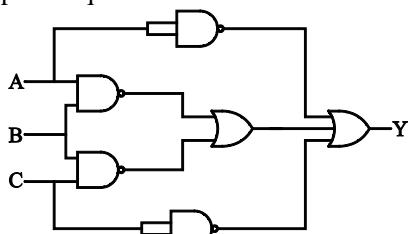
[GATE -EC - 1989]

- (65) Indicate which of the following logic gates can be used to realize all possible combinational Logic functions:

- (A) OR gates only
(B) NAND gates only
(C) EX-OR gates only
(D) NOR gates only

[GATE -EC - 1993]

- (66) For the logic circuit shown in Figure, the output is equal to



- (A) \overline{ABC}
(C) $\overline{AB} + \overline{BC} + \overline{A} + \overline{C}$
(B) $\bar{A} + \bar{B} + \bar{C}$
(D) $\overline{AB} + \overline{BC}$

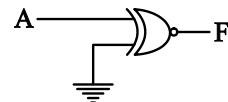
[GATE -EC - 1994]

- (67) A ring oscillator consisting of 5 inverters is running at a frequency of 1.0 MHz. The

propagation delay per gate is _____ n sec.

[GATE -EC - 1997]

- (68) The output of the logic gate in figure is



- (A) 0
(C) \bar{A}
(B) 1
(D) A

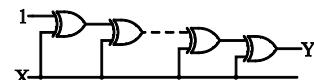
[GATE -EC - 1997]

- (69) The Boolean function $A + BC$ is a reduced form of

- (A) $AB + BC$
(B) $(A + B).(A + C)$
(C) $\overline{AB} + A\overline{BC}$
(D) $(A + C).B$

[GATE -EC - 2002]

- (70) If the input to the digital circuit (in the figure) consisting of a cascade of 20 XOR-gates is X then the output Y is equal to



- (A) 0
(C) \bar{X}
(B) 1
(D) X

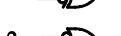
[GATE -EC - 2010]

- (71) Match the logic gates in column A with their equivalents in column B.

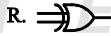
Column A



Column B



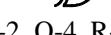
1.



2.



3.



4.

- (A) P-2, Q-4, R-1, S-3

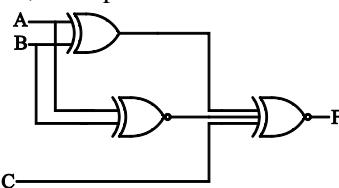
- (B) P-4, Q-2, R-1, S-3

- (C) P-2, Q-4, R-3, S-1

- (D) P-4, Q-2, R-3, S-1

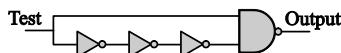
[GATE -EC - 2010]

- (72) For the output F to be 1 in the logic circuit shown, the input combination should be



- (A) $A = 1, B = 1, C = 0$
(B) $A = 1, B = 0, C = 0$

The signal TEST which was at logic LOW is switched to logic HIGH. The output



- (A) stays HIGH throughout
- (B) stays LOW throughout
- (C) pulses from LOW to HIGH to LOW
- (D) pulses from HIGH to LOW to HIGH

[GATE - EE - 2009]

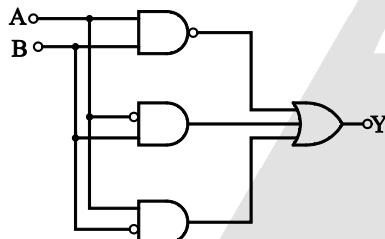
- (81) The complete set of only those Logic Gates designated as Universal gates is
- (A) NOT, OR and AND Gates
 - (B) XNOR, NOR and NAND Gates
 - (C) NOR and NAND Gates
 - (D) XOR, NOR and NAND Gates

[IES - EC - 1998]

- (82) The output of an EX-OR gate with A and B as inputs will be
- (A) $AB + \overline{AB}$
 - (B) $(A+B)(\overline{A}+\overline{B})$
 - (C) $(A+B)\overline{AB}$
 - (D) $\overline{A+B} + AB$

[IES - EC - 2008]

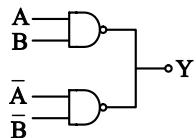
- (83) In the given circuit, the output Y equals which one of the following?



- (A) $A+B$
- (B) $\overline{AB} + A\overline{B}$
- (C) AB
- (D) $\overline{A} + \overline{B}$

[IES - EC - 1992]

- (84) The open collector wired circuit shown below functions as



- (A) EX-NOR
- (B) AND
- (C) EX-OR
- (D) NOR

[IES - EC - 1993]

- (85) The gate whose output is LOW if and only if all the inputs are HIGH, is
- (A) NAND
 - (B) NOR
 - (C) OR
 - (D) AND

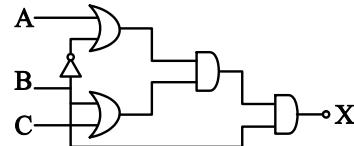
- (86) Which one of the following is equivalent to AND – OR realization?
- (A) NAND – NOR realization
 - (B) NOR – NOR realization
 - (C) NOR – NAND realization
 - (D) NAND – NAND realization

[IES - EC - 1996]

- (87) A three - input NAND gate is to be used as an inverter. Which one of the following measures will achieve better results?
- (A) The two inputs not used are kept open
 - (B) The two inputs not used are connected to ground (O level)
 - (C) The two inputs not used are connected to logic (1 level)
 - (D) None of the above

[IES - EC - 1997]

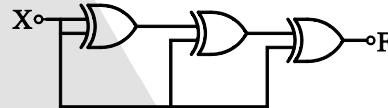
- (88) The output X of the logic circuit shown in the figure is



- (A) $A + BC$
- (B) BC
- (C) AB
- (D) $AB + C$

[IES - EC - 1999]

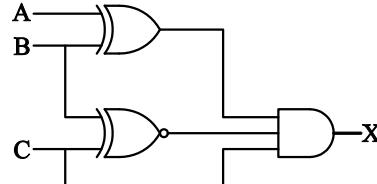
- (89) The output Y of the given circuit is



- (A) 1
- (B) zero
- (C) X
- (D) \bar{X}

[GATE - EC- 2000]

- (90) Consider the following logic circuit :



What is the required input condition (A,B,C) to make the output X = 1, for the given logic circuit?

- (A) 1,0,1
- (B) 0,0,1
- (C) 1,1,1
- (D) 0,1,1

- (91) The open collector output of two 2-input NAND gates are connected to a common pull-up resistor. If inputs of the gates are A, B and C, D respectively, then output is equal to

(A) $(A+B)(\bar{A}+C)(B+C) = (A+B)$

$$(\bar{A}+C)$$

(B) $(\bar{A}+\bar{B})(A+\bar{C})(\bar{B}+\bar{C}) = (\bar{A}+\bar{B})$

$$(A+\bar{C})$$

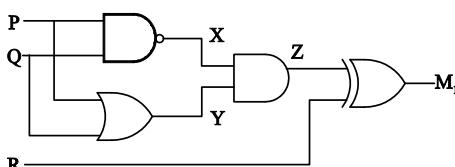
(C) $(A+B)(\bar{A}+C)(B+C) = (\bar{A}+\bar{B})$

$$(A+\bar{C})$$

(D) $\bar{A}\bar{B} + A\bar{C} + \bar{B}\bar{C} = \bar{A}\bar{B} + A\bar{C}$

[GATE – EC – 2008]

- (101) Which of the following Boolean expressions correctly represents the relation between P, Q, R and M_1 ?



(A) $M_1 = (P \text{ OR } Q) \text{ XOR } R$

(B) $M_1 = (P \text{ AND } Q) \text{ XOR } R$

(C) $M_1 = (P \text{ NOR } Q) \text{ XOR } R$

(D) $M_1 = (P \text{ XOR } Q) \text{ XOR } R$

[GATE-EC-1998]

- (102) The minimum number of 2-input NAND gates required to implement the Boolean function $Z = A\bar{B}C$, assuming that A, B and C are available, is

(A) two

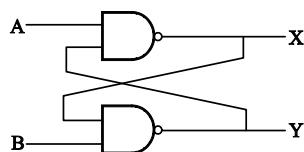
(B) three

(C) five

(D) six

[GATE – EC – 1998]

- (103) In below figure, A = 1 and B = 1. The input B is now replaced by a sequence 101010 the outputs x and y will be



(A) fixed at 0 and 1, respectively

(B) x = 1010 ----- while y = 0101 -----

(C) x = 1010 ----- and y = 1010 -----

(D) fixed at 1 and 0, respectively

[IES -EC - 2006]

- (104) The Boolean expression

$$Y(A, B, C) = A + BC$$

is to be realized using 2-input gates of only one type. What is the minimum number of gates required for the realization?

(A) 1

(B) 2

(C) 3

(D) 4 or more

[IES -EC - 2002]

- (105) How is inversion achieved using EX-OR gate?

(A) Giving input signal to the two input lines of the gate tied together

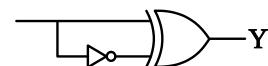
(B) Giving input to one input line and logic zero to the other line

(C) Giving input to one input line and logic one to the other line

(D) Inversion cannot be achieved using EX-OR gate

[GATE-EE-2011]

- (106) The output Y of the logic circuit given below is



(A) 1

(B) 0

(C) x

(D) \bar{x}

[GATE-S8-EE-2016]

- (107) The Boolean expression

$$\overline{(a+b+c+d)} + (b+c)$$

(A) 1

(B) $\overline{a,b}$

(C) a, b

(D) 0

[GATE-S4-IN-2016]

- (108) The Boolean expression

$$XY + (X' + Y')Z$$

(A) $XYZ' + X'Y'Z'$

(B) $X'Y'Z' + XYZ$

(C) $(X + Z)(Y + Z)$

(D) $(X' + Z)(Y' + Z)$

[GATE-S4-EC-2016]

- (109) Following is the K-map of a Boolean function of five variables P, Q, R, S and X. The minimum sum-of-product (SOP) expression for the function is :

PQ	00	01	11	10
RS	00	0	0	0
	01	1	0	1
	11	1	0	1
	10	0	0	0

$X=0$

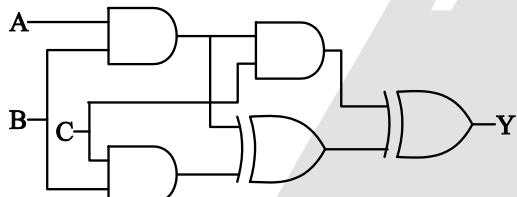
PQ	00	01	11	10
RS	00	0	1	0
	01	0	0	0
	11	0	0	0
	10	0	1	0

$X=1$

- (A) $\bar{P}\bar{Q}S\bar{X} + P\bar{Q}\bar{S}\bar{X} + Q\bar{R}\bar{S}X + QR\bar{S}X$
 (B) $\bar{Q}S\bar{X} + Q\bar{S}X$
 (C) $\bar{Q}SX + Q\bar{S}X$
 (D) $\bar{Q}S + Q\bar{S}$

[GATE-S1-EC-2016]

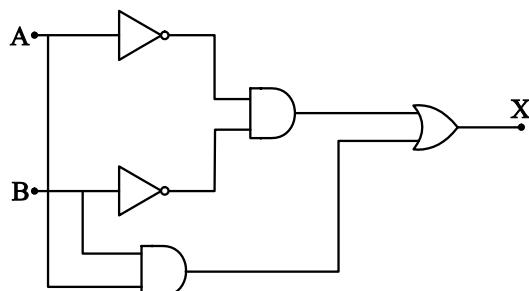
- (110) The output of the combinational circuit given below is :



- (A) $A+B+C$ (B) $A(B+C)$
 (C) $B(C+A)$ (D) $C(A+B)$

[GATE - IN - 2017]

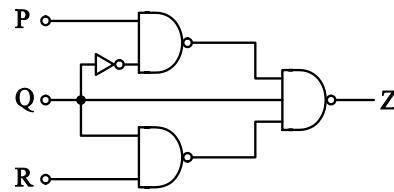
- (111) A and B are the logical inputs and X is the logical shown in the figure. The output X is related to A and B by



- (A) $X = \bar{A}B + \bar{B}A$ (B) $X = AB + \bar{B}A$
 (C) $X = AB + \bar{A}\bar{B}$ (D) $X = \bar{A}\bar{B} + \bar{B}A$

[GATE-S2-EE-2017]

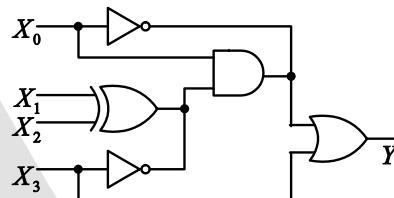
- (112) For a 3-input logic circuit shown, the output Z can be expressed as



- (A) $Q + \bar{R}$ (B) $P\bar{Q} + R$
 (C) $\bar{Q} + R$ (D) $P + \bar{Q} + R$

[GATE – EC – 2018]

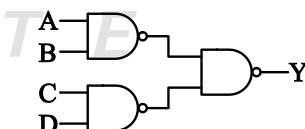
- (113) The logic gates shown in the digital circuit below use strong pull-down nMOS transistors for LOW logic level at the outputs. When the pull-downs are off, high-value resistors set the output logic levels to HIGH (i.e. the pull-ups are weak). Note that some nodes are intentionally shorted to implement “wired logic”. Such shorted nodes will be HIGH only if the outputs of all the gates whose outputs are shorted are HIGH.



The number of distinct values of $X_3X_2X_1X_0$ (out of the 16 possible values) that give $Y=1$ is _____.

[GATE – EE – 2018]

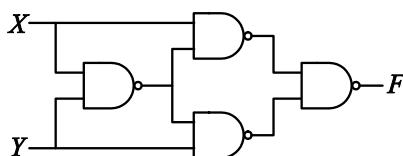
- (114) In the logic circuit shown in the figure, Y is given by



- (A) $Y = ABCD$
 (B) $Y = (A + B)(C + D)$
 (C) $Y = A + B + C + D$
 (D) $Y = AB + CD$

[GATE – IN – 2018]

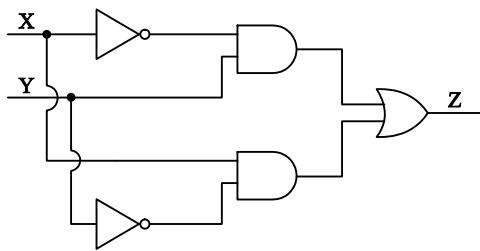
- (115) The Boolean function $F(X, Y)$ realized by the given circuit is



- (A) $\bar{X}Y + XY$ (B) $\bar{X}\bar{Y} + XY$
 (C) $X + Y$ (D) $\bar{X} \cdot \bar{Y}$

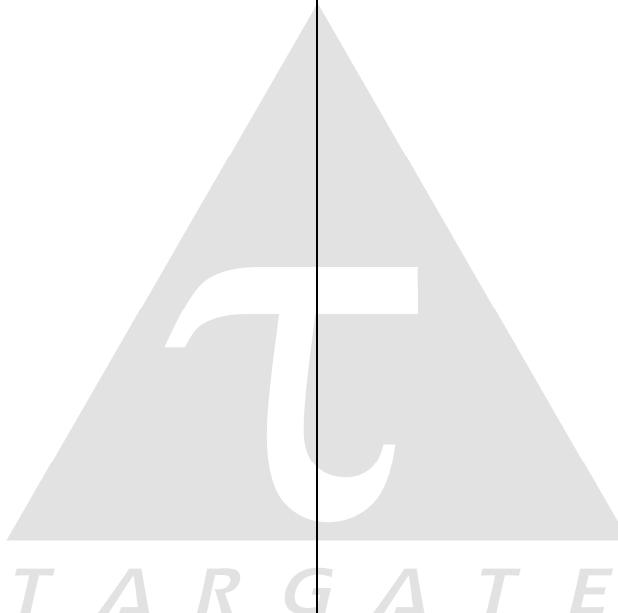
[GATE-EE-2019]

- (116) In the circuit shown below, X and Y are digital inputs, and Z is a digital output. The equivalent circuit is a



- (A) XOR gate (B) NOR gate
(C) XNOR gate (D) NAND gate

-----0000-----



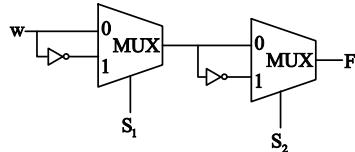
04

Combinational Digital Circuits

4.1 Multiplexer

[GATE – EC – 2014]

- (1) Consider the multiplexer based logic circuit shown in the figure. Which one of the following Boolean functions is realized by the circuit?



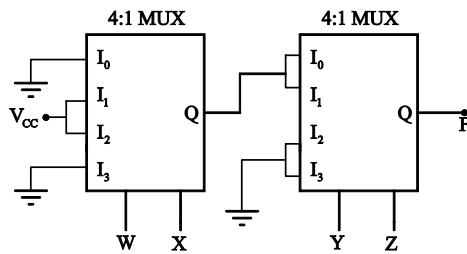
- (A) $F = W \bar{S}_1 \bar{S}_2$
- (B) $F = WS_1 + WS_2 + S_1 S_2$
- (C) $F = W + S_1 + S_2$
- (D) $F = W \oplus S_1 \oplus S_2$

[IES -EC - 2006]

- (2) What is the number of selector lines required in a single input n-output de-multiplexer?
- (A) 2
 - (B) n
 - (C) 2^n
 - (D) $\log_2 n$

[GATE – EC – 2014]

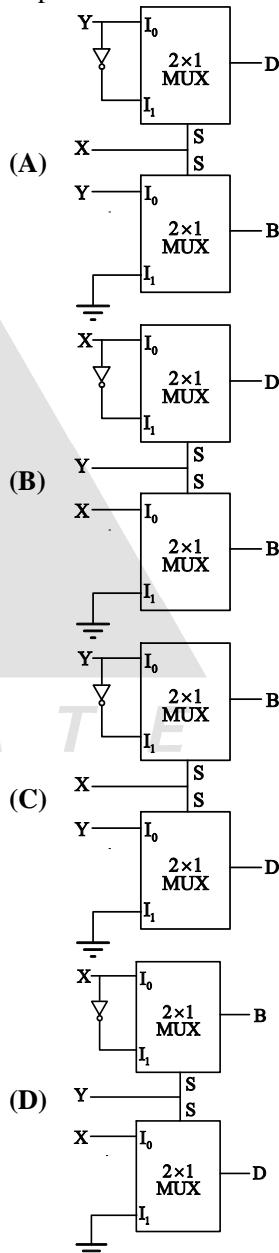
- (3) In the circuit shown, W and Y are MSBs of the control inputs. The output F is given by



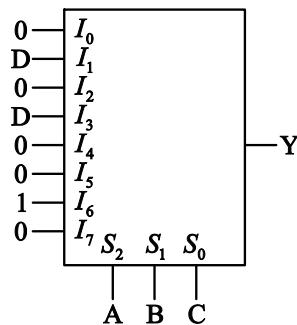
- (A) $F = W \bar{X} + \bar{W} X + \bar{Y} Z$
- (B) $F = W \bar{X} + \bar{W} X + \bar{Y} Z$
- (C) $F = W \bar{X} \bar{Y} + \bar{W} X \bar{Y}$
- (D) $F = (\bar{W} + \bar{X}) \bar{Y} \bar{Z}$

[GATE – EC – 2014]

- (4) If X and Y are inputs and the Difference (D) = $X - Y$ and the Borrow (B) are the outputs, which one of the following diagrams implements a half subtractor?



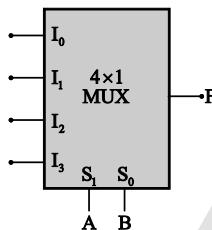
- (5) An 8-to-1 multiplexer is used to implement a logical function Y as shown in the figure. The output Y is given by



- (A) $Y = \overline{ABC} + \overline{ACD}$
(B) $Y = \overline{ABC} + \overline{ABD}$
(C) $Y = ABC\bar{C} + \overline{ACD}$
(D) $Y = \overline{ABD} + A\bar{B}\bar{C}$

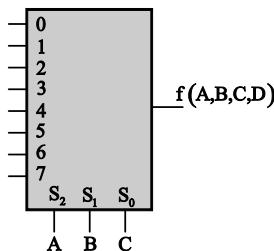
[GATE – EE – 2015]

- (6) In the 4×1 multiplexer, the output F is given by $F = A \oplus B$. Find the required input $I_3 I_2 I_1 I_0$



[GATE – EE – 2015]

- (7) A Boolean function $f(A,B,C,D) = \prod_{i=1}^4 (1,5,12,15)$ is to be implemented using an 8×1 multiplexer (A is MSB). The inputs ABC are connected to the select inputs $S_2 S_1 S_0$ of the multiplexer respectively.



Which one of the following options gives the correct inputs to pins 0,1,2,3,4,5,6,7 in order?

- (A) D, 0, D, 0, 0, 0, \bar{D} , D
 (B) \bar{D} , 1, \bar{D} , 1, 1, 1, D, \bar{D}

- (C) D, 1, D, 1, 1, 1, \bar{D} , D

- (D) \bar{D} , 0, \bar{D} , 0, 0, 0 D, \bar{D}

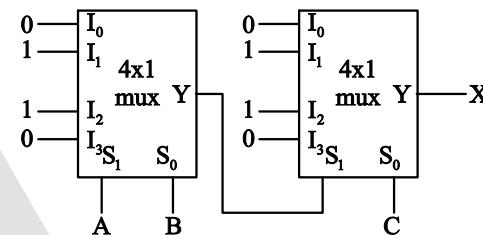
[GATE -EC - 2003]

- (8) Without any additional circuitry, an 8:1 MUX can be used to obtain

 - (A) some but not all Boolean Functions of 3 variables
 - (B) all functions of 3 variables but none of 4 variables
 - (C) all functions of 3 variables and some but not all of 4 variables
 - (D) all functions of 4 variables

[GATE -EC -2010]

- (9) In the following circuit, X is given by



- (A)** $X = \overline{ABC} + \overline{ACB} + \overline{BAC} + ABC$

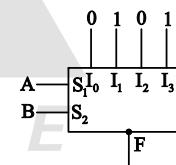
(B) $X = \overline{ABC} + \overline{ACB} + \overline{BCA} + ABC$

(C) $X = AB + BC + AC$

(D) $X = \overline{AB} + \overline{BC} + \overline{AC}$

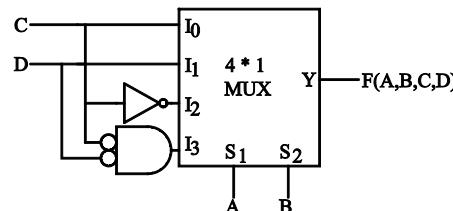
[IES – EC – 1998]

- (10) The function 'F' implemented by the multiplexer chip shown in the figure is :



[GATE -EC - 2010]

- (11) The Boolean function realized by the logic circuit shown is



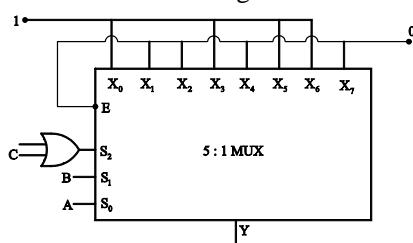
- (B) $F = \sum m(2,3,5,7,8,12,13)$

(C) $F = \sum m(1, 2, 4, 5, 11, 14, 15)$

(D) $F = \sum m(2, 3, 5, 7, 8, 9, 12)$

[IES - EC - 2004]

- (12) Consider the following circuit:



In the given TTL circuit, S_2 and S_0 are select lines and X_7 to X_0 are LBSs. What is the output Y?

- (A) Indeterminate
- (B) $A \oplus B$
- (C) $\overline{A \oplus B}$
- (D) $\overline{C \oplus B \oplus A}$

[IES - EC - 2008/2013]

- (13) A digital multiplexer can be used for which of the following?

1. Parallel to serial conversion
2. Many-to-one switch
3. To generate memory chip select
4. For code conversion

Select the correct answer using the code given below:

- (A) 1, 3 and 4
- (B) 2, 3 and 4
- (C) 1 and 2 only
- (D) 2 and 3 only

[IES - EC - 2009]

- (14) Consider a multiplexer with X and Y as data inputs and Z as control input. Z = 0 selects input X and Z = 1 selects input Y. What are the connections required to realize the 2-variable Boolean function $f = T + R$, without using any additional hardware?

- (A) R to X, 1 to Y, T to Z
- (B) T to X, R to Y, T to Z
- (C) T to X, R to Y, 0 to Z
- (D) R to X, 0 to Y, T to Z

[IES - EC - 2010]

- (15) Consider the following statements:

1. A multiplexer is analogous to a rotary switch.

2. A decoder is a combinational logic circuit that converts binary information from 'n' input lines to a maximum of 2^n distinct elements at the output.

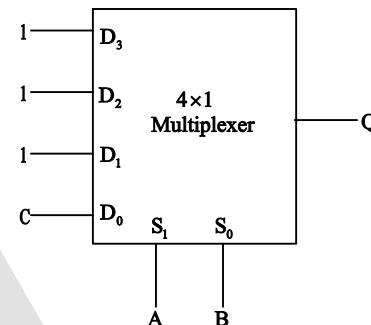
3. The Boolean expression for the output difference 'D' from a full subtractor is exactly the same as the output sum 'S' from a full adder.

Which of the above statements is/are correct?

- (A) 2 and 4 only
- (B) 4 only
- (C) 1 and 3 only
- (D) 1, 2 and 3

[GATE - IN - 1995]

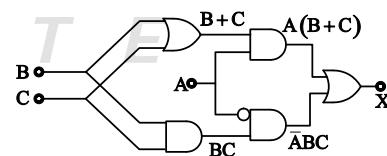
- (16) The combinatorial circuit shown in Figure employs a 4 to 1 multiplexer. The output Q of the circuit is



- (A) $\overline{A} \overline{B} C$
- (B) $A + B + C$
- (C) $A \oplus B \oplus C$
- (D) \overline{ABC}

[GATE - IN - 2001]

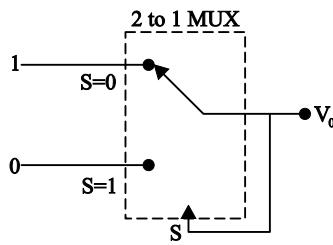
- (17) In the logic circuit shown in Fig. the output x is



- (A) $A \overline{B} + B \overline{C} + C \overline{A}$
- (B) $A + B + C$
- (C) $AB + BC + CA$
- (D) $\overline{AB} + \overline{BC} + \overline{CA}$

[GATE - IN - 2003]

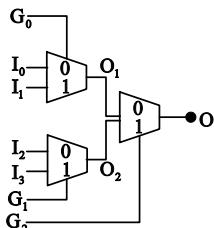
- (18) A 2-to 1 digital multiplexer having a switching delay of $1 \mu s$ is connected as shown in Fig. The output of the multiplexer is tied to its own select input S. The inputs which gets selected when S = 0 is tied to 1 and the input that is selected when S = 1 is tied to 0. The output V0 will be



- (A) 0
 (B) 1
 (C) pulse train of frequency 0.5 MHz
 (D) pulse train of frequency 1.0 MHz

[GATE - IN - 2005]

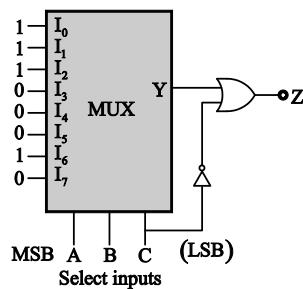
- (19) The cell of a field programmable Gate array is shown in the figure. It has three 2-to-1 – multiplexers with their select lines G_0, G_1, G_2 and 4 digital signal input lines I_0, I_1, I_2 and I_3 ,.. The logical function that relates the output O to the select and signal input lines is



- (A) $\overline{G}_0 \overline{G}_1 I_2 + \overline{G}_0 G_1 I_3 + \overline{G}_2 \overline{G}_1 I_0 + \overline{G}_2 G_1 I_1$
 (B) $\overline{G}_0 I_2 + \overline{G}_0 G_1 + \overline{G}_2 I_0 + \overline{G}_2 G_1 I_1 + G_0$
 (C) $\overline{G}_0 \overline{G}_2 I_0 + G_0 \overline{G}_2 I_1 + G_2 \overline{G}_1 I_2 + G_2 G_1 I_3$
 (D) $G_2 G_1 \overline{I}_2 + \overline{G}_2 \overline{G}_1 \overline{I}_3 + G_2 \overline{G}_0 I_0 + G_0 \overline{G}_2 I_1$

[GATE - IN - 2006]

- (20) A combinational circuit using a 8-to-1 multiplexer is shown in the following figure. The minimized expression for the output (Z) is :

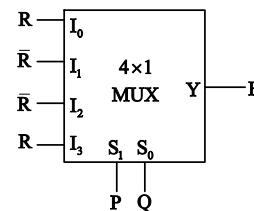


- (A) $C(\overline{A} + \overline{B})$
 (B) $C(A + B)$

- (C) $\overline{C} + \overline{AB}$
 (D) $\overline{C} + AB$

[GATE - IN - 2008]

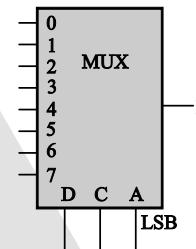
- (21) The output F of the multiplexer circuit shown below expressed in terms of the input P, Q and R is



- (A) $F = P \oplus Q \oplus R$
 (B) $F = PQ + QR + RP$
 (C) $F = (P \oplus Q)R$
 (D) $F = (P \oplus Q)\overline{R}$

[GATE - EE - 1999]

- (22) The logic function $F = AC + ABD + ACD$ is to be realized using an 8 to 1 multiplexer shown in the figure, using A, C and D as control inputs.

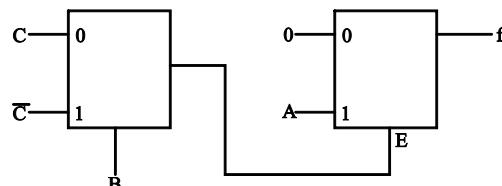


- (A) Indicate the inputs to be applied at the terminals 0 to 7.
 (B) Can the function be realized using a 4 to 1 multiplexer?

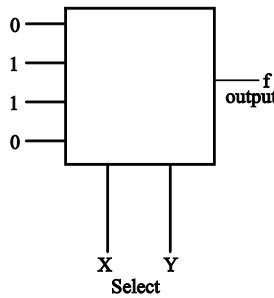
State YES or NO.

[GATE - EC - 2005]

- (23) The Boolean function f implemented in the figure using two input multiplexers is :



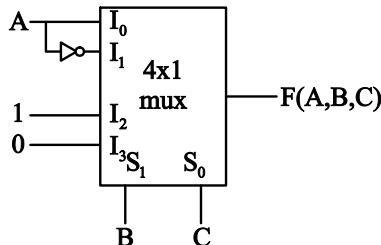
- (A) $A\overline{B}C + A\overline{B}\overline{C}$
 (B) $ABC + A\overline{B}C$
 (C) $\overline{ABC} + \overline{ABC}$
 (D) $\overline{ABC} + \overline{A}B\overline{C}$



- (A) An EXOR gate
 (B) A NOR gate
 (C) An NAND gate
 (D) A NOR gate

[GATE – EE – 2006]

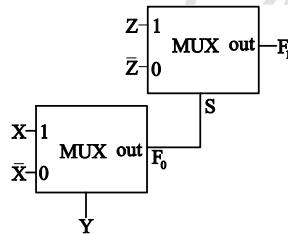
- (33) A 4×1 MUX is used to implement a 3-input Boolean function as shown below. The Boolean function $F(A, B, C)$ implemented is



- (A) $F(A, B, C) = \sum(1, 2, 4, 6)$
 (B) $F(A, B, C) = \sum(1, 2, 6)$
 (C) $F(A, B, C) = \sum(2, 4, 5, 6)$
 (D) $F(A, B, C) = \sum(1, 5, 6)$

[GATE - IN - 2007]

- (34) A MUX circuit shown in the figure below implements a logic function F_1 . the correct expression for F_1 is



- (A) $(\overline{X \oplus Y}) \oplus Z$ (B) $(\overline{X \oplus Y}) \oplus \overline{Z}$
 (C) $(X \oplus Y) \oplus \overline{Z}$ (D) $(X \oplus Y) \oplus Z$

[IES – EE – 1995]

- (35) Assertion (A) : A digital multiplexer can also be used to implement combinational logic functions.

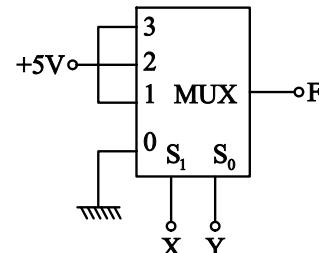
Reason (R) : In a combinational circuit, the current output depends on the previous outputs also.

Codes:

- (A) Both A and R are true and R is the correct explanation of A.
 (B) Both A and R are true but R is not the correct explanation of A
 (C) A is true but R is false
 (D) A is false but R is true

[GATE - EE - 2001]

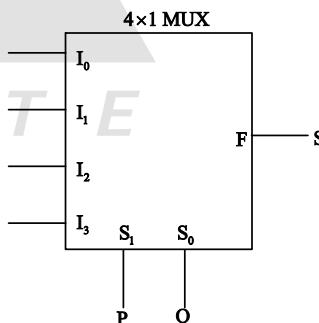
- (36) The output f of the 4-to-1 MUX shown in fig. is



- (A) $\overline{xy} + x$ (B) $x + y$
 (C) $\overline{x} + \overline{y}$ (D) $xy + \overline{x}$

[GATE - EE - 2003]

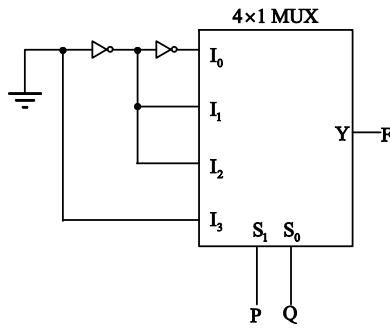
- (37) Figure shows a 4 to 1 MUX to be used to implement the sum S of a 1-bit full adder with input bits P and Q and the carry input C_{in} . Which of the following combinations of inputs to I_0, I_1, I_2 and I_3 of the MUX will realize the sum S?



- (A) $I_0 = I_1 = C_{in}; I_2 = I_3 = \overline{C_{in}}$
 (B) $I_0 = I_1 = \overline{C_{in}}; I_2 = I_3 = C_{in}$
 (C) $I_0 = I_3 = C_{in}; I_1 = I_2 = \overline{C_{in}}$
 (D) $I_0 = I_3 = \overline{C_{in}}; I_1 = I_2 = C_{in}$

[GATE - EC - 2011]

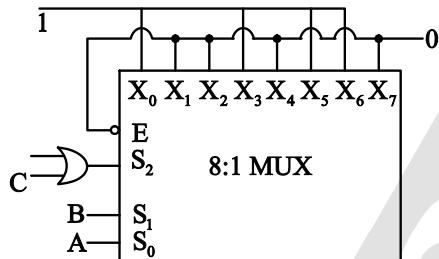
- (38) The logic function implemented by the circuit below is (ground implies a logic “0”)



- (A) $F = \text{AND}(P, Q)$
 (B) $F = \text{OR}(P, Q)$
 (C) $F = \text{XNOR}(P, Q)$
 (D) $F = \text{XOR}(P, Q)$

[GATE -EC - 2001]

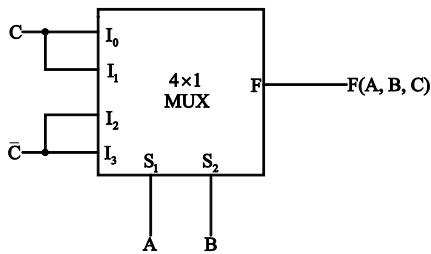
- (39) In the TTL circuit in the figure, S_2 and S_0 are select lines and X_7 and X_0 are input lines. S_0 and X_0 are LSB's. What is the output Y ?



- (A) Indeterminate
 (B) $A \oplus B$
 (C) $\overline{A \oplus B}$
 (D) $\bar{C}(\overline{A \oplus B}) + C(A \oplus B)$

[GATE -EC - 1992]

- (40) The logic realized by the circuit shown in figure is



- (A) $F = A \odot C$
 (B) $F = A \oplus C$
 (C) $F = B \odot C$
 (D) $F = B \oplus C$

[IES -EC - 2000]

- (41) Consider the following statements A Multiplexer

1. Selects one of the several inputs and transmits it to a single output
2. Routes the data from a single input to one of many output

3. Converts parallel data into serial data

4. Is a combinational circuit

Which of these statements are correct?

- (A) 1, 2 and 4 (B) 2, 3 and 4
 (C) 1, 3 and 4 (D) 1, 2 and 3

[IES -EC - 2007]

- (42) When two 16-input multiplexers drive a 2-input MUX, what is the result?

- (A) 2-input MUX
 (B) 4-input MUX
 (C) 16-input MUX
 (D) 32-input MUX

[IES -EC - 1996]

- (43) A 4-input multiplexer can be used to implement

- (A) Four combinational functions of 2-variables each
 (B) Two combinational functions of 4-variables each
 (C) One combinational function of 4-variables
 (D) One combinational function of 3-variables

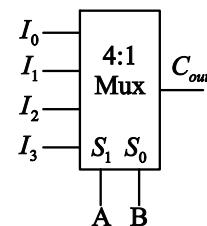
[IES -EC - 2000]

- (44) Which one of the following can be used as parallel to serial converter ?

- (A) Decoder
 (B) Digital counter
 (C) Multiplexer
 (D) De-multiplexer.

[GATE-S3-EC-2016]

- (45) A 4:1 multiplexer is to be used for generating the output carry of a full adder. A and B are the bits to be added while Cin is the input carry and Cout is the output carry. A and B are to be used as the select bits with A being the more significant select bit.



Which one of the following statements correctly describes the choice of signals to be connected to the inputs I_0 , I_1 , I_2 and I_3 so that the output is C_{out} ?

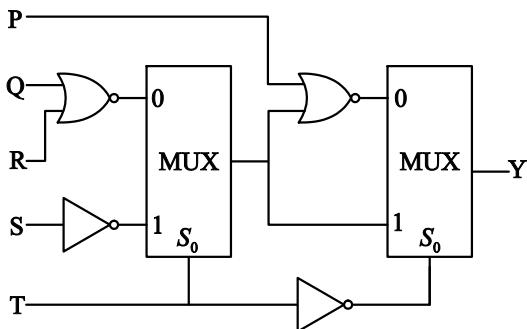
- (A) $I_0=0$, $I_1=C_{in}$, $I_2=C_{in}$ and $I_3=1$
 (B) $I_0=1$, $I_1=C_{in}$, $I_2=C_{in}$ and $I_3=1$

(C) $I_0=C_{in}$, $I_1=0$, $I_2=1$ and $I_3=C_{in}$

(D) $I_0=0$, $I_1=C_{in}$, $I_2=1$ and $I_3=C_{in}$

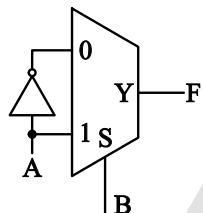
[GATE-S4-EC-2016]

- (46) For the circuit shown in the figure, the delays of NOR gates, multiplexers and inverters are 2 ns, 1.5 ns and 1 ns, respectively. If all the inputs P, Q, R, S and T are applied at the same time instant, the maximum propagation delay (in ns) of the circuit is _____



[GATE-S6-EE-2016]

- (47) Consider the following circuit which uses a 2-to-1 multiplexer as shown in the figure below. The Boolean expression for output F in terms of A and B is :



(A) $A \oplus B$

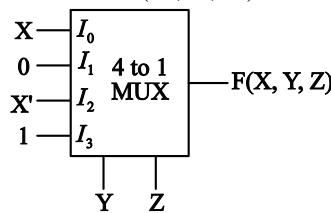
(B) $\overline{A + B}$

(C) $A + B$

(D) $\overline{A \oplus B}$

[GATE-S4-IN-2016]

- (48) A 4 to 1 multiplexer to realize a Boolean function F (X, Y, Z) is shown in the figure below. The inputs Y and Z are connected to the selectors of the MUX (Y is more significant). The canonical sum-of-product expression for F (X, Y, Z) is



(A) $\Sigma m(2,3,4,7)$

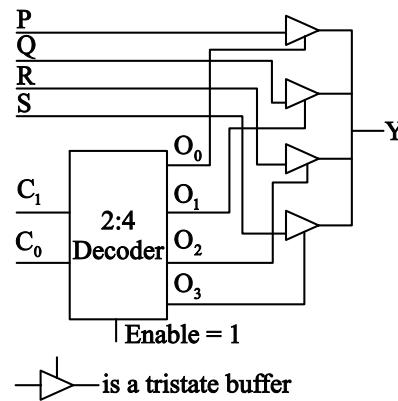
(B) $\Sigma m(1,3,5,7)$

(C) $\Sigma m(0,2,4,6)$

(D) $\Sigma m(2,3,5,6)$

[GATE-S1-EC-2016]

- (49) The functionality implemented by the circuit below is :



(A) 2-to-1 multiplexer

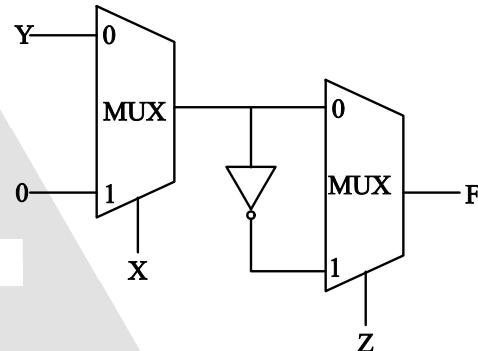
(B) 4-to-1 multiplexer

(C) 7-to-1 multiplexer

(D) 6-to-1 multiplexer

[GATE-S2-EC-2017]

- (50) Consider the circuit shown in the figure.



The Boolean expression F implemented by the circuit is

(A) $\bar{X}\bar{Y}\bar{Z} + XY + \bar{Y}Z$

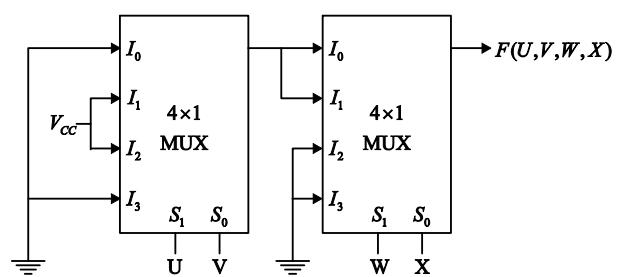
(B) $\bar{X}YZ + XZ + \bar{Y}Z$

(C) $\bar{X}Y\bar{Z} + XY + \bar{Y}Z$

(D) $\bar{X}\bar{Y}\bar{Z} + XZ + \bar{Y}Z$

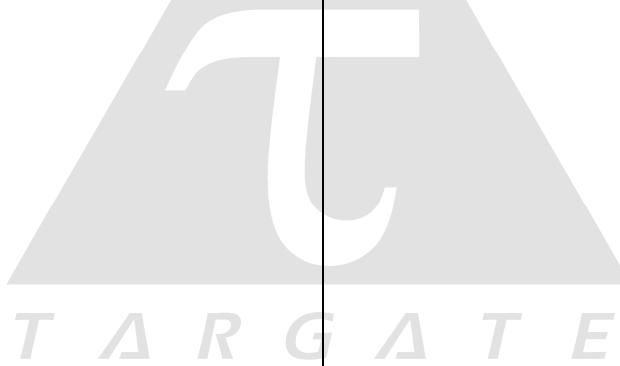
[GATE-EC-2018]

- (51) A four-variable Boolean function is realized using 4×1 multiplexers as shown in the figure.



The minimized expression for $F(U, V, W, X)$ is

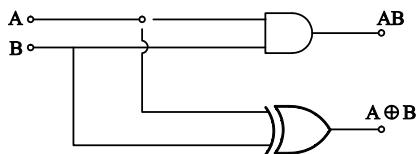
- (A) $(UV + \bar{U}\bar{V})\bar{W}$
- (B) $(UV + \bar{U}\bar{V})(\bar{W} \bar{X} + \bar{W} X)$
- (C) $(U\bar{V} + \bar{U}V)\bar{W}$
- (D) $(U\bar{V} + \bar{U}V)\bar{W} \bar{X} + \bar{W} X$



4.2 Adder

[IES – EE – 1995]

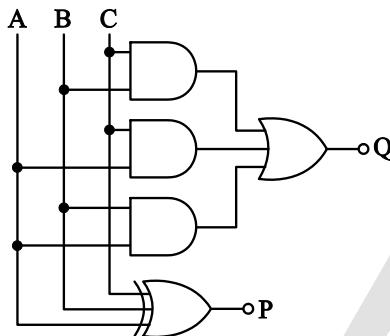
- (1) The logic circuit given in the figure represents a



- (A) Full adder
- (B) Half adder
- (C) Half subtractor
- (D) Boolean multiplier

[GATE-IN-2004]

- (2) In the circuit of figure A, B, C are the inputs and P, Q are the two outputs. The circuit is a



- (A) half adder where P is the sum and Q is the carry
- (B) half adder where P is the carry and Q is the sum
- (C) full adder where P is the sum and Q is the carry
- (D) full adder where P is the carry and Q is the sum

[GATE - IN - 2005]

- (3) Notwithstanding over flow, the addition the subtraction of K-bit signed binary numbers can be realized using One K-bit full adder and

- (A) 2 – input AND gates
- (B) 2 – input NOR gates
- (C) 2 – input OR gates
- (D) 2 – input XOR gates

[IES -EC - 2000]

- (4) Which one of the following statements correctly defines the full adder?

- (A) Having two inputs used to add two binary digits. It produces their sum and carries as input

(B) Having three inputs used to add two binary digits. It produces their sum and carries as outputs

(C) Used in the least significant position when adding two binary digits with no carry – in to consider. If produces their sum and carry as outputs

(D) Having two inputs and two output.

[IES -EC - 1996]

- (5) Which one of the following statements is correct?

(A) In serial adder, if d and D, respectively, are the full adder and flip – flop delay, then the time required to perform n bit addition is $[n(d+D)]$

(B) Maximum delay in n bit parallel adder is ‘nd’ where d is delay of full adder

(C) If d is the delay of two – level circuit, and then the total delay of a carry look ahead adder is only 3d.

(D) none of the above

[IES – EE – 1997]

- (6) In a half - adder having two inputs A and B and two outputs, (S and C are the Sum and carry output bits respectively) , the Boolean expressions for S and C in terms of A and B is

$$(A) S = \bar{A}B + A\bar{B}; C = A.B$$

$$(B) S = AB + \bar{A}\bar{B}; C = A + B$$

$$(C) S = \bar{A}\bar{B} + AB; C = A + \bar{B}$$

$$(D) S = \bar{A} + A\bar{B}; C = \bar{A} + B$$

[GATE -EC - 1997]

- (7) A 2-bit binary multiplier can be implemented using

(A) 2 input ANDs only

(B) 2 input XORs and 4-input AND gates only.

(C) Two (2) input NORs and one XNOR gate.

(D) XOR gates and shift registers.

[GATE -EC - 2014]

- (8) In a half-subtractor circuit with X and Y input the Borrow (M) and difference (N = X - Y) are given by

$$(A) M = X \oplus Y, N = XY$$

$$(B) M = XY, N = X \oplus Y$$

- (C) $M = \bar{X}Y, N = X \oplus Y$
 (D) $M = X\bar{Y}, N = \overline{X \oplus Y}$

[IES -EC - 1994]

- (9) A combinational circuit is one in which the output depends on the
 (A) Input combination at that time
 (B) Input combination and the previous output
 (C) Input combination at the time and the previous input combination
 (D) Present output and the previous outputs

[GATE -EC - 1999]

- (10) For a binary half-subtractor having two inputs A and B, the correct sets of logical expressions for the outputs D (= A minus B) and X (= borrow) are
 (A) $D = AB + \bar{A}\bar{B}, X = \bar{A}B$
 (B) $D = \bar{A}\bar{B} + A\bar{B}, X = A\bar{B}$
 (C) $D = \bar{A}\bar{B} + A\bar{B}, X = \bar{A}B$
 (D) $D = AB + \bar{A}\bar{B}, X = A\bar{B}$

[IES – EE – 2008]

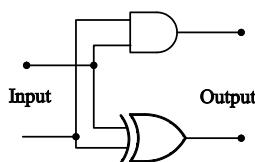
- (11) Match List -I (function/ circuit) with List -II (circuit realization) and select the correct answer using the codes given below the Lists:

List - I

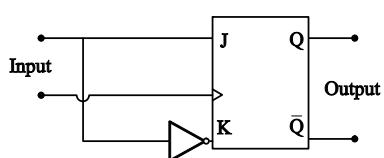
- A. D - flip flop
 B. T - flip flop
 C. Exclusive OR
 D. Half adder

List - II

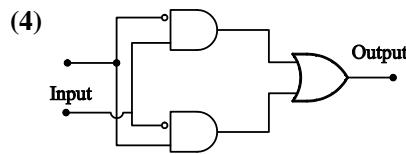
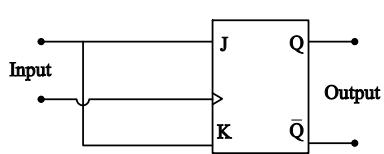
(1)



(2)



(3)



Codes :

A	B	C	D
(A) 2	3	1	4
(B) 2	3	4	1
(C) 3	2	4	1
(D) 3	2	1	4

[IES – EC – 1993]

- (12) A carry look ahead adder is frequency used for addition because it
 (A) Is faster
 (B) Is more accurate
 (C) Used fewer gates
 (D) Costs less

[IES -EC - 2003]

- (13) The addition of two binary variables A and B results into a SUM and a carry output. Consider the following expressions for the SUM and CARRY outputs:

1. $\text{SUM} = A.B + \bar{A}\bar{B}$
2. $\text{SUM} = A\bar{B} + \bar{A}.B$
3. $\text{CARRY} = A.B$
4. $\text{CARRY} = A + B$

Which of these expressions are correct?

- | | |
|-------------|-------------|
| (A) 1 and 3 | (B) 2 and 3 |
| (C) 2 and 4 | (D) 1 and 4 |

[GATE - IN - 2005]

- (14) A combinational logics circuit has three inputs A, B and C and one output Y. The output $Y = 1$ when at least two inputs are 1. Otherwise, $Y = 0$. in its minimized SOP realization, the maximum number of two input terms is

- | | |
|-------|-------|
| (A) 1 | (B) 2 |
| (C) 3 | (D) 4 |

[IES – EC – 1994]

- (15) A full – adder can be implemented with half – address and OR gates. A 4 – bit parallel full adder without any initial carry requires
 (A) 8 half – address, 4 OR gates
 (B) Three bit parity checker
 (C) 7 half – address, 4 – OR gates
 (D) 7 half – address, 3 OR gates

[IES – EC – 1994]

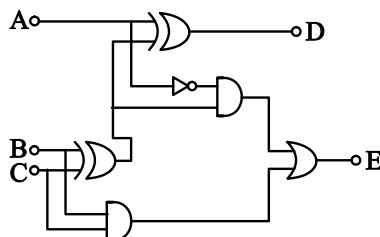
- (16) Which one of the following will give the sum of full adder as output?
- Three input majority circuit
 - Three bit parity checker
 - Three bit comparator
 - Three bit counter

[IES – EC – 1997]

- (17) A full – adder can be made out of
- Two half – address
 - Two half – address and a NOT gate
 - Two half – address and an OR gate
 - Two half – address and an AND gate

[IES – EC – 1998]

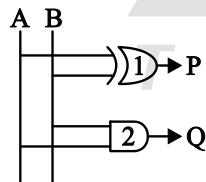
- (18) The circuit shown in the given is a



- Full adder
- Full subtractor
- Shift register
- Decade counter

[IES – EC – 2000]

- (19) The half – adder circuit in the given figure has inputs AB = 11



The logic level of P and Q outputs will be :

- P = 0 and Q = 0
- P = 0 and Q = 1
- P = 1 and Q = 0
- P = 1 and Q = 1

[IES – EC – 2005]

- (20) A 1-bit full adder takes 20ns to generate carry-out bit and 40ns for the sum bit. What is the maximum rate of addition per second when four 1-bit full adders are cascade?

- 10^7
- 1.25×10^7
- 6.25×10^6
- 10^5

[IES – EC – 2005]

- (21) Which one of the following statements is not correct?
- A full adder can be constructed using two half-adders and an OR gate.
 - Two Four bit parallel adders can be cascaded to construct 8-bit parallel adder.
 - Ripple carry adder has addition time independent of the number of bits.
 - Carry lock ahead is used to speed up the parallel addition.

[IES – EC – 2007]

- (22) Consider the following statements:

For 3 input variables $a,b,c; a$ Boolean function $y = ab + bc + ca$ represents

- a 3-input majority gate
- a 3-input majority gate
- Carry output of a full adder
- Product circuit for a,b and c

Which of the above statements are correct?

- 1 and 4 only
- 2 and 3 only
- 1 and 3 only
- 3 and 4 only

[IES – EC – 2009]

- (23) Which of the following circuits come under the class of combinational logic circuits?

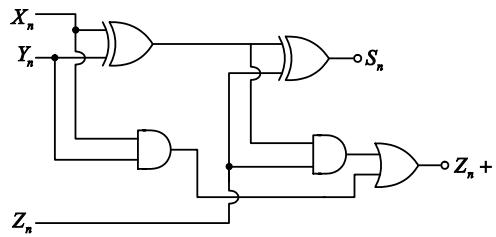
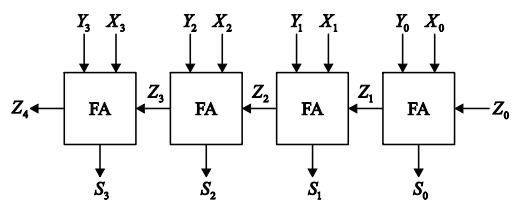
- Full adder
- Full subtractor
- Half adder
- J-K flip-flop
- Counter

Select the correct answer from the codes given below:

- | | |
|-------------|----------------|
| (A) 1 only | (B) 3 and 4 |
| (C) 4 and 5 | (D) 1, 2 and 3 |

[GATE-S2-EC-2017]

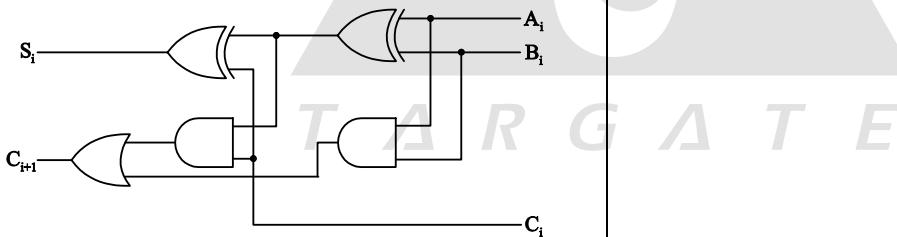
- (24) Figure I shows a 4-bit ripple carry adder realize using full adders and Figure II shows the circuit of a full-adder (FA). The propagation delay of the XOR, AND and OR gates in Figure II are 20 ns, 15 ns and 10 ns, respectively. Assume all the inputs to the 4-bit adder are initially reset to 0.



At $t = 0$, the inputs to the 4-bit adder are changed to $X_3 X_2 X_1 X_0 = 1100$, $Y_3 Y_2 Y_1 Y_0 = 0100$ and $Z_0 = 1$. The output of the ripple carry adder will be stable at t (in ns) = _____.

[GATE-IN-2019]

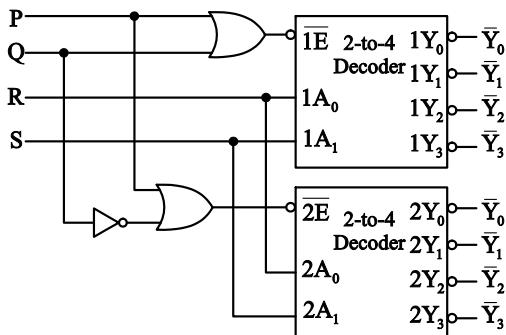
- (25) The figure below shows that i^{th} full-adder block of a binary adder circuit. C_i is the input carry and C_{i+1} is the output carry of the circuit. Assuming that each logic gate has a delay of 2 nanosecond, with no additional time delay due to the interconnecting wires. If the inputs A_i , B_i are available and stable throughout the carry propagation, the maximum time taken for an input C_i to produce a steady-state output C_{i+1} is _____ nanosecond.



4.3 Decoder

[GATE – EC – 2015]

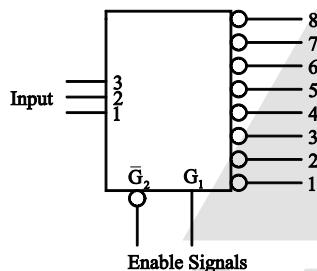
- (1) A 1-to-8 demultiplexer with data input D_{in} , address inputs S_0, S_1, S_2 (with S_0 as the LSB) and \bar{Y}_0 to \bar{Y}_7 as the eight demultiplexed outputs, is to be designed using two 2-to-4 decoders (with enable input E and address inputs A_0 and A_1) as shown in the figure. D_{in}, S_0, S_1 and S_2 are to be connected to P,Q,R and S, but not necessarily in this order. The respective input connections to P,Q,R and S terminals should be :



- (A) S_2, D_{in}, S_0, S_1
 (B) S_1, D_{in}, S_0, S_2
 (C) D_{in}, S_0, S_1, S_2
 (D) D_{in}, S_2, S_0, S_1

[IES – EE – 2002]

- (2) A 3-to-8 decoder is shown below:



All the output lines of the chip will be high, when all the inputs 1, 2 and 3

- (A) Are high; and G_1, G_2 are low
 (B) Are high; and G_1 is low, G_2 is high
 (C) Are low; and G_1 is low, G_2 is high
 (D) Are high; and G_1 is high, G_2 is low

[IES – EC – 2001]

- (3) The number of 4-line-to-16-line decoders required to make an 8-line-to-256-line decoder is

- (A) 16
 (B) 17
 (C) 32
 (D) 64

[IES -EC - 1999]

- (4) A system accepts an M-bit word and establishes the state '1' on one and only one of 2^M output line is called

(A) Decoder

(B) de-multiplexer

(C) Multiplexer

(D) Encoder

[IES -EC - 2010]

- (5) With which decoder it is possible to obtain many code conversions ?

- (A) 2 line to 4 line
 (B) 3 line to 8 line
 (C) Not possible with any decoder
 (D) 4 line to 16 line decoder

[IES – EC – 2005]

- (6) Consider the following statements:

A 4:16 decoder can be constructed (with enable input) by

- Using four 2:4 decoders (each with an enable input) only.
- Using five 2:4 decoders (each with an enable input) only.
- Using two 3:8 decoders (each with an enable input) only.
- Using two 3:8 decoders (each with an enable input) and an inverter.

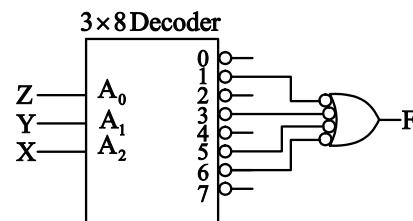
Which of the statements given above is/are correct ?

- (A) 1 only
 (B) 1 only
 (C) 2 and 4
 (D) None

[GATE - EE - 2008]

- (7) A 3 line to 8 line decoder, with active low outputs, is used to implement a 3-variable Boolean function as shown in the figure:

The simplified form of Boolean function $F(A, B, C)$ implemented in 'Product of Sum' form will be



$$(A) (x + z) \cdot (\bar{x} + \bar{y} + \bar{z}) \cdot (y + z)$$

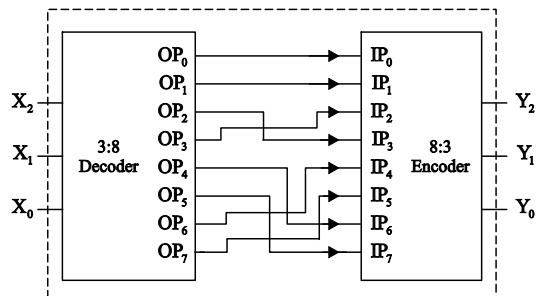
$$(B) (\bar{x} + \bar{z}) \cdot (x + y + z) \cdot (\bar{y} + \bar{z})$$

$$(C) (\bar{x} + \bar{y} + z) \cdot (\bar{x} + y + z) \cdot (x + \bar{y} + z) \\ (x + y + \bar{z})$$

$$(D) (\bar{x} + \bar{y} + \bar{z}) \cdot (\bar{x} + y + \bar{z}) \cdot (x + y + z) \\ (x + \bar{y} + \bar{z})$$

[GATE-S1-EC-2016]

- (8) Identify the circuit below.



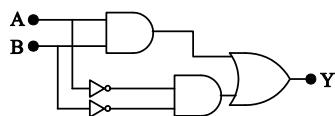
- (A) Binary to Gray code converter
- (B) Binary to XS3 converter
- (C) Gray to Binary converter
- (D) XS3 to Binary converter



4.4 Miscellaneous

[GATE - IN - 2003]

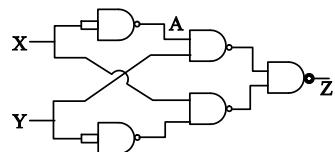
- (1) The logic circuit of Fig. is a



- (A) Half adder (B) XOR
 (C) Equality detector (D) Full adder

[GATE - IN - 2010]

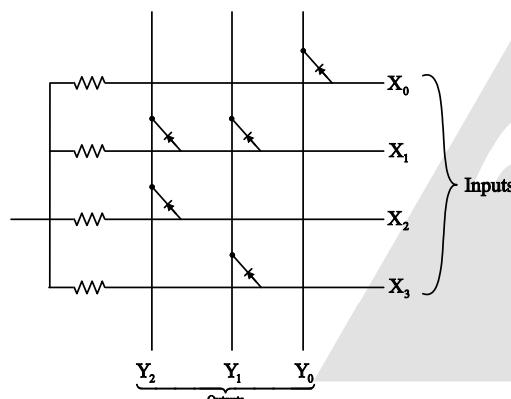
- (2) The logic gate circuit shown in the adjoining figure realizes the function



- (A) XOR (B) XNOR
 (C) Half adder (D) Full adder

[IES - EE - 1998]

- (3) For the diode matrix shown in the figure the output Y_1 will be



- (A) X_0X_2 (B) X_1X_3
 (C) $X_1 + X_3$ (D) $X_0 + X_3$

[IES - EC - 1992]

- (4) Match List – I with List – II and select the correct answer by using the codes given below the lists

List – I

- A. Multiplexer
 B. Shift – Register
 C. Encoder

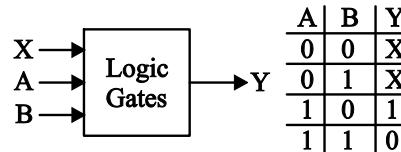
List – II

1. Sequential memory
 2. Converts decimal number to binary
 3. Data selector

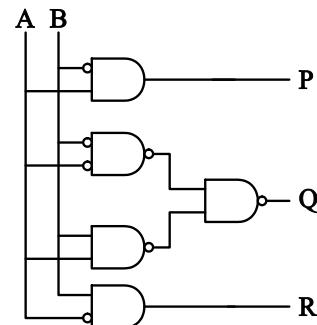
A	B	C
(A) 1	2	3
(B) 2	3	1
(C) 3	1	2
(D) 1	2	2

[GATE-IN-1997]

- (5) Design the logic system shown in figure, to satisfy the truth table given, using minimum number of gates.



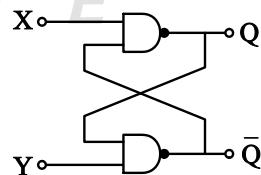
- (6) The circuits shown in the given figure is



- (A) An adder circuit
 (B) A subtractor circuit
 (C) A comparator circuit
 (D) A parity generator circuit

[GATE - EE - 1995]

- (7) For a flip-flop formed from two NAND gates as shown in figure. The unusable state corresponds to

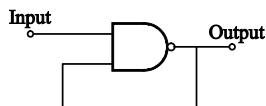


- (A) $X = 0, Y = 0$
 (B) $X = 0, Y = 1$
 (C) $X = 1, Y = 0$
 (D) $X = 1, Y = \infty$

[IES - EC - 2002]

- (8) Consider the following digital circuits :

1. Multiplexers
2. Read Only Memories
3. D-latch
4. Circuit as shown

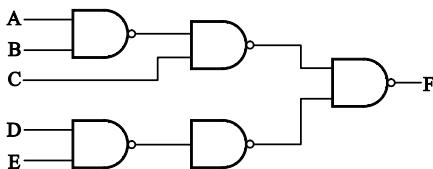


Which of these come under the class of combinational circuits?

- (A) 1 and 2
- (B) 3 and 4
- (C) 1, 2 and 3
- (D) 1, 2, 3 and 4

[IES - EC - 2005]

- (9) Which one of the following functions is realized by the circuit shown above?



- (A) $(\bar{A} + \bar{B})C + \bar{D}\bar{E}$
- (B) $(A + B)C + D + E$
- (C) $AB + C + DE$
- (D) $AB + C(D + E)$

[GATE - EC - 2005]

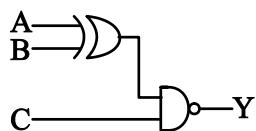
- (10) What is the Boolean expression for the truth table shown below?

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

- (A) $B(A + C)(\bar{A} + \bar{C})$
- (B) $B(A + \bar{C})(\bar{A} + C)$
- (C) $\bar{B}(A + \bar{C})(\bar{A} + C)$
- (D) $\bar{B}(A + C)(\bar{A} + \bar{C})$

[IES - EC - 2010]

- (11) The Boolean expression for the output of the below logic circuit is



(A) $Y = \bar{A}\bar{B} + AB + \bar{C}$

(B) $Y = \bar{A}B + A\bar{B} + \bar{C}$

(C) $Y = A \oplus B + \bar{C}$

(D) $Y = AB + \bar{C}$

[GATE - IN - 2009]

- (12) The minimal sum-of-products expression for the logic function f represented by the given Karnaugh map is :

		PQ	00	01	11	10
		RS	0	1	0	0
		01	0	1	1	1
		11	1	1	1	0
		10	0	0	1	0

(A) $QS + P\bar{R}S + PQR + \bar{P}RS + \bar{P}Q\bar{R}$

(B) $\bar{Q}S + \bar{P}RS + \bar{P}QR + P\bar{R}S + P\bar{Q}R$

(C) $\bar{P}RS + \bar{P}Q\bar{R} + P\bar{R}S + P\bar{Q}R$

(D) $P\bar{R}S + PQR + \bar{P}RS + \bar{P}Q\bar{R}$

[GATE - IN - 2007]

- (13) Let $X = X_1X_0$ and $Y = Y_1Y_0$ be unsigned 2-bit numbers. The function $F = 1$ if $X > Y$ and $F = 0$ otherwise. The minimized sum of products expression for F is :

(A) $Y_1Y_0 + X_0.Y_0 + \bar{X}_1.\bar{X}_0.Y_1$

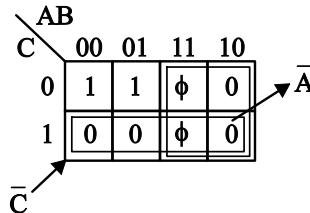
(B) $X_0\bar{Y}_1 + Y_1\bar{Y}_0 + X_1\bar{X}_0$

(C) $Y_1.\bar{X}_1 + Y_0.\bar{X}_1.\bar{X}_0 + Y_1.Y_0.\bar{X}_0$

(D) $X_1.\bar{Y}_1 + X_0.\bar{Y}_0.\bar{Y}_1 + X_0.X_1.\bar{Y}_0$

[GATE - EE - 2000]

- (14) The minimal product-of-sums function described by the K-map given in Fig.



(A) $A'C'$

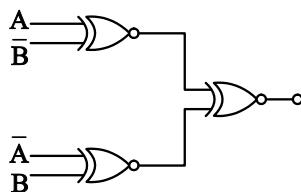
(B) $A' + C'$

(C) $A + C$

(D) AC

[GATE-EC-1995]

- (15) The output of the circuit shown in figure is equal to



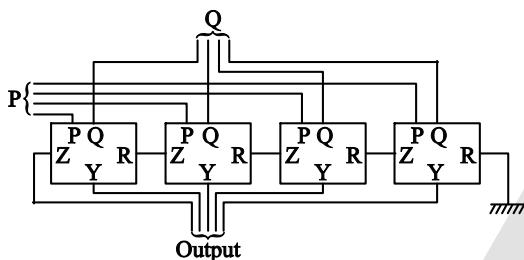
- (A) 0
 (B) 1
 (C) $\bar{A}\bar{B} + \bar{A}\bar{B}$
 (D) $(\bar{A} \oplus B) \oplus (\bar{A} \oplus B)$

[GATE-EC-2003]

- (16) The circuit shown in the figure has 4 boxes each described by inputs P, Q, R and outputs Y, Z with

$$Y = P \oplus Q \oplus R$$

$$Z = RQ + \bar{P}R + Q\bar{P}$$



The circuit acts as a

- (A) 4 bit adder giving $P + Q$
 (B) 4 bit subtractor giving $P - Q$
 (C) 4 bit subtractor giving $Q - P$
 (D) 4 bit adder giving $P + Q + R$

Statement for Linked Answer Question for Next Two Questions :

Two products are sold from a vending machine, which has two push buttons P_1 and P_2 . When a button is pressed, the price of the corresponding product is displayed in a 7-segment display.

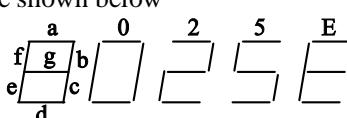
If no buttons are pressed, '0' is displayed, signifying 'Rs. 0'

If only P_1 is pressed, '2' is displayed, signifying 'Rs.2'

If only P_2 is pressed, '5' is displayed, signifying 'Rs.5'

If both P_1 and P_2 are pressed, 'E' is displayed, signifying 'Error'

The names of the segments in the 7-segment display, and the glow of the display for '0', '2', '5' and 'E' are shown below



Consider

- (i) push button pressed/not pressed in equivalent to logic 1/0 respectively,
 (ii) a segment glowing/not glowing in the display is equivalent to logic 1/0 respectively

[GATE-EC-2009]

- (17) If segments a to g are considered as functions of P_1 and P_2 , then which of the following is correct?

- (A) $g = \bar{P}_1 + P_2, d = c + e$
 (B) $g = P_1 + P_2, d = c + e$
 (C) $g = \bar{P}_1 + P_2, e = b + c$
 (D) $g = P_1 + P_2, e = b + c$

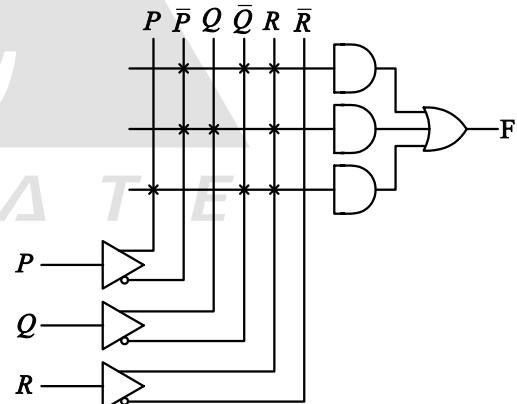
[GATE-EC-2009]

- (18) What are the minimum numbers of NOT gates and 2-input OR gates required to design the logic of the driver for this 7-segment display?

- (A) 3 NOT and 4 OR
 (B) 2 NOT and 4 OR
 (C) 1 NOT and 3 OR
 (D) 2 NOT and 3 OR

[GATE-S2-EC-2017]

- (19) A programmable logic array (PLA) is shown in the figure.

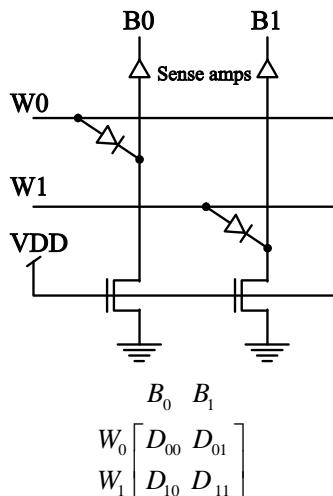


The Boolean function F implemented is

- (A) $\bar{P}\bar{Q}R + \bar{P}QR + P\bar{Q}\bar{R}$
 (B) $(\bar{P} + \bar{Q} + R) + (\bar{P} + Q + R) + (P + \bar{Q} + \bar{R})$
 (C) $\bar{P}\bar{Q}R + \bar{P}QR + P\bar{Q}R$
 (D) $(\bar{P} + \bar{Q} + R) + (\bar{P} + Q + R) + (P + \bar{Q} + R)$

[GATE – EC – 2018]

- (20) A 2×2 ROM array is built with the help of diodes as shown in the circuit below. Here W_0 and W_1 are signals that select the word lines and B_0 and B_1 are signals that are output of the sense amps based on the stored data corresponding to the bit lines during the read operation.



Bits stored in the ROM Array

During the read operation, the selected word line goes high and the other word line is in a high impedance state. As per the implementation shown in the circuit diagram above, what are the bits corresponding to D_{ij} (where $i = 0$ or 1 and $j = 0$ or 1) stored in the ROM?

(A) $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

(B) $\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$

(C) $\begin{bmatrix} 1 & 0 \\ 1 & 0 \end{bmatrix}$

(D) $\begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix}$

[GATE-IN-2019]

- (21) $X = X_1X_0$ and $Y = Y_1Y_0$ are 2-bit binary numbers. The Boolean function S that satisfies the condition “If $X > Y$, then $S = 1$ ”, in its minimized form, is

(A) $X_1Y_0 + X_0Y_1$

(B) $X_1\bar{Y}_1 + X_0\bar{Y}_0\bar{Y}_1 + X_0\bar{Y}_0X_1$

(C) $X_1\bar{Y}_1X_0\bar{Y}_0$

(D) $X_1Y_1 + X_0\bar{Y}_0Y_1 + X_0\bar{Y}_0\bar{X}_1$

-----0000-----

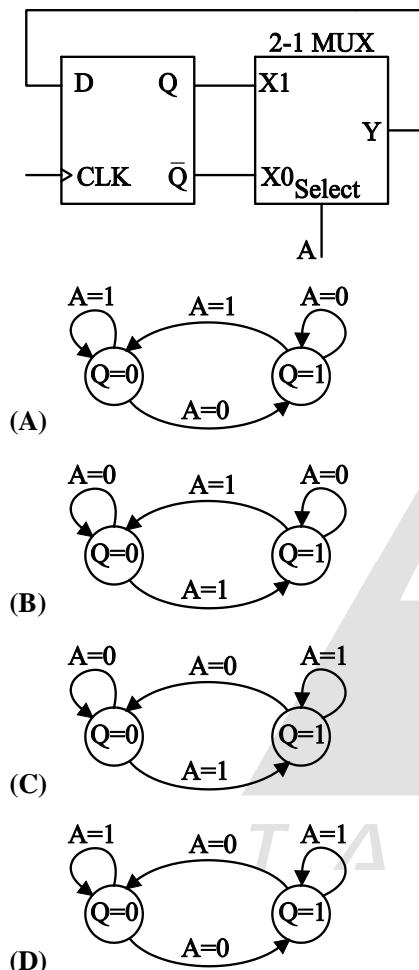
05

Sequential Digital Circuits

5.1 Counter

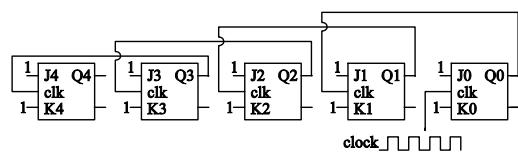
[GATE-EC/EE/IN-2012]

- (1) The state transition diagram for the logic circuit shown is :



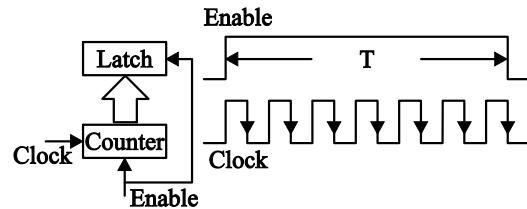
[GATE – EC – 2014]

- (2) Five JK flip flops are cascaded to form the circuit shown in figure clock pulses at a frequency of 1 MHz are applied as shown the frequency (in KHz) of the waveform at Q_3 is -----



[GATE-IN-2007]

- (3) The pulse width T of an asynchronous pulse is measured by a counter with an edge-triggered clock of known frequency f_c as shown in the figure below :



$$(A) T > \frac{100}{xf_c}$$

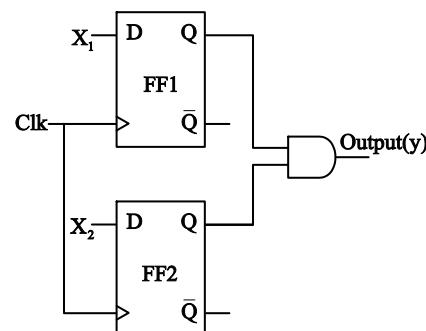
$$(B) T < \frac{100}{xf_c}$$

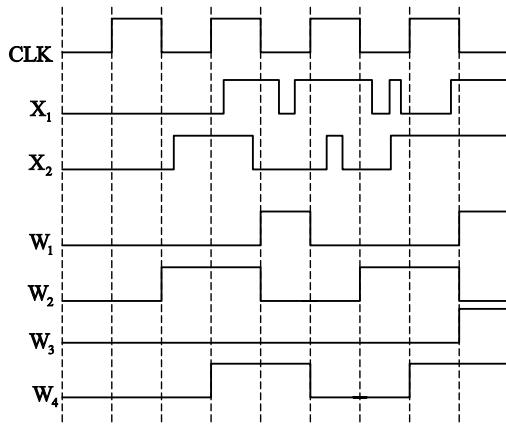
$$(C) T > \frac{200}{xf_c}$$

$$(D) T < \frac{200}{xf_c}$$

[GATE – EC – 2014]

- (4) In the circuit shown choose the correct timing diagram of the output (y) from the given wave forms W_1 , W_2 , W_3 and W_4 .

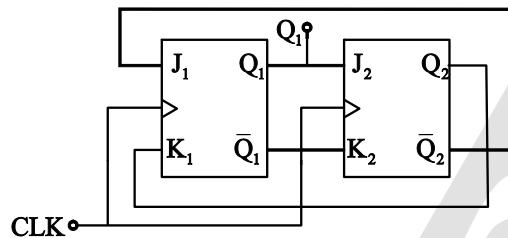




- (C) W_3 (D) W_4

[GATE – EC – 2014]

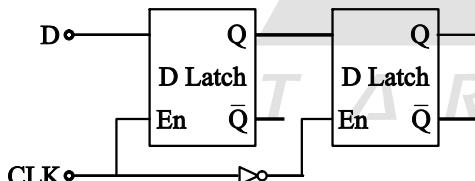
- (5) The outputs of the two flip-flops Q_1 , Q_2 in the figure shown are initialized to 0, 0. The sequence generated at Q_1 upon application of clock signal is



- (A) 01110... (B) 01010....
(C) 00110.... (D) 01100.....

[GATE – EC – 2014]

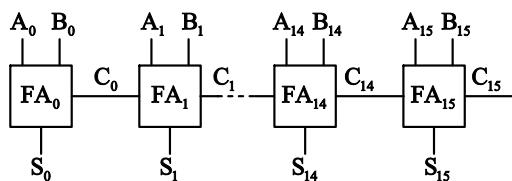
- (6) The circuit shown in the figure is a



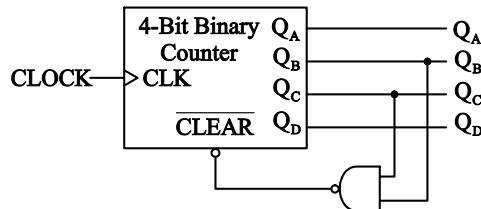
- (A) Toggle Flip Flop
 - (B) JK Flip Flop
 - (C) SR Latch
 - (D) Master-Slave D Flip Flop

[GATE – EC – 2014]

- (7) A 16-bit ripple adder is realized using 16 identical full adders (FA) as shown in the figure. The carry-propagation of delay of each FA is 12 ns and the sum propagation delay of each FA is 15 ns. Worst case delay (in ns) of this 16-bit adder will be-----.

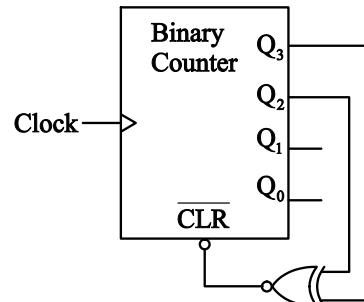


- [GATE – EC – 2015]



[GATE – EC2 – 2015]

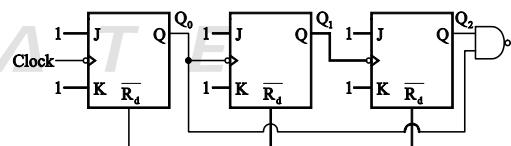
- (9) The figure shows a binary counter with synchronous clear input. With the decoding logic show, the counter works as a



- (A) mod - 2 counter
 - (B) mod - 4 counter
 - (C) mod - 5 counter
 - (D) mod - 6 counter

[GATE – EC3 – 2015]

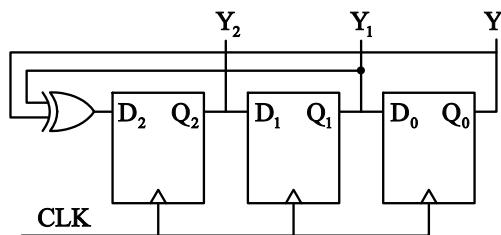
- (10) The circuit shown consists of J-K flip-flops, each with an active low asynchronous reset (\bar{R}_d input). The counter corresponding to this circuit is



- (A) a modulo-5 binary up counter
 - (B) a modulo-6 binary down counter
 - (C) a modulo-5 binary down counter
 - (D) a modulo-6 binary up counter

[GATE – EC3 – 2015]

- (11) A three bit pseudo random number generator is shown. Initially the value of output $Y = Y_2 Y_1 Y_0$ is set to 111. The value of output Y after three clock cycles is



(A) 000

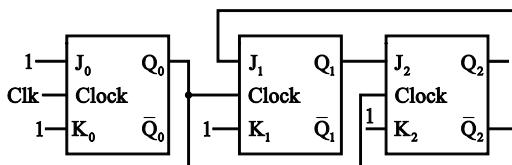
(C) 010

(B) 001

(D) 100

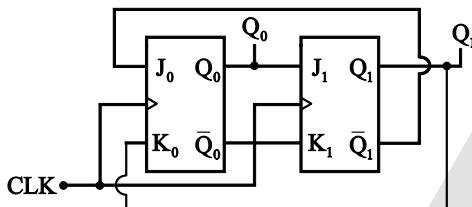
[GATE – EE – 2015]

- (12) The figure shows a digital circuit constructed using negative edge triggered J – K flip flops. Assume a starting state of $Q_2 Q_1 Q_0 = 000$. This state $Q_2 Q_1 Q_0 = 000$ will repeat after _____ number of cycles of the clock CLK.



[GATE – EE – 2015]

- (13) In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1 Q_0 = 00$. The state ($Q_1 Q_0$), $Q_1 Q_0 = 00$. The state ($Q_1 Q_0$), immediately after the 333rd clock pulse is :



(A) 00

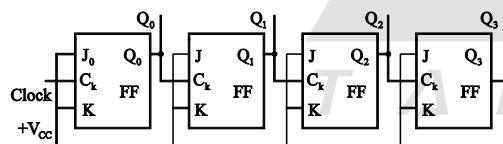
(B) 01

(C) 10

(D) 11

[IES – EE – 1997]

- (14) The circuit schematic shown in the following figure represents a 4-bit



(A) Static shift register

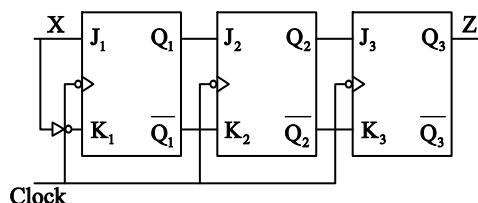
(B) Dynamic shift register

(C) Asynchronous counter

(D) Synchronous counter

[IES – EE – 2010]

- (15) Circuit shown in the fig. below is a :



(A) Shift register

(B) Binary counter

(C) Ripple counter

(D) Sequence detector

[IES – EE – 2010]

- (16) Which of the following counter results in least delay?

(A) Ring counter

(B) Ripple counter

(C) Synchronous counter

(D) Asynchronous counter

[IES – EE – 2012]

- (17) A divide-by-6 counter is obtained using

(A) 6-bit ripple counter

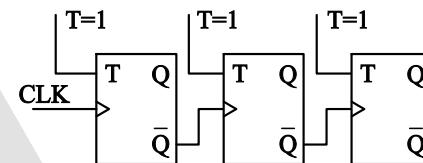
(B) 6-bit ring counter

(C) 3-bit ripple counter

(D) 3-bit twisted - ring counter

[IES – EC – 1992]

- (18) Which type of counter is shown in the figure?



(A) Synchronous

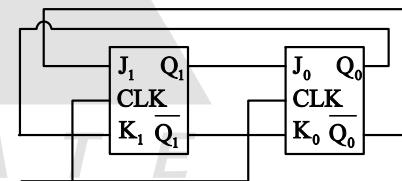
(B) Johnson

(C) Ring

(D) None

[IES – EC – 1992]

- (19) The circuit shown below is



(A) 2:1 scalar

(B) 4:1 scalar

(C) Up – down counter

(D) None

[IES – EC – 1994]

- (20) A divide – by – 78 counter can be realized by using

(A) 6 no's of mod – 13 counters

(B) 13 no's of mod – 6 counters

(C) One mod – 13 counter followed by one mod – 6 counters

(D) 13 no's of mod – 13 counters

[IES – EC – 1994]

- (21) A 4 – bit synchronous counter uses flip flop with propagation delay time of 15ns each. The maximum possible time required for change of state will be

List I		List II	
(Circuit)		(Application)	
A.	Ripple up counter	1.	Division
B.	Synchronous down counter	2.	Multiplication
C.	Shift left register	3.	To create delay
D.	Shift right register	4.	Transient states

Codes:

	A	B	C	D
(A)	2	3	4	1
(B)	4	1	2	3
(C)	2	1	4	3
(D)	4	3	2	1

[IES - EC - 2009]

- (32) Which of the following circuits come under the class of sequential logic circuits?
1. Full adder
 2. Full subtractor
 3. Half adder
 4. J-K flip-flop
 5. Counter

Select the correct answer from the codes given below:

- | | |
|-------------|-------------|
| (A) 1 and 2 | (B) 2 and 3 |
| (C) 3 and 4 | (D) 4 and 5 |

[IES - EC - 2009]

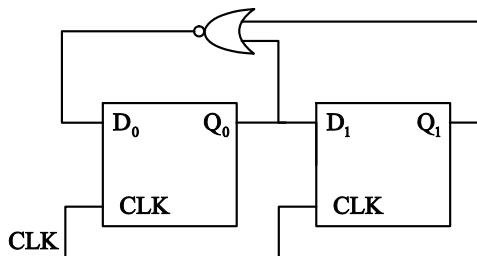
- (33) Which of the following measurements can be done using a counter?
1. Pulse duration
 2. Interval between two pulses
 3. Amplitude of the pulse
 4. Rise time of a pulse

Select the correct answer from the codes given below:

- | | |
|-------------|-------------|
| (A) 1 and 2 | (B) 2 and 3 |
| (C) 1 and 4 | (D) 2 and 4 |

[GATE - EC - 2007]

- (34) For the circuit shown below the counter state ($Q_1 Q_0$) follows the sequence



(A) 00,01,10,11,00

(B) 00,01,10,00,01

(C) 00,01,11,00,01

(D) 00,10,11,00,10

[GATE - EC - 1993]

- (35) A pulse train with a frequency of 1 MHz is counted using a mod - 1024 ripple counter built with J - K flip flops. For proper operation of the counter the maximum permissible propagation delay per flip flop stage is

- | | |
|------------|-----------|
| (A) 100 ns | (B) 50 ns |
| (C) 20 ns | (D) 10 ns |

[IES - EC - 2012]

- (36) The highest speed counter is

- (A) Asynchronous counter
- (B) Synchronous counter
- (C) Ripple counters
- (D) Ring counter

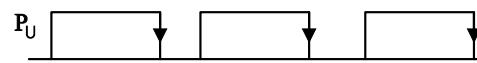
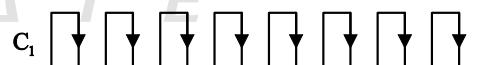
[GATE - IN - 1998]

- (37) The minimum number of flip - flops needed to make mod - 2 counter is

- | | |
|-------|-------|
| (A) 1 | (B) 2 |
| (C) 3 | (D) 4 |

[GATE - IN - 2003]

- (38) The square wave C_1 shown in Fig. is given to the clock input of a 4-bit binary up/down counter whose UP/ \overline{DN} input if fed with the pulse train P_u . The counter is a negative edge triggered one. The counter starts with 0000 and will reach 0000 again at the



(A) 15th clock pulse

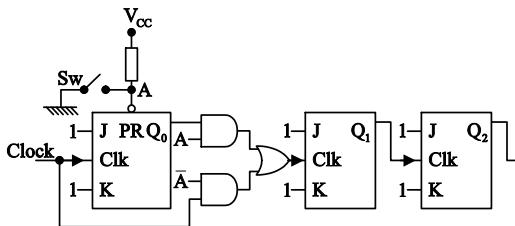
(B) 16th clock pulse

(C) 44th clock pulse

(D) 48th clock pulse

[GATE - IN - 2005]

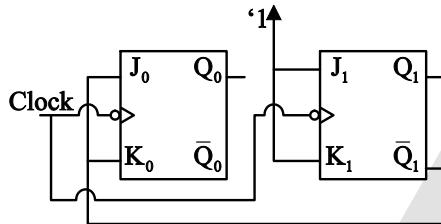
- (39) For the digital counter shown in the figure with output Q_0, Q_1, Q_2, \dots , where Q_0 indicates the LSB of the count value, the correct statement when the switch Sw is closed is



- (A) Counter outputs are both even and odd numbers
- (B) Counter outputs are only odd numbers
- (C) Counter outputs are only even numbers
- (D) Counter stops counting

[GATE - IN - 2006]

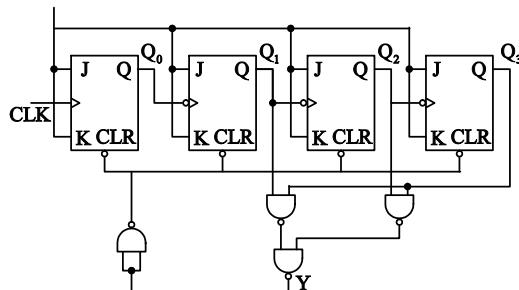
- (40) Given that the initial state (Q_1Q_0) is the counting sequence of the counter shown in the following figure is, Q_1Q_0 =



- (A) 00 – 11 – 01 – 10 - 00
- (B) 00 – 01 – 11 – 10 - 00
- (C) 00 – 11 – 10 – 01 - 00
- (D) 00 – 10 – 01 – 11 - 00

Statement for Linked Answer Questions for Next Two Questions :

Consider the counter circuit shown below:



[GATE - IN - 2008]

- (41) In the above figure, Y can be expressed as

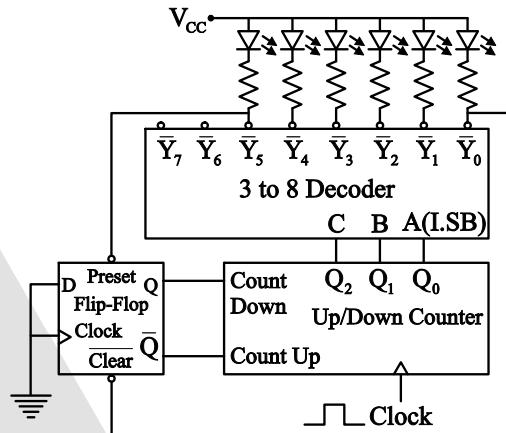
- (A) $Q_3(Q_2 + Q_1)$
- (B) $Q_3 + Q_2Q_1$
- (C) $Q_3(Q_2 + Q_1)$
- (D) $\overline{Q_3 + Q_2Q_1}$

[GATE - IN - 2008]

- (42) The above circuit is a
- (A) Mod-8 Counter
 - (B) Mod-9 Counter
 - (C) Mod-10 Counter
 - (D) Mod-11 Counter

[GATE - IN - 2011]

- (43) The circuit below shows an up/down counter working with a decode and a flip-flop. Preset and clear of the flip-flop are asynchronous active-low inputs.

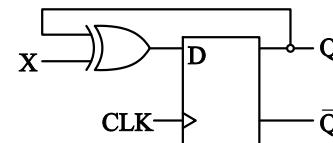


Assuming that the initial value of counter output ($Q_2Q_1Q_0$) as zero, the counter outputs in decimal for 12 clock cycles are

- (A) 0,1,2,3,4,4,3,2,1,1,2,3,4
- (B) 0,1,2,3,4,5,0,1,2,3,4,5,0
- (C) 0,1,2,3,4,5,5,,4,3,2,1,0,1
- (D) 0,1,2,3,4,5,4,3,2,1,0,1,2

[GATE - EE - 2005/IES - EE - 2009]

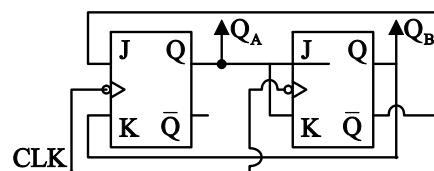
- (44) The digital circuit shown in the figure works as a



- (A) JK flip-flop
- (B) Clocked RS flip-flop
- (C) T flip-flop
- (D) Ring counter

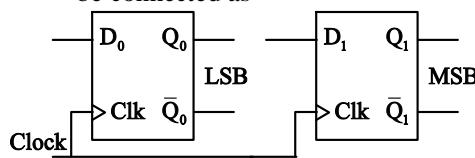
[GATE - EE - 2011]

- (45) A two-bit counter circuit is shown below



goes through the following $Q_1 Q_0$ sequence
 $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \rightarrow \dots$

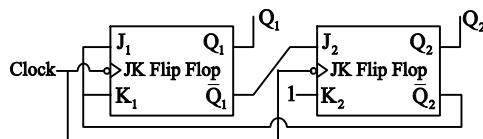
The inputs D_0 and D_1 respectively should be connected as



- (A) \bar{Q}_1 and Q_0
- (B) Q_0 and Q_1
- (C) $\bar{Q}_1 Q_0$ and $\bar{Q}_1 Q_0$
- (D) $Q_1 Q_0$ and $Q_1 Q_0$

[GATE -EC - 2009]

- (53) What are the counting states (Q_1, Q_2) for the counter shown in the figure below ?



- (A) 11, 10, 00, 11, 10,
- (B) 01, 1011, 00, 01
- (C) 00, 11, 01, 10, 00
- (D) 01, 10, 00, 01, 10

[GATE -EC - 2011]

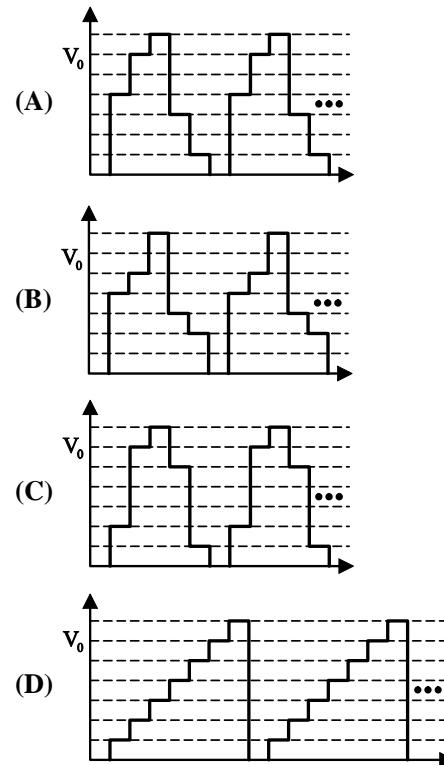
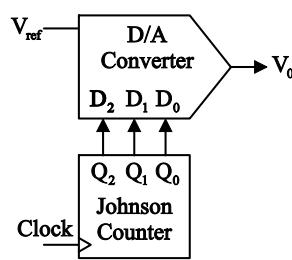
- (54) Two D flip – flops are connected as a synchronous counter that goes through the following $Q_B Q_A$ sequence $00 \rightarrow 11 \rightarrow 01 \rightarrow 10 \rightarrow 00 \rightarrow \dots$

The connections to the input D_A and D_B are

- (A) $D_A = Q_B, D_B = Q_A$
- (B) $D_A = \bar{Q}_A, D_B = \bar{Q}_B$
- (C) $D_A = (Q_A \bar{Q}_B + \bar{Q}_A Q_B), D_B = Q_A$
- (D) $D_A = (Q_A Q_B + \bar{Q}_A \bar{Q}_B), D_B = \bar{Q}_B$

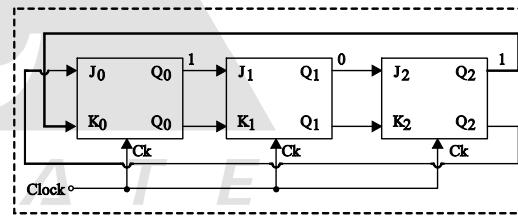
[GATE -EC - 2011]

- (55) The output of a 3-stage Johnson (twisted – ring) counter is fed to a digital – to – analog (D/A) converter as shown in the figure below. Assume all states of the counter to be unset initially. The waveform which represents the D/A converter output V_0 is :



[IES – EE – 2003]

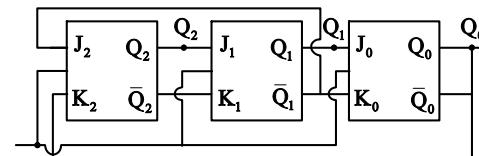
- (56) The three-stage Johnson Ring Counter as shown above is clocked at a constant frequency of f_c from the starting state of $Q_0 Q_1 Q_2 = 101$. The frequency of outputs $Q_0 Q_1 Q_2$ will be



- (A) $f_c / 8$
- (B) $f_c / 6$
- (C) $f_c / 3$
- (D) $f_c / 2$

[IES – EE – 1999]

- (57) The counter shown in the figure has initially $Q_2 Q_1 Q_0 = 000$. The status of $Q_2 Q_1 Q_0$ after the first pulse is :



- (A) 001
- (B) 010
- (C) 100
- (D) 101

[GATE – EC – 1995]

- (58) An R-S latch is

- (A) Combinatorial circuit
(B) Synchronous sequential circuit.
(C) One bit memory element
(D) One clock delay element.

[GATE – EC – 2003]

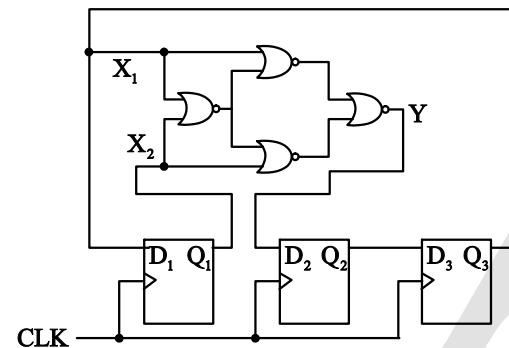
(59) A 0 to 6 counter consists of 3 flipflops and a combination circuit of 2 input gate(s).

The combination circuit consists of

(A) one AND gate
(B) one OR gate
(C) one AND gate and one OR gate
(D) two AND gates

**Statement for Linked Answer Questions for
Next Two Questions :**

Consider the circuit shown in the following figure.



- [GATE – EC – 2007]

- [GATE – EC – 2007]

- (63) The output Q_{n+1} of a J-K flip-flop for the input $J = 1, K = 1$ is :

- [IES -EC - 2009]**
- (66) Which of the following flip-flop is used as a latch?
- (A) J K flip-flop
- (B) R S flip-flop
- (C) T flip-flop
- (D) D flip-flop

- [IES -EC – 2004/2009]

- | | |
|------------------|------------------|
| (A) 1, 2 and 3 | (B) 1 and 2 only |
| (C) 2 and 3 only | (D) 3 and 4 only |

[IES -EC - 1999/2007/2014]

- (68) A 1 ms pulse can be converted into a 10 ms pulse by using which one of the following?
- (A) An astable multivibrator
 - (B) A monostable multivibrator
 - (C) A bistable multivibrator
 - (D) A J-K flip-flop

[IES -EC - 2006]

- (69) Which one of the following equations satisfies the JK flip-flop truth table?
- (A) $Q_{n+1} = J_n \bar{Q}_n + \bar{K}_n Q_n$
 - (B) $Q_{n+1} = \bar{J}_n \bar{Q}_n + \bar{K}_n Q_n$
 - (C) $Q_{n+1} = J_n Q_n + K_n Q_n$
 - (D) $Q_{n+1} = \bar{J}_n \bar{Q}_n + \bar{K}_n \bar{Q}_n$

[IES -EC - 1999]

- (70) In a negative edge triggered J – K flip flop, in order to have the output Q state 0, 0 and 1 in the next three successive clock pulses, the J – K input states required would be respectively
- (A) 00, 00 and 10
 - (B) 00, 01 and 11
 - (C) 00, 10 and 11
 - (D) 01, 10 and 11

[IES -EC - 2000/2009/2014]

- (71) Consider the following statements
1. Race around condition occurs in a JK flip – flop when both the inputs are one
 2. A flip – flop is used to store one bit of information
 3. A transparent latch consists of a D-type flip flop
 4. Master – slave configuration is used in flip – flops to store two bits of information
- Which of these statements are correct?
- (A) 1, 2 and 3
 - (B) 1, 3 and 4
 - (C) 1, 2 and 4
 - (D) 2, 3 and 4

[IES – EC – 2010]

- (72) The Q output of a J-K FLIP – FLOP is '1' the output does not change when a clock – pulse is applied. The inputs J and K will be respectively (where 'x' don't care state)
- (A) 0 and x
 - (B) x and 0
 - (C) 1 and 0
 - (D) 0 and 0

[IES -EC - 1992]

- (73) The difference between sequential and combinational circuits is that
- (A) Combinational circuits store bits
 - (B) Combinational circuits have memory
 - (C) Sequential circuits store bits
 - (D) Sequential circuits have memory

- (74) Which of the following statements are correct?

1. A flip – flop is used to store 1 – bit of information
2. Race – around condition occurs in a J-K flip flop to store 2 – bits of information
3. Master – slave configuration is used in flip flop to store 2 bits of information
4. A transparent latch consists of a D – type flip flop

Select the correct answer using the codes given below

- | | |
|----------------|----------------|
| (A) 1, 2 and 3 | (B) 1, 3 and 4 |
| (C) 1, 2 and 4 | (D) 2, 3 and 4 |

[IES – EE – 2010]

- (75) In how many different modes a universal shift register operates?

- | | |
|-------|-------|
| (A) 2 | (B) 3 |
| (C) 4 | (D) 5 |

[IES – EE – 2007]

- (76) The reduced state table of a sequential machine has 7 rows. What is the minimum number of flip-flops needed to implement the machine?
- (A) 0
 - (B) 2
 - (C) 3
 - (D) 7

- (77) For a JK flip-flop, Q_n is output at time step t_n . Which of the following Boolean expressions represents Q_{n+1} ?

- (A) $J_n \bar{Q}_n + \bar{K}_n Q_n$
- (B) $J_n Q_n K_n \bar{Q}_n$
- (C) $\bar{J}_n Q_n + K_n \bar{Q}_n$
- (D) $J_n Q_n + \bar{K}_n \bar{Q}_n$

[IES -EC - 1994]

- (78) A synchronous sequential circuit is to be designed which will produce an output '1' when previous and present input represent an even number, with present input being least significant bit. The minimum number of states of the machine will be :

(A) 2

(B) 3

(C) 4

(D) 5

[IES -EC - 1998]

- (79) If a mod-6 counter is constructed using 3-flip - flop, the counter will skip

(A) 4 counter

(B) 3 counter

(C) 2 counter

(D) None of the counts

[IES - EE - 2005]

- (80) In a ripple counter, the stage whose output has a frequency equal to $1/8^{\text{th}}$ that of the clock signal applied to the first stage, also has an output periodicity equal to $1/8^{\text{th}}$ that of the output signal obtained from the last stage. The counter is

(A) Modulo-8

(B) Modulo-6

(C) Modulo-64

(D) Modulo-16

[GATE - EE - 2000]

- (81) A dual-slope analog-to-digital converter uses an N-bit counter. When the input signal V_a is being integrated, the counter is allowed to count up to a value:

(A) Equal to $2^N - 2$ (B) Equal to $2^N - 1$ (C) Proportional to V_a (D) Inversely proportional to V_a **[IES - EC - 2012]**

- (82) Match List I with List II select the correct answer using the code given below the lists :

List I

(A) 555

(B) 74173

(C) 74163

(D) 8097

List II

1. Microcontroller

2. Register

3. Timer

4. Counter

Code :

A B C D

(A) 3 4 2 1

(B) 1 4 2 3

(C) 3 2 4 1

(D) 1 2 4 3

[IES – EC – 2011]

- (83) An eight-bit binary ripple UP counter with a modulus of 256 is holding the count 01111111. What will be the count after 135 clock pulses?

(A) 0000 0101

(B) 1111 1001

(C) 0000 0110

(D) 0000 0111

[IES - EC - 2000]

- (84) **Assertion (A):** A ring counter is preferred over a binary sequential counter

Reason (R): The decoding logic is simple for a ring counter

(A) Both A and R is true and R is the correct explanation of A

(B) Both A and R is true but R is NOT the correct explanation of A

(C) A is true but R is false

(D) A is false but R is true

[IES – EE – 2010]

- (85) A shift register with the serial output connected back to the serial input is a

(A) Feedback shift register

(B) Shift register counter

(C) Universal shift register

(D) Serial to parallel converter

[IES – EE – 2012]

- (86) To operate correctly, starting a ring counter requires

(A) Clearing all the flip-flops

(B) Presetting one filp-flop and clearing all other

(C) Clearing one flip-flop and presenting all other

(D) Presetting all the flip-flops

[IES – EE – 2012]

- (87) For a bi-directional synchronous counter

(A) Each flip-flop divides the frequency of its clock input by 2

(B) Each flip - flop output is used as the clock input to the next flip - flop

(C) No decoding logic is required

(D) Each flip-flop is clocked at the same time

[IES - EC - 1999]

- (88) The initial state MOD – 16 down counter is 0110. After 37 clock pulses, the state of the counter will be

- | | |
|----------|----------|
| (A) 1011 | (B) 0110 |
| (C) 0101 | (D) 0001 |

[IES -EC - 2004]

- (89) The total number of 1's in a 15-bit shift register is to be counted by clocking into a counter which is present to 0. The counter must have which one of the following.

- | | |
|-------------|------------|
| (A) 4-bits | (B) 5-bits |
| (C) 16-bits | (D) 6-bits |

[IES -EC - 2003]

- (90) Minimum number of J-K flip-flops needed to construct a BCD counter is

- | | |
|-------|-------|
| (A) 2 | (B) 3 |
| (C) 4 | (D) 5 |

[IES – EC – 2011]

- (91) A 4-bit ripple counter consisting of flip-flops that each has a propagation delay of 12ns from clock to Q output. For the counter to recycle from 1111 to 0000, it takes a total of

- | | |
|----------|----------|
| (A) 12ns | (B) 24ns |
| (C) 48ns | (D) 26ns |

[GATE - IN - 1995]

- (92) A 4-bit synchronous counter with a series carry, uses flip – flop and AND gates, having a propagation delay of 30 ns and 10 ns respectively. The maximum time interval required between two successive clock pulses for reliable operation of the counter is

- | | |
|-----------|-----------|
| (A) 10 ns | (B) 30 ns |
| (C) 40 ns | (D) 50 ns |

[GATE - IN - 2002/IES - EE - 2008]

- (93) Consider the following statements in Johnson counter:

1. A MOD-6 Johnson counter requires 3 FFs.
2. Johnson counter requires decoding gates.
3. To decode each count, one logic gate is used. Each gate requires only two inputs regardless of the number of FFs.

Which of the statements given above are correct?

- | |
|------------------|
| (A) 1 and 2 only |
| (B) 2 and 3 only |
| (C) 1 and 3 only |
| (D) 1, 2 and 3 |

[IES -EC - 1995]

- (94) A 1 m sec pulse can be converted into a 10 m sec pulse by using

- | |
|----------------------------------|
| (A) An astable multi vibrator |
| (B) A mono stable multi vibrator |

- | |
|--------------------------------|
| (C) A bi stable multi vibrator |
| (D) A J-K flips – flop |

[GATE -EC - 1990]

- (95) A 4 bit modulo-16 ripple counter uses JK flip-flops. If the propagation delay of each FF is 50ns, the maximum clock frequency that can be used is equal to:

- | | |
|------------|------------|
| (A) 20 MHz | (B) 10 MHz |
| (C) 5 MHz | (D) 4 MHz |

[GATE-IN-2002]

- (96) The 14-bit timer is loaded with the counter value of 07DOH. The timer input is connected to a clock with a frequency of 800 KHz. The timer is programmed to produce a continuous signature wave output. The frequency of the square wave output is

- | | |
|-------------|--------------|
| (A) 400 kHz | (B) 800 kHz |
| (C) 400 Hz | (D) 2000 kHz |

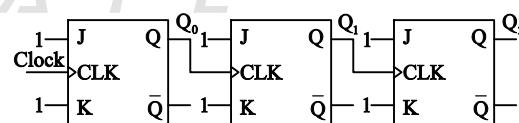
[GATE-IN-2003]

- (97) The clock frequency of a timer-counter is 10 MHz. The timer-counter is used in the period mode and the input to the timer-counter is a square wave of frequency 2 kHz. The display of the timer-counter will show a value

- | | |
|----------|-----------|
| (A) 200 | (B) 2000 |
| (C) 5000 | (D) 50000 |

[GATE-IN-2009]

- (98) The figure below shows a 3-bit ripple counter, with Q_2 as the MSB, the flip-flop are rising-edge triggered. The counting direction is



- | |
|--|
| (A) always down |
| (B) always up |
| (C) up or down depending on the initial state of Q_0 only |
| (D) up or down depending on the initial states of Q_2, Q_1 and Q_0 |

[GATE-IN-2014]

- (99) Frequency of an analog periodic signal in the range of 5kHz-10kHz is to be measured with a resolution of 100Hz by measuring its period with a counter. Assuming negligible signal and transition delays the minimum clock frequency and minimum number of bits in the counter needed, respectively, are:

- (A) 1 MHz, 10-bits (B) 1 MHz, 10-bits
 (C) 1 MHz, 8-bits (D) 10MHz, 8-bits

[GATE-EE-2014]

- (100) A cascade of three identical modulo-5 counters has an overall modulus of

- (A) 5 (B) 25
 (C) 125 (D) 625

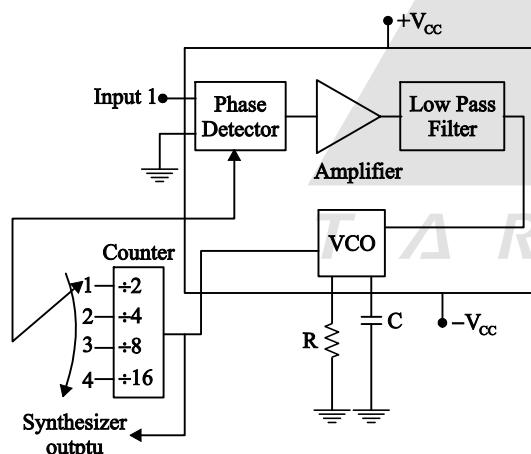
[GATE-IN-2002]

- (101) A counter timer has a basic clock of 16 MHz. The count value displayed is in error by 1 count. The frequency at which the error in the displayed value is the same whether the counter-time is used in the frequency mode of operation or period mode of operation is

- (A) 15 MHz (B) 10 MHz
 (C) 8 MHz (D) 4 MHz

[GATE-S1-EC-2016]

- (102) The block diagram of a frequency synthesizer consisting of a Phase Locked Loop (PLL) and a divide-by-N counter (comprising $\div 2$, $\div 4$, $\div 8$, $\div 16$ outputs) is sketched below. The synthesizer is excited with a 5 kHz signal (Input 1). The free-running frequency of the VCO is set to 20 kHz. Assume that the commutator switch makes contacts repeatedly in the order 1-2-3-4.

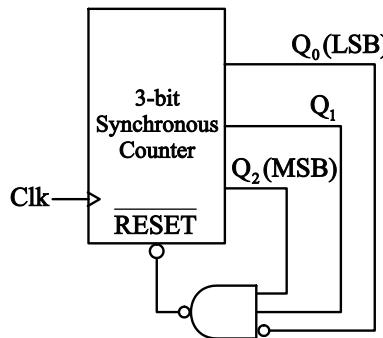


The corresponding frequencies synthesized are:

- (A) 10 kHz, 20 kHz, 40 kHz, 80 kHz
 (B) 20 kHz, 40 kHz, 80 kHz, 160 kHz
 (C) 80 kHz, 40 kHz, 20 kHz, 10 kHz
 (D) 160 kHz, 80 kHz, 40 kHz, 20 kHz

[GATE-S4-EC-2016]

- (103) For the circuit shown in the figure, the delay of the bubbled NAND gate is 2 ns and that of the counter is assumed to be zero.



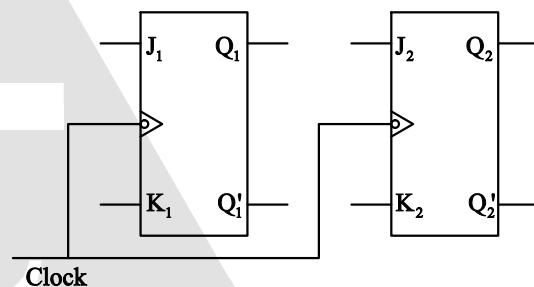
If the clock (Clk) frequency is 1 GHz, then the counter behaves as a

- (A) mod-5 counter
 (B) mod-6 counter
 (C) mod-7 counter
 (D) mod-8 counter

[GATE-S4-IN-2016]

- (104) A synchronous counter using two J - K flip flops that goes through the sequence of states:

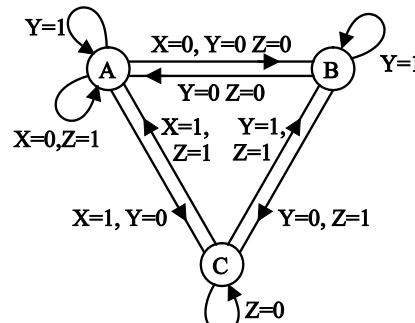
$Q_1Q_2=00 \rightarrow 1 \rightarrow 01 \rightarrow 11 \rightarrow 00 \dots$ is required. To achieve this, the inputs to the flip flops are



- (A) $J_1 = Q_2, K_1 = 0; J_2 = Q_1, K_2 = Q_1$
 (B) $J_1 = 1, K_1 = 1; J_2 = Q_1, K_2 = Q_1$
 (C) $J_1 = Q_2, K_1 = Q_2'; J_2 = 1, K_2 = 1$
 (D) $J_1 = Q_2', K_1 = Q_2; J_2 = Q_1, K_2 = Q_1'$

[GATE-S3-EC-2016]

- (105) The state transition diagram for a finite state machine with states A, B and C, and binary inputs X, Y and Z, is shown in the figure.

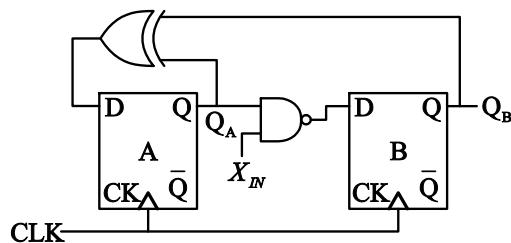


Which one of the following statements is correct?

- (A) Transitions from State A are ambiguously defined.
- (B) Transitions from State B are ambiguously defined.
- (C) Transitions from State C are ambiguously defined.
- (D) All of the state transitions are defined unambiguously.

[GATE-S1-EC-2017]

- (106) A finite state machine (FSM) is implemented using the D flip-flops A and B, and logic gates, as shown in the figure below. The four possible states of the FSM are $Q_A Q_B = 00, 01, 10$, and 11

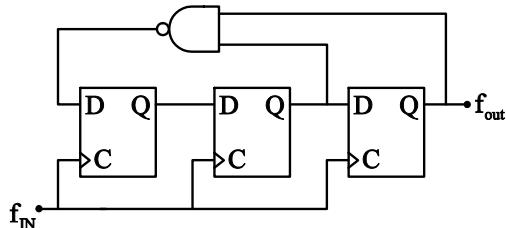


Assume that X_{IN} is held at constant logic level throughout the operation of the FSM. When the FSM is initialized to the $Q_A Q_B = 00$ and clocked, after a few clock cycles, it starts cycling through

- (A) all of the four possible states if $X_{IN} = 1$
- (B) three of the four possible states if $X_{IN} = 0$
- (C) only two of the four possible states if $X_{IN} = 1$
- (D) only two of the four possible states if $X_{IN} = 0$

[GATE - EE - 2018]

- (107) Which one of the following statements is true about the digital circuit shown in the figure

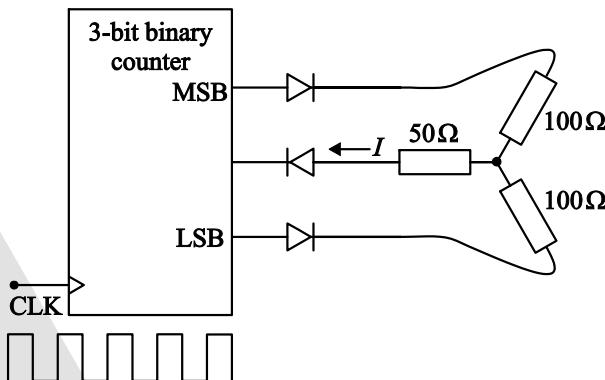


- (A) It can be used for dividing the input frequency by 3.
- (B) It can be used for dividing the input frequency by 5.
- (C) It can be used for dividing the input frequency by 7.

- (D) It cannot be reliably used as a frequency divider due to disjoint internal cycles.

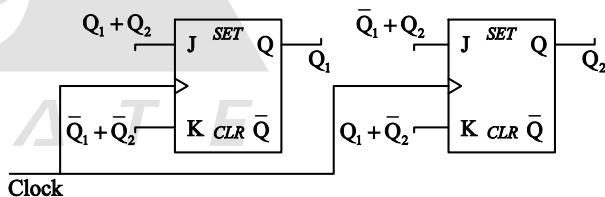
[GATE – IN – 2018]

- (108) For the 3-bit binary counter shown in the figure, the output increments at every positive transition in the clock (CLK). Assume ideal diodes and the starting state of the counter as 000. If output high is 1 V and output low is 0 V, the current I (in mA) flowing through the $50\ \Omega$ resistor during the 5th clock cycle is (up to one decimal place) _____.



[GATE – IN – 2018]

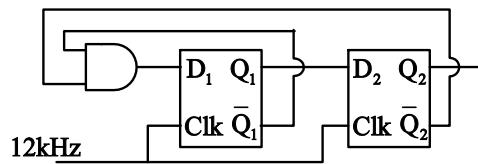
- (109) A 2-bit synchronous counter using two J-K flip flops is shown. The expressions for the inputs to the J-K flip flops are also shown in the figure. The output sequence of the counter starting from $Q_1 Q_2 = 00$ is



- (A) 00 → 11 → 10 → 01 → 00 ...
- (B) 00 → 01 → 10 → 11 → 00 ...
- (C) 00 → 01 → 11 → 10 → 00 ...
- (D) 00 → 10 → 11 → 01 → 00 ...

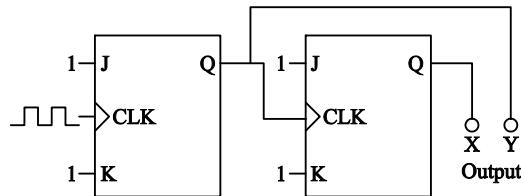
[GATE-EC-2019]

- (110) In the circuit shown, the clock frequency, i.e., the frequency of the CLK signal, is 12 kHz. The frequency of the signal at Q_2 is _____ kHz.

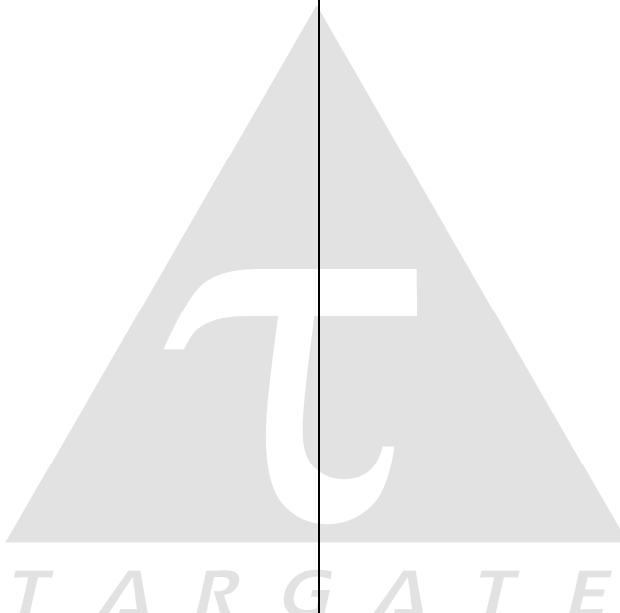


[GATE-IN-2019]

- (111) The circuit shown in the figure below uses ideal positive edge-triggered synchronous J-K flip flops with outputs X and Y. If the initial state of the outputs is $X = 0$ and $Y = 0$ just before the arrival of the first clock pulse, the state of the output just before the arrival of the second clock pulse is :



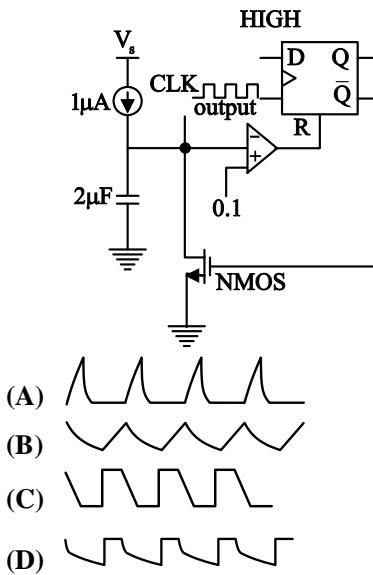
- (A) $X = 0, Y = 0$ (B) $X = 0, Y = 1$
(C) $X = 1, Y = 0$ (D) $X = 1, Y = 1$



5.2 Miscellaneous

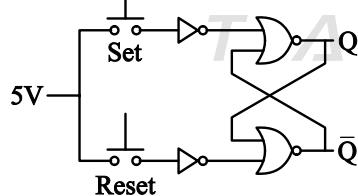
[GATE – IN – 2015]

- (1) For the circuit shown in the figure, the raising edge triggered D – flip flop with asynchronous reset has a clock frequency of 1 Hz . The NMOS transistor has an ON resistance of $1000\ \Omega$ and an OFF resistance of infinity. The nature of the output waveform is



[GATE – EC3 – 2015]

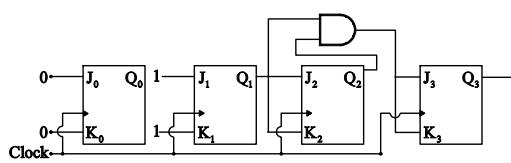
- (2) An SR latch is implemented using TTL gates as shown in the figure. The set and reset pulse inputs are provided using the push-button switches. It is observed that the circuit fails to work as desired. The SR latch can be made functional by changing



- (A)** NOR gates to NAND gates
(B) inverts to buffers
(C) NOR gates to NAND gates and inverters to buffers
(D) 5 V to ground

[IES – EE – 1996]

- (3) For the digital circuit shown in the given figure, the output $Q_3Q_2Q_1Q_0 = 0001$ initially. After a clock pulse appears, the output $Q_3Q_2Q_1Q_0$ will be



(A) 0001

(C) 0100

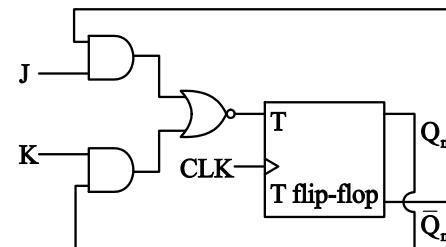
(B) 0011

(D) 1100

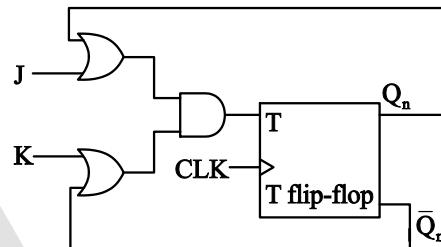
[GATE-EE-2014]

- (4) A JK flip flop can be implemented by T flip-flops. Identify the correct implementation.

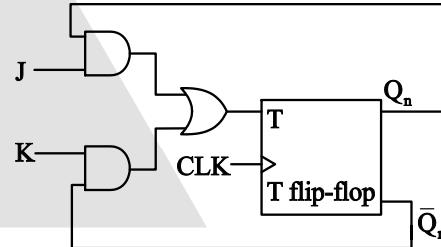
(A)



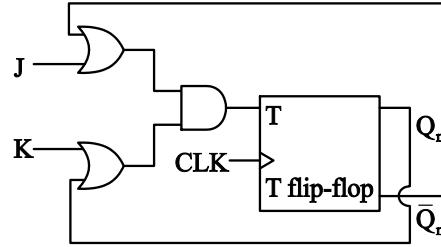
(B)



(C)

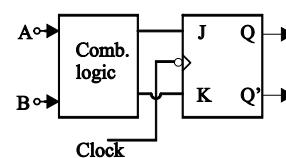


(D)



[IES – EE – 1997]

- (5) To realize the given truth table from the circuit shown in the figure, the input to J in terms of A and B would have to be



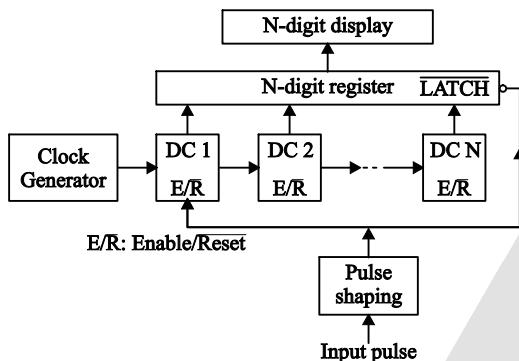
A	B	Q_{n+1}
0	0	\bar{Q}_n
0	1	1
1	0	Q_n
1	1	0

- (A) \overline{AB}
 (C) B

- (B) \bar{A}
 (D) AB

[GATE-IN-2015]

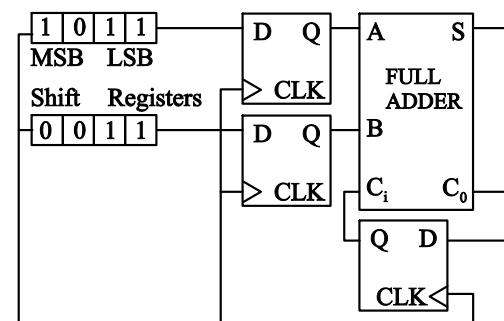
- (6) The number of clock cycles for the duration of an input pulse is counted using a cascade of N decade counters (DC 1 to DC N) as shown in the figure. If the clock frequency in mega hertz is f , the resolution and range of measurement of input pulse width, both in μs , are respectively,



- (A) $\frac{1}{f}$ and $\frac{(2^N - 1)}{f}$
 (B) $\frac{1}{f}$ and $\frac{(10^N - 1)}{f}$
 (C) $\frac{10^N}{f}$ and $\frac{(10^N - 1)}{f}$
 (D) $\frac{2^N}{f}$ and $\frac{(2^N - 1)}{f}$

[GATE-EC-2006]

- (7) For the circuit shown in the figure below, two 4-bit parallel-in serial-out shift registers loaded with the data shown are used to feed the data to a full adder. Initially, all the flip-flops are in clear state. After applying two clock pulses, the outputs of the full adder should be



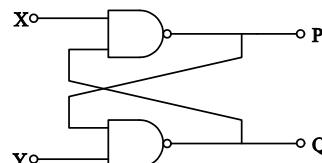
- | | |
|-------------|-----------|
| (A) $S = 0$ | $C_0 = 0$ |
| (B) $S = 0$ | $C_0 = 1$ |
| (C) $S = 1$ | $C_0 = 0$ |
| (D) $S = 1$ | $C_0 = 1$ |

[GATE -EC -2007]

- (8) The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below:

$$X = 0, Y = 1; X = 0, Y = 0; X = 1, Y = 1.$$

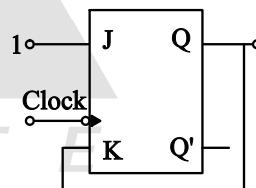
The corresponding stable P, Q outputs will be



- | |
|--|
| (A) $P = 1, Q = 0; P = 1, Q = 0; P = 1, Q = 0$ or $P = 0, Q = 1$ |
| (B) $P = 1, Q = 0; P = 1, Q = 0$; or $P = 0, Q = 1; P = 1, Q = 0$ |
| (C) $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 0$; or $P = 0, Q = 1$ |
| (D) $P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 1$ |

[IES – EE – 2008]

- (9) In the circuit shown in the figure, $Q = 0$, initially. What shall be the subsequent states of Q when clock pulses are given ?



- | |
|-----------------------|
| (A) 1, 0, 1, 0, |
| (B) 0, 0, 0, 0, |
| (C) 1, 1, 1, 1, |
| (D) 0, 1, 0, 1, |

[IES – EE – 2000]

- (10) The states of a RS flip-flop are given in the following table :

States	R	S	Q_n	Q_{n+1}
1	0	0	1	1
2	0	1	0	1
3	1	0	1	0

The mode of operation of states 1, 2 and 3 are respectively

- (A) Indeterminate, set and reset
- (B) Prohibited, set and hold
- (C) Set, hold and reset
- (D) Hold, set and reset

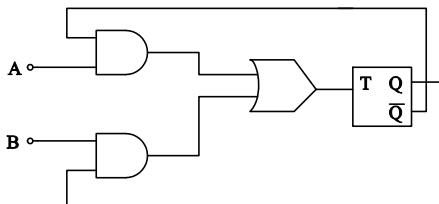
[IES – EE – 2003]

- (11) T flip-flop can be made from a J-K flip-flop by making

- (A) $J = K$
- (B) $J = K = 1$
- (C) $J = 0, K = 1$
- (D) $J = K = T$

[IES – EE – 2006]

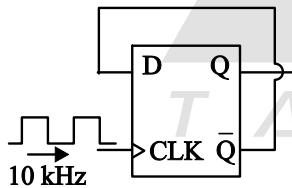
- (12) What is represented by the digital circuit given below?



- (A) An SR flip-flop with $A = S$ and $B = R$
- (B) A JK flip-flop with $A = K$ and $B = J$
- (C) A JK flip-flop with $A = J$ and $B = K$
- (D) An SR flip-flop with $A = R$ and $B = S$

[GATE – EE – 2002/IES - EE - 2007]

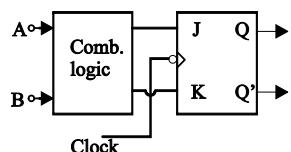
- (13) The frequency of the clock signal applied to the rising edge triggered D flip-flop shown in the above figures is 10 kHz. What is the frequency of the signal available at Q?



- (A) 2.5 kHz
- (B) 5 kHz
- (C) 10 kHz
- (D) 20 kHz

[IES – EE – 2008]

- (14) The following truth table has to be realized with the circuit shown in the figure:



A	B	Q_{n+1}
0	0	Q_n
0	1	1
1	0	Q_n
1	1	0

What is the output of the combinational logic circuit to the J input?

- (A) \overline{AB}
- (B) \overline{A}
- (C) \overline{B}
- (D) AB

[IES – EE – 2010]

- (15) Assertion(A):

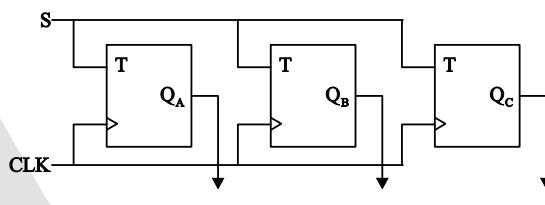
D flip-flops are used to construct a buffer registers.

Reason(R):

Buffer registers are used to store binary word temporarily.

[IES – EC – 1991]

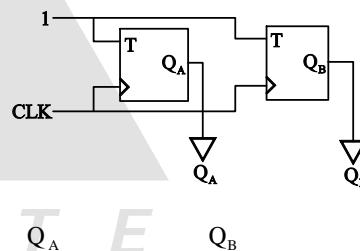
- (16) Find radix of the system shown in the figure below



- (A) 2
- (B) 4
- (C) 6
- (D) 8

[IES – EC – 1991]

- (17) What will be the state of the output after the third clock cycle?



- (A) LO LO
- (B) HI LO
- (C) LO HI
- (D) HI HI

[IES – EC – 1992]

- (18) The race around condition exists in J – K flip-flop if

- (A) $J = 0; K = 1$
- (B) $J = 0; K = 1$
- (C) $J = 0; J = 0$
- (D) $J = 1; K = 1$

[IES – EC – 1992]

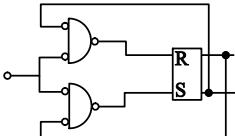
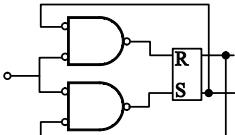
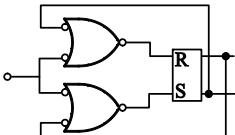
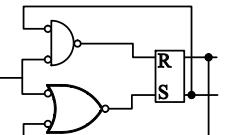
- (19) In a JK flip – flop, the output Q_n is 1 and it does not change when a clock pulse applied.

The possible combination of J_n and K_n could be (x denotes don't care)

- (A) x and 0 (B) x and 1
 (C) 0 and x (D) 1 and x

[IES – EC – 1994]

- (20) Which one of the following circuits converts an RS flip flop to T flip flop?

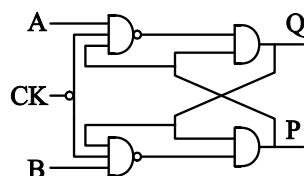
- (A) 
 (B) 
 (C) 
 (D) 

[IES – EC – 1994/2013]

- (21) In a sequential circuits, the output at any instant of time depend
- (A) Only on the inputs present at that instant of time
 (B) On past output as well as present inputs
 (C) Only on the past inputs
 (D) Only on the past outputs

[IES – EC – 1995]

- (22) Given $A = 1$, $B=1$, $Q_n = 0$ and $P_n = 1$ what will be output Q_{n+1} and P_{n+1} when the clock input (CK) is applied?



- (A) $Q_{n+1} = 0, P_{n+1} = 0$
 (B) $Q_{n+1} = 0, P_{n+1} = 1$
 (C) $Q_{n+1} = 1, P_{n+1} = 0$
 (D) $Q_{n+1} = 1, P_{n+1} = 1$

[IES – EC – 1995]

- (23) Which of the following characteristics are necessary for sequential circuits?

1. It must have at least six gates

2. It must have some feedback

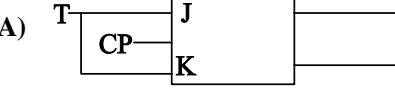
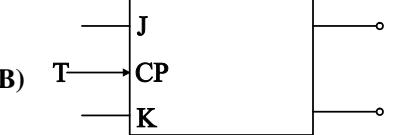
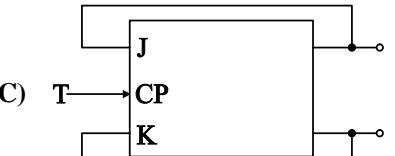
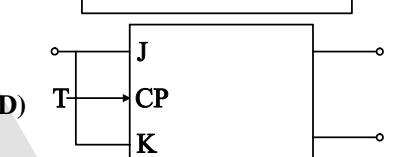
3. Its output should depend on some past value.

Codes :

- (A) 1, 2 and 3 (B) 1 and 2
 (C) 2 and 3 (D) 1 and 3

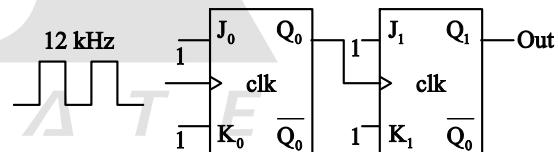
[IES – EC – 1995]

- (24) Which one of the circuits given below converts a JK F/F to a T F/F?

- (A) 
 (B) 
 (C) 
 (D) 

[IES – EC – 1995]

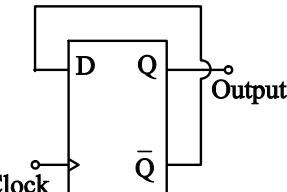
- (25) An input frequency of 12 KHz is applied to the J – K flips – flop arrangement shown in the given figure. The resulting output frequency will be



- (A) 24 KHz (B) 12 KHz
 (C) 6 KHz (D) 3 KHz

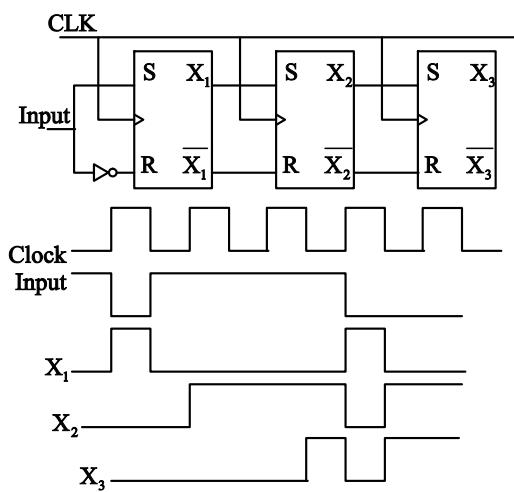
[IES – EC – 1996/2007/2015]

- (26) For the circuits shown in the given figure, the frequency of the output Q will be.



- (A) Twice the input clock frequency
 (B) Half the input clock frequency
 (C) Same as the input clock frequency
 (D) Inverse of the propagation delay of the EF

- (27) Shift register with associated waveform is shown in the following figure: Which of these is/are correct?



- (A) X_1 alone (B) X_2 alone
 (C) X_3 alone (D) X_1, X_2 and X_3

[IES – EC – 2000]

- (28) A T- flip – flop function is obtained from a JK flip – flop. If the flip – flop belongs to a TTL family, the connection needed at the input must be

- (A) $J = K = 1$ (B) $J = K = 0$
 (C) $J = 1$ and $K = 0$ (D) $J = 0$ and $K = 1$

[IES – EC – 2012]

- (29) The characteristic equation of the T-flip-flop is given by

- (A) $Q^+ = TQ + \bar{T}\bar{Q}$
 (B) $Q^+ = \bar{T}Q + QT$
 (C) $Q^+ = T + Q$
 (D) $Q^+ = T\bar{Q}$

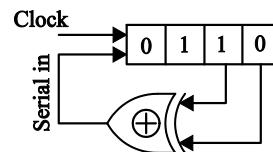
[IES – EC – 2003/2007]

- (30) The characteristic equation for the next state (Q_{n+1}) of a J-K flip-flop is

- (A) $Q_{n+1} = JQ_n + K\bar{Q}_n$
 (B) $Q_{n+1} = \bar{J}\bar{Q}_n + \bar{K}Q_n$
 (C) $Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$
 (D) $Q_{n+1} = JQ_n + KQ_n$

[GATE– EC – 1992]

- (31) The initial contents of the 4-bit serial-in parallel-out, right shift, shift register as shown in figure above are 0110. After 3 clock pulses, the contents of the shift register will be

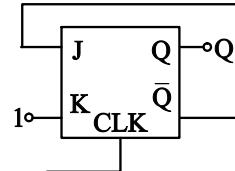


- (A) 0000 (B) 0101
 (C) 1010 (D) 1110

[GATE – EC – 1997]

- (32) Consider the following J-K flip-flop :

In the given J-K flip-flop,



$J = \bar{Q}$ and $K = 1$. Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

- (A) 010000 (B) 011001
 (C) 010010 (D) 010101

[IES – EC – 2005]

- (33) Match List-I (Type of flip-flop) with List-II (Symbol) and select the correct answer using the code given below the lists :

List-I

- A. T flip-flop
 B. Level-triggered JK flip-flop
 C. Leading edge-triggered JK flip-flop
 D. Trailing edge-triggered JK flip-flop

List II

- 1.
- 2.
- 3.
- 4.

Codes :

- | A | B | C | D |
|-------------|---|---|---|
| (A) 1 2 3 4 | | | |
| (B) 2 1 3 4 | | | |
| (C) 1 2 4 3 | | | |
| (D) 2 1 4 3 | | | |

[IES – EC – 2009]

- (38) Match List I with List II and select the correct answer using the code given below the lists:

List I**(Application of Circuit)**

1. Divider
2. Clips input voltage at two predetermined levels
3. Square wave generator
4. Narrow current pulse generator

List II**(Circuit Name)**

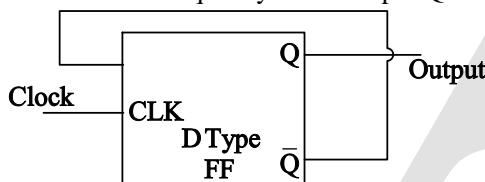
1. Astable multivibrator
2. Schmitt trigger
3. Bistable multivibrator
4. Blocking oscillator

Codes:**A B C D**

- | A | B | C | D |
|-------------|---|---|---|
| (A) 4 2 1 3 | | | |
| (B) 3 2 1 4 | | | |
| (C) 4 1 2 3 | | | |
| (D) 3 1 2 4 | | | |

[IES – EC – 2009]

- (35) For the circuit shown in the figure below, what is the frequency of the output Q?



- (A) Twice the input clock frequency
- (B) half the input clock frequency
- (C) Same as the input clock frequency
- (D) Inverse of the propagation delay of the FF

AB [IES – EC – 2008]

- (36) Assertion(A):

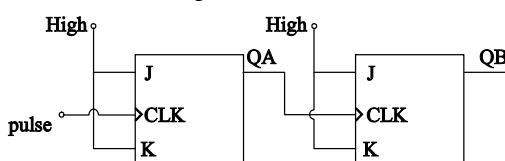
D-Flip-Flops are used as buffer register.

Reason (R):

D-Flip-Flops are free from “race-around” condition.

[IES – EC – 2008]

- (37) The circuit is given below illustrates a typical application of the JK flip-flops. What does this represent?



- (A) A shift register
- (B) A data storage device
- (C) A frequency divider circuit
- (D) A decoder circuit

- (39) Which of the following conditions should be satisfied to call an astable multivibrator circuit using discrete components as a digital circuit?

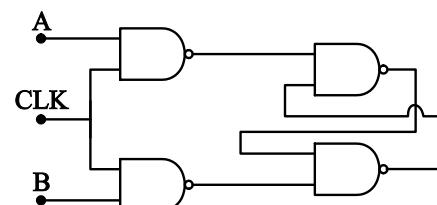
1. A flip-flop is always a digital circuit.
2. Only when we assign 1 and 0 to the high and low levels of the output, a flip-flop is called a digital circuit.
3. Only if the power supply voltage is maintained at +5V or -5V, it is called a digital circuit.
4. Only if it is in IC form, following the technology of IC manufacture, it is called a digital circuit.

Select the correct answer from the codes given below:

- | | |
|------------|-------------|
| (A) 1 only | (B) 2 and 3 |
| (C) 2 only | (D) 3 and 4 |

[GATE-EC/EE/IN-2012]

- (40) Consider the given circuit.



In this circuit, the race around

- (A) Does not occur
- (B) Occurs when $\text{CLK} = 0$
- (C) Occurs when $\text{CLK} = 1$ and $A = B = 1$
- (D) Occurs when $\text{CLK} = 1$ and $A = B = 0$

[IES – EC – 2009]

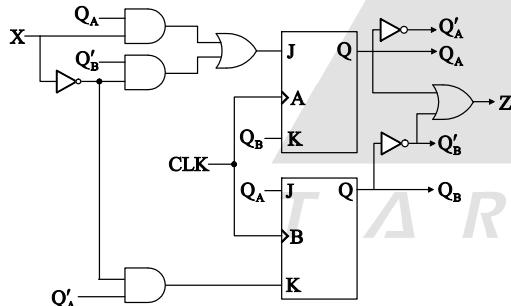
- (41) Which of the following capabilities are available in a Universal Shift Register?
1. Shift left
 2. Shift right
 3. Parallel load
 4. Serial add

Select the correct answer from the codes given below:

- (A) 2 and 4 only
- (B) 1, 2 and 3
- (C) 1, 2 and 4
- (D) 1, 3 and 4

[IES – EC – 2010]

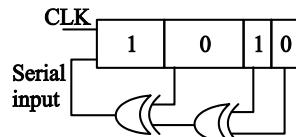
- (42) Analyze the sequential circuit shown above in figure. Assuming that initial sequence would lead to state 11?



- (A) 1 – 1
- (B) 1 – 0
- (C) 0 – 0
- (D) State 11 is unreachable

[GATE – EE – 2003]

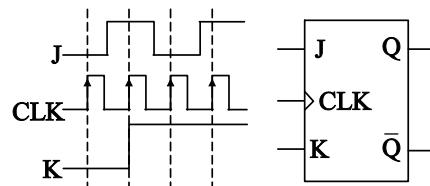
- (43) The shift register shown in the given figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (msb). After how many clock pulses will be content of the shift register become 1010 again?



- (A) 3
- (B) 7
- (C) 11
- (D) 15

[IES – EC – 2010]

- (44) The J-K flip-flop shown below is initially rest, so that $Q = 0$. If a sequence of four clock pulses is then applied, with the J and K inputs as given in the figure, the resulting sequence of values that appear at the output Q starting with its initial state, is given by



- (A) 01011
- (B) 01010
- (C) 00110
- (D) 00101

[GATE – EE – 2003]

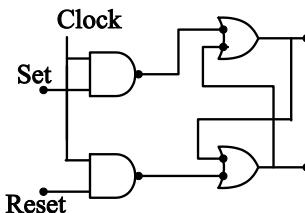
- (45) An X-Y flip flop, whose characteristic table is given below is to be implemented using J-K flip flop. This can be done by making

X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	\bar{Q}_n
1	1	0

- (A) $J = X, K = \bar{Y}$
- (B) $J = \bar{X}, K = Y$
- (C) $J = Y, K = \bar{X}$
- (D) $J = \bar{Y}, K = X$

[GATE - IN - 2004]

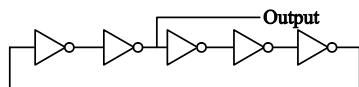
- (46) The two NAND gates before the latch circuit shown in Fig. are used to



- (A) act as buffers
- (B) operate the latch faster
- (C) avoid racing problem
- (D) invert the latching action

- [GATE - IN - 2008]

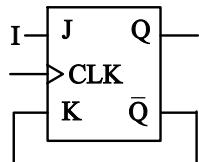
(47) The inverters in the ring oscillator circuit shown below are identical. If the output waveform has a frequency of 10 MHz, the propagation delay of each inverter is



- (A) 5ns
 - (B) 10ns
 - (C) 20ns
 - (D) 50ns

[GATE - IN - 2009]

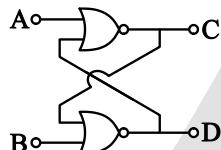
- (48) In the figure shown, the initial state of Q is 0. The output is observed after the application of each clock pulse. The output sequence at Q is



- (A) 0000... (B) 1010...
(C) 1111... (D) 1000...

[GATE - IN - 2001]

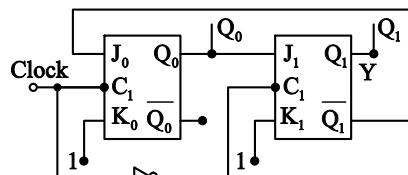
- (49) In the circuit shown in Fig. when inputs A = B = 0, the possible logic states of C and D are



- (A) $C = 0, D = 1$ or $C = 1, D = 0$
 - (B) $C = 1, D = 1$ or $C = 0, D = 0$
 - (C) $C = 1, D = 0$
 - (D) $C = 0, D = 1$

[GATE - IN - 2003]

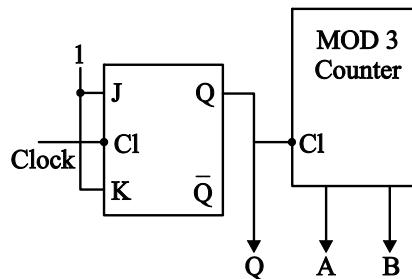
- (50) The correct cyclic sequence of the outputs (Q_0 , Q_1) for the JK master – slave flip – flop circuit shown in Fig. when the input clock is applied is



- (A) 00, 01, 10, 11, 00, 01,
 - (B) 00, 10, 01, 00, 10, 01,
 - (C) 00, 01, 10, 00, 01, 10, ...
 - (D) None

[GATE - IN - 2004]

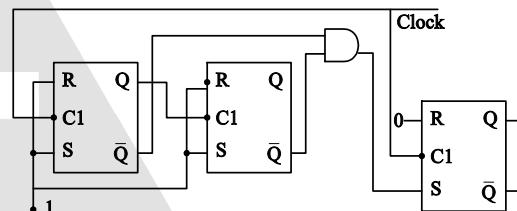
- (51) In Fig. initially $Q = A = B = 0$. After three clock triggers, the state of Q , A and B will be respectively



- (A) 110
 - (B) 011
 - (C) 011
 - (D) 101

[GATE - IN - 2004]

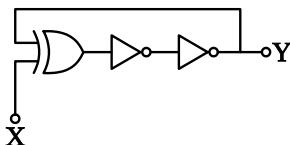
- (52) In the digital circuit shown in Fig. the flip flops have set time of 5 ns and a worst case delay of 15 ns. The AND gate has a delay of 5 ns. Maximum possible clock rate for the circuit to operate faithfully is



- (A) 21 MHz (B) 2 MHz
(C) 25 MHz (D) 30 MHz

[GATE - IN - 2006]

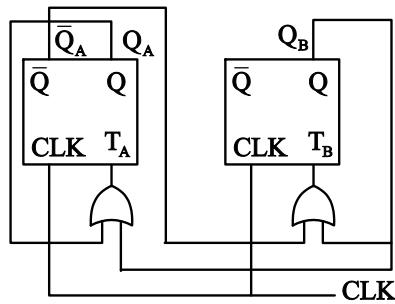
- (53) All the logic gates in the circuit shown below have finite propagation delay. The circuit can be used as a clock generator, if



- (A) $X = 0$ (B) $X = 1$
(C) $X = 0$ or 1 (D) $X = Y$

[GATE - IN - 2007]

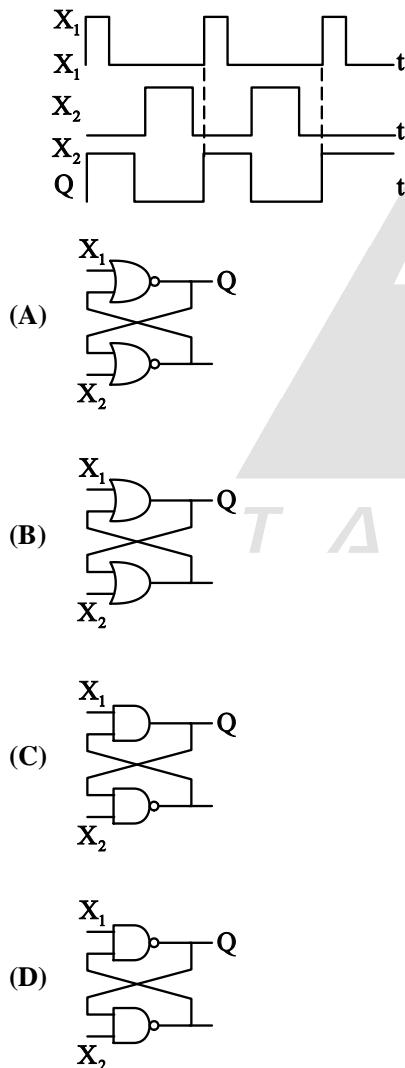
- (54) A sequential circuit is shown in the figure below. Let the state of the circuit be encoded as Q_AQ_B . The notation $X \rightarrow Y$ implies that state Y is reachable from state X in a finite number of clock transitions. Identify the INCORRECT statement.



- (A) $01 \rightarrow 00$
- (B) $11 \rightarrow 01$
- (C) $01 \rightarrow 11$
- (D) $01 \rightarrow 10$

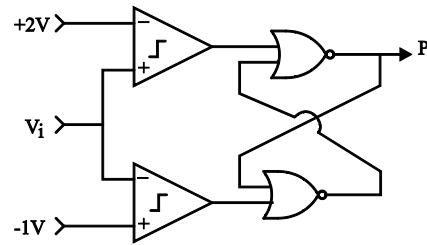
[GATE - EE - 2005]

- (55) Select the circuit which will produce the given output Q for the input signals X_1 and X_2 given in the figure.



[GATE - EC - 1987]

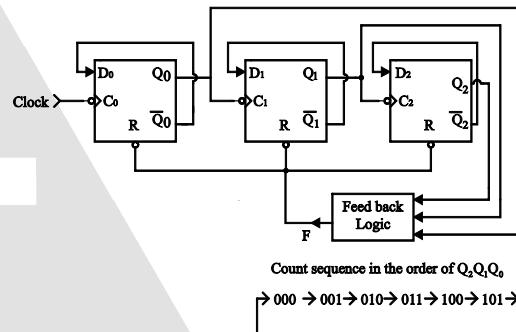
- (56) Choose the correct statements relating to the circuit of figure



- (A) For $V_i = -2v, P = 0$
- (B) For $V_i = +3v, P = 0$
- (C) For $V_i = 0_v, P = 0$ always
- (D) For $V_i = 0_v, P$ can be either 0 or 1.

[GATE -EC - 1987]

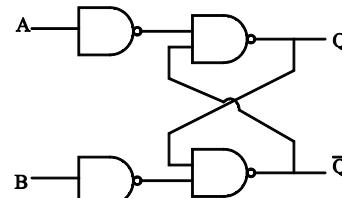
- (57) A ripple counter using negative edge-triggered D-flip flops is shown in Fig. The flip-flops are cleared to '0' at the R input. The feedback logic is to be designed to obtain the count sequence shown in the same figure. The correct feedback logic is:



- (A) $F = \overline{Q_2} \overline{Q_1} \overline{Q_0}$
- (B) $F = Q_2 \overline{Q_1} \overline{Q_0}$
- (C) $F = \overline{Q_2} Q_1 \overline{Q_0}$
- (D) $F = \overline{Q_2} \overline{Q_1} \overline{Q_0}$

[GATE -EC - 1988]

- (58) The circuit given below is a



- (A) J-K Flip-flop
- (B) Johnson's counter.
- (C) R-S latch
- (D) None of above

[GATE -EC - 1994]

- (59) Synchronous counters are _____ than the ripple counters.

[GATE -EC - 1995]

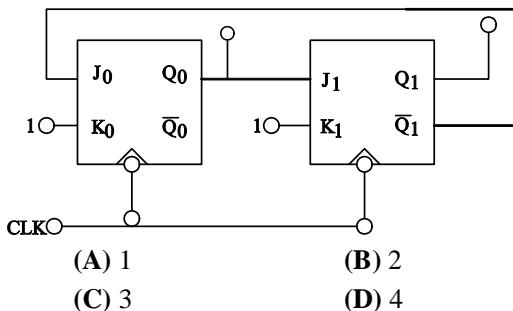
- (60) A switch-tail ring counter is made by using a single D flip-flop. The resulting circuit is a

- (A) SR flip-flop
 (C) D flip-flop

- (B) JK flip-flop
 (D) T flip-flop

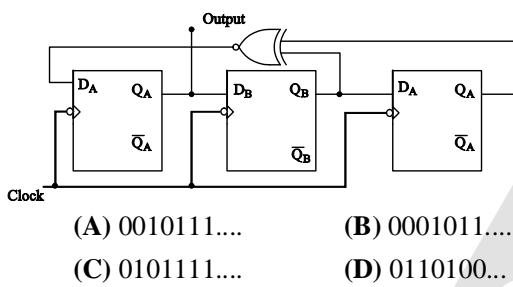
[GATE -EC - 1998]

- (61) Figure shows a mod-K counter, Here K is equal to



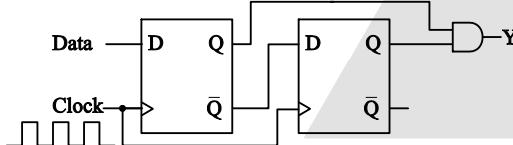
[GATE -EC - 2010]

- (62) Assuming that all flip-flops are in reset condition initially, the count sequence observed at Q_A in the circuit shown is



[GATE -EC - 2011]

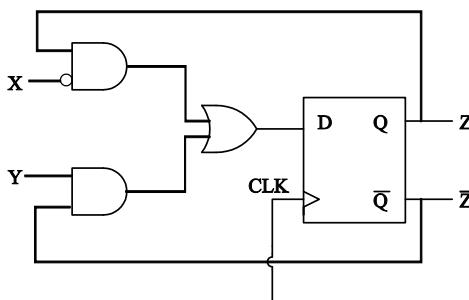
- (63) When the output Y in the circuit below is "1", it implies that data has



- (A) changed from "0" to "1"
 (B) changed from "1" to "0"
 (C) changed in either direction
 (D) not changed

[GATE -EC - 2000]

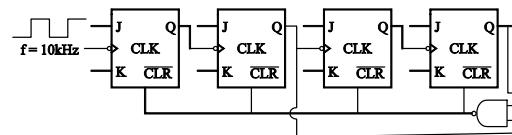
- (64) A sequential circuit using D Flip-flop and logic gates is shown in the figure, where X and Y are the inputs and Z is the output. The circuit is :



- (A) S-R Flip-flop with inputs X = R and Y = S
 (B) S-R Flip-flop with inputs X = S and Y = R
 (C) J-K Flip-flop with inputs X = J and Y = K
 (D) J-K Flip-flop with inputs X = K and Y = J

[GATE -EC - 2000]

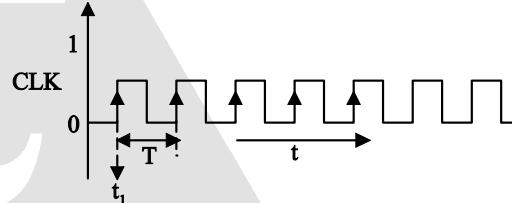
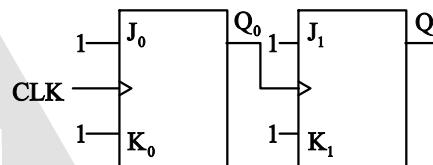
- (65) In the figure, the J and K inputs of all the four flip-flops are made high. The frequency of the signal at output Y is



- (A) 0.833 KHz (B) 1.0 KHz
 (C) 0.91 KHz (D) 0.77 KHz

[GATE -EC - 2008]

- (66) For each of the positive edge-triggered J-K flip-flop used in the following figure, the propagation delay is ΔT



Which of the following waveforms correctly represents the output at Q_1 ?

- (A)
 (B)
 (C)
 (D)

- | | |
|--|--|
| <p>(67) The output Q_n of a J-K flip-flop is zero. It changes to 1 when a clock pulse is applied. The input J_n and K_n are respectively</p> <p>(A) 1 and X (B) 0 and X
 (C) X and 0 (D) X and 1</p> <p style="text-align: center;">[IES - EC - 1997]</p> <p>(68) A J.K flip-flop can be made from an S-R flip-flop by using two additional</p> <p>(A) AND gates (B) OR gates
 (C) NOT gates (D) NOR gates</p> <p style="text-align: center;">[IES - EE - 2008]</p> <p>(69) Which of the following is not a characteristic of a flip flop?</p> <p>(A) The flip – flop is a bi – stable device with only two stable states
 (B) The flip – flop has two input signals
 (C) The flip – flop has two output signals
 (D) The outputs are complement of each other</p> <p style="text-align: center;">[IES - EC - 1992]</p> <p>(70) By placing an inverter between both inputs of an S-R flip-flop, the resulting flip - flop becomes</p> <p>(A) J-K flip-flop
 (B) D- flip-flop
 (C) T - flip-flop
 (D) Master slave JK flip-flop</p> <p style="text-align: center;">[IES - EC - 1992]</p> <p>(71) A $1 \mu s$ pulse can be converted into a $1 ms$ pulse by using</p> <p>(A) A mono stable multivibrator
 (B) An astable multivibrator
 (C) A bi – stable multivibrator
 (D) A J – K flip – flop</p> <p style="text-align: center;">[IES - EC - 2003]</p> <p>(72) The output of a Moore sequential machine is a function of</p> <p>(A) All present states of the machine
 (B) All the inputs
 (C) A few combination of inputs and the present state
 (D) All the combinations of inputs and the present state</p> <p style="text-align: center;">[IES - EC - 2001]</p> <p>(73) The 54/74164 chip is an 8-bit serial-input-parallel-output shift register. The clock is 1MHz. The time needed to shift an 8-bit binary number into the chip is</p> | <p>(A) $1\mu s$ (B) $2\mu s$
 (C) $8\mu s$ (D) $16\mu s$</p> <p>(74) Consider the following statements regarding registers and latches:</p> <ol style="list-style-type: none"> 1. Registers are made of edge-triggered FFs, whereas latches are made from level-triggered FFs. 2. Registers are temporary storage devices whereas latches are not. 3. A latch employs cross- coupled feedback connections. 4. A register stores a binary word whereas a latch does not. <p>Which of the above statements is/are correct?</p> <p>(A) 1 only (B) 1 and 3
 (C) 2 and 3 (D) 3 and 4</p> <p>(75) Consider the following statements:</p> <ol style="list-style-type: none"> 1. A flip-flop is used to store 1-bit of information. 2. Race-around condition occurs in a J-K flip-flop when both the inputs are 1. 3. Master-slave configuration is used in flip-flops to store 2-bits of information. 4. A transparent latch consists of a D-type flip-flop. <p>Which of the above statements is/are correct?</p> <p>(A) 1 only (B) 1, 3 and 4
 (C) 1, 2 and 4 (D) 2 and 3 only</p> <p>(76) Consider the following statements regarding registers and latches :</p> <ol style="list-style-type: none"> 1. Registers are temporary storage devices, whereas latches are not. 2. A latch employs cross-coupled feedback connections. 3. A register stores a binary word, whereas a latch does not. <p>The correct statement(s) is/are</p> <p>(A) 1 only (B) 2 only
 (C) 1 and 3 (D) 2 and 3</p> <p style="text-align: right;">[GATE - EE - 1995]</p> <p>(77) For a J-K flip-flop its J input is tied to its own Q output and its K input is connected to its own Q output. If the flip-flop is fed with a clock of frequency 1 MHz, its Q output frequency will be _____.</p> |
|--|--|

[IES -EC - 1992]

- (78) Which of the following flip – flop cannot be converted to D – type (Delay) flip – flop
- S – R flip flop
 - J – K flip flop
 - Master slave flip flop
 - None of the above

[IES -EC - 1997]

- (79) For the design of sequential circuits having nine state MINIMUM number of memory elements required is:

- | | |
|-------|-------|
| (A) 3 | (B) 4 |
| (C) 5 | (D) 9 |

[IES -EC - 2002]

- (80) A sequence detector is required to given a logical output of 1 whenever the sequence 1011 is detected in the incoming pulse stream. Minimum number of flip-flops needed to build the sequence detector is :

- | | |
|-------|-------|
| (A) 4 | (B) 3 |
| (C) 2 | (D) 1 |

[IES -EC - 2006]

- (81) A master slave configuration consists of two identical flip-flops connected in such a way that the output of the master is input to the slave.

Which one of the following is correct?

- Master is level triggered and slave is edge triggered
- Master is edge triggered and slave is level triggered
- Master is positive edge triggered and slave is negative edge triggered
- Master is negative edge triggered and slave is positive edge triggered

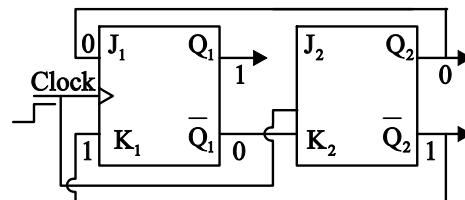
[GATE – EC – 2004]

- (82) A master slave flip-flop has the characteristic that
- change in the input immediately effected in the output
 - change in the output occurs when the state of the master is affected
 - change in the output occurs when the state of the slave is affected
 - both the master and the slave states are affected at the same time.

[GATE-IN-1993]

- (83) A sequential circuit formed by two edge triggered JK flip flops is shown in figure. If the states before the arrival of a clock edge

are $Q_1 = 1$, $Q_2 = 0$, the states after the arrival of the clock edge are $Q_1 = \dots$, $Q_2 = \dots$.



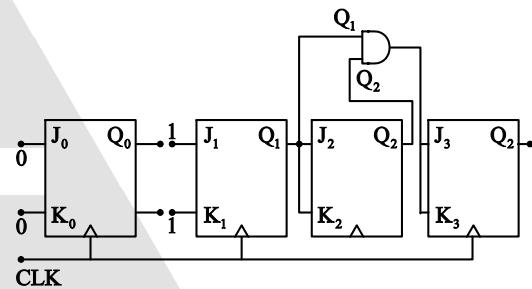
[GATE-IN-1994]

- (84) The output Q_{n+1} of a J-K flip-flop for the input $J=1$, $K=1$ is

- | | |
|-----------|-----------------|
| (A) 0 | (B) 1 |
| (C) Q_n | (D) \bar{Q}_n |

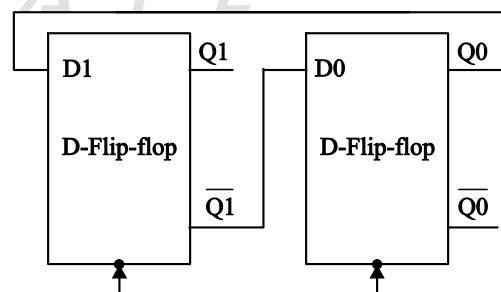
[GATE-IN-1995]

- (85) Figure shows a sequential circuit with four J-K flip-flops. Generate a table of output ($Q_3 Q_2 Q_1 Q_0$) changes with each clock pulse. Start with $Q_3 Q_2 Q_1 Q_0 = 0001$ and complete a full cycle.



[GATE-IN-2013]

- (86) The digital circuit shown below uses two negative edge-triggered D-flip-flops. Assuming initial condition of Q_1 and Q_0 as zero, the output Q_1, Q_0 of this circuit is



- (A) 00, 01, 10, 11, 00 ...

- (B) 00, 01, 11, 10, 00 ...

- (C) 00, 11, 10, 01, 00 ...

- (D) 00, 01, 11, 11, 00 ...

[GATE-EC-1991]

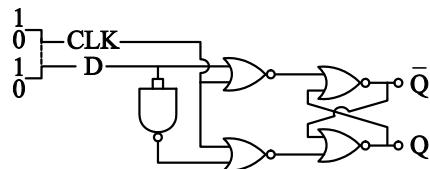
- (87) An S-R FLIP-FLOP can be converted into a T FLIP-FLOP by connecting to _____ Q and _____ to \bar{Q} .

[GATE-EC-2005]

- (88) The present output Q_n of an edge triggered JK flip-flop is logic 0. If J = 1, then Q_{n+1}
- cannot be determined
 - will be logic 0
 - will be logic 1
 - will race around

[GATE-EC-2008]

- (89) For the circuit shown in the figure, D has a transition from 0 to 1 after CLK changes from 1 to 0. Assume gate delays to be negligible

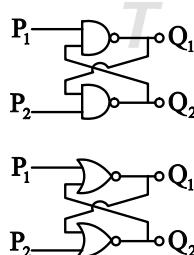


Which of the following statements is true ?

- Q goes to 1 at the CLK transition and stays at 1.
- Q goes to 0 at the CLK transition and stays at 0.
- Q goes to 1 at the CLK transition and goes to 0 when D goes to 1.
- Q goes to 0 at the CLK transition and goes to 1 when D goes to 1.

[GATE-EC-2009]

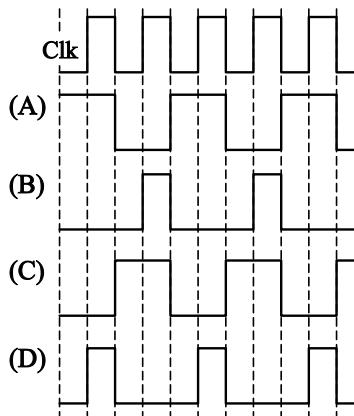
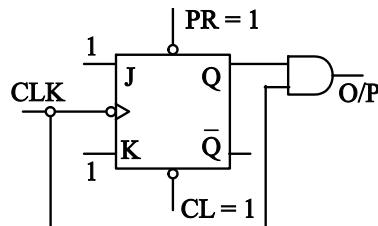
- (90) Refer to the NAND and NOR latches shown in the figure. The inputs (P_1, P_2) for both the latches are first made (0, 1) and then, after a few seconds, made (1, 1). The corresponding stable outputs (Q_1, Q_2) are



- NAND: first (0, 1) then (0, 1) NOR: first (1, 0) then (0, 0)
- NAND: first (1, 0) then (0, 1) NOR: first (1, 0) then (0, 0)
- NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (0, 0)
- NAND: first (1, 0) then (1, 1) NOR: first (1, 0) then (0, 1)

[GATE-EE-2004]

- (91) The digital circuit shown in figure generates a modified clock pulse at the output. Choose the correct output waveform from the options given below.

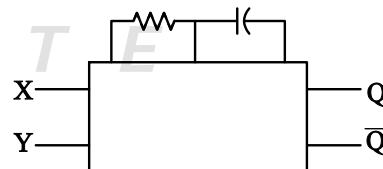


[GATE-EE-2008]

- (92) The truth table of a monoshot shown in the figures is given in the table below :

Two monoshots, one positive edge triggered and other negative edge triggered, are connected shown in the figure. The pulse widths of the two monoshot outputs, Q_1 and Q_2 are and T_{ON1} and T_{ON2} respectively.

X	Y	Q	\bar{Q}
0	↑	↑	↓
↓	1	↓	↑



The frequency and the duty cycle of the signal of Q_1 will respectively be

$$(A) f = \frac{1}{T_{ON_1} + T_{ON_2}}, D = \frac{T_{ON_1}}{T_{ON_1} + T_{ON_2}}$$

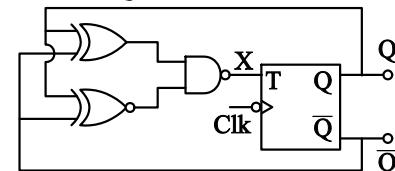
$$(B) f = \frac{1}{T_{ON_1} + T_{ON_2}}, D = \frac{T_{ON_2}}{T_{ON_1} + T_{ON_2}}$$

$$(C) f = \frac{1}{T_{ON_1}}, D = \frac{T_{ON_1}}{T_{ON_1} + T_{ON_2}}$$

$$(D) f = \frac{1}{T_{ON_2}}, D = \frac{T_{ON_1}}{T_{ON_1} + T_{ON_2}}$$

[GATE-EE-2013]

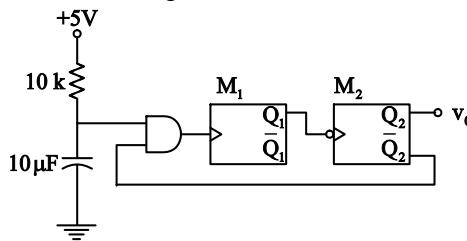
- (93) The clock frequency applied to the digital circuit shown in figure below is 1 kHz. If the initial state of the output Q of the flip-flop is '0', then the frequency of the output waveform Q in kHz is



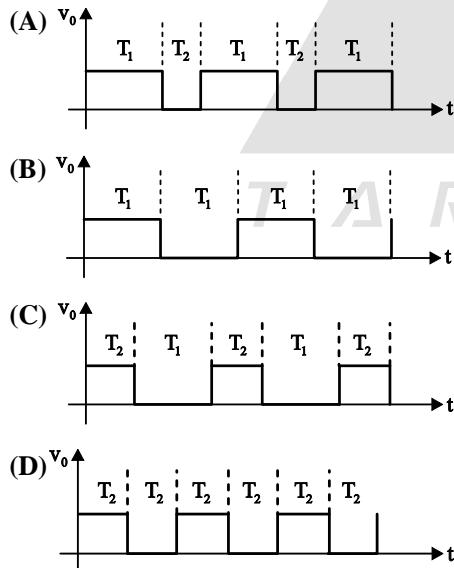
- (A) 0.25 (B) 0.5
 (C) 1 (D) 2

[GATE-EE-2014]

- (94) Two monoshot multivibrators, one positive edge triggered (M_1) and another negative edge triggered (M_2), are connected as shown in figure.

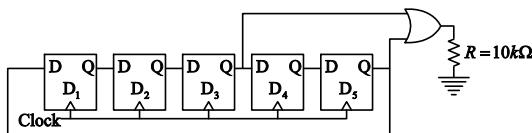


The monoshot M_1 and M_2 when triggered produce pulses of width T_1 and T_2 respectively, where $T_1 > T_2$. The steady state output voltage V_0 of the circuit is



[GATE-S3-EC-2016]

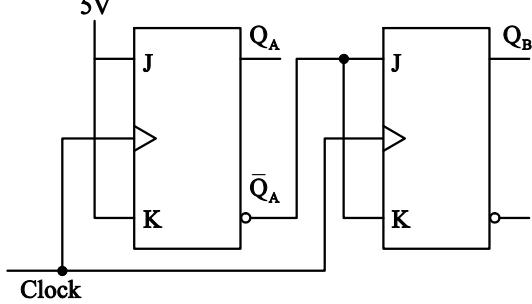
- (95) Assume that all the digital gates in the circuit shown in the figure are ideal, the resistor $R = 10 \text{ k}\Omega$ and the supply voltage is 5 V. The D flip-flops D_1, D_2, D_3, D_4 and D_5 are initialized with logic values 0, 1, 0, 1 and 0, respectively. The clock has a 30% duty cycle.



The average power dissipated (in mW) in the resistor R is _____

[GATE-S6-EE-2016]

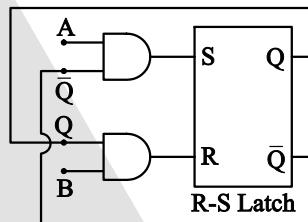
- (96) The current state $Q_A Q_B$ of a two JK flip-flop system is 00. Assume that the clock rise-time is much smaller than the delay of the JK flip-flop. The next state of the system is



- (A) 00 (B) 01
 (C) 11 (D) 10

[GATE – IN – 2017]

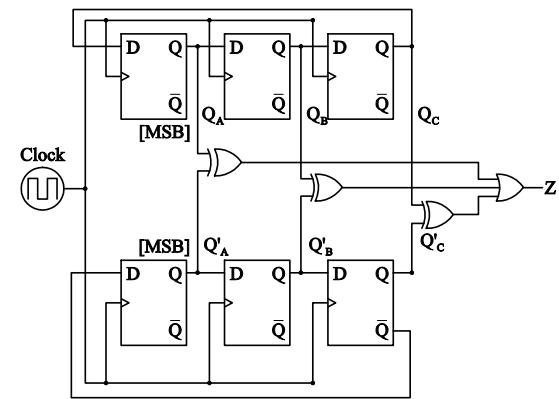
- (97) The two inputs A and B are connected to an R-S latch via two AND gates as shown in the figure. If $A = 1$ and $(B = 0)$, the output $Q\bar{Q}$ is



- (A) 00 (B) 10
 (C) 01 (D) 11

[GATE-S2-EE-2017]

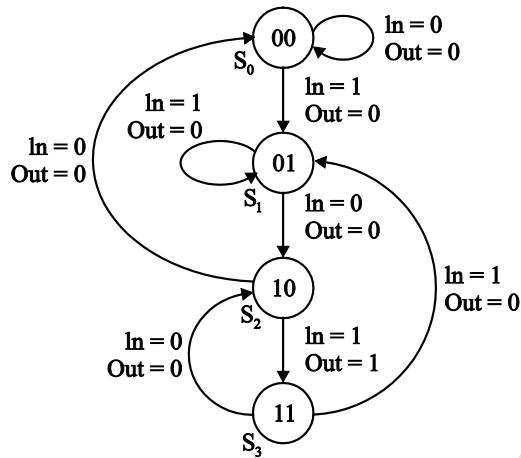
- (98) For the synchronous sequential circuit shown below, the output Z is zero for the initial conditions $Q_A Q_B Q_C = Q'_A Q'_B Q'_C = 100$.



The minimum number of clock cycles after which the output z would again become zero is _____.

[GATE-S2-EC-2017]

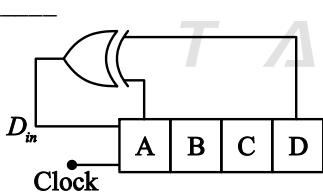
- (99) The state diagram of a finite state machine (FSM) designed to detect an overlapping sequence of three bits is shown in the figure. The FSM has an input 'In' and an output 'Out'. The initial state of the FSM is S_0 .



If the input sequence is 10101101001101, starting with the left-most bit, then the number of times 'Out' will be 1 is _____.

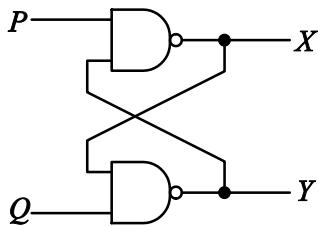
[GATE-S1-EC-2017]

- (100) A 4-bit shift register circuit configured for right-shift operation, i.e. $D_{in} \rightarrow A, A \rightarrow B, B \rightarrow C, C \rightarrow D$, is shown. If the present state of the shift register is ABCD = 1101, the number of clock cycles required to reach the state ABCD = 1111 is _____.



[GATE-S1-EC-2017]

- (101) In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is: P = Q = '0'. If the input condition is changed simultaneously to P = Q = '1', the outputs X and Y are



(A) X = '1', Y = '1'

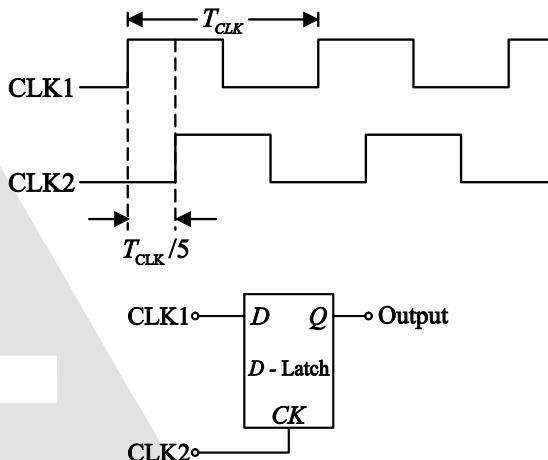
(B) either X = '1', Y = '0' or X = '0', Y = '1'

(C) either X = '1', Y = '1' or X = '0', Y = '0'

(D) X = '0', Y = '0'

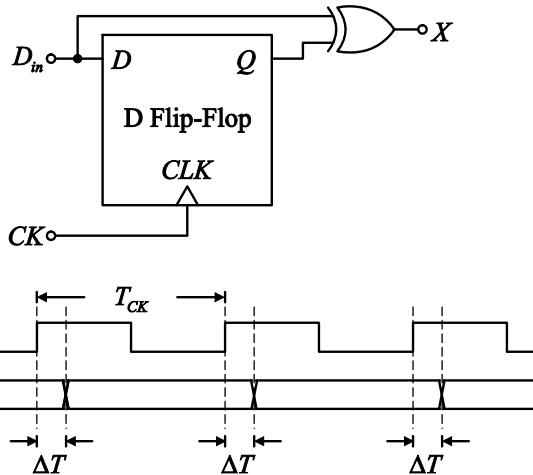
[GATE-S1-EC-2017]

- (102) Consider the D-Latch shown in the figure, which is transparent when its clock input CK is high and has zero propagation delay. In the figure, the clock signal CLK1 has a 50% duty cycle and CLK2 is a one-fifth period delayed version of CLK1. The duty cycle at the output of the latch in percentage is _____.



[GATE - EC - 2018]

- (103) In the circuit shown below, a positive edge-triggered D Flip-Flop is used for sampling input data D_{in} using clock CK . The XOR gate outputs 3.3 volts for logic HIGH and 0 volts for logic LOW levels. The data bit and clock periods are equal and the value of $\Delta T / T_{CK} = 0.15$, where the parameters ΔT and T_{CK} are shown in the figure. Assume that the Flip-Flop and the XOR gate are ideal.



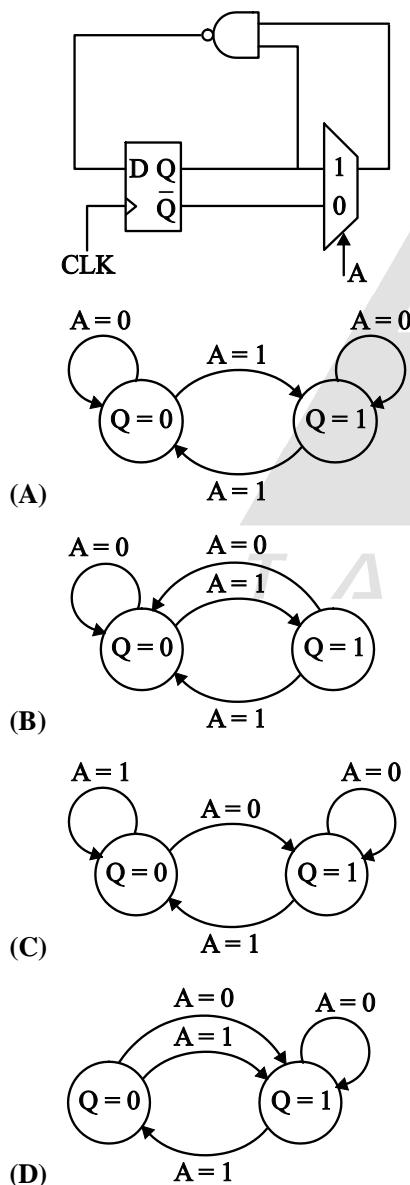
If the probability of input data bit (D_{in}) transition in each clock period is 0.3, the average value (in volts, accurate to two decimal places) of the voltage at node X, is _____.

[GATE – EC – 2018]

- (104) A traffic signal cycles from GREEN to YELLOW, YELLOW to RED and RED to GREEN. In each cycle, GREEN is turned on for 70 seconds, YELLOW is turned on for 5 seconds and the RED is turned on for 75 seconds. This traffic light has to be implemented using a finite state machine (FSM). The only input to this FSM is a clock of 5 second period. The minimum number of flip-flops required to implement this FSM is _____.

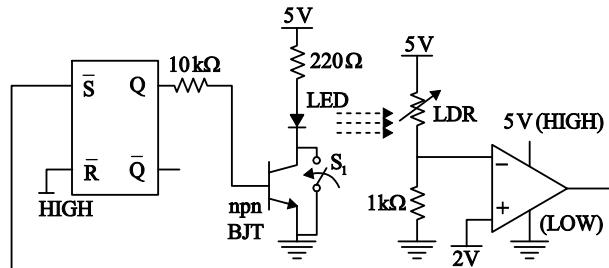
[GATE-EC-2019]

- (105) The state transition diagram for the circuit shown is



[GATE-IN-2019]

- (106) In the circuit below, the light dependent resistor (LDR) receives light from the LED. The LDR has resistances of $5k\Omega$ and 500Ω under dark and illuminated conditions, respectively. The LED is OFF at time $t < 0$. At time $t = 0$ s, the switch S_1 is closed for 1 ms and then kept open thereafter. Assuming zero propagation delay in the devices, the LED



- (A) turns ON when S_1 is closed and remains ON after S_1 is opened
 (B) turns ON when S_1 is closed and turns OFF after S_1 is opened
 (C) turns ON when S_1 is closed and toggles periodically from ON to OFF after S_1 is opened
 (D) remains OFF when S_1 is closed and continues to remain OFF after S_1 is opened.

-----0000-----

06

Semiconductor Memories

- [GATE - EE - 2009]

[GATE - EE - 2009]

- for the following devices

 - (i) Cache Memory
 - (ii) CDROM
 - (iii) Dynamic RAM
 - (iv) Processor Registers
 - (v) Magnetic Tape

(A) (v), (ii), (iii), (iv), (i)

(B) (v), (ii), (iii), (i), (iv)

(C) (ii), (i), (iii), (iv), (v)

(D) (v), (ii), (i), (iii), (iv)

[GATE -EC - 1994]

- (2) A PLA can be

 - (A) as a microprocessor
 - (B) as a dynamic memory
 - (C) to realize a sequential logic
 - (D) to realize a combinational logic.

[GATE -EC - 1994]

- (3) A dynamic RAM consists of
(A) 6 transistors
(B) 2 transistors and 2 capacitors
(C) 1 transistor and 1 capacitor
(D) 2 capacitors only

[GATE -EC - 1995]

[GATE -EC - 2001]

[IES - EC - 1992]

- (6) The number of NAND gate required for two dimensional addressing of 256×8 bit ROM using 8 to 1 selectors is

[IES - EC - 1995]

- (7) Match List – I with List – II and select the correct answer using the codes given below the lists.

List – I (Memories)

- A. Static PL memory
 - B. CCD Memory
 - C. ECL Memory
 - D. GAL memory

List – II (Particular characteristic)

1. Erasable programmable
 2. Ultra high speed
 3. Stores large volume of data
 4. Does not need redressing
 5. Non - Volatile

Codes :

A	B	C	D	
(A)	4	3	2	1
(B)	4	2	3	1
(C)	5	1	2	3
(D)	3	5	2	1

[IES - EC - 2000]

- (8) Which one of the following statements is correct?

(A) RAM is a non-volatile memory whereas ROM is a volatile memory

(B) RAM is a volatile memory whereas ROM is non – volatile memory

(C) Both RAM and ROM data is not lost when power is switched off

(D) Both RAM and ROM are non-volatile memories but in RAM data is lost when power is switched off.

[IES - EC - 2001/2015]

- (9) Four memory chips of 16×4 size have their address buses connected together. This system will be of size

(A) 64×4 (B) 16×16
(C) 32×8 (D) 256×1

- [IES – EC – 2002]

[IES – EC – 2005]

- (11)** Match List I (Programmable Logic Device) with List II (Function) and select the correct answer using the code given below the lists:

List I		List II	
(Programmable Logic Device)		(Function)	
A.	EPROM	1.	AND-gate programmable, OR-gate permanently hardwired
B.	PLA	2.	Both AND and OR gates programmable
C.	GAL	3.	AND-gate programmable, OUTPUT permanently hardwired but may be taken through Register, or tri state gate programmable
D.	PAL	4.	AND-gate permanently hardwired, OR-gate programmable

Codes:

	A	B	C	D
(A)	4	1	3	2
(B)	3	2	4	1
(C)	4	2	3	1
(D)	3	1	4	2

[GATE – EC – 1992]

- (12) Which one of the following statements is correct?

(A) PROM contains a programmable ‘AND’ array and a fixed ‘OR’ array

(B) PLA contains a fixed ‘AND’ array and a programmable ‘OR’ array

(C) PROM contains a fixed ‘AND’ array and a programmable ‘OR’ array

- (D) PLA contains a programmable ‘AND’ array and programmable ‘OR’ array

[IES – EC – 2006]

- (13) A single ROM is used to design a combinational circuit described by a truth table. What is the number of address lines in the ROM?

- (A) Number of input variables in the truth-table
 - (B) Number of output variables in the truth-table
 - (C) Number of input plus output variables in the truth-table
 - (D) Number of lines in the truth-table

[IES – EC – 2012]

- (14) Consider the following statements for a DRAM.

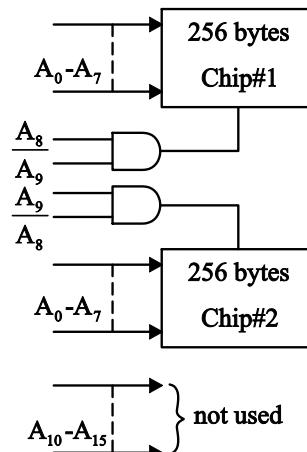
1. Bit is stored as a charge.
 2. It is made of MOS transistors
 3. Speed of DRAM is faster than processors
 4. Each memory cell requires six transistors

Which of these statements are correct?

- (A) 1 and 2 only
 - (B) 2 and 3 only
 - (C) 3 and 4 only
 - (D) 1, 2, 3 and 4

[GATE -EC - 2005]

- (15) What memory address range is NOT represented by chip#1 and chip # 2 in the figure. A_0 to A_{15} in this figure are the address lines and CS means chip select.



- (A) 0100 – 02FF
 - (B) 1500 – 16FF

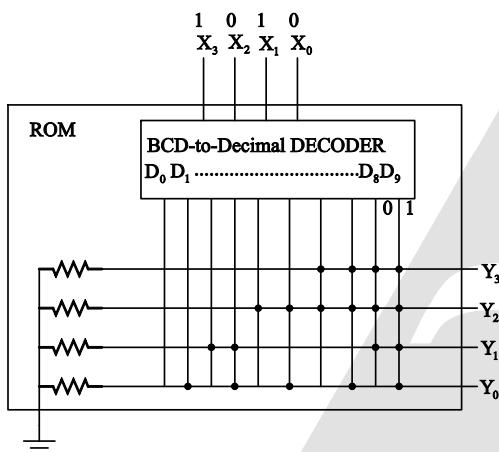
- (C) F900 – FAFF
 (D) F800 – F9FF

[GATE -EC - 1999]

- (16) If $CS = \overline{A_{15}}A_{14}A_{13}$ is used as the chip select logic of a 4k RAM in an 8085 system, then its memory range will be
 (A) 3000H – 3FFFFH
 (B) 7000H – 7FFFFH
 (C) 5000H – 5FFFFH and 6000H – 6FFFFH
 (D) 6000H – 6FFFFH and 7000H – 7FFFFH

[GATE -EC - 2002]

- (17) If the input X_3, X_2, X_1, X_0 to the ROM in the figure as 8421 BCD numbers, then the outputs Y_3, Y_2, Y_1, Y_0 are



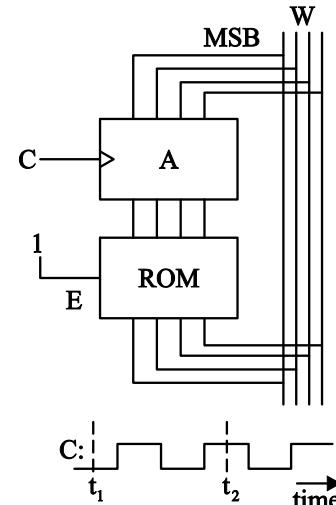
- (A) Gray code numbers
 (B) 2421 BCD numbers
 (C) excess -3 code numbers
 (D) None of the above

[GATE -EC - 2003]

- (18) In the circuit shown in the figure. A is parallel-in, parallel out 4 bit register, which loads at the rising edge of the clock 'C'. The input lines are connected to a 4 bit bus, W. Its output acts as the input to a 16×4 ROM whose output is floating when the enable input E is 0. A partial table of the contents of the ROM is as follows.

Address	0	2	4	6
Data	0011	1111	0100	1010
Address	8	10	11	14
Data	1011	1000	0010	1000

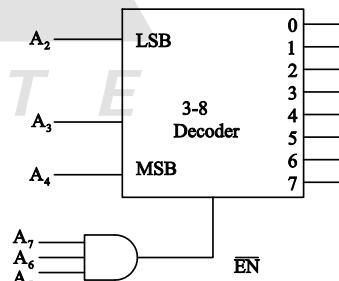
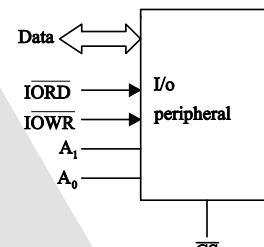
The clock to the register is shown, and the data on the W bus at time t_1 is 0110. The total data on the bus at time t_2 is :



- (A) 1111
 (B) 1011
 (C) 1000
 (D) 0010

[GATE -EC - 2006]

- (19) An I/O peripheral device shown in the figure below is to be interfaced to an 8085 microprocessor. To select the I/O device in the I/O address range $D4H - D7H$, its chip – select (\overline{CS}) should be connected to the output of the decoder shown in the figure.



- (A) output 7
 (B) output 5
 (C) output 2
 (D) output 0

[IES – EC – 2000]

- (20) Match List – I (Memory elements) with List – II (Properties) and select the correct answer using the codes given below the lists

List – I

- A. Semiconductor memory
 B. Ferrite core memory
 C. Magnetic tape memory

List – II

1. Destructive read out.

2. Combinational logic

3. Volatile.

Codes :

A	B	C
(A) 2	1	3
(B) 1	3	2
(C) 3	2	1
(D) 3	1	2

[IES – EC – 2004]

- (21) A ROM is to be used to implement a “squarer” which outputs the square of a 4-bit number. What must be the size of the ROM?
- (A) 16 address lines and 16 data lines
 - (B) 4 address lines and 8 data lines
 - (C) 8 address lines and 8 data lines
 - (D) 4 address lines and 16 data lines

[IES – EC – 2011]

- (22) The difference between PLA and ROM is
- (A) PLA is sequential, ROM is combinational
 - (B) PLA is combinational, ROM is sequential
 - (C) PLA is economizes on the number of min-terms to implement Boolean functions
 - (D) PLA has fixed AND array, ROM has fixed OR array.

[IES – EE – 1992]

- (23) PROM is
- (A) Permanent read only memory
 - (B) Polarized read only memory
 - (C) Positive read only memory
 - (D) Programmable read only memory

[IES – EE – 1992]

- (24) The advantage of magnetic drum storage is
- (A) High access time
 - (B) Large size
 - (C) Only read out is possible
 - (D) Low access time

[IES – EE – 1992]

- (25) As compared to MOS memories, bipolar memories have
- (A) Slower success time but are cheaper
 - (B) Slower access time and are costly
 - (C) Faster access time and are cheaper
 - (D) Faster access time and are costly

[IES – EE – 1992]

(26) Access in magnetic drum memory is

- (A) Completely random
- (B) Sequential and cyclic
- (C) A cyclic sequential
- (D) Partly random and partly cyclic sequential.

[IES – EE – 1992]

(27) Direct-memory-access channel facilitates data to move into and out of the system

- (A) Without subroutine
- (B) With equal time delay
- (C) Without programme intervention
- (D) on first come first serve basis.

[IES – EE – 1992]

(28) 2,764 is 65,536-bit EPROM organized as 8,192 words of 8 bits each. It has

- (A) 1C address lines and 10 data lines
- (B) 12 address lines and 10 data lines
- (C) 13 address lines and 8 data lines
- (D) 15 address lines and 12 data lines.

[IES – EE – 1992]

(29) All to the following are non-volatile memories EXCEPT

- (A) ROM's
- (B) Semiconductor RAM
- (C) PROM's
- (D) EPROM's

[IES – EE – 1992]

(30) A Semiconductor Read-only-memory basically is

- (A) a sequential circuit with flip-flop
- (B) a sequential circuit with flip-flop and gates
- (C) a set of flip-flop memory elements
- (D) a combinational logic circuit.

[IES – EE – 2012]

(31) In case of dynamic memory

- (A) Contents tend to decay over a period of time
- (B) Contents are retained without distortion
- (C) Power consumption is low.
- (D) The speed is low as compared to static memory.

- [IES – EE – 1993]

(32) Programmable ROM has a decoder at the input and

 - (A) Both these blocks being fully programmable
 - (B) Only the former block being programmable
 - (C) Only the latter block being programmable
 - (D) Both these blocks being partially programmable

[IES – EE – 1995]

(33) In computer terminology 1 M Byte memory means

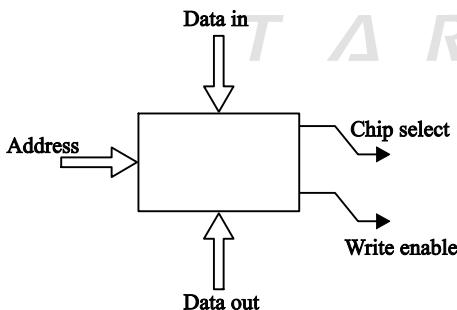
 - (A) 1000000 bytes
 - (B) 1000024 bytes
 - (C) 1024000 bytes
 - (D) 1048576 bytes

[IES – EE – 1996]

[IES – EE – 1996]

- (35) A random-access R/W semiconductor memory chip is organized into 128 words of 8 bits each. A block diagram of the chip is shown in the following figure:

Ignoring power supply connections, the minimum number of pin connections per chip is



[IES - EE - 1997]

- (36) The larger the RAM of a computer, the faster is its speed, since it eliminates

 - (A) Need for ROM
 - (B) Need for external memory
 - (C) Frequency disk I/O s
 - (D) Need for a data – wide path

[IES – EC – 2009/IES - EE- 1997]

- (37) A 3×8 decoder with two enable inputs is to be used to address 8 blocks of memory. What will be the size of each memory block when addressed from a sixteen bit bus with two MSB's used to enable the decoder?

(A) 2K (B) 4K

[IES – EE – 1998]

- (38) Which one of the following is an example of non-volatile memory?

(A) Static RAM **(B) Dynamic RAM**

MEG-EEG-2012

[IES - EE - 2012]

- (39) For a memory system, the cycle time is

 - (A) Same as the access time
 - (B) Larger than the access time
 - (C) Shorter than the access time
 - (D) Sub - multiple of the access time

[IES – EE – 2012]

[GATE-EC-2001]

- (41) In the DRAM cell in the figure, the V_t of the NMOSFET is 1V. For the following three combinations of WL and BL voltages

(A) 5V; 3V; 7V (B) 4V; 3V; 4V
(C) 5V; 5V; 5V (D) 4V; 4V; 4V

[GATE-EC-1996]

- (42) Each cell of a static Random Access Memory contains

 - (A) 6 MOS transistors
 - (B) 4 MOS transistors and 2 capacitors
 - (C) 2 MOS transistors and 4 capacitors
 - (D) 1 MOS transistor and 1 capacitor

[GATE-S2-EC-2017]

- (43) In a DRAM,

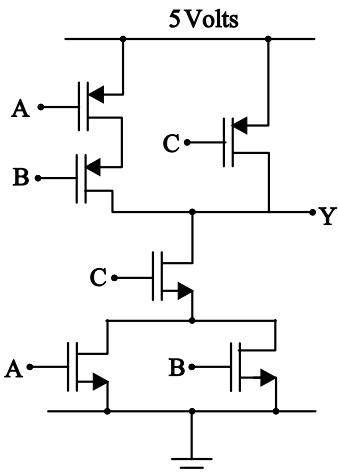
 - (A) periodic refreshing is not required
 - (B) information is stored in a capacitor
 - (C) information is stored in a latch
 - (D) both read and write operations can be performed simultaneously

.....0000.....

07

Logic Gate Families

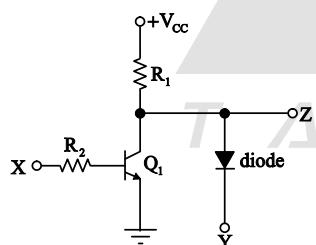
- (1) In the circuit shown



- (A) $Y = \overline{A} \overline{B} + \overline{C}$ (B) $Y = (A + B)C$
 (C) $Y = (\overline{A} + \overline{B})\overline{C}$ (D) $Y = AB + C$

[GATE-EC/EE/IN-2013]

- (2) In the circuit shown below, Q_1 has negligible collector-to-emitter saturation voltage and the diode drops negligible voltage across it under forward bias. If V_{cc} is +5 V, X and Y are digital signals with 0 V as logic 0 and V_{cc} as logic 1, than the Boolean expression for Z is

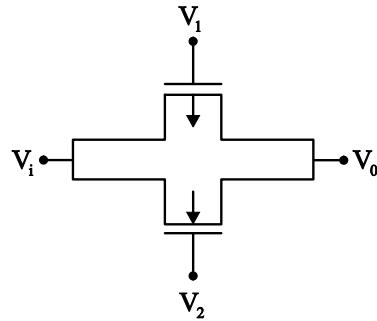


- (A) $X Y$ (B) $\overline{X} Y$
 (C) $X \overline{Y}$ (D) $\overline{X}\overline{Y}$

[GATE-IN-2003]

- (3) For the CMOS analog switch shown in figure, the positive supply is $+V_{DD}$ and the negative supply is $-V_{EE}$. The input V_i is bipolar. The switch will be ON and V_o will be equal to V_i provided

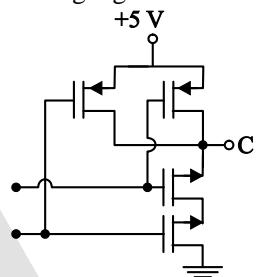
[GATE-EC/EE/IN-2012]



- (A) $V_1 = V_2 = +V_{DD}$
 (B) $V_1 = V_2 = -V_{EE}$
 (C) $V_1 = +V_{DD}$ and $V_2 = -V_{EE}$
 (D) $V_1 = -V_{EE}$ and $V_2 = +V_{DD}$

[GATE-IN-2005]

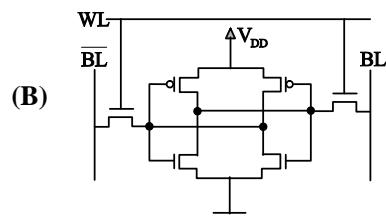
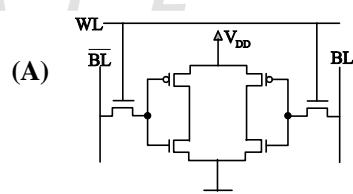
- (4) Identify the logic given in the figure

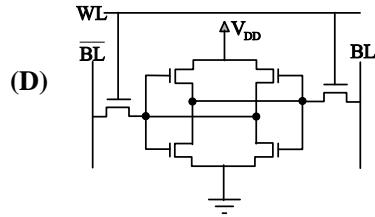
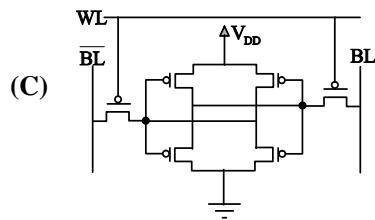


- (A) NOR (B) NAND
 (C) AND (D) OR

[GATE – EC – 2014]

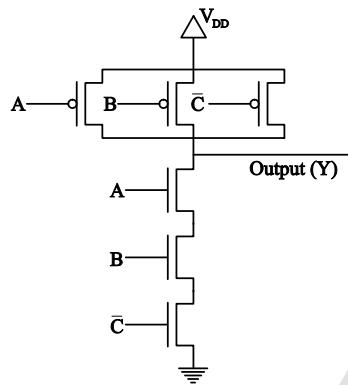
- (5) If WL is the word Line and BL the Bit Line, and SRAM cell is shown in





[GATE - EC - 2014]

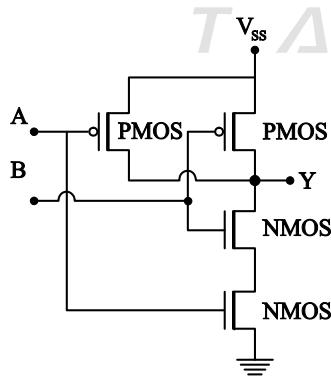
- (6) The output (Y) of the circuit shown in the figure is



- (A) $\overline{A} + \overline{B} + C$ (B) $A + \overline{B} \cdot \overline{C} + A \cdot \overline{C}$
 (C) $A + B + \overline{C}$ (D) $A \cdot B \cdot \overline{C}$

[GATE-IN-2014]

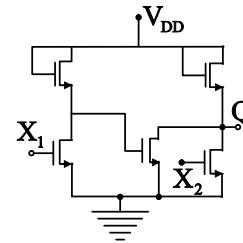
- (7) The figure is a logic circuit with inputs A and B and output Y. $V_{ss} = +5$ V. The circuit is of type



- (A) NOR (B) AND
 (C) OR (D) NAND

[GATE-EE - 2009/IES - EE - 2009]

- (8) If X_1 and X_2 are the inputs to the circuit as shown in the figure, then what is the output Q?

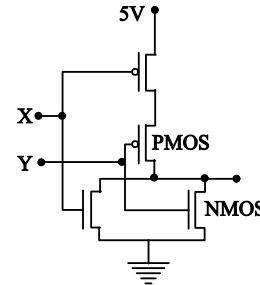


(A) $\overline{X_1 + X_2}$ (B) $\overline{X_1 \cdot X_2}$

(C) $(X_1 \cdot X_2)$ (D) $(X_1 \cdot \overline{X}_2)$

[GATE - IN - 2007]

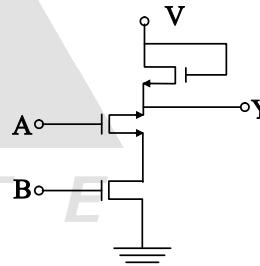
- (9) A CMOS implementation of a logic gates is shown in the following figure: The Boolean logic function realized by the circuit is :



- (A) AND (B) NAND
 (C) NOR (D) OR

[IES - EE - 2003]

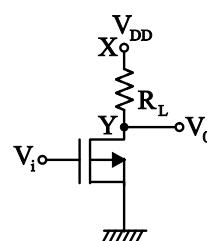
- (10) The shown NMOS circuit is a gate of the type



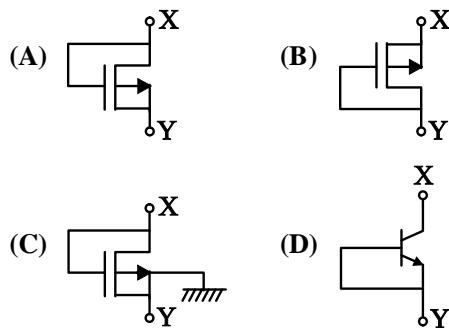
- (A) NAND (B) NOR
 (C) AND (D) EXCLUSIVE-OR

[IES - EC - 1999]

- (11) The load resistance R_L between X and Y in the switch shown in Figure – I

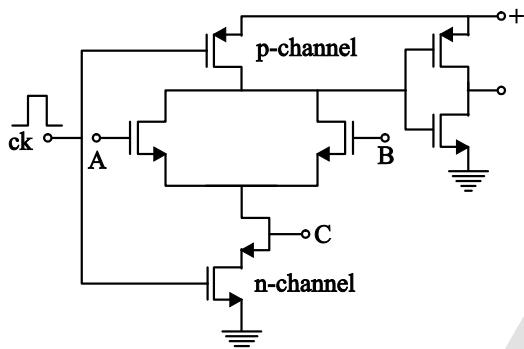


CANNOT be replaced



[GATE-EC-1991]

- (12) In figure, the Boolean expression for the output in terms of inputs A, B and C when the clock 'ck' is high, is given by

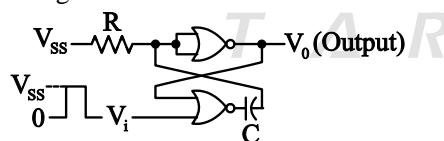


[GATE-EC-1994]

- (13) In the output stage of a standard TTL, we have a diode between the emitter of the pull-up transistor and the collector of the pull-down transistor. The purpose of this diode is to isolate the output node from the power supply V_{CC} .

AC [GATE-EC-2002]

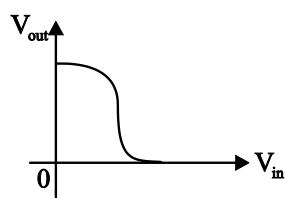
- (14) The circuit in the figure has two CMOS NOR-gates. This circuit function as a :



- (A) flip-flop
 - (B) Schmitt trigger
 - (C) monostable multi-vibrator
 - (D) astable multi-vibrator

[GATE-EC-2004]

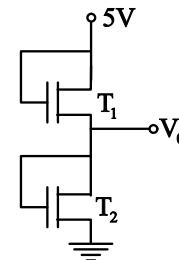
- (15) Given figure is the voltage transfer characteristic of



- (A) an NMOS inverter with enhancement mode transistor as load
 - (B) an NMOS inverter with depletion mode transistor as load
 - (C) a CMOS inverter
 - (D) a BJT inverter

[GATE-EC-2005]

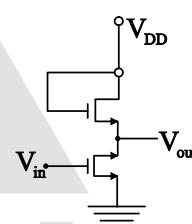
- (16) Both transistors T_1 and T_2 shown in figure, have a threshold voltage of 1 Volts. The device parameters K_1 and K_2 of T_1 and T_2 , are, respectively, $36 \mu\text{A}/\text{V}^2$ and $9 \mu\text{A}/\text{V}^2$. The output voltage V_o is



[IES – EC – 2005]

- (17) In the circuit given below, both transistors have the approximate value of the highest possible output voltage V_{out} , if V_{in} can range from 0 to V_{DD} ?

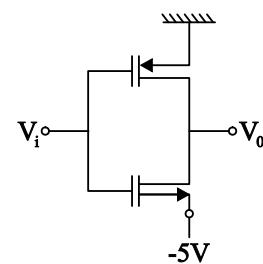
(Assume $0 \leq V_T \leq V_{DD}$)



- (A) $V_{DD} - V_T$ (B) V_{DD}
 (C) V_L (D) 0

[GATE – EC – 1998]

- (18) The threshold voltage for each transistor in the figure shown below is 2.0 V. What are the values of V_i for this circuit to work as an inverter?



- (A) -5V and 0 V
 - (B) -5 V and 5 V

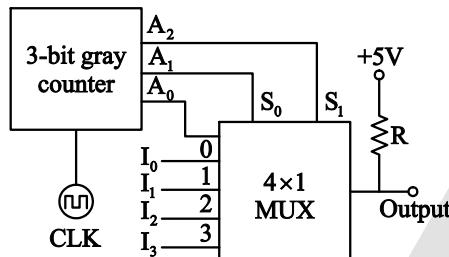
- (C) 0 V and 5 V
 (D) -3 V and 3 V

(19) Match the following :

Logic	Function
A. $\bar{X} + \bar{Y}$	P. Sum
B. XY	Q. NAND
C. $\bar{X}\bar{Y}$	R. Carry
	S. NOR

[GATE-EE-2014]

- (20) A 3-bit gray counter is used to control the output of the multiplexer as shown in the figure. The initial state of the counter is 000_2 . The output is pulled high. The output of the circuit follows the sequence



- (A) $I_0, 1, 1, I_1, I_3, 1, 1, I_2$
 (B) $I_0, 1, I_1, 1, I_2, 1, I_3, 1$
 (C) $1, I_0, 1, I_1, I_2, 1, I_3, 1$
 (D) $I_0, I_1, I_2, I_3, I_0, I_1, I_2, I_3$

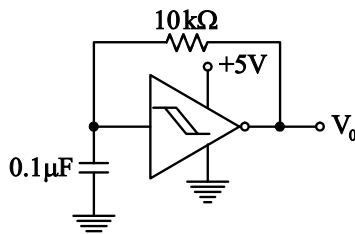
[GATE-EE-2003]

- (21) A memory system has a total of 8 memory chips, each with 12 address lines and 4 data lines. The total size of the memory system is

- (A) 16 kbytes (B) 32 kbytes
 (C) 48 kbytes (D) 64 kbytes

[GATE-EE-2014]

- (22) A hysteresis type TTL inverter is used to realize an oscillator in the circuit shown in the figure



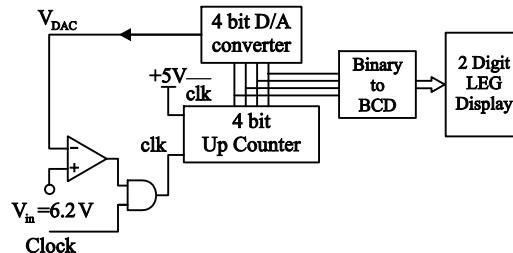
If the lower and upper trigger level voltages are 0.9 V and 1.7 V, the period (in ms), for which output is LOW, is _____

Statement for Linked Answer Questions for Next Two Questions :

In the following circuit, the comparator output is logic "1" if $V_1 > V_2$ and is logic "0" otherwise. The D/A conversion is done as per the relation

$$V_{DAC} = \sum_{n=0}^3 2^{n-1} b_n \text{ Volts, where } b_3(\text{MSB}), b_2, b_1$$

and b_0 (LSB) are the counter outputs. The counter starts from the clear state.



[GATE-EC-2008]

- (23) The stable reading of the LED displays is :

- (A) 06 (B) 07
 (C) 12 (D) 13

[GATE-EC-2008]

- (24) The magnitude of the error between V_{DAC} and V_{in} at steady state in volts is

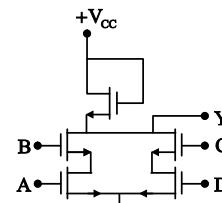
- (A) 0.2 (B) 0.3
 (C) 0.5 (D) 1.0

[GATE-EC-2015]

- (25) Consider a four bit D to A converter. The analog value corresponding to a digital signals of values 0000 and 0001 are 0V and 0.0625V respectively. The analog value(in Volts) corresponding to the digital signal 1111 is _____.

[GATE - IN - 2004]

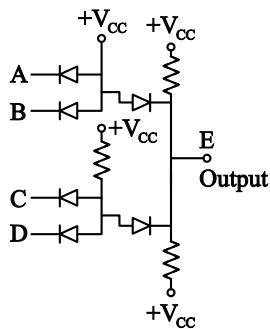
- (26) In Fig. if the input C = 0 and D = 0, the output Y can be made 0 by making



- (A) A = 0, B = 1
 (B) A = 0, B = 0
 (C) A = 1, B = 1
 (D) A = 1, B = 0

[IES – EC – 1996]

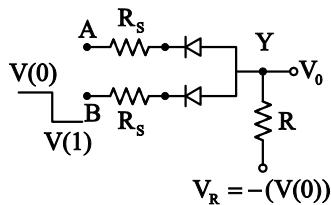
- (27) What is the output of the gate circuit shown in the above figure?



- (A) $(A + B)(C + D)$
 (B) $AB + CD$
 (C) $\overline{AB + CD}$
 (D) $\overline{(A + B)(C + D)}$

[IES - EC - 1995]

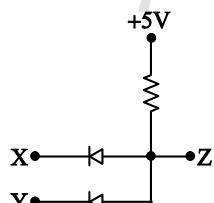
- (28) The circuit shown in the given figure is a



- (A) Positive logic OR circuit
 (B) Negative logic OR circuit
 (C) Positive logic NAND circuit
 (D) Negative logic NAND circuit

[GATE - IN - 2009]

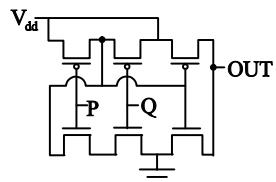
- (29) The diode in circuit shown are ideal. A voltage of 0 V represents logic 0 and +5 V represents logic 1. The logic function Z realized by the circuit for logic inputs X and Y is



- (A) $Z = X = Y$
 (B) $Z = XY$
 (C) $Z = \overline{X + Y}$
 (D) $Z = Z = \overline{XY}$

[GATE - EC - 2008]

- (30) The logic function implemented by the following circuit at the terminal out is



- (A) P NOR Q (B) P NAND Q
 (C) P OR Q (D) P AND Q

[IES - EE - 1992]

- (31) Positive logic in a logic circuit is one in which
 (A) Logic 0 and 1 are represented by 0 and positive voltage respectively
 (B) Logic 0 and 1 are represented by Then by negative and positive voltage respectively
 (C) Logic 0 voltage level is higher than logic 1 voltage level
 (D) Logic 0 voltage level is lower than logic 1 voltage level.

[IES - EE - 1996]

- (32) Match List I with List II and select the correct answer using the codes given below the lists:

List I **List II**

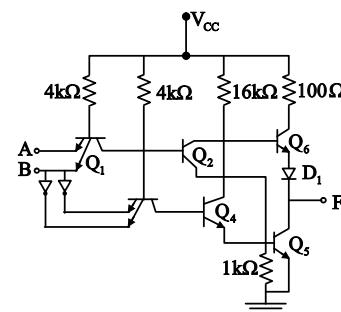
(Name of Logic gate)	(Propagation delay)
A. DTL	1. 8 ns
B. TTL	2. 10 ns
C. ECL	3. 25 ns
D. CMOS	4. 1 ns

Codes:

	A	B	C	D
(A)	3	2	1	4
(B)	4	3	2	1
(C)	3	2	4	1
(D)	2	1	4	3

[IES - EE - 1998]

- (33) The output 'F' of the circuit shown in the given figure is :



- (A) $A\bar{B}$ (B) $\bar{A}B$
 (C) $AB + \bar{A}\bar{B}$ (D) $\bar{A}\bar{B} + A\bar{B}$

[IES - EE - 2001]

- (34) Match List I with List II and select the correct answer:

List I (Type of gates)

- A. ECL
- B. TTL
- C. CMOS
- D. NMOS

List II (Values of propagation delay)

- 1. 5 ns
- 2. 20 ns
- 3. 200 ns
- 4. 1 ns

Codes:

A	B	C	D
(A) 1 4 3 2			
(B) 4 1 3 2			
(C) 1 4 2 3			
(D) 4 1 2 3			

[IES – EC – 1996]

- (35) Match List-I with List-II and select the correct answer using the code given below the lists:

List I		List II	
(Semiconductor technology)		(Characteristic)	
A.	TTL	1.	Maximum power consumption
B.	ECL	2.	Highest packing density
C.	NMOS	3.	Least power consumption
D.	CMOS	4.	Saturated logic

Codes:

A	B	C	D
(A) 1 4 2 3			
(B) 1 4 3 2			
(C) 4 1 2 3			
(D) 4 1 3 2			

[IES – EE – 2012]

- (36) **Statement (I) :** ECL gate has the highest speed of operation.

Statement (II) : The transistors in ECL gate operate in active region.

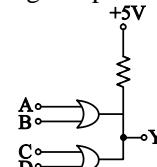
[IES – EC – 1994]

- (37) The figure of merit of logic family is given by

- (A) Gain bandwidth product
- (B) (Propagation delay time) * (Power dissipation)
- (C) (Fan – out) * (power dissipation)
- (D) (Noise Margin) * (Power dissipation)

[IES – EC – 1994]

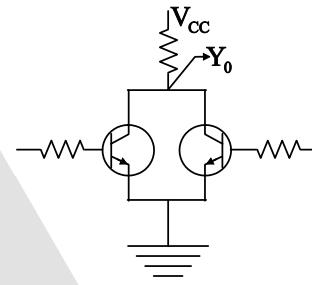
- (38) The open collector of the gates are connected together as shown in the given figure. The logic expression for Y will be



- (A) $\overline{A+B+C+D}$
- (B) $A+B+C+D$
- (C) $(A+B)(C+D)$
- (D) $AB+CD$

[IES – EC – 1995]

- (39) The logic function performed by the circuit given in the figure is



X_1, X_2 : inputs Y_0 : output

- (A) $Y_0 = X_1 X_2$
- (B) $Y_0 = X_1 + X_2$
- (C) $Y_0 = \overline{X}_1 \overline{X}_2$
- (D) $Y_0 = \overline{X}_1 + \overline{X}_2$

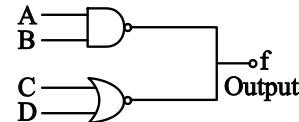
[IES – EC – 1995]

- (40) If the various logic families are arranged in the ascending order of their fan – out capabilities, the sequence will be

- (A) TTL, ECL, IIL, CMOS
- (B) ECL, TTL, IIL, CMOS
- (C) IIL, TTL, ECL, CMOS
- (D) TTL, ECL, CMOS, IIL

[IES – EC – 1996]

- (41) Which one of the following logic functions is implemented by the gates when their open collector type outputs are tied together as shown in the given figure?



- (A) $f = AB + C + D$
 (B) $f = \overline{AB} + (C + D)$
 (C) $f = AB + (C + D)$
 (D) $f = \overline{AB + C + D}$

[IES – EC – 1999]

- (42) The voltage levels of a negative logic system
 (A) Must necessarily be negative
 (B) May be negative or positive
 (C) Must necessarily be positive
 (D) Must necessarily be 0V and – 5V

[IES – EC – 1999]

- (43) Consider the following statements regarding ICs:-
 1. ECL has the least propagation delay.
 2. TTL has the largest fan – out
 3. CMOS has the biggest noise margin
 4. TTL has the lowest power consumption
 Which of these statements are correct?
 (A) 1 and 3 (B) 2 and 4
 (C) 3 and 4 (D) 1 and 2

[IES – EC – 2001]

- (44) Assertion (A) : ECL gate has the highest speed of operation as compared to other logic families.

Reason (R) : ECL gate dissipates more power.

[IES – EC – 2001]

- (45) Consider the following logic families.

1. MOS
 2. DTL
 3. RTL
 4. ECL

The sequence of these logic families in the order of their increasing noise margin is

- (A) 3, 4, 1, 2 (B) 3, 4, 2, 1
 (C) 4, 3, 1, 2 (D) 4, 3, 2, 1

[IES – EC – 2002]

- (46) Match List I with List II and select the correct answer using the code given below the lists:

List I		List II	
(Logic Gates)		(Operation)	
A.	TTL	1.	More logical swing
B.	ECL	2.	Low power dissipation

C.	HTL	3.	Current hogging
D.	CMOS	4.	NOR/OR output
		5.	Totem-pole output

Codes:

- | | A | B | C | D |
|-----|---|---|---|---|
| (A) | 3 | 5 | 4 | 2 |
| (B) | 1 | 2 | 5 | 4 |
| (C) | 3 | 2 | 5 | 4 |
| (D) | 1 | 5 | 4 | 2 |

[IES – EC – 2003]

- (47) Assertion (A) :

The switching speed of ECL gate is very high.

Reason(R) :

The devices in ECL gate operate in active region.

[IES – EC – 2003]

- (48) Assertion(A):

When transistor switches are to be used in an application where speed is a premium, it is better to reduce the storage time.

Reason(R):

It is comparatively easy to reduce storage time rather than the rise time and fall time of a transistor switch.

AC [IES – EC – 2004/2006/2007/2010]

- (49) Match List I with List II and select the correct answer using the code given below the lists:

List I		List II	
A.	HTL	1.	High fan-out
B.	CMOS	2.	Highest speed of operation
C.	I ² L	3.	High noise immunity
D.	ECL	4.	Lowest product of power and delay

Codes:

- | | A | B | C | D |
|-----|---|---|---|---|
| (A) | 3 | 4 | 1 | 2 |
| (B) | 2 | 1 | 4 | 3 |
| (C) | 3 | 1 | 4 | 2 |
| (D) | 2 | 4 | 1 | 3 |

[IES – EC – 2007&2008]

- (50) Why does an I²L (Integrated Injection Logic) have higher density of integration than TTL?

- (A) It does not require transistors with high current gain and hence they have smaller geometry
- (B) It uses multi-collector transistors
- (C) It does not require isolation diffusion
- (D) It uses dynamic logic instead of static logic

[IES – EC – 2009]

- (51) Which of the following factors are responsible to design IC logic gates to operate at a fixed supply voltage of 5 volts ?
1. Low heating of IC logic gates.
 2. Compatibility with other logic gates.
 3. Satisfactory and safe operation.
 4. Standardization from IC manufacturing point of view.

Select the correct answer from the code given below :

- | | |
|-------------|-------------|
| (A) 1 only | (B) 2 only |
| (C) 2 and 3 | (D) 3 and 4 |

[IES – EC – 2009]

- (52) Which of the following statements is **not** correct ?
- (A) Propagation delay is the time required for a gate to change its state
 - (B) Noise immunity is the amount of noise which can be applied to the input of a gate without causing the gate to change state
 - (C) Fan-in of a gate is always equal to fan-out of the same gate
 - (D) Operating speed is the maximum frequency at which digital data can be applied to a gate

T [IES – EC – 2010]

(53) Assertion(A) :

The TTL NAND gate in tristate output configuration can be used for a bus arrangement with more than one gate output connected to a common line.

Reason(R):

The tri state configuration has a control input, which can be bus line.

[IES – EC – 2011]

- (54) Match List-I with List-II and select the correct answer using the code given below the lists:

List I		List II	
A.	TTL	1.	Low power consumption
B.	ECL	2.	High speed
C.	CMOS	3.	Low propagation delay

Codes:

- | A | B | C |
|-----|---|---|
| (A) | 1 | 3 |
| (B) | 2 | 3 |
| (C) | 1 | 2 |
| (D) | 2 | 1 |

[IES – EC – 2011]

- (55) Match List-I with List-II and select the correct answer using the code given below the lists:

List I		List II	
A.	DCTL	1.	Multiple collectors
B.	ECL	2.	Current hogging
C.	I ² L	3.	High speed

Codes:

- | A | B | C |
|-----|---|---|
| (A) | 2 | 3 |
| (B) | 1 | 3 |
| (C) | 2 | 1 |
| (D) | 3 | 2 |

[GATE – EC – 1997]

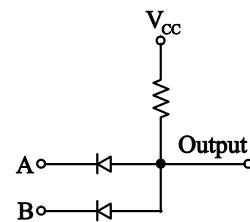
- (56) In standard TTL, the ‘Totem pole’ refers to:
- (A) Multi-emitter input stage
 - (B) The phase splitter
 - (C) The output buffer
 - (D) Open collector output stage

[IES – EC – 2012]

- (57) For a transistor used as a switch, t_d is delay time, t_r is rise time, t_s is storage time and t_f is fall time. Then turn-on time t_{ON} and turn-off time t_{OFF} are respectively
- (A) $(t_d + t_s)$ and $(t_r + t_f)$
 - (B) $(t_d + t_s)$ and $(t_s + t_r)$
 - (C) $(t_r + t_s)$ and $(t_d + t_f)$
 - (D) $(t_d + t_r)$ and $(t_s + t_f)$

[GATE - IN - 1994]

- (58) The diode circuit shown in Fig. functions as



- (A) AND gate
- (B) OR gate
- (C) NAND gate
- (D) NOR gate

[GATE - IN - 2003]

- (59) Introducing a Schottky diode between the base and collector of the output transistor in a TTL circuit
- Increases the speed of operation by inhibiting saturation
 - Decreases the speed of operation by inhibiting saturation
 - Increases the FAN OUT by enabling saturation
 - Increases the speed of operation by enabling saturation

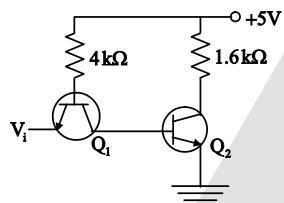
[GATE - EE - 1998]

- (60) The open collector outputs of two inputs NAND gates are connected to a common pull up resistor. If the input to the gates are P, Q and R, S respectively, the output is equal to

- $\overline{PQ} \cdot \overline{RS}$
- $\overline{PQ} + \overline{RS}$
- $PQ + RS$
- $PQRS$

[GATE - EE - 2006]

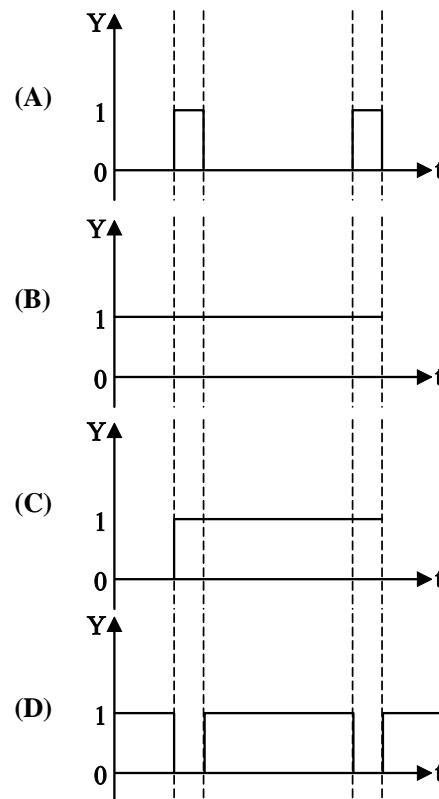
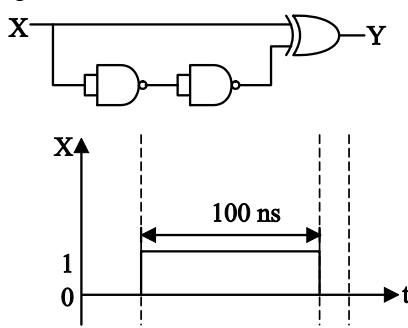
- (61) A TTL NOT gate circuit is shown in figure. Assuming $V_{BE} = 0.7$ v of both the transistors, if $V_i = 3.0$ V, then the states of the two transistors will be



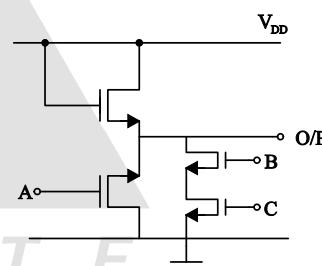
- Q_1 ON and Q_2 OFF
- Q_1 reverse ON and Q_2 OFF
- Q_1 reverse ON and Q_2 ON
- Q_1 OFF and Q_2 reverse ON

[GATE - EE - 2010]

- (62) The TTL circuit shown in the figure is fed with the waveform X (also shown.) All gates have equal propagation delay of 10 ns. The output Y of the circuit is

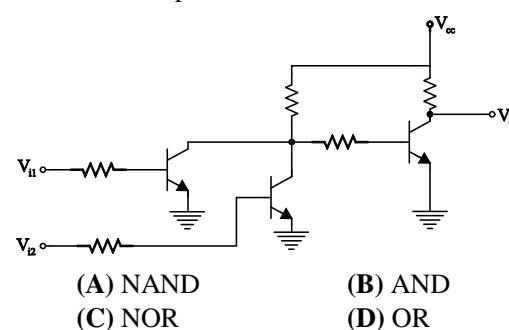


- (63) The CMOS equivalent of the following n MOS gate (figure) is _____
(draw the circuit).



[GATE - EC - 1992]

- (64) Figure shows the circuit of a gate in the Resistor Transistor Logic (RTL) family. The circuit represents a



- NAND
- AND
- NOR
- OR

[GATE - EC - 1997]

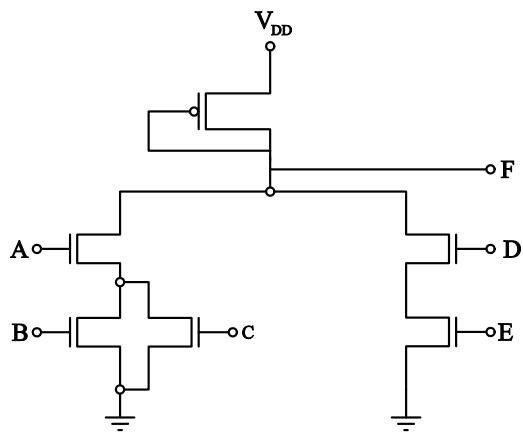
- (65) The inverter 74 AL S01 has the following specifications:

$$I_{OH\max} = -0.4mA, \\ I_{OL\max} = 8mA, I_{1H\max} = 20\mu A, I_{IL\max} = -0.1mA$$

The fan out based on the above will be

[GATE -EC - 1997]

- (66) For the NMOS logic gate shown in figure, the logic function implemented is :



- (A) \overline{ABCDE}
 (B) $(AB + \overline{C}).(\overline{D} + E)$
 (C) $\overline{A.(B + C) + D.E}$
 (D) $(\overline{A + B}).C + \overline{D.E}$

[GATE -EC - 1997]

- (67) The gate delay of an NMOS inverter is dominated by charge time rather than discharge time because

- (A) the driver transistor has a larger threshold voltage than the load transistor.
 - (B) the driver transistor has larger leakage currents compared to the load transistor.
 - (C) the load transistor has a smaller W/L ratio compared to the driver transistor.
 - (D) none of the above

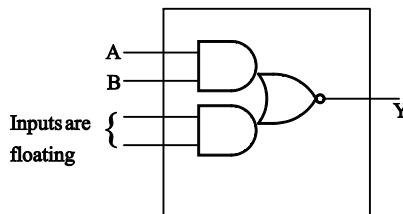
[GATE -EC - 1999]

- (68) Commercially available ECL gates use two ground lines and one negative supply in order to

 - (A) Reduce power dissipation
 - (B) increase fan-out
 - (C) Reduce loading effect
 - (D) eliminate the effect of power line glitches or the biasing circuit.

[GATE -EC - 2004]

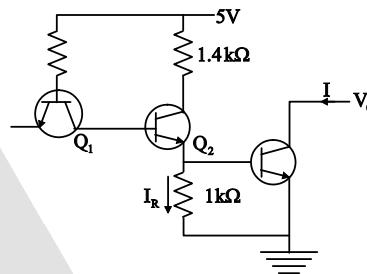
- (69) The figure shows the internal schematic of a TTL AND-OR-INVERT (AOI) gate. For the inputs shown in the figure, the output Y is :



[GATE -EC - 2005]

- (70) The transistors used in a portion of the TTL gate shown in the figure have a $\beta = 100$.

The base-emitter voltage of is 0.7 for a transistor in active region and 0.75 V for a transistor in saturation. If the sink current $I = 1\text{mA}$ and the output is at logic 0, then the current I_R will be equal to



- (A) 0.65 mA (B) 0.70 mA
 (C) 0.75 mA (D) 1.00 mA

[CATE EC 2009]

- (71) The full forms of the abbreviations TTL and CMOS in reference to logic families are

- (A) Triple Transistor Logic and chip Metal oxide semiconductor.
 - (B) Tristate Transistor Logic and chip metal oxide semiconductor
 - (C) Transistor Logic and complementary Metal oxide semiconductor
 - (D) Tristate Transistor Logic and complementary Metal oxide silicon.

[GATE -EC - 2003]

- (72) The DTL, TTL, ECL and CMOS facility GATE of digital ICS are compared in the following 4 columns

	(P)	(Q)	(R)	(S)
Fan is minimum	DTL	DTL	TTL	CMOS

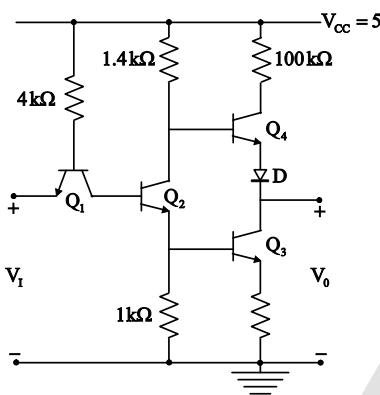
Power consumption is Minimum	TTL	CMOS	ECL	DTL
Propagation delay is minimum	CMOS	ECL	TTL	TTL

The correct column is :

- | | |
|-------|-------|
| (A) P | (B) Q |
| (C) R | (D) S |

[GATE -EC - 2007]

- (73) The circuit diagram of a standard TTL NOT gate is shown in the figure. When $V_I = 2.5V$, the modes of operation of the transistors will be :



- | | | | |
|----------------------|----------------|------------------|---------------|
| (A) Q ₁ : | Reverse active | Q ₂ : | Normal active |
| Q ₃ : | Saturation | Q ₄ : | Cut-off |
| (B) Q ₁ : | Reverse active | Q ₂ : | Saturation |
| Q ₃ : | Saturation | Q ₄ : | Cut-off |
| (C) Q ₁ : | Normal active | Q ₂ : | Cut-off |
| Q ₃ : | Cut-off | Q ₄ : | Saturation |
| (D) Q ₁ : | Saturation | Q ₂ : | Saturation |
| Q ₃ : | Saturation | Q ₄ : | Normal active |

[GATE -EC - 2003]

- (74) The output of the 74 series of TTL gates is taken from a BJT in
- (A) Totem pole and common collector configuration
 - (B) either totem pole or open collector configuration
 - (C) common base configuration
 - (D) common collector configuration

[GATE - EC - 1987]

- (75) Given that for a logic family,

V_{OH} is the minimum output high-level voltage

V_{OL} is the maximum output high-level voltage

V_{IH} is the minimum acceptable input high-level voltage and

V_{IL} is the maximum acceptable input low-level voltage,

The correct relationship is:

- (A) $V_{IH} > V_{OH} > V_{IL} > V_{OL}$
- (B) $V_{OH} > V_{IH} > V_{IL} > V_{OL}$
- (C) $V_{IH} > V_{OH} > V_{OL} > V_{IL}$
- (D) $V_{OH} > V_{IH} > V_{OL} > V_{IL}$

[GATE – EC – 1998]

- (76) The noise margin of a TTL gate is about

- (A) 0.2 V
- (B) 0.4 V
- (C) 0.6 V
- (D) 0.8 V

[GATE – EC – 1994]

- (77) In standard TTL the ‘totem pole’ stage refers to

- (A) the multi-emitter input stage
- (B) the phase splitter
- (C) the output buffer
- (D) open collector output stage.

[GATE – EC – 1989]

- (78) A logic family has threshold voltage $V_T = 2V$, minimum guaranteed output high voltage $V_{OH} = 4V$, minimum accepted input high voltage $V_{IH} = 3V$, maximum guaranteed output low voltage $V_{OL} = 1V$, and maximum accepted input low voltage $V_{IL} = 1.5V$. Its noise margin is

- (A) 2V
- (B) 1 V
- (C) 1.5 V
- (D) 0.5 V

[GATE – EE – 1998]

- (79) In standard TTL gates, the totem pole output stage is primarily used to

- (A) Increase the noise margin of the gate
- (B) Decrease the output switching delay
- (C) Facilitate a wired OR logic connection
- (D) Increase the output impedance of the circuit

[IES – EC – 2009]

- (80) Which of the following output configurations are available in a TTL gate?

1. Open collector output
2. Totem-pole output

3. Tristate output

Select the correct answer from the codes given below:

- (A) 1 only
- (B) 1 and 2 only
- (C) 2 and 3 only
- (D) 1, 2 and 3

[IES - EC - 2011]

- (81) CMOS logic families are associated with :
1. Low power dissipation
 2. High noise immunity
 3. Low Fan-out
 4. Comparatively high logic voltage swing
- (A) 1, 2 and 4 only
 - (B) 1, 2 and 3 only
 - (C) 2, 3 and 4 only
 - (D) 1, 2, 3 and 4

- (82) The figure of merit of a logic family is given by
- (A) Gain \times bandwidth
 - (B) Propagation delay time \times power dissipation
 - (C) Fan-out \times propagation delay time
 - (D) Noise margin \times power dissipation

[IES - EC - 2005]

(83) **Assertion (A) :**

The speed-power product is an important parameter for comparing various TTL series.

Reason(R) :

A low value of speed-power product indicates that a propagation delay can be achieved without excessive power dissipation and vice-versa.

[IES - EC - 2000/2008]

- (84) The figure of merit of a logic family is given by the product of
- (A) Gain and bandwidth
 - (B) Propagation delay time and power dissipation
 - (C) Fan-out and propagation delay time
 - (D) Noise margin and power dissipation

[IES - EC - 1997]

- (85) In digital circuit, Scotty transistor preferred over normal transistor because their
- (A) Lower propagation delay
 - (B) Higher propagation delay
 - (C) Lower power dissipation
 - (D) Higher power dissipation

[IES - EC - 1998]

- (86) TTL circuits with active pull - up are preferred because of their suitability for
- (A) Wired – And Operation
 - (B) Bus operated system
 - (C) Wired logic operation
 - (D) Reasonable dissipation and speed of operation

[IES - EC - 1992]

- (87) The “ECL” has very high switching speed because the transistors are
- (A) Switching between cut – off and saturation regions
 - (B) Switching between cut – off and active regions
 - (C) Switching between active and saturation regions
 - (D) Any of the above

[IES - EE - 2012]

- (88) Pull-up resistor is needed for an open collector gate
- (A) To provide V_{CC} for the I_C
 - (B) To provide ground for the I_C
 - (C) To provide the HIGH voltage
 - (D) To provide the LOW voltage

[IES - EE - 2003]

- (89) Consider the following statements in respect of ECL gate :
1. Its switching speed is high
 2. It provides OR or NOR logic operations
 3. Its power dissipation is small as compared to other logic gates
 4. Its logic levels are compatible with other logic levels are compatible with other logic family gates

Which of these statements are correct?

- (A) 1 and 2
- (B) 1, 2 and 3
- (C) 1, 2 and 4
- (D) 3 and 4

[IES - EE - 1997]

- (90) **Assertion (A) :** TTL and CMOS cannot be normally used together.

Reason (R) : TTL operates on a (5.25) V regulated supply voltage and some mA, while the CMOS operates on unregulated supply voltage of +3V to +15V and some μ A.

Codes :

- (A) Both A and R are true and R is the correct explanation of A.
- (B) Both A and R are true but R is not the correct explanation of A

- | | |
|--|--|
| <p>(C) A is true but R is false
 (D) A is false but R is true</p> <p align="center">[IES - EE - 1993]</p> <p>(91) Assertion (A) : The emitter logic reduces the transistor rise time and hence results in logic gates which switch very fast.</p> <p>Reason (R) : In emitter - coupled logic, the transistors are maintained in unsaturated condition.</p> <p>Codes:</p> <p>(A) Both A and R are true and R is the correct explanation of A.
 (B) Both A and R are true but R is not the correct explanation of A
 (C) A is true but R is false
 (D) A is false but R is true</p> <p align="center">[IES - EE - 1992]</p> <p>(92) While ___ is the fastest unsaturated logic gate ___ has the excellent noise immunity ?
 (A) ECL; TTL (B) TTL; ECL
 (C) ECI; HTL (D) RTL; DTL</p> <p align="center">[GATE - EC - 1999]</p> <p>(93) A Darlington Emitter follower circuit is sometimes used in the output stage of a TTL gate in order to
 (A) increase its I_{OL}
 (B) Reduce its I_{OH}
 (C) Increase its speed of operation.
 (D) Reduce power Dissipation.</p> <p align="center">[GATE - EC - 1989]</p> <p>(94) Among the digital IC-families – ECL, TTL and CMOS:-
 (A) ECL has the least propagation delay
 (B) TTL has the largest fan-out
 (C) TL has the lowest power consumption
 (D) CMOS has the biggest noise margin</p> <p align="center">[GATE - EC - 1987]</p> <p>(95) Fill in the blanks of the statements below concerning the following Logic Families:
 Standard TTL (74 XXLL), Low power TTL (74 LXX) Low power schottky TTL (74LSXX), schottky TTL(74 SXX), Emitter coupled Logic (ECL), CMOS</p> <p>(A) Among the TTL Families, _____ family requires considerably less power than the standard TTL(74XX) and also has comparable propagation delay.</p> <p>(B) Only the _____ family can operate over a wide range of power supply voltages</p> | <p align="right">[GATE – IN – 1999]</p> <p>(96) Indicate which one of the following statements is correct:
 (A) Static RAM are faster than dynamic RAMs
 (B) RAMs cannot be used to realize Read Write Memory (RWM)
 (C) ROMs are not Random access Devices
 (D) RAMs are generally non-volatile.</p> <p align="right">[GATE – IN – 2004]</p> <p>(97) The sink current of the TTL NAND gate shown in Fig. is 16 mA and the input capacitance of the CMOS NAND gate is 10 pF. The minimum pull-up time constant in ns for the CMOS gate with these specifications is</p> <div style="text-align: center;"> </div> <p>(A) 10.2 (B) 7.5
 (C) 8.5 (D) 6.5</p> <p align="right">[IES – EC – 2012]</p> <p>(98) In locations where the humidity is low, ICs based on one of the following technologies should be handled only after grounding the body. The technology is
 (A) TTL (B) CMOS
 (C) DTL (D) I²L</p> <p align="right">[IES – EC – 2009]</p> <p>(99) Which one of the following logic families can be operated using a supply voltage from 3 V to 15 V?
 (A) TTL (B) ECL
 (C) PMOS (D) CMOS</p> <p align="right">[IES – EC – 2006]</p> <p>(100) Consider the following statements describing the property of a complementary MOS(CMOS) inverter;</p> <ol style="list-style-type: none"> 1. It is a combination of an n-channel FET and a p-channel FET. 2. There is power dissipation when the input carries the logical 1 signal. 3. There is no power dissipation when the input carries the logical 1 signal. 4. There is power dissipation during transition from 0 to 1 or from 1 to 0. <p>Which of the statements given above are correct ?</p> |
|--|--|

- | | |
|----------------|----------------|
| (A) 1,2 and 3 | (B) 2, 3 and 4 |
| (C) 1, 3 and 4 | (D) 1, 2 and 4 |

[IES – EC – 2006]

- (101) Match List I with List II and select the correct answer using the code given below the Lists:

List I		List II
(TTL Nos.)		(Significance)
A.	74 LS 00	1. Low power/low speed
B.	74 H 00	2. High speed/high power
C.	74 00	3. Basic NAND Gate
D.	74 L 00	4. Low power Schottky

Codes:

- | A | B | C | D |
|-------|---|---|---|
| (A) 4 | 2 | 3 | 1 |
| (B) 3 | 1 | 4 | 2 |
| (C) 4 | 1 | 3 | 2 |
| (D) 3 | 2 | 4 | 1 |

[IES -EC - 2002]

- (102) Match List I with List II select the correct answer using codes given below the lists:

List I		List II
A.	TTL	1. Low propagation delay
B.	ECL	2. Low power consumption
C.	MOS	3. Higher packing density on Si wafer
D.	CMOS	4. Saturated bipolar logic
		5. High fan-out

Codes:

- | A | B | C | D |
|-------|---|---|---|
| (A) 4 | 1 | 3 | 2 |
| (B) 5 | 3 | 2 | 1 |
| (C) 4 | 3 | 2 | 1 |
| (D) 5 | 1 | 3 | 2 |

[IES – EC – 1997]

- (103) Which of the following standard TTL parameter pairs are correctly matched?

- Worst case high voltage at the input V_{IH} min..... 2v.

- Fan out ----- 40.
- Worst case output current at low level $I_{OL\ max}$ ----- 16 mA
- Direct compatibility with CMOS ----- NOT possible

Select the correct answer using the codes given below

Codes :

- | |
|-------------------|
| (A) 1, 2, 3 and 4 |
| (B) 2 and 4 |
| (C) 1, 2 and 3 |
| (D) 1, 3 and 4 |

[IES – EC – 1994]

- (104) Match List – I with List – II and select the correct answer, using the codes given below the lists

List –I (Logic gate)

- | |
|-----------|
| A. TTL |
| B. CMOS |
| C. I^2L |
| D. ECL |

List – II (Characteristic)

- High Fan – out
- Highest speed of operation
- High noise immunity
- Lowest product of power and delay

Codes :

- | A | B | C | D |
|-------|---|---|---|
| (A) 4 | 2 | 1 | 4 |
| (B) 1 | 3 | 2 | 3 |
| (C) 3 | 1 | 4 | 2 |
| (D) 3 | 4 | 1 | 2 |

[IES - EE - 1993]

- (105) Match List I (Logic circuit) with List II (Property) and select the correct answer using the codes given below the List:

List I

- A. DTL

- B. TTL

- C. NMOS

- D. CMOS

List II

1. High voltage supply

2. High speed of operation

3. High packing density

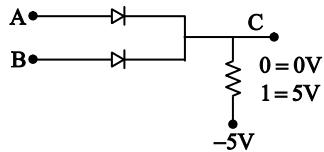
4. High noise margin

Codes:

- | A | B | C | D |
|-------|---|---|---|
| (A) 1 | 3 | 2 | 4 |
| (B) 2 | 1 | 3 | 4 |
| (C) 1 | 2 | 3 | 4 |
| (D) 2 | 3 | 4 | 1 |

[IES - EE - 1996]

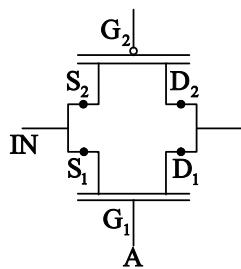
- (106) If negative logic is used, the diode gate shown in the given figure will represent



- (A) OR gate
- (B) AND gate
- (C) NOR gate
- (D) NAND gate

[IES - EC - 1997]

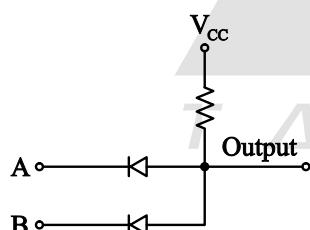
- (107) The schematic shown in the figure indicated



- (A) CMOS NOR gate
- (B) CMOS NAND gate
- (C) CMOS AND gate
- (D) CMOS transmission gate

[GATE-IN-1994]

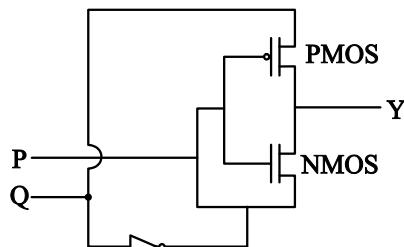
- (108) The diode circuit shown in figure functions as



- (A) AND gate
- (B) OR gate
- (C) NAND gate
- (D) NOR gate

[GATE-S2-EC-2017]

- (109) For the circuit shown in the figure. P and Q are the inputs and Y is the output.

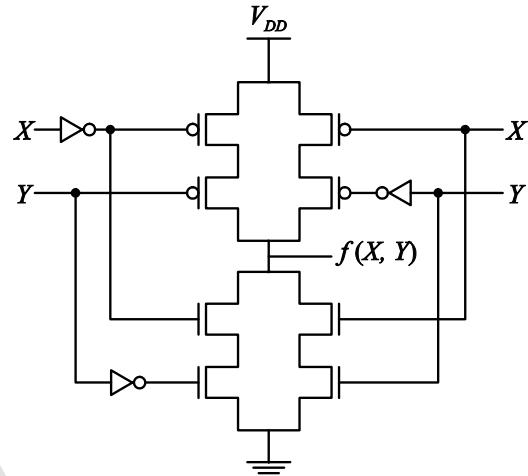


The logic implemented by the circuit is

- (A) XNOR
- (B) XOR
- (C) NOR
- (D) OR

[GATE - EC - 2018]

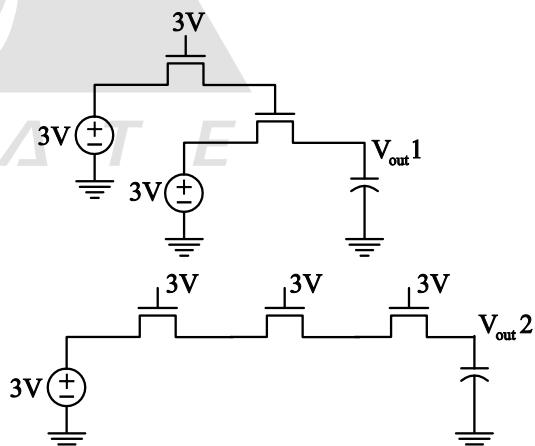
- (110) The logic function $f(X, Y)$ realized by the given circuit is



- (A) NOR
- (B) AND
- (C) NAND
- (D) XOR

[GATE-EC-2019]

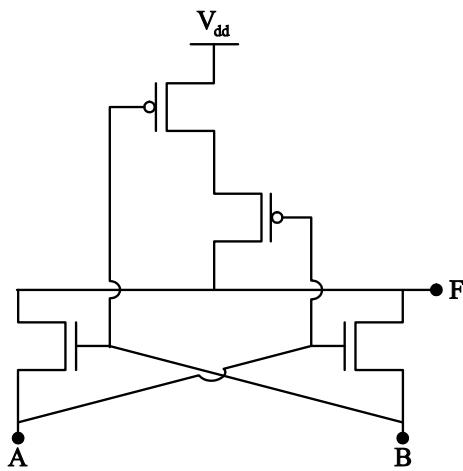
- (111) In the circuits shown the threshold voltage of each nMOS transistor is 0.6 V. Ignoring the effect of channel length modulation and body bias, the values of V_{out1} and V_{out2} , respectively, in volts, are



- (A) 1.8 and 2.4
- (B) 2.4 and 2.4
- (C) 1.8 and 1.2
- (D) 2.4 and 1.2

[GATE-EC-2019]

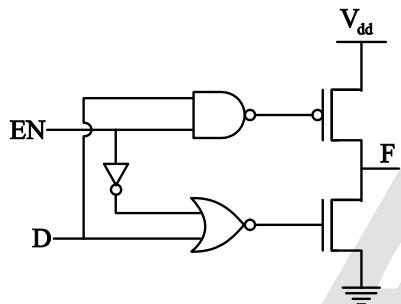
- (112) In the circuit shown, A and B are the inputs and F is the output. What is the functionality of the circuit?



- (A) XNOR (B) SRAM Cell
 (C) Latch (D) XOR

[GATE-EC-2019]

(113) In the circuit shown, what are the values of F for EN = 0 and EN = 1, respectively?



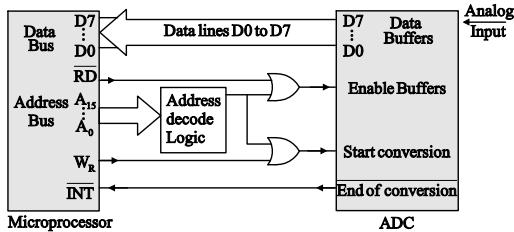
- (A) Hi-Z and D (B) 0 and D
 (C) Hi-Z and \bar{D} (D) 0 and 1

08

A/D & D/A Converters

[GATE – IN – 2015]

- (1) An ADC is interfaced with a microprocessor as shown in the figure. All signals have been indicated with typical notations. Acquisition of one new sample of the analog input signal by the microprocessor involves



- (A) one READ cycle only
- (B) one WRITE cycle only
- (C) one WRITE cycle followed by one READ cycle
- (D) one READ cycle followed by one WRITE cycle

[GATE-IN-2002]

- (2) Majority of digital voltmeters are built with a dual slope ADC because
- (A) Dual slope ADCs are less complex than other type of ADCs
 - (B) Dual slope ADCs are faster than other types of ADCs
 - (C) Dual slope ADCs can be designed to be insensitive to noise and interference
 - (D) Dual slope ADCs provide BCD outputs.

Common Data Questions for Next Two Questions :

In a dual slope ADC, the reference voltage is 100 mV and the first integration period is set as 50 msec. The input resistor of the integrator is $1\text{ k}\Omega$ and the integrating capacitor $0.047\text{ }\mu\text{F}$.

[GATE - IN - 2003]

- (3) For an input voltage of 120mV, the second integration (de-integration) period will be
- (A) 50 ms
 - (B) 60ms

(C) 100 ms

(D) 120 ms

[GATE - IN - 2003]

- (4) If the input of 120 mV is corrupted by power supply interference at 50 Hz having peak amplitude of 3π mV, the worst-case error introduced by the interference in the reading is
- (A) 0%
 - (B) 1%
 - (C) 3%
 - (D) $\pi\%$

[GATE-IN-2009]

- (5) The circuit is used at a sampling rate of 1 kHz, with an A/D converter having a conversion time to $200\mu\text{s}$. The opamp has an input bias current of 10 nA . The maximum hold error is

- (A) 1 mV
- (B) 2 mV
- (C) 5 mV
- (D) 10 mV

[GATE-IN-2014]

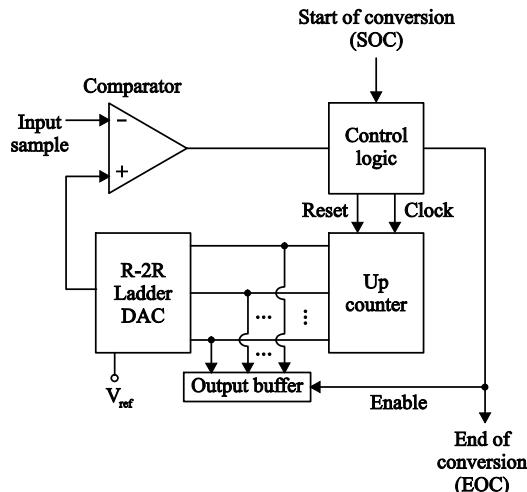
- (6) An N-bit ADC has an analog reference voltage V. Assuming zero mean and uniform distribution of the quantization error, the quantization noise power will be :

- (A) $\frac{V^2}{12(2^N - 1)^2}$
- (B) $\frac{V^2}{12(2^N - 1)}$
- (C) $\frac{V}{12(2^N - 1)}$
- (D) $\frac{V^2}{\sqrt{12}}$

[GATE-IN-2014]

- (7) The circuit in the figure represents a counter-based unipolar ADC. When SOC is asserted the counter counts up and the DAC output grows. When the DAC output exceeds the input sample value, the comparator switches from logic 0 to logic 1, disabling the clock and enabling the output buffer by asserting EOC. Assuming all components to be ideal, V_{ref} , DAC output and input to be positive,

the maximum error in conversion of the analog sample value is



- (A) directly proportional to V_{ref}
- (B) inversely proportional to V_{ref}
- (C) independent of V_{ref}
- (D) directly proportional to clock frequency

[GATE-EE-2015]

- (8) An 8-bit, unipolar Successive Approximation Register type ADC is used to convert 3.5 V to digital equivalent output. The reference voltage is +5V. The output of the ADC at the end of 3rd clock pulse after the start of conversion, is
- (A) 1010 0000
 - (B) 1000 0000
 - (C) 0000 0001
 - (D) 0000 0011

[GATE – EC – 2014]

- (9) For a given sample and hold circuit if the value of the hold capacitor is increased, then
- (A) Droop rate decreases and acquisition time decreases
 - (B) Droop rate decreases and acquisition time increases
 - (C) Droop rate decreases and acquisition time decreases
 - (D) Droop rate decreases and acquisition time increases

[IES – EE – 1994]

- (10) Number of comparators required to build a 5-bit Analog to Digital Converted (ADC) is
- (A) 5
 - (B) 11
 - (C) 21
 - (D) 31

[IES – EE – 1999]

- (11) The number of comparators needed in a 4-bit flash- type A/D converter is
- (A) 32
 - (B) 15
 - (C) 8
 - (D) 4

[IES – EE – 2003]

- (12) An n-bit A/D converter is required to convert an analog input in the range 0-5 V to an accuracy of 10 mV. The value of n should be
- (A) 16
 - (B) 10
 - (C) 9
 - (D) 8

[IES – EC – 1991]

- (13) The resolution for N bit system D/A converter is
- (A) $\frac{1}{2^N}$
 - (B) $\frac{1}{2^N - 1}$
 - (C) $2^N - 1$
 - (D) 2^N

[IES – EC – 1993]

- (14) Which one of the following is a D to A conversion technique?
- (A) Successive approximation
 - (B) Weighted resistor technique
 - (C) Dual slop technique
 - (D) Single slope technique

[IES – EC – 1994]

- (15) A 10 – bit D/A converter provides an analog output which has a maximum value of 10.23 volts. The resolution is
- (A) 10 mV
 - (B) 20 mV
 - (C) 15 mV
 - (D) 25 mV

[IES – EC – 1994]

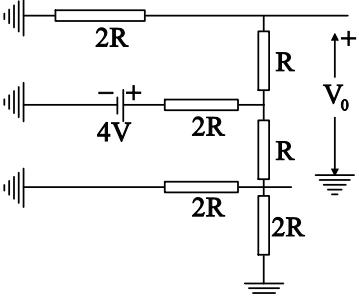
- (16) The disadvantage of a counter type A/D converter as comparator type A/D converter is that
- (A) The resolution is low
 - (B) Longer conversion time is required
 - (C) The circuitry is more complex
 - (D) Its stability is low

[IES – EC – 1994]

- (17) Flash ADC is
- (A) A serial ADC
 - (B) A parallel ADC
 - (C) Partly serial and partly parallel ADC
 - (D) Successive approximately ADC

[IES – EC – 1996]

- (18) Consider the Analog to Digital converters given below:
1. Successive Approximation ADC
 2. Dual Ramp ADC
 3. Counter method ADC
 4. Simultaneous ADC

- The correct sequence of the ascending order in terms of conversion times of these ADC's is
- (A) 3,2,4,1 (B) 2,3,4,1
 (C) 4,1,3,2 (D) 3,2,1,4
- [IES – EC – 2010]**
- (19) A D/A converter has 5 V full scale output voltage and an accuracy of $\pm 0.2\%$. The maximum error for any output voltage will be
- (A) 5 mV (B) 10 mV
 (C) 20 mV (D) 25 mV
- [IES – EC – 1997]**
- (20) A 12 bit ADC is employed to converts an analog voltage of zero to 10 volts. The resolution of the ADC is
- (A) 2.44 mV (B) 24.4 mV
 (C) 83.3 mV (D) 1.2 V
- [IES – EC – 1997]**
- (21) In a 4 – bit weighted – resistor D/A converter, the resister value corresponding to LSB is 16 K Ω . The resistor value corresponding to the MSB will be
- (A) 1 K Ω (B) 2 K Ω
 (C) 4 K Ω (D) 16 K Ω
- [IES – EC – 1998]**
- (22) The resolution of an – n – bit D/A converter with a maximum input of 5V is 5mV. The value of 'n' is
- (A) 8 (B) 9
 (C) 10 (D) 11
- [IES – EC – 1999]**
- (23) The output voltage V_o with respect to ground of the R-2R ladder network shown in the given figure is
- 
- (A) 1 V (B) 2 V
 (C) 3V (D) 4V
- [IES – EC – 2001]**
- (24) The output voltage of a 5-bit D/A binary ladder that has a digital input of 11010 (Assuming 0 = 0V and 1 = +10V) is
- (A) 3.34375V (B) 6.0 V
 (C) 8.125V (D) 16 μ s
- [IES – EC – 2001]**
- (25) An 8-bit D/A converter has a full scale output voltage of 20V. The output voltage when the input is 11011011, is
- (A) 160mV (B) 78mV
 (C) 20V (D) 17V
- [IES – EC – 2004/2009]**
- (26) Match List I with List II and select the correct answer using the code given below the lists:
- List I**
(Type of N-bit ADC)
- A. Flash Converter
 - B. Successive approximation
 - C. Counter ramp
 - D. Dual slope
- List II**
(Characteristics)
- 1. Integrating Type
 - 2. Fastest converter
 - 3. Maximum conversion time = N bits
 - 4. Uses a DAC in its feedback path
- Codes:**
- | | A | B | C | D |
|-----|---|---|---|---|
| (A) | 2 | 3 | 4 | 1 |
| (B) | 1 | 3 | 4 | 2 |
| (C) | 2 | 4 | 3 | 1 |
| (D) | 1 | 4 | 3 | 2 |
- [IES – EC – 2006]**
- (27) Which one of the following D/A converters has the resolution of approx. 0.4% of its full scale range?
- (A) 8-bit (B) 10-bit
 (C) 12-bit (D) 16-bit
- [IES – EC – 2008]**
- (28) How many bits will a D/A converter use so that its full-scale output voltage is 5V and its resolution is at the most 10 mV?
- (A) 5 (B) 7
 (C) 9 (D) 11
- [IES – EC – 2009]**
- (29) In which one of the following types of analog to digital converters the conversion time is practically independent of the amplitude of the analog signal?
- (A) The dual slope integrating type
 (B) Successive approximation type

- (C) Counter ramp type
 - (D) Tracking type

[IES – EC – 2011]

- (30) Consider the following statements for an N - bit DACs :

 1. R – 2R ladder type is based on dual slopes integration.
 2. R – 2R requires resistors of large spread in values
 3. R – 2R requires roughly $2N$ resistors.
 4. R - 2R requires roughly N Number of resistors.

Which of these statements are correct?

[IES – EC – 2012]

[IES - EC - 2012]

- (32) In which of the following type of A/D converter does the conversion time almost double for every bit added to the device?

 - (A) Counter type A/D converter
 - (B) Tracking type A/D converter
 - (C) Single – slope integrating type A/D converter
 - (D) Successive approximation type A/D converter

[IES – EC – 2012]

- (33) A 12-bit ADC is operating with a $1\text{ }\mu\text{s}$ clock period and total conversion time seen to be $14\text{ }\mu\text{s}$. The ADC must be of

 - (A) Flash type
 - (B) Counting type
 - (C) Integrating type
 - (D) Successive approximately type

[GATE - IN - 1996]

- (34) An 8 bit ADC outputs all 1's when $V_{in} = 1.275$ volts. The quantization error is

[GATE - IN - 1996]

- (35) A 3-bit resistance ladder D/A (R-2R network) has resistor values of $R = 10 \text{ k}\Omega$ and $20 \text{ k}\Omega$. V_{REF} equals 8 volts. What is I_{out} for a digital input of 111?

- (A) 0.7 mA (B) 0.2 mA
 (C) 0.1 mA (D) 1 mA

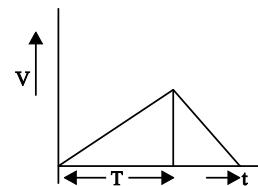
[GATE - IN - 1997]

- (36)** A sample – and – hold circuit is normally required before the following type of A/D converter

- (A) Successive approximation
 - (B) Flash (parallel) converter
 - (C) Voltage – to – frequency converter
 - (D) Dual slope integrator.

[GATE - IN - 1998]

- (37) Integrated output waveform for the dual slope ADC is shown in Fig. The time T for an 8 bit counter with 4 MHz clock will be



- (A) 0.032 ms (B) 0.064 ms
 (C) 0.64 ms (D) 0.024 ms

[GATE - IN - 1998]

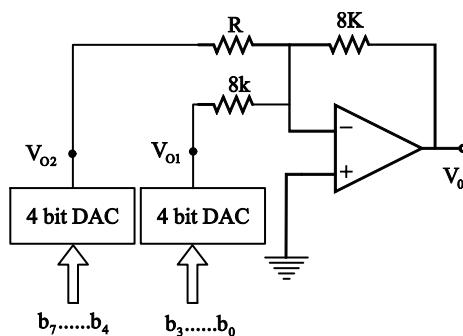
- (38) Percent resolution of an 8 bit D/A converter is
(A) 0.39 **(B)** 0.78
(C) 2.56 **(D)** None of these

[GATE - IN - 2004]

- (39) The number of comparators required in an 8-bit flash – type A/D converter is
(A) 256 **(B)** 255
(C) $(8+2)$ **(D)** 8

[GATE - IN - 2011]

- (40) Figure below shows a circuit of implementing an 8-bit Digital – to – Analog converter (DAC) using two identical 4-bit DACs with equal reference voltages. Assume that b_0 represents LSB, b_7 MSB and the opamp is ideal. To obtain correct analog values corresponding to an 8-bit DAC at the output V_0 , the value of resistor R is



- (A) $0.25 \text{ k}\Omega$ (B) $0.5 \text{ k}\Omega$
 (C) $1 \text{ k}\Omega$ (D) $8 \text{ k}\Omega$

[GATE - IN - 1999]

- (41) The advantage of a dual slope converter over successive approximation converter is that the dual slope converter
 (A) Is faster
 (B) Eliminates error due to drift
 (C) Can reduce the errors due to power supply
 (D) Does not require a stable voltage reference

[GATE - IN - 1999]

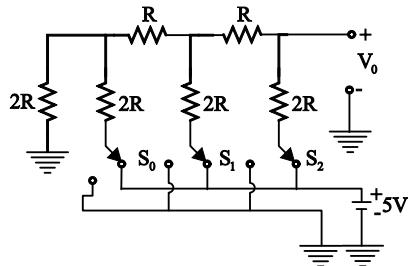
- (42) The conversion time of an 8-bits successive approximation converter with a 1 MHz clock is nearly
 (A) $512 \mu\text{s}$ (B) $256 \mu\text{s}$
 (C) $128 \mu\text{s}$ (D) $8 \mu\text{s}$

[GATE - IN - 2003]

- (43) In a dual slope ADC, the reference voltage is 100 mV and the first integration period is set as 50 ms. The input resistor of the integrator is $100 \text{ k}\Omega$ and the integrating capacitor 0.047 μF . For an input voltage of 120mV, the second integration (de-integration) period will be
 (A) 50 ms (B) 60ms
 (C) 100ms (D) 120ms

Common Data Questions for Next Two Questions :

An R – 2R ladder type DAC is shown below. If a switch status is 0, 0V is applied and if a switch status is 1, 5V is applied to the corresponding terminal of the DAC.

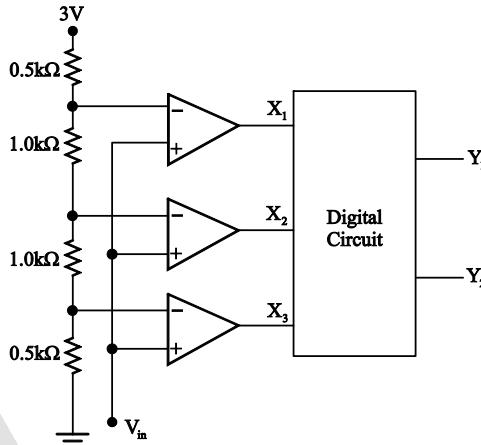


[GATE - IN - 2006]

- (44) What is the output voltage (v_o) for the switch status $S_0 = 0, S_1 = 1, S_2 = 1$?
 (A) $\frac{5}{4} \text{ V}$ (B) $\frac{15}{4} \text{ V}$
 (C) $\frac{17.5}{4} \text{ V}$ (D) $\frac{22.5}{4} \text{ V}$

- [GATE - IN - 2006]
 (45) What is the step size of the DAC?
 (A) 0.125 V (B) 0.525 V
 (C) 0.625 V (D) 0.75 V

- [GATE - IN - 2007]
 (46) The circuit shown in the figure below works as a 2-bit analog to digital converter for $0 \leq V_{in} \leq 3\text{V}$.

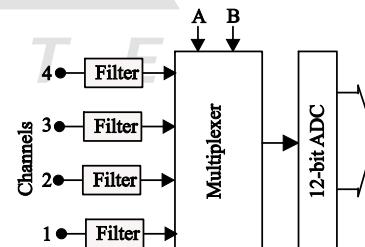


The MSB of the output Y_1 , expressed as a Boolean function of the inputs $X_1 X_2 X_3$ is given by

- (A) X_1 (B) X_2
 (C) X_3 (D) $X_1 + X_2$

Common Data Questions for Next Three Questions :

A data acquisition system (DAS) shown below employs a successive approximation type 12-bit ADC having a conversion time of $5\mu\text{s}$.



- [GATE - IN - 2008]
 (47) The quantization error of the ADC is
 (A) 0% (B) $\pm 0.012\%$
 (C) $\pm 0.024\%$ (D) $\pm 0.048\%$

- [GATE - IN - 2008]
 (48) The system is used as a single channel DAS with channel 1 selected as input to the ADC which is in the continuous conversion mode, for avoiding aliasing error, the cutoff frequency f_c of the filter in channel 1 should be

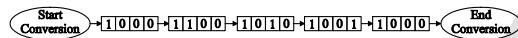
- (A) $f_c < 100 \text{ kHz}$
- (B) $f_c = 100 \text{ kHz}$
- (C) $100 \text{ kHz} < f_c < 200 \text{ kHz}$
- (D) $f_c = 200 \text{ kHz}$

[GATE - IN - 2008]

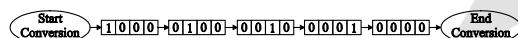
- (49) If the multiplexer is controlled such that the channels are sequenced every $5 \mu\text{s}$ as 1,2,1,3,1,4,1,2,1,3,1,4,1,....., the input connected to channel 1 will be sampled at the rate of the filter in channel 1 will be sampled at the rate of
- (A) 25k samples/s
 - (B) 50k samples/s
 - (C) 100k samples/s
 - (D) 200k samples/s

[GATE - IN - 2010]

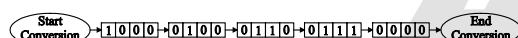
- (50) A 4-bit successive approximation type ADC has a full scale value of 15V. The sequence of the states, the SAR will traverse, for the conversion of an input of 8.15 V is



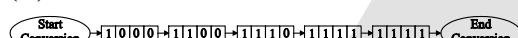
(A)



(B)



(C)



(D)

[GATE - IN - 2011]

- (51) A 4-bit successive approximation type of A/D converter has an input range of 0 to 15 volts. The output bit b_1 next to the LSB has a stuck at zero fault. The pair of input voltages that produces the same output code word is

- (A) 2V and 4V
- (B) 4V and 6V
- (C) 1V and 2V
- (D) 8V and 9V

[IES – EC – 2006/GATE - EE -1993]

- (52) A 10 bit A/D converter is used to digitize an analog signal in the 0 to 5 V range. The maximum peak to peak ripple voltage that can be allowed in the D.C. supply voltage is
- (A) Nearly 100mV
 - (B) Nearly 50mV
 - (C) Nearly 25mV
 - (D) Nearly 5.0 mV

[GATE - EE - 1994]

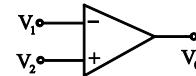
- (53) The number of comparisons carried out in a 4-bit flash-type A/D converter is
- | | |
|--------|--------|
| (A) 16 | (B) 15 |
| (C) 4 | (D) 3 |

[GATE - EE - 2001]

- (54) Among the following four, the slowest ADC (analog-to-digital converter) is
- (A) Parallel-comparator (i.e., flash) type
 - (B) Successive approximation type
 - (C) Integrating type
 - (D) Counting type

[GATE - EE - 2004]

- (55) The voltage comparator shown in Fig. can be used in the analog-to-digital conversion as



(A) a 1-bit quantizer

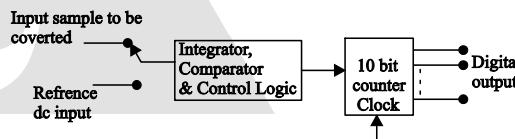
(B) a 2-bit quantizer

(C) a 4-bit quantizer

(D) a 8-bit quantizer

[GATE - EE - 2003]

- (56) The simplified block diagram of a 10-bit A/D converter of dual slope integrator type is shown in the Fig. The 10-bit counter at the output is clocked by a 1 MHz. clock. Assuming negligible timing overhead for the control logic, the maximum frequency of the analog signal that can be converted using this A/D converter is approximately.



(A) 2 kHz

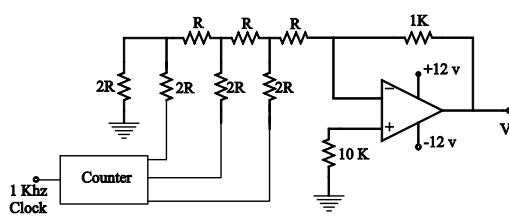
(B) kHz

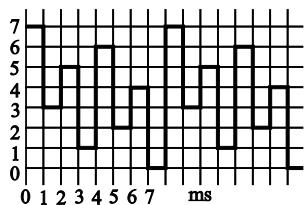
(C) 500 Hz

(D) 250 Hz

[GATE - EE - 2006]

- (57) A student has made a 3-bit binary down counter and connected to the R-2R ladder type DAC [Gain = $(-1 \text{ k}\Omega / 2R)$] as shown in figure to generate a staircase waveform. The output achieved is different as shown in figure. What could be the possible cause of this error?

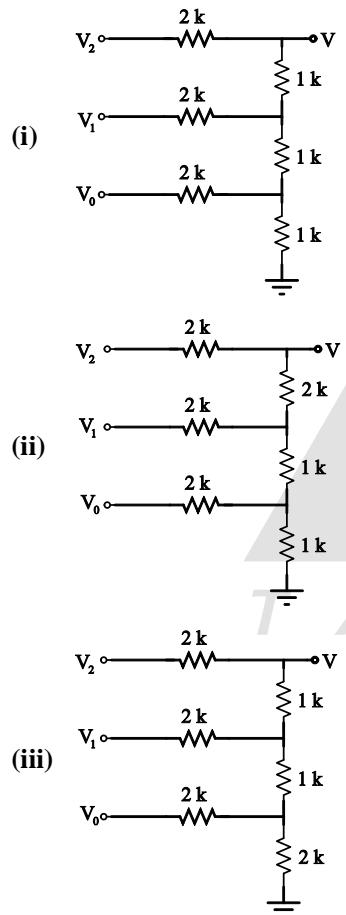




- (A) The resistance values are incorrect
 - (B) The counter is not working properly
 - (C) The connection from the counter to DAC is not proper
 - (D) The R and 2R resistances are interchanged

[GATE -EC - 1990]

- (58) Which of the resistance networks of figure can be used as 3 bit R-2R ladder DAC. Assume V_0 corresponds to LSB.



- (A) Both (i) and (iii)
 - (B) Both (i) and (iii)
 - (C) Only (iii)
 - (D) Only (ii)

[GATE -EC - 1995]

- (59)** For an ADC, match the following: if

List – I

- (A) Flash converter
 - (B) Dual slope converter
 - (C) Successive approximation Converter

List – II

- (1) requires a conversion time of the order of a few seconds
 - (2) requires a digital-to-analog converter
 - (3) minimizes the effect of power supply interference.
 - (4) requires a very complex hardware.
 - (5) is a tracking A/D converter.

[GATE -EC - 1999]

- (60) The resolution of a 4-bit counting ADC is 0.5 volts. For an analog input of 6.6 volts, the digital output of the ADC will be

- (A) 1011 (B) 1101
(C) 1100 (D) 1110

[GATE -EC - 2000]

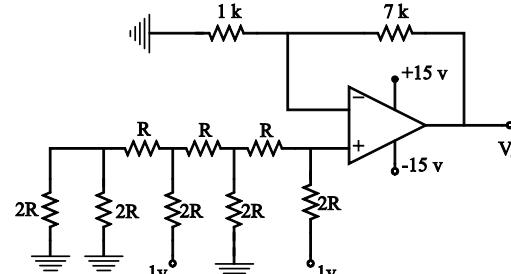
- (61) An 8-bit successive approximation analog to digital converter has full scale reading of 2.55 V and its conversion time for an analog input of 1 V is $20\mu s$. The conversion time for a 2V input will be

- (A) $10\mu s$ (B) $20\mu s$
 (C) $40\mu s$ (D) $50\mu s$

[GATE -EC -2003]

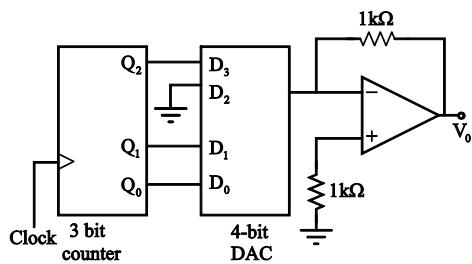
[GATE -EC - 2000]

- (63) For the 4 bit DAC shown in the figure, the output voltage V_o is :

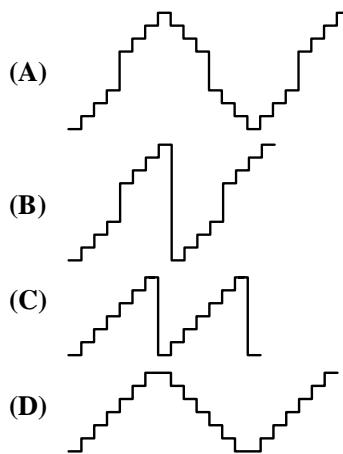


[GATE -EC - 2006]

- (64) A 4-bit D/A converter is connected to a free-running 3-bit up counter, as shown in the following figure which of the following waveforms will be observed at V_0 = ?

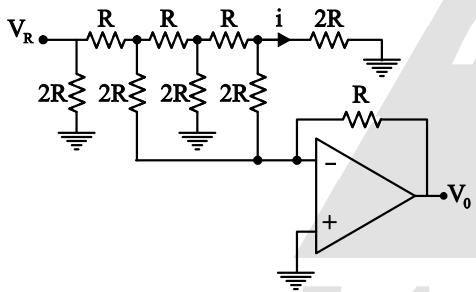


In the figure shown above, the ground has been shown by the symbol



Statement for Linked Answer Questions for Next Two Questions :

In the Digital-to-Analog converter circuit shown in the figure below, $V_R = 10\text{ V}$ and $R = 10\text{ k}\Omega$.



[GATE -EC -2007]

(65) The current i is

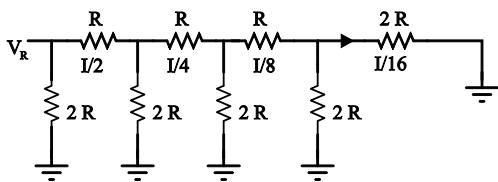
- (A) $31.25\mu\text{A}$ (B) $62.5\mu\text{A}$
 (C) $125\mu\text{A}$ (D) $250\mu\text{A}$

[GATE -EC - 2007]

(66) The voltage V_0 is

- (A) -0.781 v (B) -1.562 v
 (C) -3.125 v (D) -6.250 v

(67) The current i is :



- (A) $31.25\ \mu\text{A}$ (B) $62.5\ \mu\text{A}$
 (C) $125\ \mu\text{A}$ (D) $250\ \mu\text{A}$

(68) The number of comparators in a 4-bit flash ADC is

- (A) 4 (B) 5
 (C) 15 (D) 16

[GATE – EE – 1994]

(69) The contents of the accumulator in an 8085 microprocessor is altered after the execution of the instruction.

- (A) CMP C (B) CPI 3A
 (C) ANI 5C (D) ORA A

(70) An 8-bit ADC, with 2's compliment output, has a nominal input range of -2V to $+2\text{V}$. It generates a digital code of 00H for an analog input in the range -7.8125 mV to $+7.815\text{ mV}$. An input of -1.5 V will produce a digital output of

- (A) 90 H (B) 96H
 (C) 9 BH (D) $A0\text{H}$

[GATE -IN – 2006]

(71) A single channel single acquisition system with $0\text{-}10\text{ V}$ range consists of a sample – and – hold circuit with worst case drop rate of $100\ \mu\text{V}/\text{ms}$ and 10-bit ADC. The maximum conversion time for the ADC is

- (A) 49 ms (B) 0.49 ms
 (C) 4.9 ms (D) 49 ms

[GATE-IN-1994]

(72) The percent resolution of a 10 bit D/A converter is

[GATE – IN – 1998]

(73) The full scale input voltage to an ADC is 10V . The resolution required is 5mV . The minimum number of bits required for ADC is :

- (A) 8 (B) 10
 (C) 11 (D) 12

(74) An 8-bit 2's complement representation of an integer is FA(hex). Its decimal equivalent is

- (A) 10 (B) -6
 (C) +6 (D) +10

[IES – EC – 2012]

(75) Match List – I with List – II and select the correct answer using the code given below the lists

List – I

- A. Flash converter ADC
- B. Successive approximation ADC
- C. Counter ramp ADC
- D. Dual slope ADC

List – II

- 1. Integrating type
- 2. Fast conversion
- 3. Maximum conversion clock periods = number of bits
- 4. Uses a DAC in its feedback path

Codes :

A	B	C	D
(A) 2	3	4	1
(B) 1	3	4	2
(C) 2	4	3	1
(D) 1	4	3	2

(76) Dual-slope integration type Analog-to-Digital converters provide :

- 1. Higher speeds compared to all other types of A/D converters
 - 2. Very good accuracy without putting extreme requirements on component stability.
 - 3. Good rejection of power supply hum.
 - 4. Better resolution compared to all other types of A/D converters for the same number of bits.
- (A) 2 and 3 only
 (B) 3 and 4 only
 (C) 4 and 1 only
 (D) 1, 2, 3 and 4

[IES – EC – 2008]

(77) In order to build a 3 bit simultaneous A/D converter, what is the number of comparator circuits required?

- | | |
|--------|--------|
| (A) 7 | (B) 8 |
| (C) 15 | (D) 16 |

[IES – EC – 2003]

(78) A 10-bit ADC with full-scale output voltage of 10.24V is designed to have a \pm LSB/2 accuracy. If the ADC is calibrated at 25°C and the operating temperature ranges from 0°C to 50°C , then the maximum net temperature coefficient of ADC should not exceed.

- | | |
|---|---|
| (A) $\pm 200\mu\text{V} / {}^{\circ}\text{C}$ | (B) $\pm 400\mu\text{V} / {}^{\circ}\text{C}$ |
| (C) $\pm 600\mu\text{V} / {}^{\circ}\text{C}$ | (D) $\pm 800\mu\text{V} / {}^{\circ}\text{C}$ |

(79) In successive – approximation A/D converter, offset voltage equal to $\frac{1}{2}$ LSB is added to the D/A converter's output. This is done to

- (A) Improve the speed of operation
- (B) Reduce the maximum quantization error
- (C) Increase the number of bits at the output
- (D) Increase the range of input voltage that can be converted

[IES – EC – 1999]

(80) **Assertion (A):** The output of an 8 – bit A to D converter is 80H for an input of 2.5V

Reason(R): ADC has an output range of 00 to FFH for an input range of -5V to +5V

- (A) Both A and R is true and R is the correct explanation of A
- (B) Both A and R is true but R is NOT the correct explanation of A
- (C) A is true but R is false
- (D) A is false but R is true

[IES – EC – 1991]

(81) For a D/A converter, the resolution required is 50 mV and the total maximum output voltage is 10V. The number of bits required is

- | | |
|-------|---------|
| (A) 7 | (B) 8 |
| (C) 9 | (D) 200 |

[IES – EC – 1994]

(82) In a 4 – bit weighted resistor D/A converter, the resistor value corresponding to LSB is $32\text{ K}\Omega$. The resistor value corresponding to MSB will be

- | | |
|-------------------------|-------------------------|
| (A) $32\text{ K}\Omega$ | (B) $16\text{ K}\Omega$ |
| (C) $8\text{ K}\Omega$ | (D) $4\text{ K}\Omega$ |

[IES – EC – 2015]

(83) A 4 – bit D/A converter gives an output voltage of 4.5 V for an input code of 1001. The output voltage for an input code of 0110.

- | | |
|-----------|-----------|
| (A) 1.5 V | (B) 2.0V |
| (C) 3.0 V | (D) 4.5 V |

(84) For N-bit successive Approximation ADC's, other parameters such as clock frequency remaining constant, the conversion time is proportional to

- (A) N^2 (B) \sqrt{N}
(C) $\log N$ (D) N

[GATE – EE – 1999]

[GATE – EC – 1998]

- (86)** The advantage of using a dual slope ADC in a digital voltmeter is that

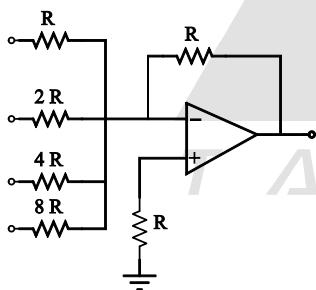
 - (A)** its conversion time is small
 - (B)** its accuracy is high
 - (C)** it gives output in BCD format
 - (D)** it does not require a comparator.

[GATE – EC – 2003]

- (87) The circuit shown in the figure is a 4 bit DAC

The input bits 0 and 1 are represented by 0 and 5v respectively. The OP-AMP is ideal, but all the resistances and the 5V inputs have a tolerance of $\pm 10\%$.

The specification (rounded to the nearest multiple of 5%) for the tolerance of the DAC is



- (A) $\pm 35\%$ (B) $\pm 20\%$
(C) $\pm 10\%$ (D) $\pm 5\%$

[GATE-EC-2000]

[GATE-EC-2002]

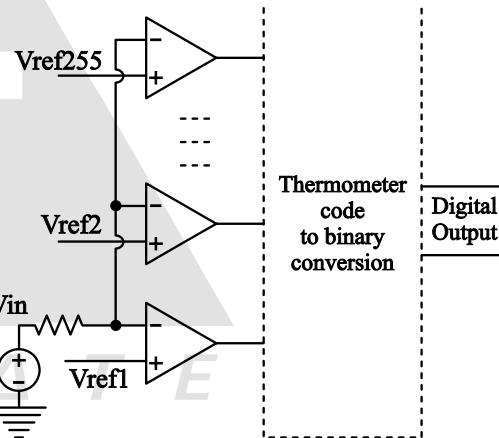
[GATE-S6-EE-2016]

- (90) A temperature in the range of -40° C to 55° C is to be measured with a resolution of 0.1° C . The minimum number of ADC bits required to get a matching dynamic range of the temperature sensor is

(A) 8
(B) 10
(C) 12
(D) 14

[GATE-S3-EC-2016]

- (91)** In an N bit flash ADC, the analog voltage is fed simultaneously to $2^N - 1$ comparators. The output of the comparators is then encoded to a binary format using digital circuits. Assume that the analog voltage source V_{in} (whose output is being converted to digital format) has a source resistance of 75Ω as shown in the circuit diagram below and the input capacitance of each comparator is 8 pF . The input must settle to an accuracy of $1/2 \text{ LSB}$ even for a full scale input change for proper conversion. Assume that the time taken by the thermometer to binary encoder is negligible.

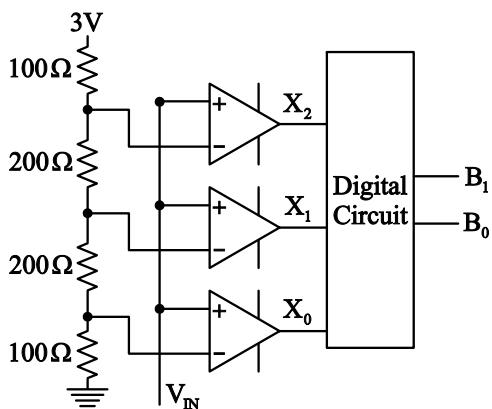


If the flash ADC has 8 bit resolution, which one of the following alternatives is closest to the maximum sampling rate?

- (A) 1 megasamples per second
 - (B) 6 megasamples per second
 - (C) 64 megasamples per second
 - (D) 256 megasamples per second

[GATE-S6-EE-2016]

- (92) A 2-bit flash Analog to Digital Converter (ADC) is given below. The input is $0 \leq V_{IN} \leq 3$ Volts. The expression for the LSB of the output B_0 as a Boolean function of X_2 , X_1 , and X_0 is



- (A)** $X_0[\overline{X_2 \oplus X_1}]$

(B) $\overline{X}_0[\overline{X_2 \oplus X_1}]$

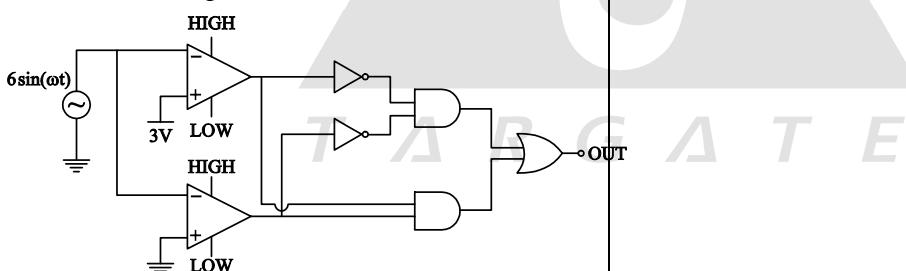
(C) $X_0[X_2 \oplus X_1]$

(D) $\overline{X}_0[X_2 \oplus X_1]$

[GATE – IN – 2018]

[GATE-IN-2019]

- (94) In the circuit shown below, assume that the comparators are ideal and all components have zero propagation delay. In one period of the input signal $V_{in} = 6\sin(\omega t)$, the fraction of the time for which the output OUT is in logic state HIGH is



- (A) $\frac{1}{12}$ (B) $\frac{1}{2}$
(C) $\frac{2}{3}$ (D) $\frac{5}{6}$

[GATE-IN-2019]

- (95) An 8-bit weighted resistor digital-to-analog converter (DAC) has the smallest resistance of 500Ω . The largest resistance has a value $k\Omega$.

-----0000-----

09

MICROPROCESSOR 8085

PROGRAMMING &

BASICS

- [GATE-EC -1997]

[GATE-EC -1997]

- (A) Only if an interrupt service routine is not being executed
 - (B) Only if a bit in the interrupt mask is made 0
 - (C) Only if interrupts have been enabled by an EI instruction
 - (D) None of the above

[GATE-EC -2000]

- (2) The number of hardware interrupts (which require an external signal to interrupt) present in an 8085 microprocessor are

[GATE-EC -2000]

- (3) In the 8085 microprocessor, the RST6 instruction transfers the program execution to the following location:

- (A) 30 H (B) 24 H
(C) 48 H (D) 60 H

[GATE-EC -2009]

- (4) In a microprocessor, the service routine for a certain interrupt start from a fixed location of memory which cannot be externally set, but the interrupt can be delayed or rejected. Such an

- (A) non-maskable and non-vectored
 - (B) maskable and non-vectored
 - (C) non-maskable and vectored
 - (D) maskable and vectored

[GATE-EE-1992]

- (5) If the HLT instruction of a 8085 microprocessor is executed

- (A) the microprocessor is disconnected from the system bus till the reset is pressed.
 - (B) the microprocessor enters into a halt state and the buses are tri-stated.
 - (C) the microprocessor halts execution of the program and returns to monitor.
 - (D) the microprocessor reloads the program from the locations 0024 and 0025H.

[GATE-EE-1993]

- (6)** Three devices A, B and C have to be connected to a 8085 microprocessor. Device A has highest priority and device C has the lowest priority and device C has the lowest priority. In this context which of the statements are correct?

- (A) A uses TRAP, B uses RST 5.5 and C uses RST6.5.
 - (B) A uses RST 7.5, B uses RST 6.5 and C uses RST 5.5.
 - (C) A uses RST 5.5, B uses RST 6.5 and C uses RST 7.5.
 - (D) A uses RST 5.5, B uses RST 6.5 and C uses TRAP.

[GATE-EE-1994]

- (7) The stack pointer of a microprocessor is at A001. At the end of execution of following instruction, the value of stack pointer is

PUSH	PSW
XTHL	
PUSH	D
JMP	FC700

[GATE-EE-1995]

- (8) In an 8085 microprocessor, after the execution of XRA A instruction

 - (A) the carry flag is set.
 - (B) the accumulator contain FFH.

- (C) the zero flag is set.
(D) the accumulator contents are shifted left by one bit.

[GATE-EE-1997]

(9) In a microprocessor, the address of the next instruction to be executed, is stored in

(A) stack pointer
(B) address latch
(C) program counter
(D) general purpose register

[GATE-EE-1997]

- (9) In a microprocessor, the address of the next instruction to be executed, is stored in

 - (A) stack pointer
 - (B) address latch
 - (C) program counter
 - (D) general purpose register

[GATE-EE-2000]

- (10) Which of the following is not a vectored interrupt ?

(A) TRAP (B) INTR
(C) RST 7.5 (D) RST 3

[GATE-EE-2001]

- (11) An Intel 8085 processor is executing the program given below :

Back:	MVI A, 10 H
	MVI B, 10 H
	NOP
	ADD B
	RLC
	JNCBACK
	HLT

The number of times that the operation NOP will be executed is equal to

[GATE-EE-2002]

- (12) When a program is being executed in an 8085 microprocessor, its program counter contains

 - (A) the number of instructions in the current program that have already been executed.
 - (B) the total number of instructions in the program being executed.
 - (C) the memory address of the instruction that is being currently executed.
 - (D) the memory address of the instruction that is to be executed next

[GATE-EE-1996]

- (13) In a 8085 microprocessor, the following instructions may results in change of accumulator contents and change in status flags. Choose the correct match for each instruction.

List-I

- (a) ANA R
 - (b) XRA R
 - (c) CMP R

List-II

Contents of CY flag ACC

- (P) unchanged may be unchanged
 SET

(Q) unchanged SET SET

(R) unchanged SET RESET

(S) may change RESET RESET

(T) may change RESET SET

[GATE-EE-2003]

- (14) The following program is written for an 8085 microprocessor to add two bytes located at memory addresses 1FFE and 1FFF

LXI	H, 1FFE
MOV	B, M
INR	L
MOV	A, M
ADD	B
INR	L
MOV	M, A
XRA	A

On completion of the execution of the program, the result of addition is found

- (A) in the register A
 - (B) at the memory address 1000
 - (C) at the memory address 1F00
 - (D) at the memory address 2000

[GATE-EE-2004]

- (15) If the following program is executed in a microprocessor, the number of instruction cycles it will take from START to HALT is :

START	MVI A, 14 H	;	MOVE 14 H to register A
SHIFT	RLC	;	Rotate left without carry
JNZ	SHIFT	;	Jump on non-zero to SHIFT
HALT		;	

[GATE-EE-2005]

- (16) The 8085 assembly language instruction that stores the content of H and L registers into the memory locations 2050_H and 2051_H , respectively is

- (A) SPHL 2050_H (B) SPHL 2051_H
 (C) SHLD 2050_H (D) STAX 2050_H

[GATE-EE-2006]

- (17) A software delay subroutine is written as given below :

```

DELAY :   MVI H, 255D
          MVI L, 255D

LOOP :    DCR L
          JNZ LOOP
          DCR H
          JNZ LOOP
  
```

How many times DCR L instruction will be executed ?

- (A) 255 (B) 510
 (C) 65025 (D) 65279

[GATE-EE-2006]

- (18) In an 8085 A microprocessor based system, it is desired to increment the contents of memory location whose address is available in (D, E) register pair and store the result in same location. The sequence of instruction is :

- | | |
|-----------|-----------|
| (A) XCHG | (B) XCHG |
| INR M | INX H |
| (C) INX D | (D) INR M |
| XCHG | XCHG |

[GATE-EE-2008]

- (19) The content of some of the memory location in an 8085 A based system are given below

Address	Content
.	.
26FE	00
26FF	01
2700	02
2701	03
2702	04
..	..

The content of stack (SP), program counter (PC) and (H, L) are 2700 H, 2100 H and 0000 H respectively. When the following sequence of instruction are executed

2100 H : DAD SP

2101 H : PCHL

the content of (SP) and (PC) at the end of execution will be

- (A) PC = 2102 H, SP = 2700 H
 (B) PC = 2700 H, SP = 2700 H
 (C) PC = 2800 H, SP = 26FE H
 (D) PC = 2A02 H, SP = 2702 H

[GATE-EE-2009]

- (20) In an 8085 microprocessor, the contents of the Accumulator, after the following instructions are executed will become

XRA A

MVIB F0H

SUB B

- (A) 01 H (B) 0F H
 (C) F0 H (D) 10 H

[GATE-EC -1992]

- (21) The following program is run on an 8085 microprocessor

Memory address is in HEX Instruction

- | | |
|------|--------------|
| 2000 | LXI SP, 1000 |
| 2003 | PUSH H |
| 2004 | PUSH D |
| 2005 | CALL 2050 |
| 2008 | POP H |
| 2009 | HLT |

After the completion of the execution of the program, program counter of the 8085 contains _____, and the stack pointer contains _____.

[GATE-EC -1996]

- (22) The following sequence of instructions are executed by an 8085 microprocessor

- | | |
|------|--------------|
| 1000 | LXI SP, 27FF |
| 1003 | CALL 1006 |
| 1006 | POP H |

The contents of the stack pointer (SP) and the register pair on completion of execution of these instructions are,

- (A) SP = 27FF, HL = 1003
 (B) SP = 27FD, HL = 1003
 (C) SP = 27FF, HL = 1006
 (D) SP = 27FD, HL = 1006

[GATE-EC -1997]

- (23) The following instructions have been executed by an 8085 μ p

ADDRESS (HEX)	INSTRUCTION

<table border="0"> <tr><td>6010</td><td>LXI H, 8A79H</td></tr> <tr><td>6013</td><td>MOV A, H</td></tr> <tr><td>6014</td><td>ADD H</td></tr> <tr><td>6015</td><td>DAA</td></tr> <tr><td>6016</td><td>MOV H, A</td></tr> <tr><td>6017</td><td>PCHL</td></tr> </table> <p>From which address will the next instruction be fetched?</p> <p>(A) 6019 (B) 0379 (C) 6979 (D) None</p> <p style="text-align: center;">[GATE-EC -2002]</p> <p>(24) Consider the following assembly language program</p> <pre>MVIB, 87H MOV A, B START: JMP NEXT MVI B, 00H XRA B OUT PORT 1 HLT NEXT: XRA B JP START OUT PORT 2 HLT</pre> <p>The execution of the above program in an 8085 microprocessor will result in</p> <p>(A) an output of 87H at PORT 1 (B) an output of 87H at PORT 2 (C) infinite looping of the program execution with accumulator data remaining at 00H (D) infinite looping of the program execution with accumulator data alternating between 00H and 87H</p> <p style="text-align: center;">[GATE-EC -2006]</p> <p>(25) Following is the segment of a 8085 assembly language program</p> <pre>LXI SP, EFFFH CALL 3000H 3000H: LXI H, 3CF4H PUSH PSW SPHL POP PSW RET</pre> <p>On completion of RET execution, the contents of SP is</p>	6010	LXI H, 8A79H	6013	MOV A, H	6014	ADD H	6015	DAA	6016	MOV H, A	6017	PCHL	<table border="0"> <tr><td>(A) 3CFOH</td><td>(B) 3CF8H</td></tr> <tr><td>(C) EFFDH</td><td>(D) EFFFH</td></tr> </table> <p>Common Data Questions for Next Two Questions :</p> <p>An 8085 assembly language program is given below</p> <table border="0"> <tr><td>Line</td><td>1: MVI A, B5H</td></tr> <tr><td></td><td>2: MVI B, 0EH</td></tr> <tr><td></td><td>3: XRI 69H</td></tr> <tr><td></td><td>4: ADD B</td></tr> <tr><td></td><td>5: ANI 9BH</td></tr> <tr><td></td><td>6: CPI 9FH</td></tr> <tr><td></td><td>7: STA 3010H</td></tr> <tr><td></td><td>8: HLT</td></tr> </table> <p style="text-align: center;">[GATE-EC -2007]</p> <p>(26) The contents of the accumulator just after execution of the ADD instruction in line 4 will be</p> <p>(A) C3H (B) EAH (C) DCH (D) 69H</p> <p style="text-align: center;">[GATE-EC -2007]</p> <p>(27) After execution of line 7 of the program, the status of the CY and Z flags will be</p> <p>(A) CY = 0, Z = 0 (B) CY = 0, Z = 1 (C) CY = 1, Z = 0 (D) CY = 1, Z = 1</p> <p style="text-align: center;">[GATE-EC -2013]</p> <p>(28) For 8085 microprocessor, the following program is executed</p> <pre>MVI A, 05H; MVI B, 05H PTR: ADD B; DCR B; JNZ PTR; ADI 03H; HLT;</pre> <p>At the end of program, accumulator contains</p> <p>(A) 17H (B) 20H (C) 23H (D) 05H</p> <p style="text-align: center;">[GATE-EC -2014]</p> <p>(29) An 8085 microprocessor executes “STA1234H” with starting address location 1FFEH (STA copies the contents of the Accumulator to the 16-bit address location). While the instruction is fetched and executed, the sequence of values written at the address pins A₁₅ – A₈ us</p>	(A) 3CFOH	(B) 3CF8H	(C) EFFDH	(D) EFFFH	Line	1: MVI A, B5H		2: MVI B, 0EH		3: XRI 69H		4: ADD B		5: ANI 9BH		6: CPI 9FH		7: STA 3010H		8: HLT
6010	LXI H, 8A79H																																
6013	MOV A, H																																
6014	ADD H																																
6015	DAA																																
6016	MOV H, A																																
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	4: ADD B																																
	5: ANI 9BH																																
	6: CPI 9FH																																
	7: STA 3010H																																
	8: HLT																																

(A) 1FH, 1FH, 20H, 12H

(B) 1FH, FEH, 1FH, FFH, 12H

(C) 1FH, 1FH, 12H, 12H

(D) 1FH, 1FH, 12H, 20H, 12H

[GATE-EC -2015]

- (30) Which one of the following 8085 microprocessor programs correctly calculates the product of two 8-bit numbers stored in registers B and C?

(A) MVI A, 00 H
JNZ LOOP

CMP C

LOOP DCR B

HLT

(B) MVI, A, 00H
CMP C

LOOP DCR B

HLT

(C) MVI, A, 00H
LOOP ADD C

DCR B

JNZ LOOP

HLT

(D) MVI A, 00H
ADD C

LOOP INR B

HLT

[GATE-EC -1988]

- (31) In register index addressing mode is given by

(A) The index register value

(B) The sum of the index register value and the operand

(C) The operand

(D) The difference of the index register value and the operand.

[GATE-EC -1993]

- (32) In a microcomputer, wait states are used to

(A) Make the processor wait during a DMA operation

(B) Make the processor wait during an interrupt processing

(C) Make the processor wait during a power shut down

(D) Interface slow peripherals to the processor

[GATE-EC -1995]

- (33) An ‘Assembler’ for a microprocessor is used for

(A) assembly of processors in a production line.

(B) creation of new programmes using different modules.

(C) translation of program from assembly language to machine language.

(D) translation of higher level language into English text

[GATE-EC -1998]

- (34) An I/O processor controls the flow of information between

(A) cache memory and I/O devices

(B) main memory and I/O devices

(C) two I/O devices

(D) cache and main memories

[GATE-EC -1998]

- (35) An instruction used to set the carry Flag in a computer can be classified as

(A) data transfer

(B) arithmetic

(C) logical

(D) program control

[GATE-EC -2015]

- (36) In a 8085 microprocessor, the shift registers which store the result of an addition and the overflow bit are, respectively

(A) B and F

(B) A and F

(C) H and F

(D) A and C

[GATE-EC -1989]

- (37) In a microprocessor system, the stack is a used for

(A) storing the program return address whenever a sub-routine jump instruction is executed

(B) transmitting and receiving

(C) storing all important CPU register contents whenever an interrupts is to be

(D) storing program instructions for interrupt service routines.

[GATE-EC -1995]

- (38) When a CPU is interrupt, it

(A) stops execution of instruction

(B) acknowledges interrupt and continues

(C) acknowledge interrupt and continues

(D) acknowledges interrupt and awaits for the next instruction from the interrupting device.

[GATE-EC -2010]

- (47) For the 8085 assembly language program given below, the content of the accumulator after the execution of the program is :

```

3000 MVI A, 45
3002 MOV B, A
3003 STC
3004 CMC
3005 RAR
3006 XRA B

```

- (A) 00H (B) 45H
 (C) 67H (D) E7H

[GATE-EC -2011]

- (48) An 8085 assembly language program is given below. Assume that the carry flag is initially unset. The content of the accumulator after the execution of the program is :

```

MVI A, 07H
RLC
MOV B, A
RLC
RLC
ADD B
RRC

```

- (A) 8CH (B) 64H
 (C) 23H (D) 15H

[GATE-EC -2015]

- (49) In an 8085 microprocessor, which one of the following instructions changes the content of the accumulator ?

- (A) MOV B, M (B) PCHL
 (C) RNZ (D) SBI BEH

[GATE-EE-2010]

- (50) When a "CALL Addr" instruction is executed, the CPU carries out the following sequential operations internally:

Note :

(R) means content of register R

((R)) means content of memory location pointed to by R

PC means Program Counter

SP means Stack Pointer

(A) (SP) incremented

(PC) ← Addr

((SP)) ← (PC)

(B) (PC) ← Addr

((SP)) ← (PC)

(SP) incremented

(C) (PC) ← Addr

(SP) incremented

((SP)) ← (PC)

(D) ((SP)) ← (PC)

(SP) incremented

(PC) ← Addr

[GATE-EE-2011]

- (51) A portion of the main program to call a subroutine SUB in an 8085 environment is given below :

```

:
LXI D, DISP
LP : CALL SUB
:
:
```

It is desired that control be returned to LP + DISP + 3 when the RET instruction is executed in the subroutine. The set of instructions that precede the RET instruction in the subroutine are

- (A) POP D (B) POP H

 DAD H DAD D

 PUSH D INX H

 INX H

 PUSH H

- (C) POP H (D) XTHL

 DAD D INX D

 PUSH H INX D

 INX D

 XTHL

[GATE-EE-2014]

- (52) In 8085 A microprocessor, the operation performed by the instruction LHLD 2100_H is

- (A) (H) ← 21_H, (L) ← 00_H

- (B) (H) ← M(2100_H), (L) ← M(2101_H)

- (C) (H) ← M(2101_H), (L) ← M(2100_H)

- (D) (H) ← 00_H, (L) ← 21_H

- [GATE-IN-1994]**

[GATE-IN-1994]

- (54) The program counter on a 8-bit microprocessor is always a 8-bit register.

Ans.: PC contains the address of next instruction to be fetched thus it is a 16-bit register.

[GATE-IN-1997]

- (55) The stack pointer in a microprocessor is a register containing

 - (A) the address of the next operand
 - (B) the current size of the stack
 - (C) the address of the top of the stack
 - (D) the address for storing the result of arithmetic operations

[GATE-IN-1998]

[GATE-IN-2000]

- (57) For an 8085 microprocessor, the Stack Pointer and Program Counter registers contain the number F000 and 2400 in Hex respectively. The contents of the register after execution of the instruction CALL E000 would be

(A) PC : F003	SP : 2400
(B) PC : 2400	SP : 2400
(C) PC : E000	SP : 2401
(D) PC : E000	SP : 23FE

[GATE-IN-2001]

- (58) An m-bit microprocessor has an m-bit

 - (A) flag register
 - (B) instruction register
 - (C) data counter
 - (D) program counter

[GATE-IN-2001]

- (59) In 8085 microprocessor , CY flag may be set by the instruction

B) INX

- (C) CMA (D) ANA

[GATE-IN-2001]

- (66) Microprocessor 8085 regains control of the bus

- (A) immediately after HOLD goes low
 - (B) immediately after HOLD goes high
 - (C) after half-clock cycle after HLDS goes low
 - (D) after half-clock cycle after HIDA goes high

[GATE-IN-2002]

- (61)** In an INTEL 8085 microprocessor the ADDRESS-DATA bus and the DATA bus are

 - (A) Non multiplexed
 - (B) Multiplexed
 - (C) Duplicated
 - (D) Same as CONTROL bus

[GATE-IN-2002]

- (62) In an 8085 based system the subroutine TEST given below is called by another program. When the processor returns from the subroutine TEST, the value in the accumulator will be

Test	MOV A, #00H
	CALL TEST
TEST	INR A
	RET
02	(B) 00
FF	(D) 20

[GATE-IN-2002]

- (63) Some of the pins of an 8085 CPU and their functions are listed below. Identify the correct answer that matches the pins to their respective functions.

Group-I

- P.** RST 7.5
 - Q.** H OLD
 - R.** IO/ \overline{M}
 - S.** ALE

Group-II

1. Selects I/O or memory
 2. Demultiplexes the address and data bus
 3. Is a vectored interrupt
 4. Facilitates direct memory access
 5. Is a clock
 6. Selects BCD mode of operation

(A) P-3, Q-2, R-1, S-4

(B) P-4, Q-1, R-5, S-3

(C) P-3, Q-4, R-1, S-2

(D) P-2, Q-3, R-6, S-1

[GATE-IN-2003]

- (64) In an 8085 system containing 8 KB of ROM and 8 KB of RAM, the ROM is selected when A_{15} is 0 and the RAM is selected when A_{15} is 1. A_{13} and A_{14} are unused. The CPU executes the following program

Prog 1 MVI A, 00H
 STA 8080H
 DCR A
 STA C080H
 RET

The content of memory location 8080H after the execution of the return instruction is

- (A) FFH (B) FEH
 (C) 01H (D) 00H

[GATE-IN-2004]

- (65) The vectored address corresponding to the software interrupt command RST7 in 8085 Microprocessor is

- (A) 0017H (B) 0027H
 (C) 0038H (D) 0700H

[GATE-IN-2004]

- (66) The following 8085 instructions are executed sequentially.

Prog : XRA A

MOV L, A
 MOV H, L
 INX H
 DAD H

After execution, the content of HL register pair is

- (A) 0000H (B) 0101H
 (C) 0001H (D) 0002H

[GATE-IN-2005]

- (67) The time period of a square wave in the audio frequency range is measured using an 8085 Microprocessor by feeding the square wave to one of the four interrupts, namely, RST 7.5, RST 6.5, RST 5.5, or INT. The algorithm used starts a timer at the beginning of a time period, stops the time at the beginning of the next time period and reads the time values for time measurement. Which of the following interrupts should be selected for this applications?

- (A) INTR (B) RST 5.5
 (C) RST 6.5 (D) RST 7.5

[GATE-IN-2005]

- (68) In an 8085 microprocessor, which one of the following is the correct sequence of the machine cycles for the execution of the DCR M instruction ?

- (A) op-code fetch
 (B) op-code fetch, memory read, memory write
 (C) op-code fetch, memory read
 (D) op-code fetch, memory write, memory write

[GATE-IN-2005]

- (69) A microprocessor has an instruction XOR (r_1, r_2), which perform an Exclusive OR operation of register r_1, r_2 and stores the result in r_1 . After the following instructions are executed

XOR	(r_2, r_1)
XOR	(r_1, r_2)
XOR	(r_2, r_1)

Which one of the following is true ?

- (A) Content of register r_1 is half sum of r_1 and r_2
 (B) Content of register r_2 is half sum of r_1 and r_2
 (C) Content of registers r_1 and r_2 unaltered
 (D) Contents of registers r_1 and r_2 are swapped

[GATE-IN-2005]

- (70) In a 8085 Microprocessor the value of the stack pointer (SP) is 2010H and that of DE register pair is 1234H before the following code is executed. The value of the DE register pair after the following code is executed is :

LXI H,	0000H
PUSH,	H
PUSH	H
POP B	
DAD	SP
XCGH	
(A) 200EH	(B) 200CH
(C) 2010H	(D) 1232H

[GATE-IN-2006]

- (71) A memory mapped I/O device has an address of 00F0H. Which of the following 8085 instructions output the content of the accumulator to the I/O device?

- (A) LXI, 00F0H
MOV M, A

(B) LXI H, 00F0H
OUT M

(C) LXI H, 00F0H
OUT F0H

(D) LXI H, 00F0H
MOV A, M

[GATE-IN-2006]

- (72) An 8085 assembly language program is given as follows. The execution time of each instruction is given against the instruction in terms of T-state.

Instruction	T-states
.....
MVI B, 0AH	7T
LOOP: MVI C, 05H	7T
DCR C	4T
DCR B	4T
JNZLOOP	10T/7T

The execution time of the program in terms of T-states is

- (A) 247 T (B) 250 T
(C) 254 T (D) 257 T

[GATE-IN-2007]

- (73) A snapshot of the address, data and control buses of an 8085 microprocessor executing a program is given below :

Address	2020H
Data	24H
IO/ M	Logic High
RD	Logic High
WR	Logic Low

The assembly language instruction being executed is :

- (A) IN 24H (B) IN 20H
(C) OUT 24H (D) OUT 20H

[GATE-IN-2007]

- (74) 8-bit signed integers in 2's complement form are read into the accumulator of an 8085 Microprocessor from an I/O port using the following assembly language program segment with symbolic addresses.

```
BEGIN:      IN PORT
          RAL
          JNC BEGIN
          RAR
END:        HLT
```

This program

- (A) halts upon reading a negative number
(B) halts upon reading a positive number
(C) halts upon reading a zero
(D) never halts

[GATE-IN-2008]

- (75) A part of a program written for an 8085 microprocessor is shown below. When the program execution reaches LOOP2, the value of register C will be

```
SUB A
C, A
LOOP 1 :    INR A
              DAA
              JC LOOP 2
              INR C
              JNC LOOP 1
LOOP 2:    NOP
(A) 63 H
(B) 64 H
(C) 99 H
(D) 100 H
```

[GATE-EE-2014]

- (76) In an 8085 microprocessor, the following program is executed.

Address location-instruction

2000 H	XRA A
2001 H	MVI B, 04 H
2003 H	MVI A, 03 H
2005 H	RAR
2006 H	DCR B
2007 H	JNZ 2005
200 AH	HLT

At the end of program, register A contains

- (A) 60 H (B) 30 H
(C) 06 H (D) 03 H

- (C) Ext INT1 → INT → INTA → Address write

- (D) Ext INT1 → INT → Data Read → Address write

[GATE-S4-EC-2016]

- (84) In an 8085 microprocessor, the contents of the accumulator and the carry flag are A7 (in hex) and 0, respectively. If the instruction RLC is executed, then the contents of the accumulator (in hex) and the carry flag, respectively, will be
- (A) 4E and 0 (B) 4E and 1
 (C) 4F and 0 (D) 4F and 1

[GATE-S3-EC-2016]

- (85) An 8 Kbyte ROM with an active low Chip Select input (\overline{CS}) is to be used in an 8085 microprocessor based system. The ROM should occupy the address range 1000H to 2FFFH. The address lines are designated as A_{15} to A_0 , where A_{15} is the most significant address bit.
- Which one of the following logic expressions will generate the correct (\overline{CS}) signal for this ROM ?

- (A) $A_{15} + A_{14} + (A_{13} \cdot A_{12} + \overline{A_{13}} \cdot \overline{A_{12}})$
 (B) $A_{15} \cdot A_{14} \cdot (A_{13} + A_{12})$
 (C) $\overline{A_{15}} + \overline{A_{14}} + (A_{13} \cdot \overline{A_{12}} + \overline{A_{13}} \cdot A_{12})$
 (D) $\overline{A_{15}} + \overline{A_{15}} + A_{13} \cdot A_{12}$

[GATE-S1-EC-2016]

- (86) In an 8085 system, a PUSH operation requires more clock cycles than a POP operation. Which one of the following options is the correct reason for this?
- (A) For POP, the data transceivers remain in the same direction as for instruction fetch (memory to processor), whereas for PUSH their direction has to be reversed.
 (B) Memory write operations are slower than memory read operations in an 8085 based system.
 (C) The stack pointer needs to be pre-decremented before writing registers in a PUSH, whereas a POP operation uses the address already in the stack pointer.
 (D) Order of registers has to be interchanged for a PUSH operation, whereas POP uses their natural order.

[GATE – IN – 2017]

- (87) An 8-bit microcontroller with 16 address lines has 3 fixed interrupts i.e. Int 1, In2 and Int3 with corresponding interrupt vector

addresses as 0008H, 0010H and 0018H. To execute a 32-byte long interrupt service subroutine for Int1 starting at the address ISS1, the location 0008H onwards should ideally contain

- (A) a CALL to ISS1
 (B) an unconditional JUMP to ISS1
 (C) a conditional JUMP to ISS1
 (D) Only ISS1

[GATE-S1-EC-2017]

- (88) The clock frequency of an 8085 microprocessor is 5 MHz. If the time required to execute an instruction is $1.4\ \mu s$, then the number of T-states needed for executing the instruction is
- (A) 1 (B) 6
 (C) 7 (D) 8

[GATE-S1-EC-2017]

- (89) The following FIVE instructions were executed on an 8085 microprocessor.

MVI A, 33 H
 MVI B, 78 H
 ADD B
 CMA
 ANI 32 H

The accumulator value immediately after the execution of the fifth instruction is

- (A) 00H (B) 10H
 (C) 11H (D) 32H

[GATE – IN – 2018]

- (90) A portion of an assembly language program written for an 8-bit microprocessor is given below along with explanations. The code is intended to introduce a software time delay. The processor is driven by a 5 MHz clock. The time delay (in μs) introduced by the program is_____.

MVI B, 64H ; Move immediate the given byte into register B. Takes 7 clock periods.

LOOP : DCR B ; Decrement register B. Affects Flags. Takes 4 clock periods.

JNZ LOOP ; Jump to address with Label LOOP if zero flag is not set. Takes 10 clock periods when jump is performed and 7 clock periods when jump is not performed.

-----0000-----

10

MEMORIES & INTERFACING

- [GATE-IN-1994]**

[GATE-IN-1999]

[GATE-IN-1999]

- (3) The important feature of a microcontroller is that it has on-chip

 - (A) math co-processor
 - (B) program memory
 - (C) interface for I/O devices
 - (D) hardware multiplier

[GATE-IN-2000]

- (4) Find the correct match among the following pair in the context of an 8085 microprocessor

 - A. DAA
 - B. LXI
 - C. RST
 - D. JMP
 - 1. Program control instruction
 - 2. Data movement Instruction
 - 3. Interrupt instruction
 - 4. Arithmetic instruction

Codes :

- (A)** (A) - (i), (B) - (ii), (C) - (iii), (D) - (iv)
(B) (A) - (iv), (B) - (ii), (C) - (iii), (D) - (i)
(C) (A) - (iv), (B) - (iii), (C) - (ii), (D) - (i)
(D) (A) - (ii), (B) - (iv), (C) - (iii), (D) - (i)

[GATE-IN-2001]

- (5) In a microprocessor with 16 address and 12 data lines, the maximum number of opcodes is :

(A) 2^6 (B) 2^8
 (C) 2^{12} (D) 2^{16}

[GATE-IN-2002]

- (6) A minimal microcomputer system is constructed using INTEL 8085 microprocessor, an 8156 RAM and an 8355 ROM. The chip enable CE of 8355 are connected to address line A_{12} of 8085 the address of port A of the 8156 chip is :

[GATE-EC -1988]

- (7) For a microprocessor system using I/O-mapped the following statement(s) is NOT true

 - (A) Memory space available is greater
 - (B) Not all data transfer instruction are available
 - (C) I/O and Memory address spaces are distinct
 - (D) I/O address space is greater

[GATE-EC -2004]

- (8) The 8255 Programmable Peripheral Interface is used as described below

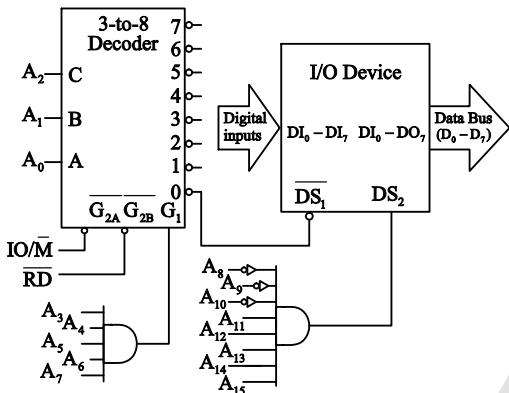
 - (I) An A/D converter is interfaced to a microprocessor through an 8255. The conversion is initiated by a signal from the 8255 on Port C. A signal on Port C causes data to be strobed into Port A
 - (II) Two computers exchange data using a pair of 8255s. Port A works as a bidirectional data port supported by appropriate handshaking signals/

The appropriate modes of operation of the 8255 for (I) and (II) would be

- (A) Mode 0 for (I) and Mode 1 for (II)
- (B) Mode 1 for (I) and Mode 0 for (II)
- (C) Mode 2 for (I) and Mode 0 for (II)
- (D) Mode 2 for (I) and Mode 1 for (II)

[GATE-EC -2014]

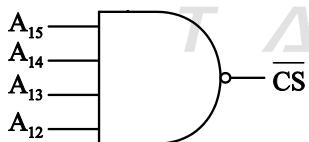
- (9) For the 8085 microprocessor, the interfacing circuit to input 8-bit digital data ($DI_0 - DI_7$) from an external device is shown in the figure. The instruction for correct data transfer is



- (A) MVI A, F8H
- (B) IN F8H
- (C) OUT F8H
- (D) LDA F8F8H

[GATE-EE-2002]

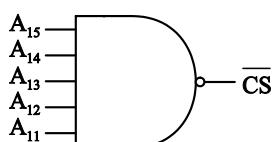
- (10) The logic circuit used to generate the active low chip select (CS) by an 8085 microprocessor to address a peripheral is shown in figure. The peripheral will respond to addresses in the figure.



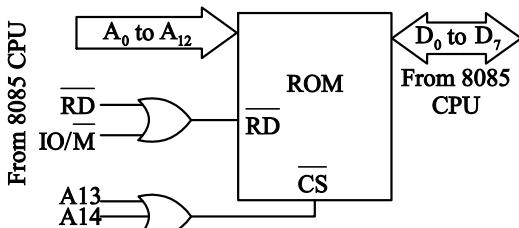
- (A) E000-EFFF
- (B) 000E-FFFE
- (C) 1000-FFFF
- (D) 0001-FFF1

[GATE-EE-1997]

- (11) The range of addresses for which the memory chip shown in figure, will be selected is to



- [GATE-IN-2003]**
(12) A ROM is interfaced to an 8085 CPU as indicated in figure. The address range occupied by the ROM is



- (A) 0000 - 0FFF
- (B) 0000 - 1FFF
- (C) 0000 - 2FFF
- (D) 8000 - 9FFF

[GATE-IN-2005]

- (13) An 8-bit microcontroller has an external RAM is the memory map from 8000H to 9FFFH. The number of bytes this RAM can store is

- | | |
|----------|----------|
| (A) 8193 | (B) 8191 |
| (C) 8192 | (D) 8000 |

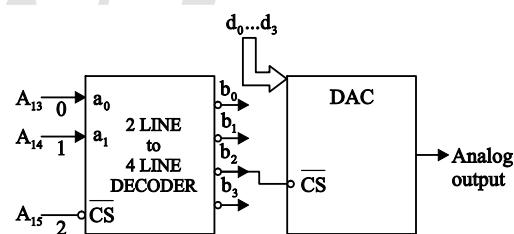
[GATE-IN-2008]

- (14) A $2K \times 8$ bit RAM is interfaced to an 8-bit microprocessor. If the address of the memory location in the RAM is 0800H, the address of the last memory location will be

- | | |
|------------|-----------|
| (A) 1000 H | (B) 0FFFH |
| (C) 4800H | (D) 47FFH |

[GATE-IN-2010]

- (15) An 8-bit DAC is interfaced with a microprocessor having 16 address lines ($A_0 \dots A_{15}$) as shown in the adjoining figure. A possible valid address for this DAC is :



- | | |
|-----------|-----------|
| (A) 3000H | (B) 4FFFH |
| (C) AFFFH | (D) C000H |

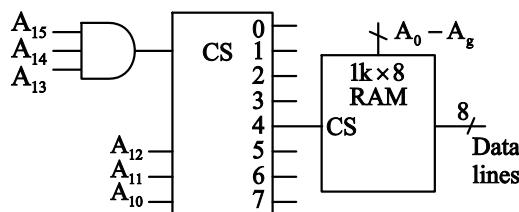
[GATE-IN-2011]

- (16) An $8K \times 8$ bit RAM is interfaced to an 8085 microprocessor. In a fully decoded scheme if the address of the last memory location of this RAM is 4FFFH, the address of the first memory location of the RAM will be

- | | |
|------------|------------|
| (A) 1000 H | (B) 2000 H |
| (C) 3000 H | (D) 4000 H |

[GATE-EC -1988]

- (17) A 8-bit microprocessor has 16-bit address bus $A_0 - A_{15}$. The processor has a 1 kB Byte memory chip as shown. The address range for the chip is



- (A) F00FH TO F40EH
- (B) F100 TO F4FFH
- (C) F000H TO F3FFH
- (D) F700H TO FAFFH

[GATE-EC -1988]

- (18) A microprocessor with a 16-bit address bus is used in a linear memory selection configuration(i.e. Address bus lines are directly used as chip selects of memory chips) with 4 memory chips. The maximum addressable memory space is

- (A) 64 k
- (B) 16 k
- (C) 8 k
- (D) 4 k

[GATE-EC -1992]

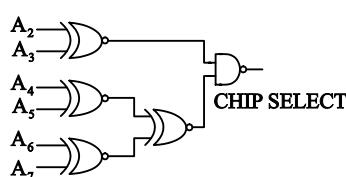
- (19) In an 8085 microprocessor system with memory mapped I/O,

- (A) I/O devices have 16-bit address
- (B) I/O devices are accessed using IN and OUT instructions.
- (C) there can be a maximum of 256 input devices and 256 output devices
- (D) arithmetic and logic operations can be directly performed with the I/O data.

[GATE-EC -1997]

- (20) The decoding circuit shown in Fig. has been used to generate the active low chip select signal for a microprocessor peripheral.(The address lines are designated as A_0 to A_7 for I – O addresses)

The peripheral will correspond to IO address in the range



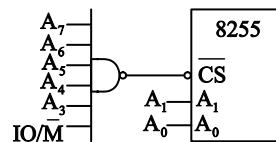
- (A) 60 H to 63 H
- (B) A4 H to A7 H

- (C) 50 H to AF H

- (D) 70 H to 73 H

[GATE-EC -2007]

- (21) An 8255 chip is interfaced to an 8085 microprocessor system as an I/O mapped I/O as shown in the figure. The address lines A_0 and A_1 of the 8085 are used by the 8255 chip to decode internally its three ports and the Control register. The address lines A_3 to A_7 as well as the IO / M signal are used for address decoding. The range of address for which the 8255 chip would get selected is



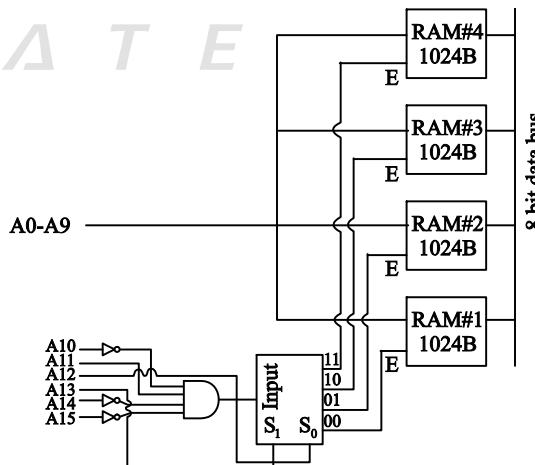
- (A) F8H - FBH
- (B) F8H - FCH
- (C) F8H – FFH
- (D) F0H – F7H

[GATE-EC-2015]

- (22) A 16 kB ($=16,384$ bit) memory array is designed as a square with an aspect ratio of one (number of rows is equal to the number of columns). The minimum number of address lines needed for the row decoder is _____.

[GATE-EC-2013]

- (23) There are four chips each of 1024 bytes connected to a 16 big address bus as shown in the figure below. RAMs 1, 2, 3 and 4 respectively are mapped to address



- (A) 0C00H-0FFFH, 1C00H-1FFFH, 2C00H-2FFFH, 3C00H-3FFFH

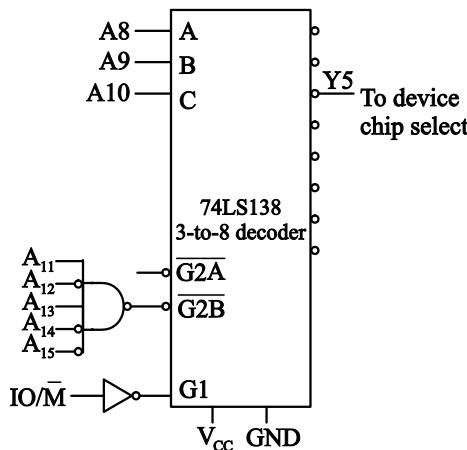
- (B) 1800H-1FFFH, 2800H-2FFFH, 3800H-3FFFH, 4800H-4FFFH

(C) 0500H-08FFH, 1500H-18FFH, 3500H-38FFH, 5500H-58FFH

(D) 0800H-0BFFH, 1800H-1BFFH, 2800H-2BFFH, 3800H-3BFFH

[GATE-EC -2010]

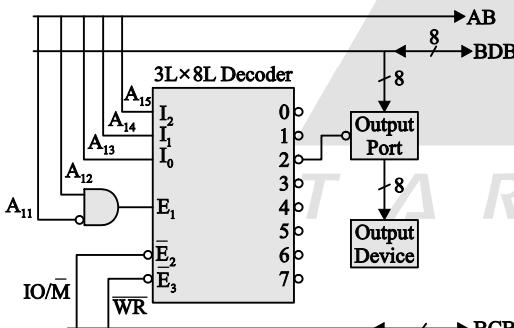
- (24) In the circuit shown, the device connected to Y5 can have address in the range



- (A) 2000 – 20 FF
 (B) 2D00 – 2DFF
 (C) 2E00 – 2EFF
 (D) FD00 – FDFF

[GATE-EE-2014]

- (25) An output device is interfaced with 8-bit microprocessor 8085 A. The interfacing circuit is shown in figure.



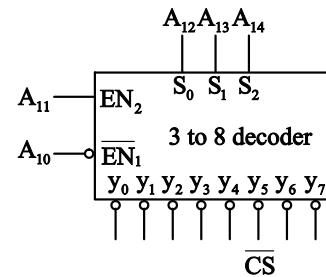
The interfacing circuit makes use of 3 Line to 8 Line decoder having 3 enable lines $E_1, \bar{E}_2, \bar{E}_3$. The address of the device is

- (A) 50H (B) 5000H
 (C) A0H (D) A000H

[GATE-IN-2016]

- (26) A 1 Kbyte memory module has to be interfaced with an 8-bit microprocessor that has 16 address lines. The address lines A₀ to A₉ of the processor are connected to the corresponding address lines of the memory module. The active low chip select CS of the memory module is connected to the y₅

output of a 3 to 8 decoder with active low outputs. S₀, S₁, and S₂ are the input lines to the decoder, with S₂ as the MSB. The decoder has one active low \bar{EN}_1 and one active high EN₂ enable lines as shown below. The address range(s) that gets mapped onto this memory module is (are)



- (A) 3000_H to 33FF_H and E000_H to E3FF_H
 (B) 1400_H to 17FF_H
 (C) 5300_H to 53FF_H and A300_H to A3FF_H
 (D) 5800_H to 5BFF_H and D800_H to DBFF_H

[GATE-IN-2019]

- (27) In a microprocessor with a 16 bit address bus, the most significant address lines A₁₅ to A₁₂ are used to select a 4096 word memory unit, while lines A₀ to A₁₁ are used to address a particular word in the memory unit. If the 3 least significant lines of the address bus A₀ to A₂ are short-circuited to ground, the addressable number of words in the memory unit is _____.

-----0000-----

Answers :

01 - NUMBER SYSTEM

1.1 (R)'S AND (R-1)'S COMPLIMENT

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
B	C	A	D	B	A	C	D	D	C	D	A	A	D	C	C
17.	18.	19.	20.	21.	22.	23.	24.								
A	C	B	C	C	B	B	C								

1.2 Miscellaneous

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
D	D	A	D	*	C	C	B	A	D	D	B	D	B	D	B
17.	18.	19.	20.	21.	22.	23.	24.	25.	26.	27.	28.	29.	30.	31.	32.
B	A	B	C	A	B	A	B	B	B	C	D	D	B	C	A
33.	34.	35.	36.	37.	38.	39.	40.	41.	42.	43.	44.	45.	46.	47.	48.
D	A	B	B	C	B	D	C	D	D	D	A	C	C	B	C
49.	50.	51.													
B	D	B													

5. 3.9-4.1

02 - BOOLEAN ALGEBRA

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
D	D	B	*	D	A	B	D	B	D	D	B	C	A	A	D
17.	18.	19.	20.	21.	22.	23.	24.	25.	26.	27.	28.	29.	30.	31.	32.
D	B	A	A	A	A	D	A	A	A	B	A	A	C	B	D
33.	34.	35.	36.	37.	38.	39.	40.	41.	42.	43.	44.	45.	46.	47.	48.
C	D	D	C	C	D	B	C	C	C	B	A	C	C	A	D
49.	50.	51.	52.	53.	54.	55.	56.	57.	58.	59.	60.	61.	62.	63.	64.
D	C	C	C	B	A	C	B	D	D	A	D	B	B	A	A
65.	66.	67.	68.	69.	70.	71.	72.	73.	74.	75.	76.	77.	78.	79.	80.
C	D	C	D	D	C	A	D	D	B	C	A	A,B	A	A	C
81.	82.	83.	84.	85.	86.	87.	88.	89.	90.	91.	92.	93.	94.	95.	96.
B	C	A	C	C	D	C	B	D	B	B	B	A	D	C	B
97.	98.	99.	100.	101.	102.	103.	104.	105.	106.	107.	108.	109.	110.	111.	112.
A	D	B	A	A	D	D	D	C	A	C	A	B	A	D	B
113.	114.	115.	116.	117.	118.	119.	120.	121.	122.	123.	124.	125.	126.	127.	
A	B	D	D	A	B	B	A	B	D	C	B	B	B	256	

4. TRUE

03 - LOGIC GATES

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
B,D	*	A	B	A	A	C	A	C	A	A	D	C	*	B	A
17.	18.	19.	20.	21.	22.	23.	24.	25.	26.	27.	28.	29.	30.	31.	32.
D	B	C	B	B	A	A	D	D	D	A	A	A	B	A	D
33.	34.	35.	36.	37.	38.	39.	40.	41.	42.	43.	44.	45.	46.	47.	48.
B	B	A	C	D	A	D	C	A	A	C	C	B	A	A	D
49.	50.	51.	52.	53.	54.	55.	56.	57.	58.	59.	60.	61.	62.	63.	64.
B	B	A	B	B	D	D	B	D	C	D	B,C	C	B	D	B
65.	66.	67.	68.	69.	70.	71.	72.	73.	74.	75.	76.	77.	78.	79.	80.
B,D	B	100	A	B	B	D	D	B	C	B	A	B	A	40	D
81.	82.	83.	84.	85.	86.	87.	88.	89.	90.	91.	92.	93.	94.	95.	96.
C	C	D	C	A	D	C	C	B	D	A	D	D	A	D	D
97.	98.	99.	100.	101.	102.	103.	104.	105.	106.	107.	108.	109.	110.	111.	112.
D	B	A	A	D	C	A	C	C	A	D	C	B	C	C	C
113.	114.	115.	116.												
8	D	A	A												

2. A-ii,B-iv,C-iii,D-i

14. $\overline{AC} + \overline{AB} + \overline{BA}$

70. 100nsec

84. 40

04 – COMBINATIONAL DIGITAL CIRCUITS**4.1 – Multiplexer**

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
D	D	C	A	C	B	B	C	A	A	D	B	C	A	C	B
17.	18.	19.	20.	21.	22.	23.	24.	25.	26.	27.	28.	29.	30.	31.	32.
C	C	C	C	A	*	A	C	A	A	A	B	B	D	B	A
33.	34.	35.	36.	37.	38.	39.	40.	41.	42.	43.	44.	45.	46.	47.	48.
A	B	C	B	C	D	B	B	C	D	D	C	A	*	D	A
49.	50	51													
B	B	C													

46. 6.0

4.2 – Adder

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
B	C	D	B	C	A	B	C	A	C	C	A	B	C	D	B
17.	18.	19.	20.	21.	22.	23.	24.	25.							
C	B	B	A	C	C	D	50	4							

4.3 – Decoder

1.	2.	3.	4.	5.	6.	7.	8.								
D	B	B	A	D	C	A	MTA								

4.4 – Miscellaneous

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
C	A	C	C	*	C	A	A	A	A	D	D	A	B	B	
17.	18.	19.	20.	21.											
B	D	C	A	B											

05 – SEQUENTIAL DIGITAL CIRCUITS

5.1 – Counter

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
D	*	A	C	D	D	*	*	C	A	D	6	B	C	A	C
17.	18.	19.	20.	21.	22.	23.	24.	25.	26.	27.	28.	29.	30.	31.	32.
B,D	D	B	C	A	C	D	C	C	A	C	C	A	A	D	D
33.	34.	35.	36.	37.	38.	39.	40.	41.	42.	43.	44.	45.	46.	47.	48.
A	B	A	B	A	C	B	A	A	C	D	C	C	B	B	D
49.	50.	51.	52.	53.	54.	55.	56.	57.	58.	59.	60.	61.	62.	63.	64.
C	B	C	A	A	D	A	D	C	C	D	D	B	B	B	A
65.	66.	67.	68.	69.	70.	71.	72.	73.	74.	75.	76.	77.	78.	79.	80.
B	D	A	B	A	A,B	A	D	C,D	C	C	C	A	B	B	A
81.	82.	83.	84.	85.	86.	87.	88.	89.	90.	91.	92.	93.	94.	95.	96.
C	B	C	A	B	B	D	D	A	C	C	D	A	B	C	D
97.	98.	99.	100.	101.	102.	103.	104.	105.	106.	107.	108.	109.	110.	111.	
C	A	C	C	*	A	D	B	C	D	B	10	C	4	D	

2. 62 - 63

7. 194.9to195.1

8. 6

5.2 – Miscellaneous

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
A	D	B	B	B	B	D	C	A	D	D	C	B	B	A	A
17.	18.	19.	20.	21.	22.	23.	24.	25.	26.	27.	28.	29.	30.	31.	32.
D	D	A	B	B	A	C	A	D	B	C	A	B	C	C	D
33.	34.	35.	36.	37.	38.	39.	40.	41.	42.	43.	44.	45.	46.	47.	48.
D	A	B	B	C	D	A,B	A	B	C	B	D	D	D	B	C
49.	50.	51.	52.	53.	54.	55.	56.	57.	58.	59.	60.	61.	62.	63.	64.
A	B	A	C	B	C	B	B	A	C	*	D	C	D	A	D

65.	66.	67.	68.	69.	70.	71.	72.	73.	74.	75.	76.	77.	78.	79.	80.
B	B	A	A	B	B	A	A	C	B	C	D	0.5	D	B	C
81.	82.	83.	84.	85.	86.	87.	88.	89.	90.	91.	92.	93.	94.	95.	96.
C	C	0,1	D	*	B	*	C	C	C	B	A	B	C	*	C
97.	98.	99.	100.	101.	102.	103.	104.	105.	106.						
B	6	4	10	B	*	*	5	D	A						

48. TRUE

59. Faster

92. 0.5

95. 1.45-1.55

102. 29.9-30.1

103. 0.82-0.86

06 – SEMICONDUCTOR MEMORIES

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
B	D	C	B	C	*	C	B	C	C	C	C,D	A	A	D	D
17.	18.	19.	20.	21.	22.	23.	24.	25.	26.	27.	28.	29.	30.	31.	32.
B	C	B	A	B	A	D	A	D	D	C	C	B	D	A,D	C
33.	34.	35.	36.	37.	38.	39.	40.	41.	42.	43.					
D	C	B	C	A	C	B	D	B	A	B					

6. None

07 – LOGIC GATE FAMILIES

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
A	B	D	B	B	A	D	D	C	A	D	*	*	C	C	C
17.	18.	19.	20.	21.	22.	23.	24.	25.	26.	27.	28.	29.	30.	31.	32.
A	A	*	A	A	*	D	B	*	C	B	B	B	D	D	D
33.	34.	35.	36.	37.	38.	39.	40.	41.	42.	43.	44.	45.	46.	47.	48.
D	D	A	A	B	C	C	C	D	B	A	B	B	B	A	A
49.	50.	51.	52.	53.	54.	55.	56.	57.	58.	59.	60.	61.	62.	63.	64.
C	B	C	C	A	B	A	C	D	A	A	A	C	A	*	D
65.	66.	67.	68.	69.	70.	71.	72.	73.	74.	75.	76.	77.	78.	79.	80.
B	C	C	D	A	C	C	B	B	B	B	B	B	B	B	D
81.	82.	83.	84.	85.	86.	87.	88.	89.	90.	91.	92.	93.	94.	95.	96.
A	B	A	B	A	D	B	A	A	D	A	C	C	A	*	A
97.	98.	99.	100.	101.	102.	103.	104.	105.	106.	107.	108.	109.	110.	111.	112.
B	B	B	A	A	A	C	C	D	B	D	A	MTA	D	A	A
113.															
A															

19. A-Q, B-R, C-S

22. 0.62-0.66

63. $A + BC$

95. A : 74LS B: CMOS

08 – A/D & D/A CONVERTERS

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
C	C	B	C	B	A	A	A	B	D	B	C	B	B	A	B
17.	18.	19.	20.	21.	22.	23.	24.	25.	26.	27.	28.	29.	30.	31.	32.
B	C	B	A	B	C	C	C	D	A	A	C	B	D	D	A
33.	34.	35.	36.	37.	38.	39.	40.	41.	42.	43.	44.	45.	46.	47.	48.
A	A	B	A	B	A	B	B	C	D	B	B	C	B	C	D
49.	50.	51.	52.	53.	54.	55.	56.	57.	58.	59.	60.	61.	62.	63.	64.
C	A	C	D	B	C	A	B	C	C	*	B	B	C	B	B
65.	66.	67.	68.	69.	70.	71.	72.	73.	74.	75.	76.	77.	78.	79.	80.
B	C	B	C	C	D	D	*	C	B	A	A	A	A	D	B
81.	82.	83.	84.	85.	86.	87.	88.	89.	90.	91.	92.	93.	94.	95.	
B	D	C	D	A	B	A	C	C	B	A	A	C	D	64	

59. A-4,B-3,C-2

72. 0.097

09 – MICROPROCESSOR 8085 PROGRAMMING & BASICS

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
C	C	A	D	B	B	*	C	C	B	C	D	*	C	D	C
17.	18.	19.	20.	21.	22.	23.	24.	25.	26.	27.	28.	29.	30.	31.	32.
D	A	B	D	*	C	D	B	B	B	C	A	A	C	A	D
33.	34.	35.	36.	37.	38.	39.	40.	41.	42.	43.	44.	45.	46.	47.	48.
C	B	C	B	A	D	D	A	A	B	C	D	C	C	C	C
49.	50.	51.	52.	53.	54.	55.	56.	57.	58.	59.	60.	61.	62.	63.	64.
D	D	C	C	*	#	C	B	C	C	A	B	B	*	C	D
65.	66.	67.	68.	69.	70.	71.	72.	73.	74.	75.	76.	77.	78.	79.	80.
C	D	A	B	D	A	A	C	D	A	A	A	A	D	B	D
81.	82.	83.	84.	85.	86.	87.	88.	89.	90.						
B	C	B	D	A	C	*	C	B	*						

13. a-T, b-S, c-P

53. FALSE

87. A or B

90. 279-282

10 – MEMORIES & INTERFACING

1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.	12.	13.	14.	15.	16.
?	A	C	B	C	?	D	?	D	A	*	B	C	B	B	C
17.	18.	19.	20.	21.	22.	23.	24.	25.	26.	27.					
C	B	A,D	A	C	7	D	B	B	D	*					

11. F800 to FFFFH

27. 512

***** END OF THE BOOKLET *****

