Physical Design

Few Words Before We Start

- Note, the topics will be timely updated as per requirement, any feedback and suggestions are welcome

- The training material is/will be maintained by the people who have real time experience in the field of physical design from RTL to GDSII in the technologies node of 90nm, 65 nm, 45nm, 40nm, 32nm, 28nm, 22nm, 16nm, 14nm, 10nm and less.

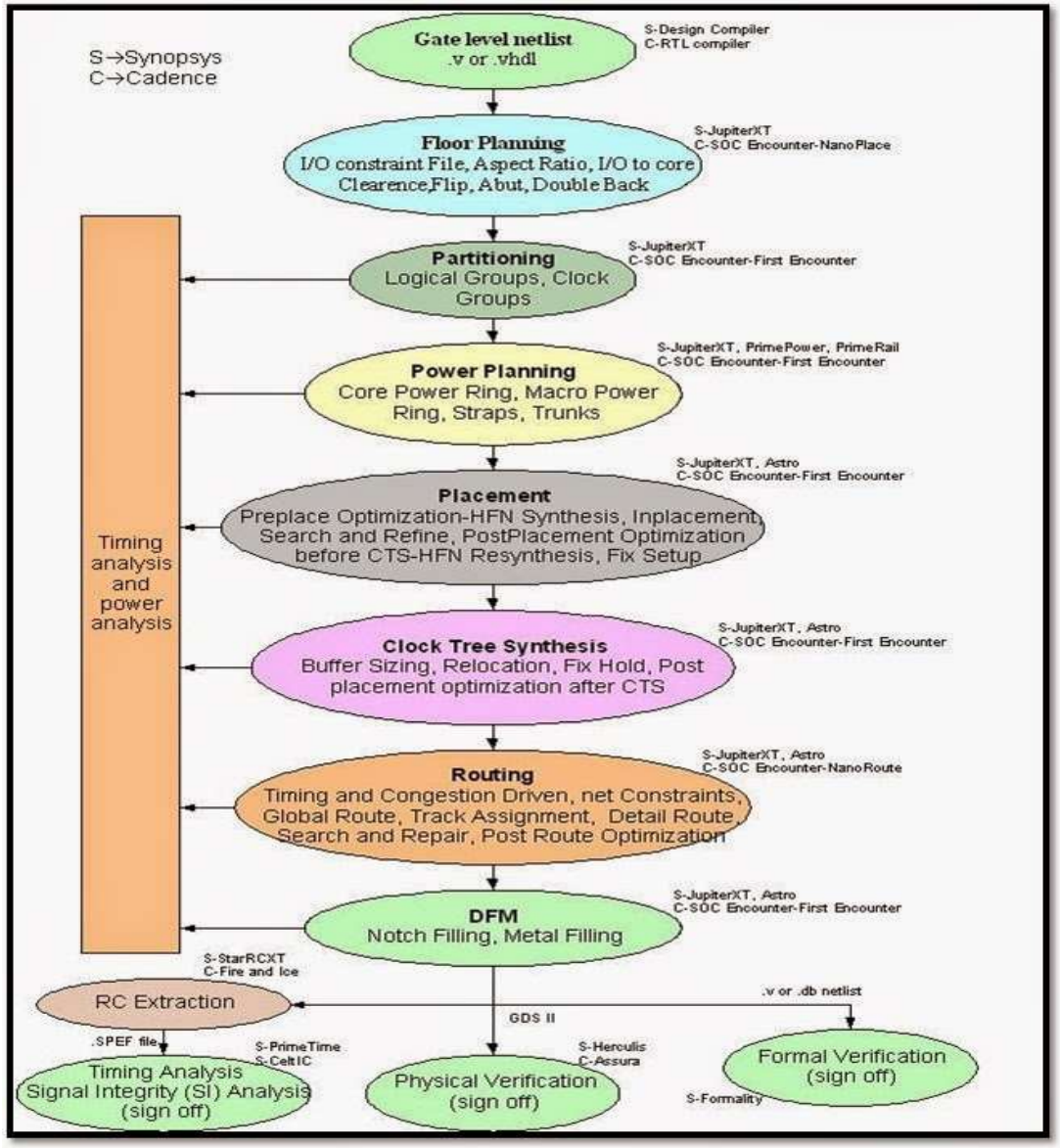
- Will discuss/share day to day challenges in real time work in the field of physical design.

- **Pre - Requisite :**
    - **A.** Digital & Analog Electronics Fundamentals
    - **B.** CMOS Fundamentals
    - **C.** Wafer Fabrication Technique
    - **D.** Basic Linux Commands

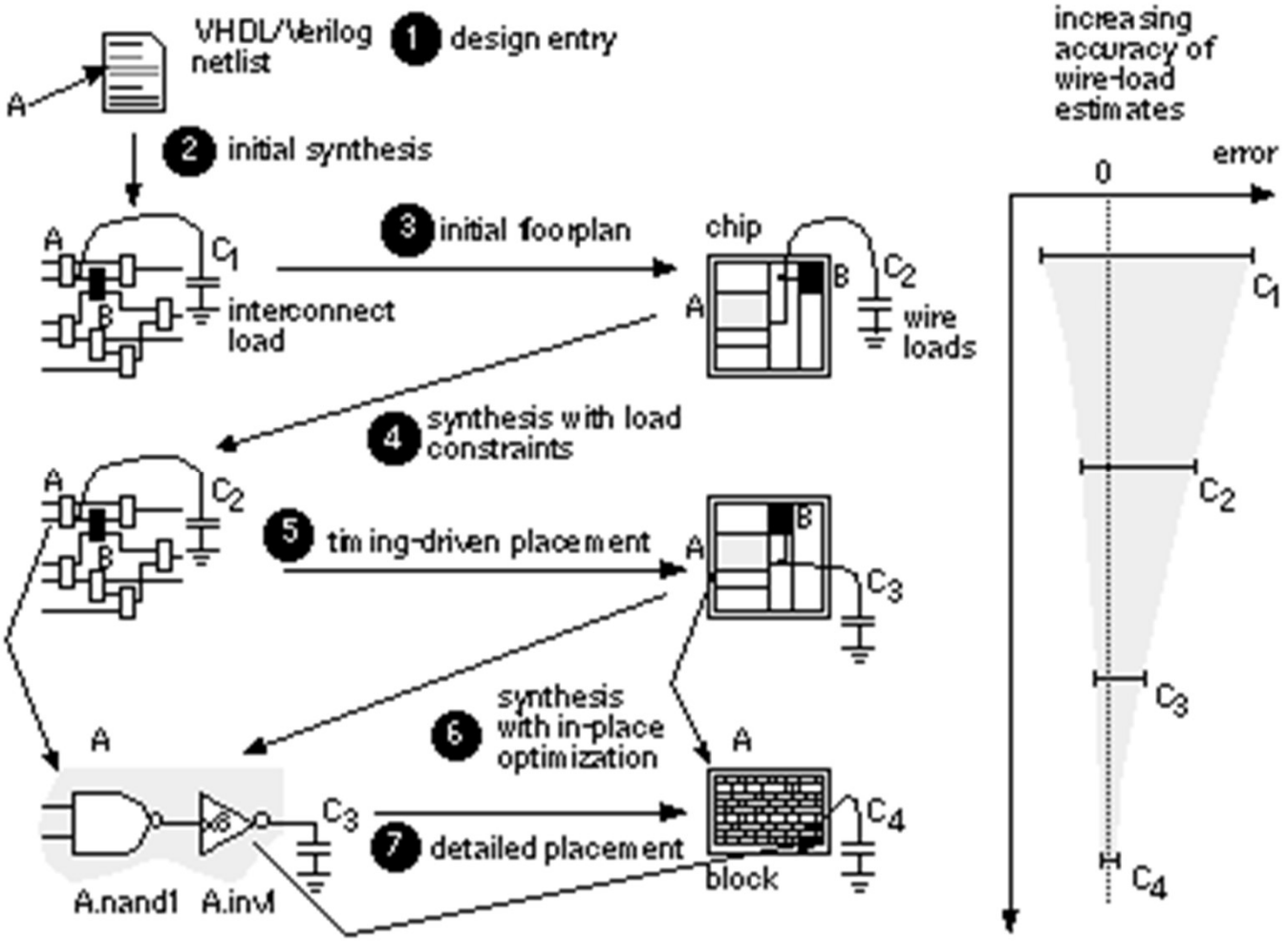
Topics To Be Covered

- Introduction to PD Flow
- PD Terminology
- Input Files
- Sanity Checks
- LPP (Low Power Planning)
- Floor Planning
- Power Planning
- Placement
- CTS
- Routing
- Signoff
  - STA PV + DFM IR Drop

Introduction to PD Flow



Introduction to PD Flow



PD Terminology

- PD
- Design*Cell
- Port*Pin*Net*Clock*Metal*Metal Layers* Node*Technology
- PnR*Floorplan*Place*CTS*PCO*Post CTS*CTS Opt*Route*PRO*Post Route
- Lib*Library*SDC*CN*Constraints*Cons
- Trans*Transition*Cap*Capacitance*Delay*MCP*Multi Cycle Path*False Path
- Skew*Latency*Uncertainty*Jitter
- Setup*Hold*Buffer*Inverter*Driving Strength*Delay Cell
- Sign off*PV*STA*PDN*Redhawk*IR*FV*CLP

Input Files

In Physical Design mainly Six inputs are present

1. Logical libraries	--> format is .lib	--> given by Vendors
2. physical libraries	--> format is .lef	--> given by vendors
3. Technology file	--> format is .tf	--> given by fabrication peoples
4. TLU+ file	--> format is .TLUP	--> given by fabrication people
5. Netlist	--> format is .v	--> given by Synthesis People
6. Synthesis Design Constraints	-->format is .SDC	--> given by Synthesis People

LOGICAL LIBRARIES

1. Timing information of Standard cells, Soft macros and Hard macros.
2. Functionality information of Standard cells, Soft macros and also Contain Power information.
3. Design rules like max transition ,max capacitance, max fanout, Cell delays, Setup, Hold time are present.
4. Cell delay is Function of input transition and output load and is calculated based on lookup tables.
5. Cell delays are calculated by using linear delay models, Non linear delay models, CCS models.
6. It contains Leakage power for Default cell, Leakage Power Density for cell, Default Input voltage, Output voltage and PVT contains

Input Files

PHYSICAL LIBRARIES

Physical libraries: format is .lef:

1. physical information of std cells, macros.
2. Pin information and hight of the placement Rows .
6. Preferred routing and routing Blockages

In physical info height, area, width are present and also it contains two views

1)Cell View:

In this all layout information is present, it is used at the time of tapeout

2)FRAM view:

FRAM view is abstract view, it is used at the Place & Route

TECHNOLOGY FILE

Technology file: format is .tf:

1. It contains Name, Number conventions of layer and via
2. It contains Physical, electrical characteristics of layer and via
3. In Physical characteristics Min width, area, height are present.
4. In Electrical characteristics Current Density is present.
5. Units, Precisions, Colors and pattern of layer and via .
6. Physical Design rules of layer and via
7. In Physical Design rules Wire to Wire Spacing, Min Width between Layer and via are present.

Input Files

TLU PLUS

TLU+ files: format is .TLUP:

1. R,C parasitic of metal per unit length.
2. These(R,C parasitic) are used for calculating Net Delays.
3. If TLU+ files are not given then these are getting from .ITF file.
4. For Loading TLU+ files we have load three files .
5. Those are Max TLU+,Min TLU+,MAP file.
6. MAP file maps the .ITF file and .tf file of the layer and via names.

NETLIST

Netlist: Format is .V

It contains Logical connectivity Of all Cell(Std cells,Macros).
It contain List of nets.
In the design for Knowing connectivity by using Fly lines.

Input Files

SDC

SDC :Format is .SDC :
These Constraints are timing Constraints and used for to meet timing requirements.
Constraints are

1. CLOCK DEFINITIONS: Create Clock Period.
2. Generated Clock Definitions
3. Input Delay
4. Output Delay
5. I/O delay
6. Max delay
7. Min Delay
8. ---------->Exceptions<----------
9. Multi cycle path
10. False path
11. Half cycle path
12. Disable timing arcs
13. Case Analysis

Multi cycle path, False path are Exceptions.

Sanity Checks

- These must be performed to get best TAT (Turn Around Time).
- Sanity checks to be performed on Inputs and Outputs both.
- Sanity check on Inputs will make sure TAT will be best.
- Sanity check on Outputs will make sure task performed correctly.
- Sanity check has to be performed for each and every stage.
- Sanity check on every stage is more important as run time is more.
- Ex. If anything goes wrong in floorplan and we came to know at sign-off stage then it will cost minimum 10 days of rework.

LPP (Low Power Planning)

- LPP is related to multi low voltage.
- It will help to execute design with intercommunication in multi low voltage modules.
- UPF (Unified Power Format) is used for all the PnR activity. This is designed by Synopsys, Mentor Graphics and Magma.
- CPF (Common Power Format) is used by FE (First Encounter) tool by Cadence.
- We will discuss it through out in design. More details will be discussed in Floorplan stage.

Floor Planning

- Introduction
- Inputs Required & Sanity Check
- Aspect Ratio, Core Utilization, Die Area calculation
- Macro Placement Tips & Rules
- IO Placement / Pin placement
- Types of Blockages
- Physical Cells
- Brief on Power Planning
- Do’s and Don’ts of Floor Plan
- Sanity Check & Floor Plan Sign-off
- Time to share

Introduction to floorplanning

- The first step in the Physical Design flow is Floor Planning.
- Floorplanning is the process of identifying structures that should be placed close together, and allocating space for them to meet the required performance.
- Based on the area of the design and the hierarchy, a suitable floorplan is decided upon. Floor Planning takes into account the macro's used in the design, memory, other IP cores and their placement needs, the routing possibilities and also the area of the entire design.
- Floor planning also decides the IO structure, aspect ratio of the design.
- A bad floor-plan will lead to waste-age of die area and routing congestion.

Inputs Required and Sanity Check

- Synthesized Netlist (.v, .vhdl)
- Logical and Physical Libraries
- TLU+ Files
- Physical partitioning information of the design
- Design Constrains (SDC)
- Physical information of your design (rules for targeted technology)
- Floorplan parameters like height, width, utilization, aspect ratio etc.
- Pin/pad Position

Aspect Ratio

The Role of Aspect Ratio on the Design:

- The aspect ratio effects the routing resources available in the design
- The aspect ratio effects the congestion
- The floor planning need to be done depend on the aspect ratio
- The placement of the standard cells also effect due to aspect ratio
- The timing and there by the frequency of the chip also effects due to aspect ratio
- The clock tree build on the chip also effect due to aspect ratio
- The placement of the IO pads on the IO area also effects due to aspect ratio

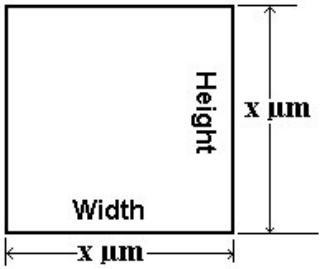


Fig.1: Aspect Ratio = 1.0

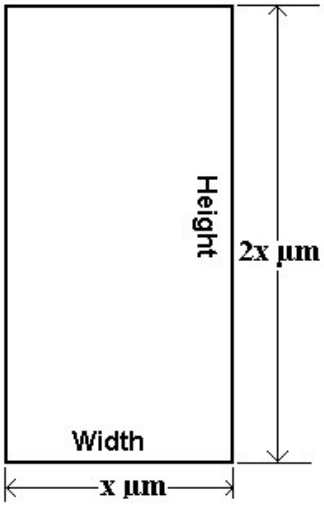


Fig.2: Aspect Ratio = 2.0

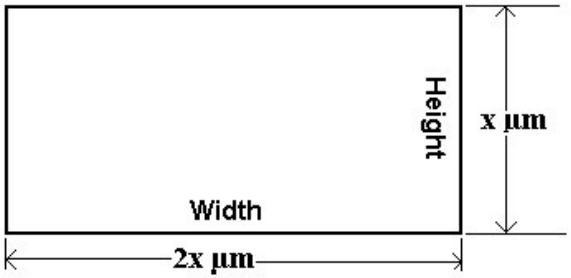


Fig.3: Aspect Ratio = 0.5

$$\text{Aspect Ratio} = \frac{\text{Height of the Core}}{\text{Width of the Core}}$$

Core Utilization, Die Area calculation

- **Core Utilization**
- **Utilization:** Utilization defines the area occupied by standard cell, macros and blockages. In general 70 to 80% of utilization is fixed because more number of inverters and buffers will be added during the process of CTS (Clock Tree Synthesis) in order to maintain minimum skew.

- **Core utilization = (standard cell area+ macro cells area)/ total core area**
- A core utilization of 0.8 means that 80% of the area is available for placement of cells, whereas 20% is left free for routing.

- **Methods to estimate die area**

  Method 1:
  Each cell has got its area according to a specific library. Go through all your cells and multiply each cell in its corresponding area from your vendor's library. Then you can take some density factor - usually for a standard design you should have around 80% density after placement. So from this data you can estimate your required die area.

  Method 2:
  One more way of doing it is, Load the design in the implementation tool, try to change the floorplan (x & y coordinates) in a such a way that the Starting utilization will be around 50% -to- 60%. Again, it depends on the netlist quality & netlist completion status (like Netlist is 75%, 80% & 90% completed).

Macro Placement Tips & Rules

- Once you have the size & shape of the floorplan ready and initialized the floorplan, thereby creating standard cell rows, you are now ready to hand place your macros.
- Do not use any auto placement, I have not seen anything that works.
- Flylines in your tool will show you the connection between the macros and standard cells or IOs.
- Use flylines and make sure you place blocks that connects to each other closer
- For a full-chip, if hard macros connect to IOs, place them near the respective IOs
- Consider the power straps while placing macros. You can club macros/memories
- Creating Power Rings and Straps
- Avoided the placement of macros in front of ports.
- Arranged the macros to get contiguous core area.
- Macro spacing given by space={[(no. of pins) * pitch] + space} / (no of metal layers in horizontal or vertical direction)

1. Place macros around chip periphery.
Placing a macro inside the core can invite serious consequence during routing due to a lot of detour routing, because macros are equal to a large obstacle for routing. Another advantage to placing the hard macros around the core periphery is it's easier to supply power to them, and reduces the change of IR drop problems to macros consuming high amounts of power.
2. Consider connections to fixed cells when placing macros.
Place macros near their associate fixed element. Check connections by displaying flight lines in the GUI.
3. Orient macros to minimize distance between pins.
When you decide the orientation of macros, you also have to take account of pins positions and their connections.
4. Reserve enough room around macros.
For regular net routing and power grid, you have to reserve enough routing space around macros. In this case estimating routing resources with precision is very important. Use the congestion map from trialRoute to identify hot spots between macros and adjust their placement as needed.
5. Reduce open fields as much as possible.
Except for reserved routing resources, remove dead space to increase the area for random logic. Choosing different aspect ratio (if that option is available) can eliminate open fields.
6. Reserve space for power grid.
The number of power routes required can change based on power consumption. You have to estimate the power consumption and reserve enough room for the power grid. If you underestimate the space required for power routing, you can encounter routing problems.

Blockages

- Placement blockages prevent the placement engine from placing cells at specific locations.
- Routing blockages block routing resources on one or more layers and it can be created at any point in a design flow.
- In general placement blockages are created at floor planning stage and routing blockages are created before using any routers. It acts like guidelines for placement of standard cells.
- Blockages will not be guiding the tool to place the standard cells at some particular area, but it won't allow the tool to place the standard cell in the blocked areas (in both placement and routing blockages).
- During the CTS process (Clock Tree Synthesis) in order to balance the skew, more number of buffers and inverters are added and blockages are used to reserve space for buffers and inverters.

Placement blockages
Use placement blockages to:
•Define std-cells and macro area
•Reserve channels for buffer insertion
•Prevent cells from being placed at or near macros
•Prevent congestion near macros

Soft (Non buffer blockage)
Only buffers can be placed and standard cells cannot be placed.

Hard (Std-cell blockage)
Blocks all std-cells and buffers to be placed. Std-cell blockages are mostly used to:
•Avoid routing congestion at macro corners
•Restrict std-cells to certain regions in the design
•Control power rails generation at macro cells

Partial blockages
By default a placement blockage has a blockage factor of 100%. No cells can be placed in that area, but flexibility of blockages can be chosen by partial blockages. To reduce placement density without blocking 100% of the area, changing the blockage factor of an existing blockage to lower value will be a better option.

Keepout Margin (Halo)
It's the region around the boundary of fixed macros in design in which no other macros or std-cells can be placed. It allows placement of buffers and inverters in its area. Pictorial representation of halo is mentioned in the figure-1.
Halos of adjacent macros can overlap; there the size of halo determines the default top level channel size between macros. Prevent cells from being placed at or near the macros.
If the macros are moved from one place to another, hallows will also be moved.

Power Planning

- Power Planning is one of the most important stage in Physical design. Power network is being synthesized, It is used provide power to macros and standard cells within the given IR-Drop limit. Steady state IR Drop is caused by the resistance of the metal wires comprising the power distribution network. By reducing the voltage difference between local power and ground, steady-state IR Drop reduces both the speed and noise immunity of the local cells and macros.

- Power planning management can be divided in two major category first one is core cell power management and second one I/O cell power management. In core cell power planning power rings are formed around the core and macro. In IO cell power planning power rings are formed for I/O cells and trunks are created between core power ring and power pads.

- power planning is part of floor plan stage. In power plan, offset value for rings around the core and vertical and horizontal straps is being define

- I/O cell library contains I/O cell and VDD/VSS pad cell libraries. It also contain IP libraries for reusable IP like RAM, ROM and other pre designed, standard, complex blocks.

Using below mentioned equations we can calculate vertical and horizontal strap width and required number of straps for each macro.

- Block current:

$$I_{block} = P_{block} / V_{ddcore}$$

- Current supply from each side of the block:

$$I_{top} = I_{bottom} = \{ I_{block} * [W_{block} / (W_{block} + H_{block})] \} / 2$$
$$I_{left} = I_{right} = \{ I_{block} * [H_{block} / (W_{block} + H_{block})] \} / 2$$

- Power strap width based on EM:

$$W_{strap\_vertical} = I_{top} / J_{metal}$$
$$W_{strap\_horizontal} = I_{left} / J_{metal}$$

- Refresh width:

$$W_{refresh\_vertical} = 3 * \text{routing pitch} + \text{minimum width of metal (M4)}$$
$$W_{refresh\_horizontal} = 3 * \text{routing pitch} + \text{minimum width of metal (M3)}$$

- Refresh number

$$N_{refresh\_vertical} = \max (W_{strap\_vertical}) / W_{refresh\_vertical}$$
$$N_{refresh\_horizontal} = \max (W_{strap\_horizontal}) / W_{refresh\_horizontal}$$

- Refresh spacing

$$S_{refresh\_vertical} = Wblock / N_{refresh\_vertical}$$
$$S_{refresh\_horizontal} = Hblock / N_{refresh\_horizontal}$$

Floorplan Signoff

- PV Health
- PDN Health
- FV Health

Placement

- Introduction
- Inputs Required & Sanity Check
- Special Cell Placement
- Optimizing and Reordering Scan Chains
- Placement Methodology
- Major Placement Steps
- Post Placement Analysis
- Do’s and Don’ts of Placement
- Sanity Check & Placement Sign-off
- Time to share

Introduction to Placement

- After we have done floor planning, i.e. created the core area, placed the macros, and decided the power network structure of your design, it is time to let the tool to do standard cell placement.
- The tool determines the location of each of the components on the die. Various factors come into play, like the timing requirement of the system, the interconnect lengths and hence the connections between cells, power dissipation etc.
- The interconnect lengths depend on the placement solution used, and it is very important in determining the performance of the system as the geometries shrink. Placement also determines the routability of your design.
- Placement does not just place the standard cells available in the synthesized netlist. It also optimizes the design, thereby removing any timing violations created due to the relative placement on die.

Inputs Required and Sanity Check

- Floorplan Netlist (.v, .vhdl)
- Logical and Physical Libraries
- TLU+ Files
- Physical partitioning information of the design
- Design Constrains (SDC) (It includes SCAN DEF also)
- TECH LEF
- Floorplan DEF
- UPF

1. Special Cell Placement :- Placement of Well-Tap Cells, End-Cap Cells, Spare Cells, Decap Cells, JTAG and Other Cells Close to the I/Os

2. Optimizing and Reordering Scan Chains

3. Placement Methodology :- Congestion Driven Placement Timing Driven Placement

4. Major Placement Steps :- Virtual Placement, HFN synthesis, Initial (Global) Placement, Detailed, placement (Legalization) –Refine Placement

5. Post Placement Analysis-

1. Timing, Congestion Analysis

2. Placement Congestion: cell density

3. Global Route Congestion

Placement Signoff

- PV Health
- PDN Health
- FV Health
- CLP Health
- Timing Health