

Assignment -1 (Number System & Codes)

Q1. Complete the following table with equivalents in the respective number systems.

<u>Decimal</u>	<u>Binary</u>	<u>Octal</u>	<u>Hexa</u>
143.75	10001111.11	217.6	8F.C
27.625	11011.101	33.5	1B.A
299	100101011	453	12B
31.75	00011111.1100	37.6	1F.C

$$\begin{array}{r}
 2 \overline{) 143} \\
 2 \overline{) 71} \quad 1 \\
 2 \overline{) 35} \quad 1 \\
 2 \overline{) 17} \quad 1 \\
 2 \overline{) 8} \quad 1 \\
 2 \overline{) 4} \quad 0 \\
 2 \overline{) 2} \quad 0 \\
 \hline 0 \quad 0
 \end{array}
 \quad
 \begin{array}{l}
 0.75 \times 2 = 1.5 \\
 0.5 \times 2 = 1.0 \\
 \cancel{0 \times 2 = 0}
 \end{array}
 \quad
 (10001111.11\cancel{0})_2$$

$$\begin{array}{r}
 8 \overline{) 143} \\
 8 \overline{) 17} \quad 7 \\
 \hline 2 \quad 1
 \end{array}
 \quad
 \begin{array}{l}
 0.75 \times 8 = 6.0 \\
 \cancel{0 \times 8 = 0}
 \end{array}
 \quad
 (217.6)_8$$

$$\begin{array}{r}
 16 \overline{) 143} \\
 8 \quad F
 \end{array}
 \quad
 \begin{array}{l}
 0.75 \times 16 = C.0 \\
 \cancel{0 \times 16 = 0}
 \end{array}
 \quad
 (8F.C)_{16}$$

$$\begin{aligned}
 & 1 \times 2^{-3} + 0 \times 2^{-2} + 1 \times 2^{-1} + 1 \times 2^0 + 1 \times 2^1 + 0 \times 2^2 + 1 \times 2^3 + 1 \times 2^4 \\
 &= 0.125 + 0 + 0.5 + 1 + 2 + 0 + 8 + 16 \\
 &= (27.625)_{10}
 \end{aligned}$$

$$\left(\underline{\underline{11011}} \cdot \underline{\underline{101}}\right)_2 = (33.5)_8$$

011 011 101

$$\left(\underline{\underline{11011}} \cdot \underline{\underline{101}}\right)_2 = (1B.A)_{16}$$

0001 1011 1010

$$\begin{aligned} & 4 \times 8^2 + 5 \times 8^1 + 3 \times 8^0 \\ &= 256 + 40 + 3 \\ &= (299)_{10} \end{aligned}$$

$$\left(\underline{\underline{45}} \underline{\underline{3}}\right)_8 = (\underline{\underline{100101011}})_2$$

$$\left(\underline{\underline{45}} \underline{\underline{3}}\right)_8 = (2B)_{16}$$

$$C \times 16^{-1} + E \times 16^0 + I \times 16^1$$

$$\begin{aligned} &= 0 \cdot 25 + 15 + 16 \\ &= (31.75)_{10} \end{aligned}$$

$$\left(\underline{\underline{1E}} \underline{\underline{C}}\right)_{16} = (\underline{\underline{00011111.1100}})_2$$

$$\left(\underline{\underline{1E}} \underline{\underline{C}}\right)_{16} = (37.6)_8$$

2. Find the equivalents for the given numbers.

a) $(324)_5 = (89)_{10}$

$$3 \times 5^2 + 2 \times 5^1 + 4 \times 5^0$$
$$= 25 + 10 + 4$$
$$= (89)_{10}$$

b) $(32.23)_4 = (14.6875)_{10}$

$$3 \times 4^1 + 2 \times 4^0 + 2 \times 4^{-1} + 3 \times 4^{-2}$$
$$= 12 + 2 + 0.5 + 0.1875$$
$$= (14.6875)_{10}$$

c) $(231)_{10} = (450)_7$

$$\begin{array}{r} 7 \overline{)231} \\ 7 \overline{)33} \quad 0 \\ 4 \quad 5 \end{array}$$

d) $(189)_{10} = (513)_6$

$$\begin{array}{r} 6 \overline{)189} \\ 6 \overline{)31} \quad 3 \\ 5 \quad 1 \end{array}$$

Q3. Find the radix

a) $(121_2)_r = (13, 1)_r$

$$\frac{3r^2 + r + 2}{2r} = r + 3 + \frac{1}{r}$$

$$\Rightarrow (3r^2 + r + 2) = 2r^2 + 6r + 2$$

$$\Rightarrow r^2 - 5r = 0$$

$$\Rightarrow r(r - 5) = 0$$

$$r = 0 \text{ or } r = 5$$

$\times \quad \checkmark$

$$b) (264)_8 + (136)_8 = (433)_8$$

$$2x^2 + 6x^1 + 4x^0 + x^2 + 3x^1 + 6 = 4x^2 + 3x + 3$$

$$\Rightarrow -x^2 + 6x + 7 = 0$$

$$\Rightarrow -x^2 + 7x - x + 7 = 0$$

$$\Rightarrow -x(x-7) - 1(x-7) = 0$$

$$x = -1 \quad \text{or} \quad x = 7$$

$$c) (221505)_8 = (2345)_8$$

$$\Rightarrow 2 \times 8^5 + 2 \times 8^4 + 1 \times 8^3 + 5 \times 8^2 + 0 \times 8^1 + 5 \times 8^0 = x^4 + 2x^3 + 3x^2 + 4x + 5$$

$$\Rightarrow 65536 + 8192 + 512 + 320 + 0 + 5 = x^4 + 2x^3 + 3x^2 + 4x + 5$$

$$x^4 + 2x^3 + 3x^2 + 4x + 5 = 74565$$

$$x = 16$$

Q4. Develop your own technique for converting a base 3 number into base 9 number directly. Use your own technique for converting $(12010210.1120222)_3$ into base 9 number.

Ans \rightarrow Since, $2^3 = 8$ for converting Binary number to Octal no. we have created group with 3 digits.

Similarly since $3^2 = 9$, we have to create group with 2 digits & represent each group with equivalent base 9 no.

$$\begin{array}{r} 12010210.1120222 \\ \hline 5 \quad 1 \quad 2 \quad 3 \quad 4 \quad 6 \quad 8 \quad 7 \end{array}$$

$$\Rightarrow (12010210.1120222)_3 = (5123.4687)_9$$

5. Solve the following

a) $(1101)_2 + (110111)_2 = (1111100)_2$

$$\begin{array}{r} 1101 \\ + 110111 \\ \hline 1111100 \end{array}$$

b) $(27652)_8 + (26543)_8 = (171415)_8$

$$\begin{array}{r} 27652 \\ + 26543 \\ \hline 176415 \end{array}$$

c) $(528A)_{16} + (ABDE)_{16} = (10368)_{16}$

$$\begin{array}{r} 528A \\ + ABDE \\ \hline 10368 \end{array}$$

d) $(234)_6 + (315)_6 = (553)_6$

$$\begin{array}{r} 234 \\ + 315 \\ \hline 553 \end{array}$$

Q6. Solve the following using $(n-1)$'s complement where n is the radix of the given numbers.

$$a) (1101)_2 - (10111)_2 = (-1100010)_2$$

$1^{\text{'}}\text{s comp.}$ of 1101111 is 0010000

$$\begin{array}{r} 1101 \\ + 0010000 \\ \hline 0011101 \end{array}$$

$1^{\text{'}}\text{s comp.}$ of 0011101 is 1100010

$$b) (77652)_8 - (76543)_8 = (1107)_8$$

$7^{\text{'}}\text{s comp.}$ of 76543 is $77777 - 76543 = 01234$

$$\begin{array}{r} 77652 \Rightarrow \\ - 76543 \Rightarrow \\ \hline + 01234 \end{array}$$

$$01106 + 1 = 1107$$

$$c) (578A)_{16} - (ABDE)_{16} = (-5454)_{16}$$

$15^{\text{'}}\text{s comp.}$ of $ABDE$ is $FFFF - ABDE = 5421$

$$\begin{array}{r} 578A \Rightarrow \\ - ABDE \Rightarrow \\ \hline + 5421 \\ ABAB \end{array}$$

$15^{\text{'}}\text{s comp.}$ of $ABAB$ is $FFFF - ABAB = 5454$

$$d) (315)_2 - (243)_2 = (32)_2$$

5's comp of 243 is $555 - 243 = 312$

$$\begin{array}{r} 315 \Rightarrow 315 \\ - 243 \Rightarrow +312 \\ \hline 1031 \end{array}$$

$$031 + 32$$

Q7. Solve the following using n's complement where n is the radix of given numbers.

$$g) (110111)_2 - (11011)_2 = (101000)_2$$

2's comp of 001111 is $110000 + 1 = 110001$

$$\begin{array}{r} 110111 \Rightarrow 110111 \\ - 11011 \Rightarrow +1000 \\ \hline 1101000 \end{array}$$

$$b) (652)_8 - (765)_8 = (-113)_8$$

8's comp of 765 is $777 - 765 + 1 = 013$

$$\begin{array}{r} 652 \Rightarrow 652 \\ - 765 \Rightarrow +013 \\ \hline 665 \end{array}$$

8's comp of 665 is $777 - 665 + 1 = 113$

$$c) (CD4)_{10} - (A2D)_{10} = (2A7)_{10}$$

16's comp of A2D is $FFF - A2D + 1 = 5D3$

$$\begin{array}{r} CD4 \Rightarrow CD4 \\ - A2D \Rightarrow + \frac{5D3}{12A7} \end{array}$$

$$d) (243)_6 - (315)_6 = (-326)$$

6's comp of 315 is $555 - 315 + 1 = 241$

$$\begin{array}{r} 243 \Rightarrow 243 \\ - 315 \Rightarrow + \frac{241}{524} \end{array}$$

6's comp of 524 is $555 - 524 + 1 = 032$

Q8. Convert the following Binary numbers into Gray code.

$$a) (10101)_2 = (11111)_{\text{gray}}$$

$$\begin{array}{ccccc} 1 & 0 & 1 & 0 & 1 \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 1 & 1 & 1 & 1 & 1 \end{array}$$

$$b) (01110)_2 = (01001)_{\text{gray}}$$

$$\begin{array}{ccccc} 0 & 1 & 1 & 1 & 0 \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 0 & 1 & 0 & 0 & 1 \end{array}$$

Q9. Convert the following Gray code into binary code.

a) $(01101)_\text{gray} = (01001)_2$

$\begin{array}{ccccc} 0 & / & 1 & / & 0 \\ \downarrow & / & \downarrow & / & \downarrow \\ 0 & 1 & 0 & 0 & 1 \end{array}$

b) $(10101)_\text{gray} = (11001)_2$

$\begin{array}{ccccc} 1 & 0 & / & 0 & / \\ \downarrow & / & \downarrow & / & \downarrow \\ 1 & 1 & 0 & 0 & 1 \end{array}$

Q10. Construct a table for 7321 weighted code & represent 5698 using this code.

Ans	<u>Decimal</u>	<u>7321</u>
0		0000
1		0001
2		0010
3		0011, 0100
4		0101
5		0110
6		0111
7		1000
8		1001
9		1010

$(0 \frac{110}{5} \frac{0111}{6} \frac{1010}{9} \frac{100}{8})$ using 7321

Assignment-2 (Boolean Algebra & logic gates)

Q. Represent each of the following statements by a Boolean Expression.

- a) The company safe(S) should be unlocked only when Mr. Jones (J) is in office or Mr. Evans (E) is in office and only when company(C) is open for business and only security guard(G) is present

Ans → Safe(S) is unlocked if Mr. Jones(J) or Mr. Evans(E) & are in office Company(C) is open & Guard(G) is present

S

J+E

CG

$$Q = (J+E) CG$$

- b) The elevator door(D) should be opened if the elevator is stopped(S) & in level with the Floor(F) & timer has not expired(T) or if the elevator is stopped(S) & in level with the floor(F) & a button(B) is pressed.

Ans → Door(D) is opened if Elevator stopped(S) & level with floor(F) & Time not expired(T) or Elevator stopped(S) & level with floor(F) & Button is pressed(B)

D

SFT

SFB

$$D = SFT + SFB$$

c) The Alarm(A) will ring if the Alarm Switch(S) is turned on & door(D) is not closed, or time(T) is after 6:00 PM & window(W) is not closed.

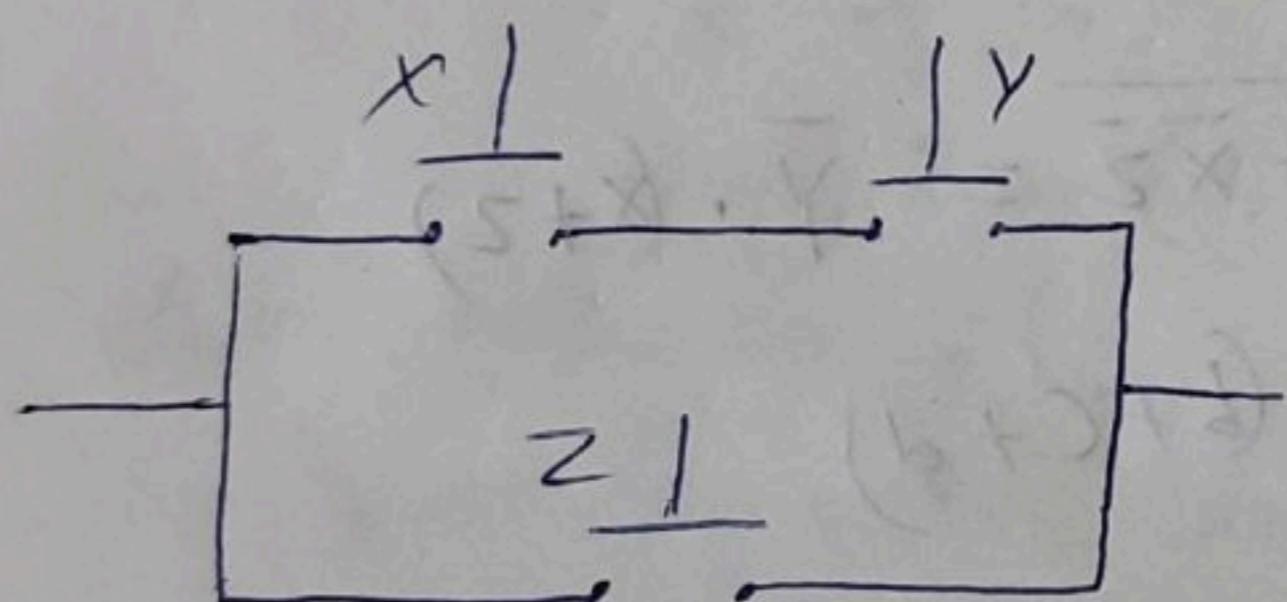
\rightarrow Alarm(A) will ring if $S \bar{D} + T \bar{W}$

Alarm switch(s) is On & Door(D) is not closed, Time(T) after 6:00 PM & Window(W) is not closed

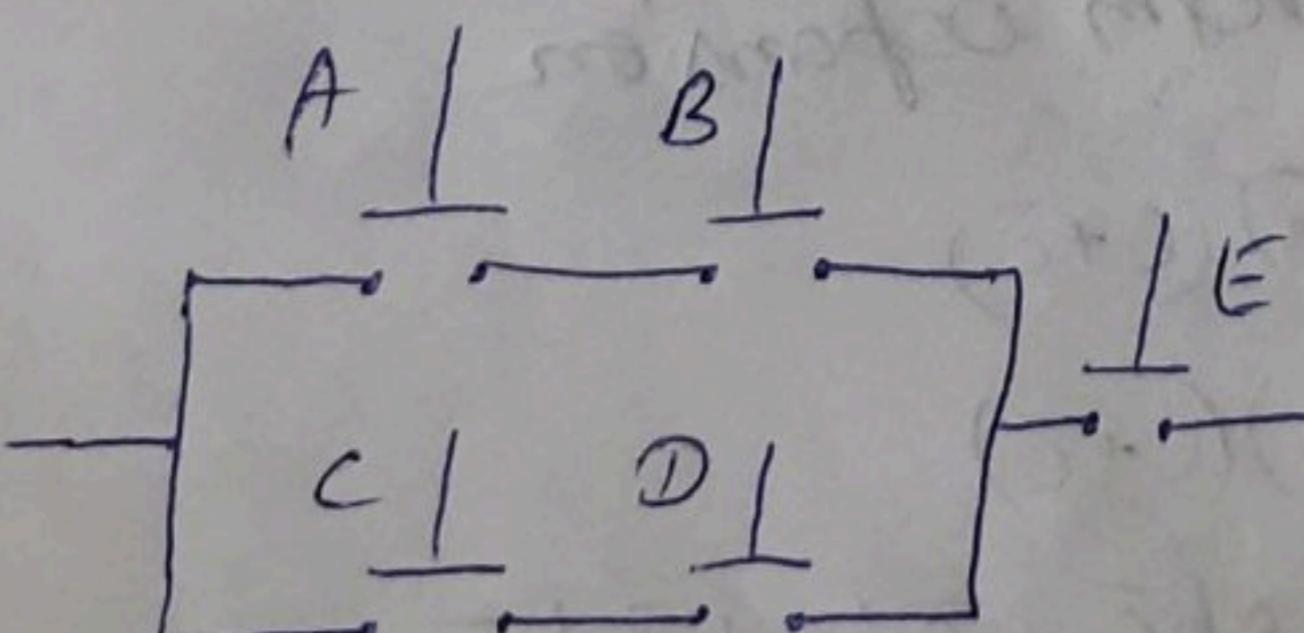
$$A = S \bar{D} + T \bar{W}$$

Q2. Illustrate the following expressions using circuits with switches.

a) $F(x,y,z) = xy + z$



b) $F(A,B,C,D,E) = (AB + CD)E$



Q3. Determine dual of the following functions

a) $F(A, B, C, D) = (A + \bar{B} + D)(\bar{A} + C)(A + B + C + D)(B + \bar{D})$

Ans $F^D(A, B, C, D) = A\bar{B}D + \bar{A}C + ABCD + B\bar{D}$

b) $F(P, Q, R) = PQ + \bar{P}\bar{Q}\bar{R} + P\bar{Q}R$

Ans $F^D(P, Q, R) = (P + Q)(\bar{P} + \bar{Q} + \bar{R})(P + \bar{Q} + R)$

Q4. Determine the complements of following functions

a) $F(X, Y, Z) = Y + \bar{X}\bar{Z}$

Ans $\bar{F}(X, Y, Z) = \overline{Y + \bar{X}\bar{Z}} = \bar{Y} \cdot (X + Z)$

b) $F(a, b, c, d) = (a+c)(b+c+d)$

Ans $\bar{F}(a, b, c, d) = \overline{(a+c)(b+c+d)} = \overline{ac} + \overline{bcd}$

Q5. Given $f(a, b, c) = ab\bar{c} + b$

a) Express f as a Minterm expansion.

$$\begin{aligned} f &= ab\bar{c} + b(a + \bar{a})(c + \bar{c}) \\ &= ab\bar{c} + (ab + \bar{a}b)(c + \bar{c}) \\ &= ab\bar{c} + abc + a\bar{b}\bar{c} + \bar{a}bc + \bar{a}\bar{b}\bar{c} \end{aligned}$$

$$f(a, b, c) = \sum m(2, 3, 6, 7)$$

b) Express complement of f as a Minterm expansion.

Ans $\bar{f}(a, b, c) = \sum m(0, 1, 4, 5)$

c) Express f as a Maxterm expansion.

$$\text{Ans} \rightarrow f(a, b, c) = \prod M(0, 1, 4, 5)$$

d) Express Complement of f as a Maxterm expansion.

$$\text{Ans} \rightarrow f(a, b, c) = \prod M(2, 3, 6, 7)$$

Q6. Prove that $F(x, y, z) = \sum m(1, 2, 4, 7)$ is a self dual func.

$$\begin{aligned}\text{Ans} \rightarrow f(x, y, z) &= \sum m(1, 2, 4, 7) \\ &= \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z} + xyz\end{aligned}$$

$$\begin{aligned}f^d(x, y, z) &= (\bar{x} + \bar{y} + z)(\bar{x} + y + \bar{z})(x + \bar{y} + \bar{z})(x + y + z) \\ &= \prod M(0, 3, 5, 6) \\ &= \sum m(1, 2, 4, 7)\end{aligned}$$

f is same as f^d .

So, given function can be considered as self dual func.

Q7. Given following truth table for a given Boolean function, complete the truth tables for complement & dual of the function F .

A	B	C	$F(A, B, C)$	A	B	C	$F'(A, B, C)$
0	0	0	1	0	0	0	0
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	1
0	1	1	0	0	1	1	1
1	0	0	1	1	0	0	0
1	0	1	1	1	0	1	0
1	1	0	0	1	1	0	1
1	1	1	1	1	1	1	0

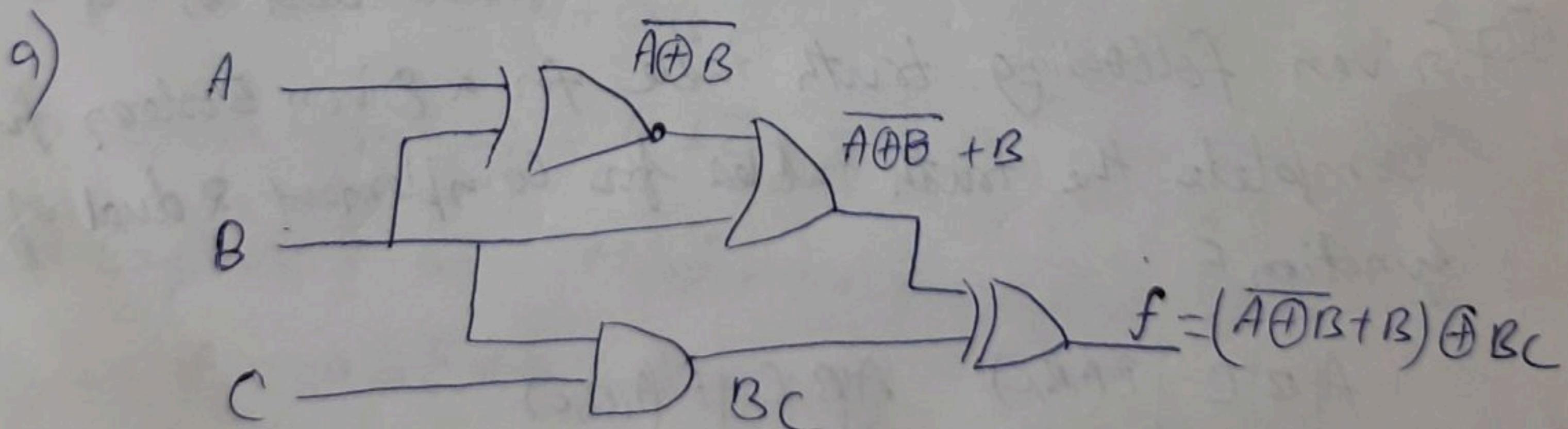
$$f(A, B, C) = \sum m(0, 1, 4, 5, 7) \quad \bar{f}(A, B, C) = \sum m(2, 3, 6)$$

A	B	C	$F^D(A, B, C)$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

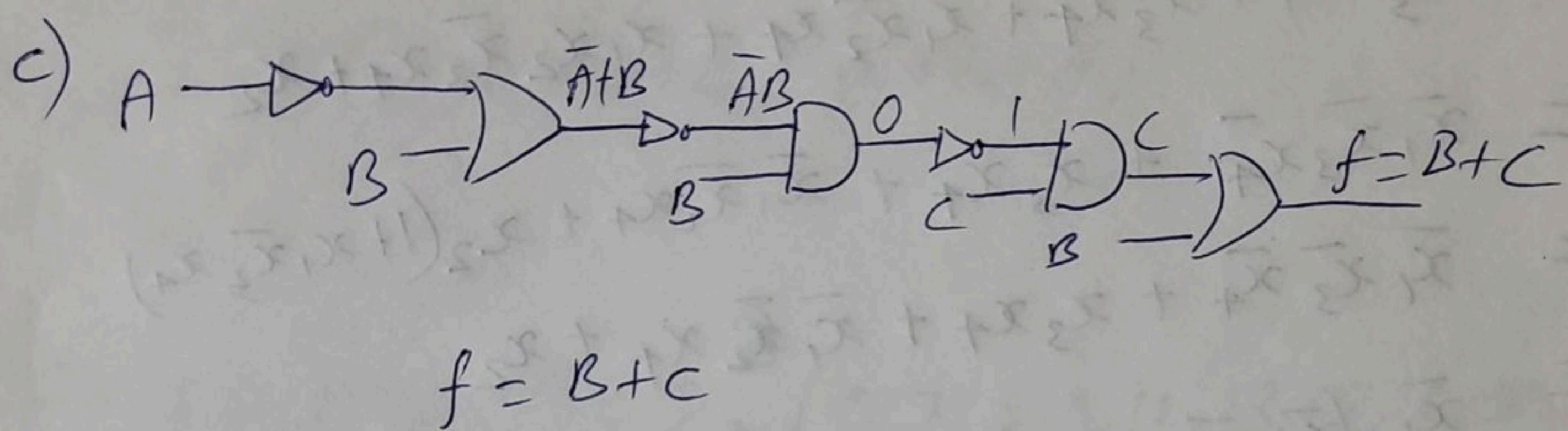
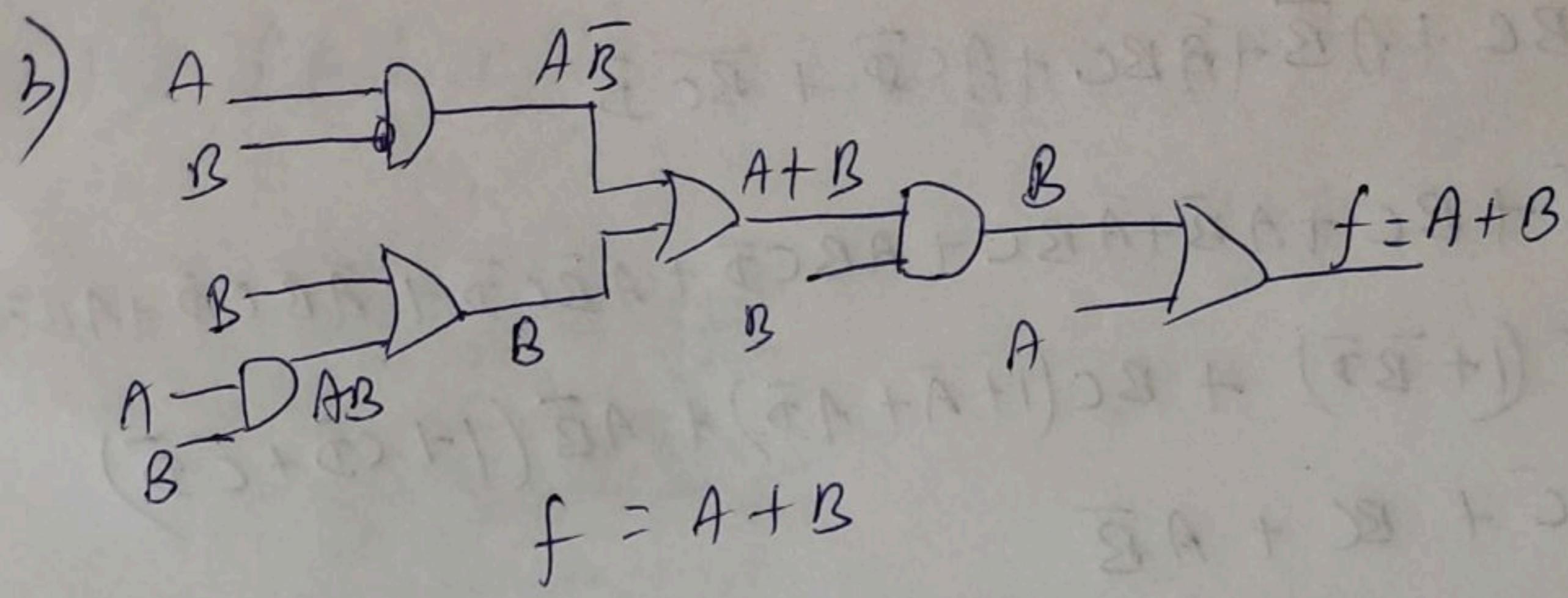
$$f(A, B, C) = \sum m(0, 1, 4, 5, 7) = \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + ABC$$

$$\begin{aligned} f^D(A, B, C) &= (\bar{A} + \bar{B} + C)(\bar{A} + \bar{B} + \bar{C})(A + \bar{B} + \bar{C})(A + \bar{B} + C)(A + B + C) \\ &= \prod M(0, 2, 3, 6, 7) \\ &= \sum m(1, 4, 5) \end{aligned}$$

Q8. Derive output expression 'f' for below CKT & draw the simplified circuits



$$\begin{aligned} f &= (\bar{A}\bar{B} + AB + B) \oplus BC \\ &= (\bar{A} + B) \oplus BC \\ &= (\bar{A} + B)BC + (\bar{A} + B)\bar{B}\bar{C} \\ &= (A\bar{B})BC + (\bar{A} + B)(\bar{B} + \bar{C}) \\ &= \bar{A}\bar{B} + \bar{A}\bar{C} + B\bar{C} \\ &= \bar{A}\bar{B} + B\bar{C} \end{aligned}$$



Q 9. Minimize following Boolean Expression using Boolean postulates.

a) $\bar{A}C\bar{D}E + \bar{A}\bar{B}\bar{D} + ABCDE + ABD$

$$= \bar{A}C\bar{D}E(B+\bar{B}) + \bar{A}\bar{B}\bar{D} + ABD + ABCDE(\bar{D}+\bar{D})$$

$$= \bar{A}BC\bar{D}E + \bar{A}\bar{B}C\bar{D}E + ABCDE + ABC\bar{D}E + \bar{A}\bar{B}\bar{D} + ABD$$

$$= BC\bar{D}E(\bar{A}+A) + \bar{A}\bar{B}\bar{D}(CE+I) + ABD(CE+I)$$

$$= BC\bar{D}E + \bar{A}\bar{B}\bar{D} + ABD$$

b) $\bar{A}\bar{B}\bar{C} + ABD + \bar{A}C + \bar{A}C\bar{D} + A\bar{C}D + A\bar{B}\bar{C}$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}C + A(BD + \bar{C}D + \bar{B}\bar{C})$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}C + A(BD + \bar{B}\bar{C})$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}C + ABD + A\bar{B}\bar{C}$$

$$= \bar{B}\bar{C} + \bar{A}C + ABD$$

$$\begin{aligned}
 & \Rightarrow \overline{AC} + BC + A\overline{B} + \overline{ABC} + AC\overline{D} + \overline{BC}\overline{D} \\
 & = \overline{AC} + BC + A\overline{B} + \overline{ABC} + ABC\overline{D} + A\overline{BC}\overline{D} + \overline{ABC}\overline{D} + A\overline{B}\overline{C}\overline{D} \\
 & = \overline{AC}(1 + \overline{BD}) + BC(1 + \overline{A} + A\overline{D}) + A\overline{B}(1 + \overline{CD} + \overline{C}\overline{D}) \\
 & = \overline{AC} + BC + A\overline{B}
 \end{aligned}$$

d)

$$\begin{aligned}
 & \overline{x_1} \overline{x_3} \overline{x_4} + x_3 x_4 + \overline{x_1} \overline{x_2} x_4 + x_1 x_2 \overline{x_3} x_4 + x_2 \\
 & = \overline{x_1} \overline{x_3} \overline{x_4} + x_3 x_4 + \overline{x_1} \overline{x_2} x_4 + x_2(1 + x_1 \overline{x_3} x_4) \\
 & = \overline{x_1} \overline{x_3} \overline{x_4} + x_3 x_4 + \overline{x_1} \cancel{x_2} x_4 + x_2 \\
 & = \overline{x_1} (\overline{x_3} \overline{x_4} + x_4) + x_3 x_4 + x_2 \\
 & = \overline{x_1} \overline{x_3} + \overline{x_1} x_4 + x_3 x_4 + x_2 \\
 & = \overline{x_1} \overline{x_3} + x_3 x_4 + x_2
 \end{aligned}$$

Q10. Minimize following Boolean expression using K-Map.

a) $f(a, b, c, d) = \sum_m(4, 6, 8, 10, 11, 12, 15) + \sum_d(3, 5, 7, 9)$

$ab \backslash cd$	\overline{cd}	$\overline{c}\overline{d}$	\overline{cd}	cd	$c\overline{d}$
\overline{ab}	0	1	X	3	2
\overline{ab}	4	X	X	6	
ab	12	13	15	14	
ab	8	X	11	10	

$$cd + \overline{ab} + a\overline{b} + b\overline{c}\overline{d}$$

$$b) f(a, b, c, d) = \prod_m(0, 2, 4, 6, 7, 9) \cdot \prod_D(10, 11)$$

$ab \backslash cd$	$\bar{c}\bar{d}$	$\bar{c}d$	$c\bar{d}$	cd
$\bar{a}b$	0	1	3	2
$a\bar{b}$	4	5	6	7
ab	12	13	15	14
$a\bar{b}$	8	9	X	X

$$(\bar{a} + \bar{d})(a + \bar{b} + \bar{c})(\bar{a} + \bar{b} + \bar{d})$$

$$c) f(A, B, C, D, E) = \sum_m(0, 7, 8, 9, 12, 13, 15, 16, 23, 25, 30, 31)$$

$BCDE$	\bar{A}	$\bar{D}\bar{E}$	$\bar{D}E$	$D\bar{E}$	DE
$\bar{B}C$	0	1	3	2	
$\bar{B}C$	+	5	7	6	4
$B\bar{C}$	12	13	15	14	
$B\bar{C}$	8	9	11	10	

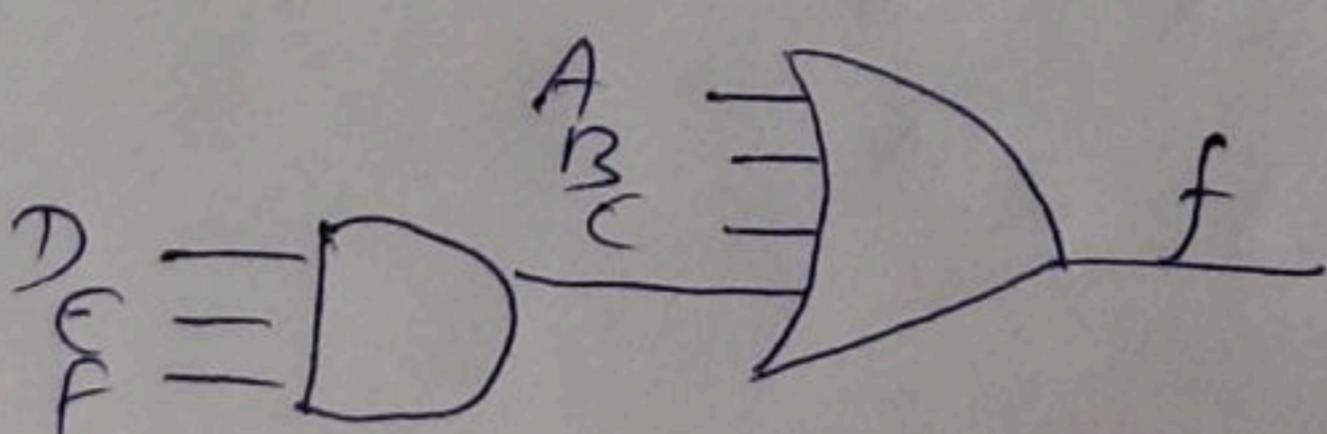
$BCDE$	A	$\bar{D}\bar{E}$	$\bar{D}E$	$D\bar{E}$	DE
$\bar{B}C$	18	18	17	16	
$\bar{B}C$	22	23	21	20	
$B\bar{C}$	30	31	29	28	
$B\bar{C}$	26	27	25	24	

$$\bar{A}\bar{B}\bar{D} + \bar{A}\bar{C}\bar{D}E + ACD + \bar{B}\bar{C}\bar{D}\bar{E}$$

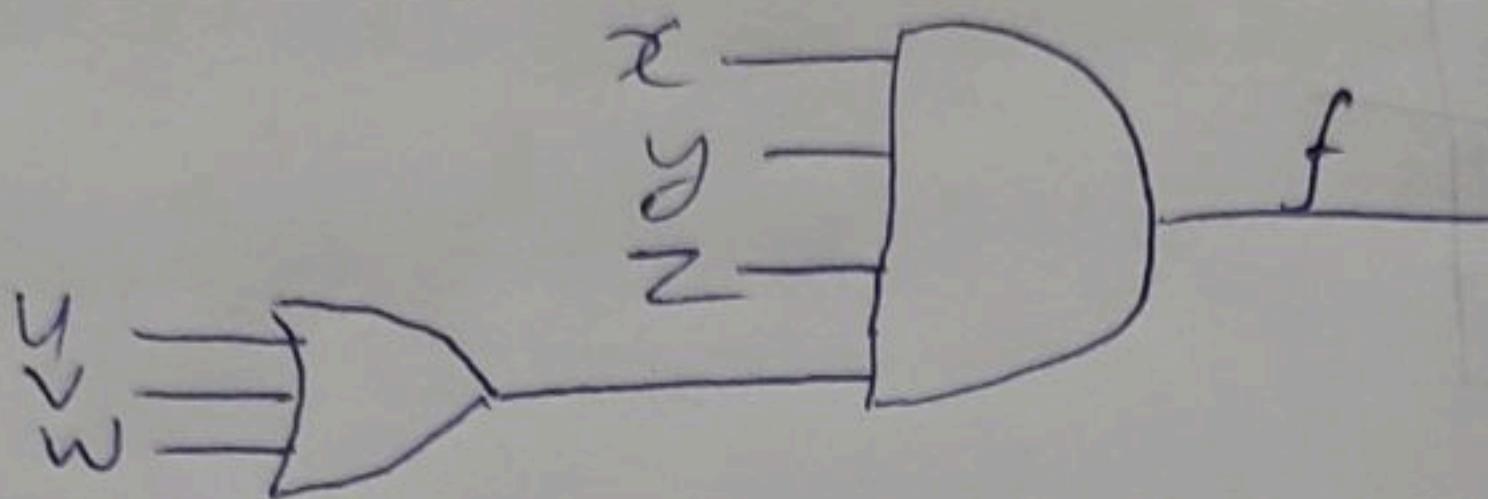
Q11.

Draw a circuit that uses, only one AND gate & one OR gate to realize following function.

$$a) f(A, B, C, D, E, F) = (A + B + C + D)(A + B + C + E)(A + B + C + F) \\ = A + B + C + DEF$$



$$\begin{aligned} \text{Q9: } f(u, v, w, x, y, z) &= wxyz + vxzy + uxzy \\ &= xyz(w + v + u) \end{aligned}$$



Q12. Draw a circuit to realize the following function.

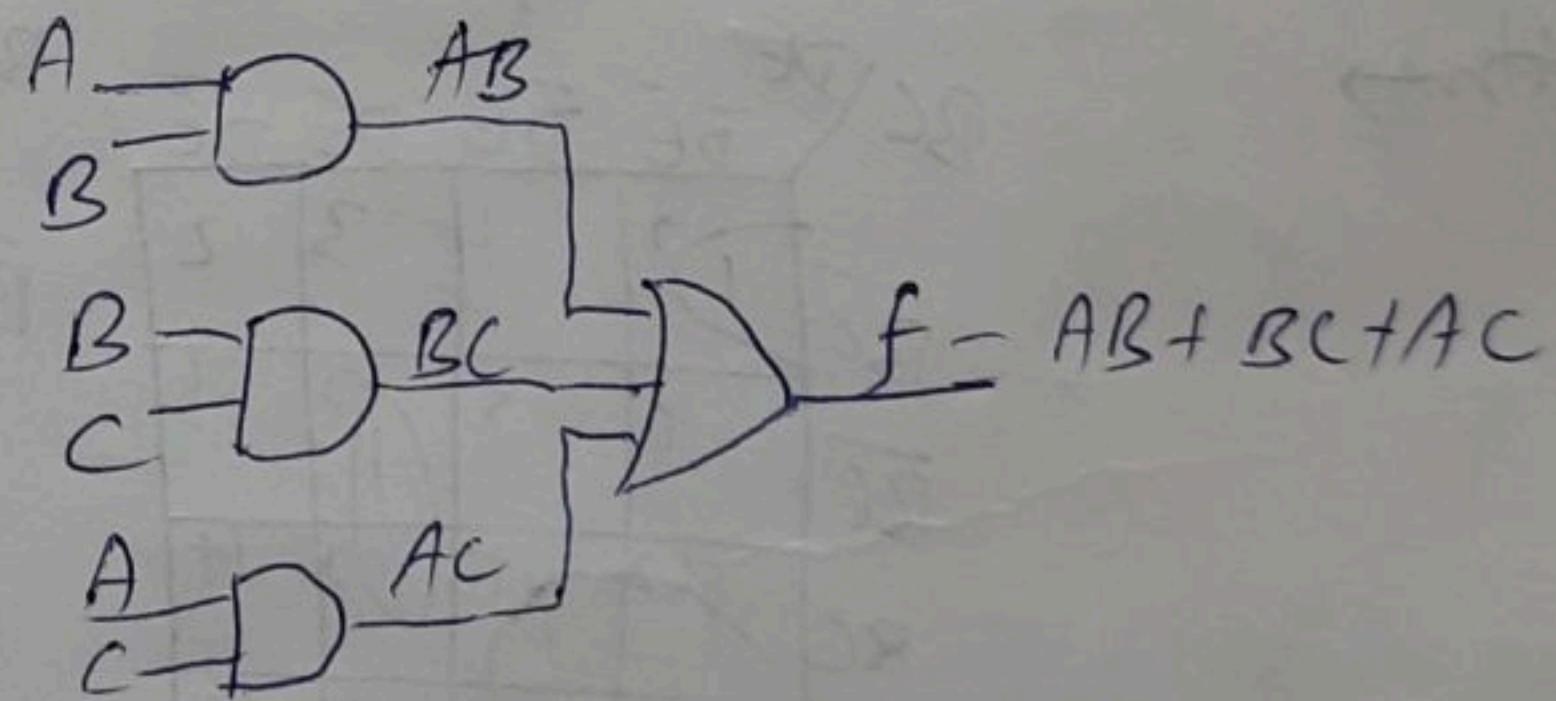
$$f(A, B, C) = ABC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C$$

a) Using 1 OR gate & 3 AND gates. The AND gates should have 2 inputs.

Ans →

	BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
A	0	0	1	1	0
\bar{A}	0	1	0	0	1
A	0	1	0	0	1

$$AB + BC + AC$$

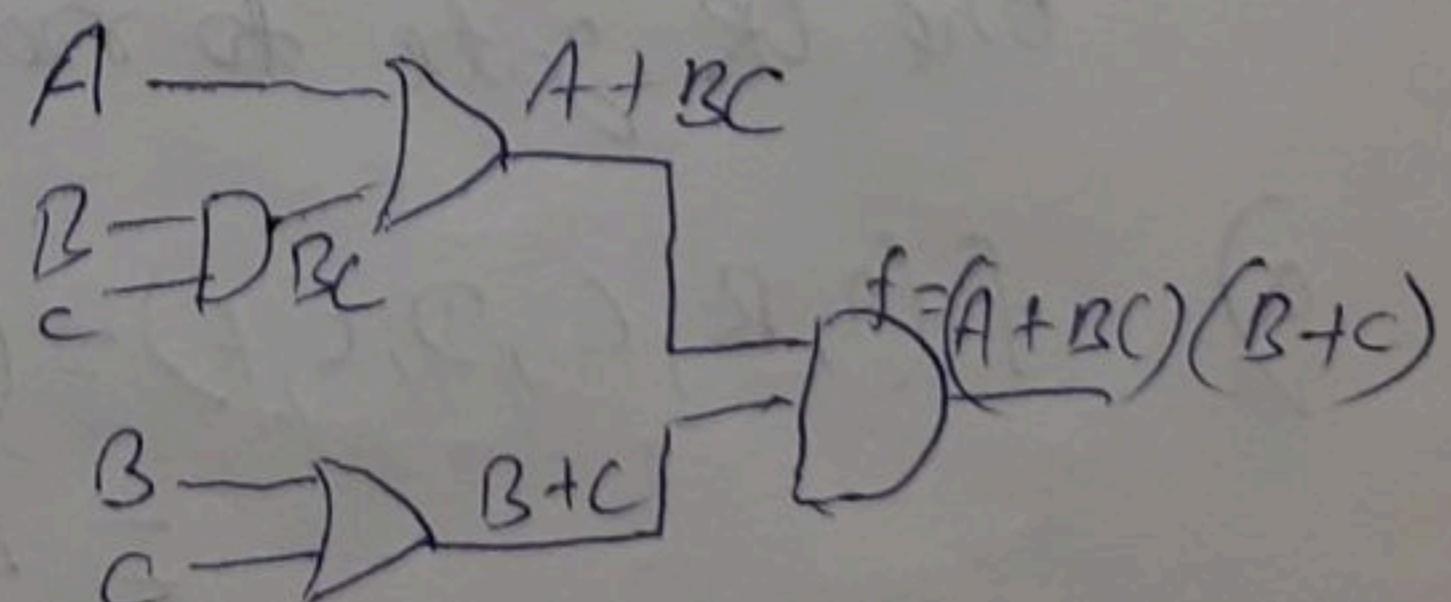


b) Using 2 OR gates & 2 AND gates. All of the gates should have 2 inputs.

Ans →

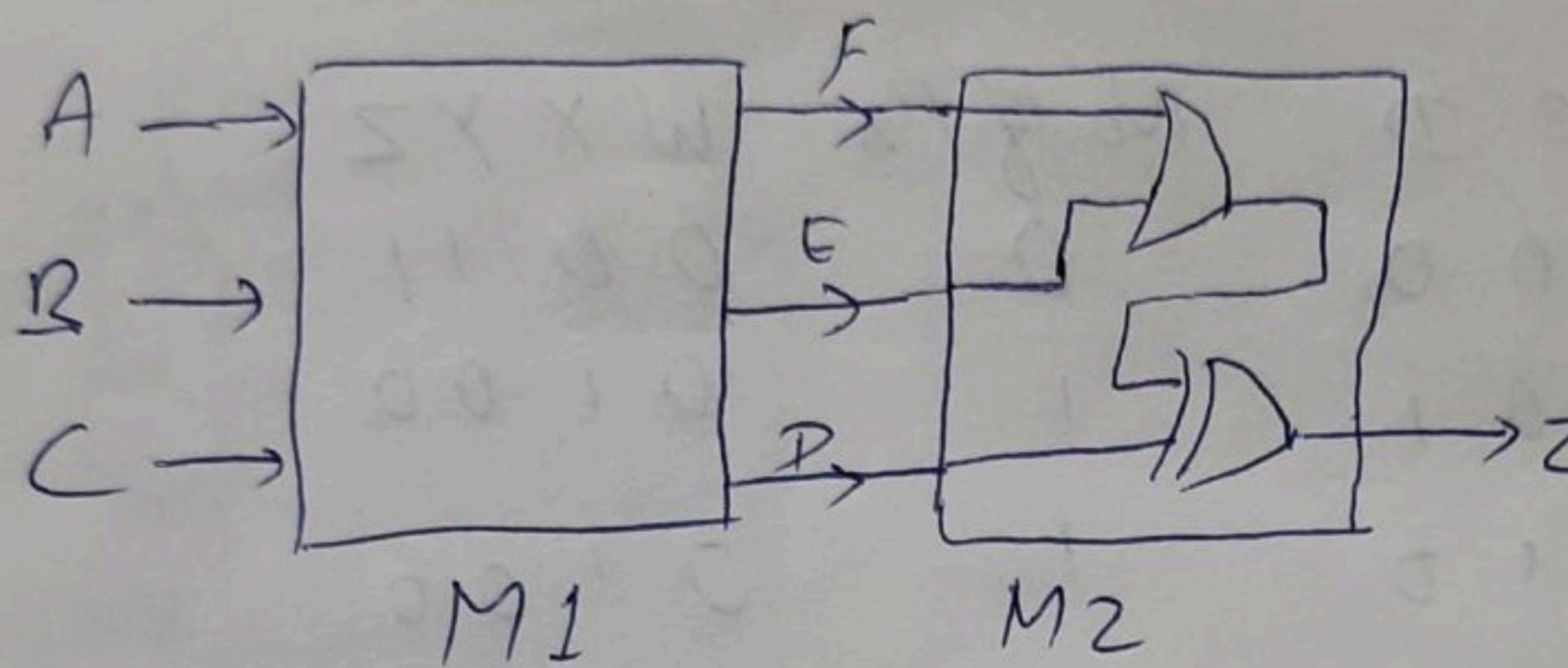
	BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
A	0	1	1	0	1
\bar{A}	0	1	0	1	0
A	0	1	1	1	0

$$\begin{aligned} &(A+B)(A+C)(B+C) \\ &= (A+BC)(B+C) \end{aligned}$$



Q13. A combinational ckt is divided into 2 modules M₁, M₂ as shown in fig. below. The behaviour of module M₁ is described in below truth table. Assume that IP combinations ABC = 011 & ABC = 110 will never occur. Optimize the module M₂, if possible.

Ans →



A	B	C	D	E	F
0	0	0	1	1	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	0	0	0
1	0	0	0	0	1
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	1	0	1

$$Z = f(D, E, F) = D \oplus (E + F)$$

$$= \bar{D}(E + F) + D(\bar{E} + \bar{F})$$

$$= \bar{D}E(F + \bar{F}) + \bar{D}\bar{F}(E + \bar{E}) + D\bar{E}\bar{F}$$

$$= \bar{D}EF + \bar{D}E\bar{F} + \bar{D}\bar{E}F + \bar{D}\bar{E}\bar{F} + D\bar{E}F$$

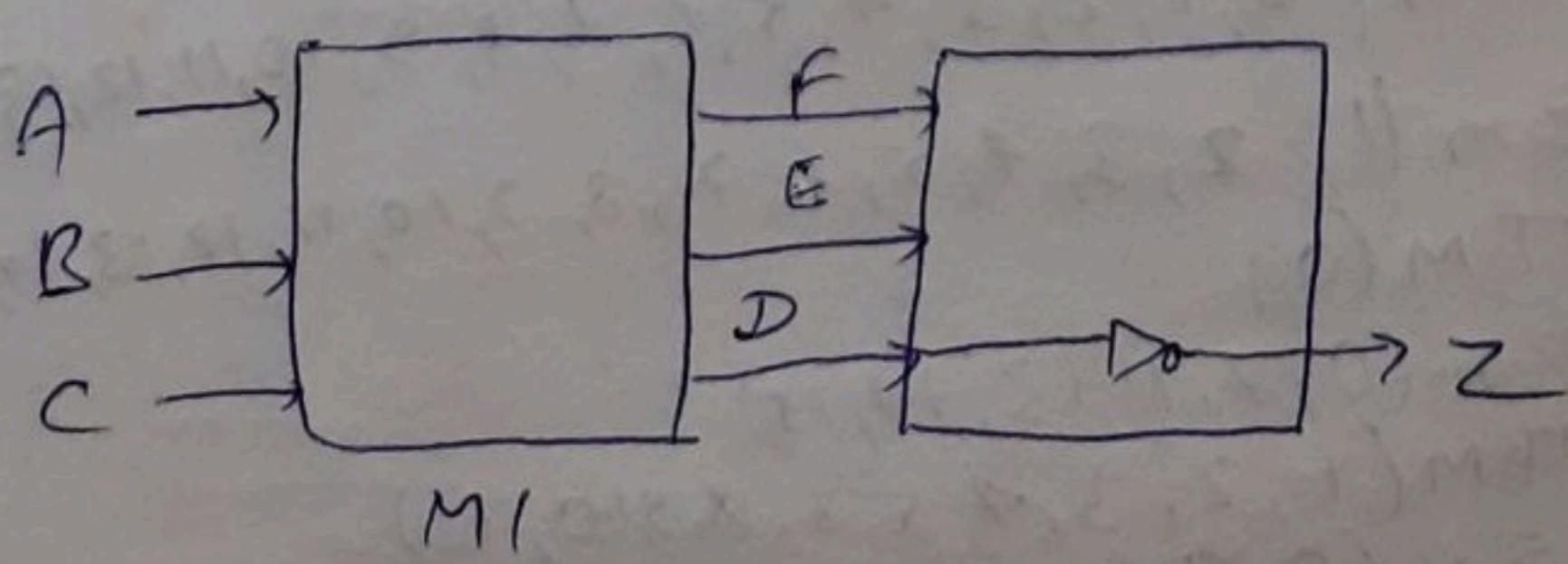
$$= \Sigma m(1, 2, 3, 4)$$

Since the combination 011 & 110 will never occur in ABC, 000, 011, 100, 111 will never occur in DEF.

$$Z = f(D, E, F) = \Sigma m(1, 2) + \Sigma d(0, 3, 4, 7)$$

D	EF	EF	EF	EF
D	0	1	3	2
D	X	1	X	1
D	X	1	X	1

$$Z = \bar{D} \quad D \rightarrow \text{D} \rightarrow Z = \bar{D}$$



Q14. A combinational CKT. has 4 I/Ps (A, B, C, D) & 4 O/Ps (W, X, Y, Z) . $WXYZ$ represents an excess 3 coded No. whose value equals the No. of 1's at the I/P. For example if $ABCD = 1101$, $WXYZ = 0110$. Find minterm & maxterm expansions for $W, X, Y \& Z$.

Ans	$A\ B\ C\ D$	No. of 1's	$W\ X\ Y\ Z$
	0 0 0 0	0	0 0 1 1
	0 0 0 1	1	0 1 0 0
	0 0 1 0	1	0 1 0 0
	0 0 1 1	2	0 1 0 1
	0 1 0 0	1	0 1 0 0
	0 1 0 1	2	0 1 0 1
	0 1 1 0	2	0 1 0 1
	0 1 1 1	3	0 1 1 0
	1 0 0 0	1	0 1 0 0
	1 0 0 1	2	0 1 0 1
	1 0 1 0	2	0 1 0 1
	1 0 1 1	3	0 1 1 0
	1 1 0 0	2	0 1 0 1
	1 1 0 1	3	0 1 1 0
	1 1 1 0	3	0 1 1 0
	1 1 1 1	4	0 1 1 1

$$W = f(A, B, C, D) = 0$$

$$= \overline{\text{IM}}(0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15)$$

$$X = f(A, B, C, D) = \sum m(1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15)$$

$$= \overline{\text{IM}}(0)$$

$$Y = f(A, B, C, D) = \sum m(0, 7, 11, 13, 14, 15)$$

$$= \overline{\text{IM}}(1, 2, 3, 4, 5, 6, 8, 9, 10, 12)$$

$$Z = f(A, B, C, D) = \sum m(0, 3, 4, 5, 9, 10, 12, 15)$$

$$= \overline{\text{IM}}(1, 2, 6, 7, 8, 11, 13, 14)$$

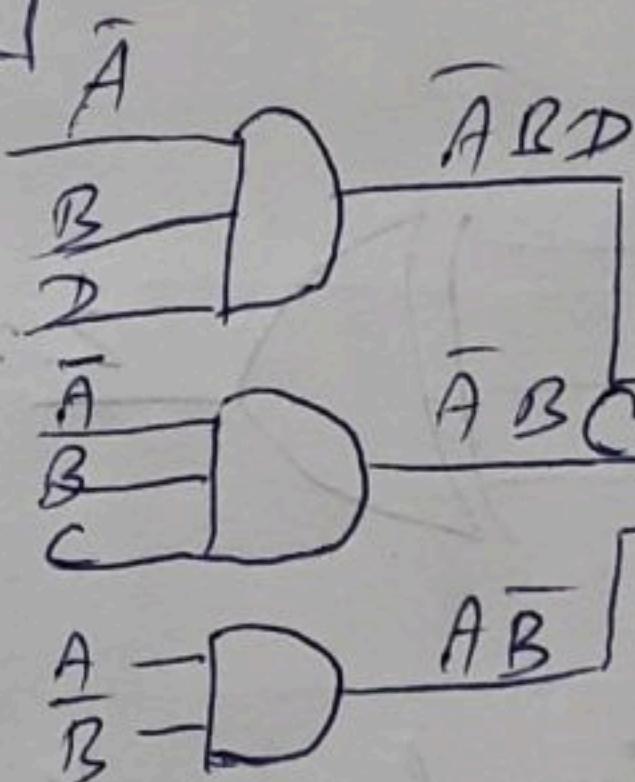
Q15. Design a combinational clkt. which has 10/p Z & 4 bit I/P ABCD representing a binary No. Z should be 1 if the I/P is at least 5, but is no greater than 11. Use 1 OR gate (Σ I/Ps) & 3 AND gates (with no more than 3 I/Ps each). Assume that complemented form of I/Ps are available.

Ans →

$$Z = f(A, B, C, D) = \Sigma m(5, 6, 7, 8, 9, 10, 11)$$

$A\bar{B}$	$C\bar{D}$	$\bar{C}\bar{D}$	CD	$C\bar{D}$
0	1	2	3	
4	5	6		
7	8	9	10	
11	12	13	14	
15				

$$\bar{A}BD + \bar{A}BC + A\bar{B}$$



Q16. Prove the following

a) $A \oplus B \oplus C = (A \oplus B) \oplus C$

$$\begin{aligned}
 (A \oplus B) \oplus C &= (\bar{A}B + A\bar{B}) \oplus C \\
 &= (\bar{A}B + A\bar{B})C + (\bar{A}B + A\bar{B})\bar{C} \\
 &= (\bar{A} + B)(\bar{A} + B)C + \bar{A}B\bar{C} + A\bar{B}\bar{C} \\
 &= AB\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C}
 \end{aligned}$$

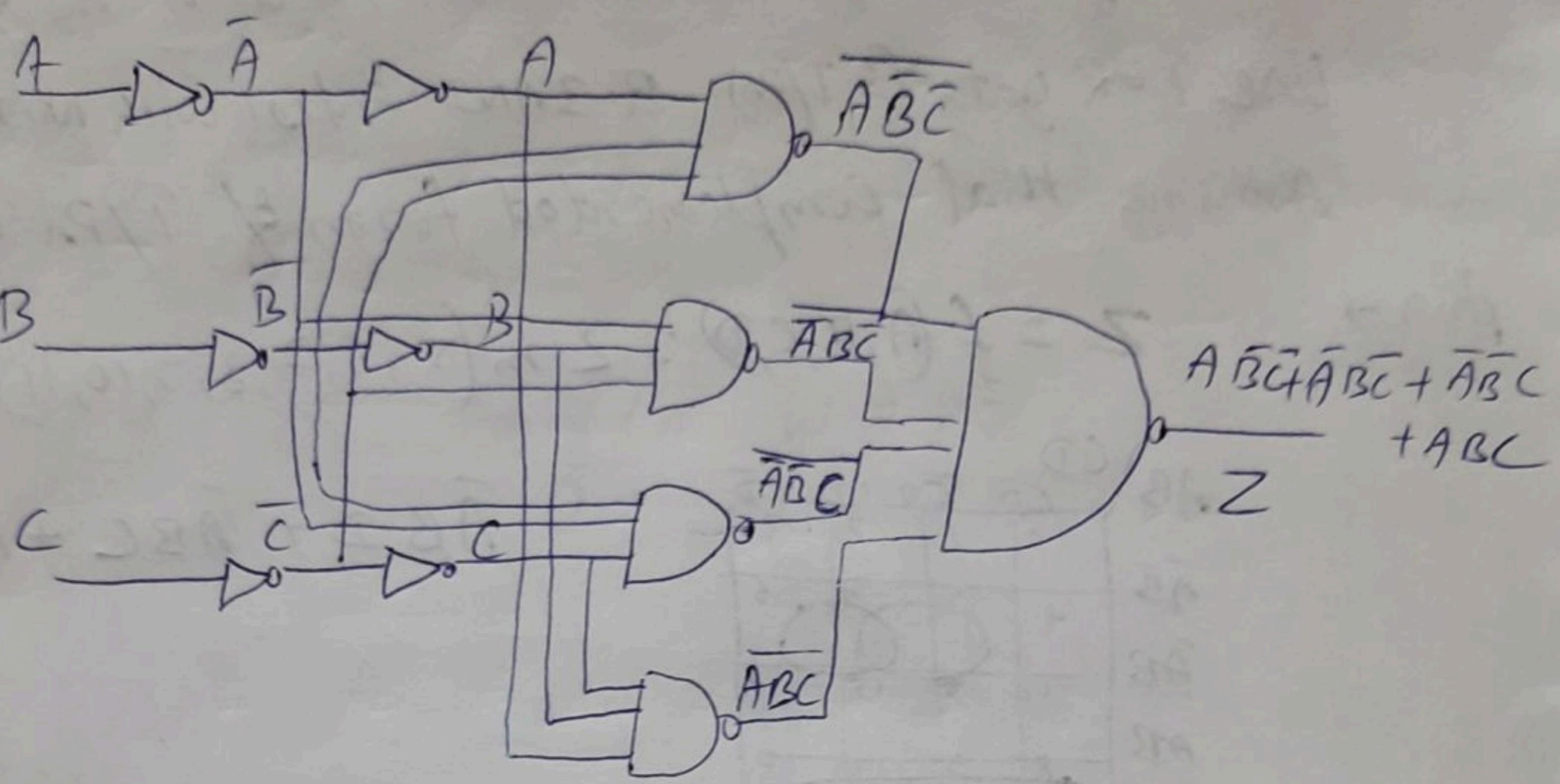
$$A \oplus B \oplus C = AB\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C}$$

b) $A \odot B \odot C \neq (A \odot B) \odot C$

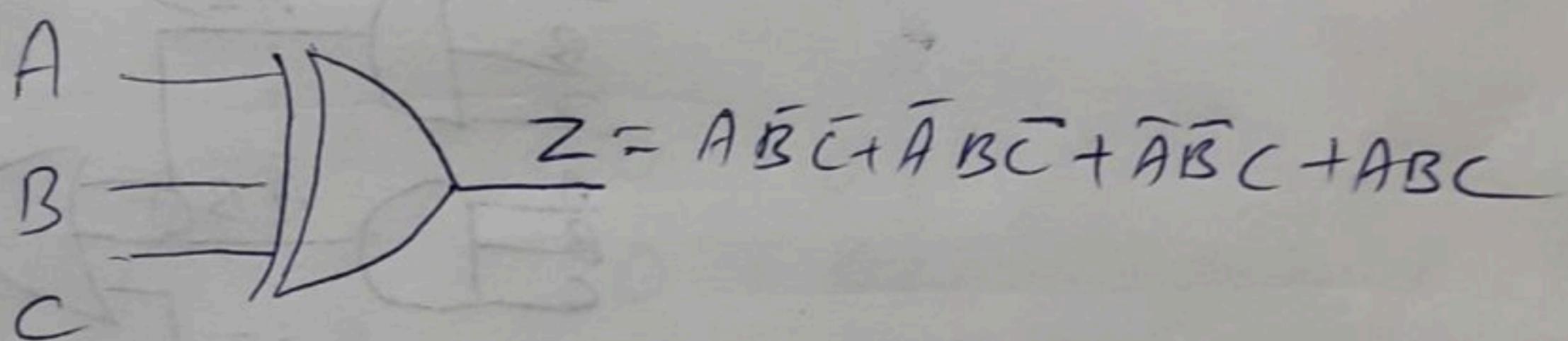
$$\begin{aligned}
 (A \odot B) \odot C &= (AB + \bar{A}\bar{B}) \odot C \\
 &= (\overline{(AB + \bar{A}\bar{B})})\bar{C} + (AB + \bar{A}\bar{B})C \\
 &= (\bar{A} + \bar{B})(A + B)\bar{C} + ABC + \bar{A}\bar{B}C \\
 &= \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C = A \oplus B \oplus C
 \end{aligned}$$

$$A \odot B \odot C = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

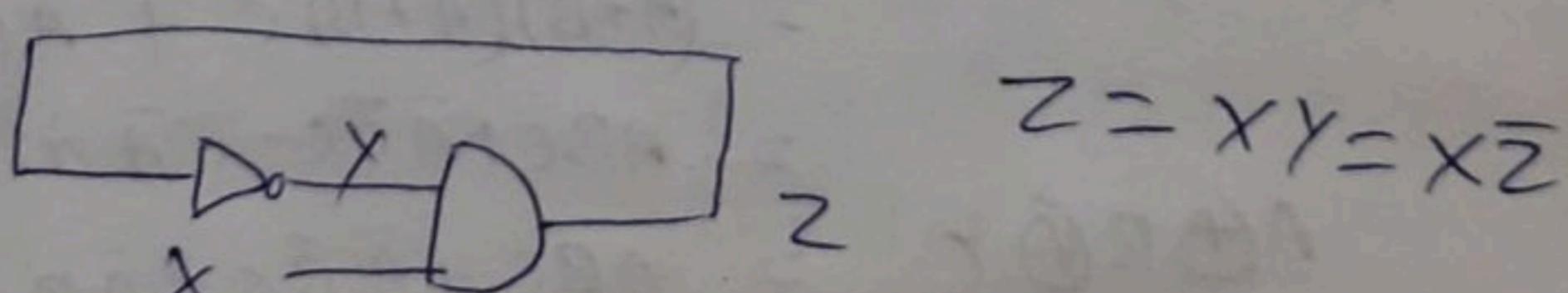
Q17. Which single gate can represent the functionality of given ckt?



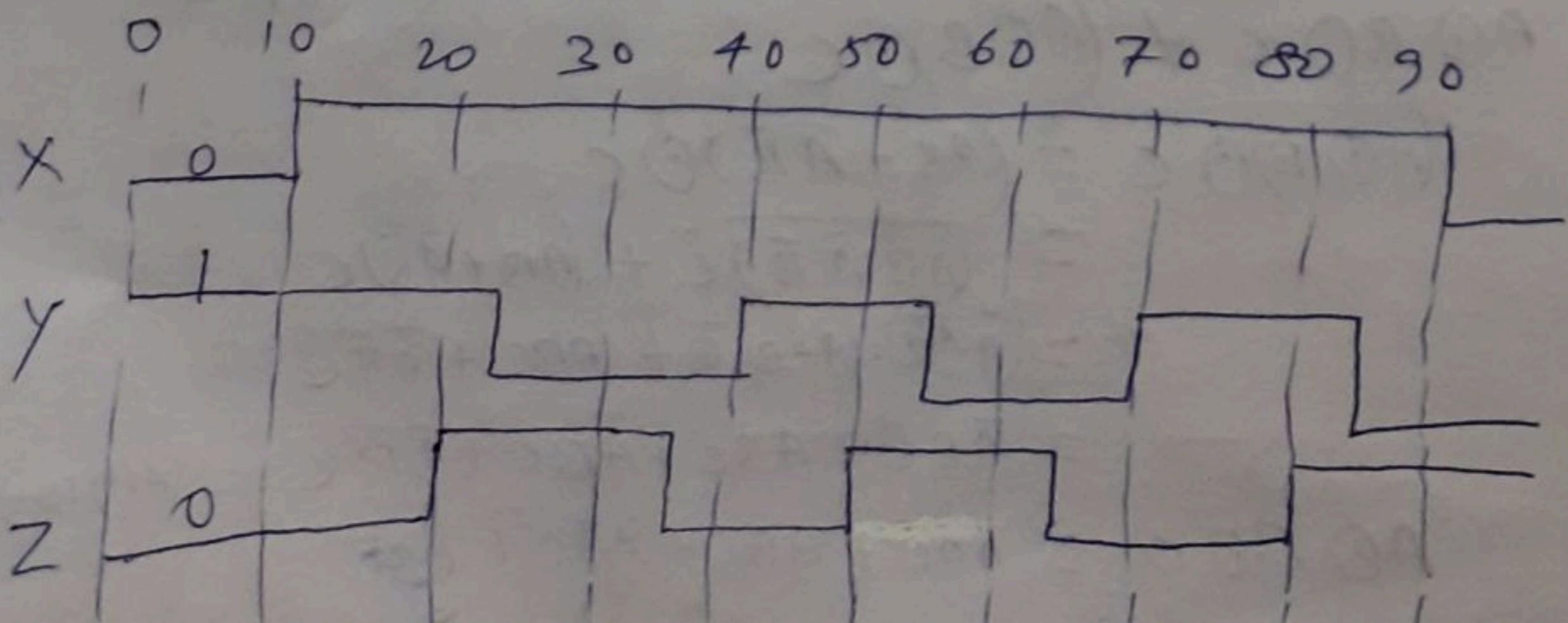
Ans →



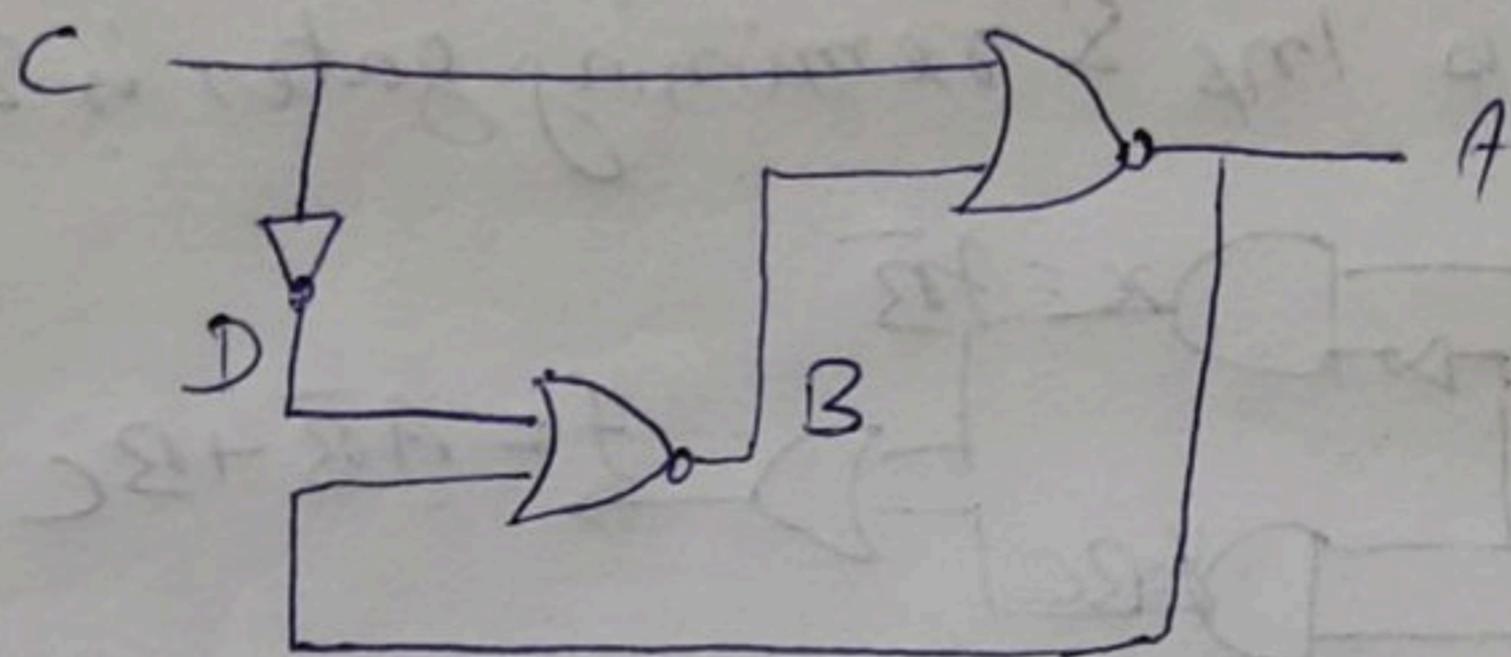
Q18. Assume that inverter in the N/w below has a propagation delay of 5ms & AND gate has propagation delay of 10ms. Draw timing diagram for the network showing X, Y, Z. Assume that X is initially 0, Y is initially 1. After some time, X becomes 1 for 80ms & then X is 0 again.



Ans →



Q13. Consider below ckt. diagram. Assume that $I/P C$ is driven by a square wave signal with a 50% duty cycle. Draw a timing diagram that shows the waveform at A & B, by assuming ~~at~~ gate delay Δ (1ns) for all gates.



$$D = \bar{C}$$

$$B = \overline{A+D}$$

$$A = \overline{B+C}$$

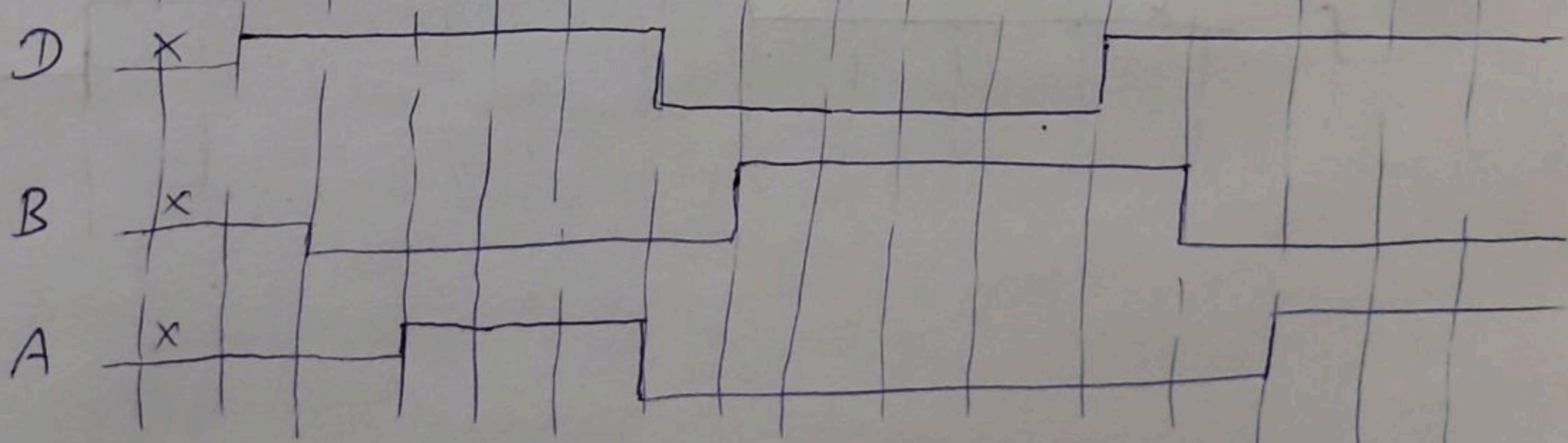
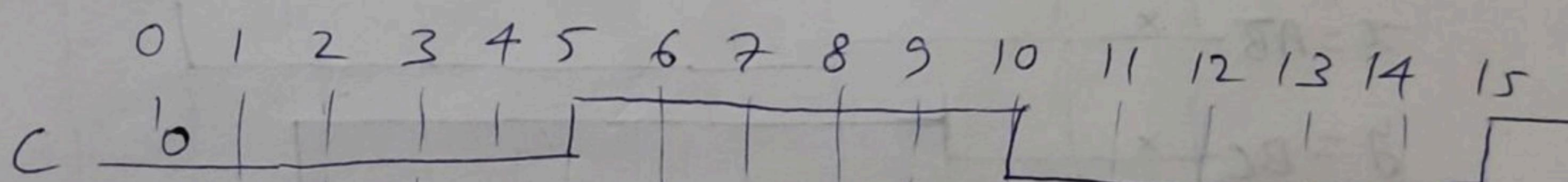
Time 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

C 0 0 0 0 0 1 1 1 1 1 0 0 0 0 0 0 1

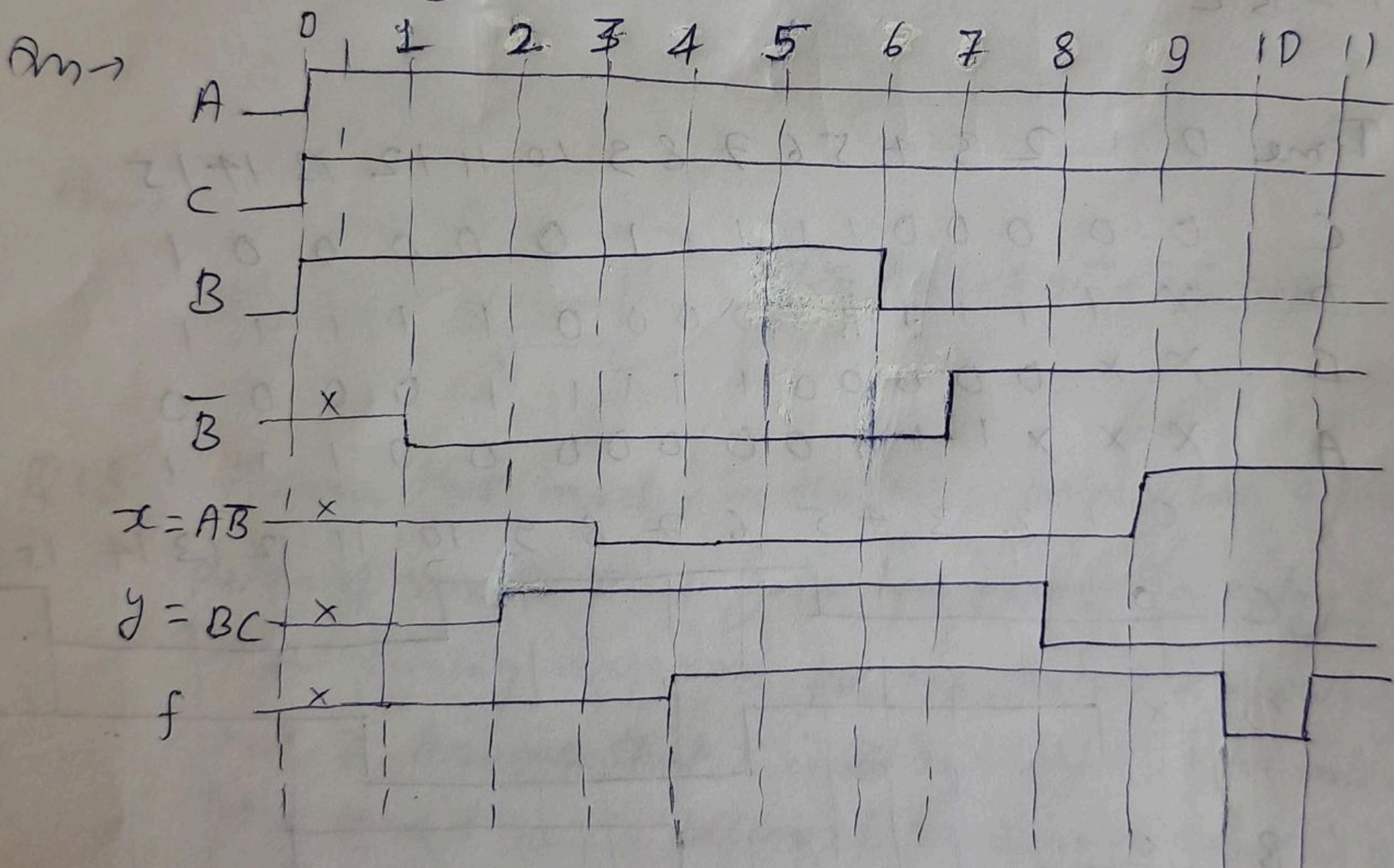
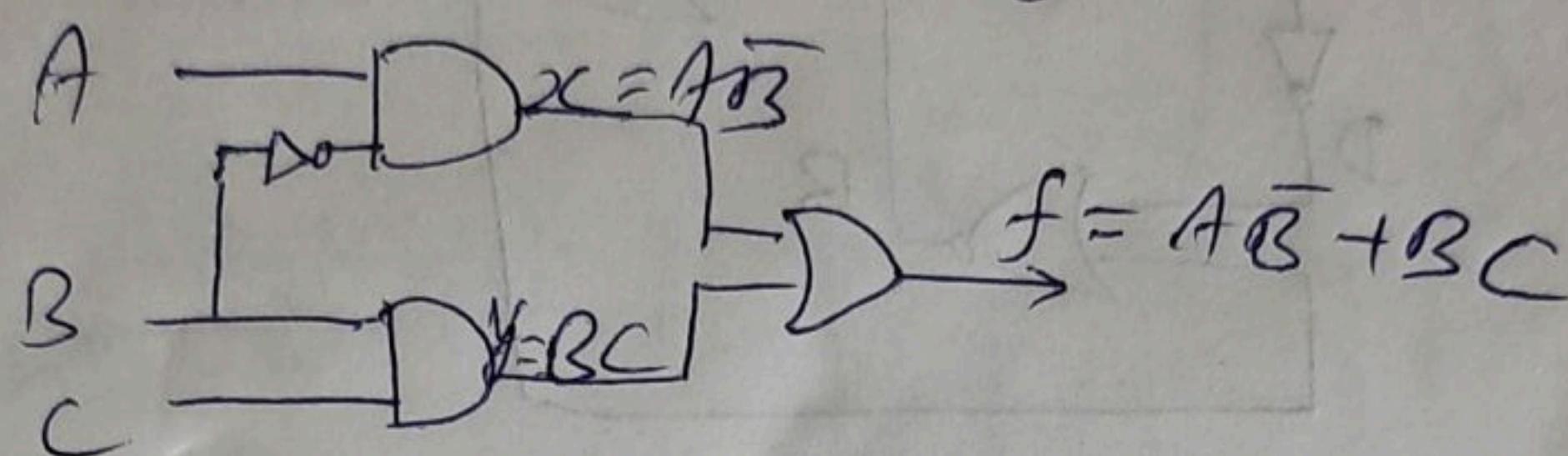
D X 1 1 1 1 1 0 0 0 0 0 1 1 1 1 1 1

B X X 0 0 0 0 0 1 1 1 1 1 0 0 0 0 0

A X X X 1 1 1 0 0 0 0 0 0 0 1 1 1



Q20. Consider the below CKF diagram. Draw waveforms for signals x , y & f . Assume initial values of A, B & C are 1. At time $t=6\text{ns}$, value of B is 0. A & C remain unchanged. The propagation delays of NOT gate is 1ns & remaining gates is 2ns .



Assignment-3 (Combinational logic CKt.)

Q1. Following sequences of bits (right most bit first) appear on the inputs to a 74LS83A 4 bit ripple carry adder. Determine resulting sequence of bits on each output.

A₀ 1001

B₀ 1111

A₁ 1110

B₁ 1100

A₂ 0000

B₂ 1010

A₃ 1011

B₃ 0010

Ans

$$\begin{array}{r}
 A_3 \ A_2 \ A_1 \ A_0 \\
 + B_3 \ B_2 \ B_1 \ B_0 \\
 \hline
 S_0 \ S_1 \ S_2 \ S_3 \ S_4
 \end{array}
 \quad
 \begin{array}{r}
 S_0 \ 0 \ 1 \ 1 \ 0 \\
 S_1 \ 1 \ 0 \ 1 \ 1 \\
 S_2 \ 0 \ 1 \ 1 \ 0 \\
 S_3 \ 0 \ 0 \ 0 \ 1 \\
 S_4 \ 1 \ 0 \ 1 \ 0
 \end{array}$$

$$\begin{array}{r}
 1 \ 0 \ 0 \ 1 \\
 + 0 \ 0 \ 0 \ 1 \\
 \hline
 1 \ 0 \ 1 \ 0
 \end{array}$$

1010

$$\begin{array}{r}
 + 1101 \\
 \hline
 10111
 \end{array}$$

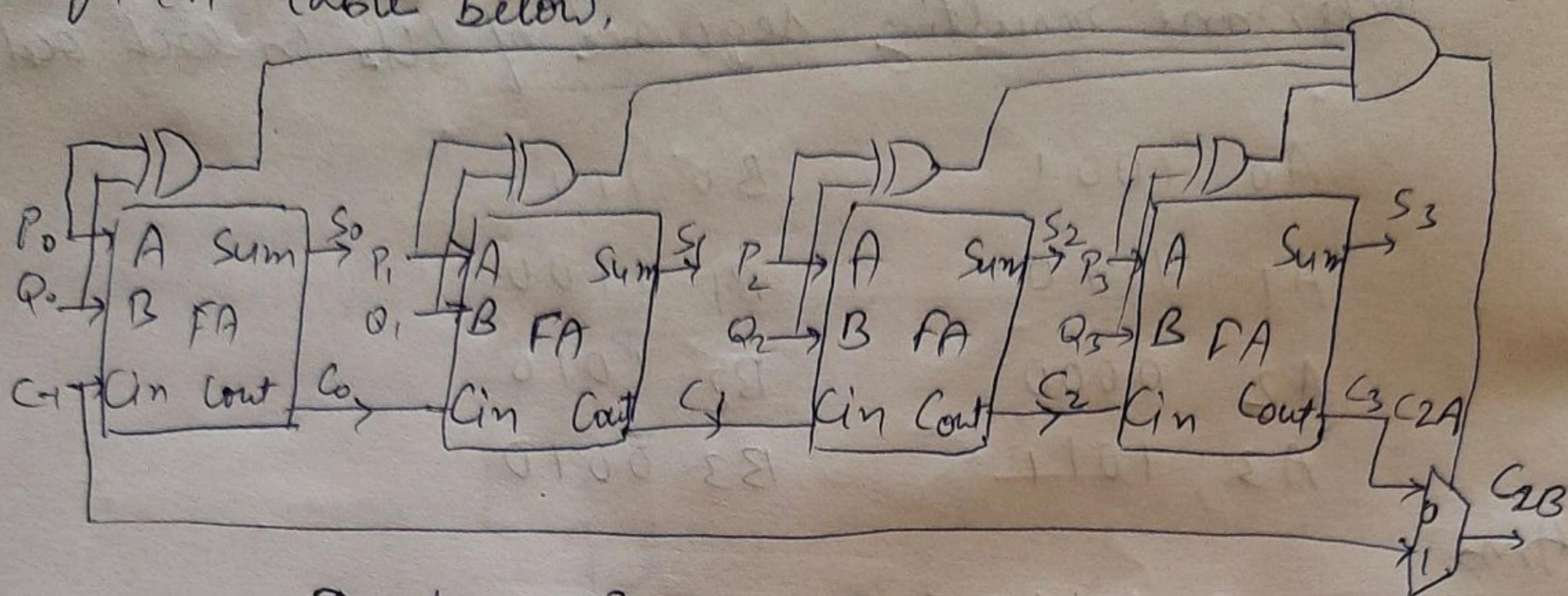
0100

$$\begin{array}{r}
 + 0011 \\
 \hline
 0101
 \end{array}$$

1011

$$\begin{array}{r}
 + 0111 \\
 \hline
 10010
 \end{array}$$

Q2. Below figure shows circuit of 4 bit carry skip adder. The worst case propagation delays of ckt elements are given table below,



Device Path Delay

Adder	Any I/P \rightarrow Sum	3
	Any I/P \rightarrow Cout	2
MUX	SEL \rightarrow O/P	3
	data I/P \rightarrow O/P	2
XOR	Any I/P \rightarrow O/P	2
AND	Any I/P \rightarrow O/P	1

- i) Determine worst case propagation delay to C_{2A} from P_0 & from C_1 .
- ii) Explain briefly why C_{2A} & C_{2B} are identical except for propagation delay.
- iii) Determine worst case propagation delay to C_{2B} from P_0 & from C_1 .

Ans i) From P_0 to $C_{2A} = 2 + 2 + 2 + 2 = 8 \text{ ns}$

From C_1 to $C_{2A} = 2 + 2 + 2 + 2 = 8 \text{ ns}$

- ii) If P & Q are complement to each other then C_{2B} will arrive first & C_{2A} will arrive later. Else C_{2A} will arrive first & same will be propagated as C_{2B} .
- iii) From P_0 to $C_{2B} = 2 + 2 + 2 + 2 + 2 = 10 \text{ ns}$ (through FA)

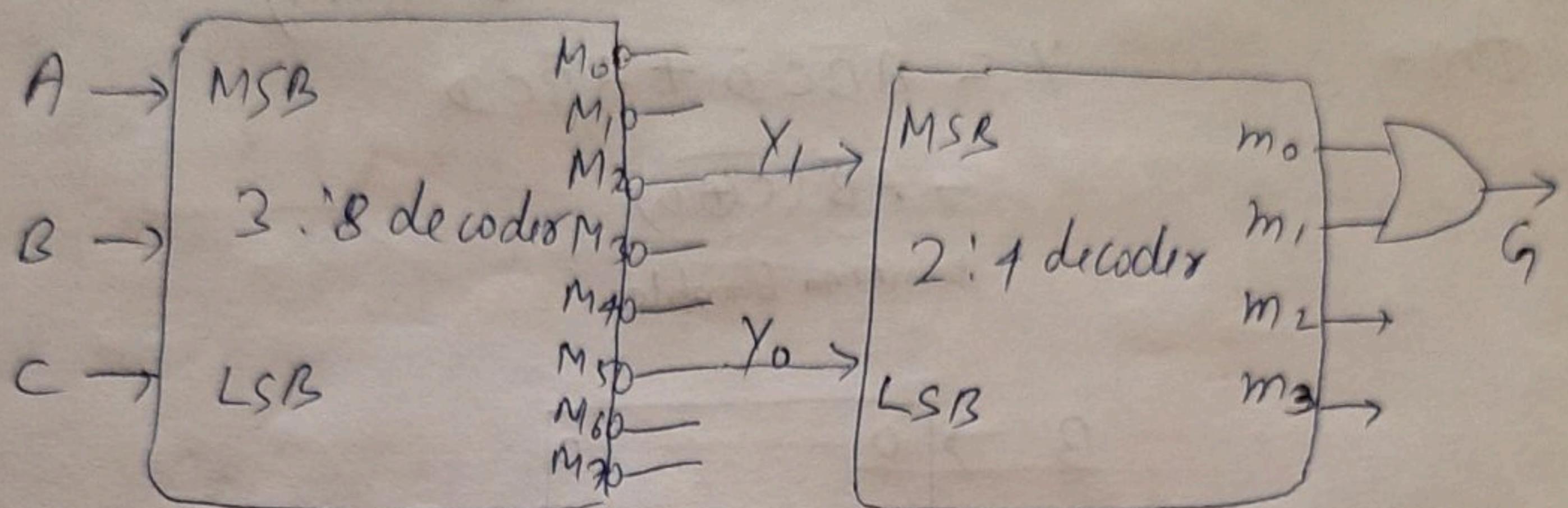
$$= 2 + 1 + 3 = 6 \text{ ns} \quad (\text{through XOR, AND, MUX})$$

worst case is 10 ns

From C_1 to $C_{2B} = 2 + 2 + 2 + 2 + 2 = 10 \text{ ns}$ (through FA)

$$= 2 \text{ ns} \quad (\text{through MUX})$$

Q3. Given following ckt comprising a 3×8 decoder with negated O/Ps & 2x4 decoder with normal O/Ps, what is Boolean func. for G in terms of A, B, C. How do you label intermediate O/Ps Y_0 & Y_1 ?

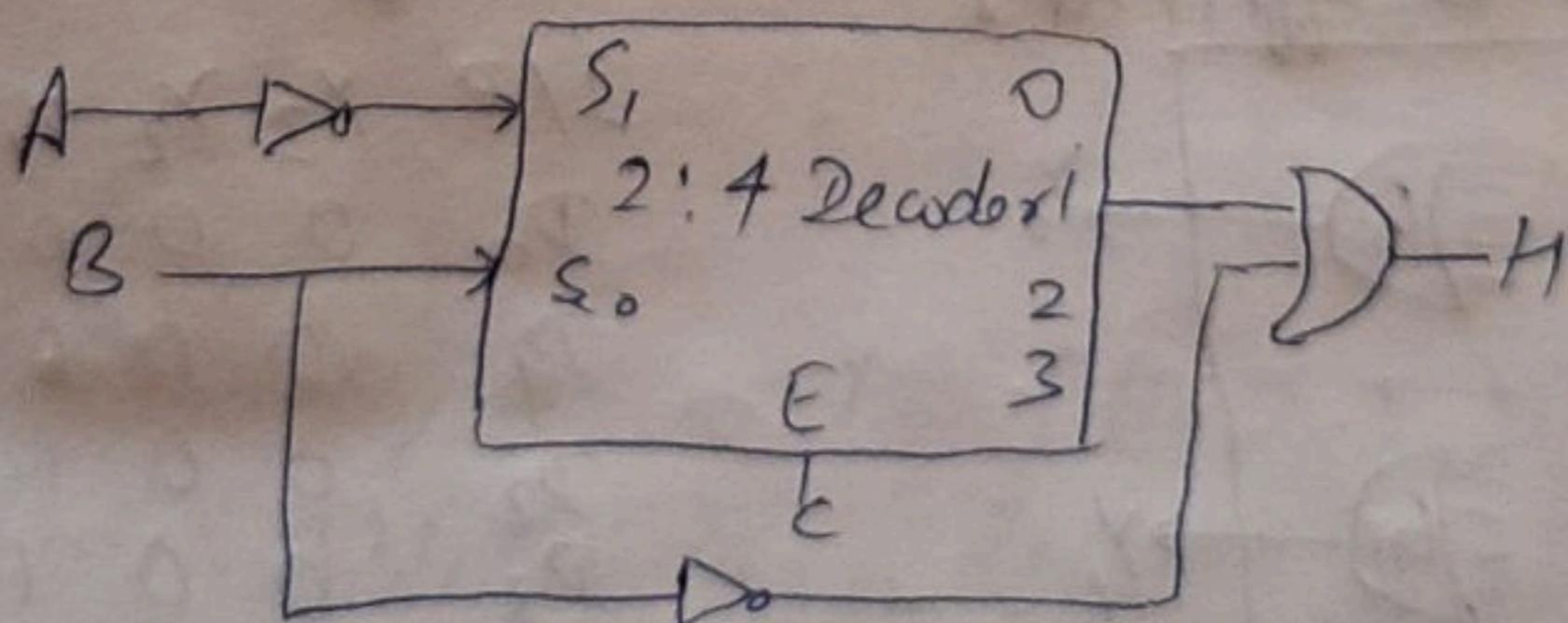


$$\text{Ans} \quad G = \sum m(0,1) = \bar{Y}_1 \bar{Y}_0 + \bar{Y}_1 Y_0 = \bar{Y}_1$$

= Complement of Maxterm 2

= Minterm 2 = $\bar{A}BC$

Q4. Given following ckt comprising a 2:4 decoder with normal O/Ps & one enable, what is simplified SOP expression of Boolean func. H in terms of A, B, C?



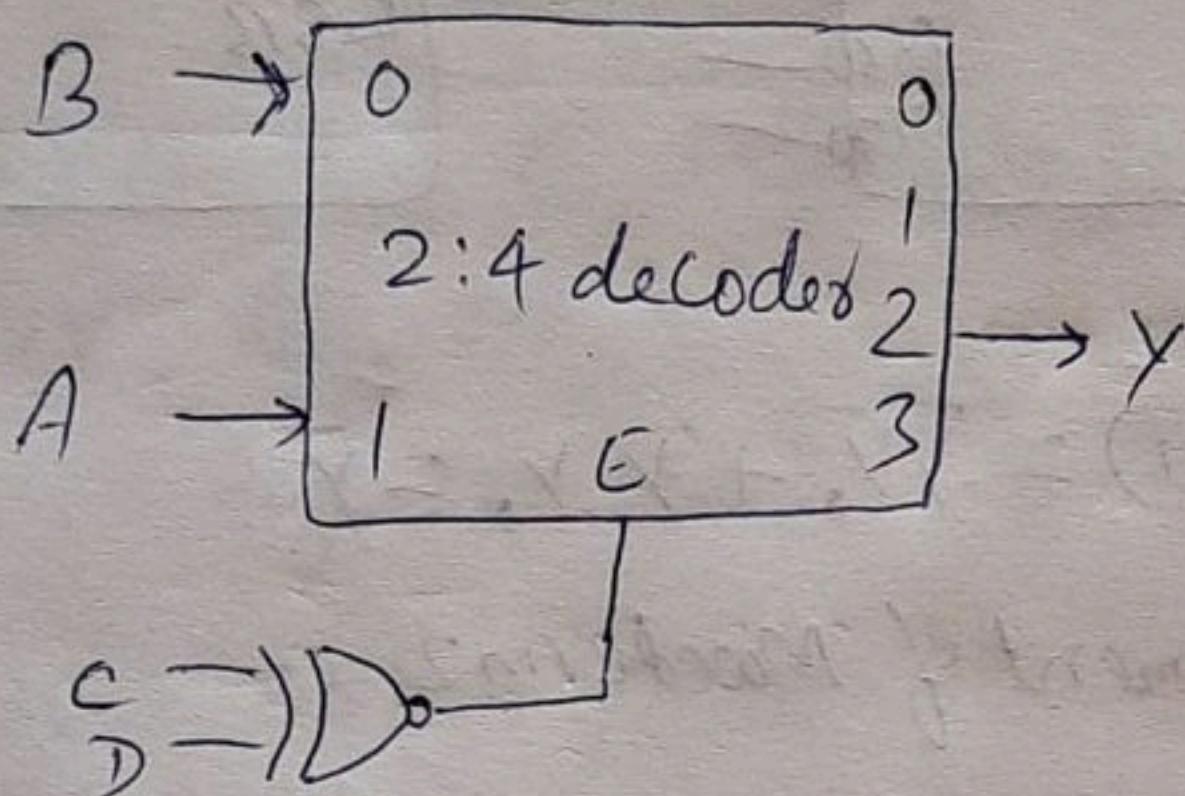
$$\begin{aligned} \text{Ans} \quad H &= (\bar{S}_1 \bar{S}_0)C + \bar{B} \\ &= ABC + \bar{B} \\ &= AC + \bar{B} \end{aligned}$$

Q5. Implement following function using 2:4 decoder with active high enable & active high o/p and only 1 logic gate

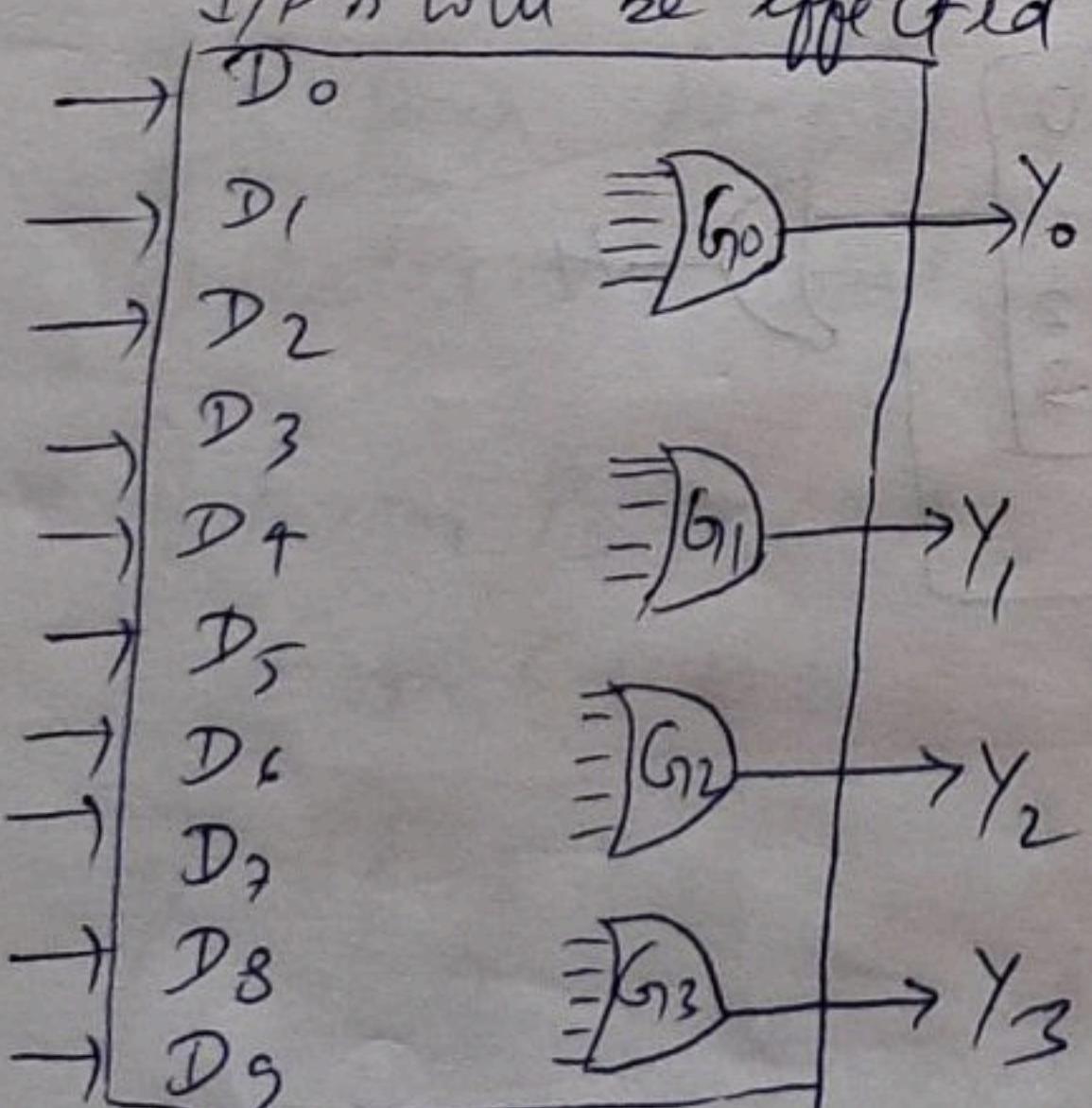
$$Y = F(A, B, C, D) = \sum m(8, 11)$$

Ans →

$$\begin{aligned} Y &= A\bar{B}\bar{C}\bar{D} + A\bar{B}CD \\ &= \underbrace{A\bar{B}}_{\text{minterm}} \underbrace{(C \oplus D)}_{\text{Enable}} \end{aligned}$$



Q6. Implement a ckrt for a 10:4 encoder (with D_0 to D_9 as I/P₁, and Y_0 to Y_3 as O/P₁, Y_3 being MSB) with 4 No. of OR gates as shown in below block. The I/P₁ for OR gates can be anything from D_0 to D_9 . If gate G_2 is faulty (stuck at 0) then which I/P₁ will be effected?



I/P	Y_3	Y_2	Y_1	Y_0
D_0	0	0	0	0
D_1	0	0	0	1
D_2	0	0	1	0
D_3	0	0	1	1
D_4	0	1	0	0
D_5	0	1	0	1
D_6	0	1	1	0
D_7	0	1	1	1
D_8	1	0	0	0
D_9	1	0	0	1

Ans → Gate Connected I/P₁

G_0 D_1, D_3, D_5, D_7, D_9

G_1 D_2, D_3, D_6, D_7

G_2 D_4, D_5, D_6, D_7

G_3 D_8, D_9

So if there is a fault in gate G_2 I/P₁ D_4, D_5, D_6 & D_7 will be effected.

Q7. A priority encoder is an encoder ckt with priority. If 2 or more I/Ps are equal to 1, the I/P with highest priority will take precedence. The truth table of 4 I/P priority encoder is shown below. An O/P V is added which is set to 1 when 1 or more I/Ps are equal to 1; otherwise V is 0. The 2 O/Ps X & Y are not impacted when V equals 0 & hence they are specified don't care O/Ps. Note where X's in O/P columns represent don't care O/Ps, the X's in the I/P columns are useful for representing a truth table in compact form.

For example I/P X100 represents 2 I/P combinations 0100 & 1100.

Derive simplified SOP expressions for X , Y & V & draw logic diagram.

Ans,

<u>I/Ps</u>	<u>O/Ps</u>	<u>Minterms</u>
D ₃ D ₂ D ₁ D ₀	X Y V	f(D ₀ D ₁ D ₂ D ₃)
0 0 0 0	X X 0	0
1 0 0 0	0 0 1	8
X 1 0 0	0 1 1	4, 12
X X 1 0	1 0 1	2, 6, 10, 14
X X X 1	1 1 1	1, 3, 5, 7, 9, 11, 13, 15

$$X = f(D_0, D_1, D_2, D_3) \oplus$$

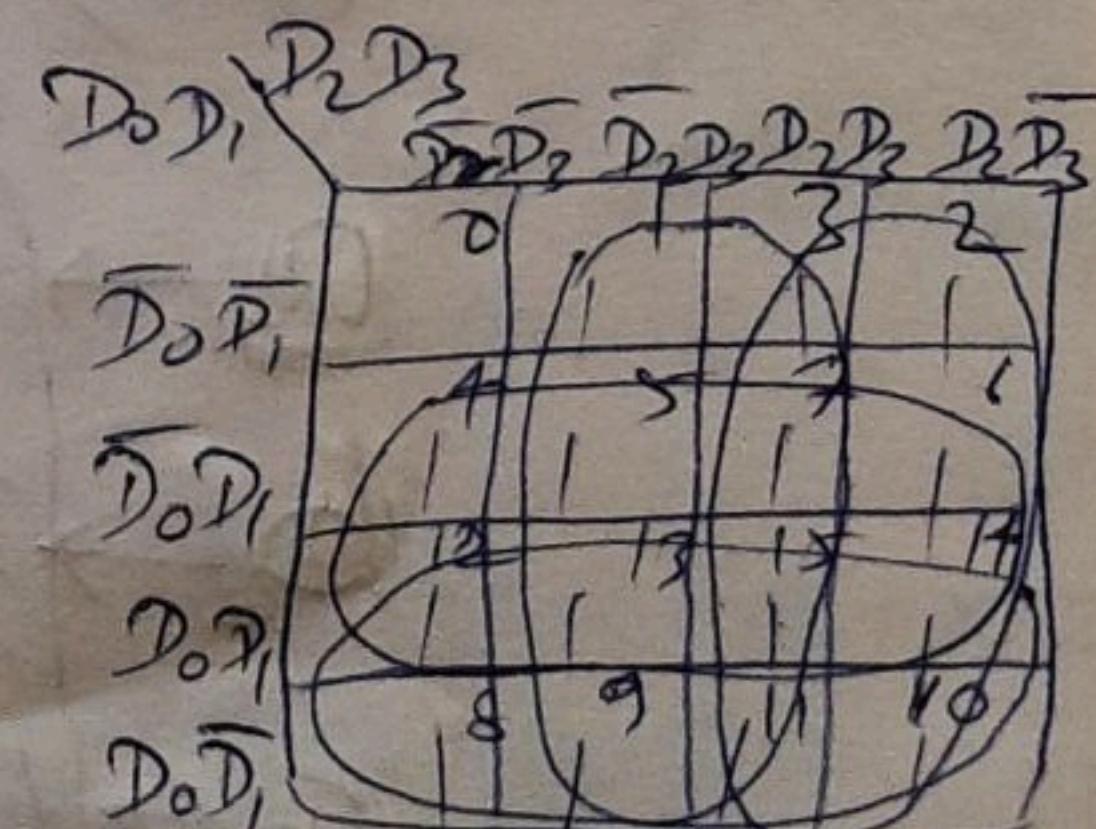
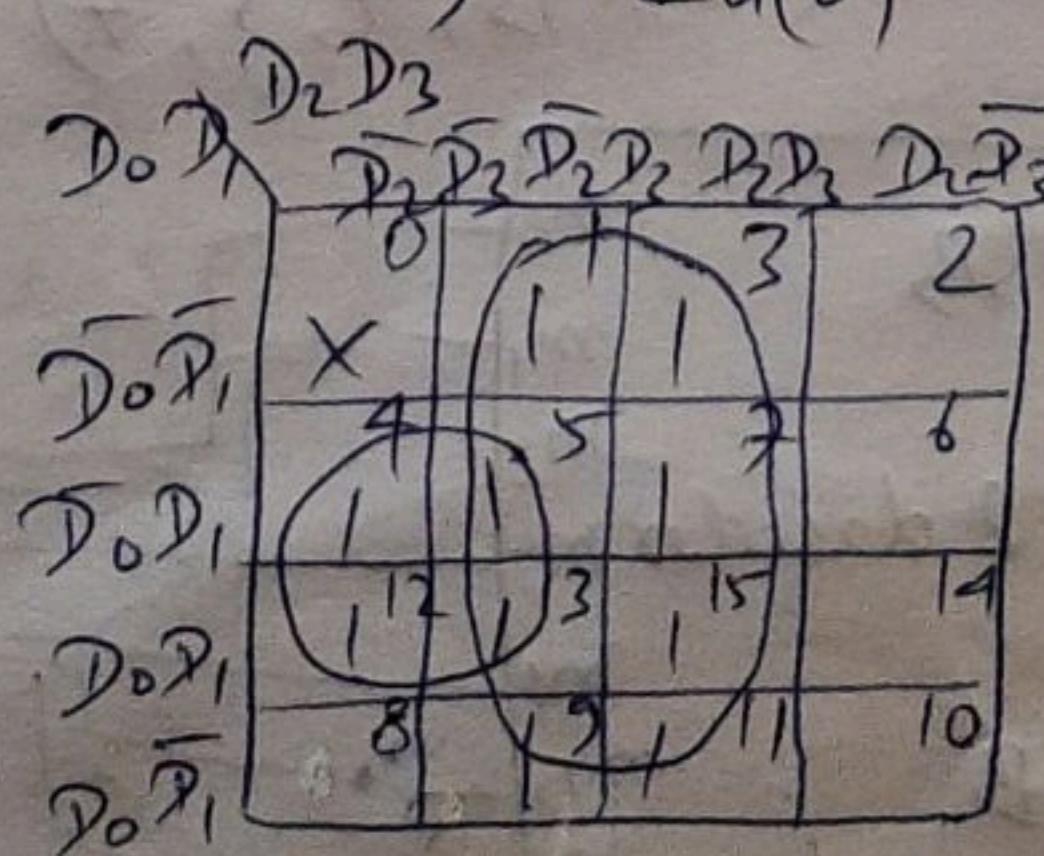
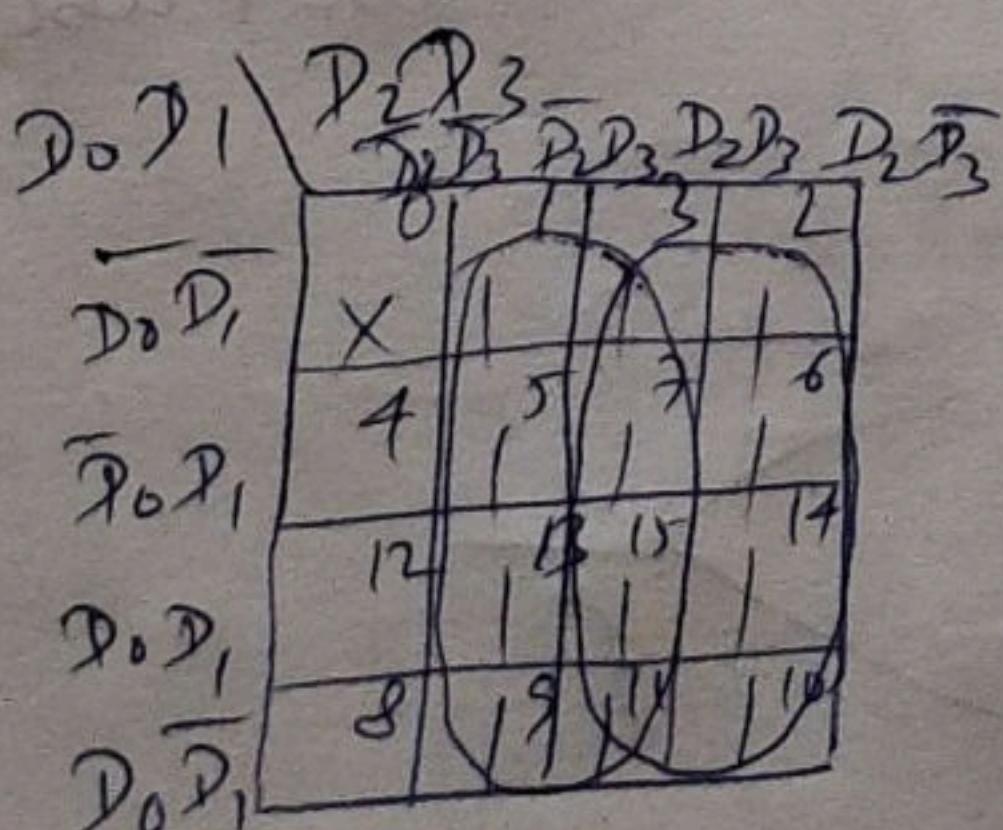
$$= \sum m(1, 2, 3, 5, 6, 7, 9, 10, 11, 13, 15)$$

$$Y = f(D_0, D_1, D_2, D_3)$$

$$= \sum m(1, 3, 4, 5, 7, 9, 11, 12, 13, 15)$$

$$V = f(D_0, D_1, D_2, D_3)$$

$$= \sum m(1, 3, 4, 5, 7, 9, 11, 12, 13, 15)$$



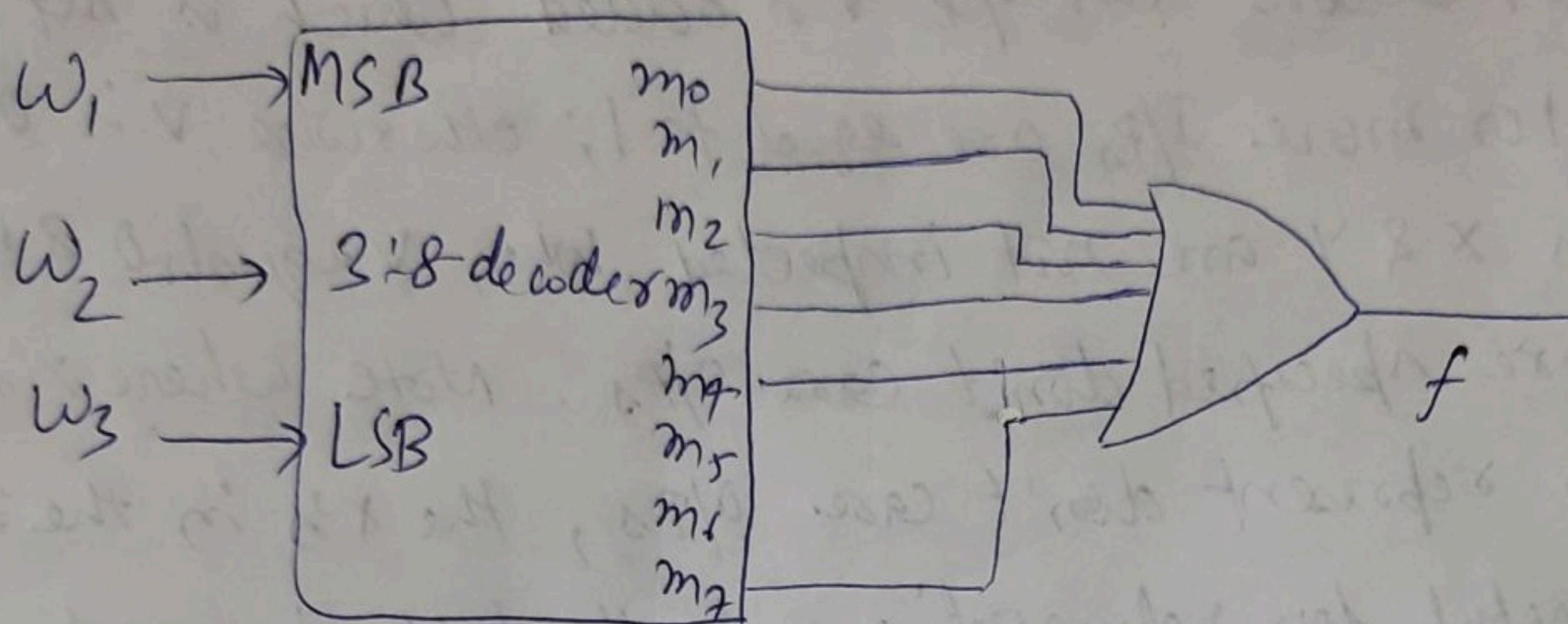
$$X = D_3 + D_2$$

$$Y = D_3 + D_1 \bar{D}_2$$

$$V = D_3 + D_2 + D_1 + D_0$$

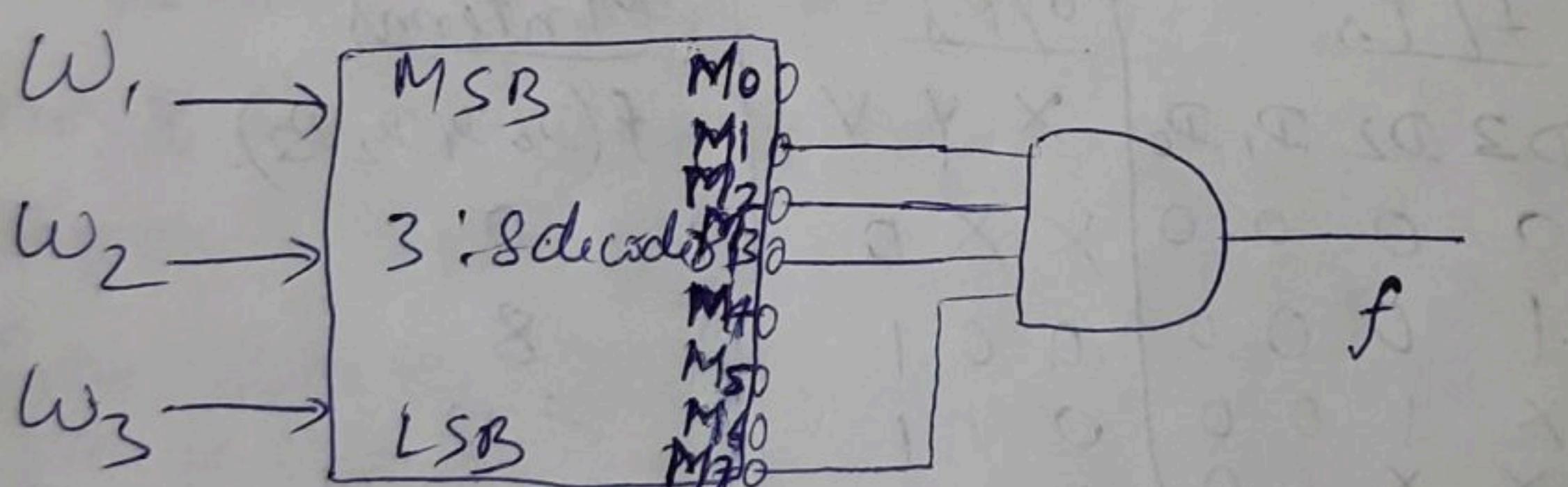
Q 8. Implement

a) $f(w_1, w_2, w_3) = \sum m(0, 1, 2, 3, 4, 7)$ using 3-8 decoder & OR gate



b) $f(w_1, w_2, w_3) = \sum m(0, 4, 5, 6)$ using 3-8 decoder & AND gate

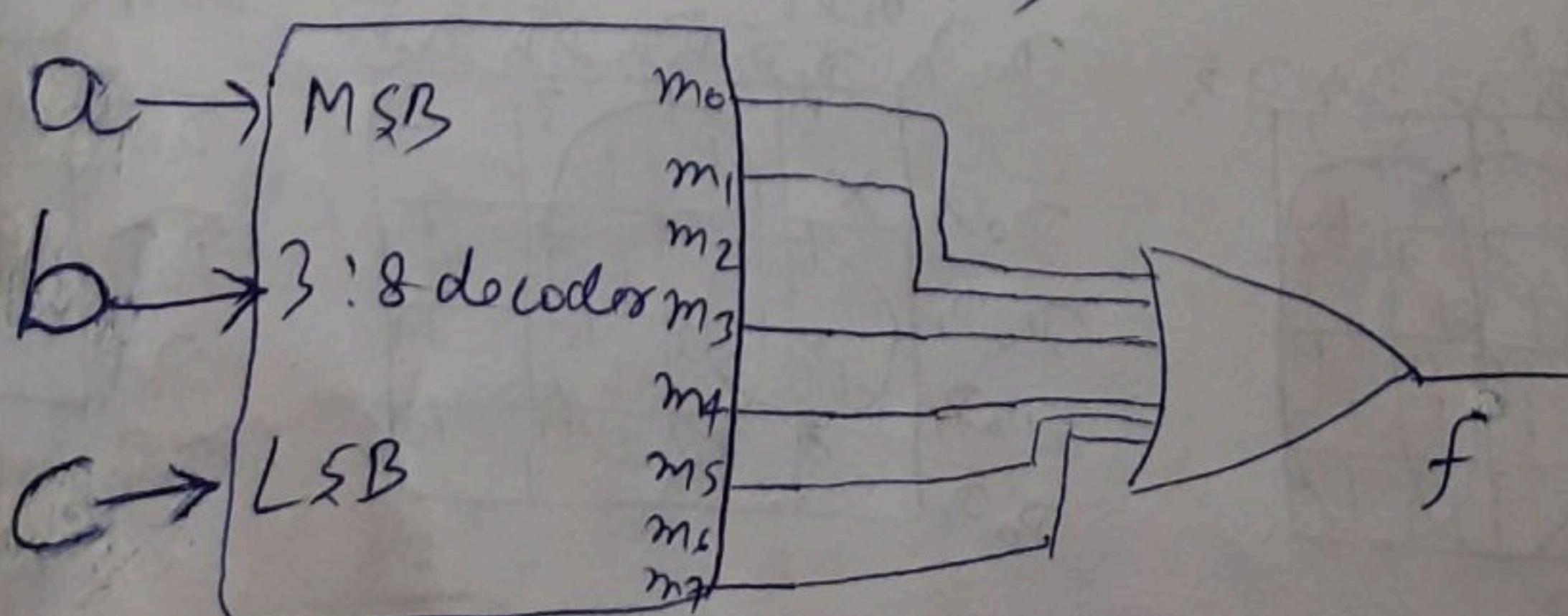
$$f(w_1, w_2, w_3) = \overline{\oplus} \prod M(1, 2, 3, 7)$$



c) $f(a, b, c) = \bar{b} + c$ using 3:8 decoder & OR gate

$$= (a + \bar{a})\bar{b}(c + \bar{c}) + (a + \bar{a})(b + \bar{b}) + c = a\bar{b}c + \bar{a}\bar{b}c + a\bar{b}\bar{c} + \bar{a}bc$$

$$f(a, b, c) = \sum m(0, 1, 3, 4, 5, 7) + ab\bar{c} + a\bar{b}\bar{c} + \bar{a}bc + \bar{a}\bar{b}c$$



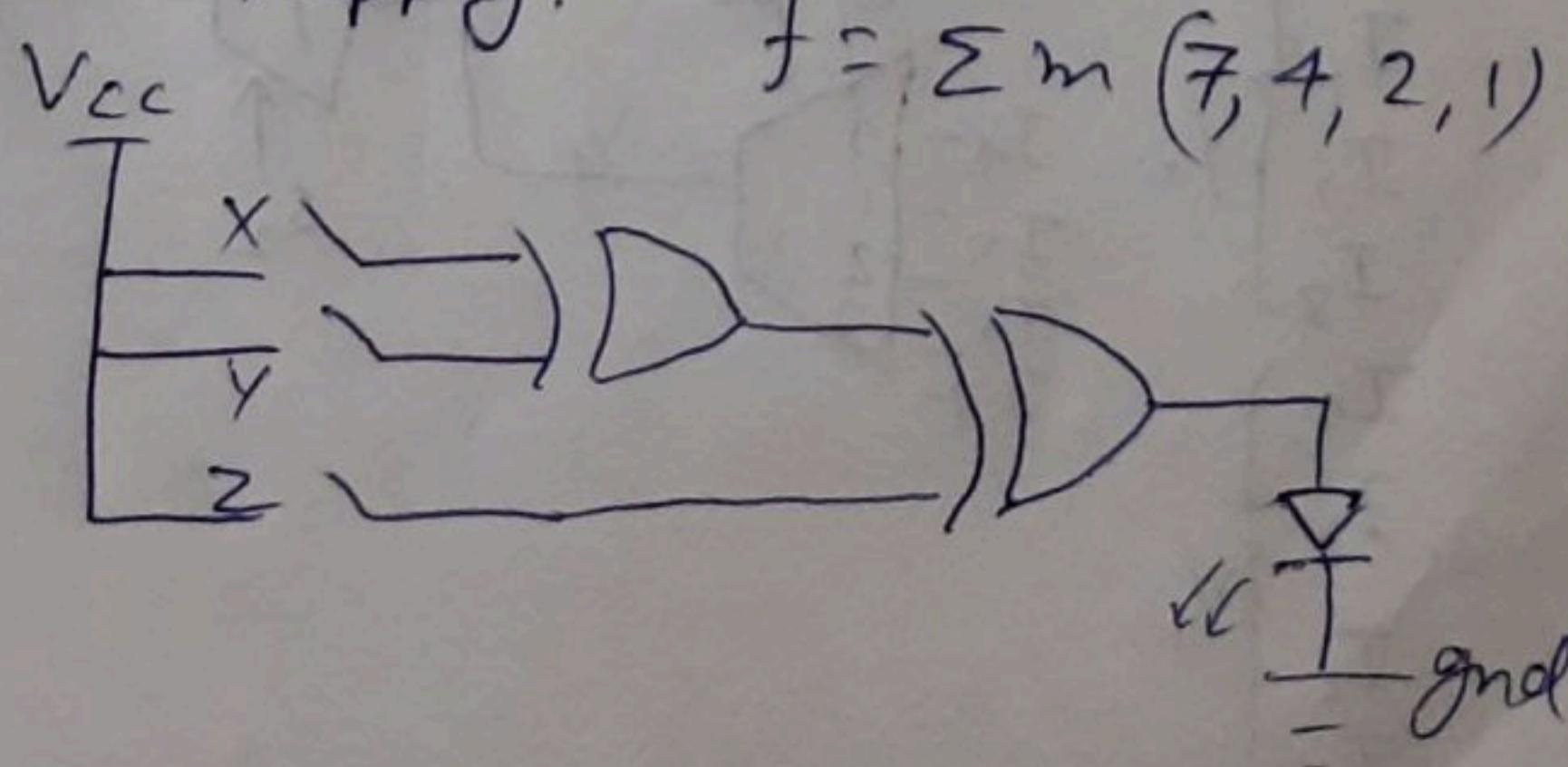
Q3. Resigned at last to be banned from island, you now turn your attention to American Idol, where judges are in dire need of some digital assistance to resolve issues concerning which contestant should be allowed to remain in vocal competition. After watching program for several hundred hours, you determine following "vote encoding": (Note that pairs of like votes appear to cancel each other).

Randy X	Paula Y	Simon Z	Contestant Stays
1	1	1	Yes
1	0	0	Yes
0	1	0	Yes
0	0	1	Yes
1	1	0	No
0	1	1	No
1	0	1	No
0	0	0	No

Of course above table doesn't make sense but neither do most of judges on the show

- a) In an interesting twist, you are asked to implement this circuit using only 2 I/P XOR gates (74x86 chips), a breadboard, some wires, some SPST switches, an LED, resistors & a power supply.

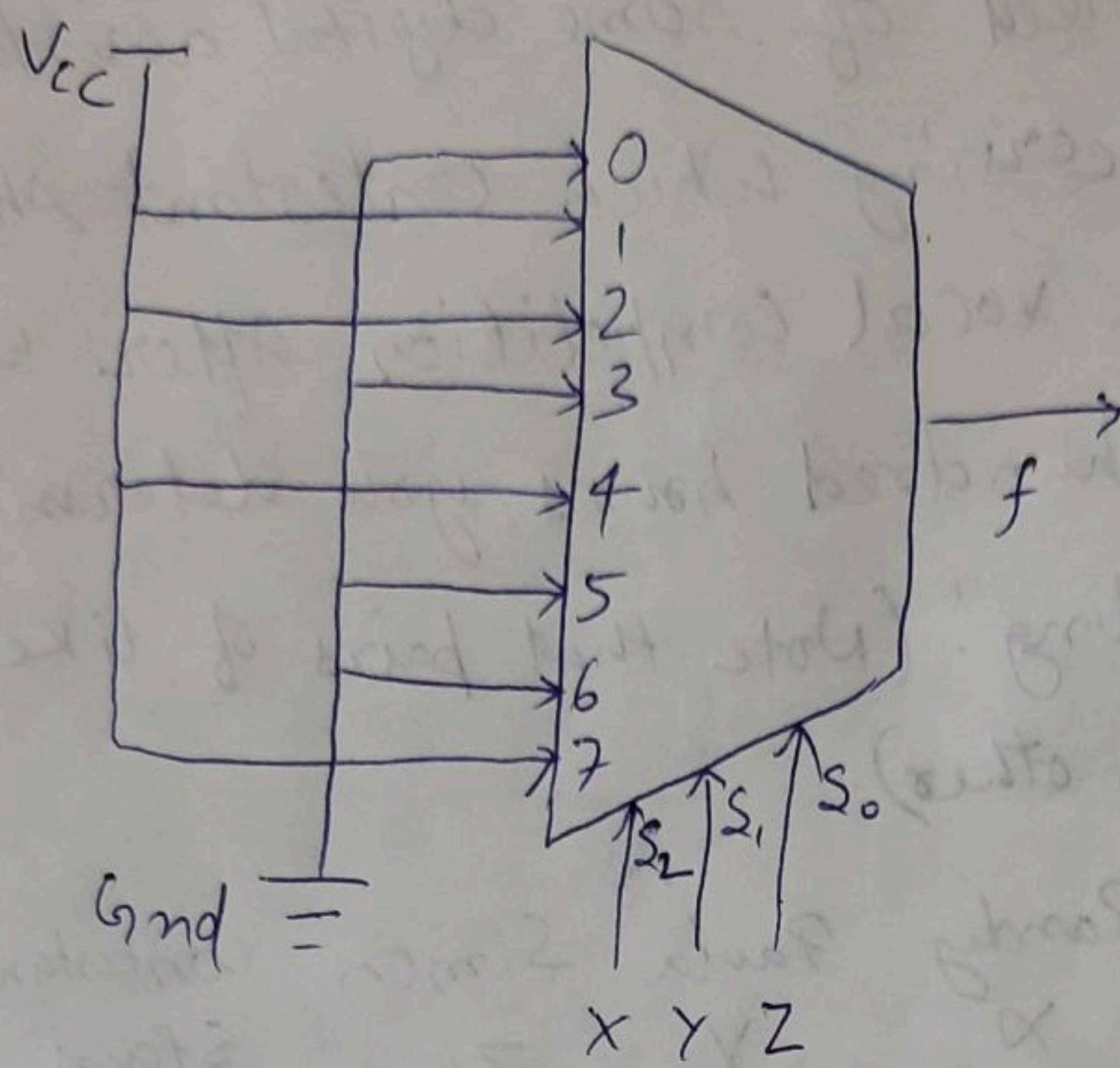
Ans →



$$\begin{aligned}
 f = \sum m(7, 4, 2, 1) &= \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z} + xy\bar{z} \\
 &= \bar{x}(y \oplus z) + x(\bar{y} \oplus z) \\
 &= \bar{x} \times \oplus y \oplus z
 \end{aligned}$$

b) Implement the above using multiplexer.

Ans $\rightarrow f(x,y,z) = \sum m(7,4,2,1)$

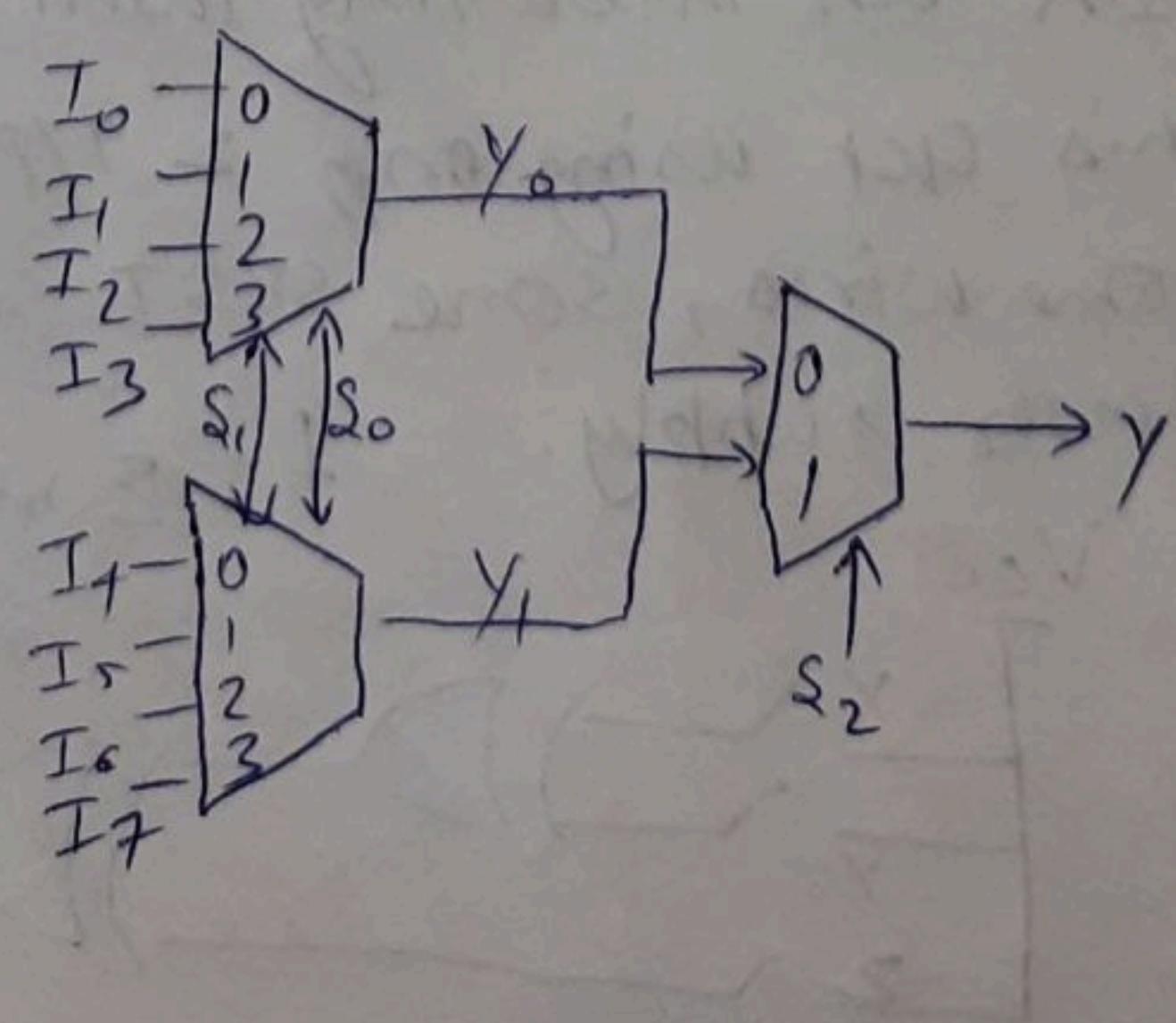


c) Finally Compare & Contrast the logic circuit realization which would be easier to build? which would use fewer parts/wires? which would be easier to modify?

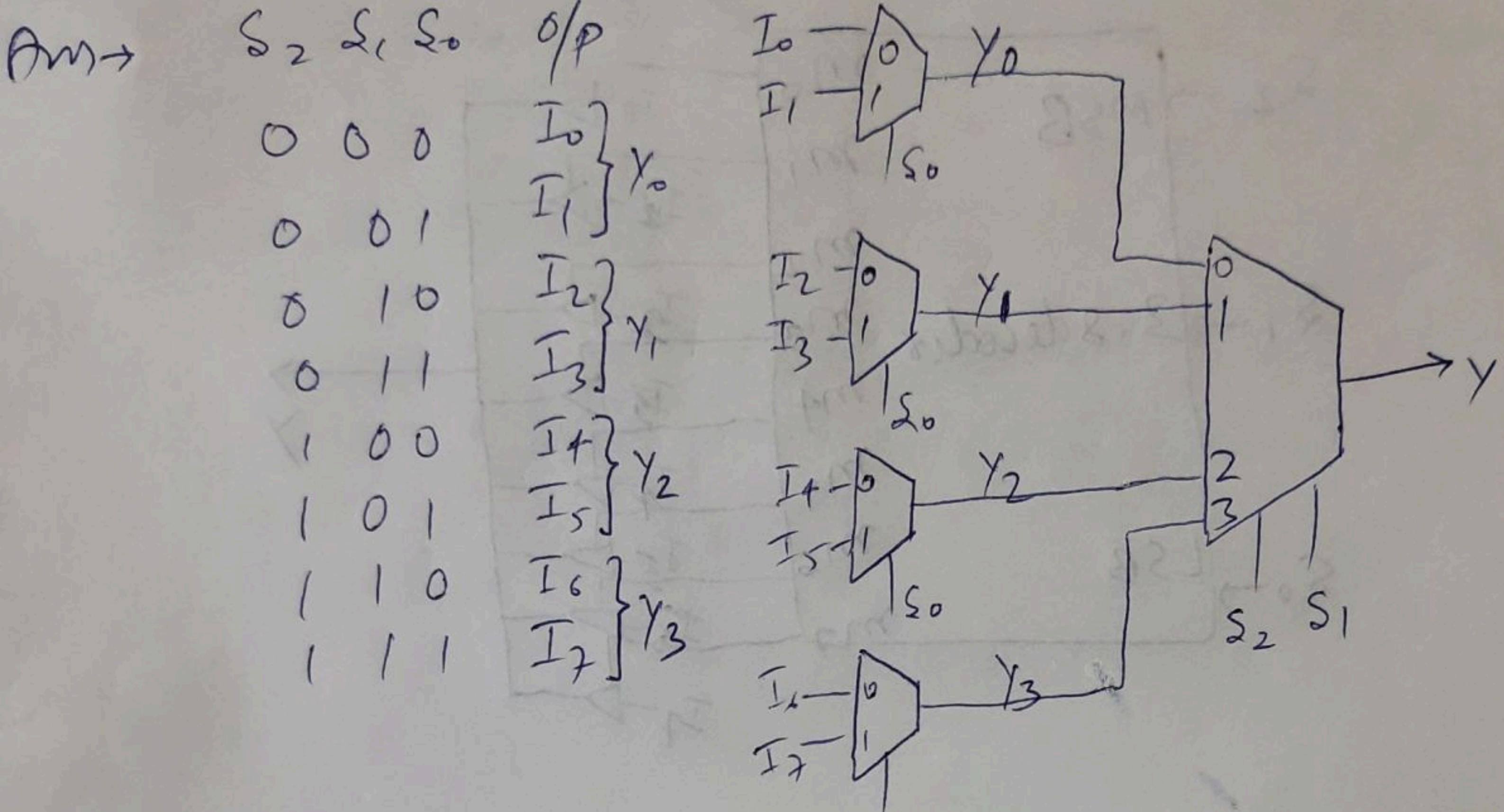
Ans \rightarrow Multiplexers implementation is reliable as combinations can be changed/modified very easily. But XOR is easier to build & has less wiring cost.

Q10. Show how to make an 8:1 MUX using 2 No. of 4:1 MUX & 1 no. of 2:1 MUX.

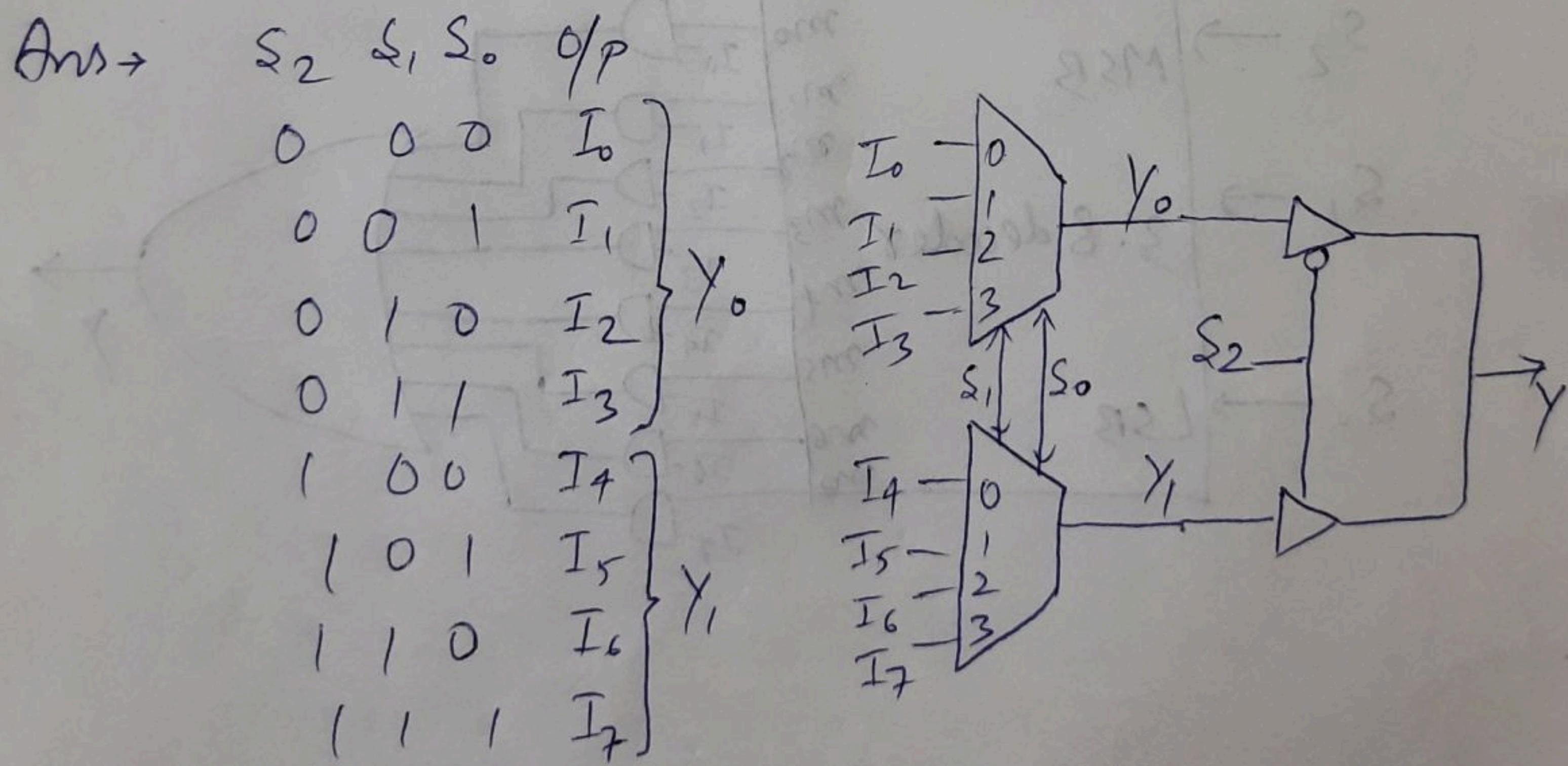
$S_2\ S_1\ S_0$	O/P
0 0 0	I_0
0 0 1	I_1
0 1 0	I_2
0 1 1	I_3
1 0 0	I_4
1 0 1	I_5
1 1 0	I_6
1 1 1	I_7



Q11. Show how to make an 8:1 MUX using 1 No. of 4:1 MUX & 4 Nos. of 2:1 MUX.

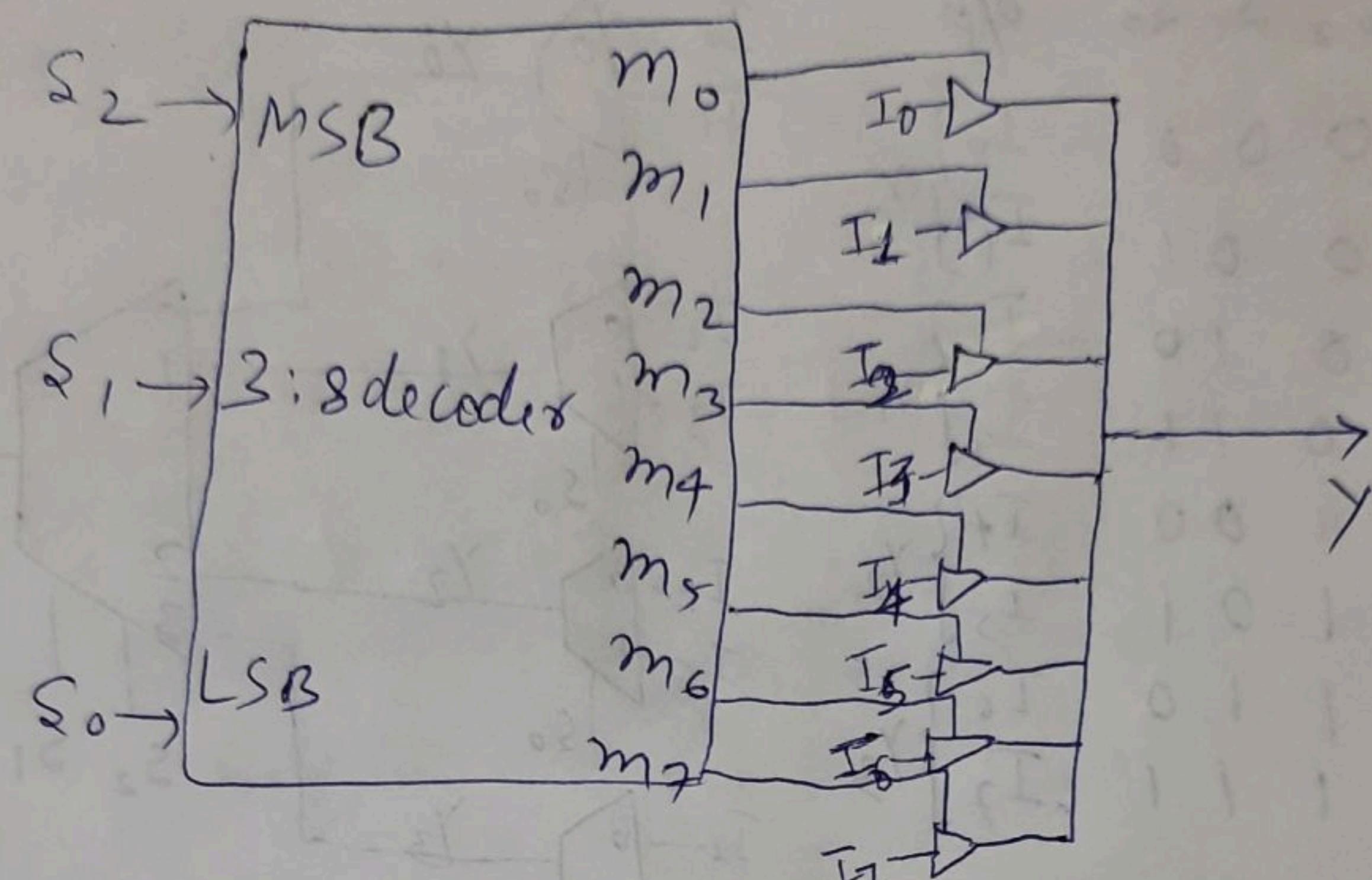


Q12. Show how to make an 8:1 MUX using 2 No. of 4:1 MUX & 2 No. of tristate buffers.



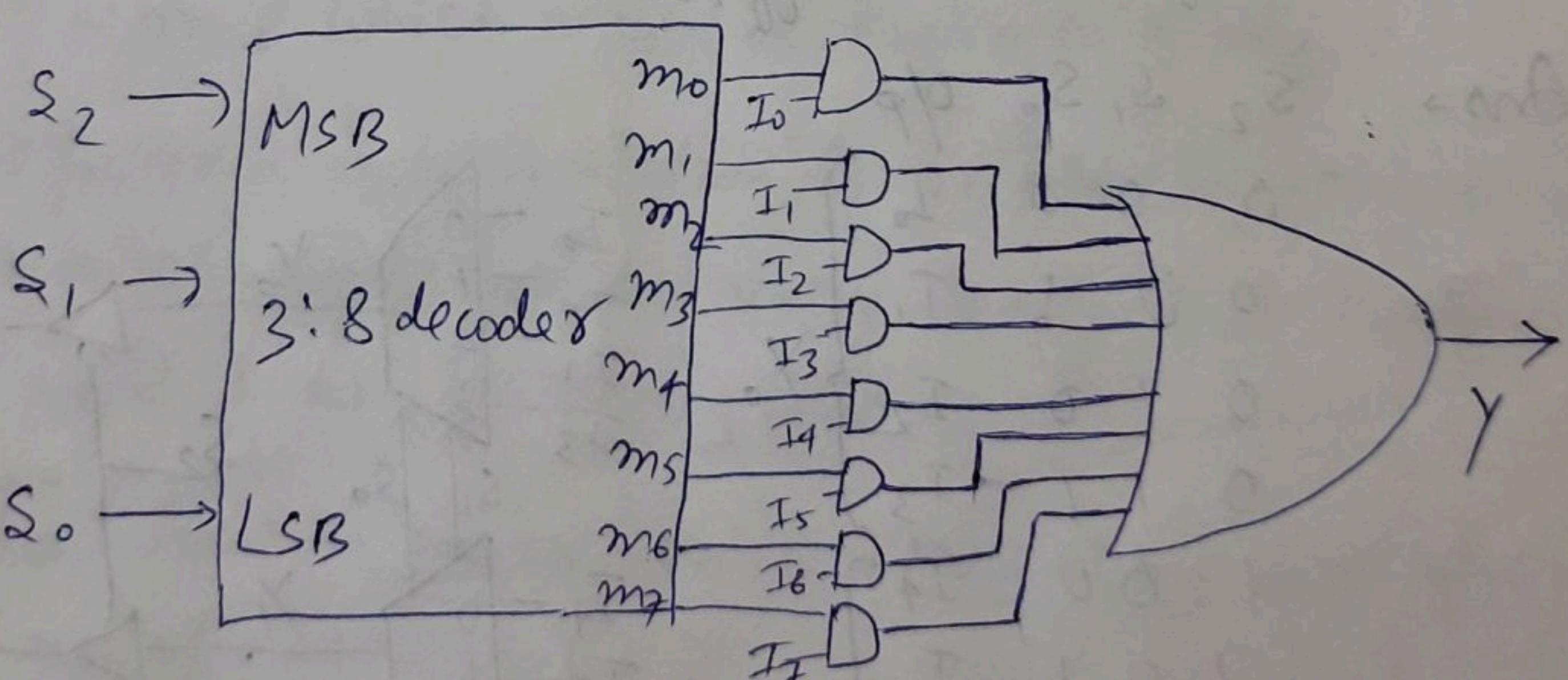
Q13. Show, how to make an 8:1 MUX using a 3:8 decoder and tristate buffers.

Ans →



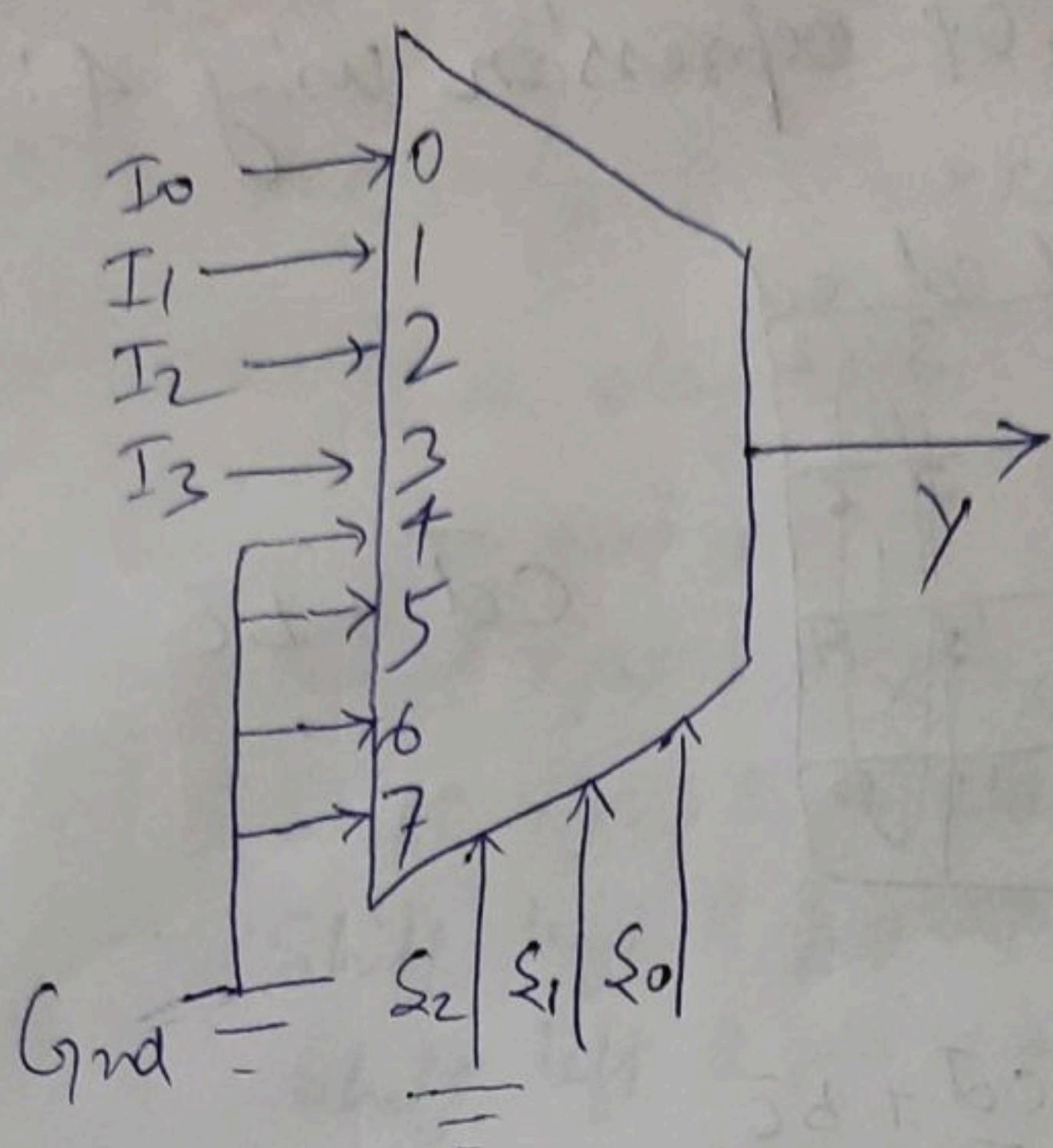
Q14. Show, how to make an 8:1 MUX using a 3:8 decoder and few logic gates.

Ans →



Q15. Show, how to make use 8:1 MUX to make 4:1 MUX.

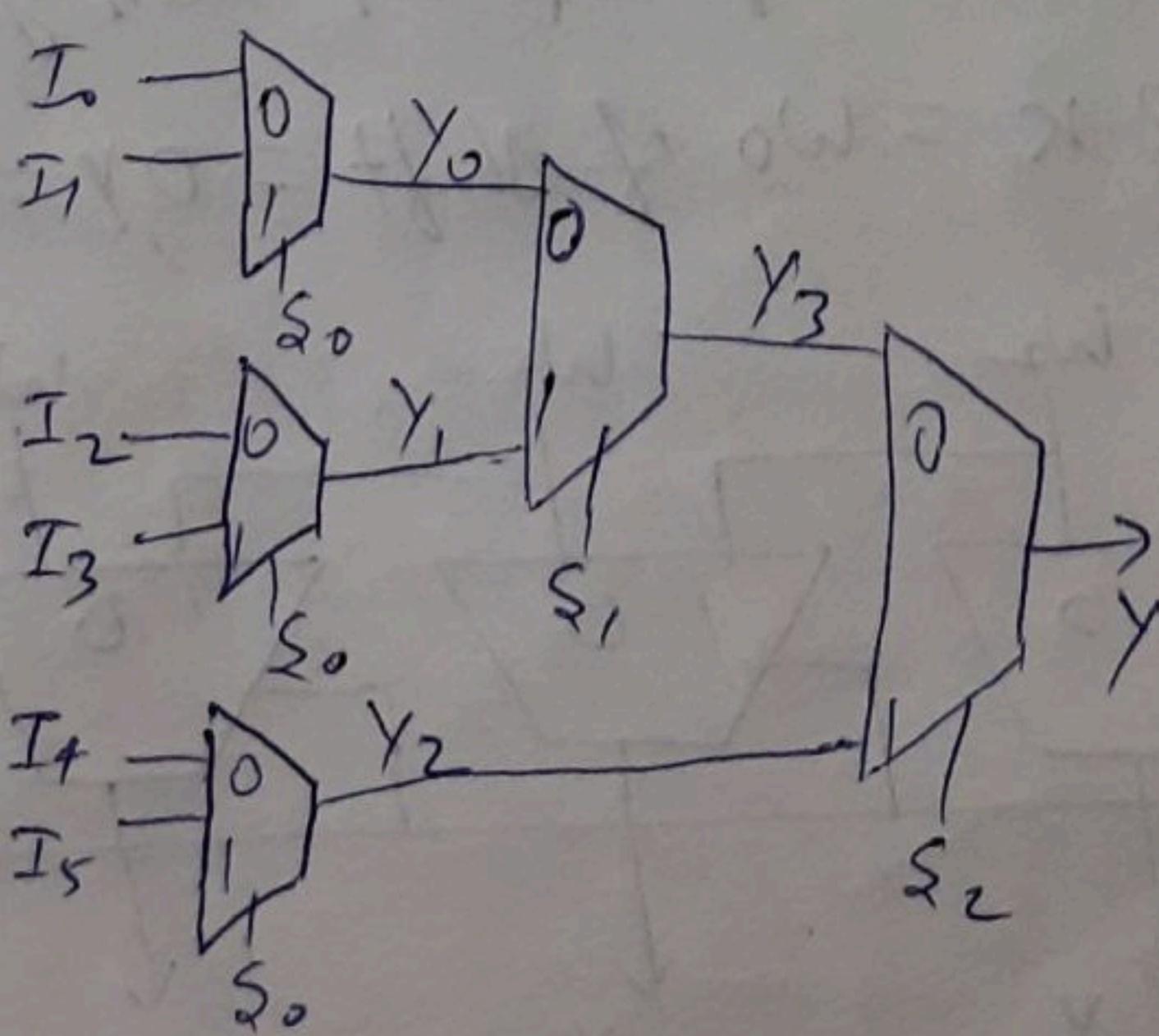
Ans →



Q16. Design a 6:1 multiplexer using 2:1 multiplexers.

Ans →

S_2	S_1	S_0	O/P
0	0	0	$I_0 \} Y_0 \}$
0	0	1	$I_1 \} Y_0 \}$
0	1	0	$I_2 \} Y_1 \}$
0	1	1	$I_3 \} Y_1 \}$
1	0	0	$I_4 \} Y_2 \}$
1	0	1	$I_5 \} Y_2 \}$



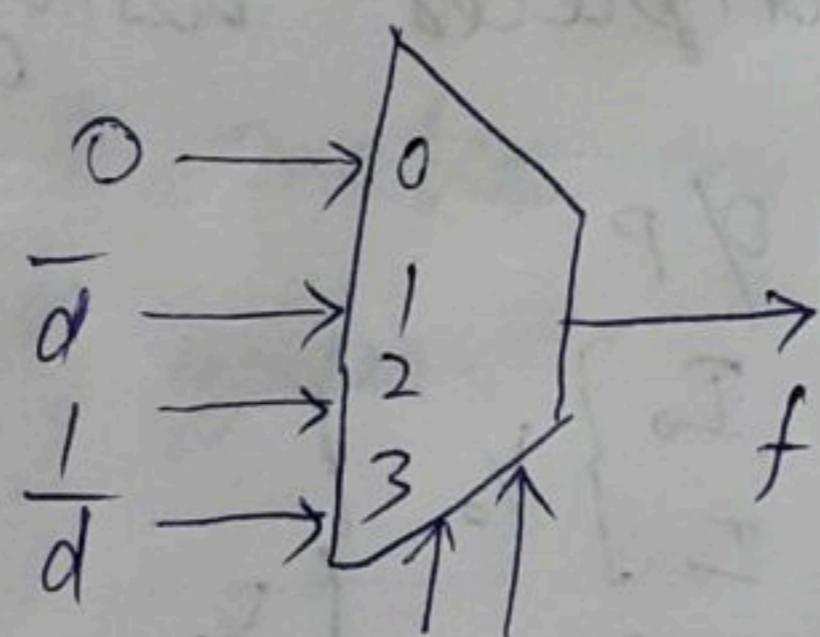
Q17. Simplify $f(a, b, c, d) = \sum m(2, 4, 5, 6, 10) + D(12, 13, 14, 15)$
 & implement SOP expression using 4:1 MUX.

Ans →

ab\cd	$\bar{c}\bar{d}$	$\bar{c}d$	$c\bar{d}$	cd
$\bar{a}\bar{b}$	0	1	3	2
$\bar{a}b$	4	5	7	6
$a\bar{b}$	X	X	X	X
ab	8	3	11	10

$$cd + b\bar{c}$$

$$\begin{aligned} f(a, b, c, d) &= cd + b\bar{c} \\ &= \bar{b}c\bar{d} + bc\bar{d} + b\bar{c}(1) + \bar{b}\bar{c}(0) \end{aligned}$$

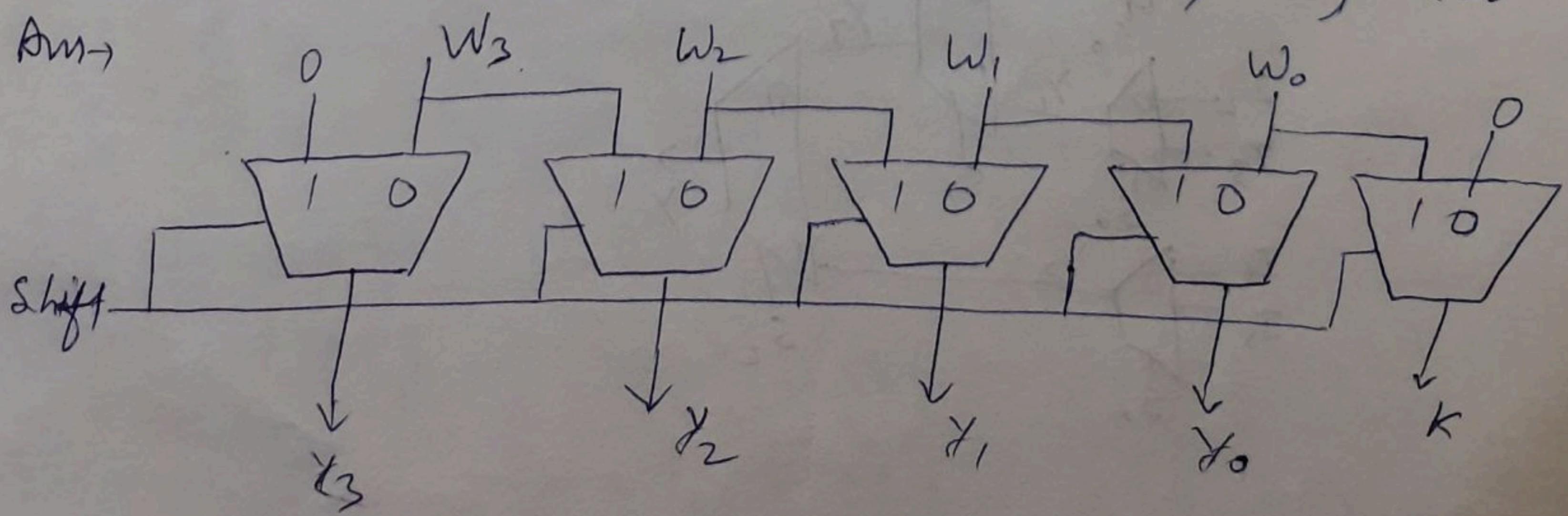


Q18. Design a ckt. that can shift a 4 bit vector $w = w_3 w_2 w_1 w_0$

1 bit position to right when a control signal shift is equal to 1. Let O/P of ckt be 4 bit vector $y = y_3 y_2 y_1 y_0$

2 signal K such that if shift = 1 then $y_3 = 0, y_2 = w_3, y_1 = w_2, y_0 = w_1$, & $K = w_0$ if shift = 0, $y = w$, & $K = 0$

Ans →

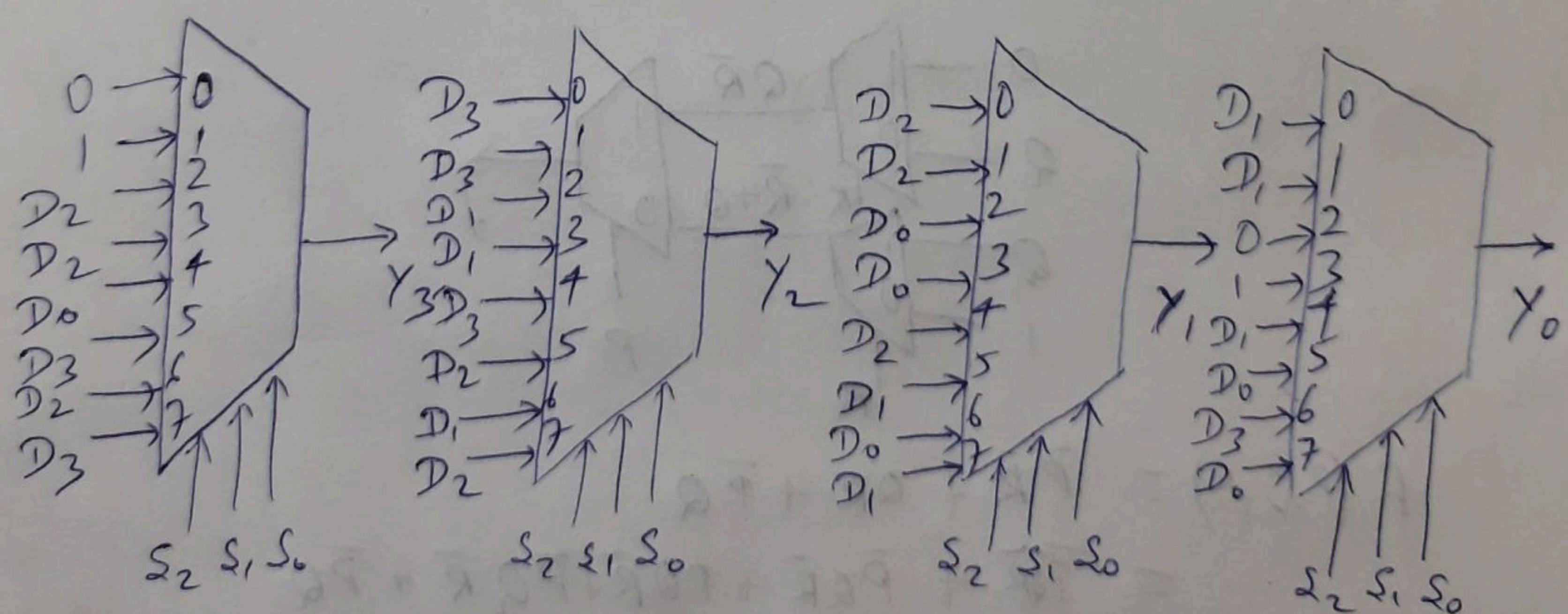


Q19. Implement a ckt with control I/Ps (S_2, S_1, S_0) & data I/Ps (D_3, D_2, D_1, D_0 where D_3 being MSB) & 4 O/Ps (Y_3, Y_2, Y_1, Y_0 where Y_3 being MSB). Use only 8:1 Muxes for implementation.

The functionality is described in below table.

Ans →

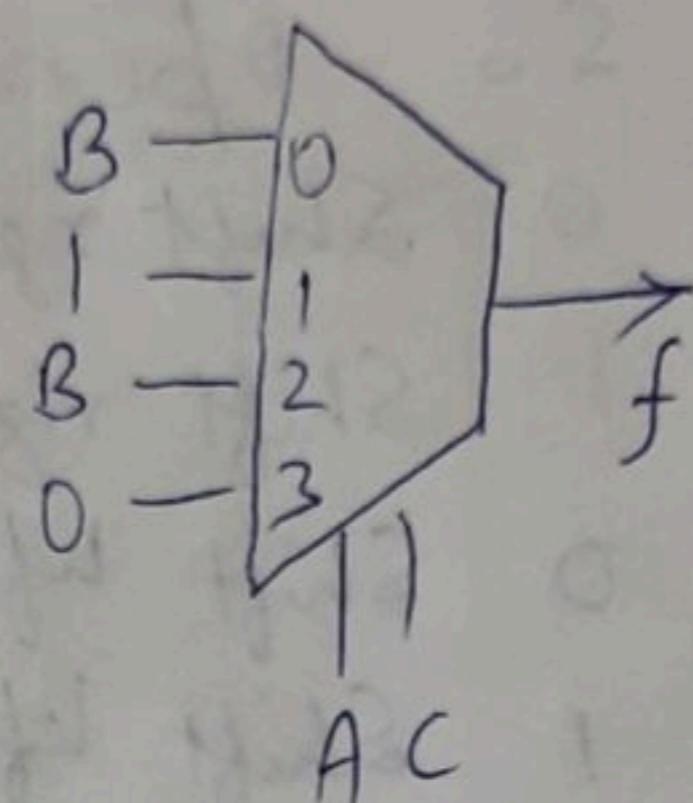
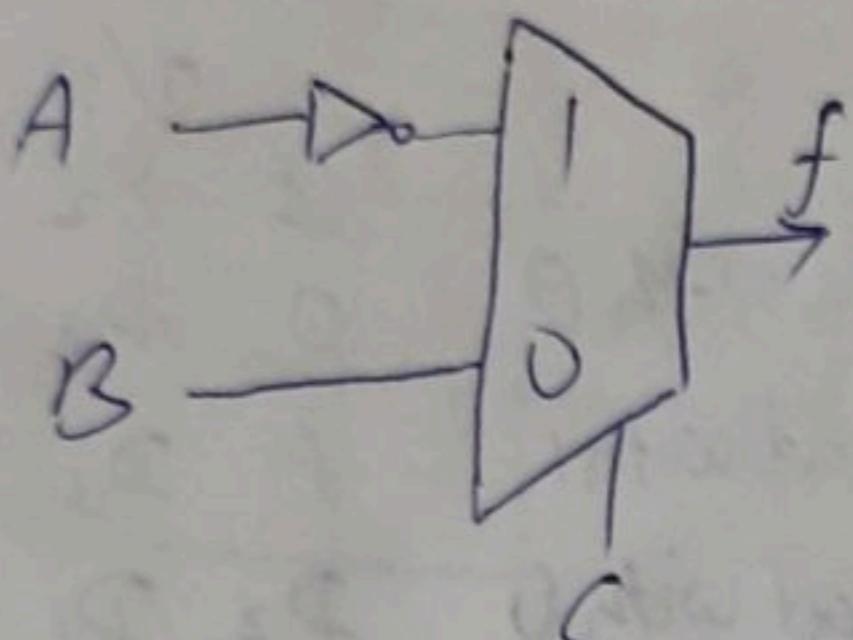
S_2	S_1	S_0	Operation	Y_3	Y_2	Y_1	Y_0
0	0	0	Shift right & pad with 0	0	D_3	D_2	D_1
0	0	1	Shift right & pad with 1	1	D_3	D_2	D_1
0	1	0	Shift left & pad with 0	D_2	D_1	D_0	0
0	1	1	Shift left & pad with 1	D_2	D_1	D_0	1
1	0	0	Rotate right	D_0	D_3	D_2	D_1
1	0	1	pass through	D_3	D_2	D_1	D_0
1	1	0	Rotate left	D_2	D_1	D_0	D_3
1	1	1	pass through	D_3	D_2	D_1	D_0



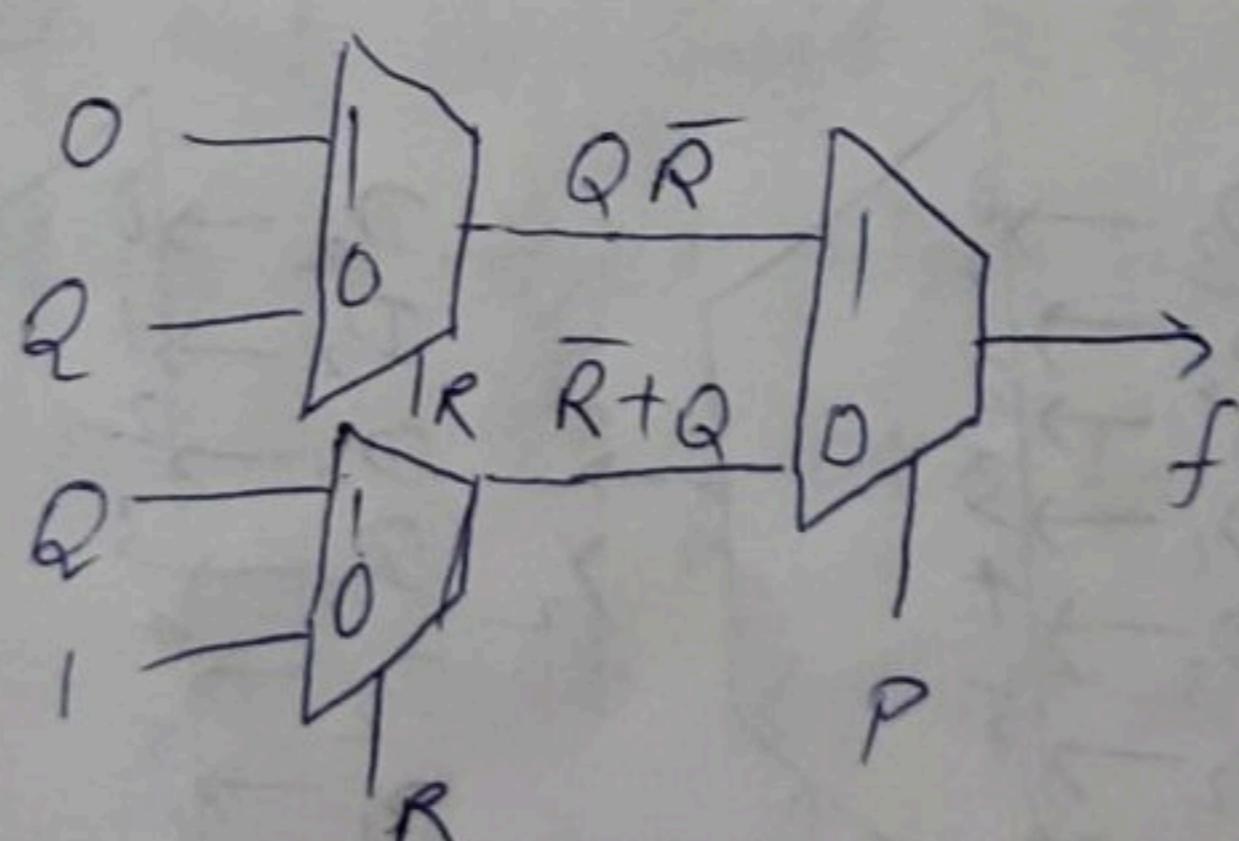
Q 20. Implement following functions using

i) 2:1 MUX & NOT gates ii) 4:1 MUX

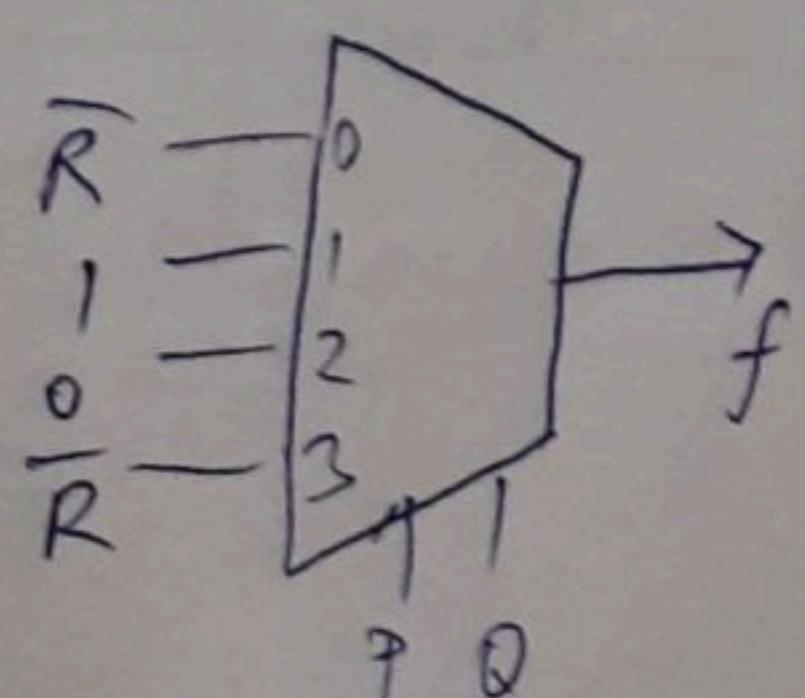
9) $F(A, B, C) = \bar{A}C + BC = \bar{A}C(1) + \bar{A}BC + ABC$



$$\begin{aligned} b) F(P, Q, R) &= \bar{P}\bar{R} + QR + \bar{P}Q \\ &= \bar{P}\bar{R} + \bar{P}QR\bar{R} + PQR\bar{R} + \bar{P}Q \\ &= \bar{P}(\bar{R} + QR + Q) + PQR\bar{R} \\ &= \bar{P}(\bar{R} + Q) + PQR\bar{R} \end{aligned}$$

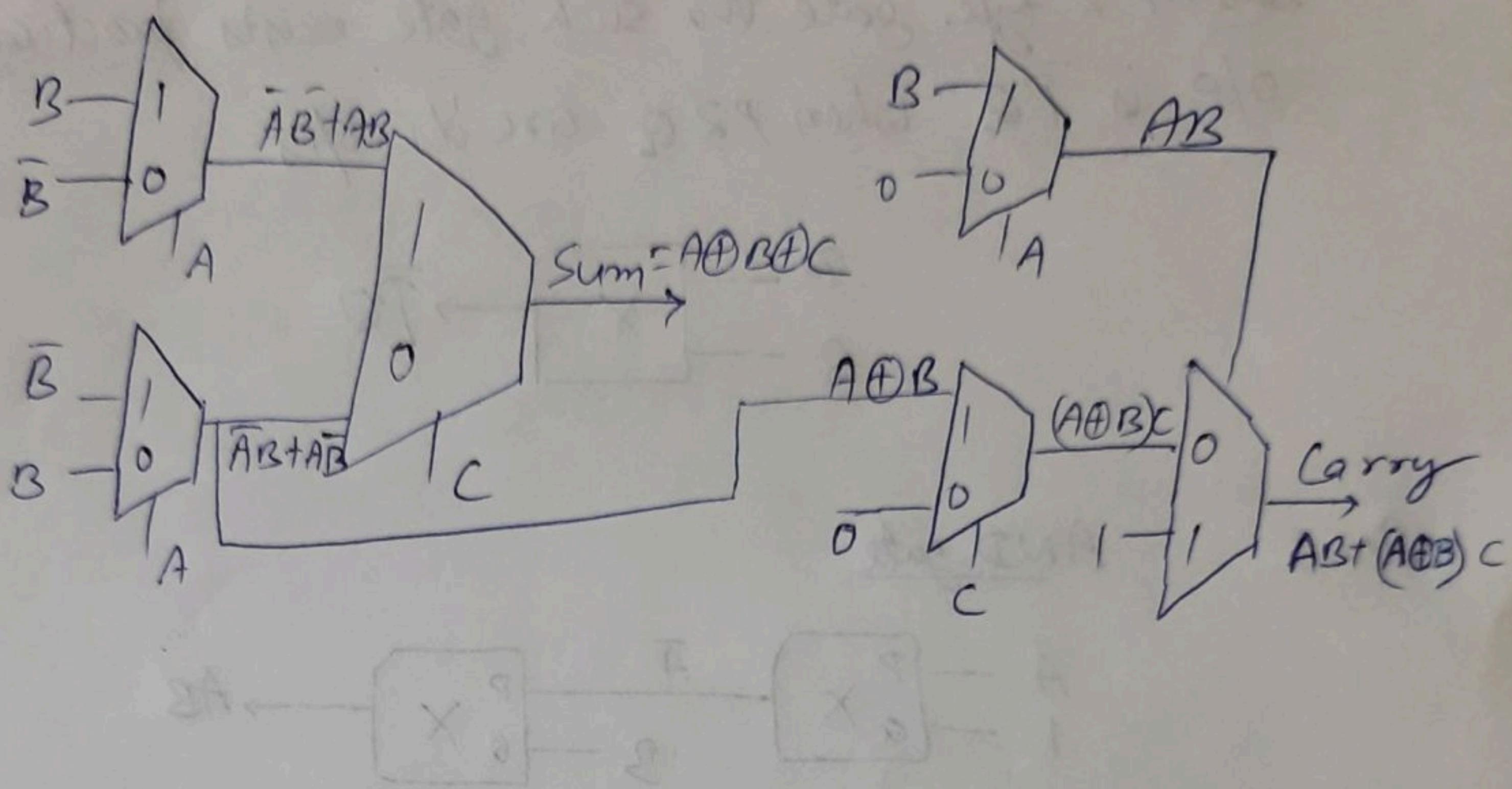


$$\begin{aligned} F(P, Q, R) &= \bar{P}\bar{R} + QR + \bar{P}Q \\ &= \bar{P}\bar{Q}\bar{R} + \bar{P}Q\bar{R} + PQR\bar{R} + \bar{P}Q\bar{R} + \bar{P}Q \\ &= \bar{P}\bar{Q}\bar{R} + \bar{P}Q\bar{R} + PQR\bar{R} + \bar{P}Q(1) + P\bar{Q}(0) \\ &= \bar{P}\bar{Q}\bar{R} + \bar{P}Q(1) + P\bar{Q}(0) + PQR\bar{R} \end{aligned}$$



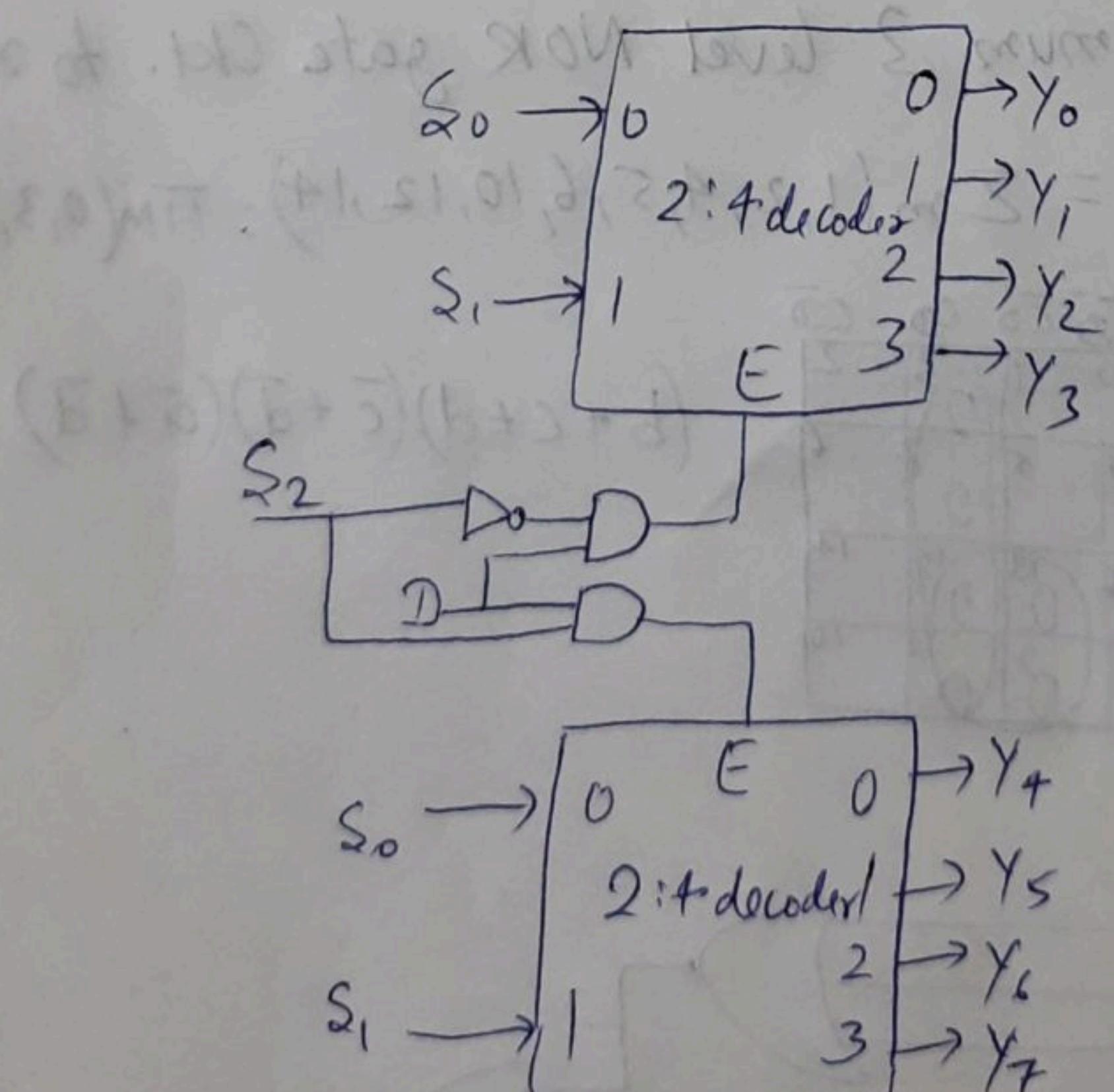
Q21. Implement the functionality of full adder using 2:1 mux only.

Ans →

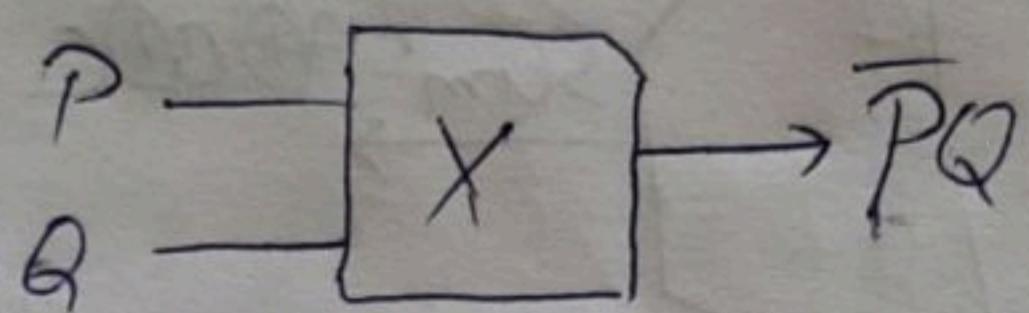


Q22. Implement functionality of 1:8 Demux using 2 No. of 2:4 decoders with enable I/Ps & few other logic gates (max^m of 3 gates)

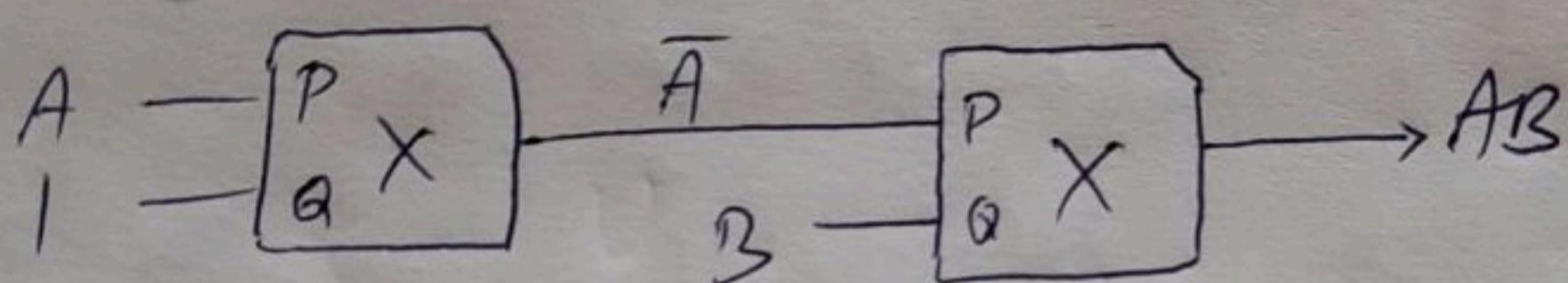
Ans →



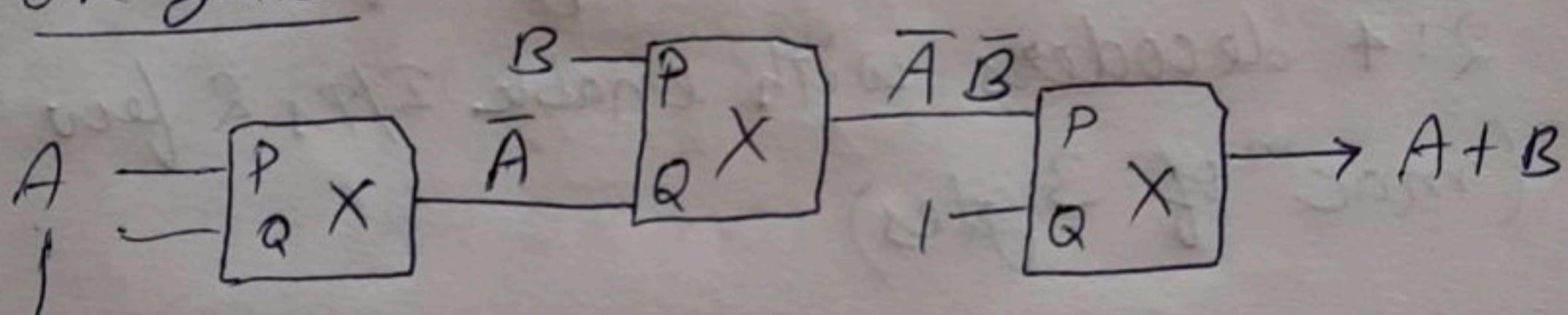
Q23. Implement AND gate & OR gate using below shown X type gate (No such gate exists practically) whose O/P is \overline{PQ} when PQ are its I/Ps.



Ans → AND gate



OR gate

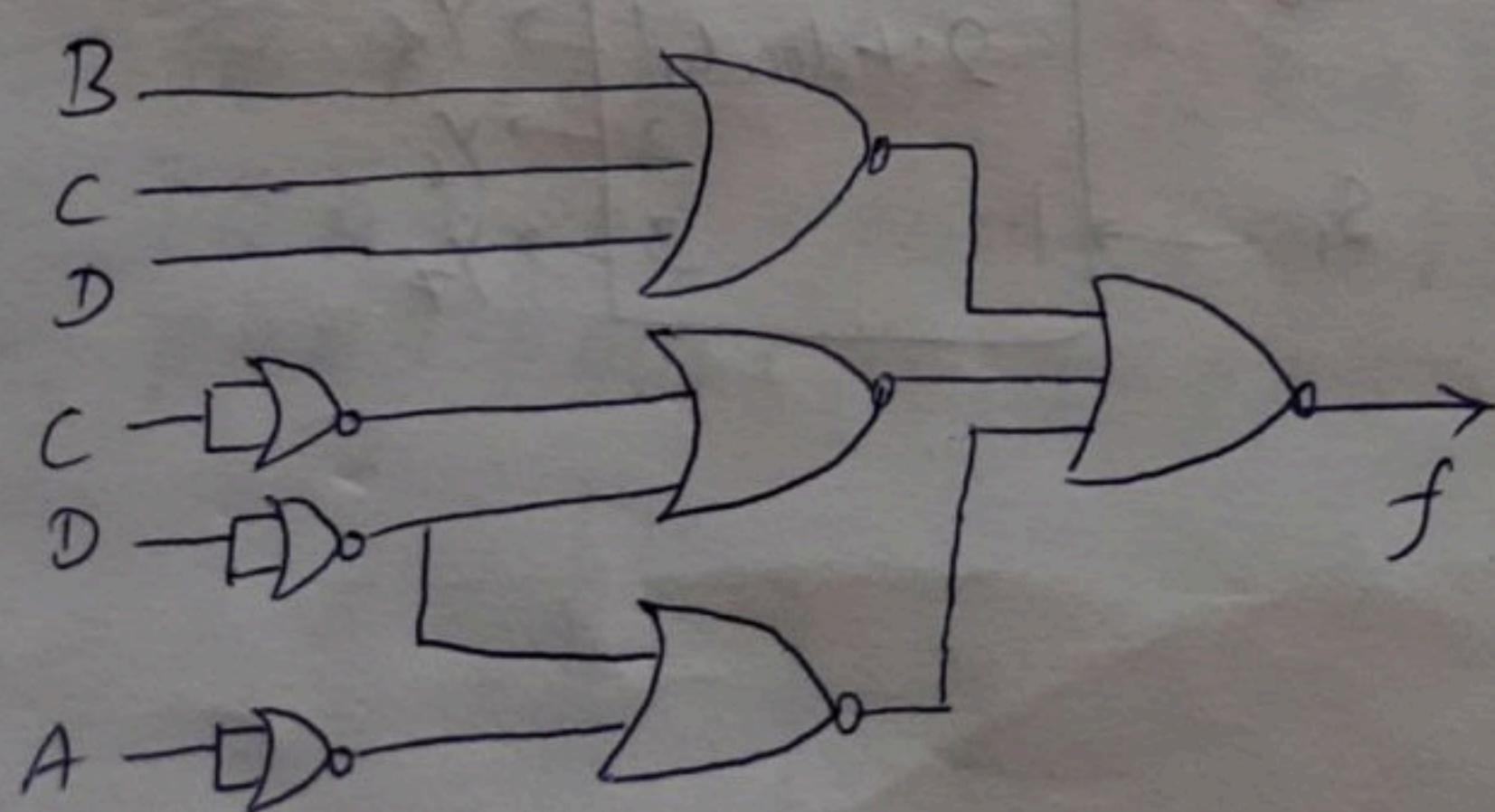


Q24. Find a minimum 3 level NOR gate Ckt. to realize F.

Ans → $F(A, B, C, D) = \sum_m(1, 2, 4, 5, 6, 10, 12, 14) = \prod_m(0, 3, 7, 8, 9, 11, 13, 15)$

AB	CD	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	0	1	0	3	2
$\bar{A}B$	4	5	0	7	6
$A\bar{B}$	12	0	13	0	14
AB	8	0	9	0	10
$A\bar{B}$	0	1	0	2	1

$(b+c+d)(\bar{c}+\bar{d})(\bar{a}+\bar{d})$



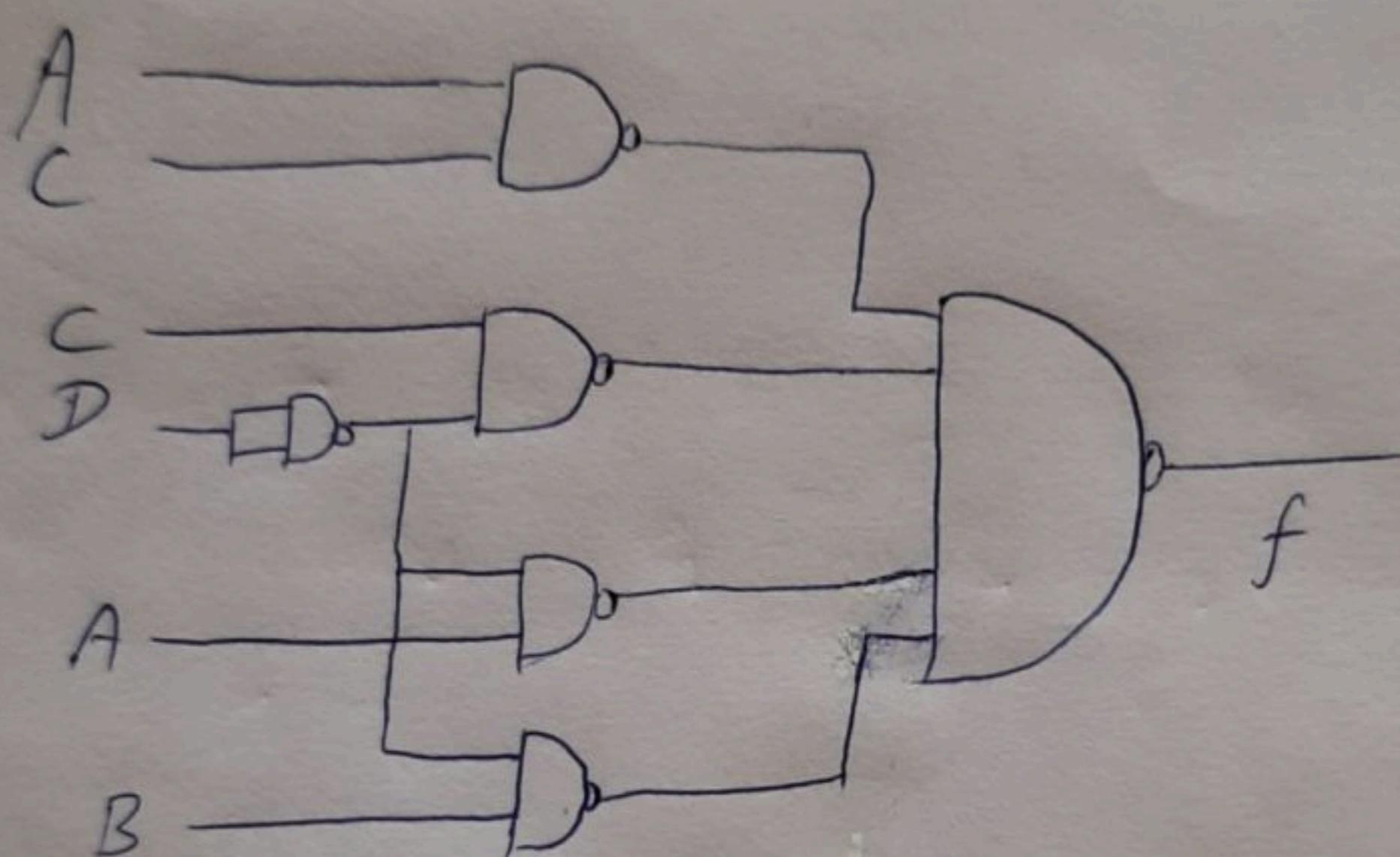
Q25. Find a minimum 3 level NAND gate ckt to realize F

$$F(A, B, C, D) = \sum m(2, 4, 6, 8, 10, 11, 12, 14, 15)$$

Ans →

AB	CD	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$A\bar{B}$	0	1	3	2	
$\bar{A}B$	4	5	7	1	6
$\bar{A}\bar{B}$	12	13	15	14	
AB	8	9	11	10	
$A\bar{B}$	1				

$$C\bar{D} + AC + A\bar{D} + B\bar{D}$$



Q26. A 16 bit ripple carry adder is realized using 16 identical full adder (FA). The carry propagation delay of each FA is 12 ns. 2 sum propagation delay of each FA is 15 ns. Find worst case delay of this 16 bit adder.

Ans → Carry Propagation delay = 12 ns

Sum Propagation delay = 15 ns

16 bit Ripple carry adder: sum of 2nd bit from LSB will be calculated only if carry is propagated

$$\begin{aligned} \text{Worst Case delay} &= (\text{Carry propagation delay} \times 15) + 15 \\ &= (12 \times 15) + 15 \\ &= 195 \text{ ns} \end{aligned}$$

Assignment 4 (Latches & Flip Flops)

Q1. Design an MN latch whose functionality is described with below table.

Ctrl	M	N	Q	\bar{Q}	State
0	X	X	-	-	No change
1	0	0	0	1	Reset
1	0	1	-	-	toggle
1	1	0	-	-	No change
1	1	1	1	0	Set

Ans →

Ctrl	M	N	Q_n	Q_{n+1}	State
1	0	0	0	0	Reset
1	0	0	1	0	Reset
1	0	1	0	1	toggle
1	0	1	1	0	toggle
1	1	0	0	0	No change
1	1	0	1	1	No change
1	1	1	0	1	Set
1	1	1	1	1	Set

$$Q_{n+1} = f(M, N, Q_n) = \sum m(2, 5, 6, 7)$$

		NQ_n			
		$\bar{M}\bar{N}$	$\bar{M}N$	$M\bar{N}$	MN
M	\bar{N}	1	0	1	0
	N	0	1	0	1

$$= M Q_n + N \bar{Q}_n$$

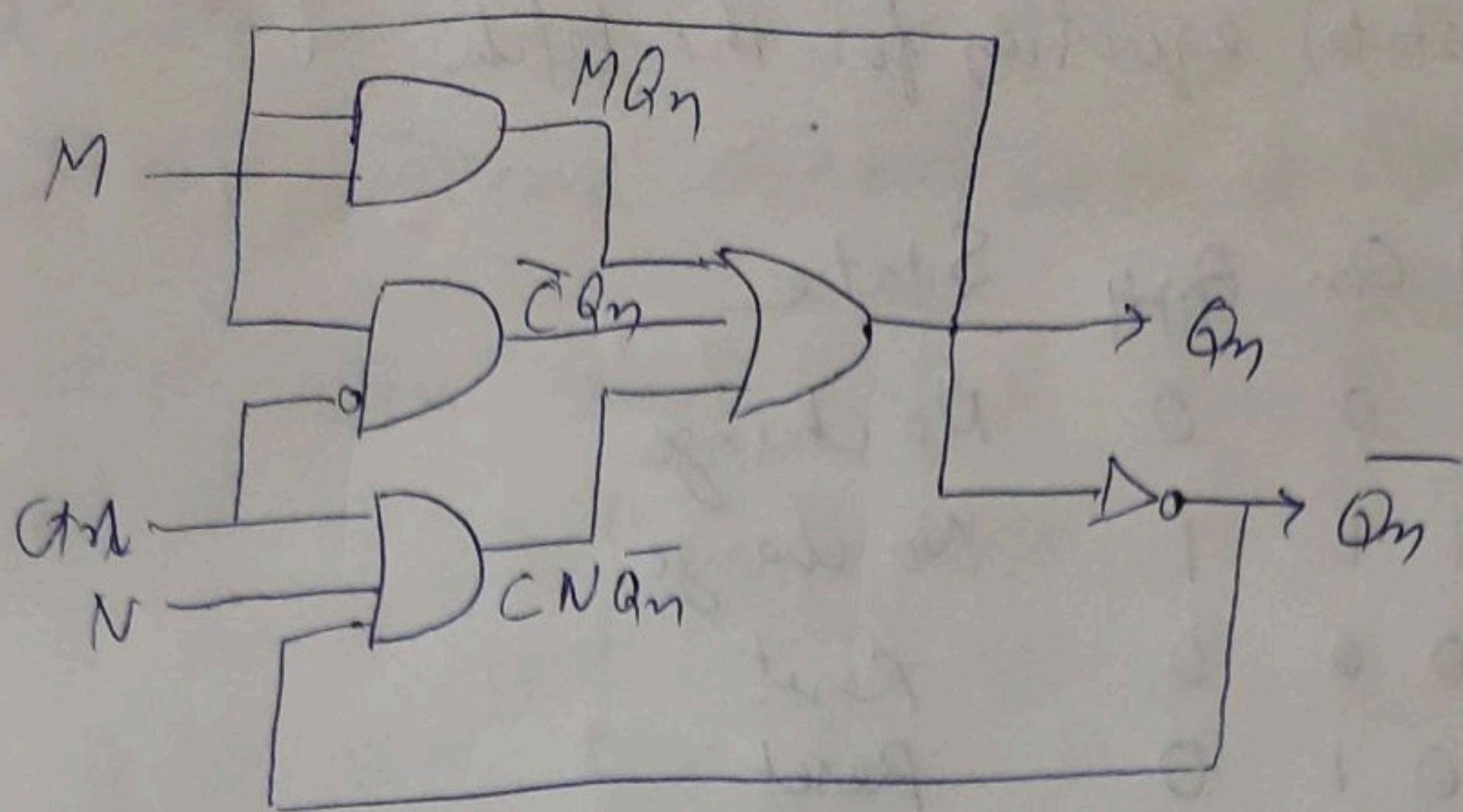
$$= C(M Q_n + N \bar{Q}_n) + \bar{C} Q_n$$

$$= CMQ_n + CN\bar{Q}_n + \bar{C} Q_n$$

$$= Q_n(CM + \bar{C}) + CN\bar{Q}_n$$

$$= Q_n(M + \bar{C}) + CN\bar{Q}_n$$

$$= M Q_n + \bar{C} Q_n + CN\bar{Q}_n$$



Q2. Draw excitation table of MN latch described in the previous problem.

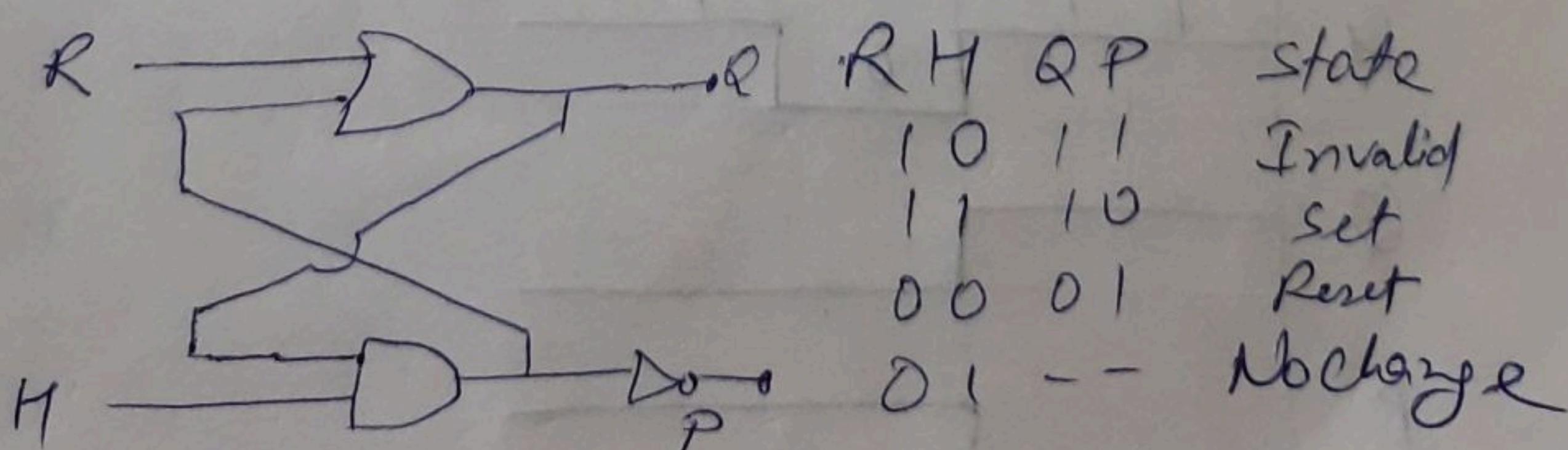
Ans →

Q_n	Q_{n+1}	M	N
0	0	X	0
0	1	X	1
1	0	0	X
1	1	1	X

Q3. A latch can be constructed from an OR gate, an AND gate & an inverter connected as follows—

- a) What restriction must be placed on R & H so that P will always equal \bar{Q} (under steady state conditions)?

Ans →



The restriction is that $\{R, H\}$ should not be equal to $\{1, 0\}$ to make sure that Q & P are always complement to each other.

b) construct a next state table & derive the characteristic (next state) equation for the latch.

Ans → RH Q_n Q_{n+1} State

0 1 0 0 No change

0 1 1 1 No change

0 0 0 0 Reset

0 0 1 0 Reset

1 1 0 1 Set

1 1 1 1 Set

1 0 0 X Invalid

1 0 1 X Invalid

$$Q_{n+1} = f(RH, Q_n)$$

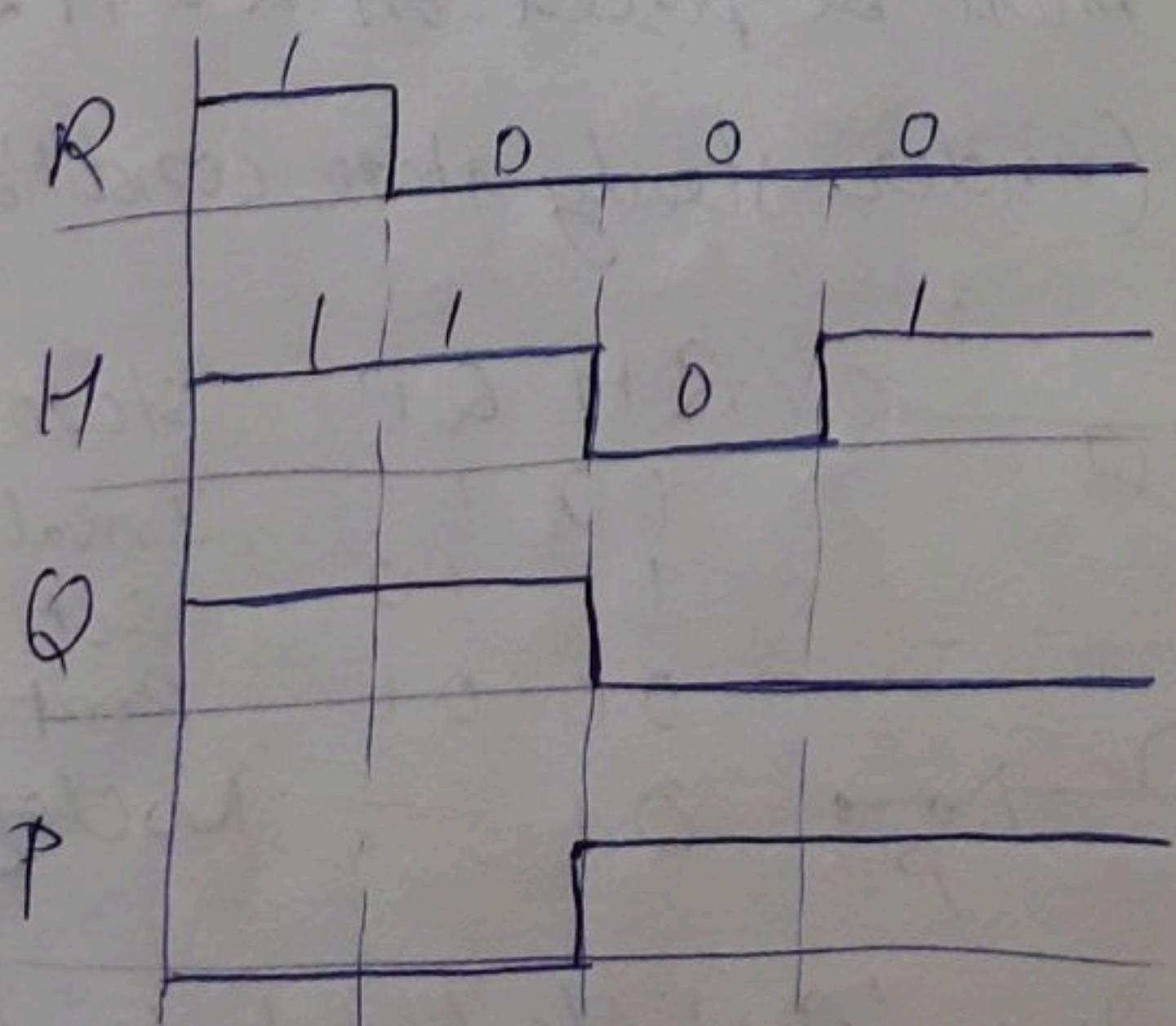
$$= \sum_m(3, 6, 7) + \sum_d(4, 5)$$

R	H Q _n	$\bar{H} \bar{Q}_n$	$\bar{H} Q_n$	$H \bar{Q}_n$	$H Q_n$
0	0	1	3	2	
1	X	X	1	0	D
2	X	D	0	D	6
4	X	D	1	0	
5	X	D	0	1	

$$Q_{n+1} = R + H Q_n$$

c) complete following timing diagram for latch.

Ans →



Q7. A reset dominant latch behaves like an SR latch, except that F/P S-R-1 is allowed, R latch is reset when S-R-1. Derive characteristic eqn & show construction

Ans → S R Q_n Q_{n+1} State

0 0 0 0 No change

0 0 1 1 No change

0 1 0 0 Reset

0 1 1 0 Reset

1 0 0 1 Set

1 0 1 1 Set

1 1 0 0 Reset

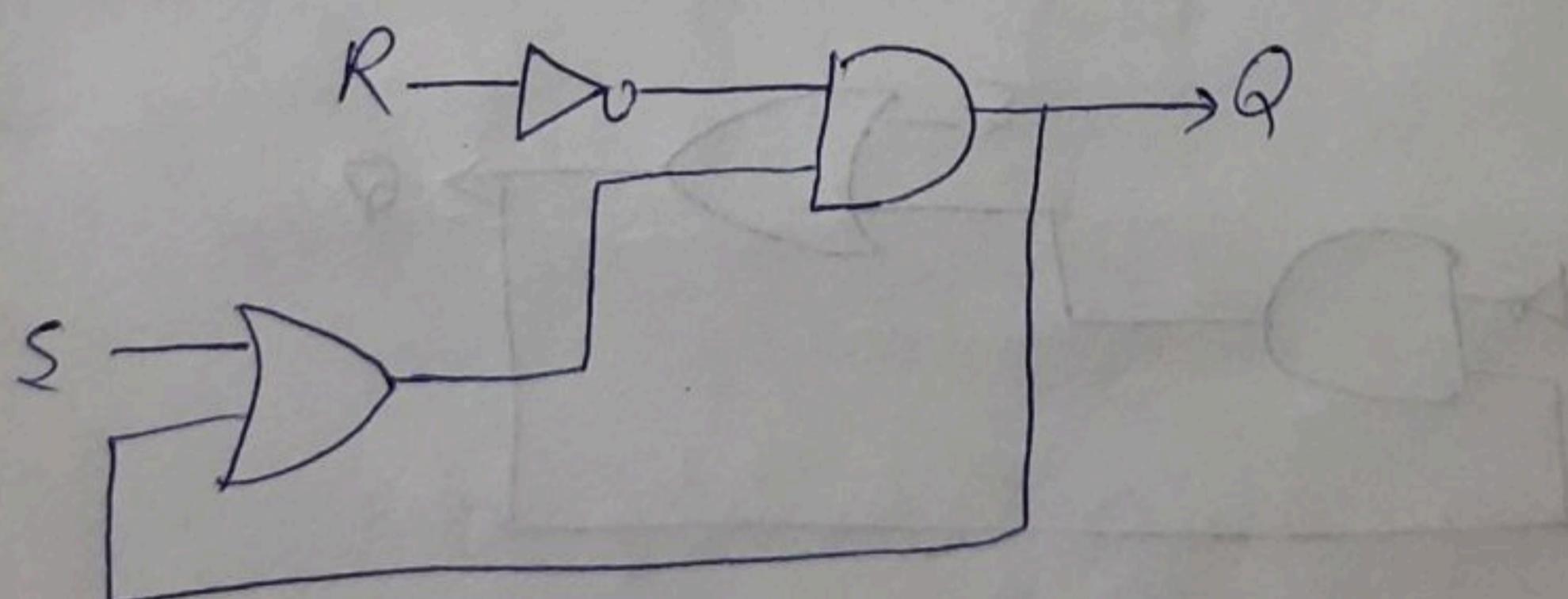
1 1 1 0 Reset

$$Q_{n+1} = f(S, R, Q_n)$$

$$= \sum_m (1, 4, 5)$$

S	R	Q_n	$\bar{R}Q_n$	$\bar{R}\bar{Q}_n$	$R\bar{Q}_n$	RQ_n	\bar{S}
0	0	0	1	0	0	0	1
0	0	1	0	1	0	0	1
0	1	0	0	1	1	0	0
0	1	1	0	0	0	1	0
1	0	0	1	0	0	1	0
1	0	1	0	1	0	1	0
1	1	0	0	1	1	0	0
1	1	1	0	0	0	1	0

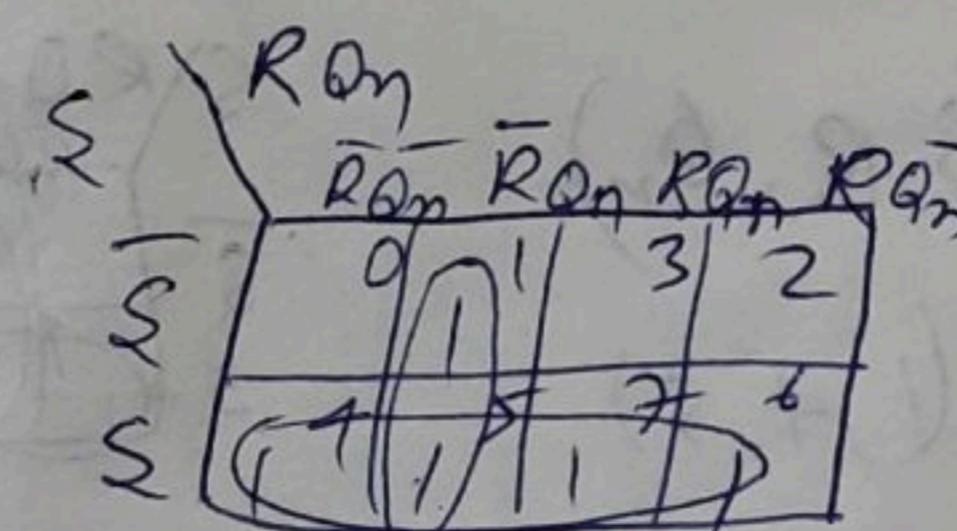
$$\begin{aligned} Q_{n+1} &= \bar{R}Q_n + S\bar{R} \\ &= \bar{R}(Q_n + S) \end{aligned}$$



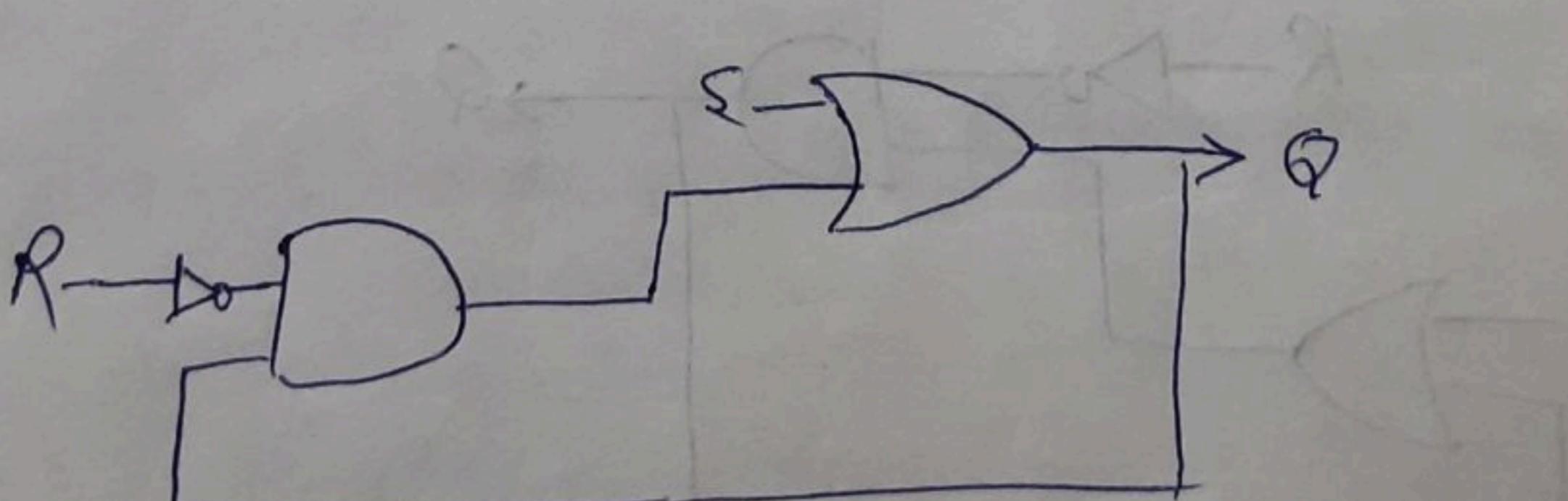
Q5. A set dominant latch behaves like an SR latch,
 - except that I/P $S-R-1$ is allowed & latch is set
 when $S-R-1$. Derive characteristic eqn & show construction.

S	R	Q_n	Q_{n+1}	State
0	0	0	0	No change
0	0	1	1	No change
0	1	0	0	Reset
0	1	1	0	Reset
1	0	0	1	Set
1	0	1	1	Set
1	1	0	1	Set
1	1	1	1	Set

$$Q_{n+1} = f(S, R, Q_n) \\ = \sum_m(1, 4, 5, 6, 7)$$



$$Q_{n+1} = \bar{R}Q_n + S$$



Q6. Show how a reset dominant SR flip flop can be constructed by adding gates to a normal SR flip flop.

Ans -

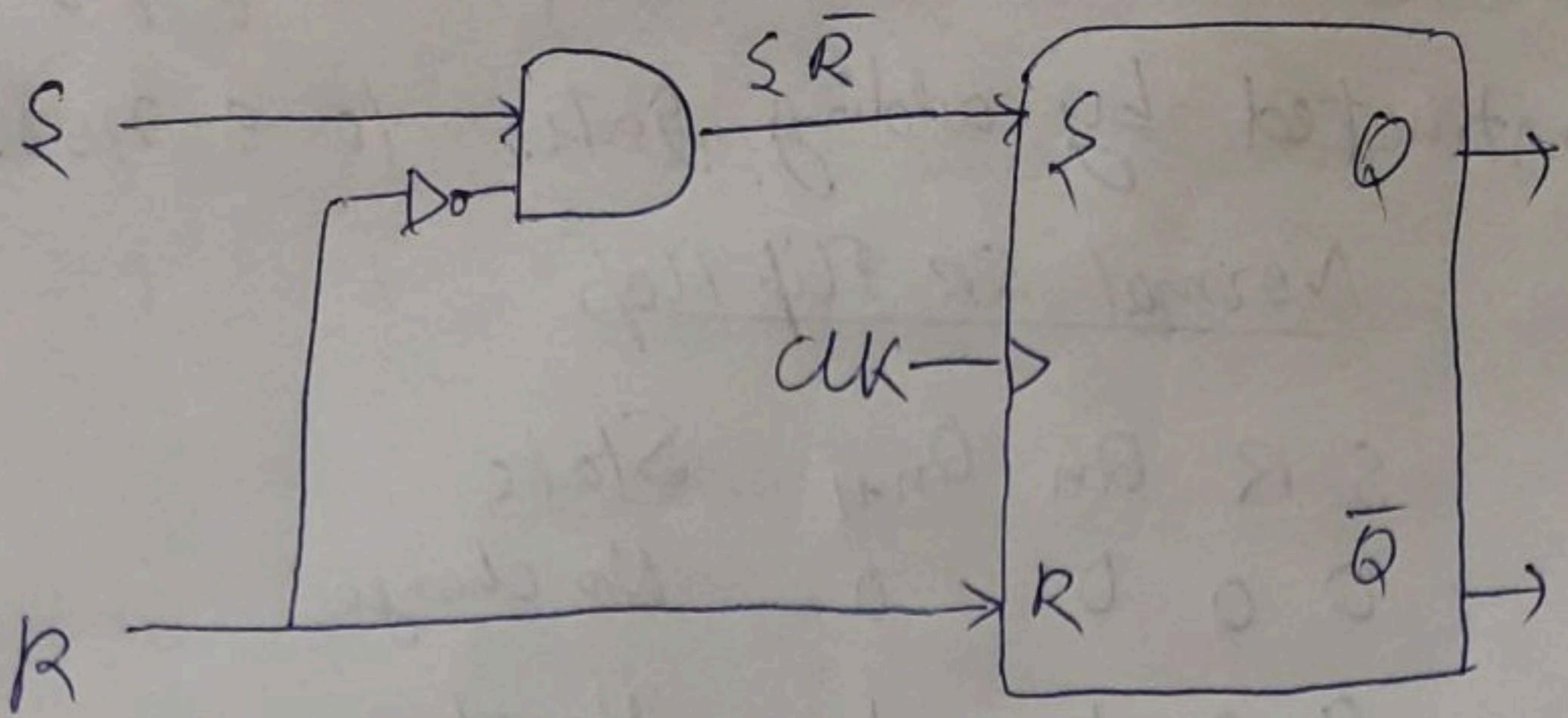
Normal SR Flip Flop

S R	Q _n	Q _{n+1}	State
0 0	0	0	No change
0 0	1	1	No change
0 1	0	0	Reset
0 1	1	0	Reset
1 0	0	1	Set
1 0	1	1	Set
1 1	0	X	Invalid
1 1	1	X	Invalid

Reset dominant SR Flip Flop

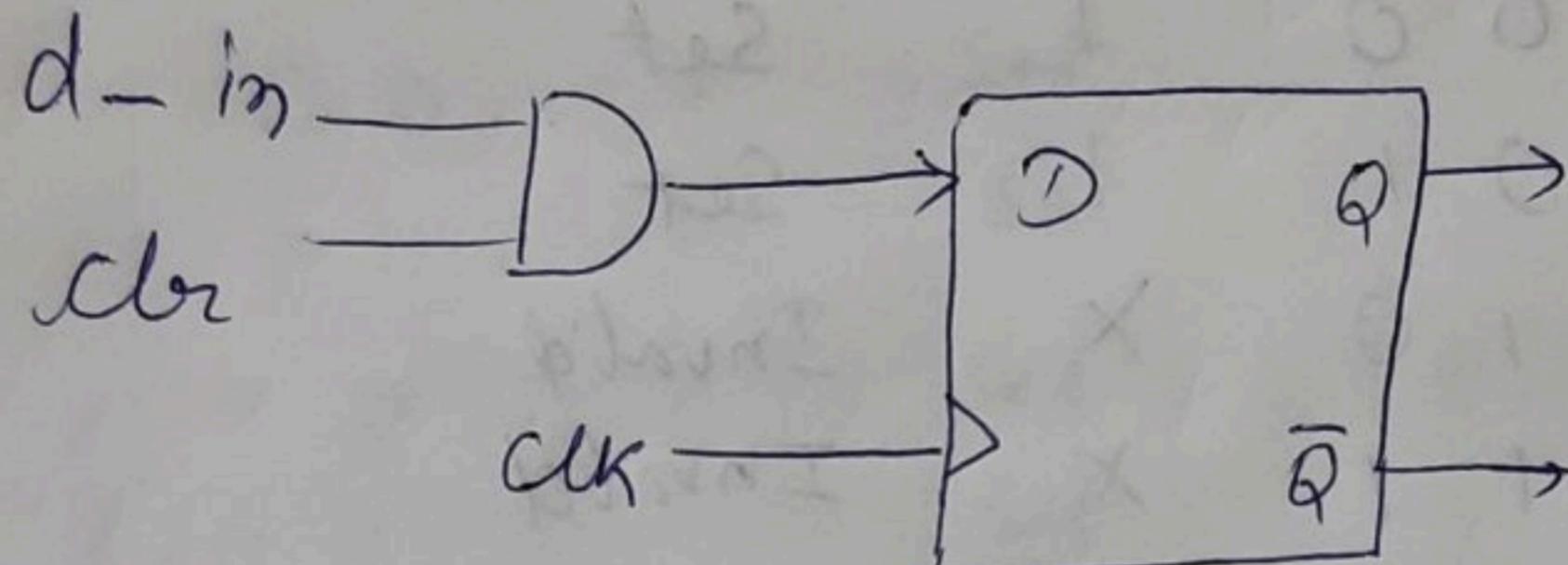
S R	Q _n	Q _{n+1}	State
0 0	0	0	No change
0 0	1	1	No change
0 1	0	0	Reset
0 1	1	0	Reset
1 0	0	1	Set
1 0	1	1	Set
1 1	0	0	Reset
1 1	1	0	Reset

In order to make a normal SR flip flop to work like reset dominant SR flip flop, we need to make sure that S-I/P of normal SR flip flop must be supplied with 0 when both S & R are 1.



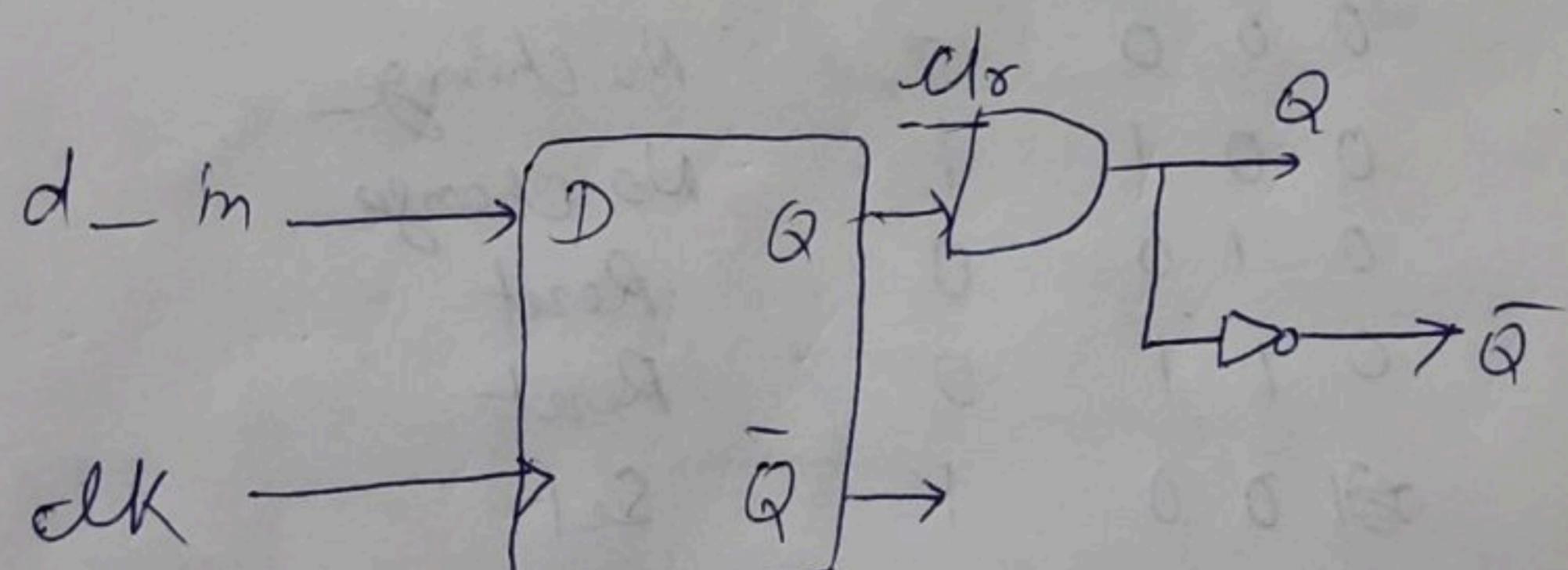
Q7. Design a D-FF with synchronous clear signal.

Ans →



Q8. Design a D-FF with Asynchronous clear signal.

Ans →



Q9. Convert by adding external gates:

a) A D-flip flop to a J-K flip flop

Ans →

$$\begin{array}{cccc} JK & Q_n & Q_{n+1} & D \end{array}$$

$$J = f(J, K, Q_n) = \sum m(1, 4, 5, 6)$$

$$\begin{array}{cccc} 0 & 0 & 0 & 0 \end{array}$$

$$\begin{array}{cccc} 0 & 0 & 1 & 1 \end{array}$$

$$\begin{array}{cccc} 0 & 1 & 0 & 0 \end{array}$$

$$\begin{array}{cccc} 0 & 1 & 1 & 0 \end{array}$$

$$\begin{array}{cccc} 1 & 0 & 0 & 1 \end{array}$$

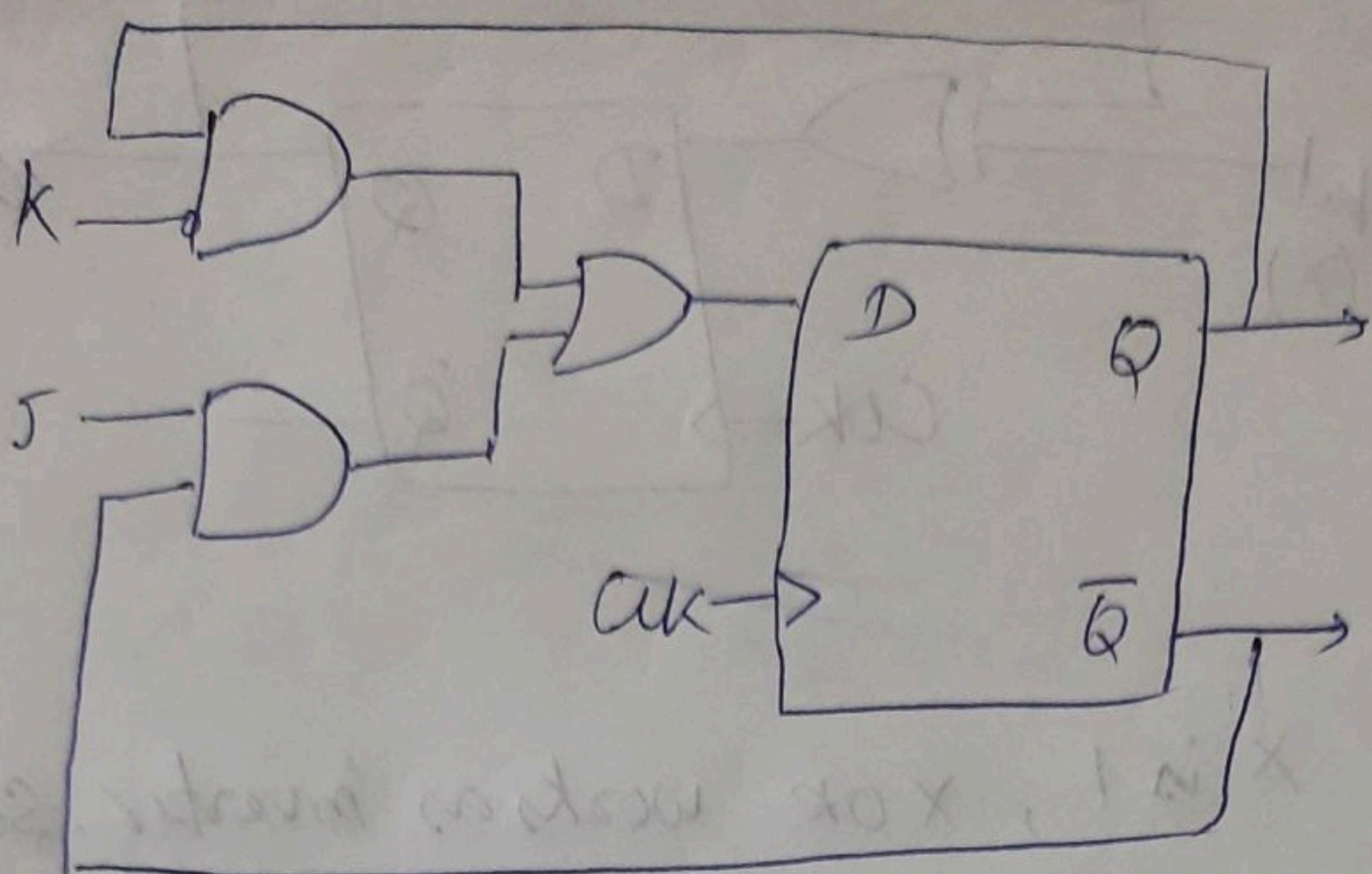
$$\begin{array}{cccc} 1 & 0 & 1 & 1 \end{array}$$

$$\begin{array}{cccc} 1 & 1 & 0 & 1 \end{array}$$

$$\begin{array}{cccc} 1 & 1 & 1 & 0 \end{array}$$

J	KQ_n	$\bar{K}Q_n$	$K\bar{Q}_n$	$\bar{K}\bar{Q}_n$
0	0	1	3	2
0	1	0	1	7
1	0	1	0	6
1	1	1	1	1

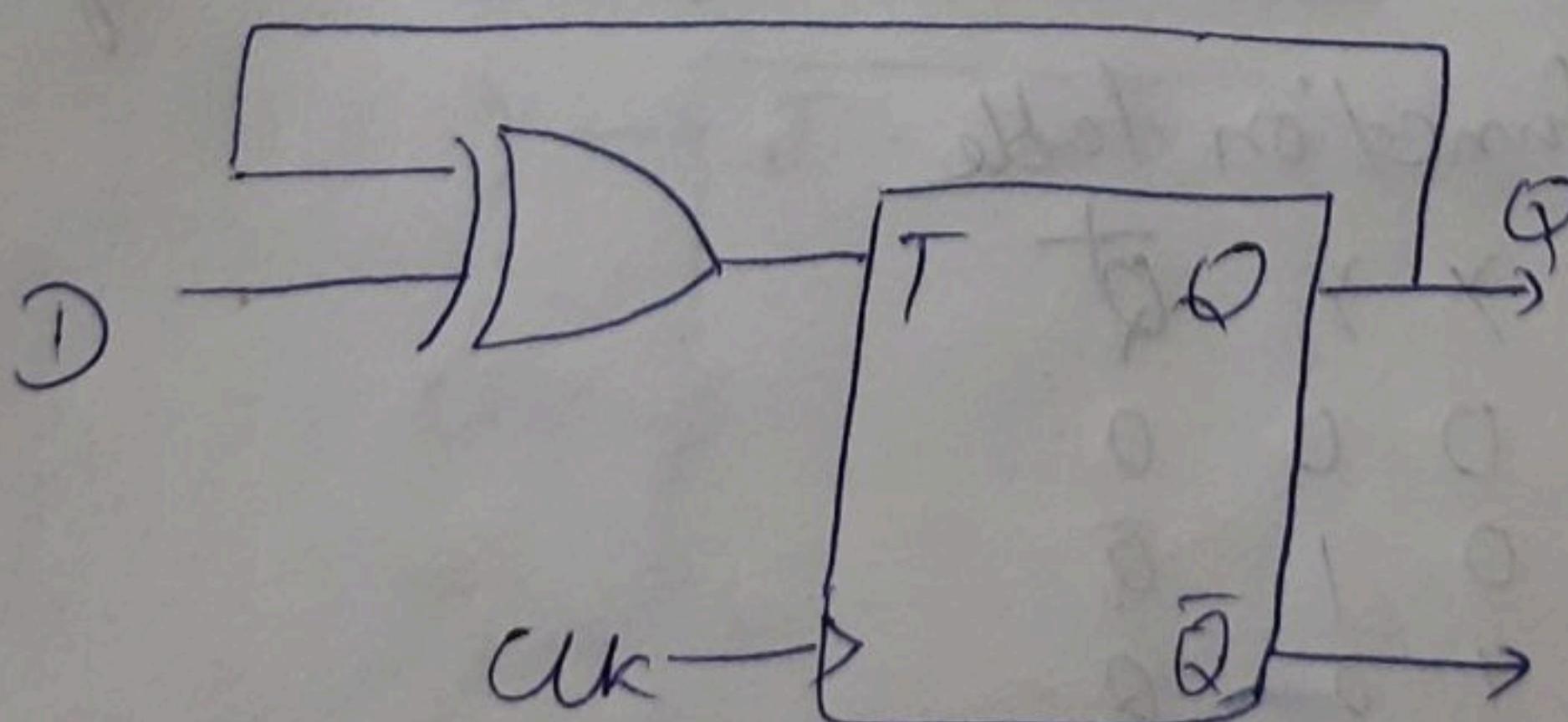
$$D = \bar{J}Q_n + \bar{K}Q_n$$



b) A T-flip flop to a D-flip flop

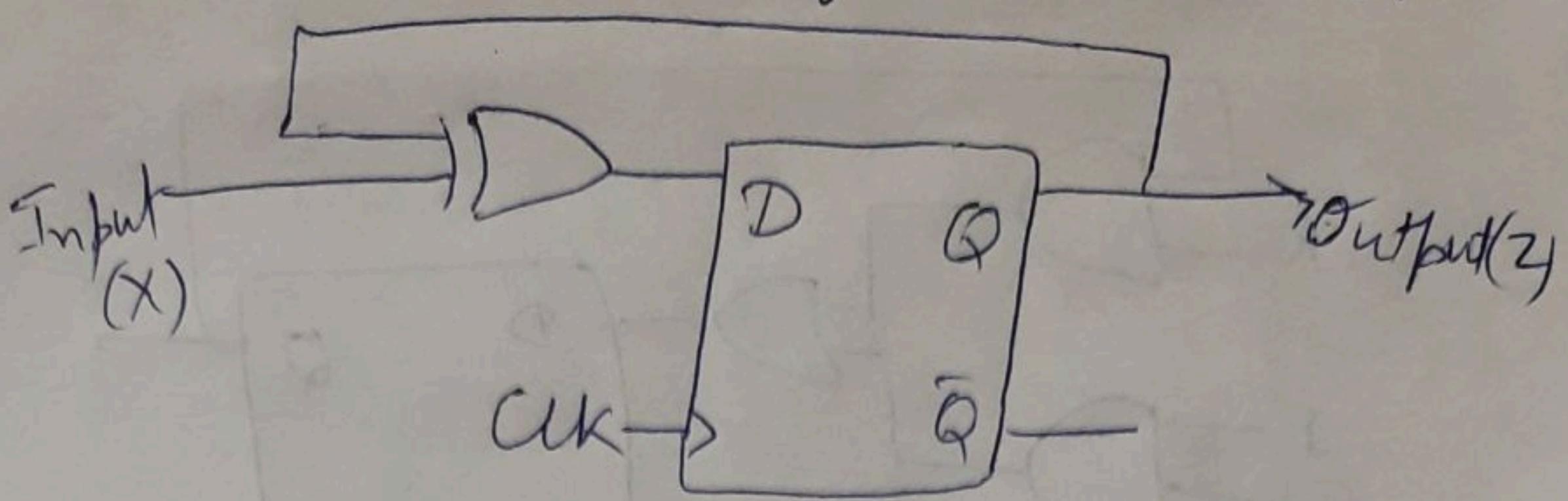
D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

$$T = f(P, Q_n) = D \bar{Q}_n + \bar{D} Q_n \Leftrightarrow D \oplus Q_n$$



Q10. Explain the behaviour of given circuit.

Ans



When X is 1, XOR works as inverter. So, D will be supplied with \bar{Q} for every cycle. So O/P toggles for every cycle in the clock.

When X is 0, XOR work as buffer. So, D will be supplied with Q for every cycle. So O/P remains the same.

So, this circuit works like T flip flop.

Q11. Convert a positive edge triggered JK flip flop to a positive edge triggered XY flip flop as defined by following function table:

X	Y	Q ^t
0	0	0
0	1	\bar{Q}
1	0	Q

Ans →

Excitation Table

Q _n	Q _{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
(X	0)

X	Y	Q_n	Q_{n+1}	JK
0	0	0	0	0 X
0	0	1	0	X 1
0	1	0	1	1 X
0	1	1	0	X 1
1	0	0	0	0 X
1	0	1	1	X 0
1	1	0	1	1 X
1	1	1	1	X 0

$$J = f(X, Y, Q_n) = \sum m(2, 6) + \sum d(1, 3, 5, 7)$$

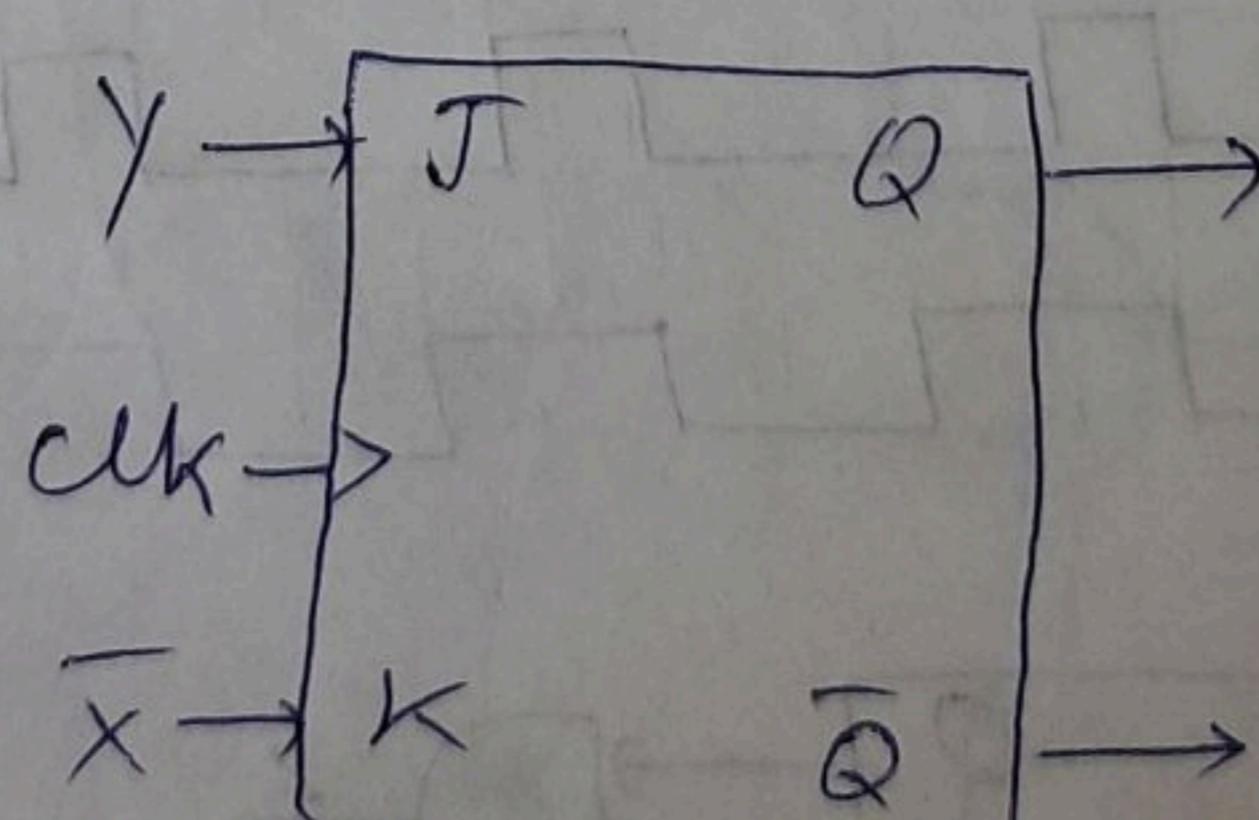
$$K = f(X, Y, Q_n) = \sum m(1, 3) + \sum d(0, 2, 4, 6)$$

X	Y	Q_n	$\bar{X}Q_n$	$\bar{Y}Q_n$	YQ_n	$X\bar{Q}_n$	$\bar{Y}\bar{Q}_n$
0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1
0	1	0	1	0	0	1	0

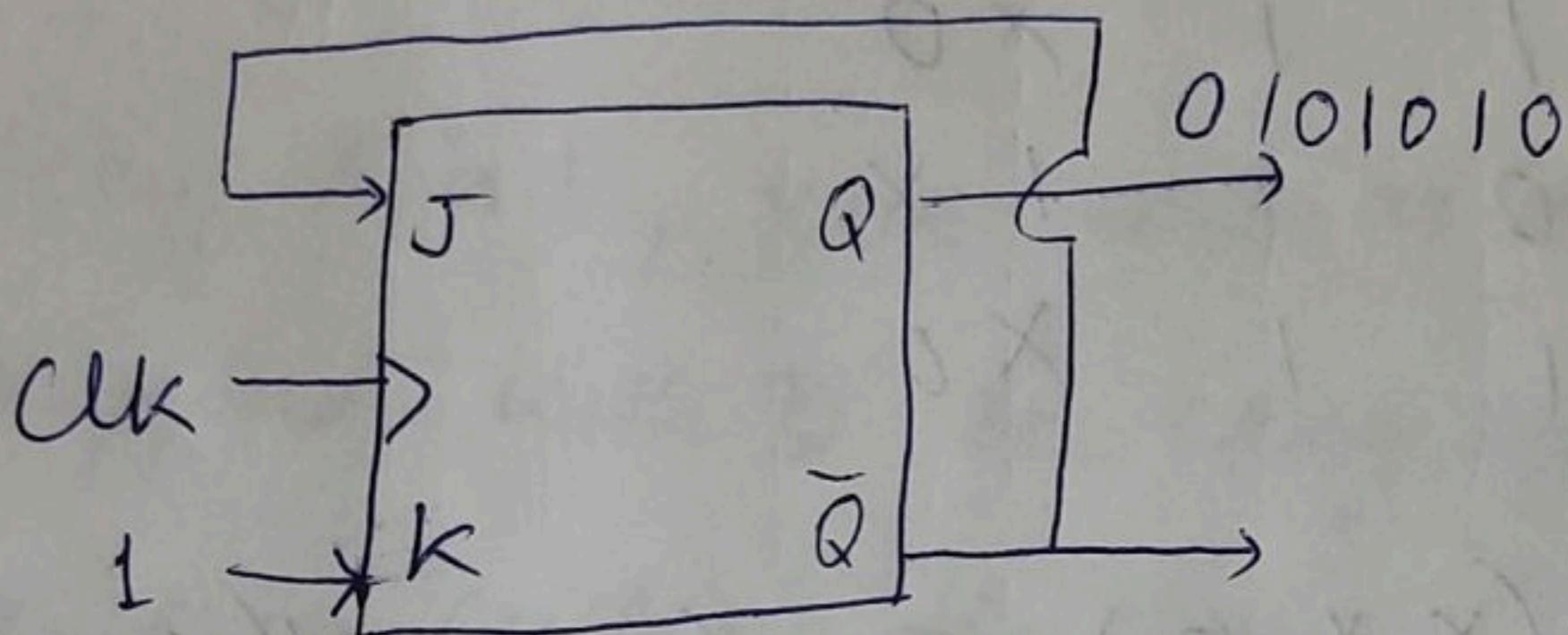
X	Y	Q_n	$\bar{X}Q_n$	$\bar{Y}Q_n$	YQ_n	$X\bar{Q}_n$	$\bar{Y}\bar{Q}_n$
0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1
0	1	1	1	0	0	1	0

$$J = Y$$

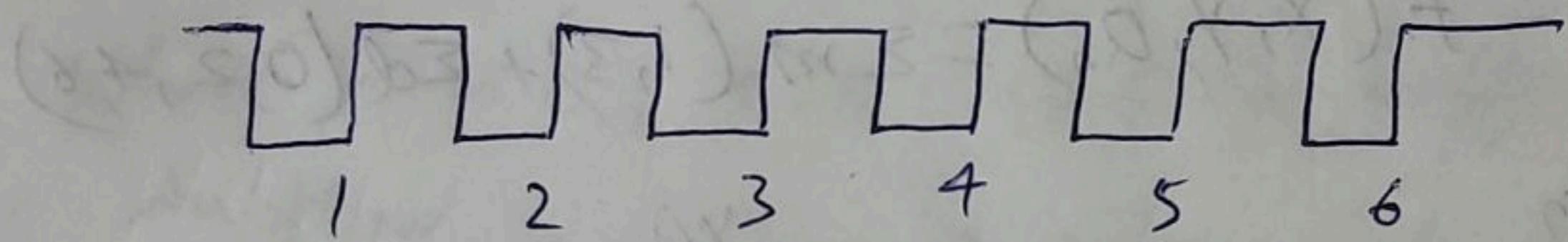
$$K = \bar{X}$$



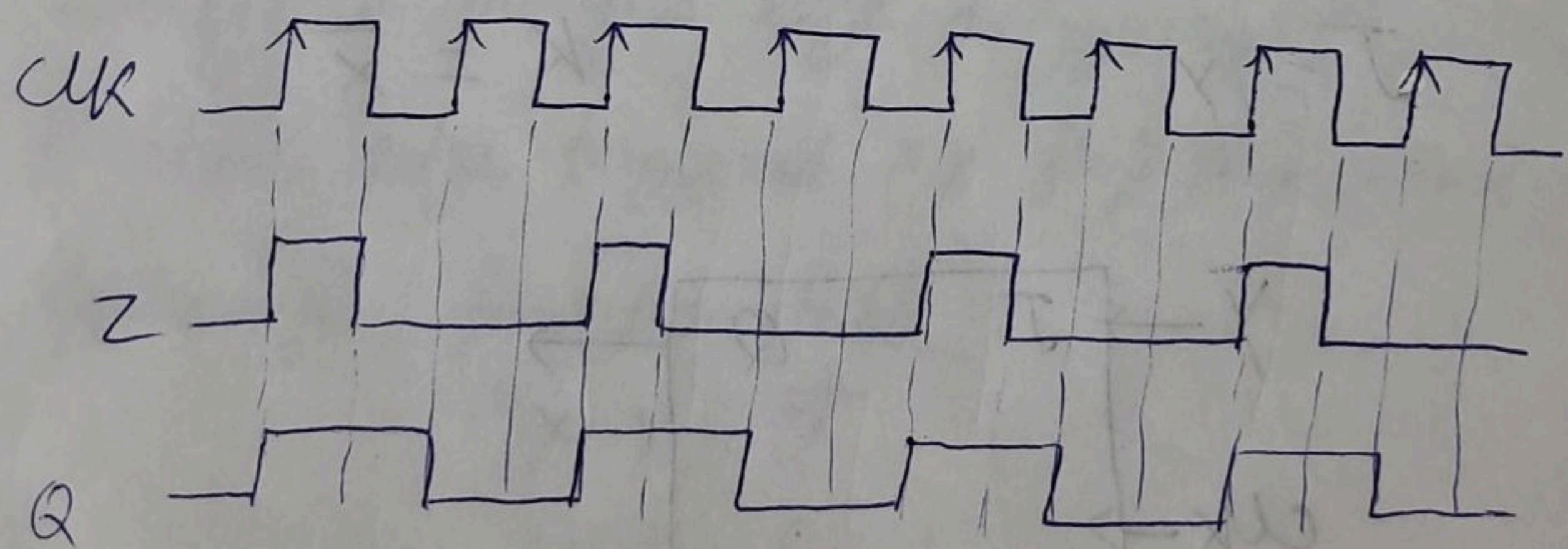
Q12. In a positive edge triggered JK flip flop, we have $J = \bar{Q}$ & $K = 1$ as shown in figure below. Assume the flip flop was initially cleared & then clocked for 6 clock pulses, find sequence at Q output for those 6 clock cycles.



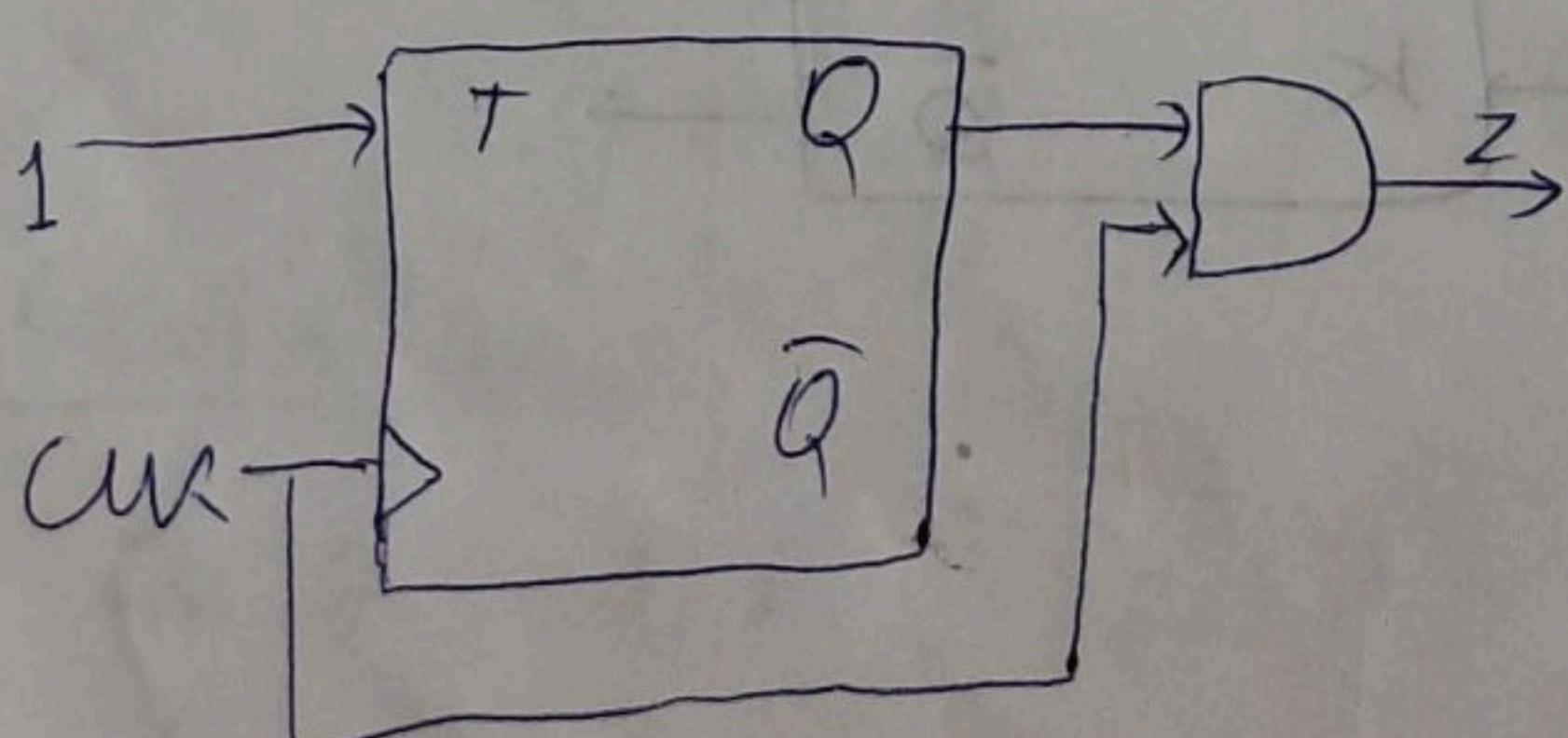
Ans→



Q13. Design a circuit whose input clock & output Z relationship as shown in diagram below.



Ans→

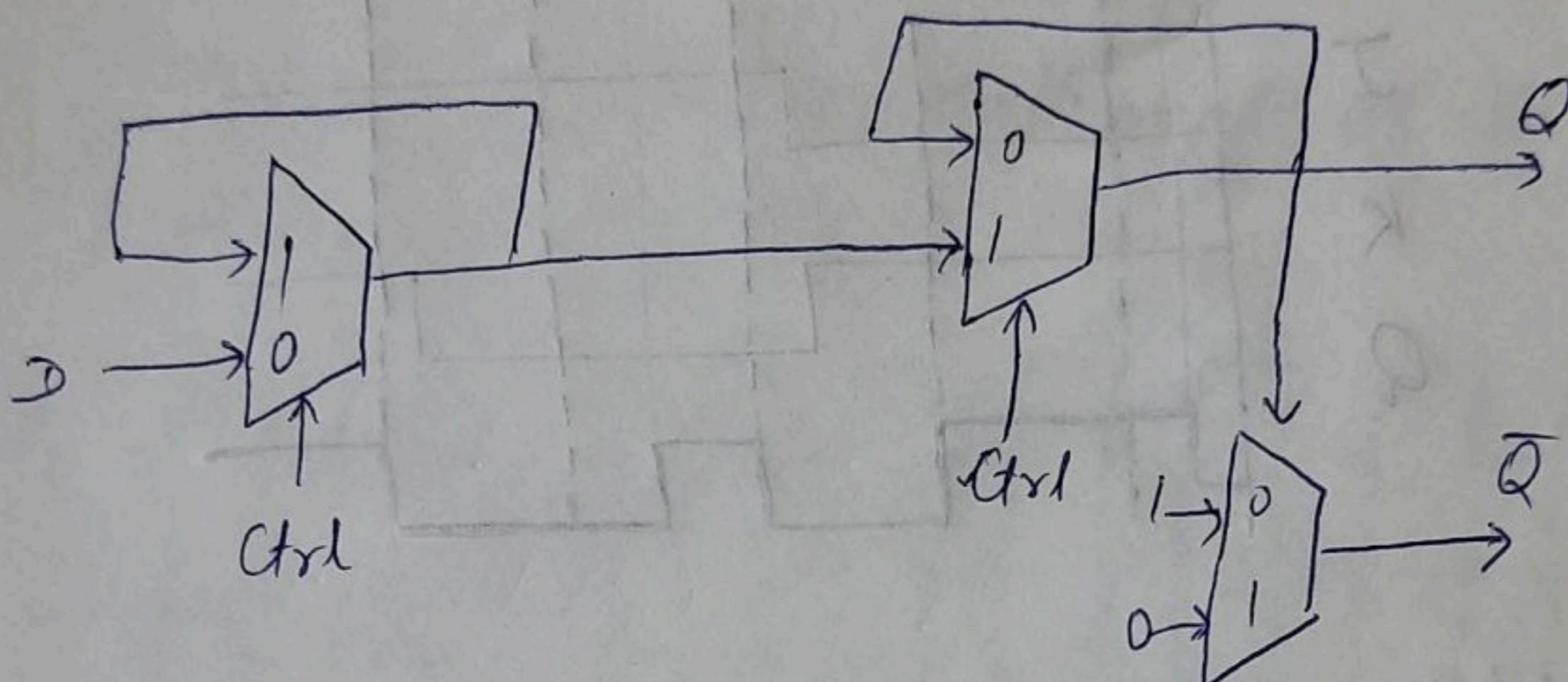


Q14. Design a posedge triggered D flip flop using 2:1 Muxes only.

Ans → Active low Latch Active High Latch

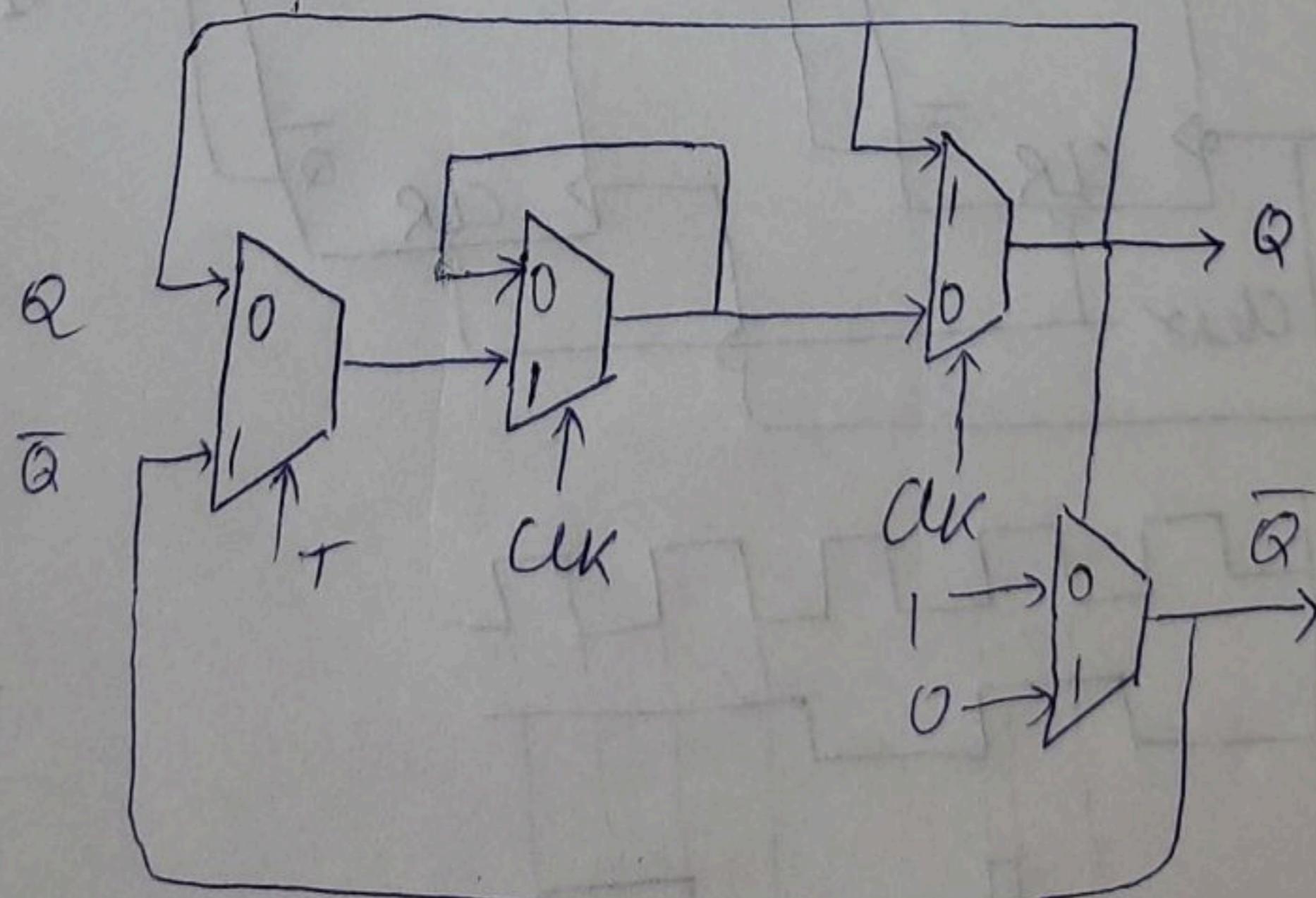
Ctrl Q_{n+1}
0 D
1 Q_n

Ctrl Q_{n+1}
1 D
0 Q_n

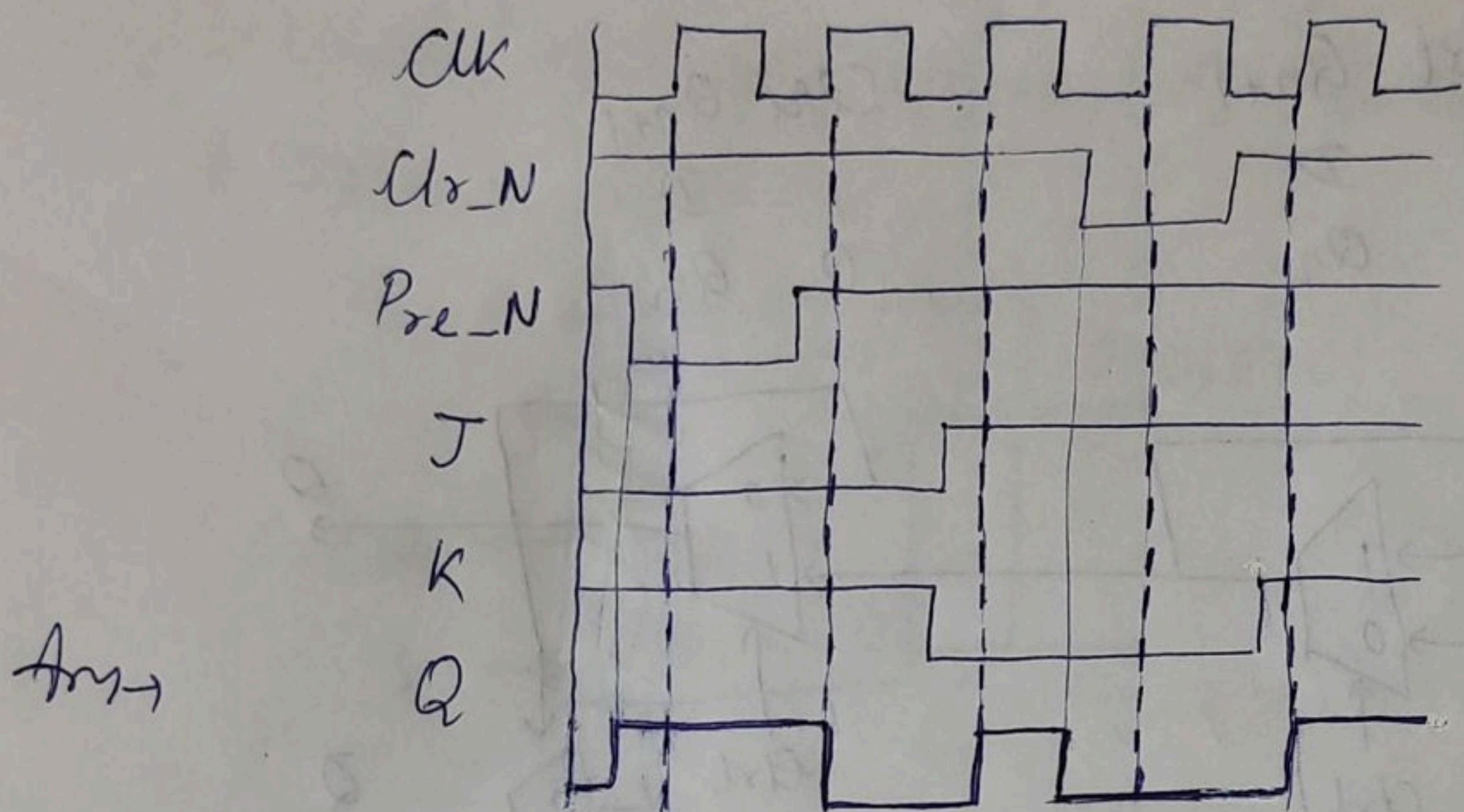


Q15. Design a negedge triggered T flip flop using 2:1 Muxes only.

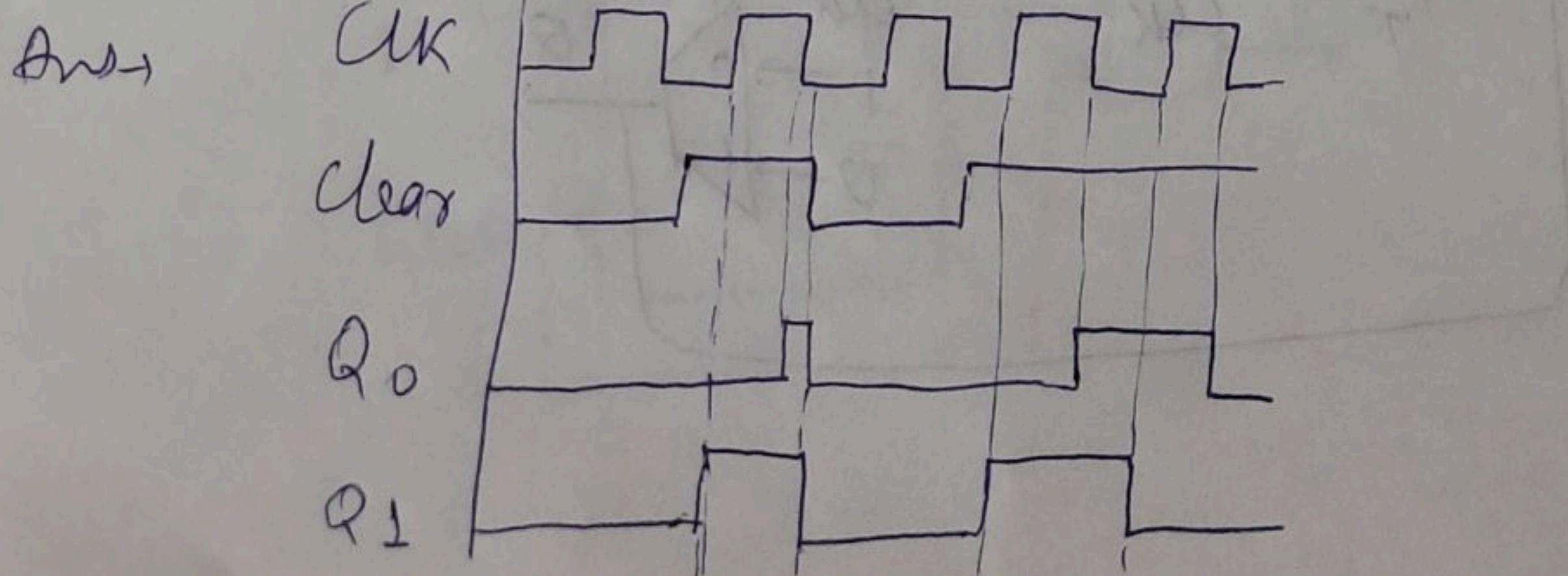
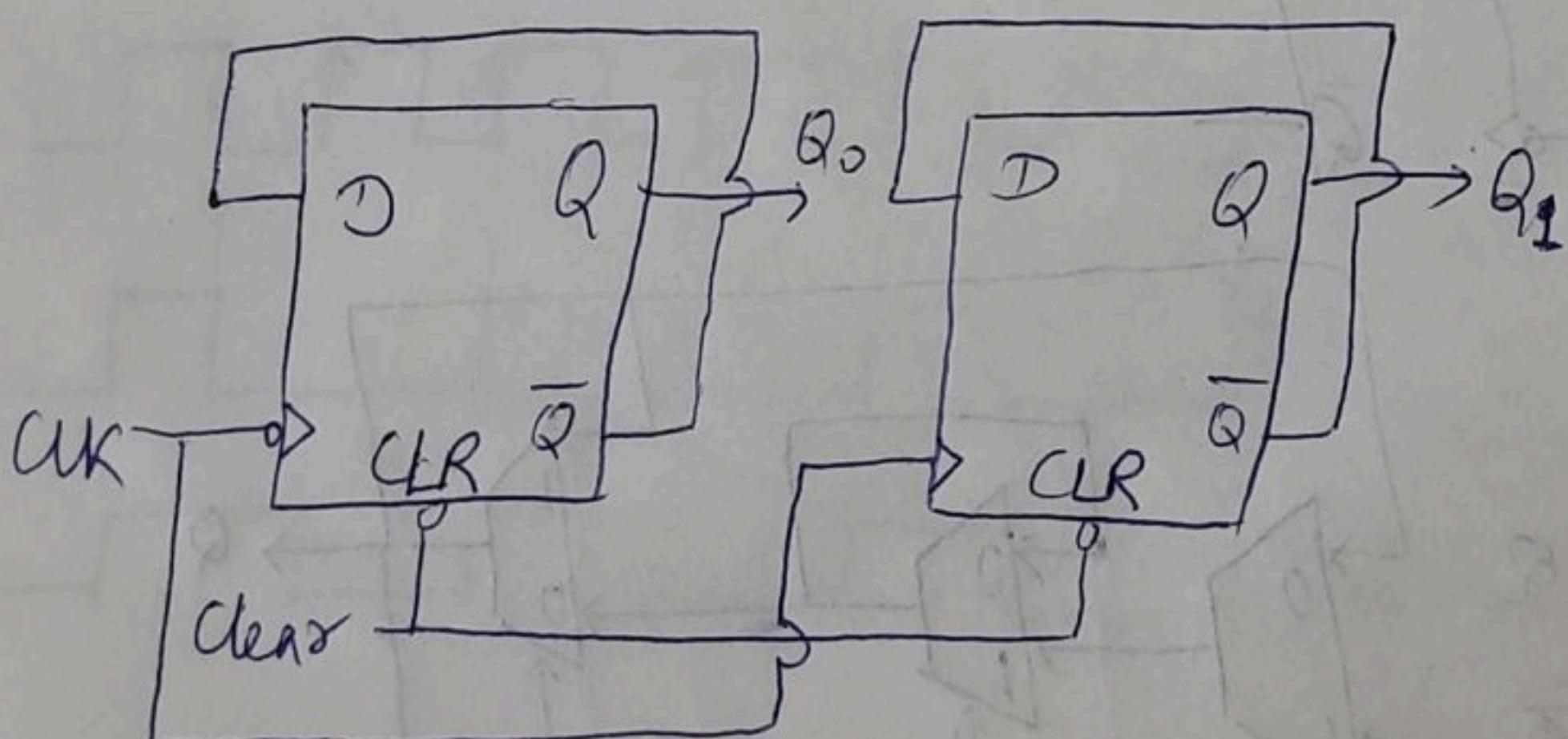
Ans →



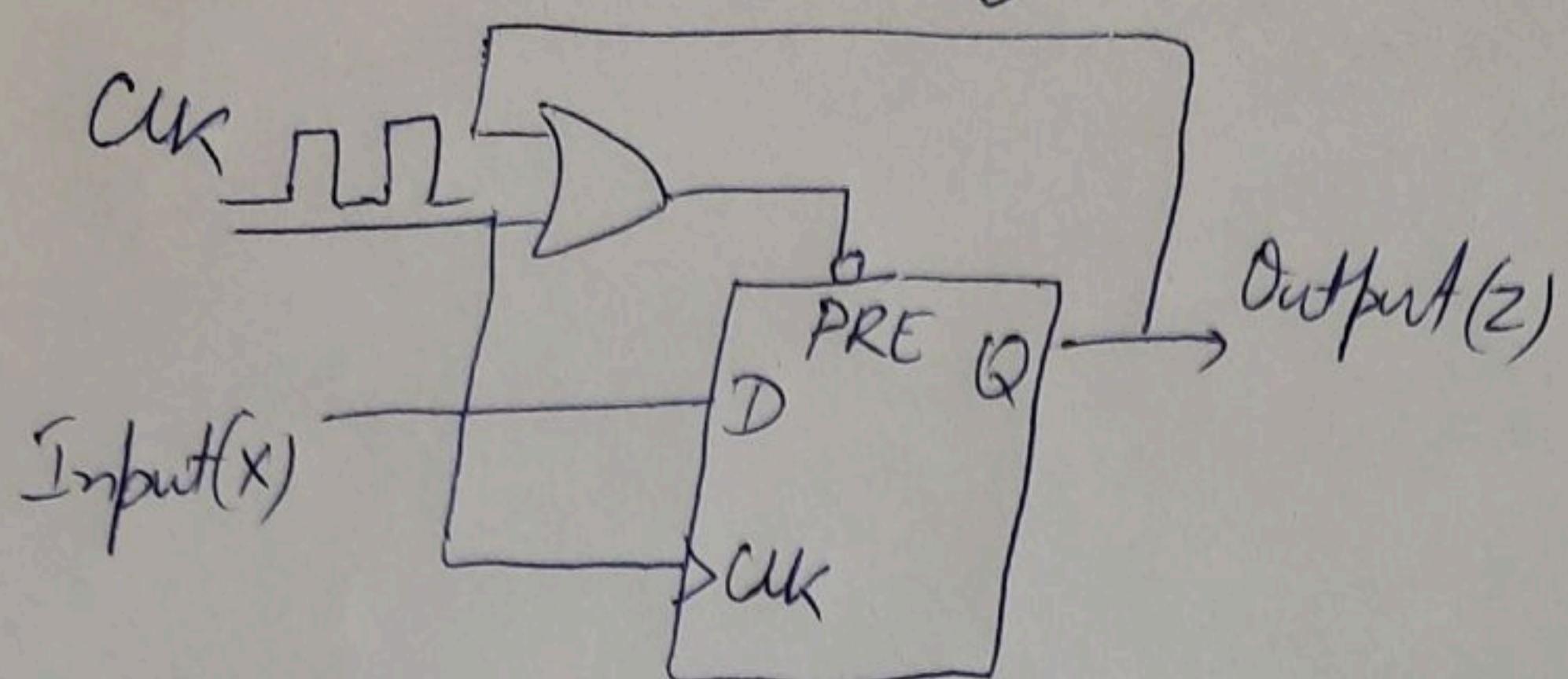
Q16. Complete following timing diagram for JK flip flop with a raising edge trigger & Asynchronous Active low Clr_N & Pre_N inputs.



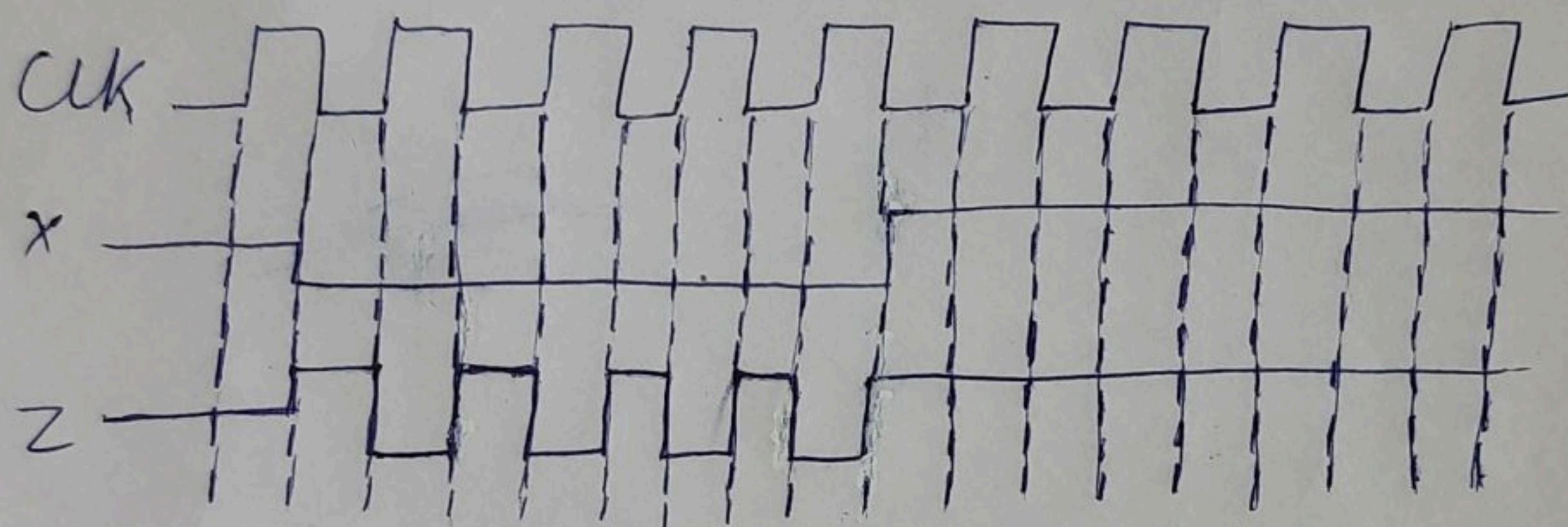
Q17. Complete timing diagram for following circuit. Note that clock inputs on 2 flip flops are different. The flip flops are with asynchronous clear inputs.



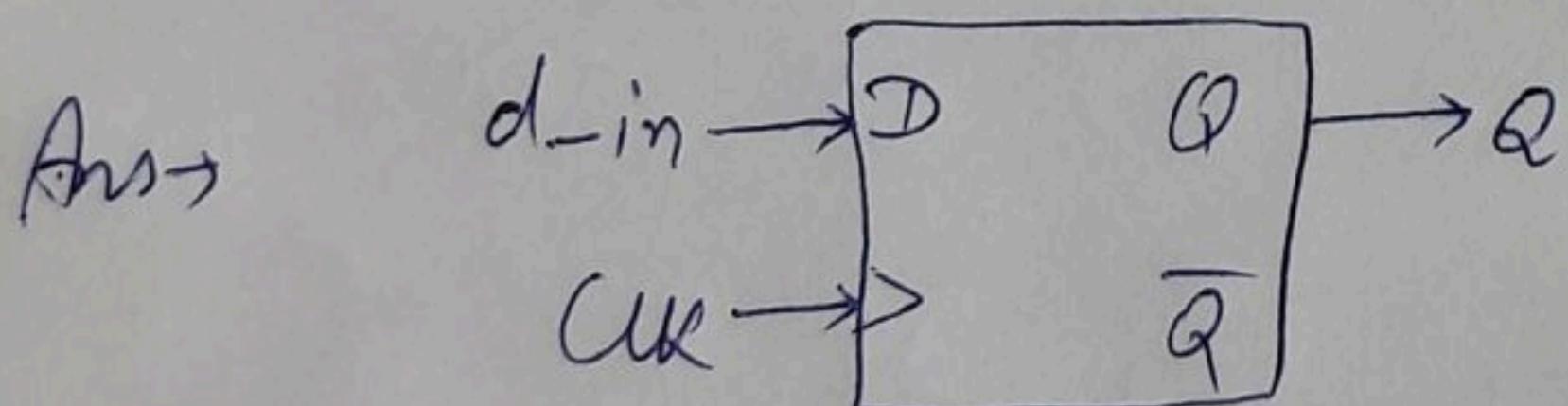
Q18. Explain what following circuit does? (Draw waveforms also)



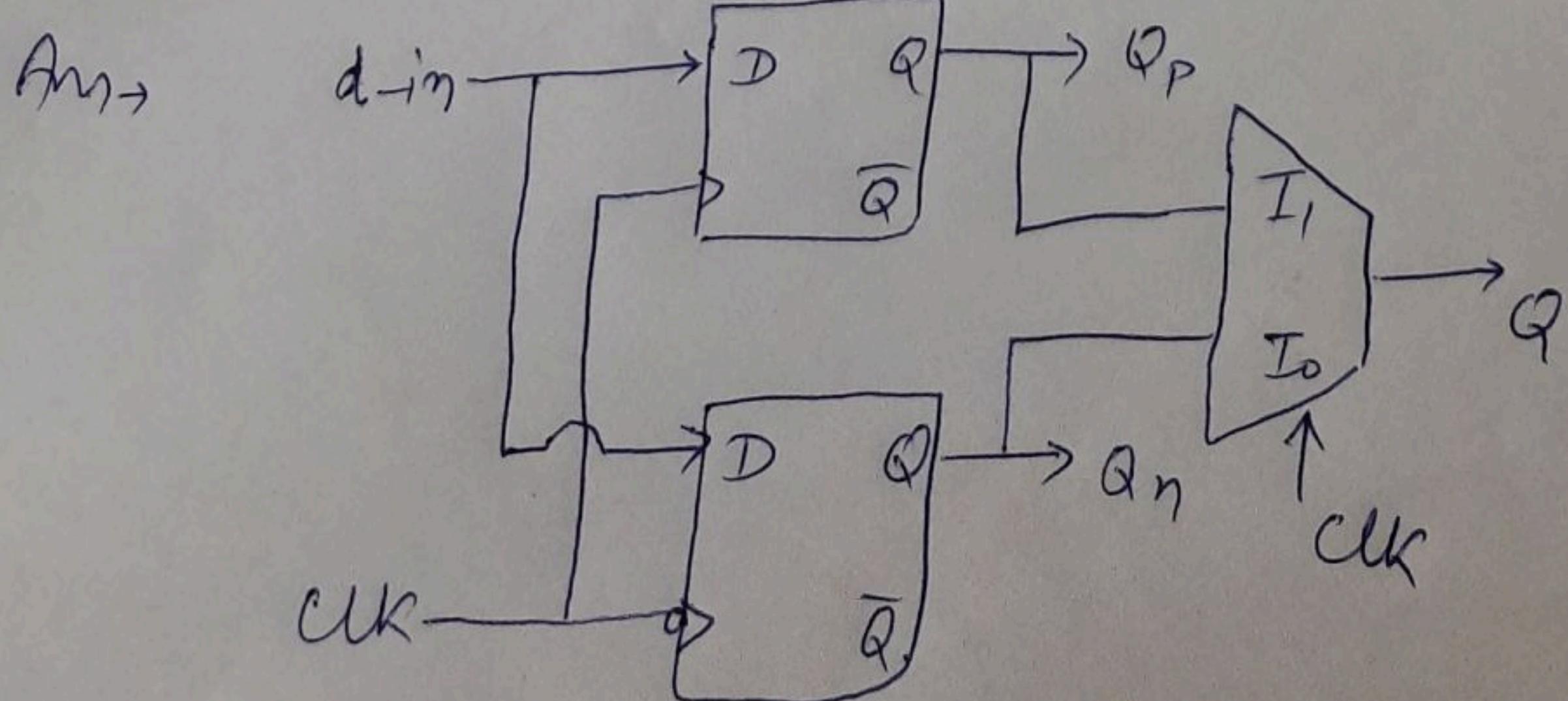
Ans → When $x=0$, O/P is complement of clk signal
When $x=1$, O/P $z=1$



Q19. Design a circuit which can produce a Single Data Rate (SDR) output (one data in one cycle i.e., one data at each posedge)



Q20. Design a ckt. which can produce a Double Data Rate (DDR) output (2 data's in 1 cycle i.e., 1 data at posedge & 1 data at negedge)

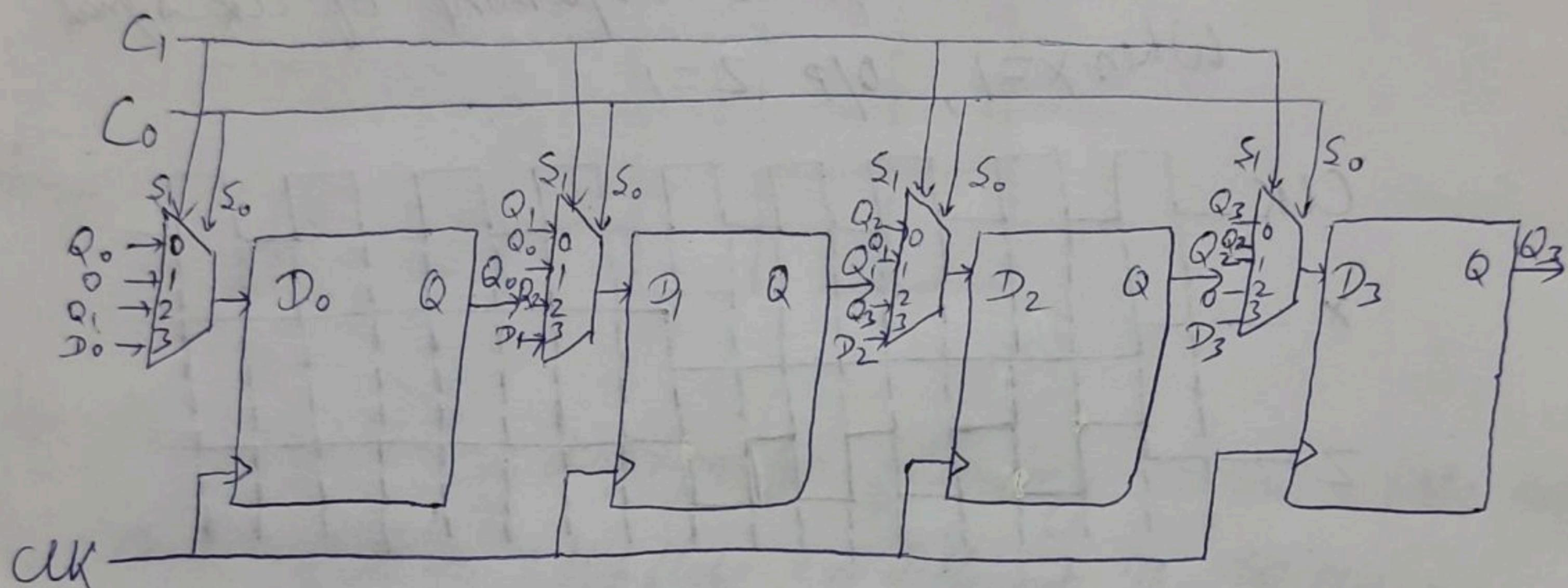


Assignment-5 (Registers & counters)

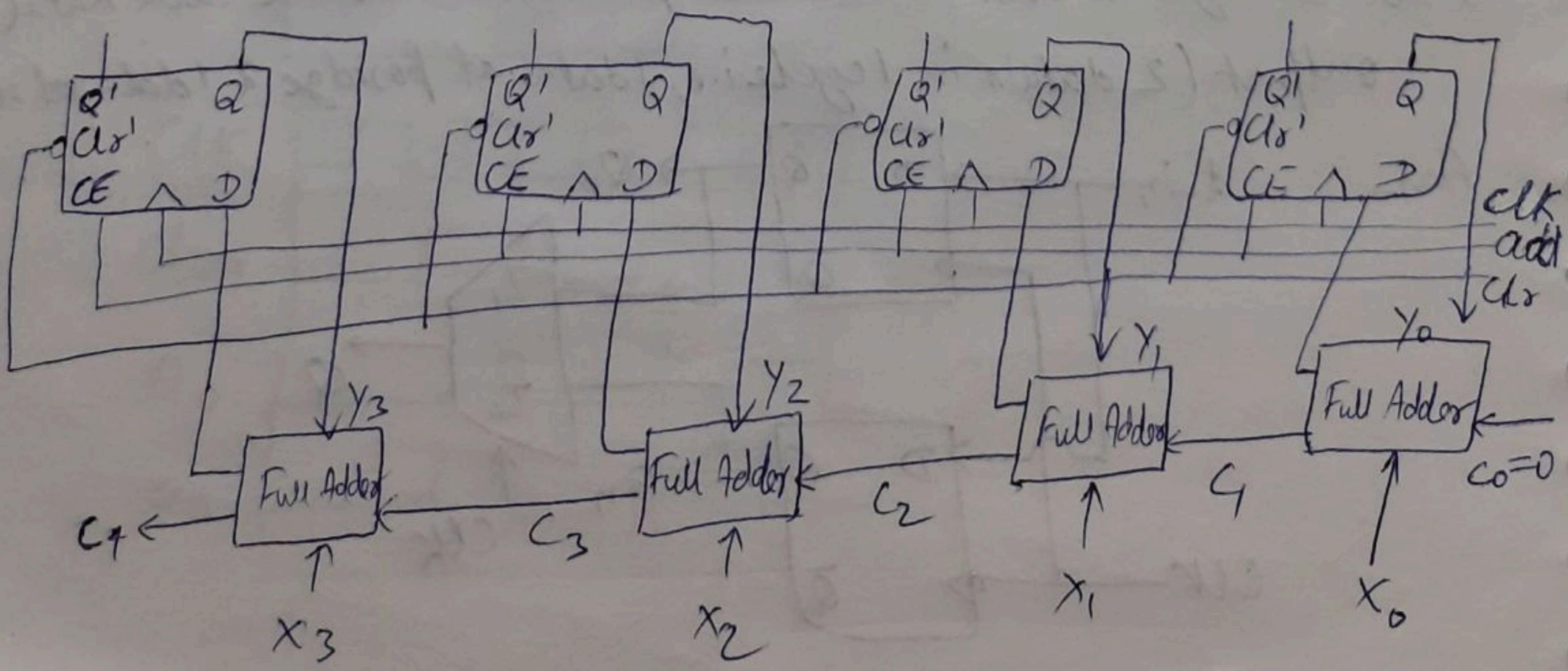
Q1. Design a 4 bit Parallel In Parallel Out Shift Register with 2 control inputs & below given functionality.

<u>C₁</u>	<u>C₀</u>	<u>Action</u>	<u>Q₀</u>	<u>Q₁</u>	<u>Q₂</u>	<u>Q₃</u>
0	0	No change	Q ₀	Q ₁	Q ₂	Q ₃
0	1	Right shift	0	Q ₀	Q ₁	Q ₃
1	0	left shift	Q ₁	Q ₂	Q ₃	0
1	1	Load data	D ₀	D ₁	D ₂	D ₃

Am

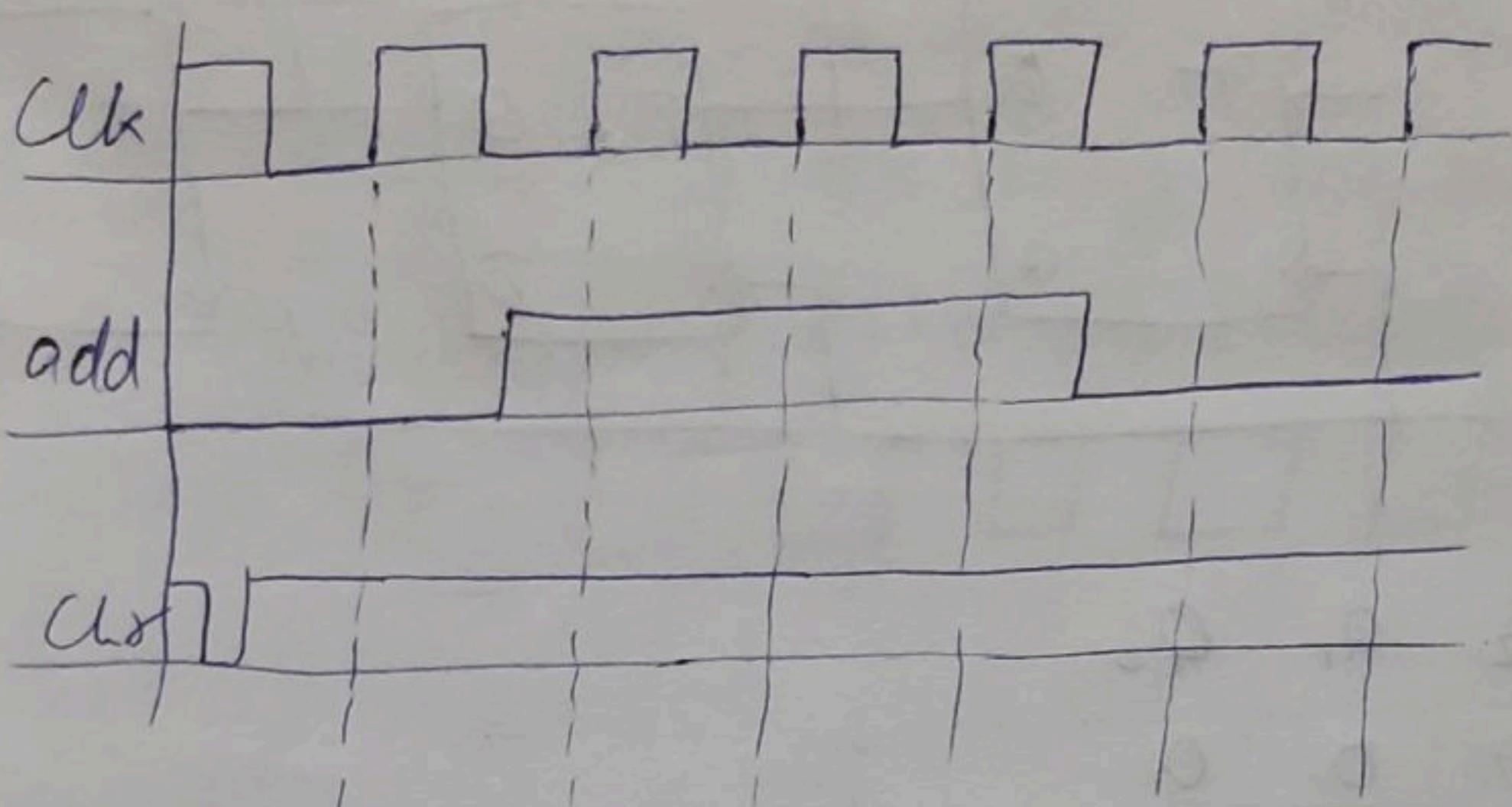


Q2. Consider a 4 bit adder with an accumulator as in below figure. Suppose Y register (with asynchronous clear input) contains a number from a previous calculation. We do not want this number. Instead, we want Y to equal $3XX$ ($X = X_3 X_2 X_1 X_0$ & $Y = Y_3 Y_2 Y_1 Y_0$).

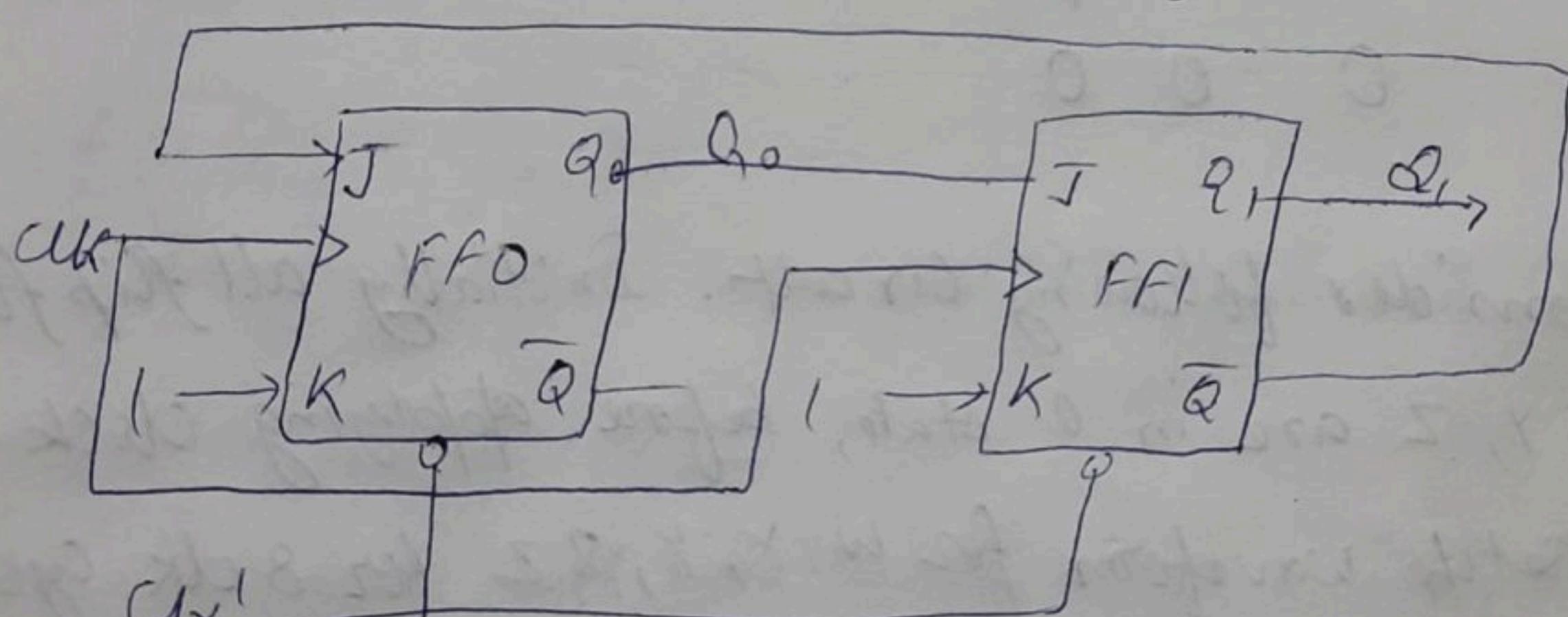


In below timing diagram, give values for 'add' & 'clr' so that we will have $Y = 3 \times X$ held in accumulator.

Ans →



Q3. Determine functional behaviour of ckt in diagram below. Assume that input 'clk' is driven by a square wave signal.



Ans →

Let initial O/P is 0.

$Q_1 \quad Q_0$

0 0

0 1

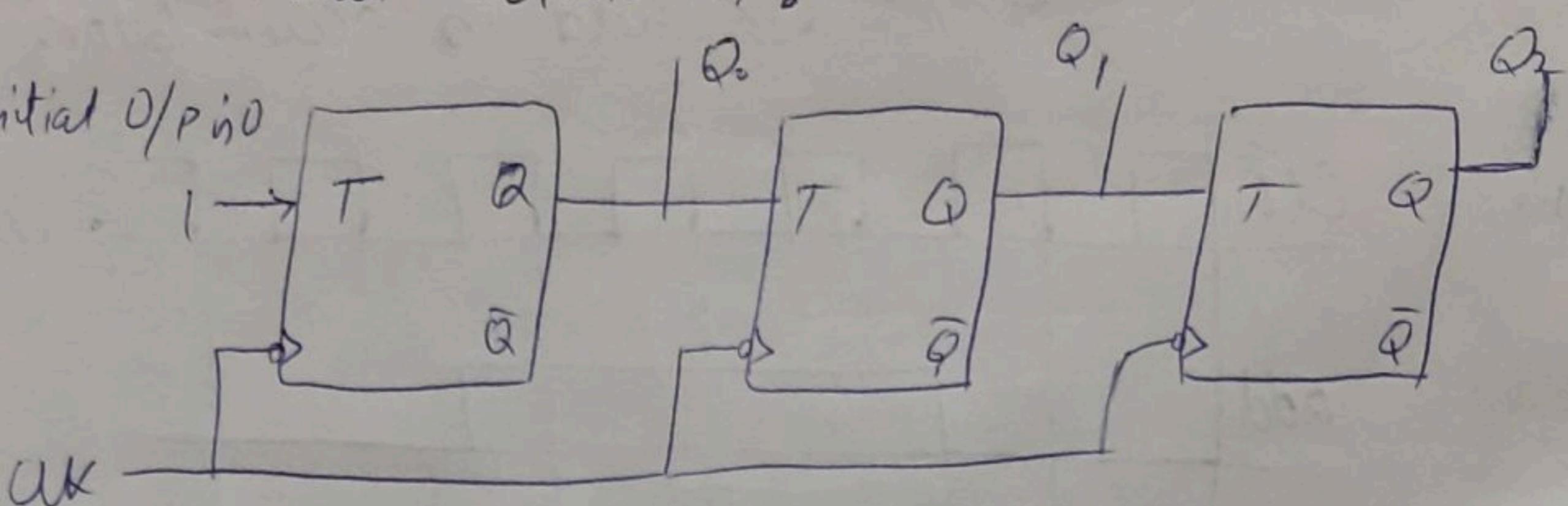
1 0

0 0

So, this circuit work as Mod-3 counter.

Q4. The circuit in figure below is counter. What is sequence that this circuit counts in 2

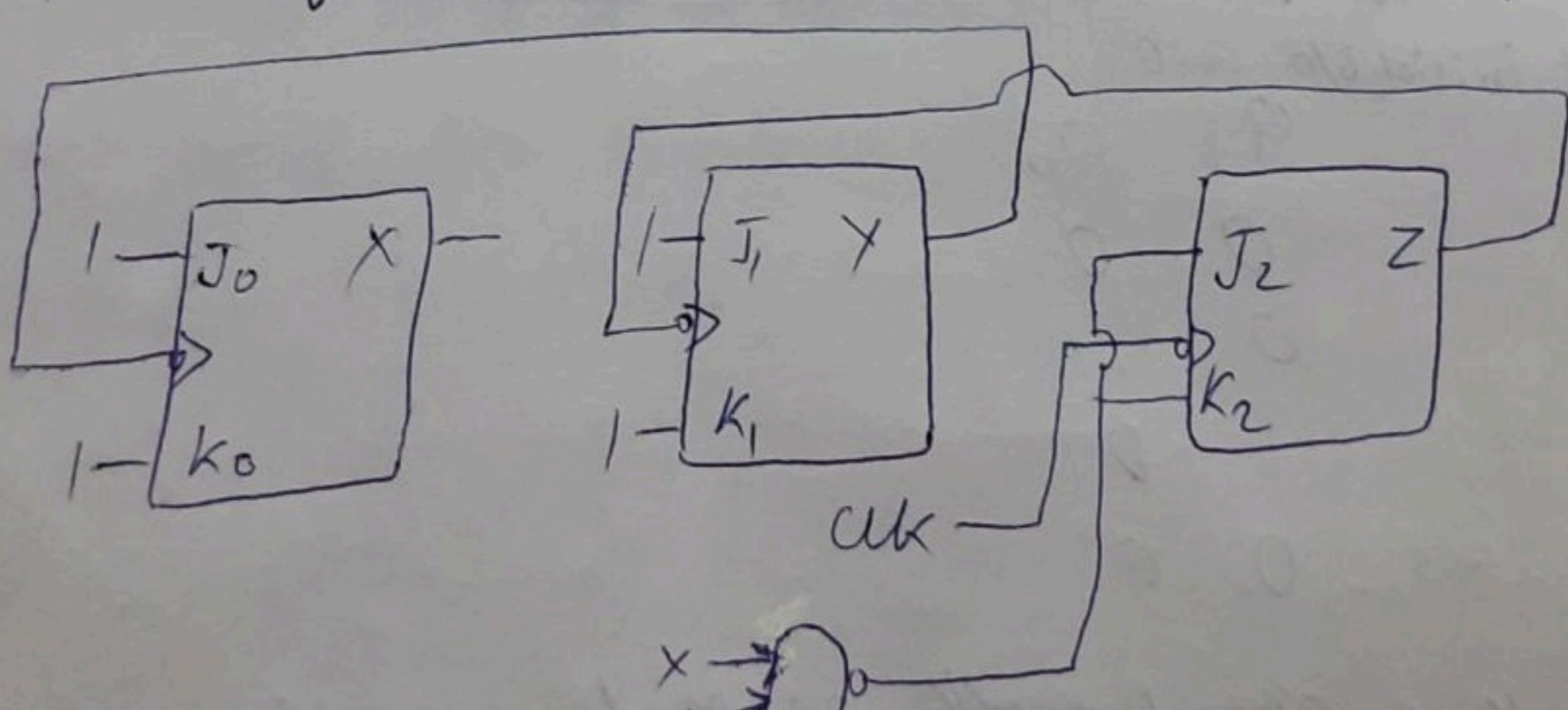
Ans → let initial O/P in 0



	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	0
0	1	0	0
1	1	1	0
0	0	0	0

Q5. Consider following circuit. Initially all flip flop's o/p x, y, z are in 0 state, before applying clock pulses.

Sketch waveform for w, x, y, & z for 8 clk cycles.



Ans →

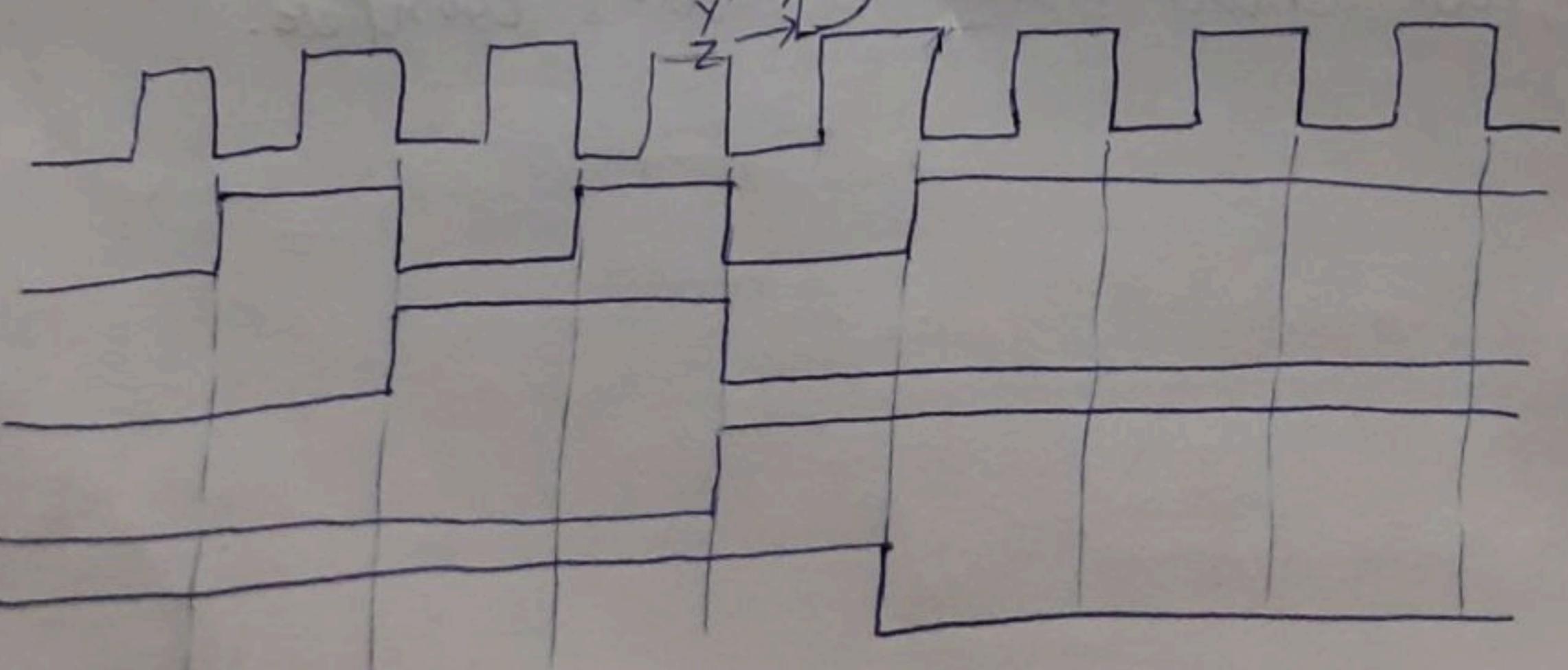
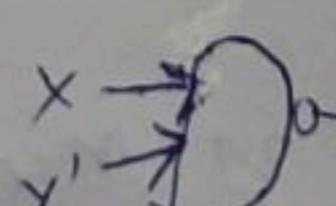
clk

z

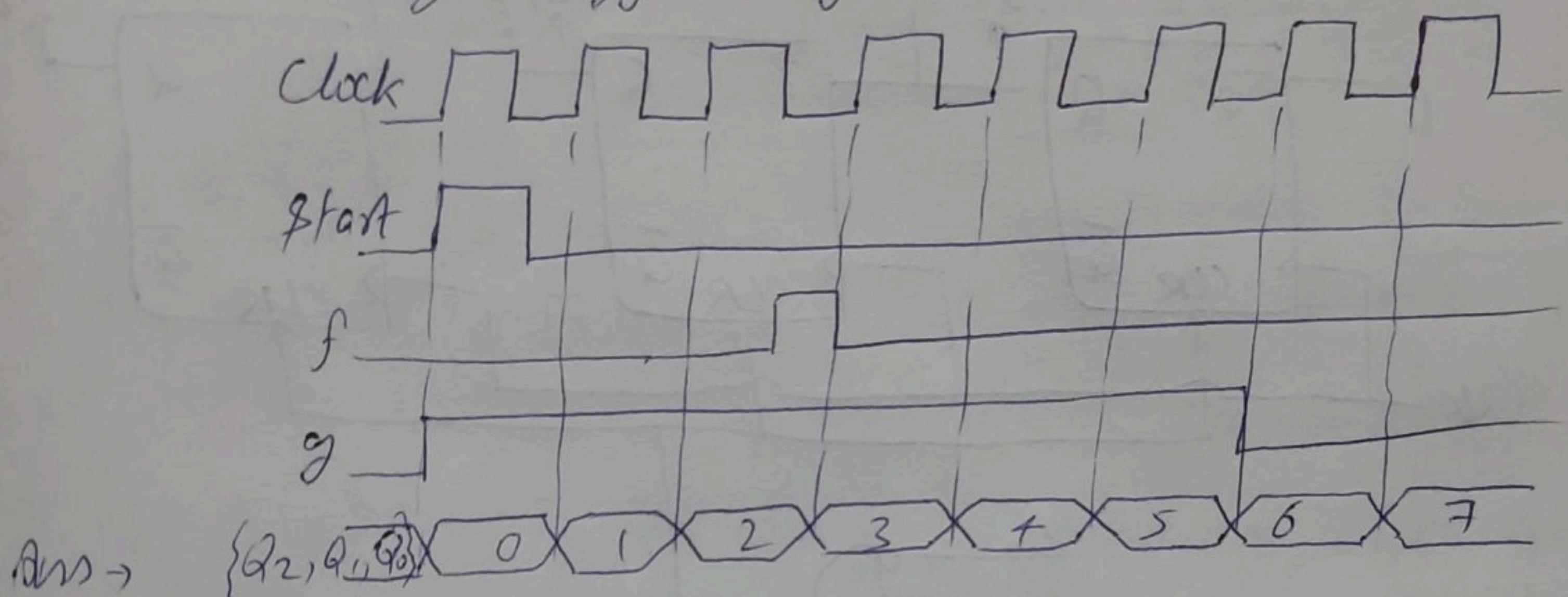
y

x

w



Q6. Design a logic circuit that has 2 I/Ps, Clock & start, and 2 O/Ps f & g. When a pulse is received on 'start' signal the circuit produces pulse on the O/Ps as shown in timing diagram. Design this ckt. using only a 3 bit resettable positive edge triggered synchronous counter & basic gates.



$$f = \overline{Q_2} Q_1 \overline{Q_0} \cdot \bar{clk}$$

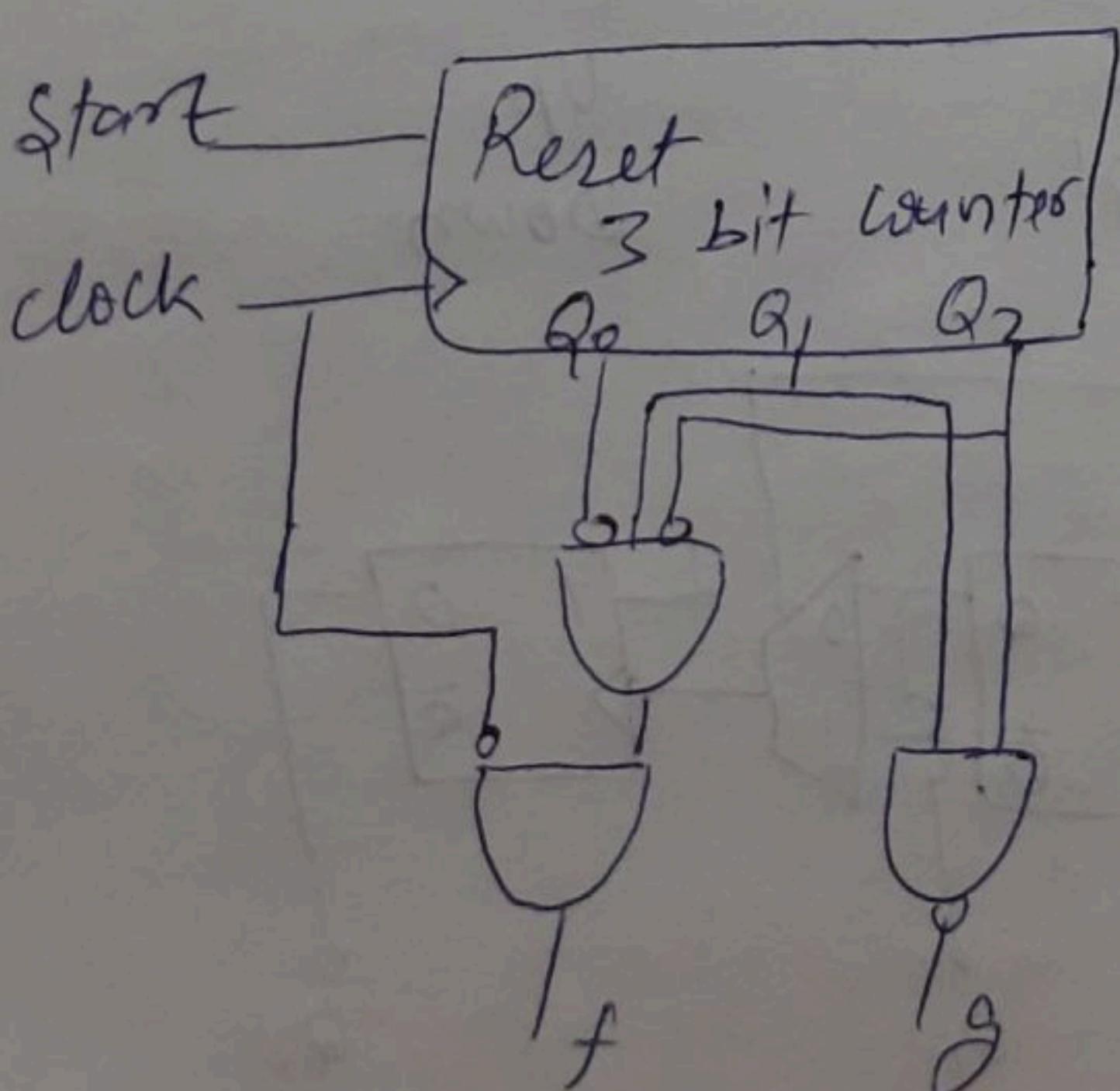
f is becoming high when counter's O/P is 2 & clock is low.

$$g = \sum m[0, 1, 2, 3, 4, 5]$$

g is becoming high when counter's O/P is either 0 or 1 or 2 or 3 or 4 or 5.

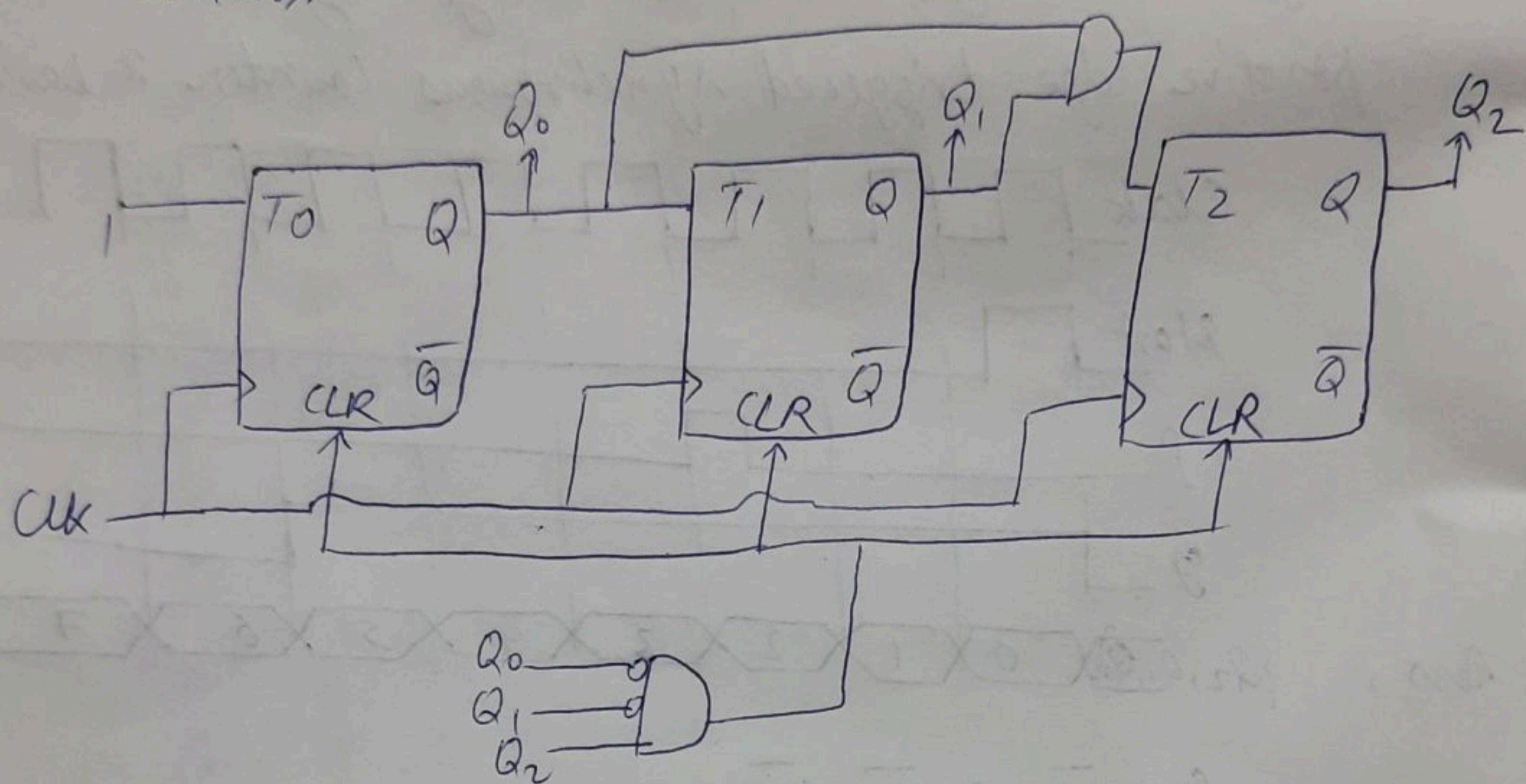
$$g = \overline{Q_1} + \overline{Q_2}$$

$Q_2 Q_1 Q_0$	000	001	010	011	100	101	110	111
$\overline{Q_2}$	1	1	1	1	0	0	0	0
$\overline{Q_1}$	1	0	0	1	1	0	0	1
$\overline{Q_0}$	0	1	1	0	0	1	1	0
	1	1	1	1	1	1	1	1



Q7. Convert a MOD 8 counter made with T flip flops with Synchronous Reset I/P as a MOD 5 counter by using some additional gates & without modifying existing electrical connections.

Ans →



Q8. Design a 3 bit up/down counter using negative edge triggered T-FF.

Ans →

Edge sensitivity of flip flops used Clock Source Counting Sequence

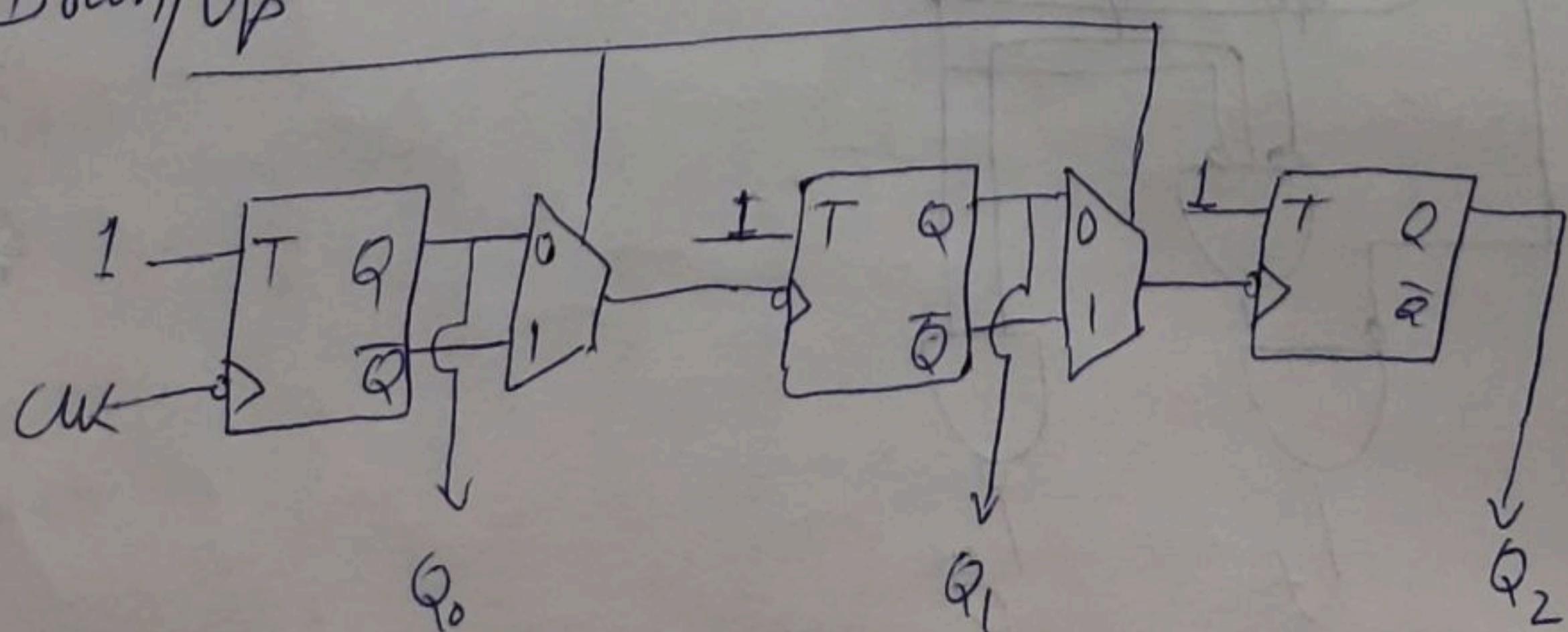
posedge

Q	Down
Q'	Up

negedge

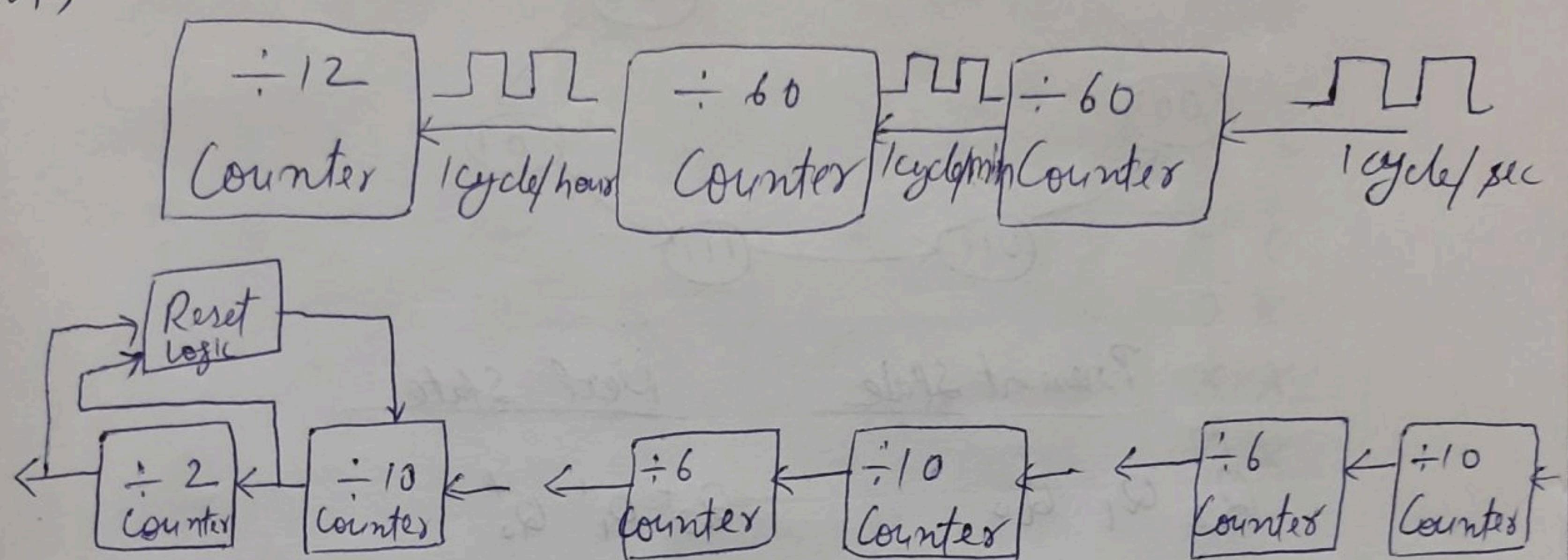
Q	Up
Q'	Down

Down/Up



Q9. Explain how can counters be used to construct a digital clock using 7 segment displays.

Ans →



Q10. Change an n -bit counter (a normal one, which counts in order) to one which counts down rather than up, just by rewiring it, adding no additional circuitry of any kind. (no additional gates)

Ans → Positive edge triggered flip flop

change wiring to Q instead of Q' in b/w the flip flops.

Negative edge triggered flip flop

change wiring to Q' instead of Q in b/w the flip flops.

Q11. An L-M flip flop work as follows-

if $L=M=00$, the next state of ff is 1.

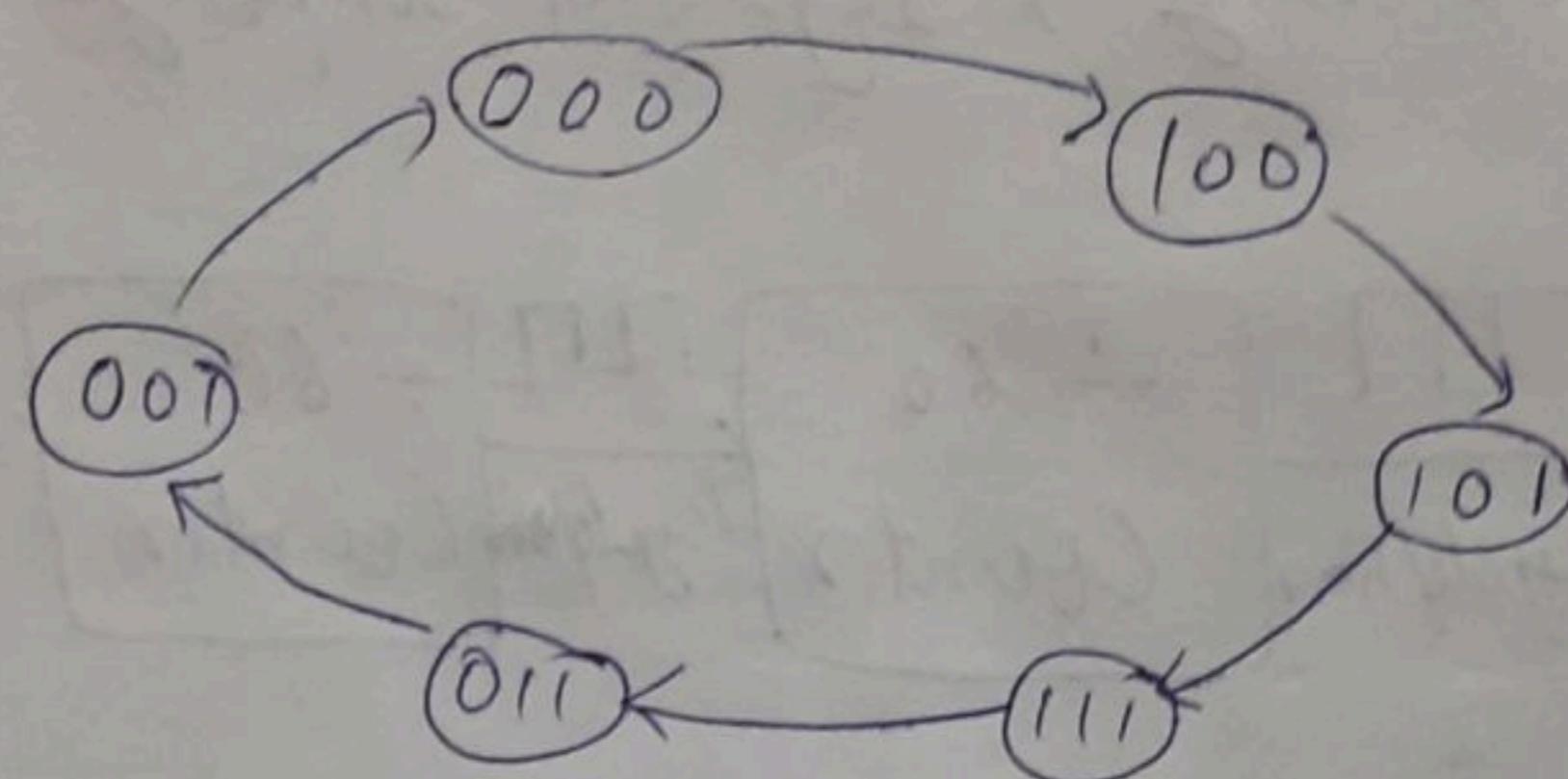
if $L=M=01$, the next state of ff is same as present state.

if $L=M=10$, the next state of ff is complement of present state

if $L=M=11$, the next state of ff is 0.

L	M	Q_{n+1}
0	0	1
0	1	Q_n
1	0	Q_n'
1	1	0

Using this LM flip flop, design a counter with following counting sequence 000, 100, 101, 111, 011, 001, 000 ...



<u>Present State</u>	<u>Next State</u>
$Q_2 \ Q_1 \ Q_0$ 0 0 0	$Q_2^+ \ Q_1^+ \ Q_0^+$ 1 0 0
0 0 1	0 0 0
0 1 0	x x x
0 1 1	0 0 1
1 0 0	1 0 1
1 0 1	1 1 1
1 1 0	x x x
1 1 1	0 1 1

L M	$Q_n \ Q_{n+1}$	State
0 0	0 1	Set
0 0	1 1	Set
0 1	0 0	No change
0 1	1 1	No change
1 0	0 1	Toggle
1 0	1 0	Toggle
1 1	0 0	Reset
1 1	1 1	Reset

<u>Excitation Table</u>		
Q_n	Q_{n+1}	L M
0	0	x 1
0	1	x 0
1	0	1 x
1	1	0 x

<u>Present State</u>	<u>Next State</u>	<u>LM-Inputs</u>
$Q_2 \ Q_1 \ Q_0$	$Q_2' \ Q_1' \ Q_0'$	$L_2 \ M_2 \ L_1 \ M_1 \ L_0 \ M_0$
0 0 0	1 0 0	x 0 x 1 x 1
0 0 1	0 0 0	x 1 x 1 1 x
0 1 0	x x x	x x x x x x
0 1 1	0 0 1	x 1 1 x 0 x
1 0 0	1 0 1	0 x x 1 x 0
1 0 1	1 1 1	0 x x 0 0 x
1 1 0	x x x	x x x x x x
1 1 1	0 1 1	1 x 0 x 0 x

$$M_0 = f(Q_2, Q_1, Q_0) = \sum m(0) + \sum d(1, 2, 3, 5, 6, 7) = \overline{Q_2}$$

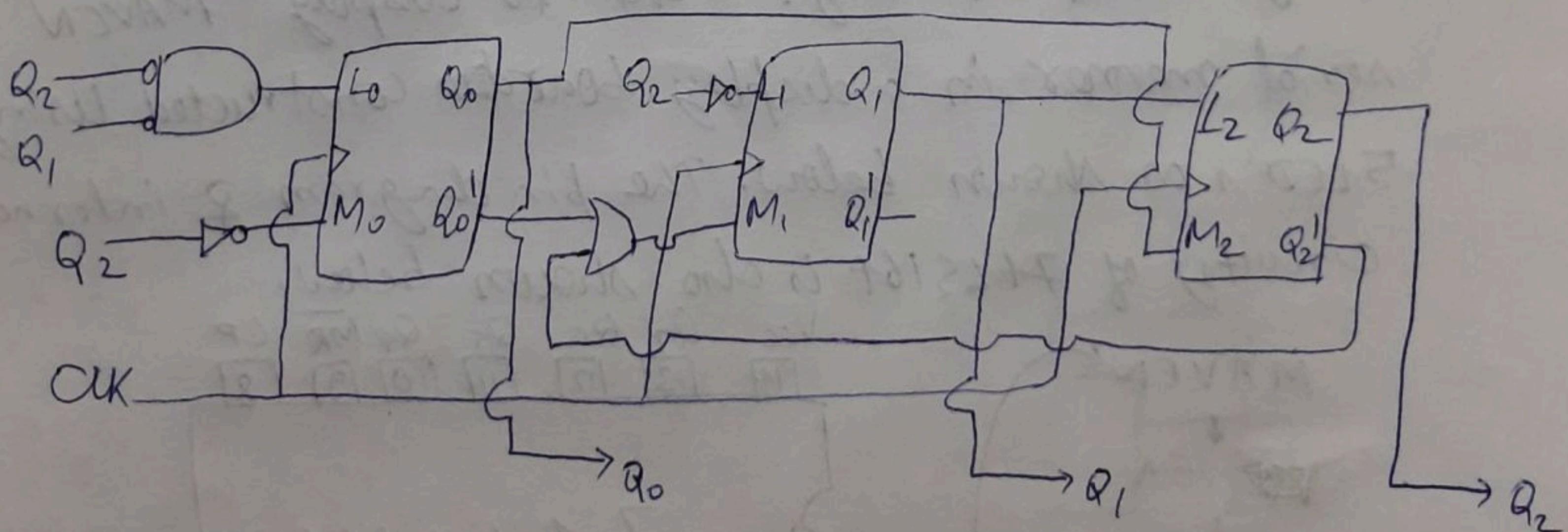
$$L_0 = f(Q_2, Q_1, Q_0) = \sum m(1) + \sum d(0, 2, 4, 6) = \overline{Q_1} \overline{Q_2}$$

$$M_1 = f(Q_2, Q_1, Q_0) = \sum m(0, 1, 4) + \sum d(2, 3, 6, 7) = \overline{Q_2} + \overline{Q_0}$$

$$L_1 = f(Q_2, Q_1, Q_0) = \sum m(3) + \sum d(0, 1, 2, 5, 6) = \overline{Q_2}$$

$$M_2 = f(Q_2, Q_1, Q_0) = \sum m(1, 3) + \sum d(2, 4, 5, 6, 7) = Q_0$$

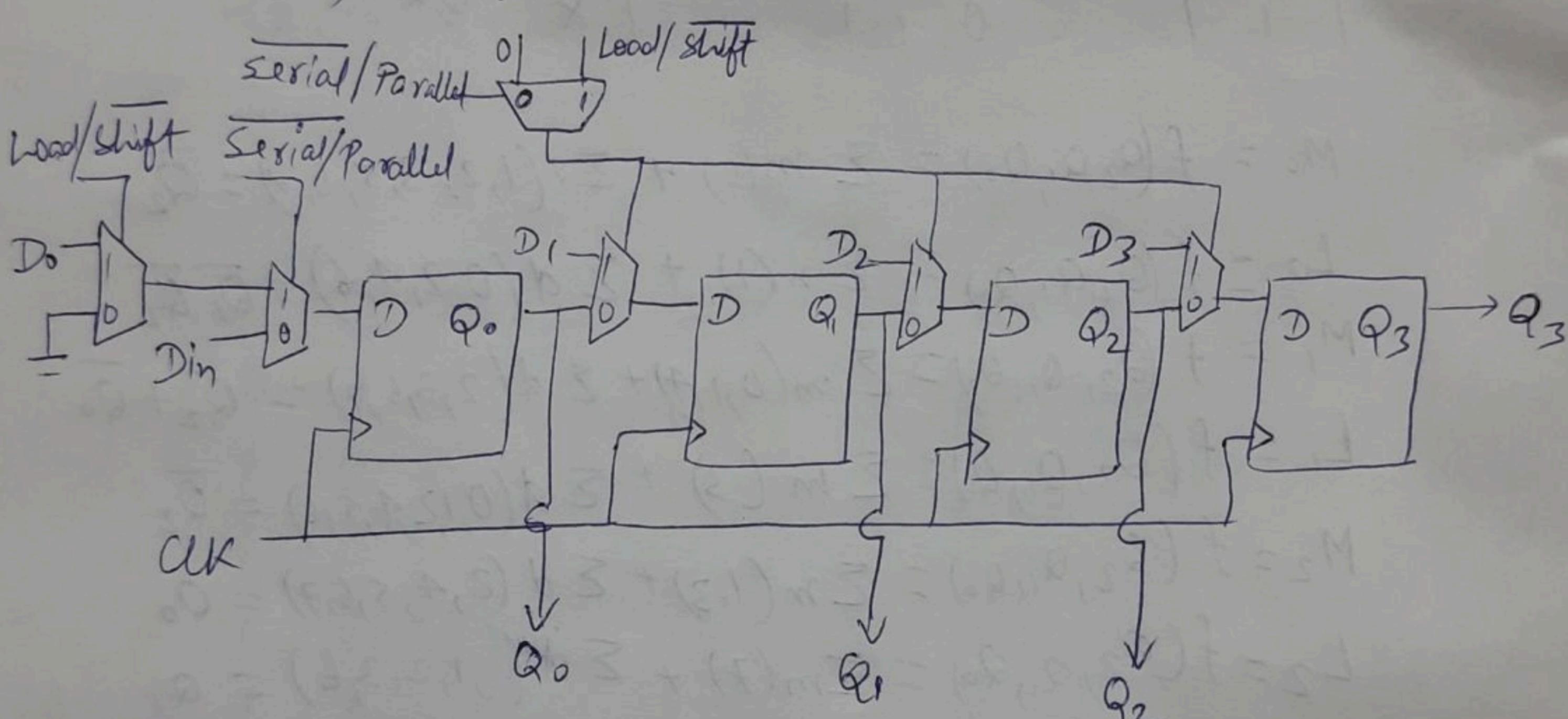
$$L_2 = f(Q_2, Q_1, Q_0) = \sum m(7) + \sum d(0, 1, 2, 3, 6) = Q_1$$



Q12. Design a 4 bit right shift register with one mode signal. If mode signal is logic 0, ckt. should work like Serial In Parallel Out Shift Register. And if mode signal is logic 1, ckt. should work like Parallel In Parallel Out Shift Register.

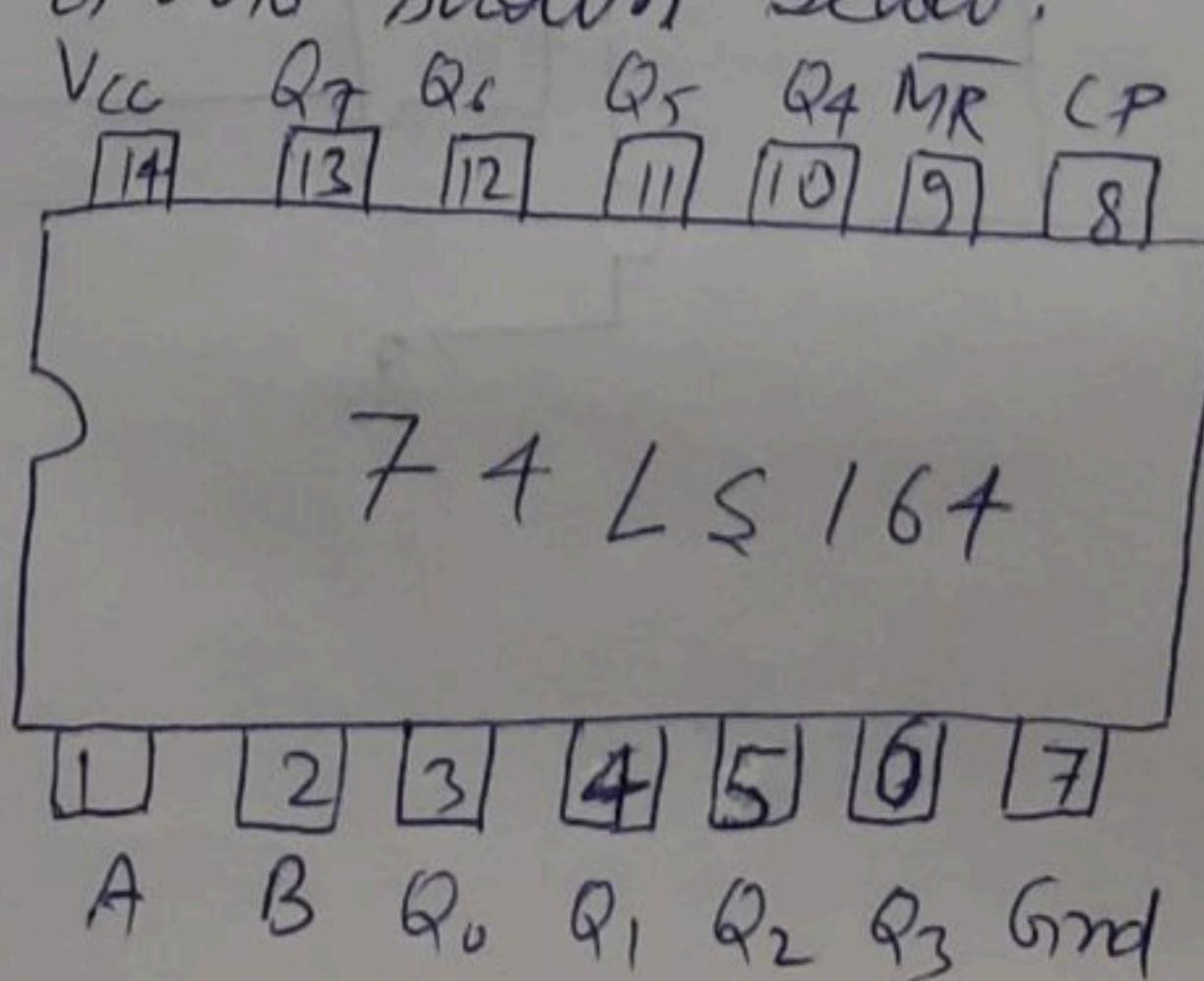
Ans

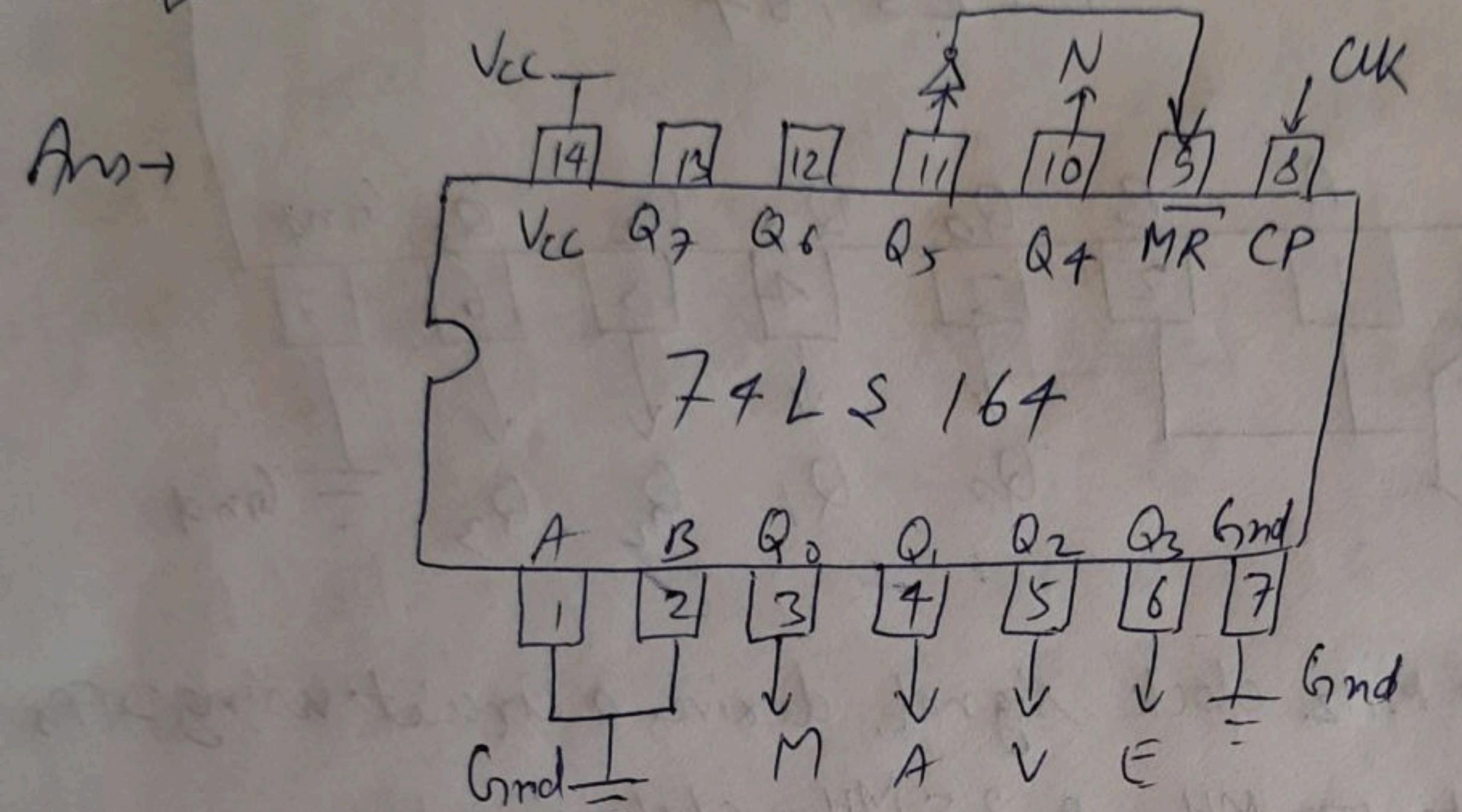
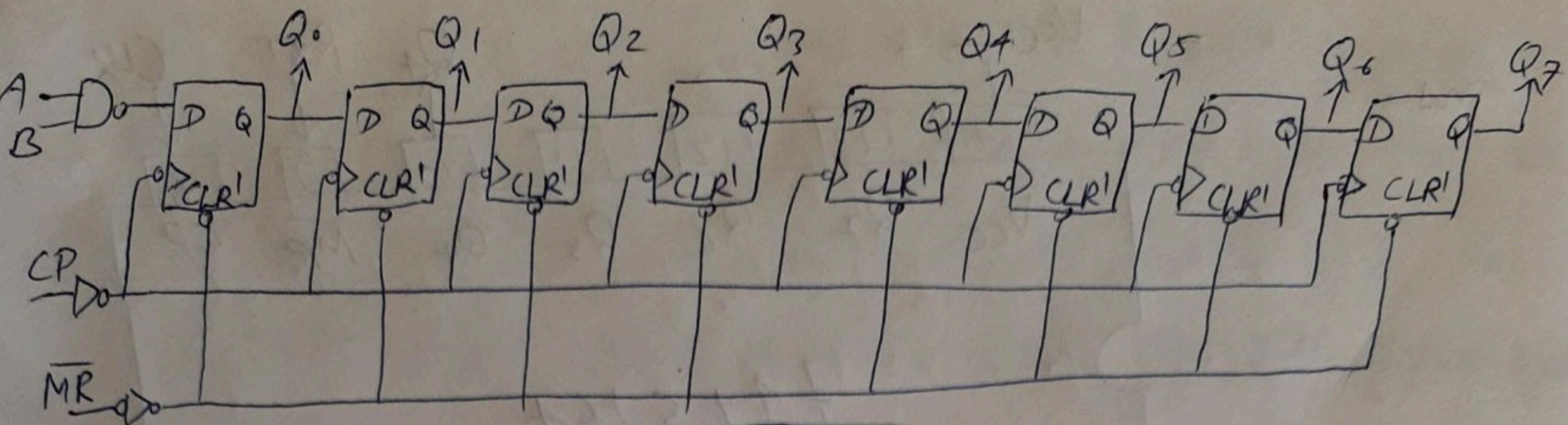
Mode	Action	Q_0	Q_1	Q_2	Q_3
serial ($m=0$)	Serial	D_{in}	Q_0	Q_1	Q_2
Parallel ($m=1$)	Load	D_0	D_1	D_2	D_3
Parallel ($m=1$)	shift	0	Q_0	Q_1	Q_2



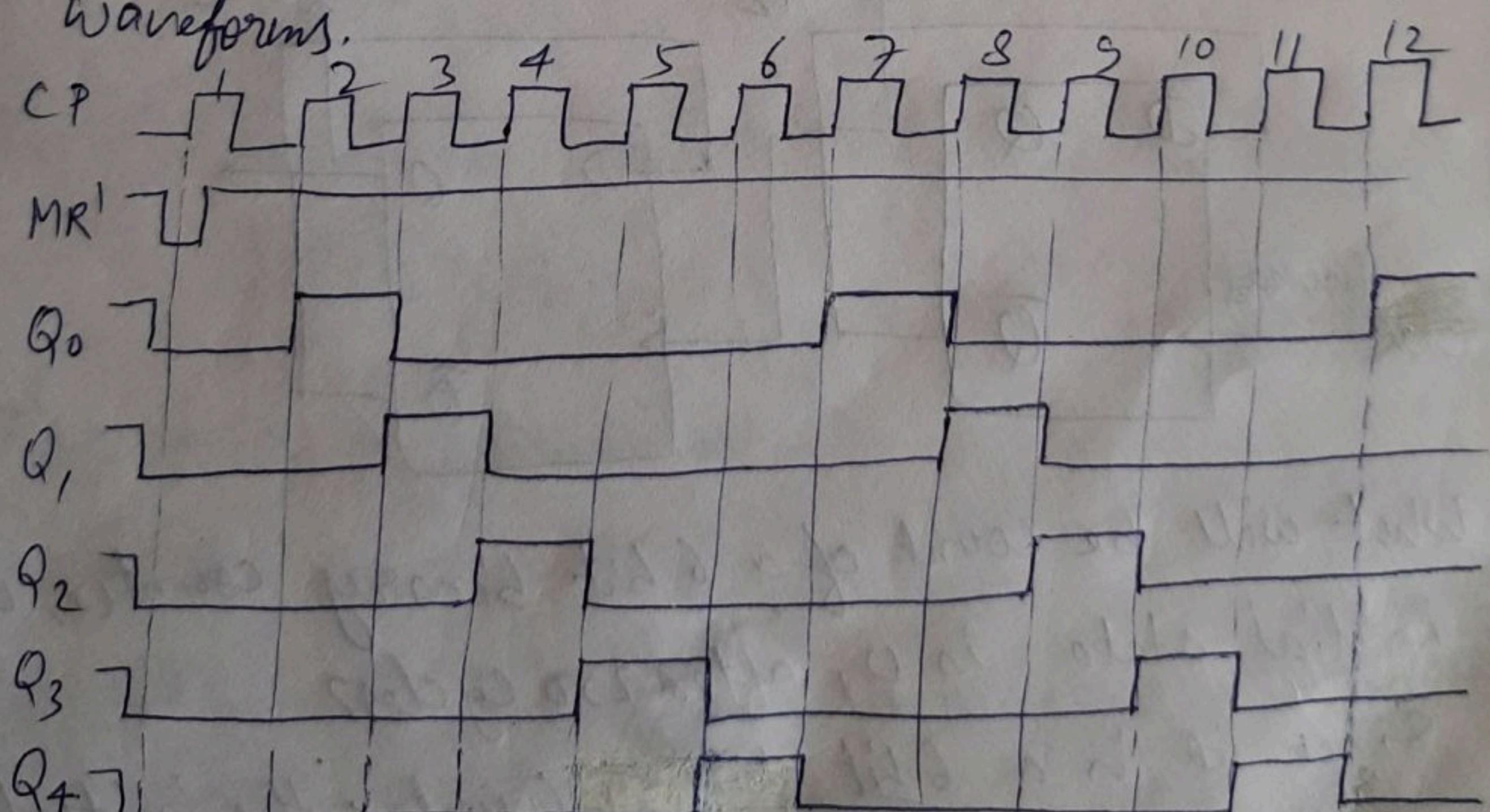
Q13. Using 74LS164, design a ckt to display "MAVEN" in serial manner in a display board constructed using 5 LED's as shown below. The pin diagram & internal circuitry of 74LS164 is also shown below.

MAVEN
↓
MAVEN
↓
MAVEN
↓
MAVEN
↓
MAVEN
↓
MAVEN

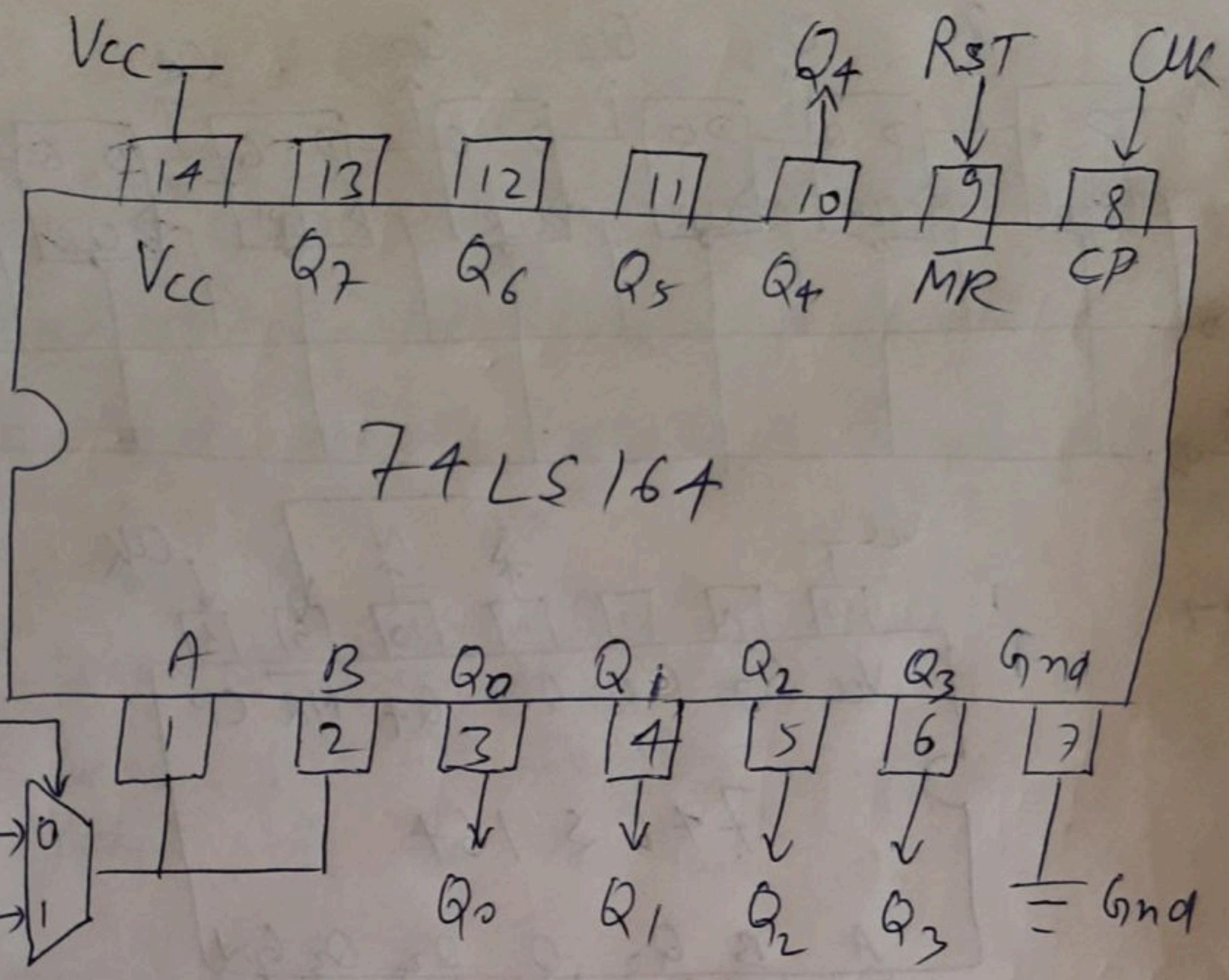




Q14. Use some combination of ~~at least~~ blocks & same 74LS164 described in previous question to mimic behavior of a 5bit ring counter whose functionality is described with following waveforms.

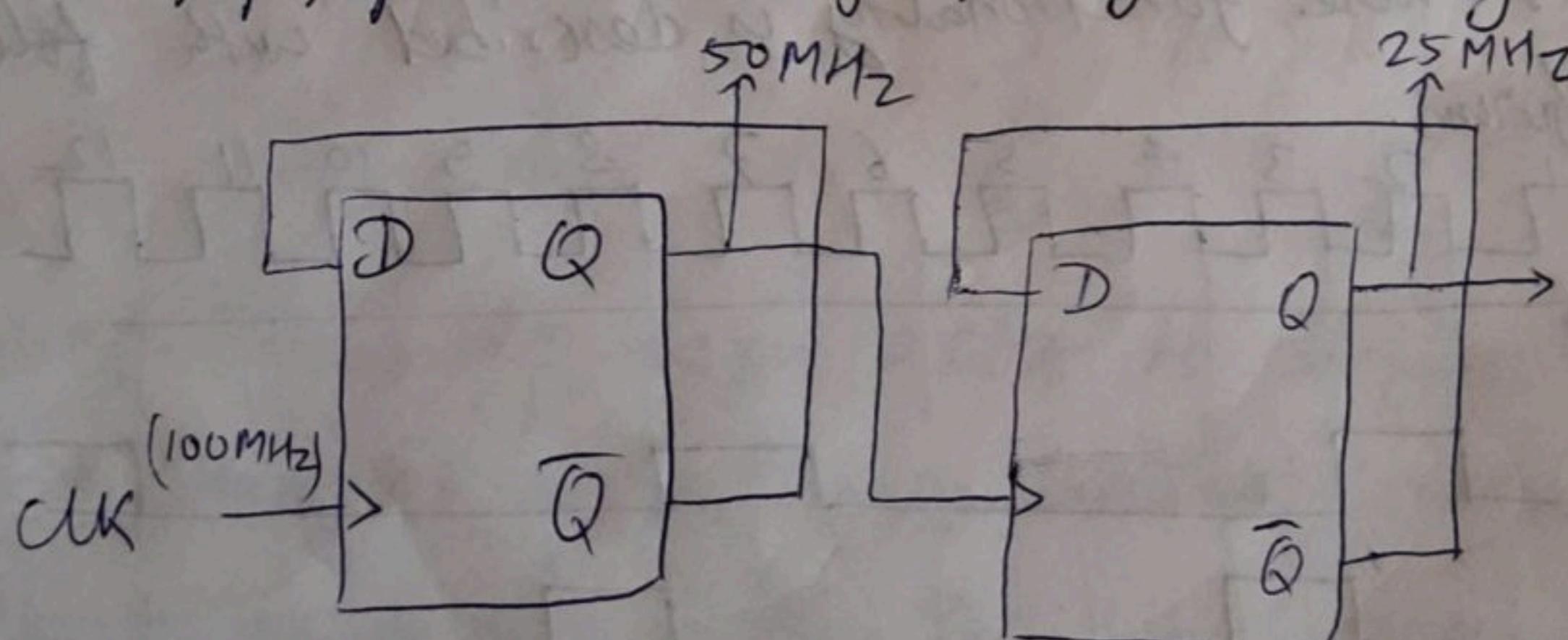


Ans →



Q15. Given a 100 MHz clock signal, derive a circuit using DFFs to generate 50 MHz & 25 MHz clock signals.

Ans → If we connect Q' output of a 'D' flip flop to 'D' input, the flip flop acts as a frequency divide by 2 circuit.



Q16. What will be count of a 6 bit binary counter, whose initial state is 0, after 250 cycles?

Ans → since it is a 6 bit binary counter, the initial count repeats after every 64 clock cycles.

$0 \rightarrow 0$	$255 \rightarrow 63$
$64 \rightarrow 0$	$254 \rightarrow 62$
$128 \rightarrow 0$	$253 \rightarrow 61$
$192 \rightarrow 0$	$252 \rightarrow 60$
$256 \rightarrow 0$	$251 \rightarrow 59$
	$250 \rightarrow 58$

Q17. A 3 bit ring counter's initial state output is 0100010. After how many clock cycles, will it return to initial state?

Ans → Since, modulus of 3 bit ring Counter is 7, this counter will return to initial state after 7 No. of clock cycles.

Q18. Design a counter with T flip flops whose count sequence is 0, 2, 4, 5, 3, 1, 0 ...

<u>Present State</u>	<u>Next state</u>	<u>T-Input</u>
$Q_2 \ Q_1 \ Q_0$	$Q_2 + Q_1 + Q_0$	$T_2 \ T_1 \ T_0$
0 0 0	0 1 0	0 1 0
0 0 1	0 0 0	0 0 1
0 1 0	1 0 0	1 1 0
0 1 1	0 0 1	0 1 0
1 0 0	1 0 1	0 0 1
1 0 1	0 1 1	1 1 0
1 1 0	x x x	x x x
1 1 1	x x x	x x x

$$T_0 = f(Q_2, Q_1, Q_0) = \sum_m(1, 4) + \sum_d(6, 7)$$

$$= \bar{Q}_2 \bar{Q}_1 Q_0 + Q_2 \bar{Q}_0$$

Q_2	Q_1	Q_0	$\bar{Q}_2 \bar{Q}_1 \bar{Q}_0$	$\bar{Q}_2 \bar{Q}_1 Q_0$	$Q_2 \bar{Q}_1 \bar{Q}_0$	$Q_2 \bar{Q}_1 Q_0$	$Q_2 Q_1 \bar{Q}_0$
-	0	1	1	3	2		
\bar{Q}_2	0	1	1	3	2		
\bar{Q}_2	1	0	1	3	2		
Q_2	1	1	0	1	3	2	
Q_2	1	1	1	x	x	x	x
Q_2	1	1	1	x	x	x	x

$$T_1 = f(Q_2, Q_1, Q_0) = \sum m(0, 2, 3, 5) + \sum d(6, 7)$$

$$= Q_1 + \bar{Q}_2 \bar{Q}_0 + Q_2 Q_0$$

Q_2	Q_1	Q_0	$\bar{Q}_2 \bar{Q}_0$	$\bar{Q}_2 Q_0$	$Q_2 \bar{Q}_0$	$Q_2 Q_0$
-	0	1	1	3	2	
\bar{Q}_2	0	1	1	3	2	
\bar{Q}_2	1	0	1	3	2	
Q_2	1	1	0	1	3	2
Q_2	1	1	1	x	x	x
Q_2	1	1	1	x	x	x

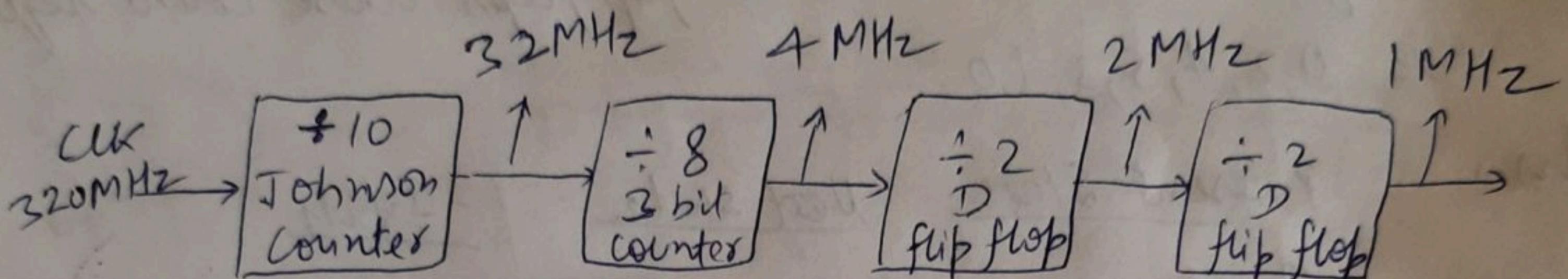
$$T_2 = f(Q_2, Q_1, Q_0) = \sum m(2, 5) + \sum d(6, 7)$$

$$= Q_2 Q_0 + Q_1 \bar{Q}_0$$

Q_2	Q_1	Q_0	$\bar{Q}_2 \bar{Q}_0$	$\bar{Q}_2 Q_0$	$Q_2 \bar{Q}_0$	$Q_2 Q_0$
-	0	1	1	3	2	
\bar{Q}_2	0	1	1	3	2	
\bar{Q}_2	1	0	1	3	2	
Q_2	1	1	0	1	3	2
Q_2	1	1	1	x	x	x
Q_2	1	1	1	x	x	x

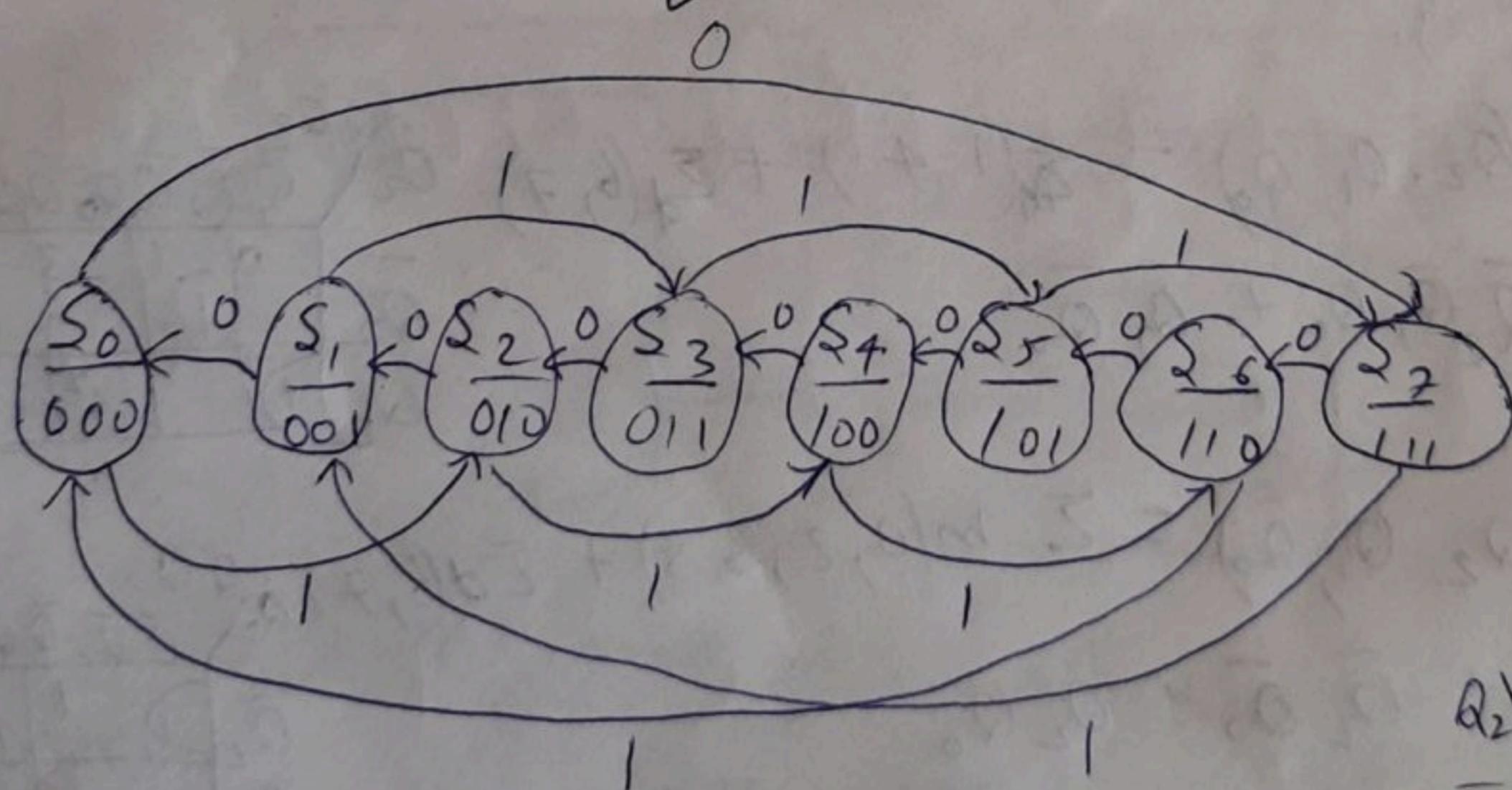
Q19. Show how 3 bit binary counters, 5 bit Johnson counters & D flip flops can be used to derive a signal with frequency of 1 MHz from an input clock with a frequency of 320 MHz.

Ans →



Q20. Design a 3 bit counter like circuit controlled by the input w, if $w=1$, then counter adds 2 to its contents, wrapping around if count reaches 8 or 9. Thus if present state is 6 or 7 then next state becomes 0 or 1 respectively. If $w=0$, then counter subtracts 1 from its contents, acting like a normal down counter.

Ans →



Present State Next state w=0 D-Input

Q_2	Q_1	Q_0	$Q_2 + Q_1 + Q_0$	D_2	D_1	D_0
0	0	0	1	1	1	1
0	0	1	0	0	0	0
0	1	0	0	0	1	0
0	1	1	0	1	0	0
1	0	0	0	1	1	1
1	0	1	1	0	0	0
1	1	0	1	0	0	1
1	1	1	0	1	0	0

Q_2	Q_1	Q_0	$\bar{Q}_2 \bar{Q}_1 \bar{Q}_0$	$\bar{Q}_1 \bar{Q}_0$	$Q_1 Q_0$	$Q_1 \bar{Q}_0$
0	0	0	1	1	0	0
0	0	1	0	0	1	0
0	1	0	0	0	0	1

$$D_2 = \bar{Q}_2 \bar{Q}_1 \bar{Q}_0 + Q_2 \bar{Q}_1 \bar{Q}_0 + Q_2 Q_1 \bar{Q}_0$$

Q_2	Q_1	Q_0	$\bar{Q}_2 \bar{Q}_1 \bar{Q}_0$	$Q_2 \bar{Q}_1 \bar{Q}_0$	$Q_2 Q_1 \bar{Q}_0$
0	0	0	1	0	0
0	0	1	0	1	0
0	1	0	0	0	1

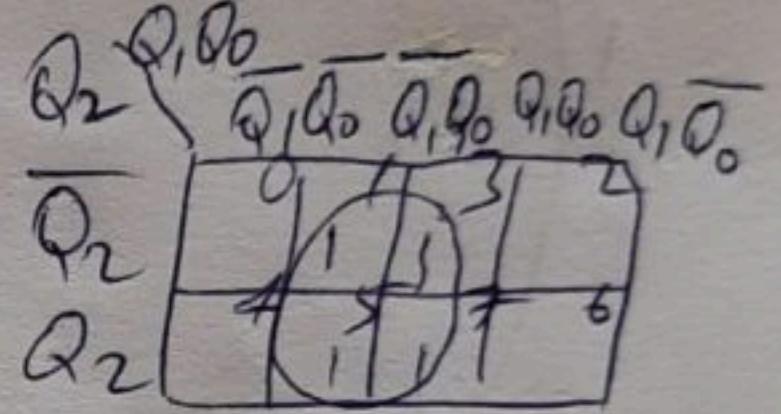
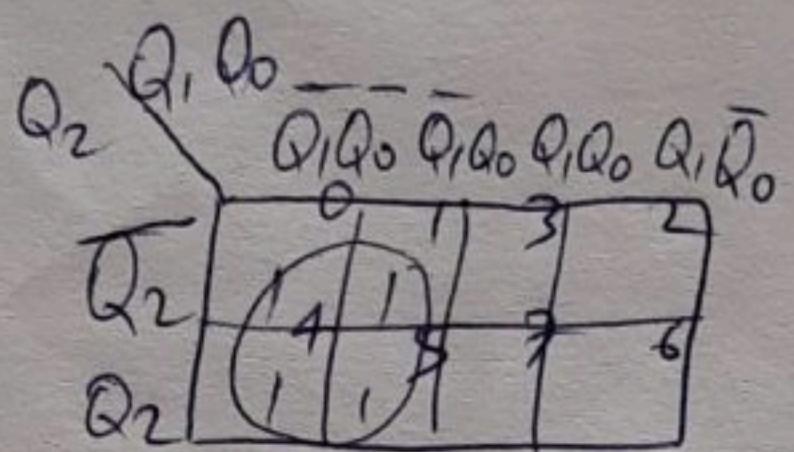
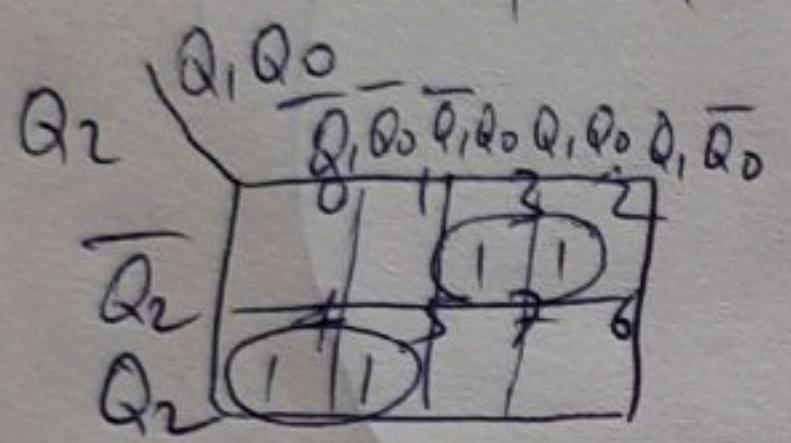
$$D_1 = Q_1 \bar{Q}_0 + Q_1 Q_0$$

$$D_0 = \bar{Q}_0$$

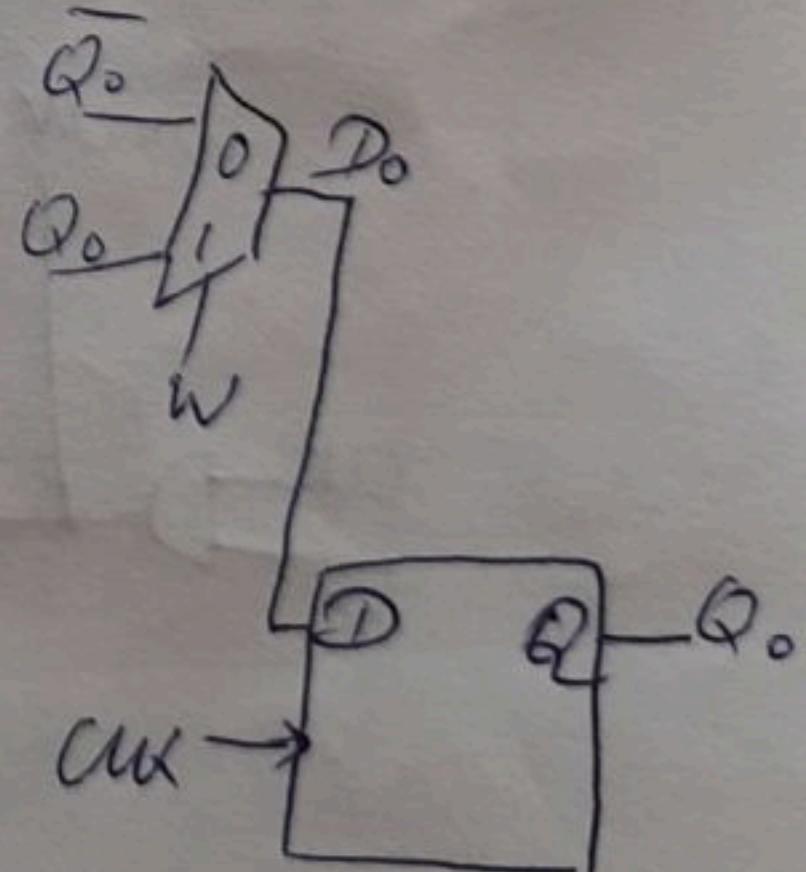
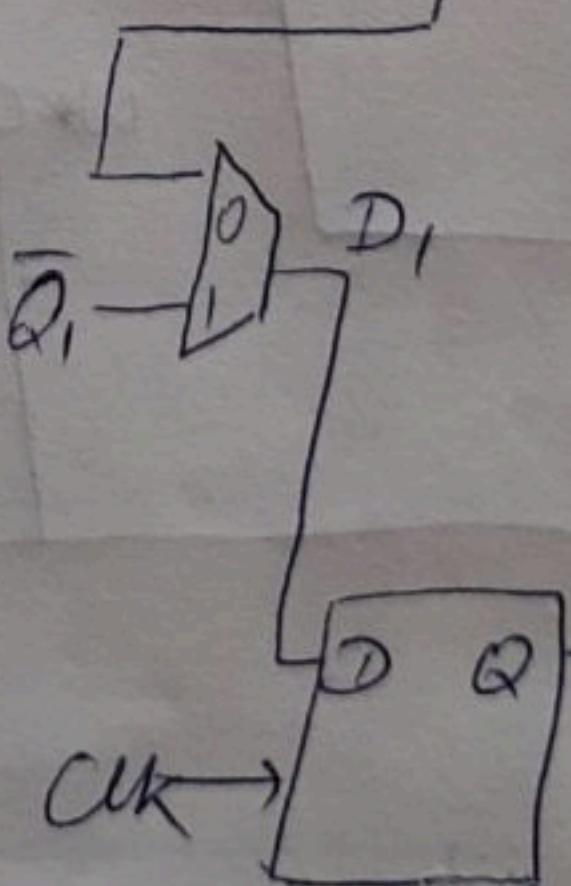
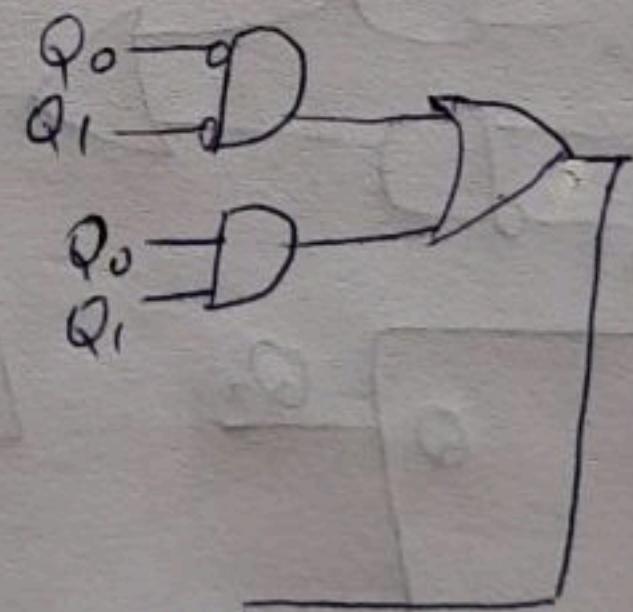
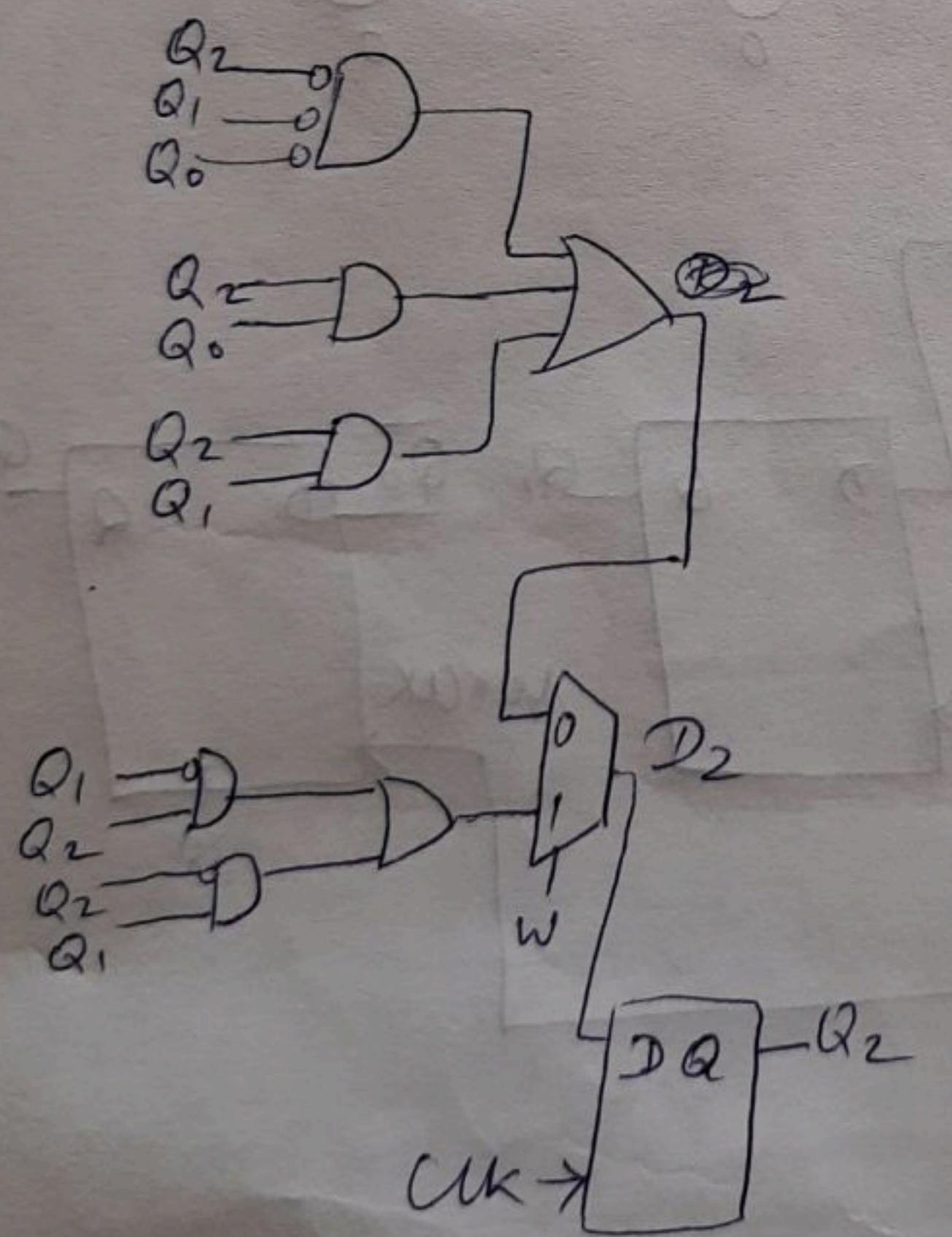
Q_2	Q_1	Q_0	$\bar{Q}_2 \bar{Q}_1 \bar{Q}_0$	$\bar{Q}_2 \bar{Q}_1 Q_0$	$\bar{Q}_2 Q_1 \bar{Q}_0$	$Q_2 \bar{Q}_1 \bar{Q}_0$
0	0	0	1	1	0	0
0	0	1	0	0	1	0
0	1	0	0	0	0	1
0	1	1	1	0	0	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	0	0	1
1	1	1	0	0	0	0

Present state Next State w=1 D T-Input

$Q_2 \ Q_1 \ Q_0$	$Q_2 + Q_1 + Q_0 +$	$D_2 \ D_1 \ D_0$
0 0 0	0 1 0	0 1 0
0 0 1	0 1 1	0 1 1
0 1 0	1 0 0	1 0 0
0 1 1	1 0 1	1 0 1
1 0 0	1 1 0	1 1 0
1 0 1	1 1 1	1 1 1
1 1 0	0 0 0	0 0 0
1 1 1	0 0 1	0 0 1



$$D_2 = Q_2 \bar{Q}_1 + \bar{Q}_2 Q_1 \quad D_1 = \bar{Q}_1 \quad D_0 = Q_0$$

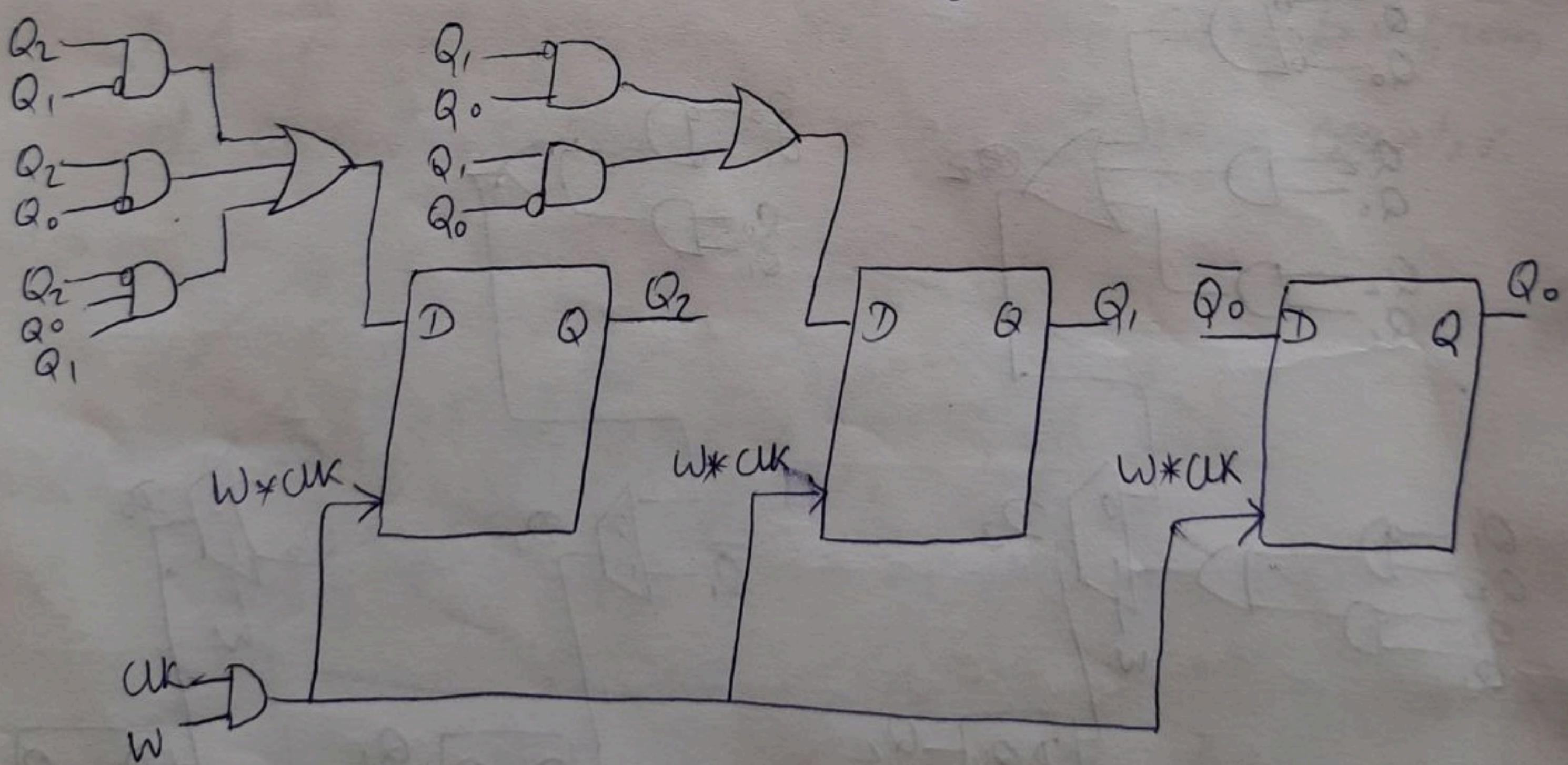
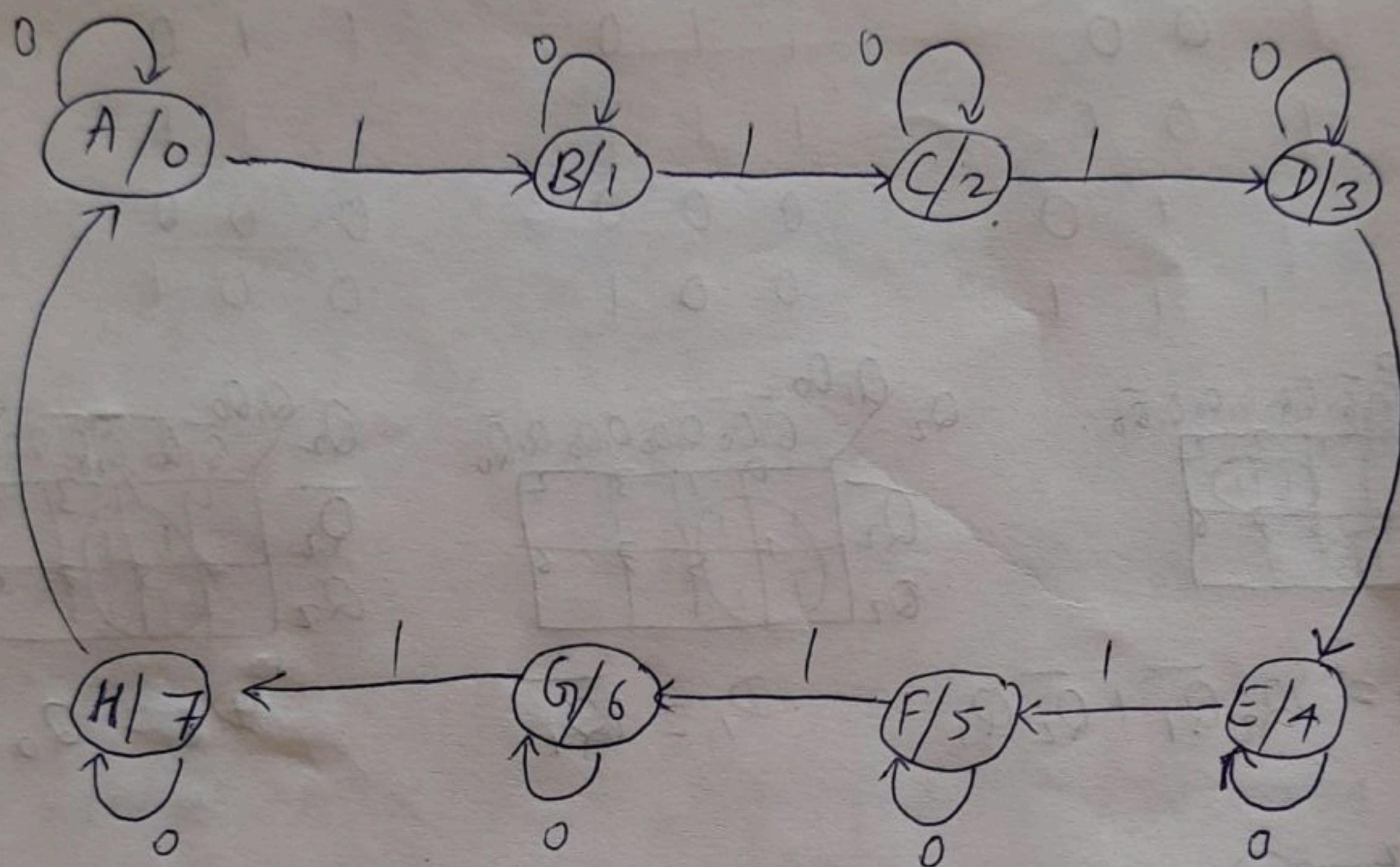


Q21. Design a counter using D flipflops 8 with following specifications:

The counting sequence is 0, 1, 2, ..., 6, 7, 0, 1, ...

There is an input signal w ; if $w=0$, the present count remains the same & if $w=1$, the count increments by 1.

Ans →



Q22. Design a counter which counts following given sequence.

Use D flip flops & NAND gates.

000, 110, 111, 100, 101, 001, 000, ...

<u>Ans → Present State</u>	<u>Next State</u>	<u>D - Input</u>
$Q_2 \ Q_1 \ Q_0$	$Q_2 + Q_1 + Q_0 +$	$D_2 \ D_1 \ D_0$
0 0 0	1 1 0	1 1 0
0 0 1	0 0 0	0 0 0
0 1 0	X X X	X XX
0 1 1	X X X	X XX
1 0 0	1 0 1	1 0 1
1 0 1	0 0 1	0 0 1
1 1 0	1 1 1	1 1 1
1 1 1	1 0 0	1 0 0

$$D_2 = f(Q_2, Q_1, Q_0) = \sum m(0, 4, 6, 7) + \sum d(2, 3)$$

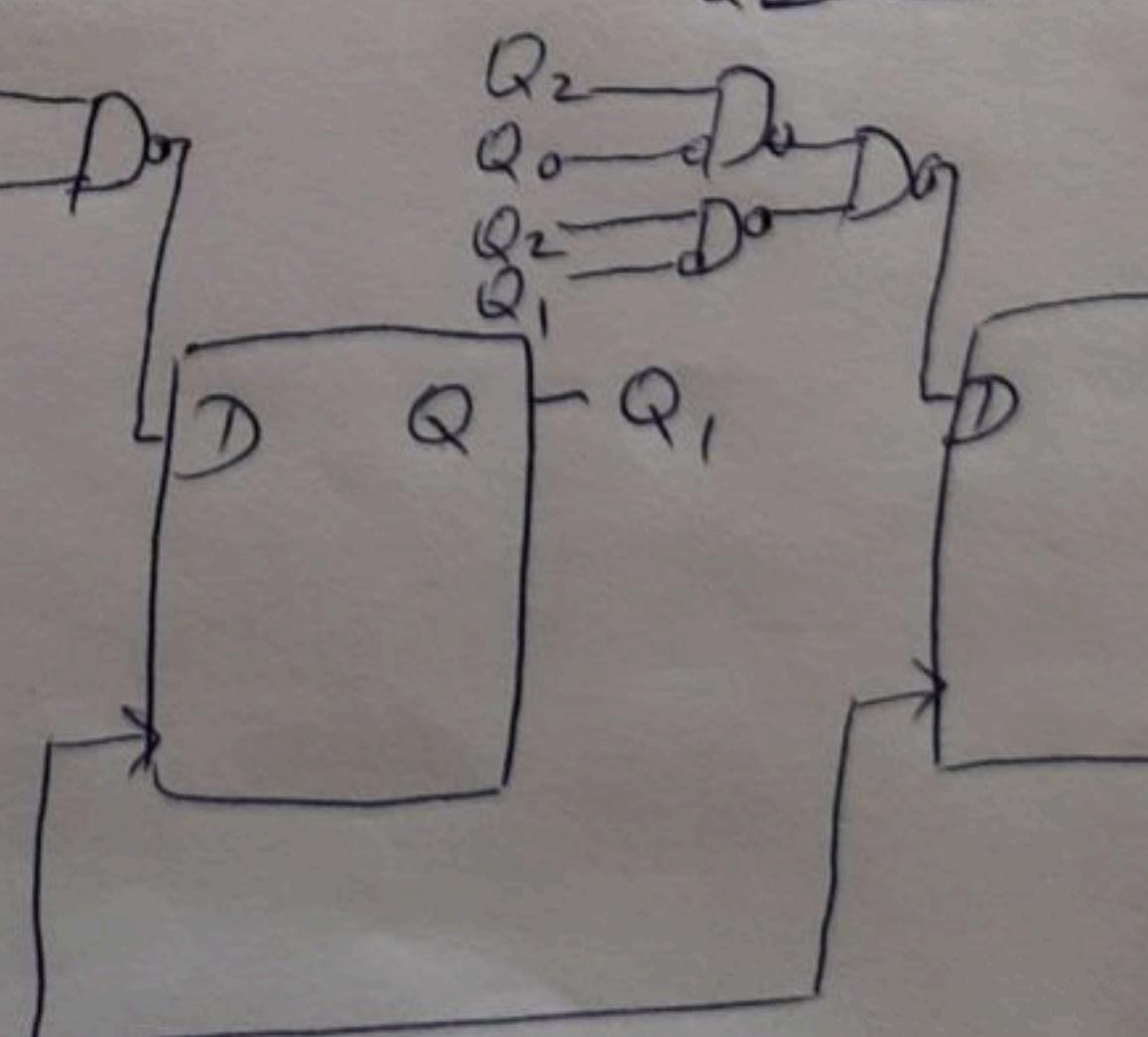
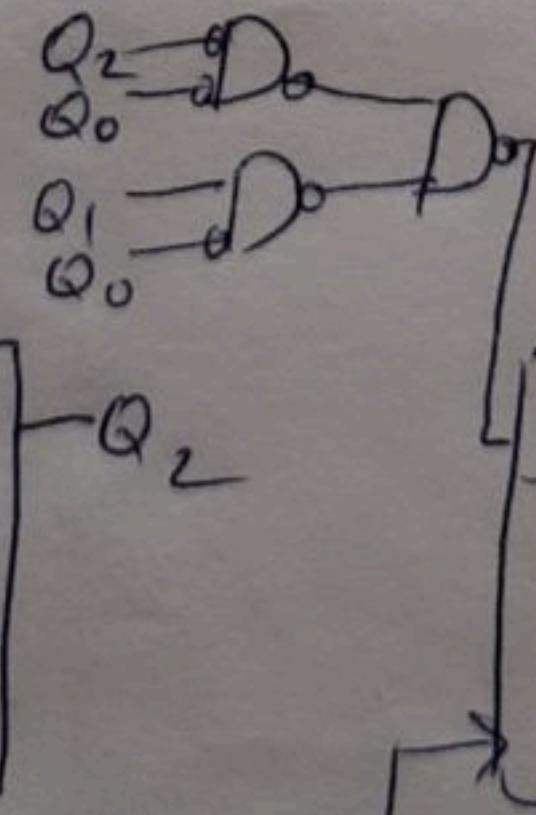
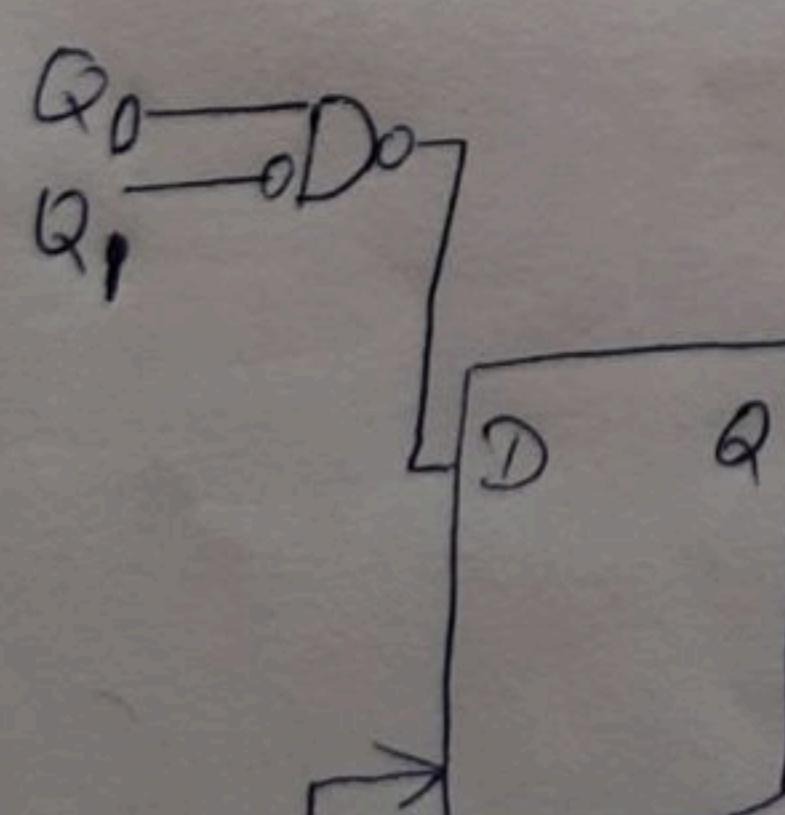
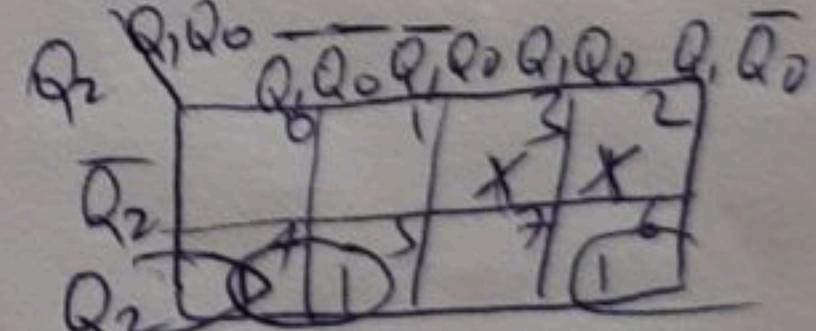
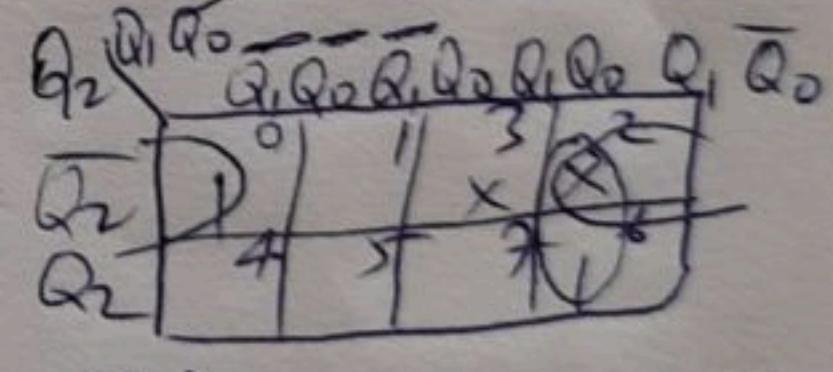
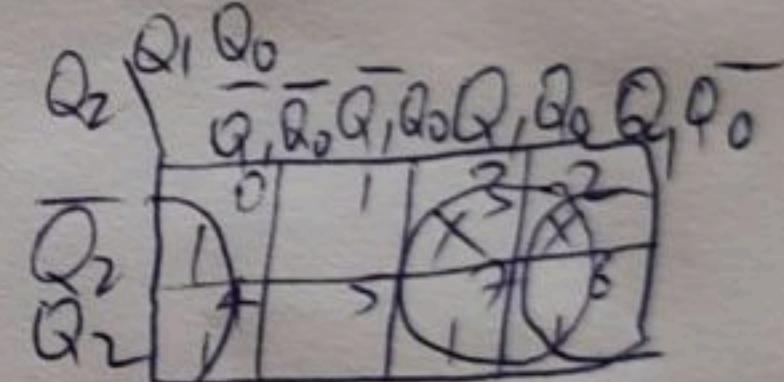
$$= \overline{Q_0} + Q_1$$

$$D_1 = f(Q_2, Q_1, Q_0) = \sum m(0, 6) + \sum d(2, 3)$$

$$= \overline{Q_2} \overline{Q_0} + Q_1 \overline{Q_0}$$

$$D_0 = f(Q_2, Q_1, Q_0) = \sum m(4, 5, 6) + \sum d(2, 3)$$

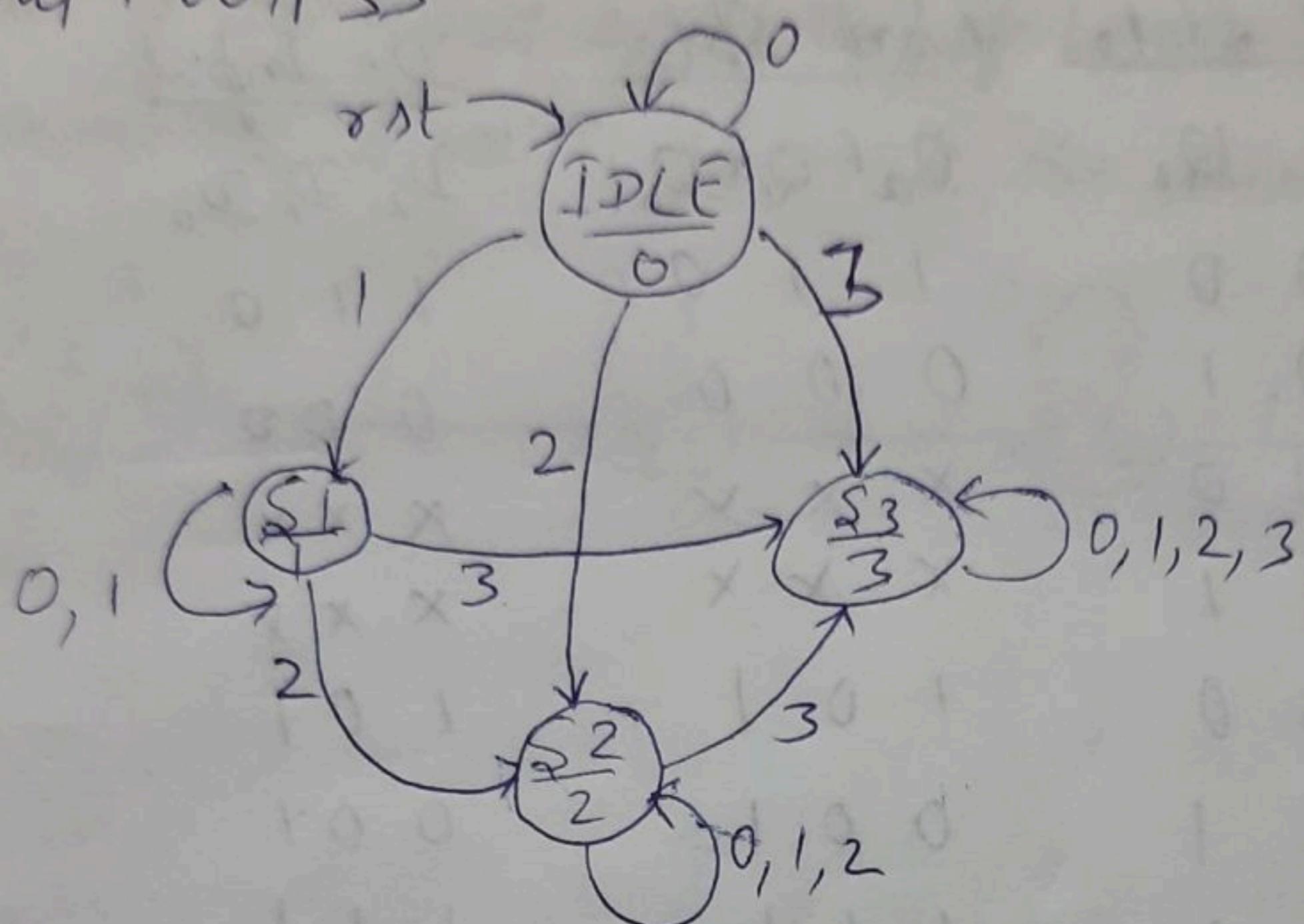
$$= Q_2 \overline{Q_0} + Q_2 \overline{Q_1}$$



Assignment-6 (Finite State Machines)

- Q1. Design a FSM over $\{0, 1, 2, 3\}$ that will output largest input digit read so far. Eg: Input: 001032 will produce output: 001133

Ans →

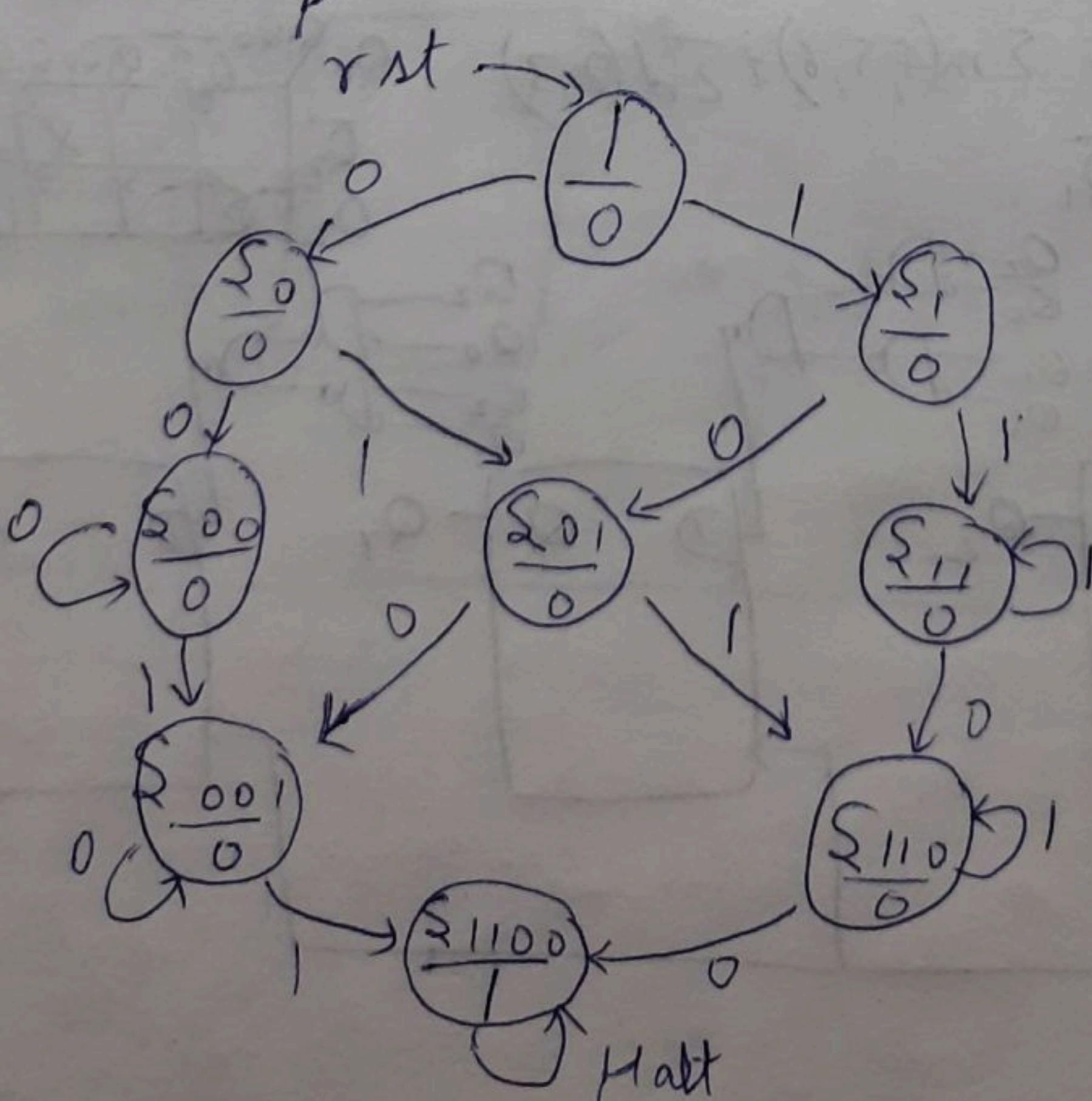


- Q2. Design an FSM that has 1 input & 1 output. The o/p becomes 1 & remains 1 when at least two 0's & two 1's have occurred as i/p's

Ans →

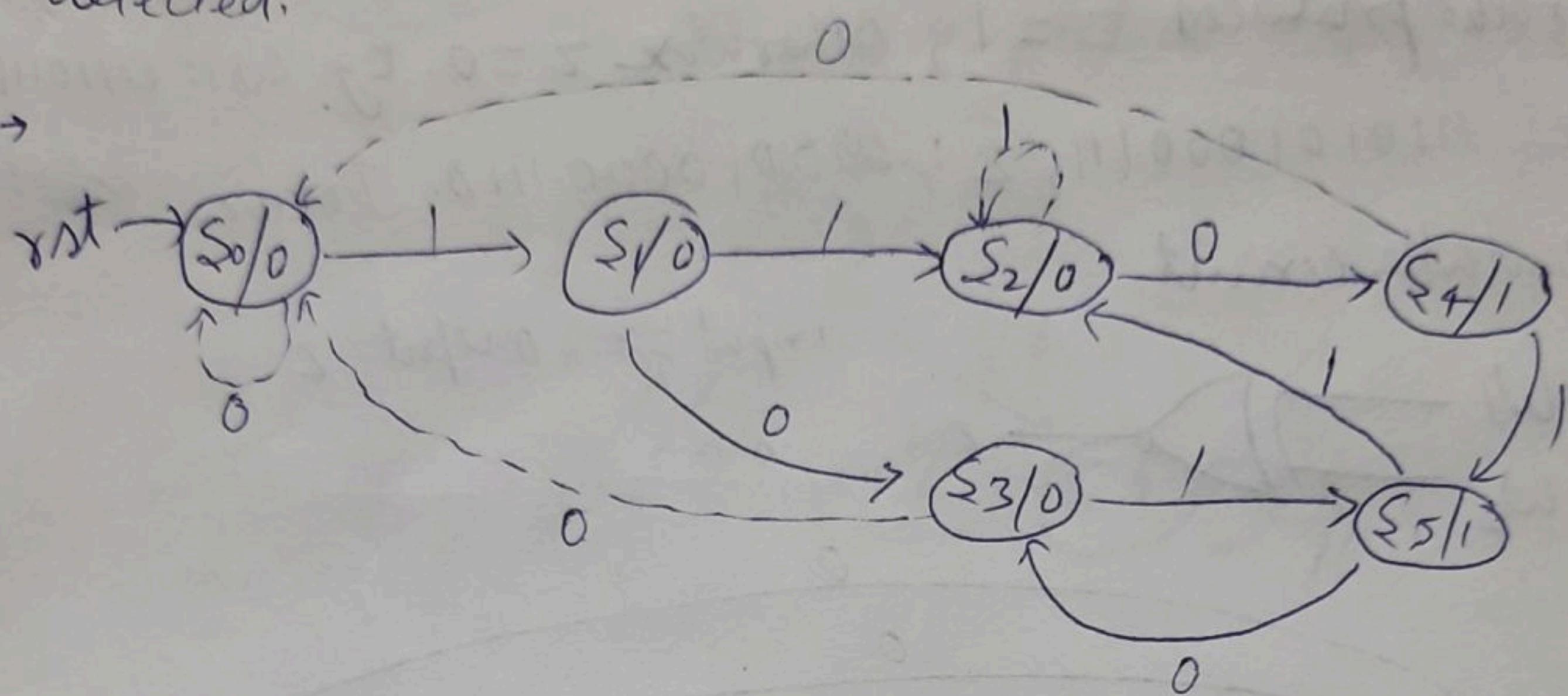
Input: 0 0 0 0 1 0 0 0 1 0 1 0 1 1

Output: 0 0 0 0 0 0 0 1 1 1 1 1



Q3. Derive a single I/P & single O/P Moore type FSM that produces an output of 1 if in the I/P sequence it detects either 110 or 101 patterns. Overlapping sequence should be detected.

Ans →



Q4. Derive a minimal State table for an FSM that acts a 3 bit parity generator. For every 3 bits observed on input 'w' during 3 consecutive cycles, the FSM generates the parity $p=1$ if & only if the No. of 1s is odd.

Ans →

000

001

010 ✓

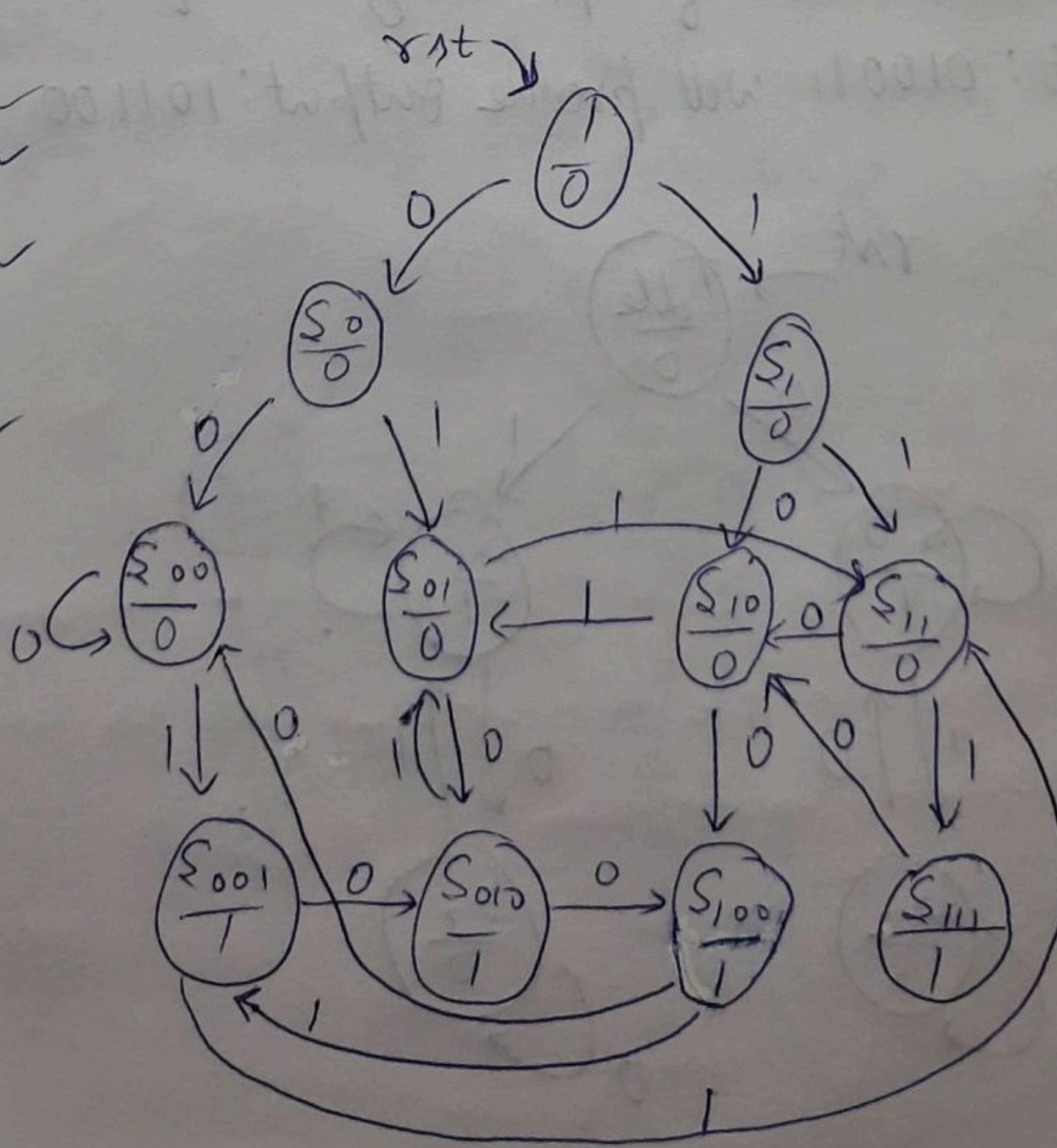
011

100 ✓

101

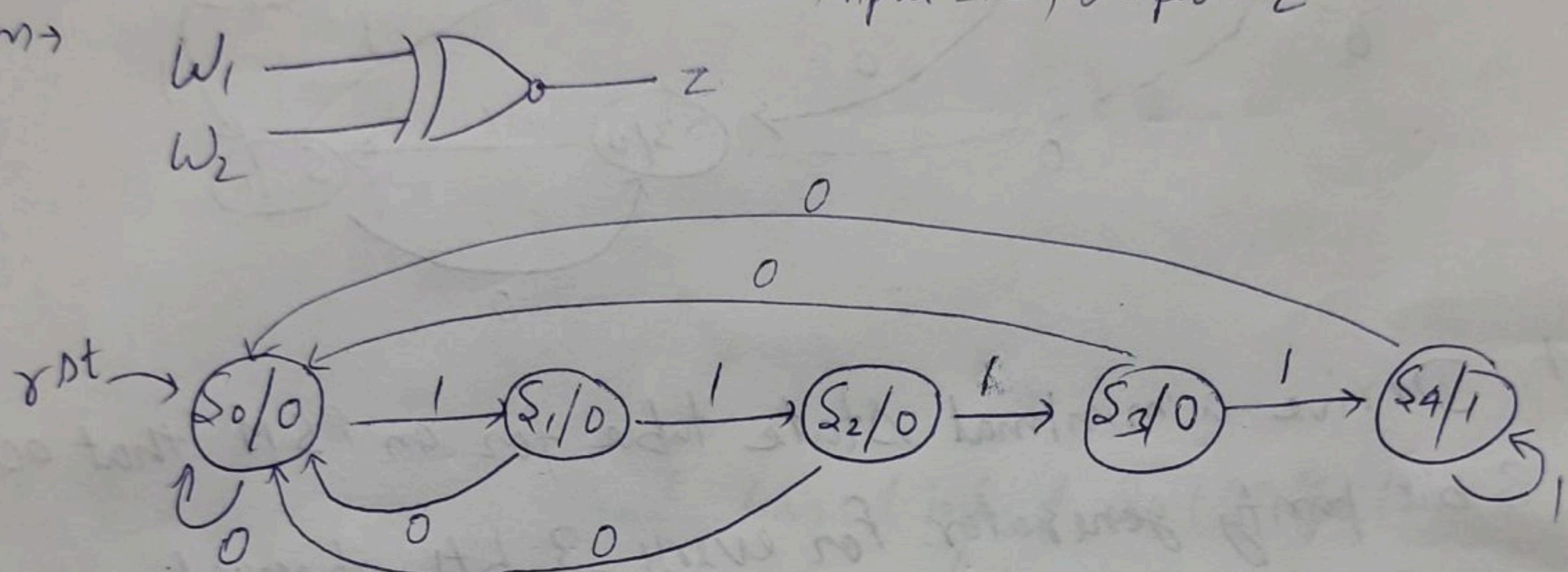
110

111 ✓



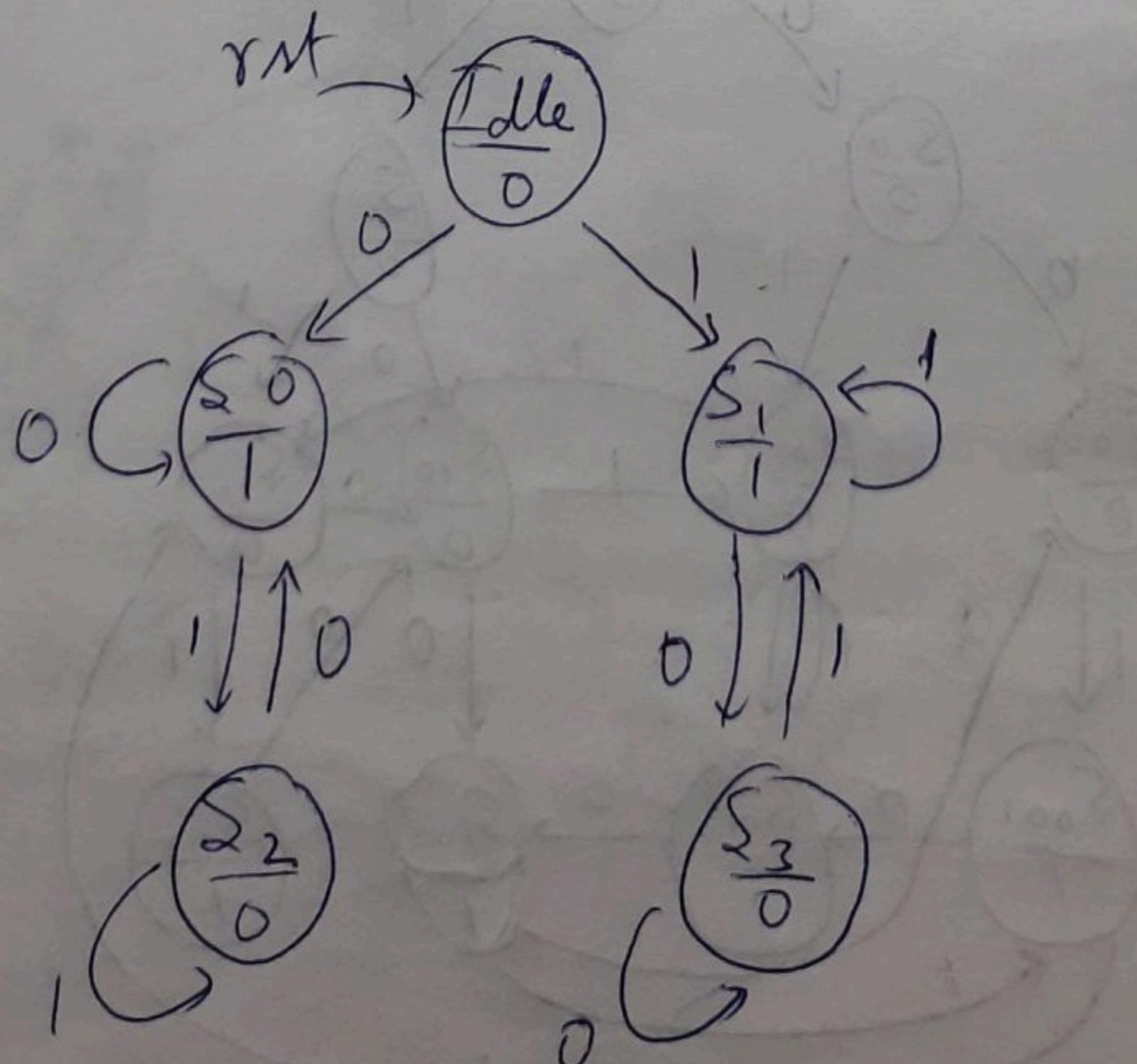
Q5. A sequential circuit has 2 I/Ps w_1 & w_2 & O/P z . Its function is to compare I/P sequences on 2 I/Ps. If $w_1 = w_2$ during any 4 consecutive clock cycles, the circuit produces $z = 1$; otherwise $z = 0$. Eg $w_1: 0110111000110$ $w_2: 1110101000111$, $z: 0000100001110$. Derive a suitable circuit.

Ans →



Q6. Design a FSM over $\{0, 1\}$ that will output 1 if the first bit & current bit of I/P string are equal, 0 otherwise. Eg - input : 010011 will produce output : 101100

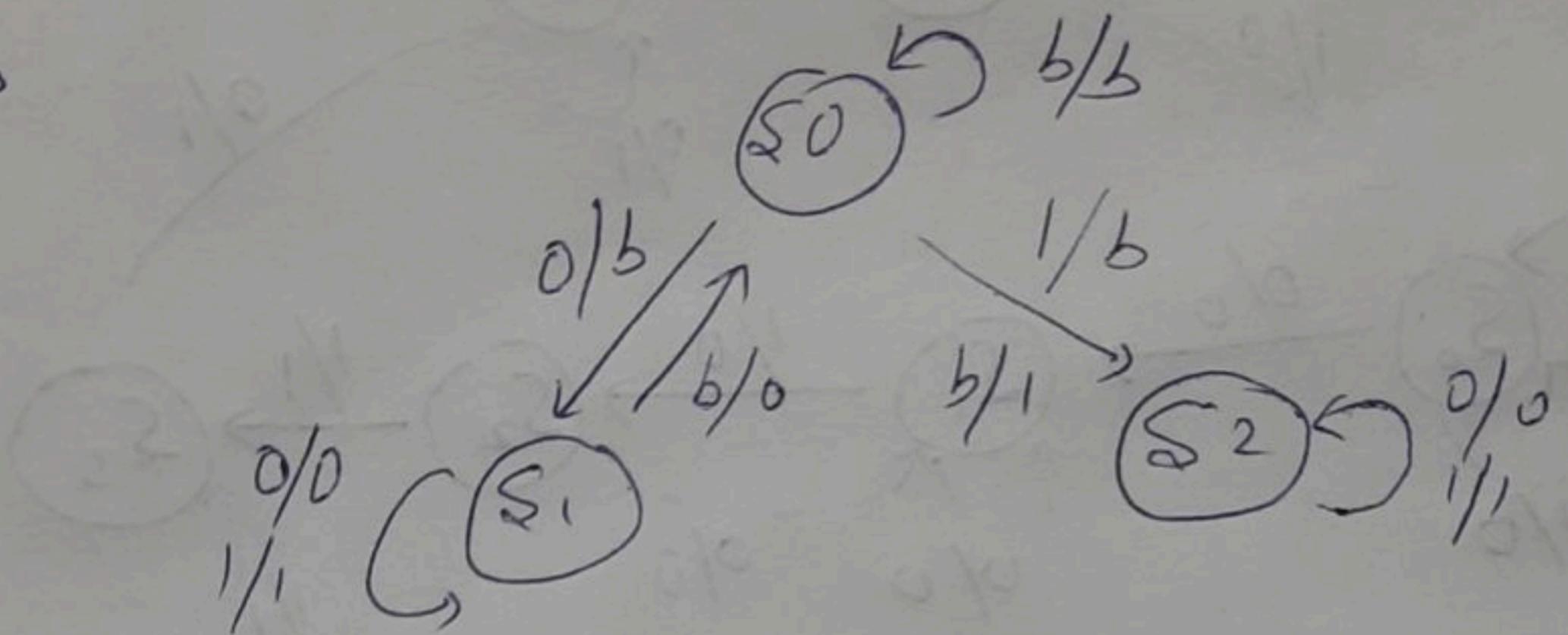
Ans →



Q7. Design a FSM over $\{0, 1, b\}$ that will output a copy of the input string except that first bit will have been moved to end of the string. ("b" represents a blank here)

Eg. input: 1010011 will produce output: 0100111

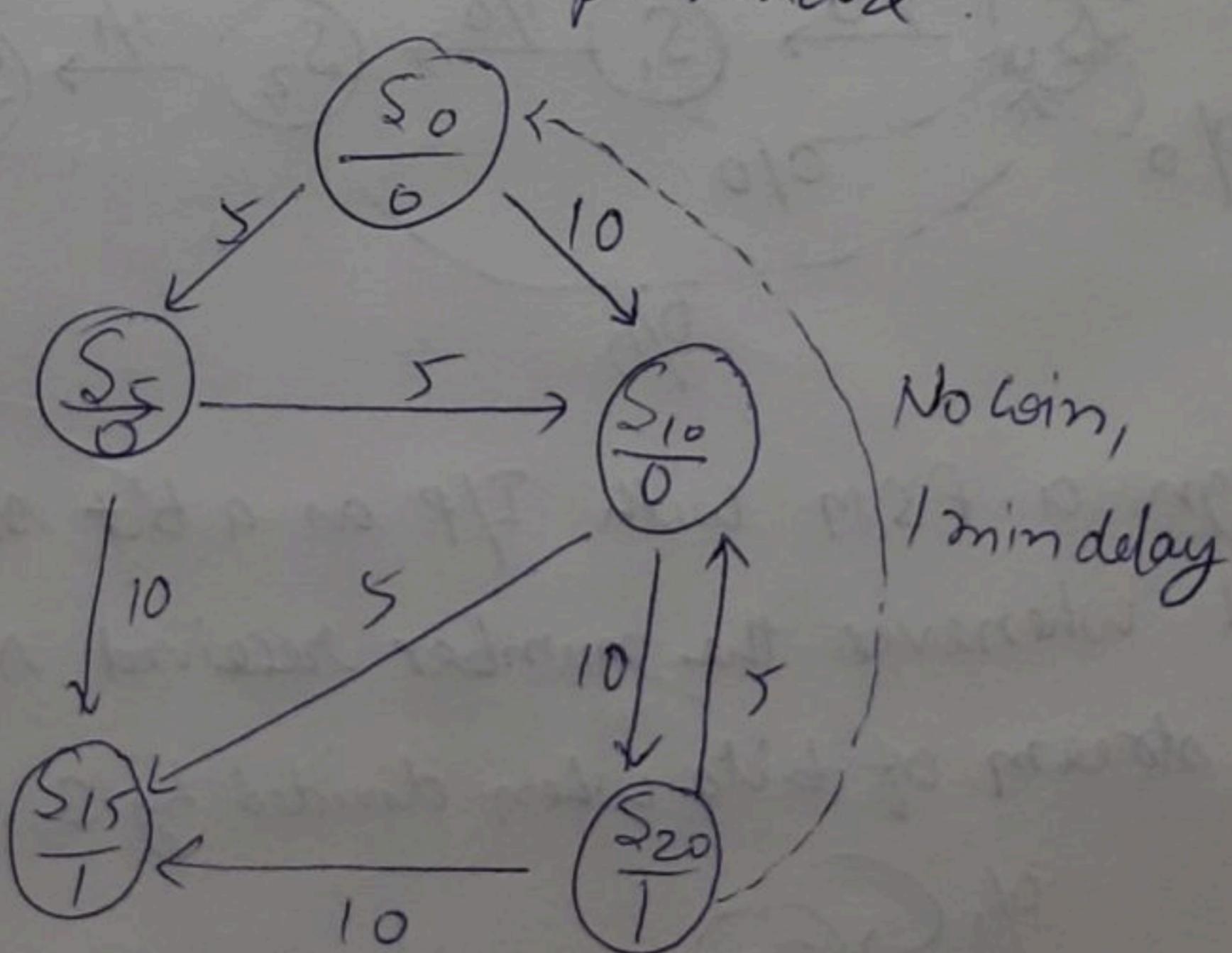
Ans →



Q8. Design a coin operated vending machine that dispenses candy under the following conditions:

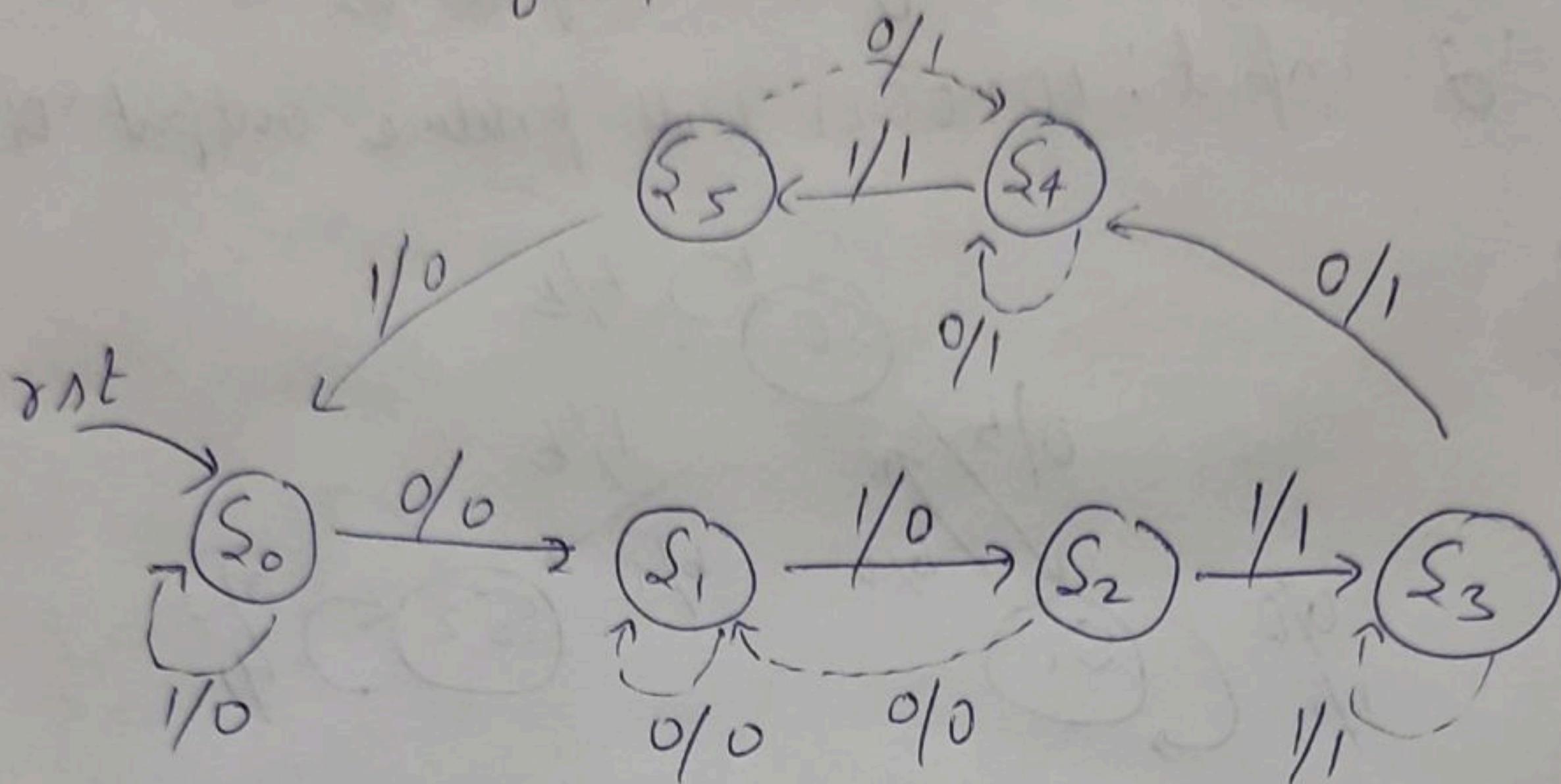
- The machine accepts Rs 5 & Rs 10.
- It takes Rs 15 for a candy to be released from machine.
- If Rs 20 is deposited, the machine will not return the change but it will credit the buyer with Rs 5 & wait for 1 min. for buyer to make a 2nd purchase.

Ans →



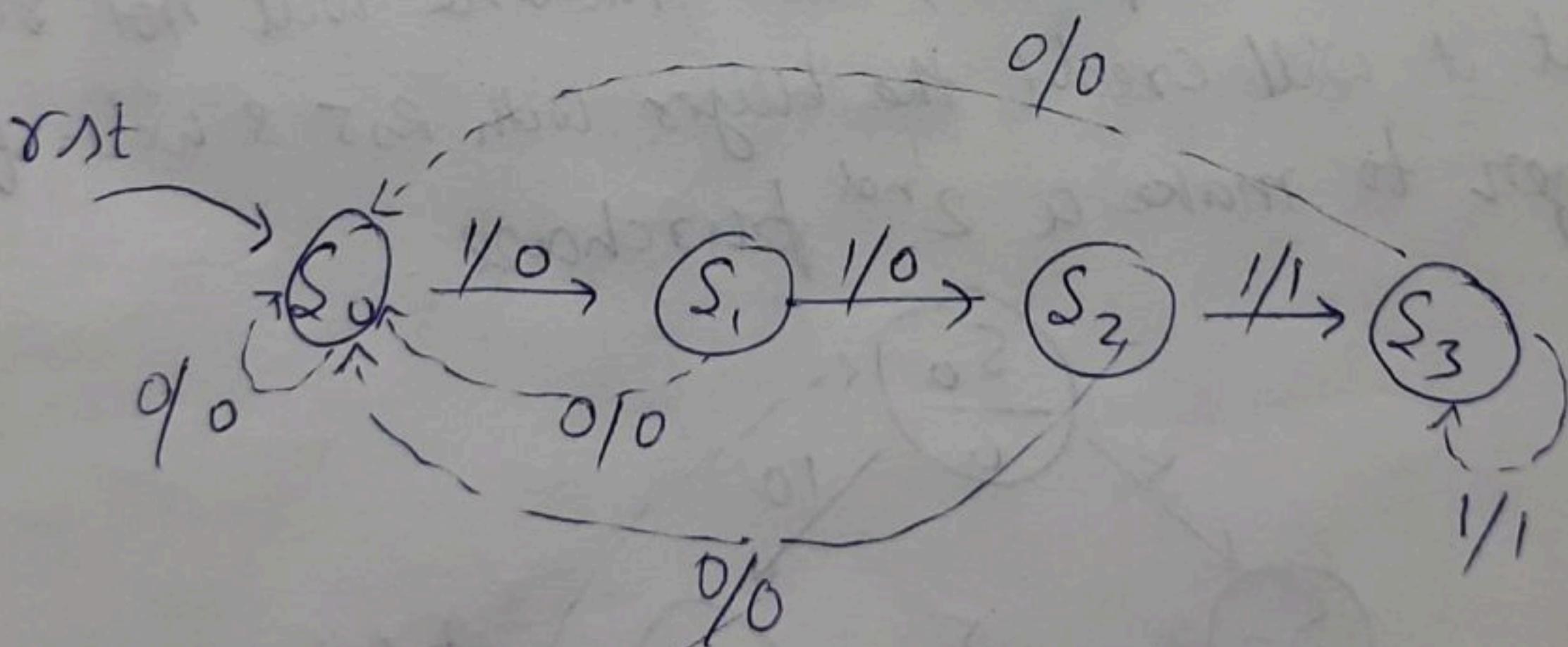
Q9. Draw state diagram for a FSM, the O/P toggles whenever it detects '110' LSB first (overlapping). Consider initial value of O/P as 0.

Ans →



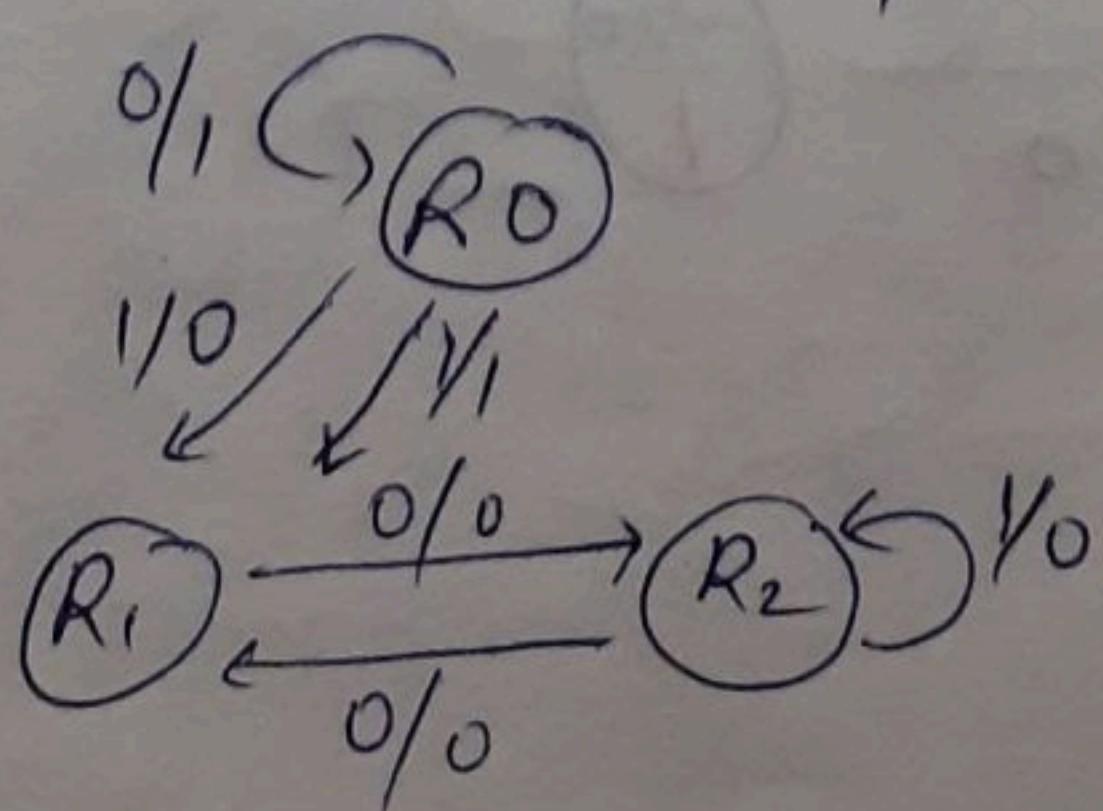
Q10. Describe a finite state machine using state diagram that will detect 3 consecutive coin tosses (of one coin) that results in heads.

Ans → Sequence detector : 111



Q11. Design a FSM with I/P as a bit stream, 2 o/p which goes 1 whenever the number received so far is divisible by 3.

Ans → Any stream of bits when divided by 3,



Q12. A sequential circuit has 2 I/Ps & 2 O/Ps. The inputs (X_1, X_2) represents a 2 bit binary number, N. If the present value of N is greater than previous value, then $Z_1=1$. If present value of N is less than previous value, then $Z_2=1$. Otherwise Z_1, Z_2 are 0. Draw FSM for the same.

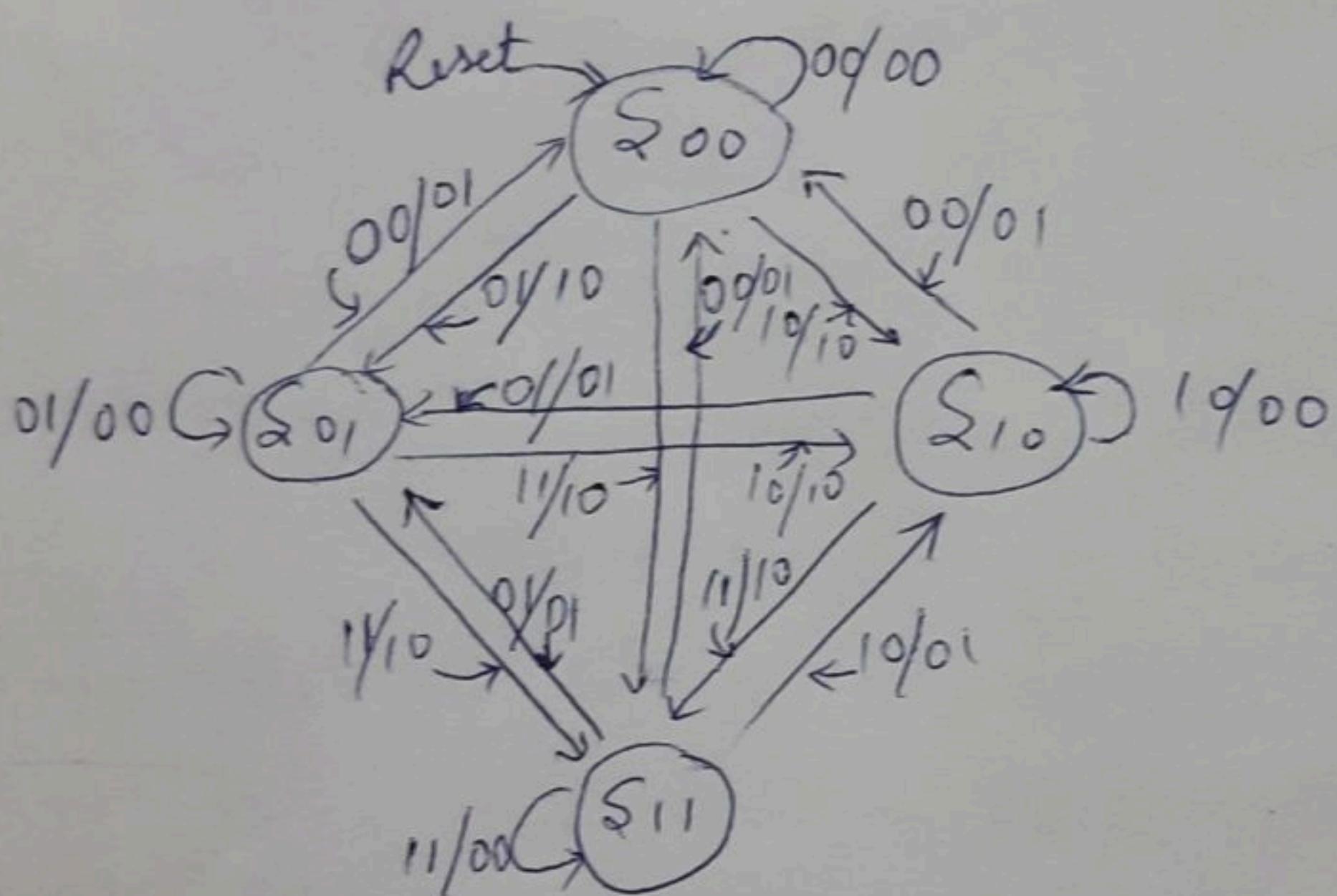
Ans →

$$X_1: 0 \ 0 \ 1 \ 1 \ 0 \ 0$$

$$X_2: 0 \ 1 \ 0 \ 0 \ 1 \ 0$$

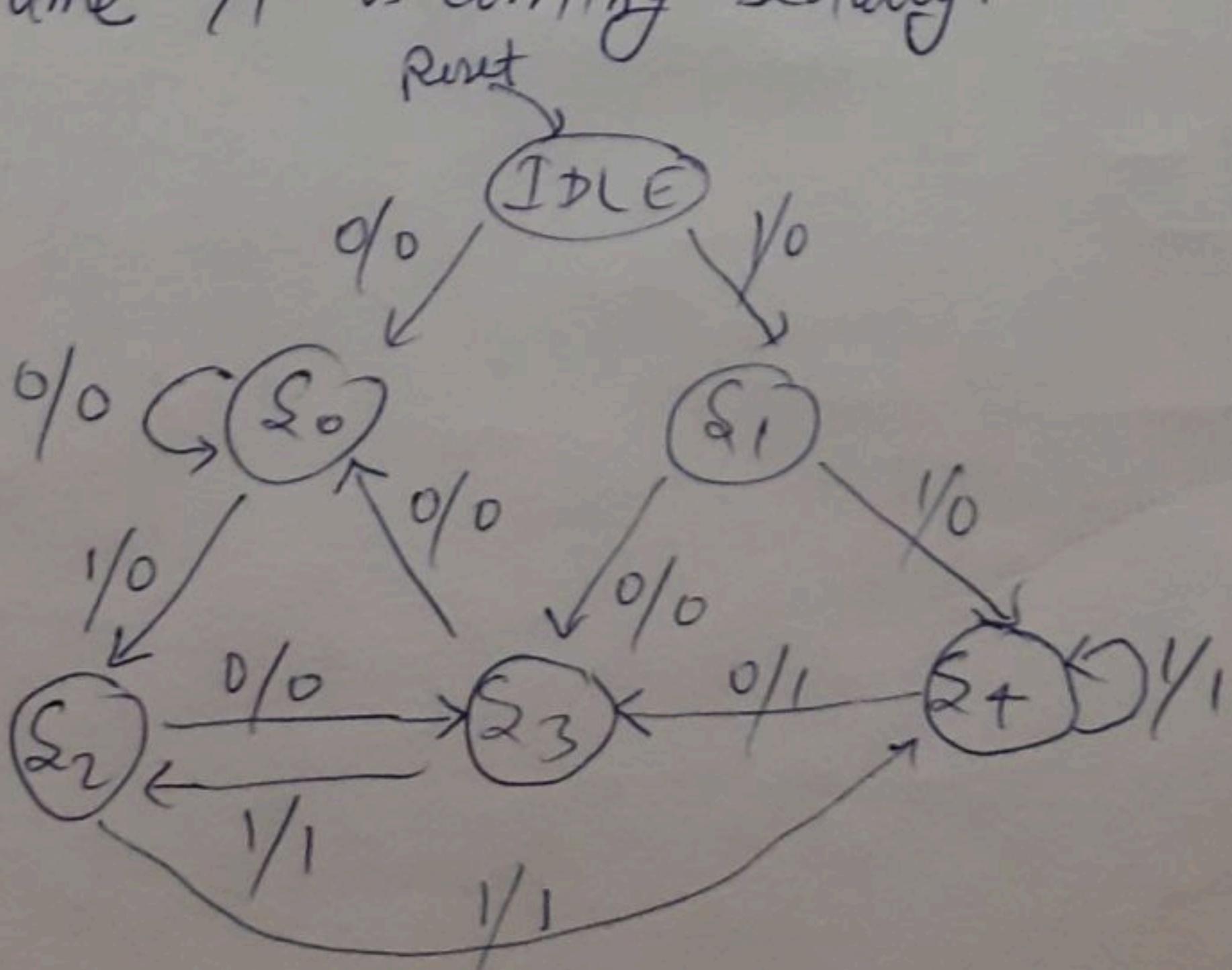
$$Z_1: 0 \ 1 \ 1 \ 0 \ 0 \ 0$$

$$Z_2: 0 \ 0 \ 0 \ 0 \ 1 \ 1$$



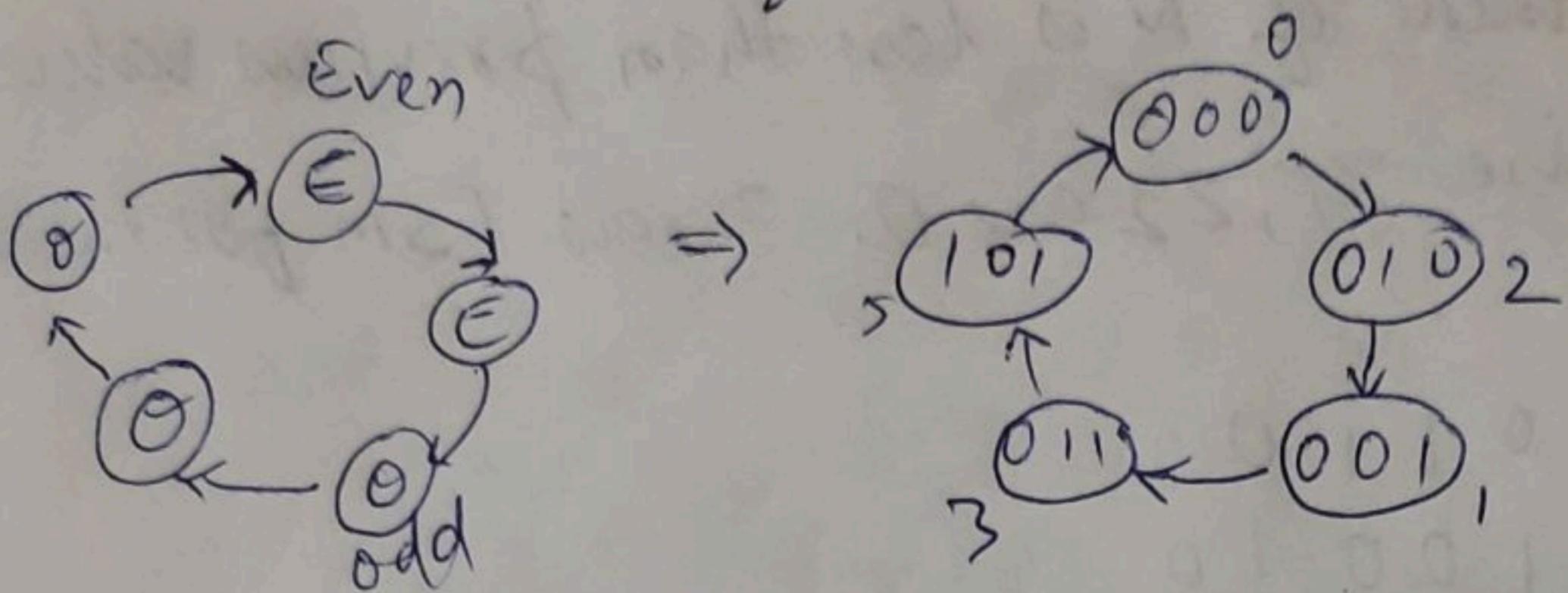
Q13. Design FSM for a system which gives o/p high when bit-1 is in majority in 3 bit number (overlapping is allowed). Assume I/P is coming serially.

Ans →



Q14 How to design a divide by 5 Counter with equal duty cycle?

Ans → 00111 seq. detector = $\div 5$ counter



Transition Table

Present State $Q_2\ Q_1\ Q_0$	$Q_2 + Q_1 + Q_0$	Next State $Q_2 + Q_1 + Q_0$	D-Input		
			$D_2\ D_1\ D_0$	$D_2\ D_1\ D_0$	$D_2\ D_1\ D_0$
0 0 0	0	0 1 0	0 1 0	0 1 0	0 1 0
0 0 1	1	0 1 1	0 1 1	0 1 1	0 1 1
0 1 0	2	0 0 1	0 0 1	0 0 1	0 0 1
0 1 1	3	1 0 1	1 0 1	1 0 1	1 0 1
1 0 0	4	x x x	x x x	x x x	x x x
1 0 1	5	0 0 0	0 0 0	0 0 0	0 0 0
1 1 0	6	x x x	x x x	x x x	x x x
1 1 1	7	x x x	x x x	x x x	x x x

$$\begin{aligned}D_0 &= \sum_m(1, 2, 3) + \sum_d(4, 5, 7) \\&= \overline{Q_2} Q_0 + Q_1\end{aligned}$$

$Q_2\ Q_1\ Q_0$	$\bar{Q}_2\bar{Q}_1\bar{Q}_0$	$\bar{Q}_1\bar{Q}_0$	$Q_1\bar{Q}_0$	$Q_2\bar{Q}_0$
\bar{Q}_2	0	1	3	2
Q_2	4	5	7	6

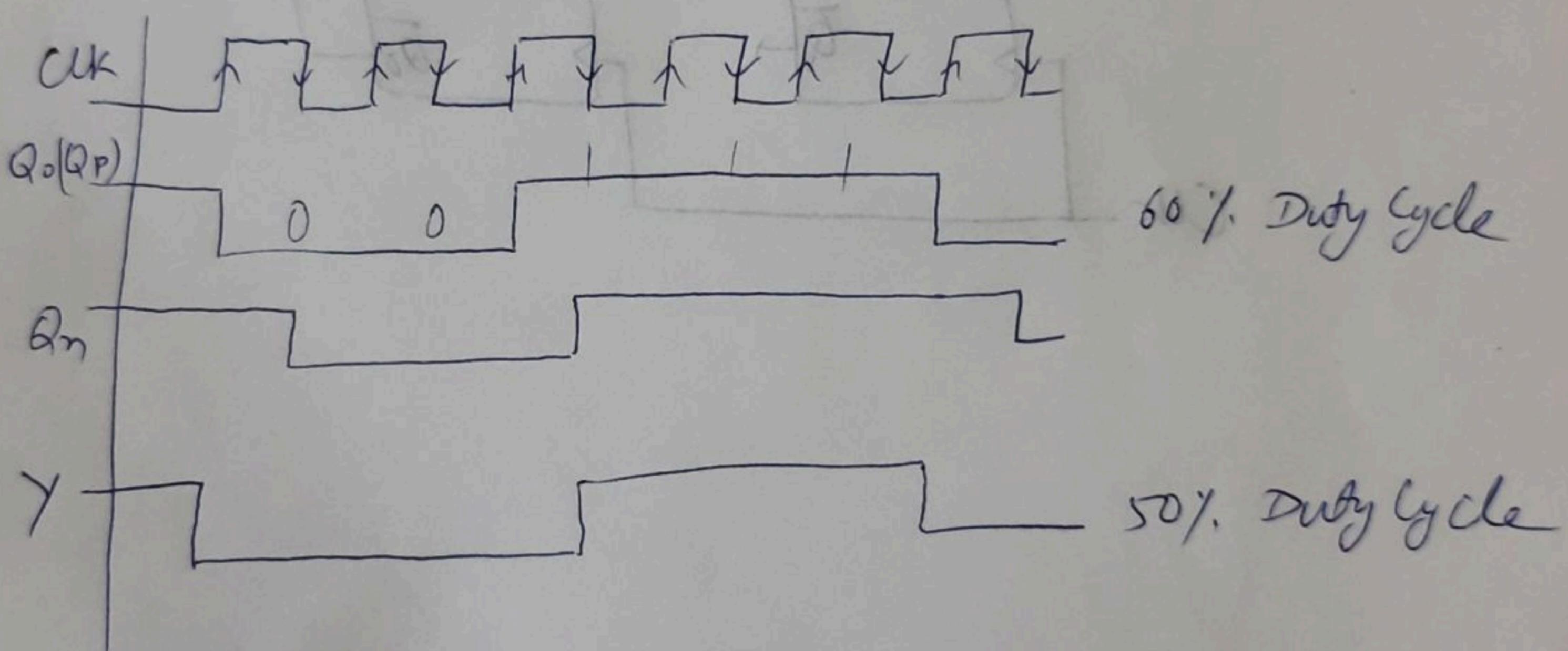
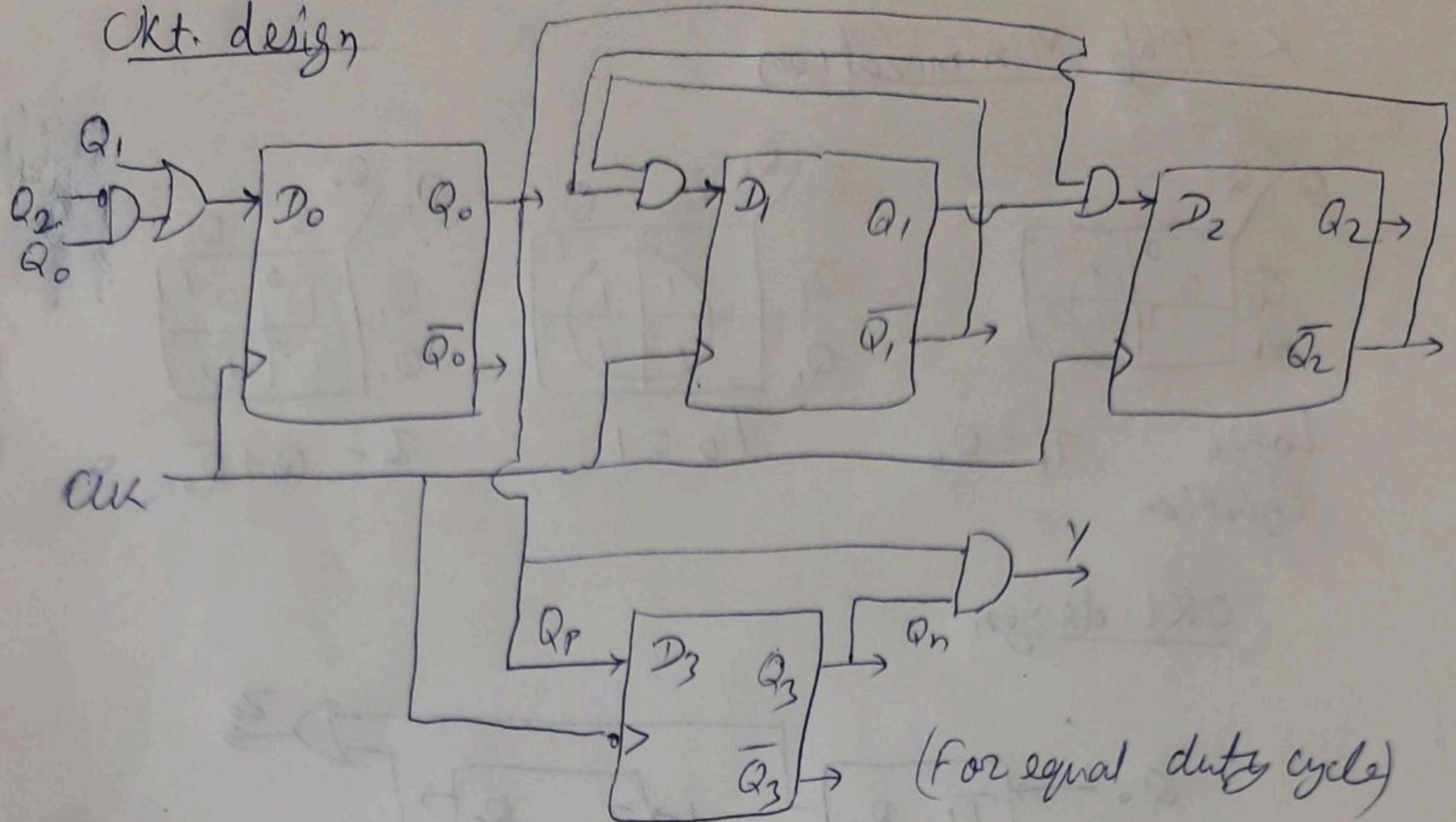
$$\begin{aligned}D_1 &= \sum_m(0, 1) + \sum_d(4, 6, 7) \\&= \overline{Q_2}\overline{Q_1}\end{aligned}$$

$Q_2\ Q_1\ Q_0$	$\bar{Q}_2\bar{Q}_1\bar{Q}_0$	$\bar{Q}_1\bar{Q}_0$	$Q_1\bar{Q}_0$	$Q_2\bar{Q}_0$
\bar{Q}_2	0	1	3	2
Q_2	4	5	7	6

$$\begin{aligned}D_2 &= \sum_m(3) + \sum_d(4, 6, 7) \\&= Q_1 Q_0\end{aligned}$$

$Q_2\ Q_1\ Q_0$	$\bar{Q}_2\bar{Q}_1\bar{Q}_0$	$\bar{Q}_1\bar{Q}_0$	$Q_1\bar{Q}_0$	$Q_2\bar{Q}_0$
\bar{Q}_2	0	1	3	2
Q_2	4	5	7	6

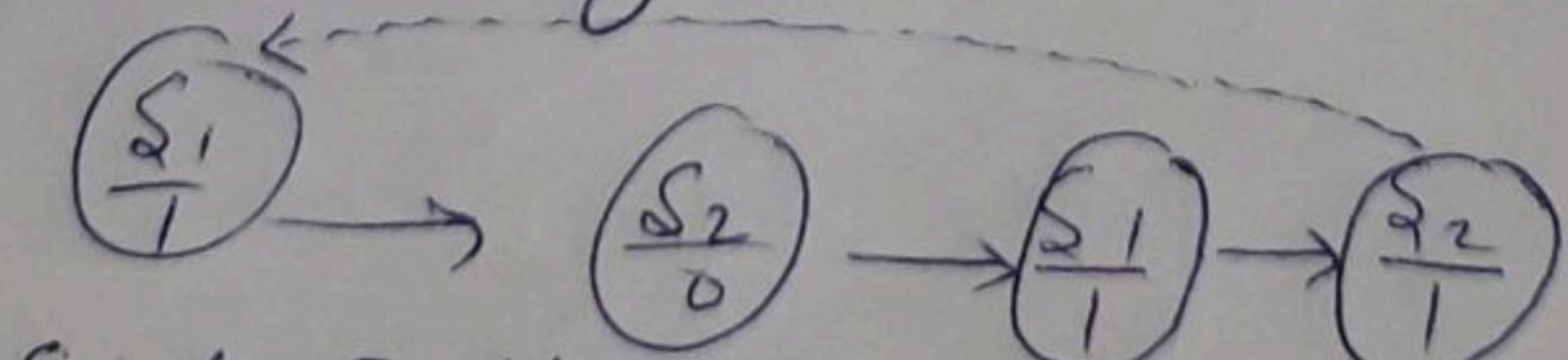
Ckt. design



Q15. Design a sequence generator which generates 1011 continuously. Use T flip-flops for this design.

Ans →

State Diagram

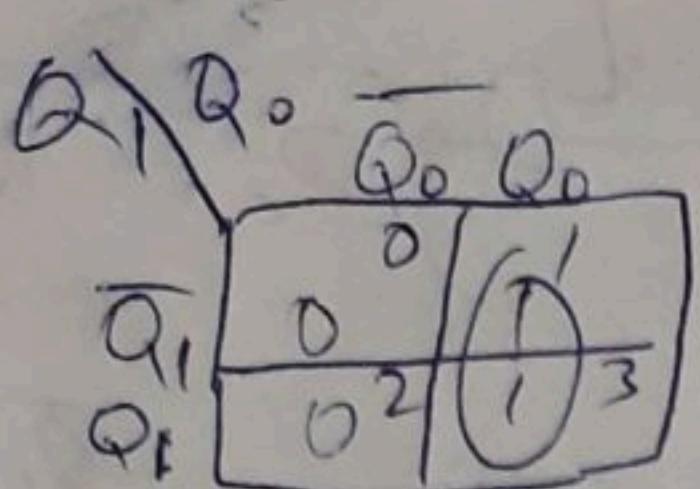


State Table

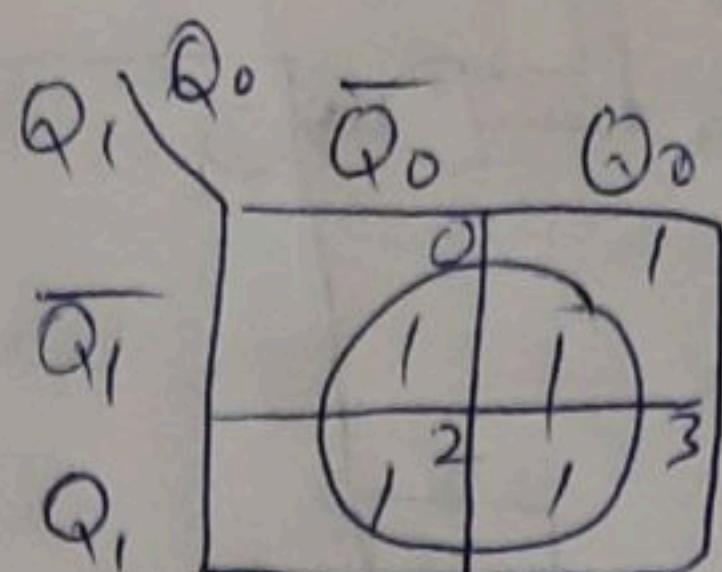
Present State	Next State	Data I/P	O/P
---------------	------------	----------	-----

	Q ₁ , Q ₀	Q ₁ +Q ₀ t	T ₁ , T ₀	Z
S ₁	0 0	0 1	0 1	1
S ₂	0 1	1 0	1 1	0
S ₃	1 0	1 1	0 1	1
S ₄	1 1	0 0	1 1	1

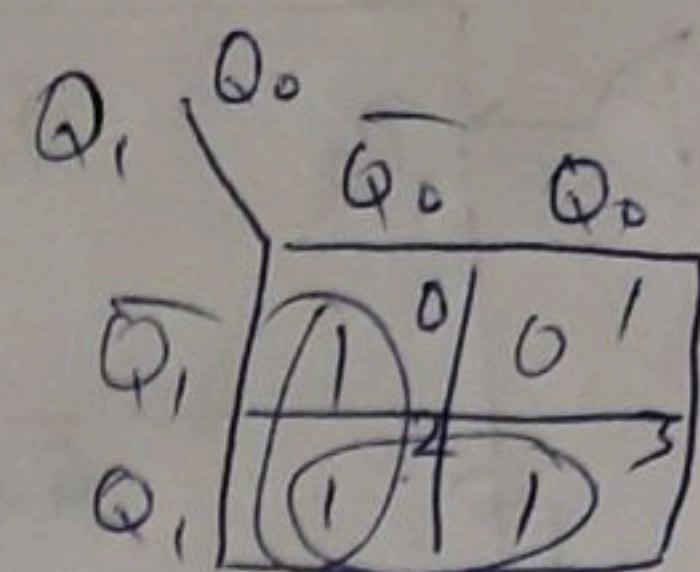
K-Map Minimization



Logic Equation $T_1 = Q_0$

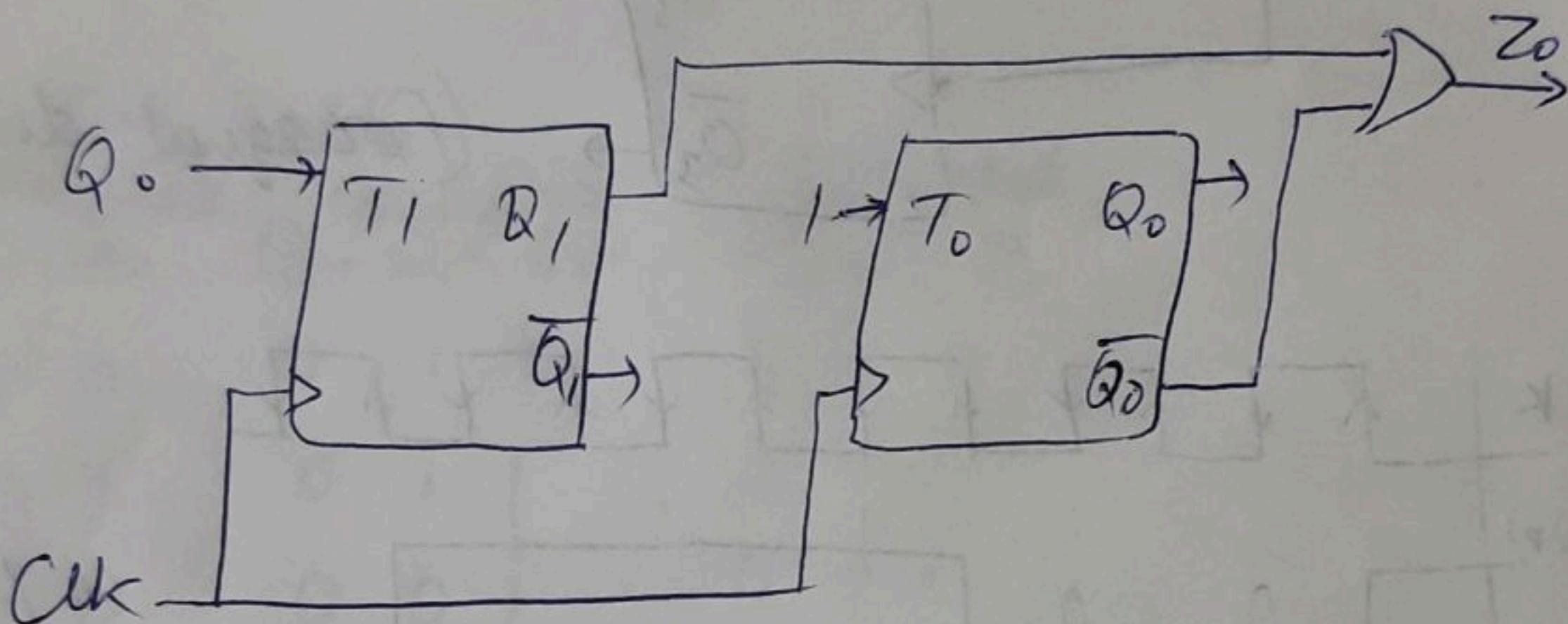


$T_0 = 1$



$Z = Q_1 + \bar{Q}_0$

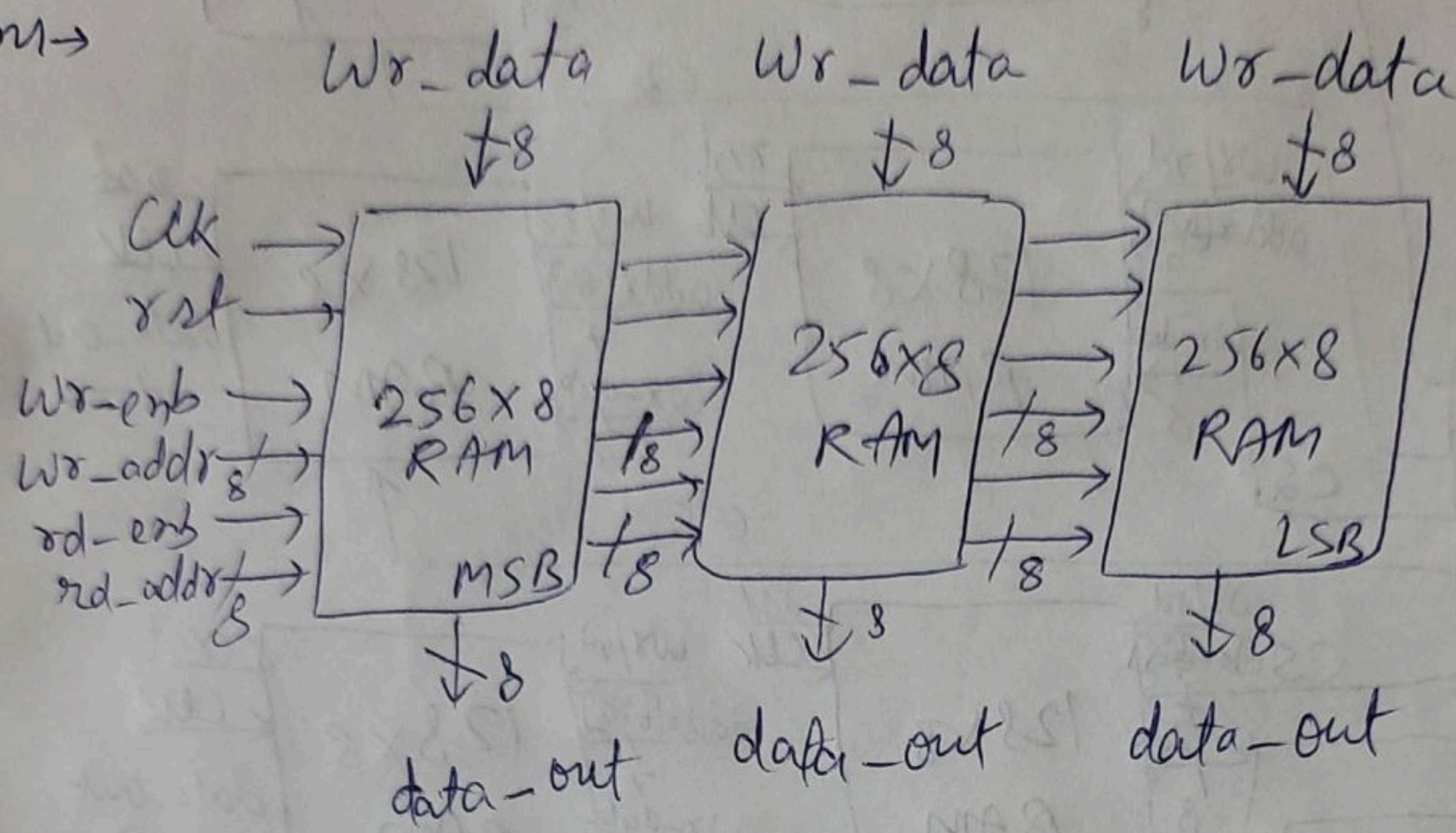
CKT. design



Assignment-7 (Memories, FIFO, Glitches & PLD)

Q1. Make a 256×24 ROM from 256×8 ROM chips.

Ans →



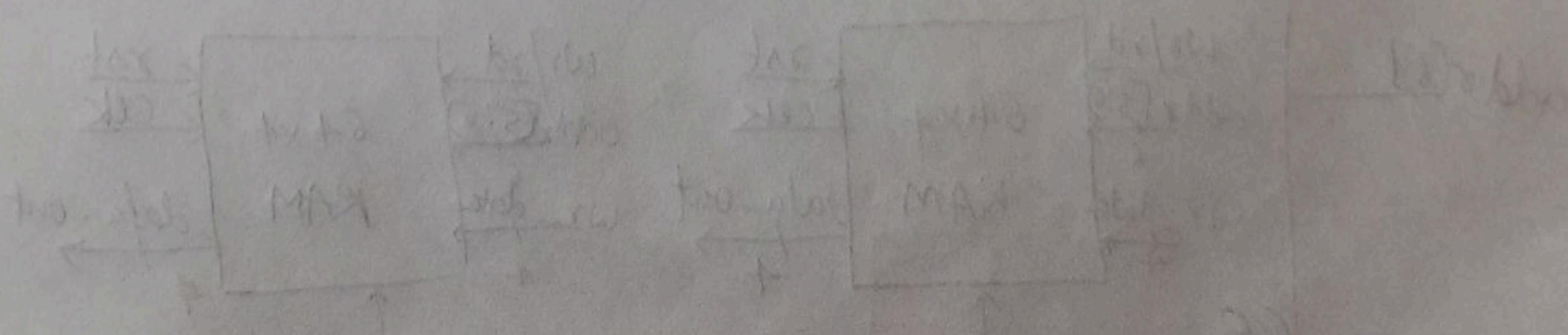
Q2. Make a $1K \times 8$ RAM using 128×8 RAM chips.

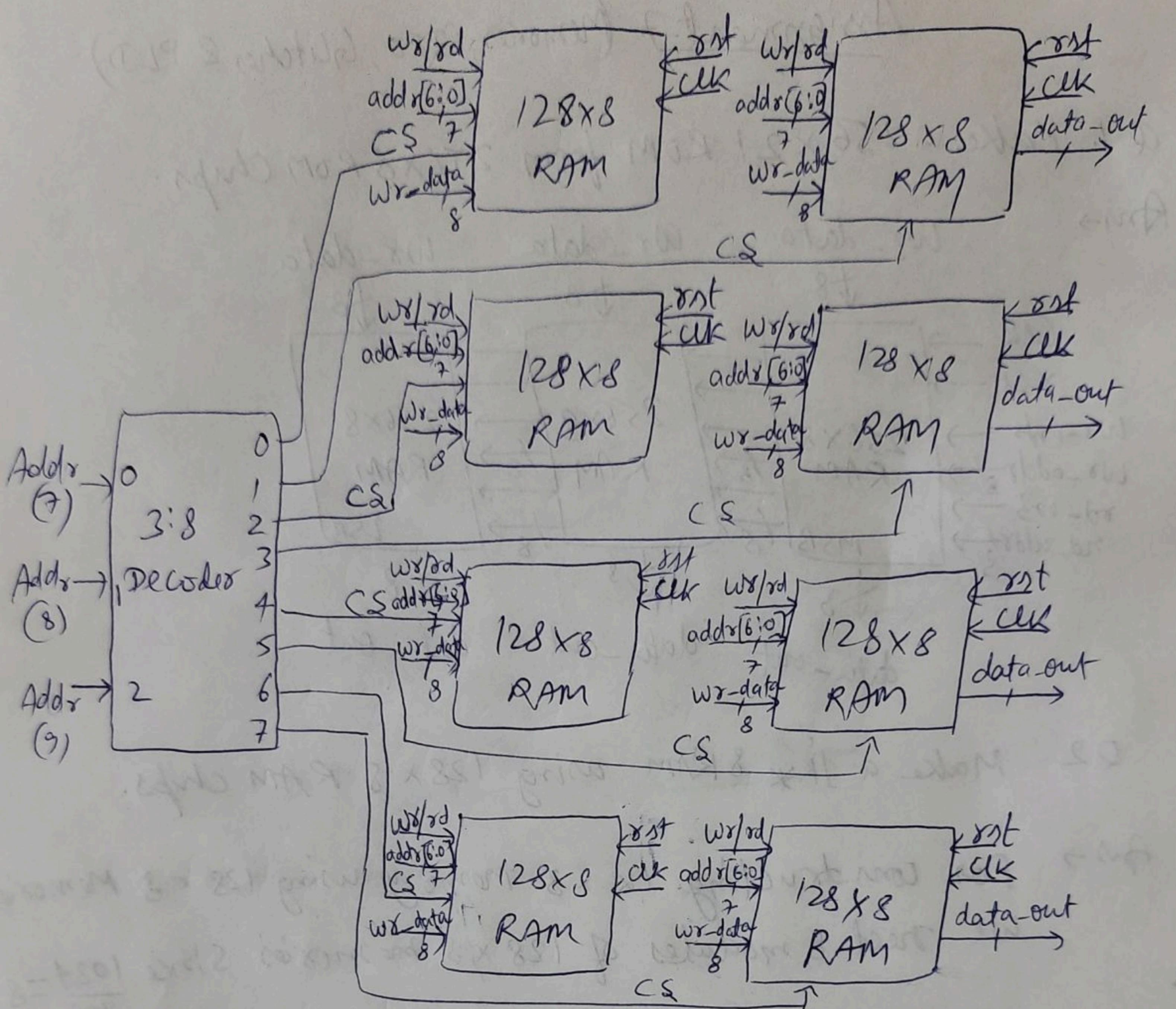
Ans →

For constructing $1K \times 8$ memory using 128×8 memories, we need 8 modules of 128×8 memories since $\frac{1024}{128} = 8$

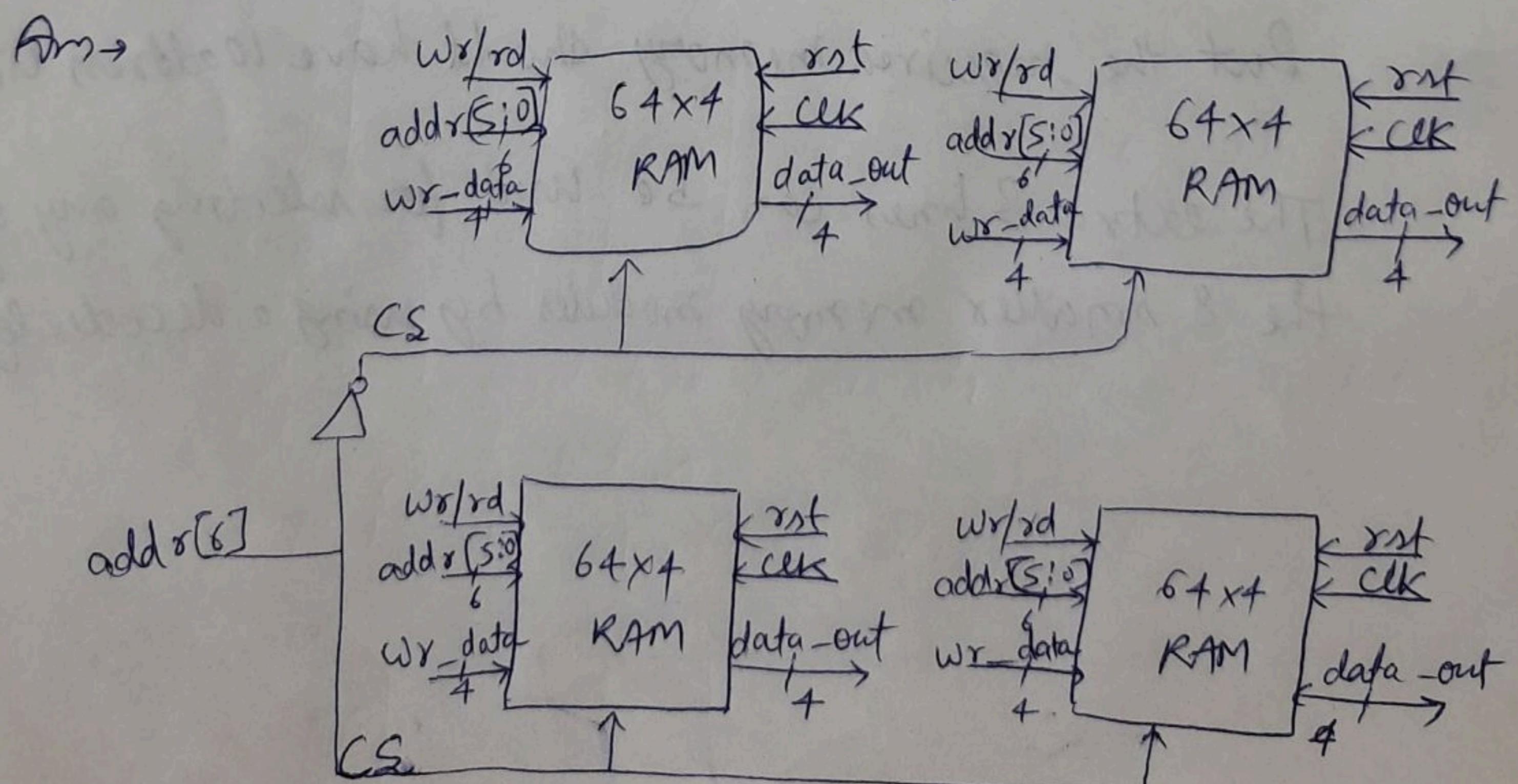
The available 128×8 memory will have 7 address lines.

But the required memory should have 10 address lines.
The extra 3 lines can be used for selecting any of the 8 smaller memory modules by using a decoder logic.





Q3. Make a 128×8 RAM chip using 64×4 RAM chips.



Q4. Determine the depth of FIFO required for following specifications.

- Writing frequency is 100 MHz.
- Reading frequency is 80 MHz.
- Writing Rate is 80 data/100 clock cycles (20 random idle cycles)
- Reading side is 60 data/100 clock cycles (40 random idle cycles)
- Burst Length = 80

Ans → FIFO depth must be calculated for worst case
i.e., Maximum write frequency & minⁿ read frequency

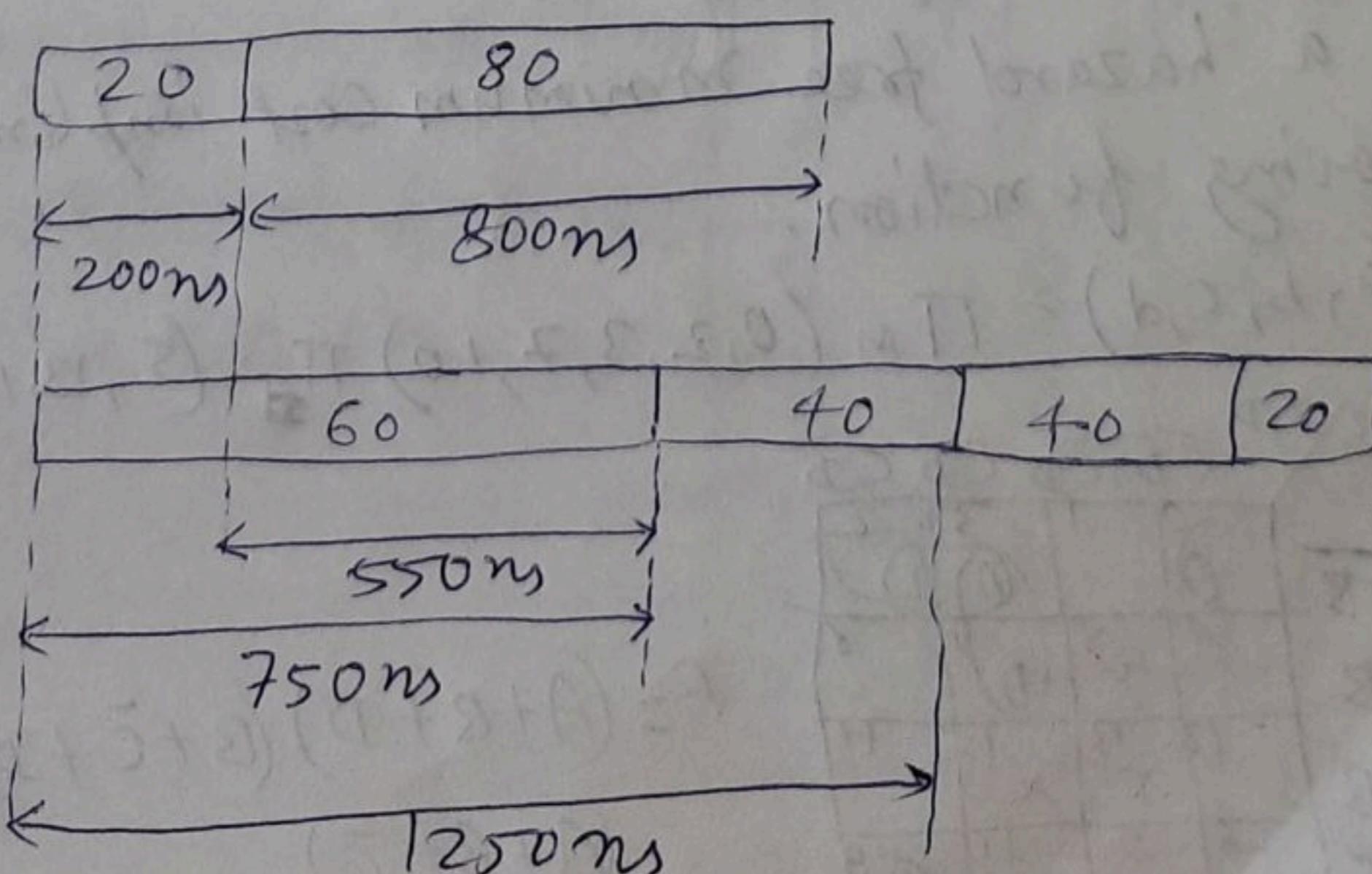
$$\begin{aligned} \text{Time taken to write } 80(D) \text{ items to FIFO} &= D/F_{\text{write}} \\ &= 80/100M \\ &= 800 \text{ ns} \end{aligned}$$

$$\begin{aligned} \text{Time taken to read 1 data} &= 1/80 M \\ &= 12.5 \text{ ns} \end{aligned}$$

$$\text{Time taken to read 60 data} = 60 \times 12.5 \text{ ns} = 750 \text{ ns}$$

$$\text{No. of data's read in } 550 \text{ ns} = 550/12.5 = 44$$

$$\text{Excess Data is FIFO depth (Backlog)} = 80 - 44 \\ = 36$$



Q5. If 8 chips are used to design a memory of 2MB,
What is size of individual chip?

Ans → 8 chips → 2 MB memory

$$1 \text{ chip} \rightarrow \frac{2 \text{ MB}}{8} = \frac{2 \times 1024 \text{ KB}}{8} = 256 \text{ KB}$$

* How many 256×8 chips are required to implement a memory of 1 KB?

Ans → 256×8 chip can be used to store 256 bytes of memory

$$1 \text{ KB of memory} = 1024 \text{ Bytes}$$

$$\text{No. of chips} = \frac{1024}{256} = 4$$

Q6. Find a hazard free minimum cost implementation of following function.

$$F(a, b, c, d) = \sum_m(0, 4, 11, 13, 15) + \sum_d(2, 3, 5, 10)$$

Ans → AB

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	0	1	$\times 3$	$\times 2$
$\bar{A}B$	4	$\times 5$	7	6
$A\bar{B}$	12	13	15	14
AB	8	9	11	$\times 10$

$$F = \bar{A}\bar{C}\bar{D} + ABD + ACD$$

Q7. Find a hazard free minimum cost implementation of following function.

$$F(a, b, c, d) = \prod_M(0, 2, 3, 7, 10) + \prod_D(5, 13, 15)$$

Ans → AB

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$	0	1	3	2
$\bar{A}B$	4	$\times 5$	0	6
$A\bar{B}$	12	13	15	14
AB	8	9	11	$\times 10$

$$F = (A+B+D)(B+\bar{C}+D)(A+\bar{C}+\bar{D})(A+B+\bar{C})$$

Q8. Implement a full adder using PAL, PLA & PROM.

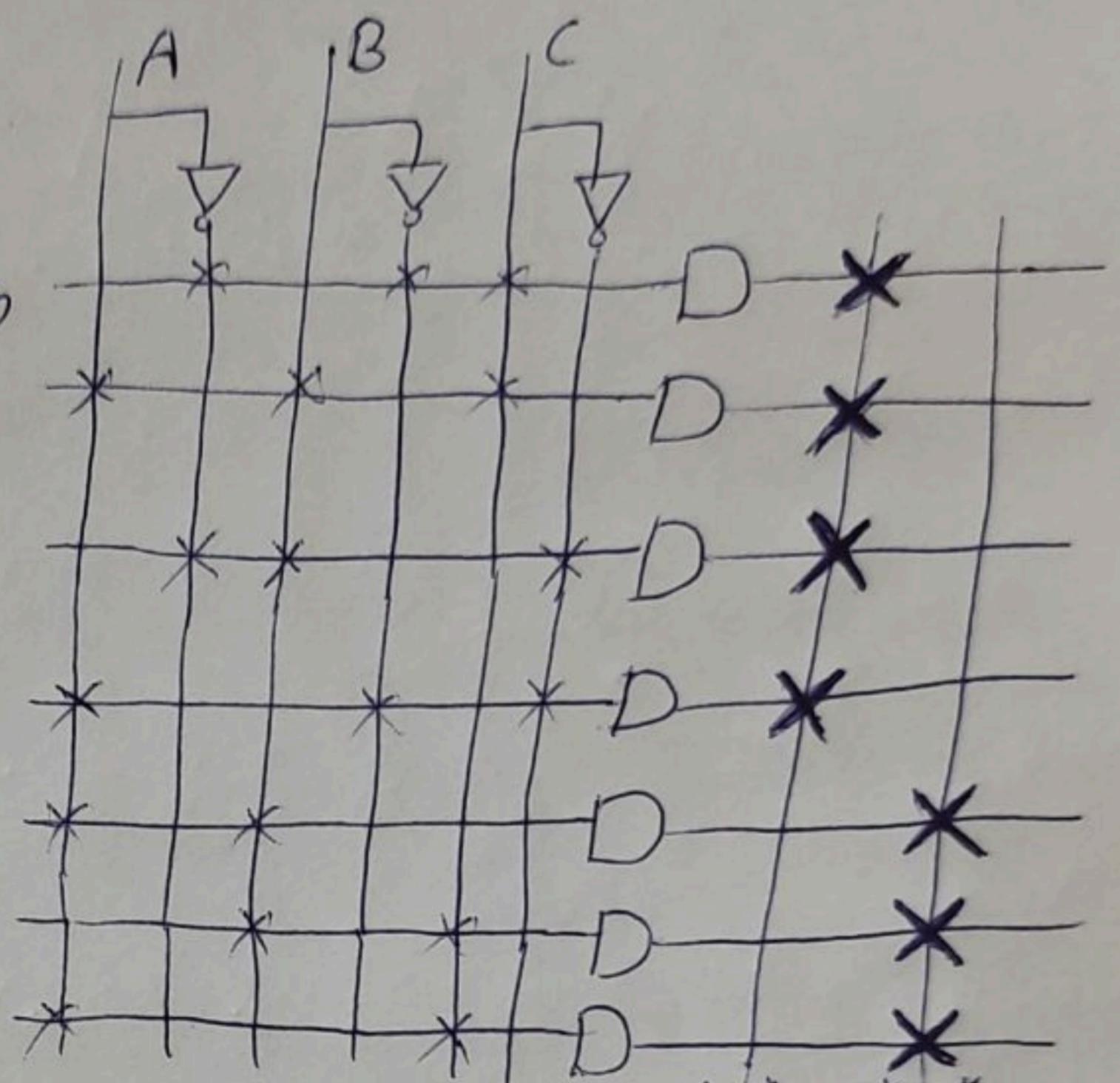
Ans PAL (Programmable Array Logic)

$$\text{Sum} = \bar{A}\bar{B}C + ABC + \bar{A}BC + A\bar{B}C$$

$$\text{Carry} = AB + BC + CA$$

X Programmable Connection

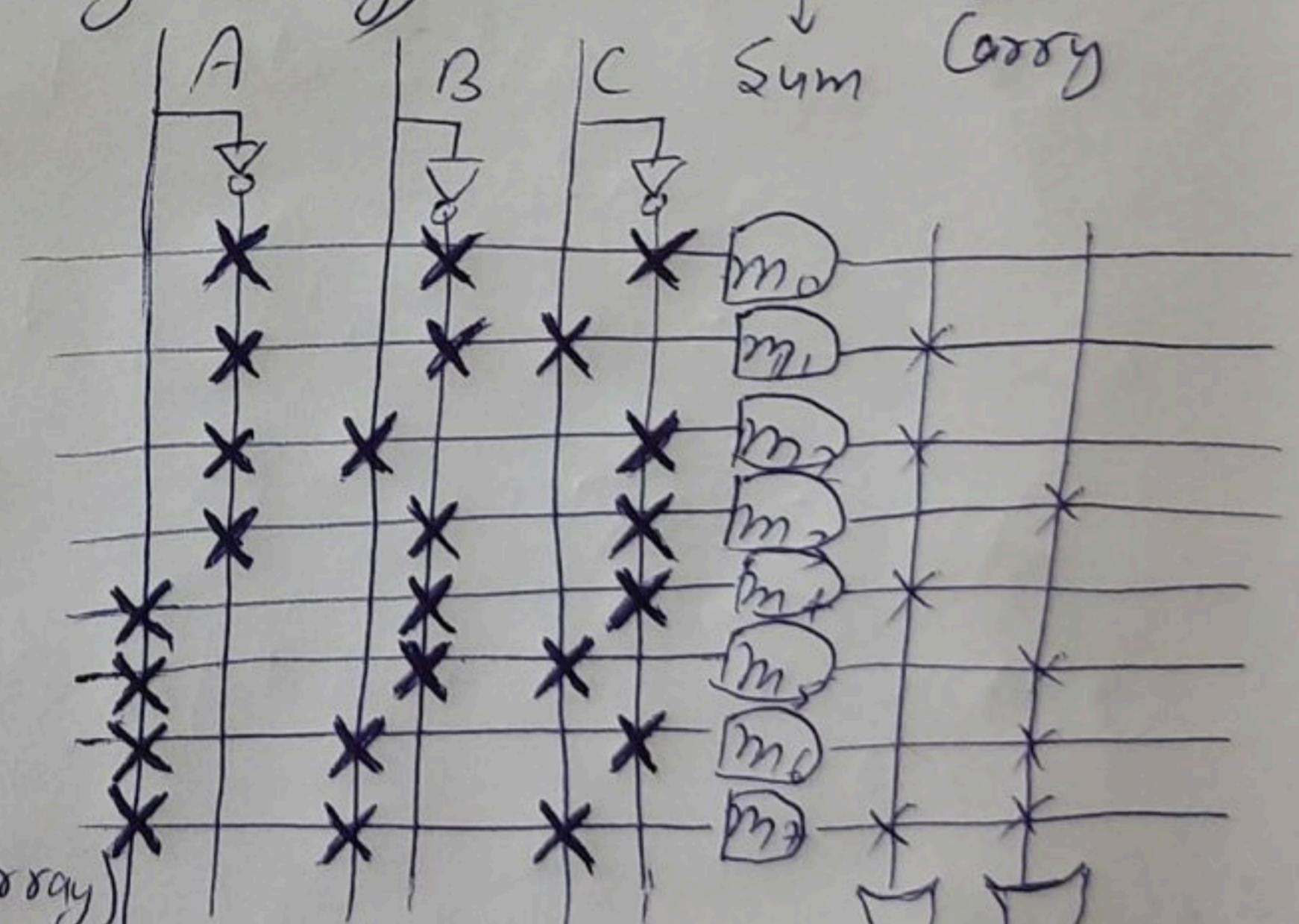
X Fixed Connection



PROM (Programmable Read Only Memory)

$$\text{Sum} = \sum m(1, 2, 4, 7)$$

$$\text{Carry} = \sum m(3, 5, 6, 7)$$



PLA (Programmable Logic Array)

$$\text{Sum} = \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C} + A\bar{B}C$$

$$\text{Carry} = AB + BC + AC$$

