ECE5009 Advanced VLSI System Design	L	T	P	J	C
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Prerequisite: Nil

Objectives:

- To describe the fundamental principles of digital design using CMOS logic
- To analyze the performance characteristics of the digital circuits
- To provide an in-depth understanding of digital logic and system design
- To design digital circuits using Verilog HDL
- To carryout the design of advanced digital hardware systems with the help of FPGAs.

Outcomes:

- An ability to analyze I-V characteristics and C-V characteristics of MOSFET.
- An ability to design combinational and sequential circuits using CMOS logic
- An ability to design and manually optimize complex combinational and sequential digital Circuits
- An ability to model combinational and sequential digital circuits using Verilog HDL
- An ability to design and model digital circuits with Verilog HDL at behavioral, structural, and RTL Levels

			SLO : 1,5,6,9,17,18	
Module:1	**CMOS Logic Design:**	**5**	**hours**	**SLO: 1,9,14**
Introduction to VLSI Design, Review of MOS Transistor Theory: nMOS, pMOS Enhancement Transistor, Ideal I-V characteristics, C-V characteristics, Non-ideal I-V effects. CMOS logic: Basic gates, Compound Gates, Transmission Gates based combinational and sequential logic design.				
Module:2	**CMOS Circuit characterization and Performance Estimation**	**5**	**hours**	**SLO: 1,9**
DC transfer Characteristics of CMOS inverter, Circuit characterization and performance Estimation: Delay estimation, Logical effort and Transistor Sizing. Power Dissipation: Static & Dynamic Power Dissipation.				
Module:3	**Verilog HDL Part-I**	**4**	**hours**	**SLO: 17,18**
Lexical Conventions - Ports and Modules – Operators - Gate Level Modeling - Data Flow Modeling - System Tasks & Compiler Directives - Test Bench				
Module:4	**Verilog HDL Part-II**	**4**	**hours**	**SLO: 1,17, 18**
Behavioral level Modeling- Procedural Assignment Statements- Blocking and Non-Blocking Assignments -Tasks & Functions - Useful Modeling Techniques.				
Module:5	**Verilog Modeling of Combinational Circuits**	**3**	**hours**	**SLO: 1,17**
Behavioral, Data Flow and Structural Realization of Adders and Multipliers				
Module:6	**Verilog Modeling of Sequential Circuits**	**3**	**hours**	**SLO: 1,17**
Synchronous and Asynchronous FIFO – Single port and Dual port ROM and RAM. FSM Modeling of Sequence detector, serial adder, vending machine.				
Module:7	**FPGA Architecture**	**4**	**hours**	**SLO: 1,5,6**
Types of Programmable Logic Devices-PLA, PAL, CPLD and FPGA Architecture.– Programming Technologies-Chip I/O- Programmable Logic Blocks- Fabric and Architecture of FPGA.				
Module:8	**Contemporary Topics**	**2**	**hours**	**SLO: 1,5,6,18**
# Mode: Flipped Class Room, [Any one of Lecture to be videotaped], Use of physical and computer models to lecture, Min of 2 lectures by industry experts				
	Total Lecture:	**30**	**hours**	

Text Books:		
1.	Neil H.Weste, Harris, A. Banerjee, "CMOS VLSI Design, A circuits and System Perspective", Fourth Edition, Pearson Education, 2010.	
2.	SamirPalnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", PHI, Second Edition,2003	
Reference Books:		
1.	Jan M. Rabaey, Anantha Chadrakasan, BorivojeNikolic, "Digital Integrated Circuits: A Design Perspective", Second Edition, Prentice Hall India, 2005.	
2.	T.N.Padmanabhan , ThirupuraSundari," Design Through VerilogHDL", Wiley Student Edition,2009.	
3.	Wayne Wolf, "FPGA Based System Design", Prentices Hall Modern Semiconductor Design Series, 2004.	
	Typical Projects:	**SLO: 5,17,18**
	Design and Implementation of 16-bit Ripple Carry Adder Design and Implementation of 8-bit Baugh-Woolley Multiplier Design and Implementation of 8-bit Arithmetic Logic Unit Design and Implementation of Simple Processor Design and Implementation of FIFO	