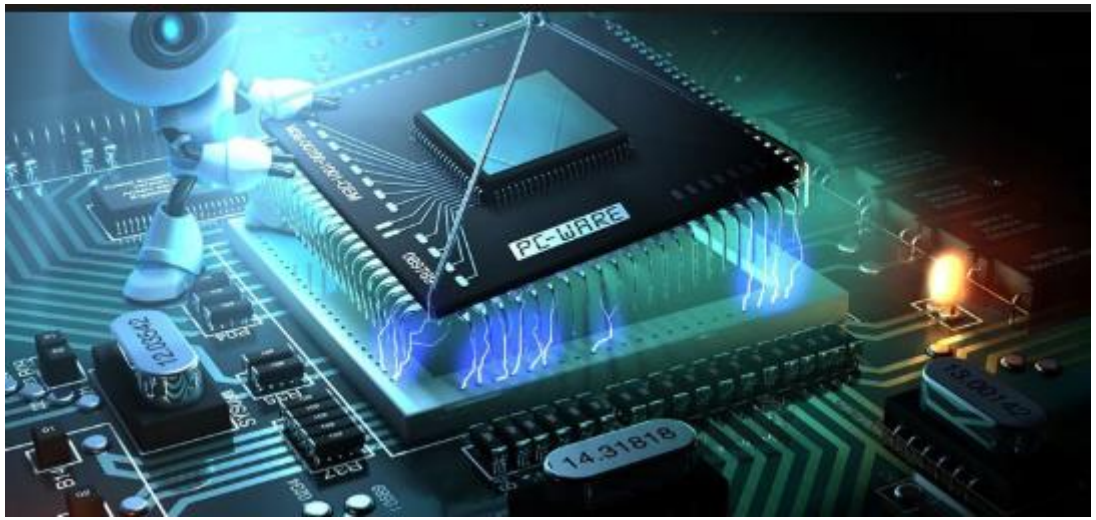
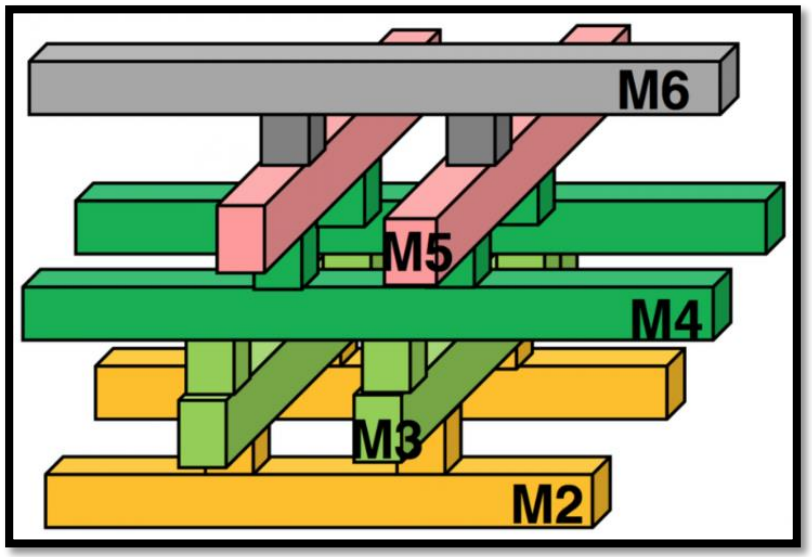
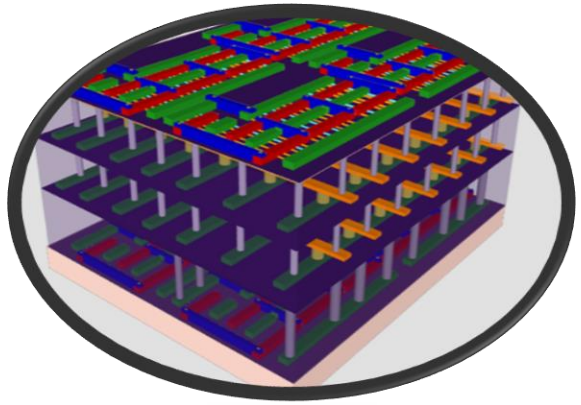




Routing & Post route optimization



Post cts checks (routing readiness)/Qualification checks to say that data is good enough to start route & post route

Below are the few post cts sanity checks to be performed before starting “routing and post route optimization”.

1. Congestion jump due to CTS /Is it acceptable
2. Cell/Pin/Congestion density map analysis - Acceptable pin/cell density
3. Reg2Reg WNS/TNS timing -Acceptable or/not
4. Acceptable SKEW /ID targets
5. Utilization jump from place_opt to clock_opt (utilization growth shouldn’t be big). If it’s the case, netlist is dirty/some basic problem exists in the design
6. Clock routing should be completed and clock net DRC’s were under control .

Pre –route checks

- **Check design for routing stage readiness**
- **There should not be:**
  - Ideal nets
  - High fanout nets greater than 500
- **Use `check_routeability` to check a design's prerequisites for detail routing and report a list of violations**


```
check_physical_design -stage pre_route_opt
all_ideal_nets
all_high_fanout -nets -threshold 501
check_routeability
```

check_routability

This sanity check command helps to identify many critical routing problems before routing stage.

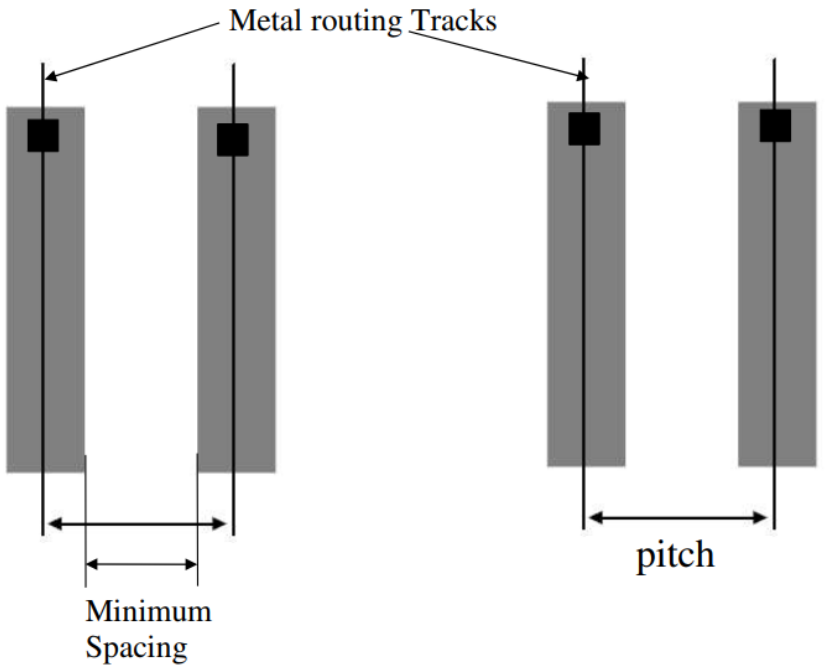
- Checks pin access points
- cell instance wire tracks
- pin out of boundaries, min-grid
- pin design rules and blockages to ensure they meet the design requirements.

You can use this command at every stage between placement and detail routing. Verify errors in the generated error cell or log file. You may have to perform manual fixes, as these problems may relate to library problems or issues with the floorplan

Design status before routing stage

1. Floorplan – Completed
2. Power and ground nets – prerouted
3. Placement – Completed
4. Estimated congestion – acceptable Horizontal and Vertical
5. Estimated timing – acceptable WNS/TNS value (Expected 0 ~ns)
6. Estimated Logical DRC’s
7. Acceptable clock physical DRC’s

Terminologies

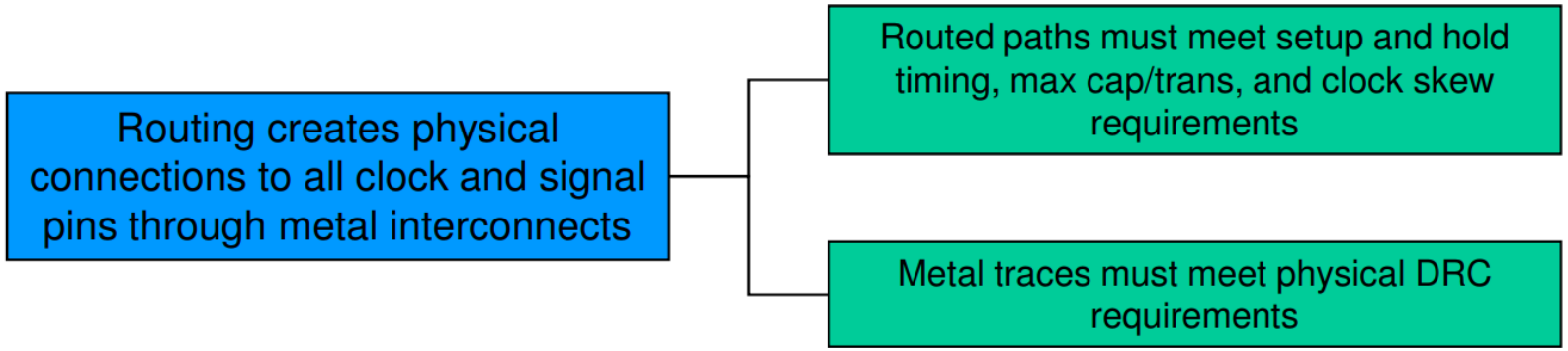


Pitch = minimum width + minimum spacing

Routing

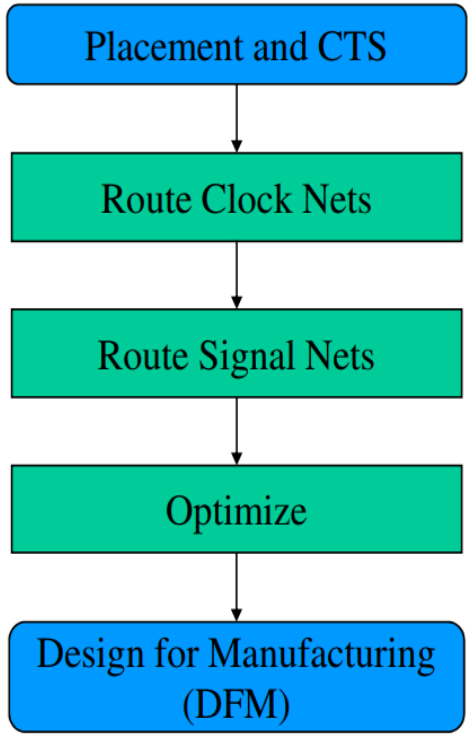
- As in 90nm and below technologies interconnect delays started to play a crucial role on IC performance, and routing issue is becoming more and more significant
- After all, routing substitutes the idealized connection lines of IC by real physical structures and provides physical operation of the circuit in real exploitation conditions
- Routing and its optimization are followed by finishing, which prepares the designed IC for manufacturing

Routing fundamentals :- Goal



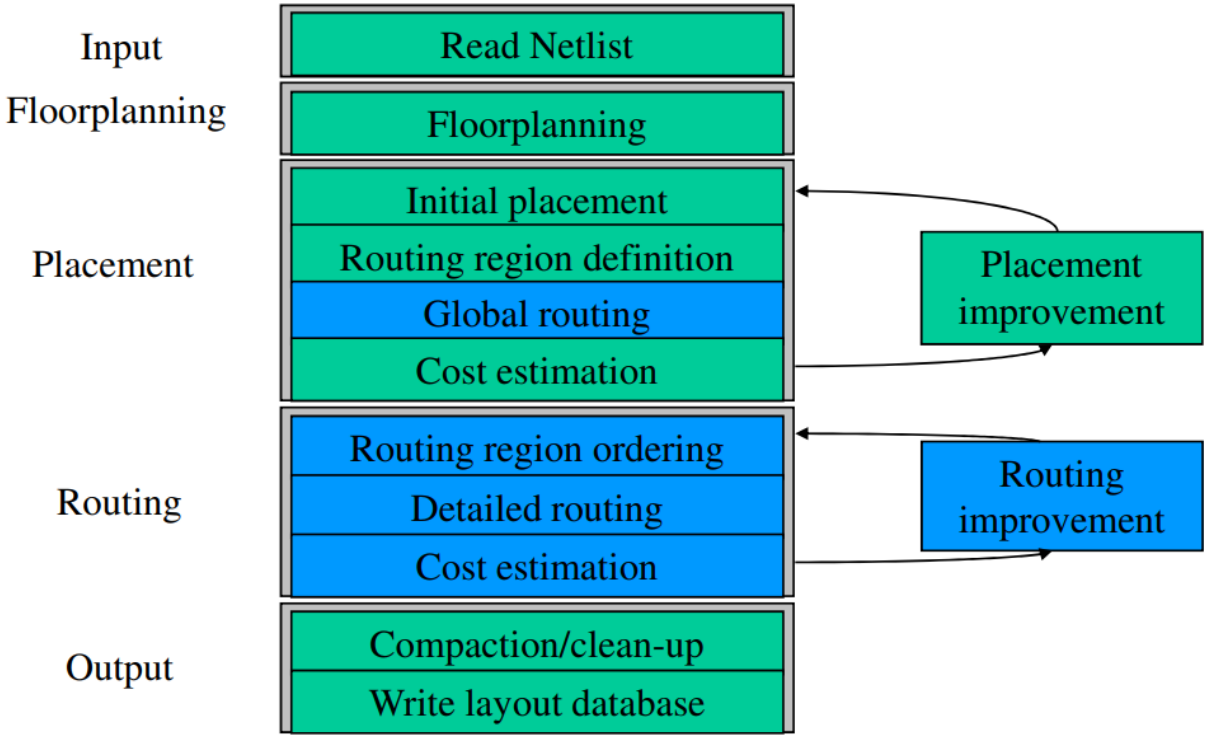
- Routing is the physical realization of all those interconnects between pins which are connected by an electrical circuit
- Those interconnects provide both signal and clock/power circuit realization and meet physical (DRC) and electrical (timing, capacitance/transmission, clock, etc) requirements
- Globally interconnects must provide minimal distortions from circuit operation by ideal connection lines to pass the operation through physical interconnects

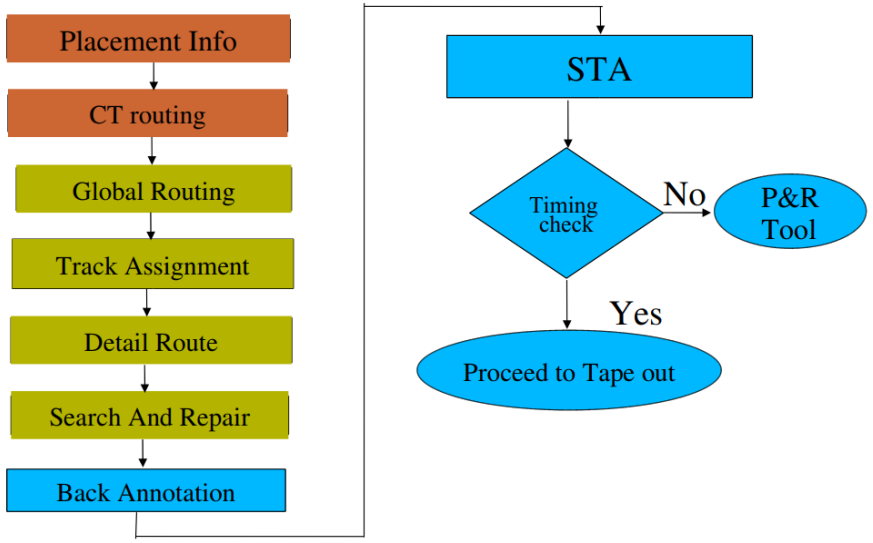
General flow of routing



- In all the design stages, preceding routing (floorplan, placement and CTS), provision of better conditions has been the most important for further routing. This is
  also called routability
- Generally IC electrical circuits in the sense of functionality are divided into 3 groups – signal nets, clock nets and power nets
- In the stage of routing, the physical design of clock nets and power nets are performed (illustrated in figure)

Routing steps in physical synthesis





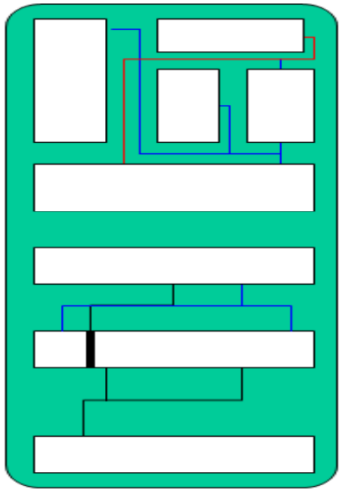
Steps in routing step

1. Global routing
2. Track assignment
3. Detailed routing
4. Search and repair technique

Global routing

- Global Route (GR) is the first step in routing and it gives more accurate parasitic and delay estimates compared to VR.
- The global Route that is performed during routing will be used by the subsequent Track Assign stage
- Global routing is not DRC aware

- ✓ Given
  - Placement of blocks/cells
  - Channel capacities
- ✓ Determine
  - Routing topology of each net
- ✓ Optimize
  - Maximum number of nets round
  - Minimum routing area
  - Minimum total wirelength



Track assignment

- Track Assignment (TA):
  – Assigns each net to a specific track and lays down the actual metal traces.
- It also attempts to:
  – Make long, straight traces.
  – Reduces the number of vias.
- It does not check or follow physical DRC rules

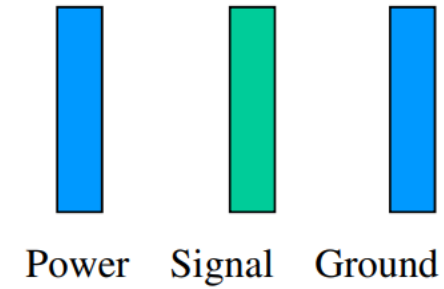
Detailed routing

Detail Routing
– Input channels and approximate routing from the global routing phase
– Determine the exact route and layers for each net
– **Objective**: valid routing, minimize area (congestion), meet timing constraints
– Additional objectives: minimum via, power

Shielding

- ✓ Shielding
  - Same-layer shielding
  - Adjacent-layer shielding

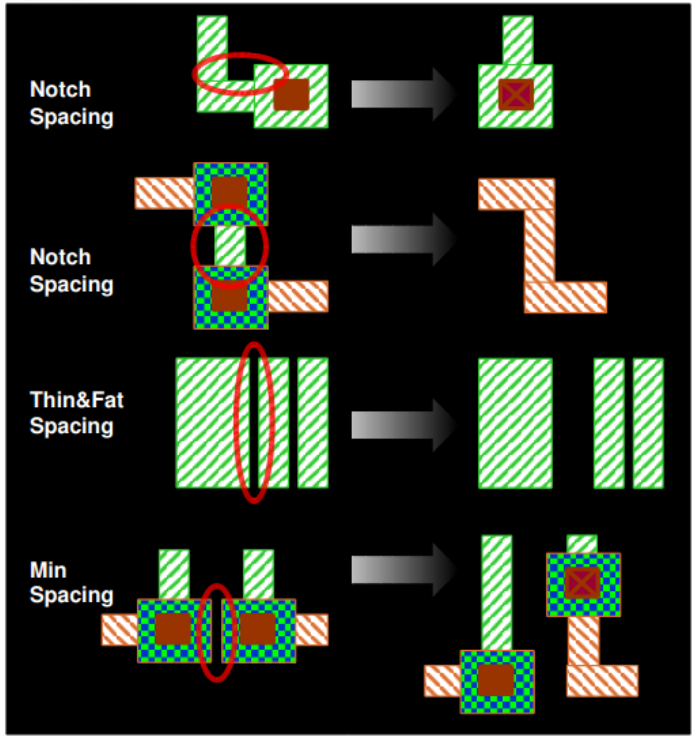
Same-layer shielding



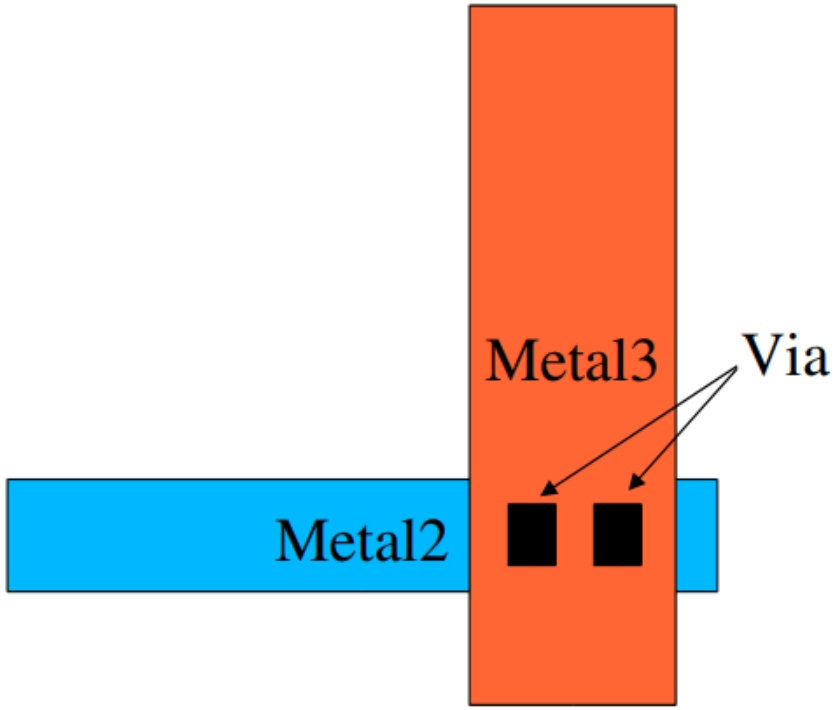
Adjacent-layer shielding

Important Metal DRC's

1. Shorts
2. Notch spacing
3. Diff net spacing
4. Same net spacing
5. Diff net via cut spacing
6. Thin/Fat spacing

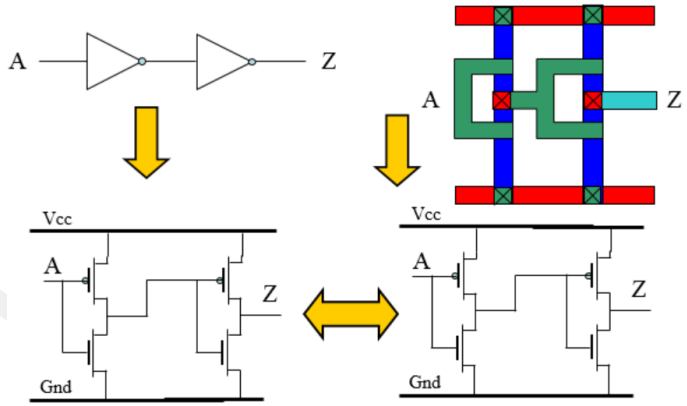


Redundant via



LVS (Layout versus schematic)

- LVS is check it determines whether a particular IC layout corresponds to the original schematic or circuit diagram (Verilog netlist in this case) .
- DRC ensures that layout confirm to the rules designed/required for faultless fabrication , it doesn't guarantee if it really represent the circuit desire to fabricate.



Common errors encountered during LVS

1. Shorts: Two or more wires that should not be connected have been and must be separated.

2. Opens: Wires or components that should be connected are left dangling or only partially connected. These must be connected properly to fix this.

3. Component Mismatches: Components of an incorrect type have been used (e.g. a low Vt MOS device instead of a standard Vt MOS device)

4. Missing Components: An expected component has been left out of the layout.

Key metrics to be checked after routing/route-optimization

1. Nets routed without any opens (verify_lvs)
2. Physical DRC numbers (verify_zrt_route/verify_route)
3. Timing QORs details
4. Apply the logical PG connection to newly added cells (derive_pg_connection)
5. Acceptable congestion values
6. Acceptable DRV’s
7. LVS error understandings/fixes (verify_lvs)

Tools used for routing

1 ICC2 – Synopsys

2. EDI and Innovus (CCOPT) – Cadence

3. Aprisa – Avatar integrated systems

Route and route opt related lab exercises

1. Complete route and route_opt
2. RVI insertion flow
3. Filler cells insertion flow
4. analyze the timing before/after route
5. Create / Understand the DRC’s


THANKS