FARADAY

Embedded Flash Modules

Frequently Asked Questions

Do I Want Embedded Flash in My ASIC?

Embedding Flash memory on an ASIC can have significant system-level advantages. But it adds to the design process and the number of layers in IC fabrication.

Why would I want to use eFlash?

Most designers use embedded Flash memory for code storage, especially for boot code. It can also be used for parameter storage—for instance, to store weights for a deep-learning inference engine—or security or encryption purposes. Placing the Flash memory block on the ASIC die can have significant advantages for the system.

So what are these advantages?

Our customers often compare eFlash with the next best alternative, a system in package (SiP) that combines an external Flash die with their ASIC. Compared to a SiP approach, eFlash eliminates one die from the SiP, potentially making room for another die, such as SRAM, DRAM, or a wireless chip. Moving these dies into the SiP will improve system power, performance, and area (PPA).

But looking just at the impact on Flash operation, on-die eFlash will offer lower latency to first data availability because of the much faster on-die interconnect. It will also provide higher transfer rates because eFlash can have up to a 128-bit-wide connection to the rest of the ASIC circuitry compared to 4 or 8 bits for a separate Flash die. And the eFlash will consume less power because it won't continually toggle I/O lines that pass between dies.

If we compare Flash in a separate package, the advantages are the same but more significant due to the slower, more power-hungry connections between packages.

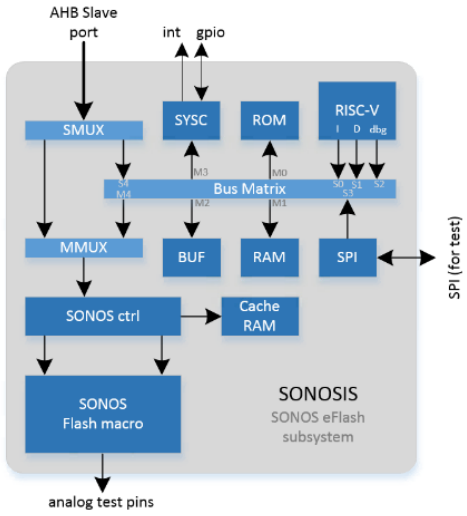
And what are the disadvantages?

The main disadvantage of eFlash is that, compared to a pure logic process, eFlash requires more mask layers and will increase wafer costs. In most designs, an eFlash solution will have a slightly higher bill-of-materials cost than a system using a separate Flash die. But even that cost difference may be balanced by the added costs of using a separate Flash die: having known good die for the SiP, the added assembly and test requirements, and so on.

Additionally, some designers have avoided exploring embedded Flash because of the technology's reputation for requiring specialized logic, mixed-signal circuitry, and extra CPU software for reading, writing, and control functions. But with Faraday's solution and our extensive IP, that is no longer an issue for the design team. Using eFlash can be nearly as simple as including a block of SRAM.

Do you mean I don't have to deal with all that Flash-specific circuitry?

That is correct. Faraday's eFlash solution includes the Flash array and an embedded controller. Faraday has integrated these into a complete Flash subsystem. For example, in our 40nm eFlash solution, which we co-designed with Infineon, you get the bus interface, integrated clock control circuits, and additional features, such as automatic eFlash initialization, a simplified erase/write procedure that offloads these tasks from the CPU, read/write protection, and a pseudo-random write buffer. The result is seamless IP integration and utilization of eFlash IP.



The complete 40nm SONOS eFlash subsystem

What if I need additional features, such as error correction or encryption?

We can discuss these needs on a case-by-case basis. Faraday's extensive IP libraries can support these needs directly. And our design support team will work with you on implementing your requirements.

What about test? I understand Flash requires specific test equipment and algorithms.

Faraday's three 40nm integrated eFlash subsystems include memory built-in self-test functionality. This functionality means that you can test your ASIC on a conventional logic test system but still get the quality and reliability guarantees you would from a dedicated Flash test system. And our BIST approach cuts total test time.

In which processes is eFlash available?

Faraday currently produces eFlash on our 55nm and 0.11µm ASIC processes and SONOS eFlash—codeveloped with Infineon—on our 40nm process. In the future, we will provide a different eFlash technology, RRAM, on 22nm.

Geometry	0.11um	55nm	40nm
Process	eFlash	55ULP/LP eFlash	40ULP
Extra mask	11	11	6
eFlash macro/ **Vendor**	eFlash UMC	SST UMC, UDS	SONOS Infineon

What maximum capacity and what kind of performance does eFlash offer?

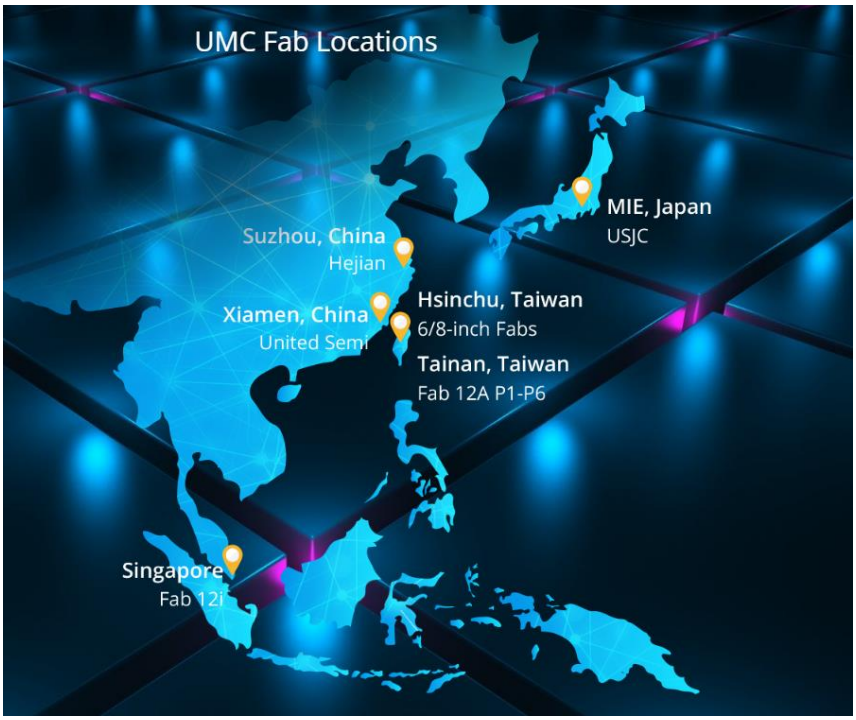
On our 55nm process, we offer up to 16Mbits per eFlash macro. On our 40nm SONOS process, this expands to 32Mbits per macro. In either case, the read access time is approximately 25nm for a 64-bit access.

What about the endurance, data retention, and operating temperature range?

In both 55nm and 40nm processes, we spec the eFlash endurance at 100K cycles and the operating temperature range at -40 to +125C. Data retention varies between the two processes: 20 years for the 55nm eFlash, and ten years for the 40nm SONOS array.

I have to be careful about supply-chain constraints. Am I limiting myself to one fab or geographic region using eFlash?

No. Faraday can supply eFlash from various 12-inch wafer fabs throughout Asia, including Taiwan, China, Singapore, and Japan.



UMC offers a geographically diverse selection of fabs

Who should I contact to discuss our design needs further?

We at Faraday are ready to engage with your design team today. We want to discuss your specific needs and dive into greater detail about our fully integrated eFlash IP subsystem, how we can work with your team on each step in the design process, and how you can best exploit the fabs, assembly, and test facilities in our global supply chain.

Please get in touch with us at ussales@faraday-tech.com