ECE5024	IC TECHNOLOGY	L	T	P	J	C
		3	0	0	0	3
Pre-requisite	**Nil**					**v 1.1**

Course Objective:

The course is aimed to

1. Introduce the process involved in semiconductor manufacturing and fabrication.
2. Model the oxidation growth rate & to understand oxidation process and the process of diffusion and to expound the Ion Implantation process.
3. Explain the thin film deposition process and review the difference between MOS and Bipolar Process Integration.

Expected Course Outcome:

At the end of the course the student will be able to

1. Understand the process involved in semiconductor manufacturing and fabrication.
2. Understand the various lithography techniques used for pattern transfer.
3. Model the oxidation growth.
4. Model the diffusion mechanism in semiconductors.
5. Understand the process involved in thin film deposition.
6. Analyse the difference between MOS and Biploar Process.

Student Learning Outcomes (SLO): **1,17**

Module:1	**Crystal Growth**	**5 hours**

Introduction to Semiconductor Manufacturing and fabrication, Clean Room types and Standards, Physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers.

Module:2	**Lithography:**	**7 hours**

The Photolithographic Process, Photomask Fabrication, Comparison between positive and negative photoresists, Exposure Systems, Characteristics of Exposure Systems, E-beam Lithography, X- ray lithography.

Module:3	**Thermal Oxidation of Silicon:**	**6 hours**

The Oxidation Process, Modeling Oxidation, Masking Properties of Silicon Dioxide, Technology of Oxidation, Si-SiO2 Interface.

Module:4	**Diffusion and Ion Implantation:**	**7 hours**

The Diffusion Process , Mathematical Model for Diffusion, Constant- ,The Diffusion Coefficient , Successive Diffusions, Diffusion Systems, Implantation Technology, Mathematical Model for Ion Implantation, Selective Implantation, Channeling, Lattice Damage and Annealing, Shallow Implantations.

Module:5	**Thin film deposition, contacts, packaging and yield:**	**7 hours**

Chemical Vapor Deposition, Physical Vapor Deposition, Epitaxy, Metal Interconnections and Contact Technology, Silicides and Multilayer-Contact Technology, Copper Interconnects and Damascene Processes, Wafer Thinning and Die Separation, Die Attachment, Wire Bonding,

Packages, Yield.		
Module:6	**MOS Process Integration:**	**5 hours**
Basic MOS Device Considerations, MOS Transistor Layout and Design Rules, Complementary MOS (CMOS) Technology.		
Module:7	**Bipolar Process Integration:**	**6 hours**
Isolation Techniques in BJT fabrication, Advanced Bipolar Structures, Other Bipolar Isolation Techniques. Deep Submicron Processes, Low-Voltage/Low-Power CMOS/BiCMOS Processes. Future Trends and Directions of CMOS/BiCMOS Processes.		
Module:8	**Contemporary issues:**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	S.M. Sze, VLSI technology, Tata McGraw-Hill, SecondEdition, 2017.
2.	R.C. Jaeger, Introduction to microelectronic fabrication, Prentice Hall, Second Edition, 2013.
Reference Books	
1.	S.A. Campbell, The science and engineering of microelectronics fabrication, Oxford University Press, UK, SecondEdition, 2012.
2.	Simon M. Sze, Gary S. May Fundamentals of Semiconductor Fabrication, Wiley, 2011.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

Recommended by Board of Studies	28/02/2017		
Approved by Academic Council	47th AC	Date	05/10/2017