Analog IC Design Process

Specifications
&
Expected Performance

Choose Circuit
Topology

Hand Design
(sizing & biasing)

OrCAD PSpice
Cadence Design Systems

Schematic Capture
(Schematics)

Net list

MOSIS 0.8 µm
"EE534 Process"

Optimization &
Trade-offs

Simulation
(PSpice A/D)

Device
Libraries

LASI

Physical Layout
(LASI)

Table of
Layers

Design Rule Checker
(LasiDrc)

Design
Rules

Net list Extractor
(LasiCkt)

Parasitics

Net list

Simulation
(PSpice A/D)

Layout
vs.
Schematic

OK

Codification
(Gds2Tlc)

Conversion
Table

Wafer Foundry Processing