LP Verification challenges and coverage recipe to sign-off PA verification

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Introduction

- Today's system - on-chip (SoC) designs are composed of different blocks running multiple applications with varying power requirements.
- Power intents are defined ONLY in UPF (Unified Power Format) as a separate and standard power specification format.

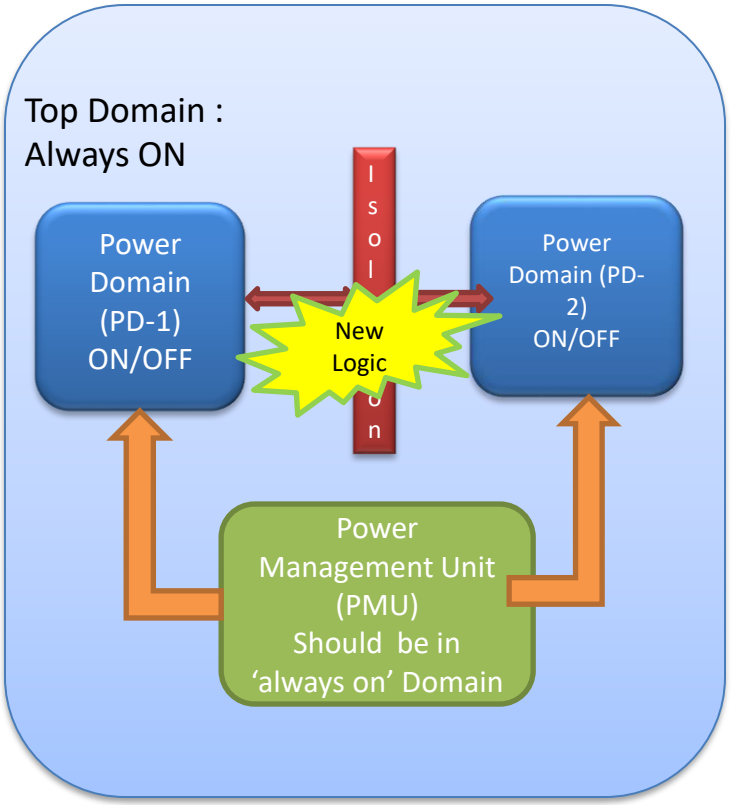
Power aware (PA) verification totality :UPF needs to be verified along with the RTL such that the design meets both *functional and power intent.*

Why low power verification ?

Power aware(PA) verification ensures :

-Correctness of design when Power Domains(PD) are OFF/ design is Powered-down

-Power domains come up in good known states by signal restoration of retained values for the sequential elements



Power Aware Design

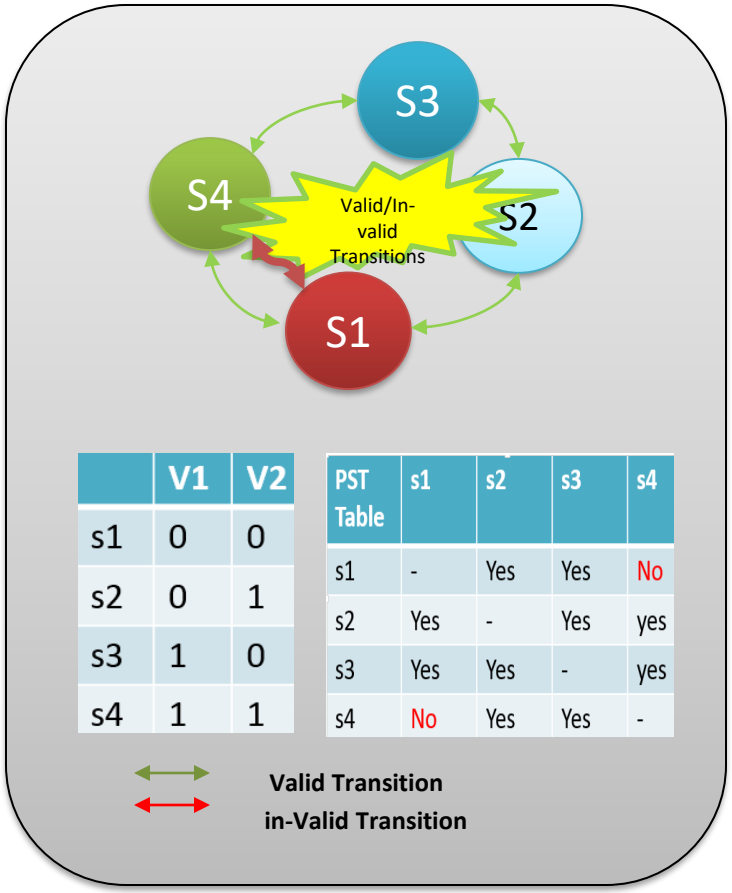
Why low power verification ?

Power aware(PA) verification allows Valid and In-valid states/transitions /Scenarios to be checked early in the design cycle.

Lets say design has 2 supply- v1 & V2

Possible states: 2^2 (s1, s2, s3 & S4)

Illegal transition :“s1->S4” and “s4 ->s1”



	V1	V2
s1	0	0
s2	0	1
s3	1	0
s4	1	1

PST Table	s1	s2	s3	s4
s1	-	Yes	Yes	No
s2	Yes	-	Yes	yes
s3	Yes	Yes	-	yes
s4	No	Yes	Yes	-

Power Aware Verification

Low Power Verification challenges

Verification of “Power intents” in aggregation with RTL remains a challenge with sprouting power format.

Low power verification challenges are:

- To retain sufficient state information to enable restoration of functionality when power is restored
- Power switch off/on duration
- Transitions between different power modes and states
- Interface between power domains
- Missing of level shifters, isolation and retention
- Legal and illegal transitions
- Clock enabling/toggling
- Verifying retention registers and isolation cells and level shifter Strategies

Debug challenges in PA verification

Power–related error during verification can be due to :

Error found in PA designs ***"caused by RTL"*** or the behavior defined in the ***"power specification code (UPF)"***

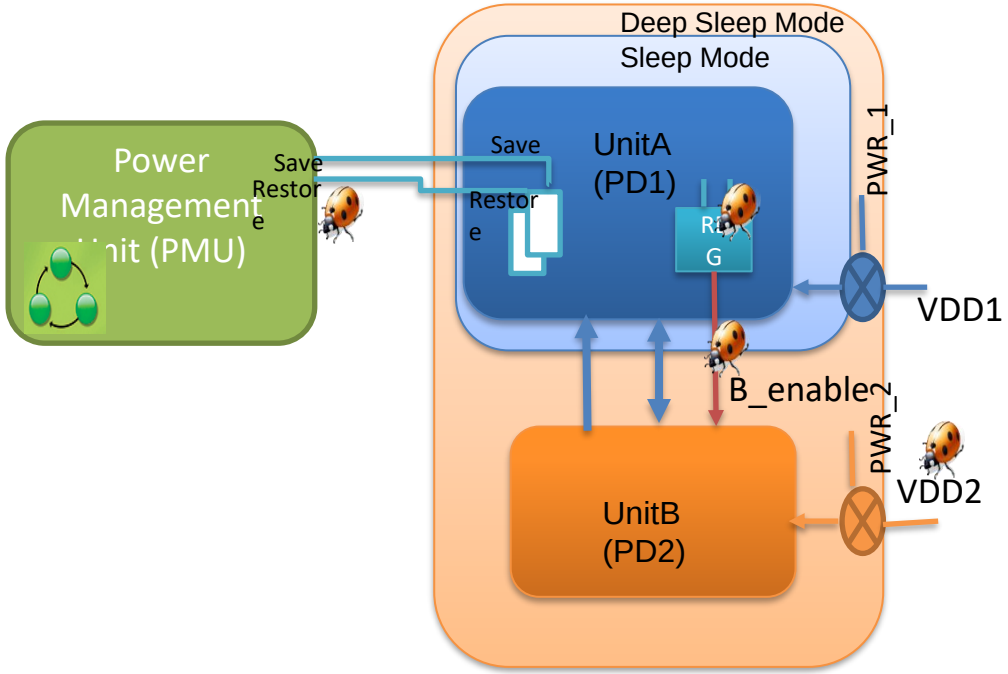
Cause of "X" in power aware simulations:

*Is it due to **"Power down/off"** ?*
or
"Functional Bugs " *?*

Verification "Debug" tools/ Capablities must understand the power specifications

Typical challenging scenario in PA verification

- Due to missing isolation cells
- Incorrect Specification of Save Signal in UPF
- Missing Retention cell between Power Domain
- Due to incorrect save & restore power sequence
- Incorrect connections of Power supply to power domains

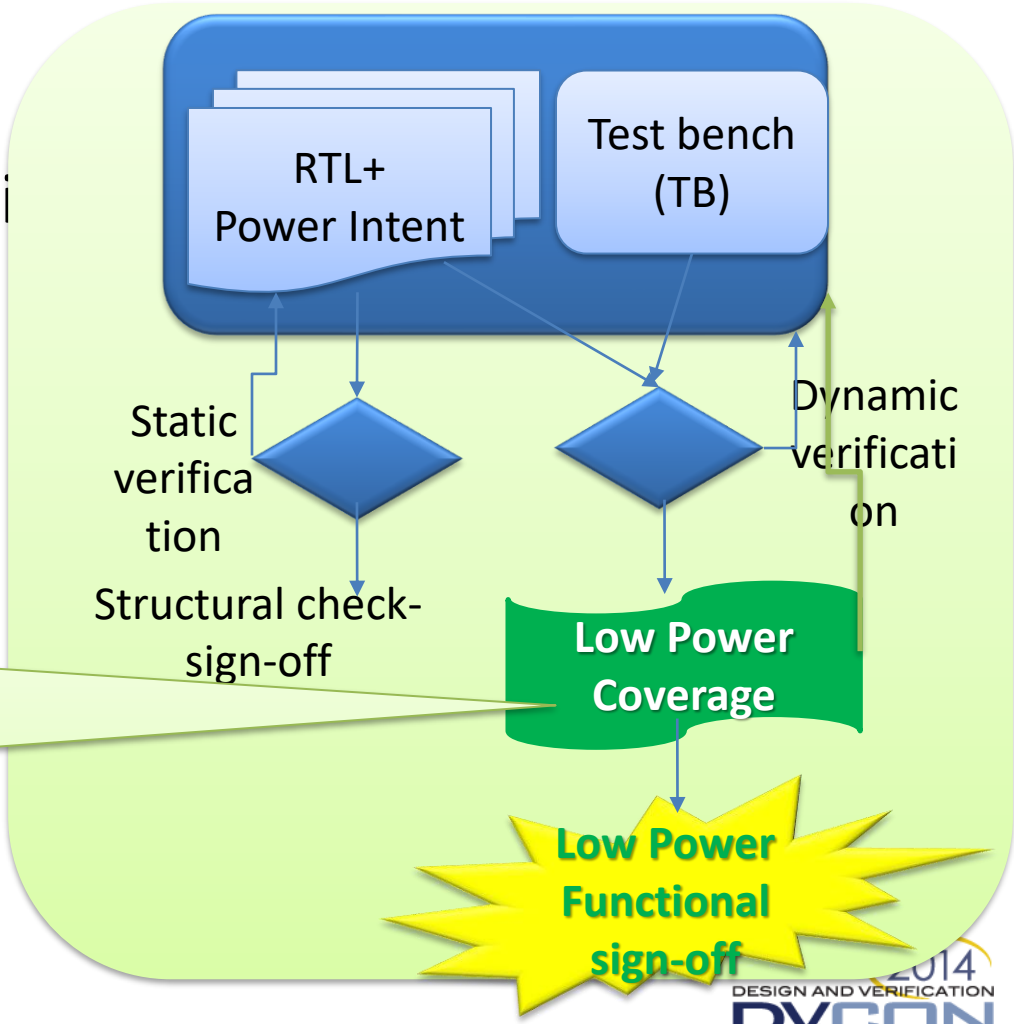


Debug solution: Features requisite for LP debug capabilities

Power Map/Schematic	•Schematic representation of power domains and power networks to understand the UPF
Cross-probe between different views	•Through cross-probing , power elements (isolation , retentionl etc) in UPF can be visualized in the schematic view, so the signal's connection can be inspected
Locate the root cause of a bad value ("X") in either RTL or UPF	•Trace power related unknowns •Understand design /Power intent behavior and locate the "X" •Easy visualization of behavior with time and structure
Annotate power intent on RTL, schematic and waveform views	•Annotate power modes on different views, e.g RTL, waveform, schematic and Trace retention, isolation & level shifter signals & power related unknowns
Un-roll paths through different power domains	•Un-roll paths through different power domains •Trace the failing pattern cycle-by-cycle through data paths until the causes are located.
Provide visualization for the signals driven by UPF	•Provide visualization for the signals driven by UPF

Sign-off criteria for PA verification

Low power coverage is a essential requisite in addition to “static & dynami checks” for low power functional sign-off confidence as



what is “not verified” by static and dynamic checks can be validated ONLY by Low power coverage.

LP coverage intercept during PA verification

What is LP coverage methodology ?

Low power coverage methodology identifies the coverage of low power objects for sign-off confidence.

Low Power coverage methodology :

- Ensure all states in Power state table (PST) has been exercised
- Ensure all transitions in Power state transition table has been occurred as per power specification
- Ensure power switch switched between ON and OFF states
- Ensure Control signals toggle
- Full power-up /power down sequence
- Do we see illegal states/transitions?
- *Assist validation engineers to identify the holes/un-covered test – sequences during power aware verification*

Detailed Coverage analysis for PST

PST coverage help to identify the power states/transitions which has not been verified hence pinpoints the test sequences to exercise the unverified power states/transitions.

Legal states: S1, S2, S3, S4, S5 and S6

Legal Transitions: Any transitions between S1 to S6

Illegal states: S7-S32

Illegal transitions: Any transition between Legal states to illegal states

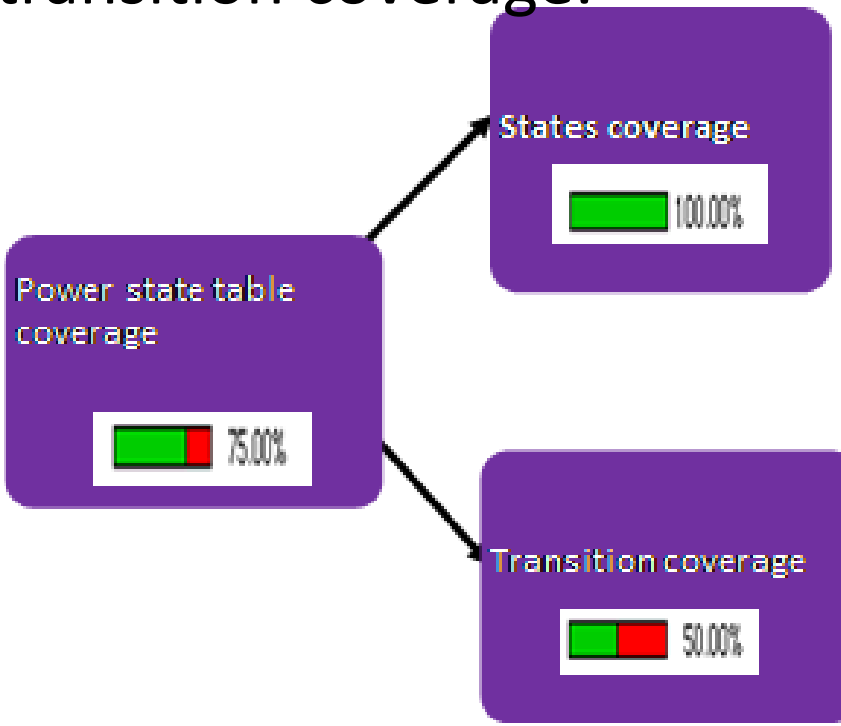
S1->(S7-S32), S2->(S7-S32), S3->(S7-S32), S4->(S7-S32), S5->(S7-S32),S6->(S7-S32),

```
create_pst pt -supplies          { V1  V2 V3 V4 V5 }
add_pst_state S1 –pst pt –state { ON ON ON ON OFF }
add_pst_state S2 –pst pt –state { ON ON ON OFF ON }
add_pst_state S3 –pst pt –state { ON ON OFF ON ON }
add_pst_state S4 –pst pt –state { ON OFF ON ON ON }
add_pst_state S5 –pst pt –state { OFF ON ON ON ON }
add_pst_state S6 –pst pt –state { ON ON ON ON  ON }
```

Legal PST entries in UPF

Detailed Coverage analysis for PST

Overall PST coverage is the accumulative coverage of state and transition coverage.



Status	Bin Name	At Least	Size	Hit Count
Illegal Bin	ILLEGAL	1	1	0
✓	cnn_OFF	1	1	602
✓	cnn_ON	1	1	602
✓	cnn_new	1	1	275

Status	Bin Name	At Least	Size	Hit Count
Illegal Bin	ILLEGAL => cnn_OFF_Ille...	1	1	0
Illegal Bin	ILLEGAL => cnn_ON_Illegal	1	1	0
Illegal Bin	ILLEGAL => cnn_new_Ille...	1	1	0
Illegal Bin	cnn_OFF => ILLEGAL_Ille...	1	1	0
✓	cnn_OFF => cnn_ON	1	1	602
X	cnn_OFF => cnn_new	1	1	0
Illegal Bin	cnn_ON => ILLEGAL_Illegal	1	1	0
✓	cnn_ON => cnn_OFF	1	1	327
X	cnn_ON => cnn_new	1	1	0
Illegal Bin	cnn_new => ILLEGAL_Ille...	1	1	0
✓	cnn_new => cnn_OFF	1	1	275
X	cnn_new => cnn_ON	1	1	0

Detailed Power State Table (PST) coverage analysis in Dynamic simulator

“Key” takeaways of LP coverage

The Quality of Power Aware verification is measured through “Low Power coverage” and it improves the power aware verification ***sign-off confidence***.

Key benefits includes:

- It provides dynamic approach to validate low power implementation
- Identify Uncovered gaps in the low power verification test plan
- Easy bucketization of the low power checks for improving coverage
- As part of regression, the verification engineers gets to know both his functional and low power coverage with zero impact

Recommendation

- Static and dynamic checks of RTL & Power-intent for PA verification
- Need for Low power debugger capabilities to reduce the validation effort.
- LP coverage should be a part of overall verification test plan.
- Run the LP tests along with functional tests -It confirm the functionality of the design doesn't get impacted by enabling power-saving features.
- LP tests should be checked with coverage numbers in addition to traditional pass/fail mechanism.

It is extremely important to plan low power specific coverage from start and track it till design closure

Questions