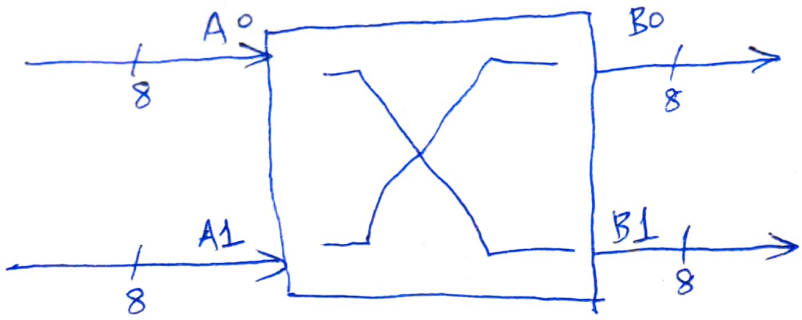
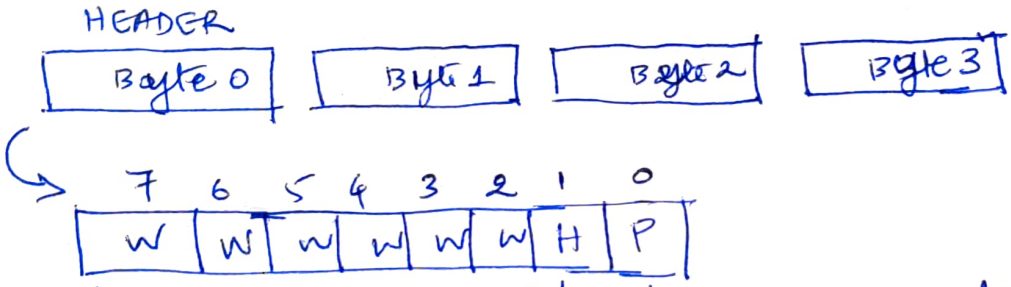
SIMPLE SWITCH



- Needs to perform switching function @ 100MHz clock frequency
- Packets consist of 4 bytes



0 – output is on port B0

1 – output is on port B1

Indicates high priority packet

max. Wait time in clock cycles if it is a high priority packet

- Input and output width is 1 byte or 8-bits
- ~~Design~~ Submissions (hand written is also allowed)

1. Detailed design document
2. Verilog code
3. Verification strategy
4. Switch latency