ECE5022	VLSI DIGITAL SIGNAL PROCESSING	L	T	P	J	C
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Pre-requisite	**Nil**					**v 1.1**

Course Objective :

The course aimed to:

1. Familiarise various representation methods of DSP algorithms, understand the significanceof the iteration bound and to calculate the same for a given single-rate and/or multi-rate DFG.
2. Understand and apply the architectural transformation techniques such as retiming, unfolding and folding on a given DFG.
3. Introduce the algorithmic and numerical strength reduction methods for performance improvement.
4. Signify and calculate the effects of scaling and round-off noise for a given digital filter with limited word length.

Expected Course Outcome:

The students will be able to:

1. Compare various representation methods of DSP algorithms.
2. Find iteration bound of a given single and/or multi-rate DFG.
3. Understand and transform the given DFG using retiming with constraints.
4. Apply unfolding and folding transformations on the given DFG.
5. Understand and apply algorithmic and numerical strength reduction methods.
6. Understand and calculate scaling and round-off noise of the given digital filter with limited word length.

Student Learning Outcomes (SLO):	**1, 9**

Module:1	**Introduction to Digital Signal Processing**	**5hours**

Typical DSP Algorithms - DSP Application Demands and Scaled CMOS Technologies - Representations of DSP Algorithms - Data-Flow Graph Representations.

Module:2	**Iteration Bound**	**5hours**

Introduction - Loop Bound and Iteration Bound - Algorithms for Computing Iteration Bound: Longest Path Matrix and Multiple Cycle Mean algorithms - Iteration Bound of Multi-rate Data Flow Graphs.

Module:3	**Pipelining, Parallel processing and Retiming**	**8hours**

Pipelining and Parallel Processing - Introduction to Retiming - Definitions and Properties - Solving Systems of Inequalities - The Bellman-Ford Algorithm - The Floyd Warshall Algorithm- Retiming Techniques.

Module:4	**Unfolding**	**6 hours**

Introduction, An Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding, and Retiming, Applications of Unfolding.

Module:5	**Folding**	**6hours**

Introduction, Folding Transformation, Register Minimization Techniques, Register Minimization

in Folded Architectures.		
Module:6	**Algorithmic & Numerical Strength Reduction**	**7hours**
Introduction to Algorithmic Strength Reduction, Cook-Toom Algorithm, Iterated Convolution, Cyclic Convolution, Discrete Cosine Transform. Introduction to Numerical Strength Reduction,Canonic Signed Digit Arithmetic, Sub-expression Elimination, Multiple Constant Multiplication, Sub-expression Sharing in Digital Filters.		
Module:7	**Scaling and Rounding Noise**	**6hours**
Introduction, Scaling and Rounding Noise, State Variable Description of Digital Filters, Scaling and Rounding Noise Computation, Rounding Noise in Pipelined IIR Filters.		
Module:8	**Contemporary issues:**	**2hours**
	Total Lecture:	**45hours**
Text Book(s)		
1.	KeshabK.Parhi, VLSI Digital Signal Processing Systems: Design and Implementation,Reprint,Wiley, Inter Science, 2014.	
Reference Books		
1.	John G. Proakis, Dimitris K Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, Prentice Hall, Fourth Edition, 2015.	
2.	Mohammed Ismail and Terri Fiez, Analog VLSI Signal and Information Processing,McGraw-Hill, 2014.	
3.	S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, PHI, 2010.	
4.	S. K. Mitra, Digital Signal Processing – A Computer Based Approach, Fourth Edition, McGraw-Hill, 2010.	
Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).		
Recommended by Board of Studies	28/02/2017	
Approved by Academic Council	47th AC	Date 05/10/2017