vlsi4freshers

ROADMAP TO START YOUR CAREER IN VLSI

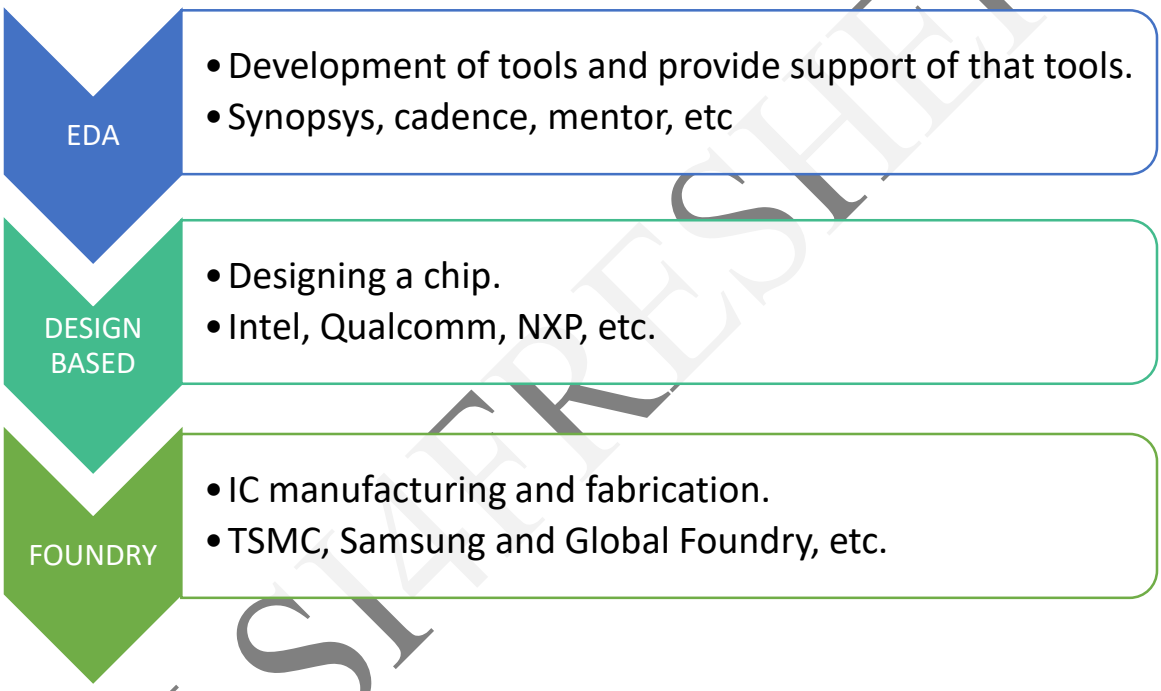
Prepared By: Vivek Arya

LinkedIn Profile: https://www.linkedin.com/in/vivek-arya-532558143/

How to prepare for a VLSI profile from scratch?

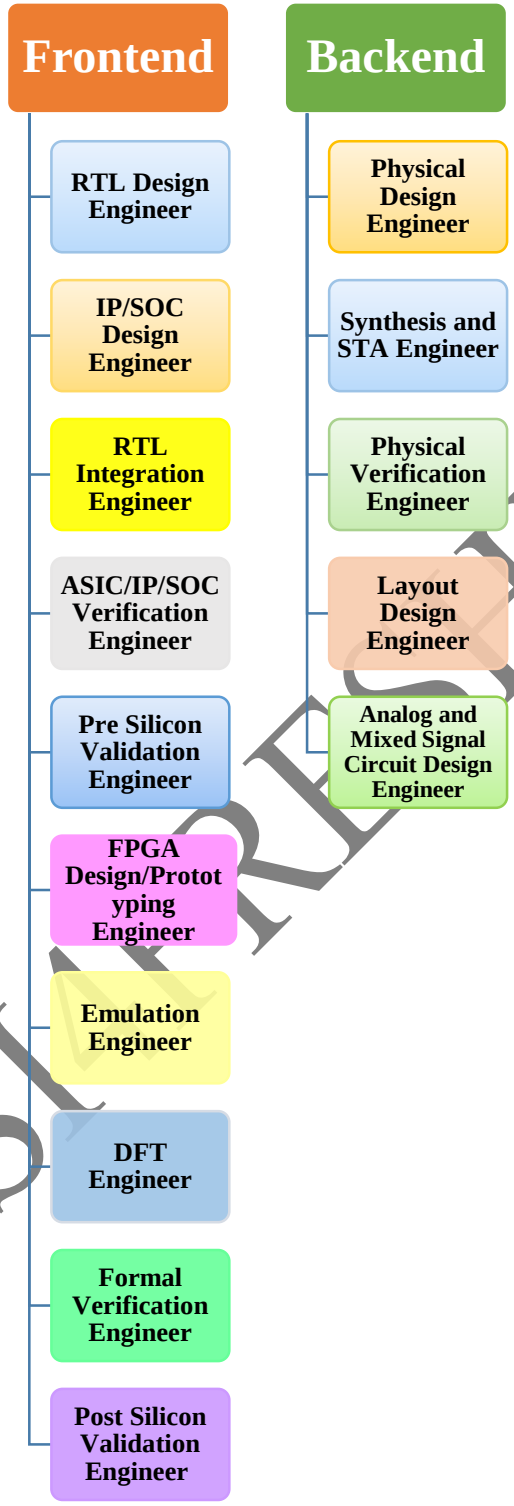
- If you are a fresher and want to start your career in VLSI and don't know from where you have to start the preparation then follow this document it will help you to understand about VLSI domain.

First, you should know the types of VLSI or Semiconductors companies.



There are many job profiles in VLSI Companies.

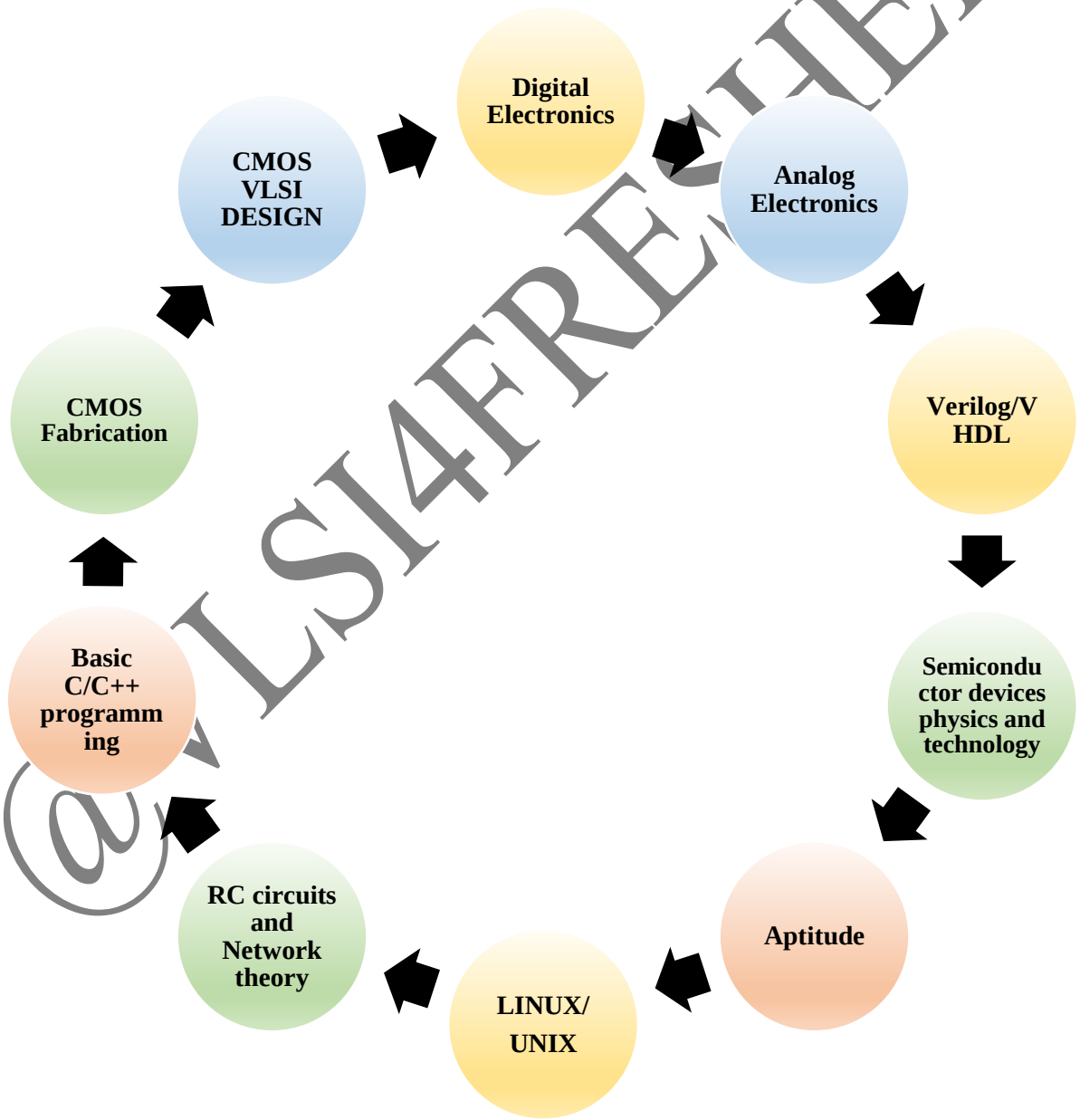
- VLSI is mainly divided into two parts:
- There are specific job roles in front-end design and backend design listed below.
- All stages from logic synthesis to GDS2 are considered as backend end design.



What are the skills required for each profile.

- First study all fundamentals subject which is part your academic course. Then move to VLSI profile specific topics.
- There are different topics required to learn for different profiles.

Fundamentals topics which is essential for every VLSI profile.



For RTL Design and Verification Profile

- Good understanding of digital design along with some advanced topics like metastablity, CDC basics and STA.
- Knowledge of ASIC design Flow and FPGA flow.
- Good knowledge of Verilog/VHDL.
- Good knowledge of computer architecture .
- Understanding of System Verilog basics.
- Understanding on protocols like APB,UART ,I2C SPI,USB and AHB.
- Knowledge on building verification environment using methodologies like UVM.
- Basics knowledge of C/C++ and OOPs.
- Hands on experience on UNIX

For DFT Profile

- Good understanding of digital design along with some advanced topics like metastablity, CDC basics and STA.
- Knowledge of ASIC design Flow.
- Good knowledge of Verilog/VHDL.
- Knowledge of scripting language such as TCL and Perl.
- Hands on experience on UNIX.
- Good understanding of CMOS design.
- Knowledge of some basic DFT related topics:
- Fault models, Fault coverage ,Scan chain Insertion ATPG tool, MBIST and boundary scan etc.

For PD/STA/PV profile

- Good understanding of digital design along with some advanced topics like metastablity, CDC basics.
- Knowledge of ASIC design Flow .
- Knowledge of scripting language such as TCL and Perl.
- Good understanding of CMOS vlsi design.
- Basic understanding of Diode, BJT, MOSFET amplifiers, Op-Amp, comparators, Oscillators(VCO), PLL.
- Hands on experience on UNIX.
- Knowledge of physical design flow: Floor planning , Placement, CTS, routing ,timing and signoff.
- Knowledge of static timing analysis(STA): Timing Checks ,timing models, timing paths, setup and hold check, delay concepts, input/outputs files and SI analysis.
- Basic Knowledge of DRC checks, LVS checks, antenna checks, parasitic extraction and IR drop.

For Analog design and layout profile

- Good understanding of digital design and analog design.
- Knowledge of ASIC design Flow .
- Knowledge of scripting language such as TCL and Perl.
- Good understanding of CMOS design.
- Good understanding of IC fabrication steps.
- Good understanding of Diode, BJT, MOSFET amplifiers, Op-Amp, comparators, Oscillators(VCO), PLL.
- Good understanding of RC circuits and voltage and current reference circuits.
- Hands on experience on UNIX.
- Basic Knowledge of static timing analysis(STA).
- Knowledge of layout design and physical verification tools.
- Basic Knowledge of DRC checks, LVS checks, antenna checks, parasitic extraction and IR drop.

For Memory Design profile

- Good understanding of digital design along with some advanced topics like metastablity, CDC basics.
- Knowledge of ASIC design Flow .
- Knowledge of scripting language such as TCL and Perl.
- Good understanding of CMOS vlsi design.
- Basic understanding of Diode, BJT, MOSFET, Op-Amp.
- Hands on experience on UNIX.
- Knowledge of static timing analysis(STA).
- Knowledge of memory basics
- Good understanding of SRAM and DRAM memory read/write operation and FIFO depth.
- Basic Knowledge of DRC checks, LVS checks, parasitic extraction.

Study reference for Digital Design

- Book: Digital design by M.Morris mano
- Book: Digital design by John F. wakerly
- Link: https://nptel.ac.in/courses/106105185
- Link: https://nptel.ac.in/courses/117108040
- Link: https://nptel.ac.in/courses/117106086
- Link: https://onlinecourses.nptel.ac.in/noc20_ee05/preview
- Link: https://onlinecourses.nptel.ac.in/noc21_ee39/preview

Study reference for Digital IC Design:

- Book: Digital Integrated Circuits 2nd Edition by Jan Rabaey
- Link: https://onlinecourses.nptel.ac.in/noc20_ee05/preview
- Link: https://nptel.ac.in/courses/108106158

Study reference for CMOS VLSI Design

- Book: CMOS VLSI Design by Neil H. E. Weste David Money Harris
- Book: CMOS digital integrated circuits analysis and design by s.m kang and y.leblebici
- Book: Low-Power VLSI Circuits and Systems by Ajit Pal
- Book: CMOS Analog Circuit Design 2nd Edition by Phillip E. Allen
- Book: Design of Analog CMOS Integrated Circuits by Behzad Razavi
- Link: **https://nptel.ac.in/courses/108107129**
- For CMOS fabrication: **https://archive.nptel.ac.in/courses/117/106/117106093/**

Study reference for Analog design

- Book: Design of Analog CMOS Integrated Circuits by Behzad Razavi
- Book: Analysis and Design of Analog Integrated Circuits by PAUL R. GRAY & MEYER.
- Book: Fundamentals of electric circuits by alexander sadiku
- Book: Microelectronic circuits by sedra and smith

- Link: https://www.youtube.com/playlist?list=PL6qRG5-NfbLvagdQOwShX9FMrzb5hSvrq
- Link: https://www.youtube.com/playlist?list=PL6qRG5-NfbLvCFCeCDwLWrIoeOrQxP9ZE
- Link: https://www.youtube.com/playlist?list=PLm2lpI_krGU7w5rfCdD_tEd4ttUBAtRkG
- Link: https://www.youtube.com/playlist?list=PLO4mxQzfcml_56XSGcA8ULOv7qEtZd0Hy
- Link: https://nptel.ac.in/courses/117106108
- Link: https://nptel.ac.in/courses/108106084
- Link: https://nptel.ac.in/courses/117106030
- Link: https://archive.nptel.ac.in/courses/117/101/117101105/

Study reference for Verilog and System Verilog

- Book: Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar
- Book : A Verilog HDL primer by J.Bhasker
- Book : System Verilog for verification by chris spear
- Book: Application-Specific Integrated Circuits by John Smith
- Book: System Verilog assertion handbook by Ajeetha Kumari, Ben Cohen, and Srinivasan Venkataramanan
- The UVM Primer: An Introduction to the Universal Verification Methodology by Ray Salemi

- System Verilog 3.1a Language Reference Manual from accellera
- System Verilog for design Book by Stuart Sutherland , Simon Davidmann and Peter Flake
- Universal Verification Methodology (UVM) 1.2 Class Reference from accellera
- Universal Verification Methodology (UVM) 1.2 User's Guide from accellera
- UVM cookbook from verification academy.
- Verilog Lecture Link: https://nptel.ac.in/courses/106105165
- Log In here to learn UVM: https://verificationacademy.com/
- Link: https://verificationguide.com/
- Link: https://www.youtube.com/playlist?list=PLBIILfL2t1lnvzw7vF0arlvu36Wj4--D7
- Link: http://www.sunburst-design.com/papers/

Study reference for Design for Testability (DFT)

- Book: Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits by Michael Lee Bushnell and Vishwani Agrawal
- Book: VLSI TEST PRINCIPLES AND ARCHITECTURES DESIGN FOR TESTABILITY by Laung-Terng Wang, Cheng-Wen Wu ,Xiaoqing Wen
- Link: https://nptel.ac.in/courses/106103016
- Link: https://nptel.ac.in/courses/106103116
- Link: https://nptel.ac.in/courses/117106092
- Link: https://archive.nptel.ac.in/courses/117/105/117105137/

- Link: https://archive.nptel.ac.in/courses/117/103/117103125/
- Link for DFT (refer Lecture 47 to Lecture 56) https://archive.nptel.ac.in/courses/106/105/106105161/

Study reference for Physical Design (PD)/STA/Synthesis

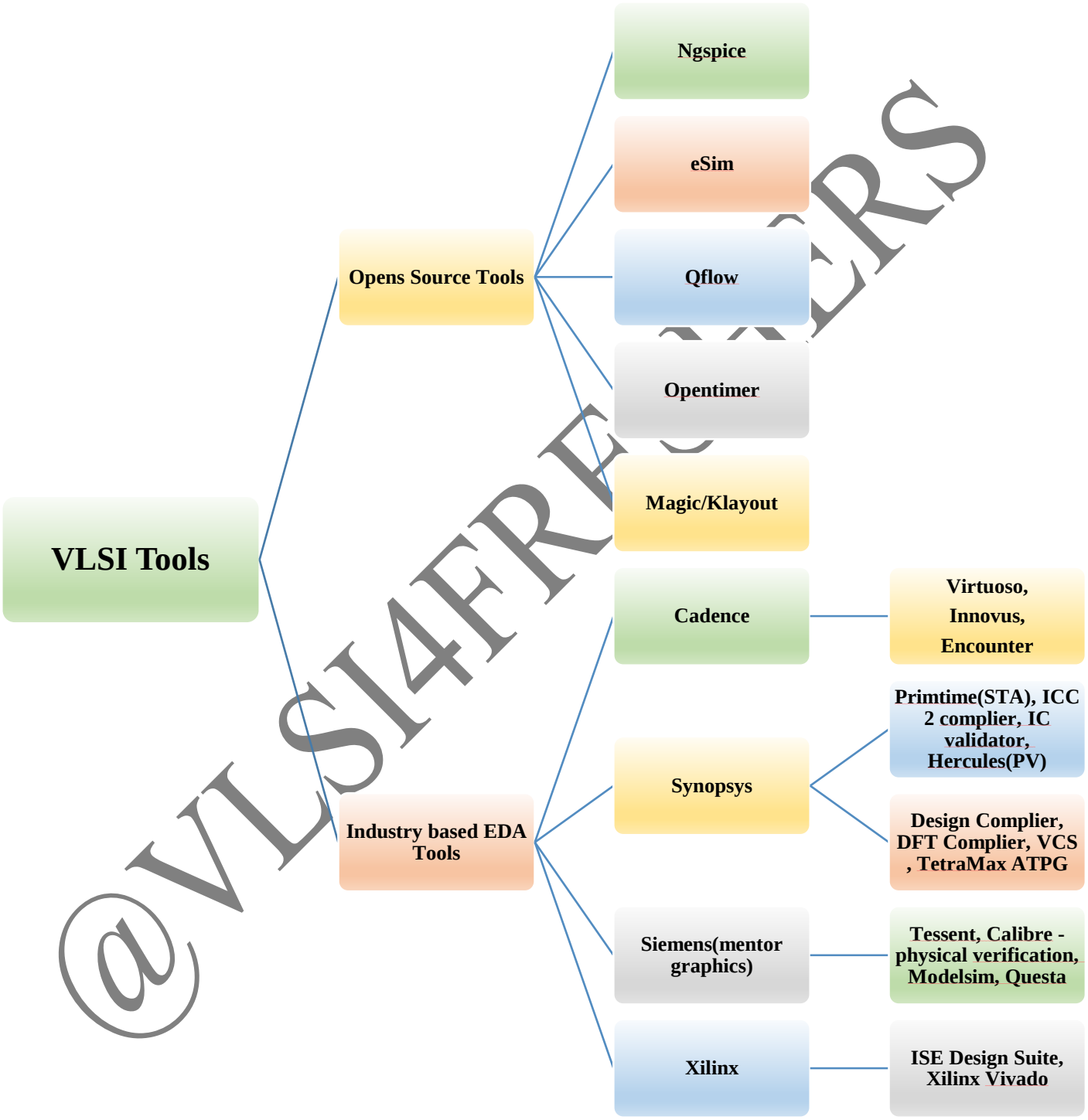
- Book for STA: Static Timing Analysis for Nanometer Designs: A Practical Approach by Jayaram Bhasker and Rakesh Chadha
- Book: Advanced ASIC Chip Synthesis Using Synopsys Tools by Himanshu Bhatnagar
- Book: Constraining Designs for Synthesis and Timing Analysis: A Practical Guide to Synopsys Design by Sridhar Gangadharan & Sanjay Churiwala
- Book: Physical design essentials: an ASIC design implementation perspective by Khosrow Golshan
- Book: Algorithms for VLSI Physical Design Automation by Sherwani, N. A.
- **Link: http://www.vlsi-expert.com/p/static-timing-analysis.html**
- **Link: https://archive.nptel.ac.in/courses/106/105/106105161/**
- **Link: https://www.udemy.com/course/vlsi-academy-sta-checks/**
- **Link: https://www.udemy.com/course/vlsi-academy-physical-design-flow/**
- **Link: https://www.youtube.com/c/Vlsi-expert/playlists**
- **Link: https://www.vlsisystemdesign.com/inception-content-vsd/**

Study reference for TCL/Perl

- Book: Using Tcl With Synopsys Tools by Synopsys

- Book: Tcl and the Tk Toolkit Book by John Ousterhout and Ken Jones
- Book: Tcl/Tk in a Nutshell Book by Jeff Tranter and Paul Raines
- Link: https://www.youtube.com/playlist?list=PLtChGkQ0aIK-h8WHzPYHu9hwedupUM1Hm
- Link: https://archive.org/details/ebookpdfteachyourselfperlin21days/page/n513/mode/2up
- Link: https://archive.nptel.ac.in/courses/117/106/117106113/
- Link: https://www.perltutorial.org/
- Link: https://www.ee.columbia.edu/~shane/projects/sensornet/part1.pdf
- Link: https://www.tutorialspoint.com/tcl-tk/index.htm
- Link: https://www.tcl.tk/man/tcl8.5/tutorial/tcltutorial.html

VLSI EDA Tools/Softwares



Tool Description and installation guidelines

- Refer this video to install: https://www.udemy.com/course/vsd-a-complete-guide-to-install-open-source-eda-tools/
- Ngspice – General purpose circuit simulation program for non-linear and linear analyses
- Magic – VLSI Layout editor, extraction and DRC tool
- Opentimer – Open-source high performance timing analysis tool
- eSim – Complex Circuit design, SPICE simulation, analysis and PCB design
- Qflow – Tool chain (like Yosys, Graywolf) for complete RTL2GDS flow
- Cadence: Virtuoso, Innovus, encounter,
- Siemens(mentor graphics): Tessent, Calibre-physical verification, Modelsim, Questa
- Synopsys: Primtime(STA), ICC 2 Complier, IC validator, Hercules(PV)
- Design complier, DFT complier, VCS , TetraMax ATPG,
- Xilinx: ISE Design Suite, Xilinx Vivado.
- Simulation tools: LT Spice, Pspice, Multisim.
- For Verilog/SV Coding practice: https://www.edaplayground.com/
- http://makerchip.com/
- Download Model Sim from this link https://eda.sw.siemens.com/en-US/modelsim-student-edition-unavailable/
- https://fossee.in/
- https://riscv.org/
- https://opencores.org/projects

- https://github.com/efabless/openlane
- https://github.com/OpenTimer/OpenTimer
- For Glade Layout Design Tool: https://peardrop.co.uk/

VLSI Interview Topics CheatSheet - By vlsi4freshers

Link: https://whimsical.com/vlsi-interview-topics-cheatsheet-by-vlsi4freshers-CmqnfqJ7gCHAWEHmAvxAJH