ECE5026	SYSTEM DESIGN WITH FPGA	L	T	P	J	C
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Prerequisite	**Nil**			**v 1.0**		

Course Objective:

This course is aimed to

1. review the fundamental concepts of C language.
2. expound the architecture of NIOS II soft core processor and the various peripheral interfaces used for system design.
3. implement the interconnect fabrics for the system and to design the system using NIOS II Soft core Processor.

Expected Course Outcome:

After completion of the course the student will be able to:

1. Understand the concepts of C language.
2. Understand the NIOS II soft core processor architecture.
3. Interpret the usage of various peripheral interfaces for system design.
4. Develop system by choosing suitable interconnect fabrics.
5. Design the system using NIOS II soft core processor.
6. Model the system by using IP block.
7. Design and develop embedded synthesis using FPGA.

Student Learning Outcomes (SLO):	**5,12,17**

Module:1	**Basic C Concepts**	**5hours**

Loops, Arrays, structures, pointers, functions, linked list

Module:2	**Soft Core Processor**	**5hours**

Nios II Processor – Configurability Features – Processor Architecture-Instruction set

Module:3	**Peripheral Interfaces**	**5hours**

LCD, PS2, RS232, SDRAM, SRAM Controller, VGA, Audio and Video,PIO, External Bus bridge and IrDA

Module:4	**NIOS II programming for peripheral Interfaces**	**4hours**

LCD, PS2, RS232, SDRAM, SRAM, VGA, Audio, IrDA.

Module:5	**Interconnect Fabrics**	**3hours**

Avalon Switch Fabric Interconnect - Implementation and Functions- Integrated Design Environment

Module:6	**System Design**	**4hours**

Traffic light Controller, Real Time Clock - Interfacing using FPGA: VGA, , LCD, Camera

Module:7	**IP Block Implementation**	**2hours**

Edge detection algorithm, Colour and Brightness Enhancement algorithm

Module:8	**Contemporary issues:**	**2hours**
	Total Lecture hours:	**30hours**

Text Book(s)	
1.	ZainalabedinNavabi, “Embedded Core Design with FPGAs”, TATA McGraw Hill Ltd, 2011.
2.	Paul J. Deitel, Harvey M. Deitel, “C: How to Program”, Pearson Education, 2012
Reference Books	
1	NIOS II Handbook, 2014.
2	T.N.Padmanabhan,ThirupuraSundari, “Design Through VerilogHDL”,Wiley Student Edition, 2010.

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

TypicalProjects

1. Implementation of edge detection algorithm
2. Implementation of self-guided vehicle.
3. Implementation of smart home system
4. Implementation of Health Monitoring System
5. Implementation of Music Synthesizer.

Mode of Evaluation:Review I, II and III

Recommended by Board of Studies	13-12-2015	
Approved by Academic Council	No. 40	18-03-2016