

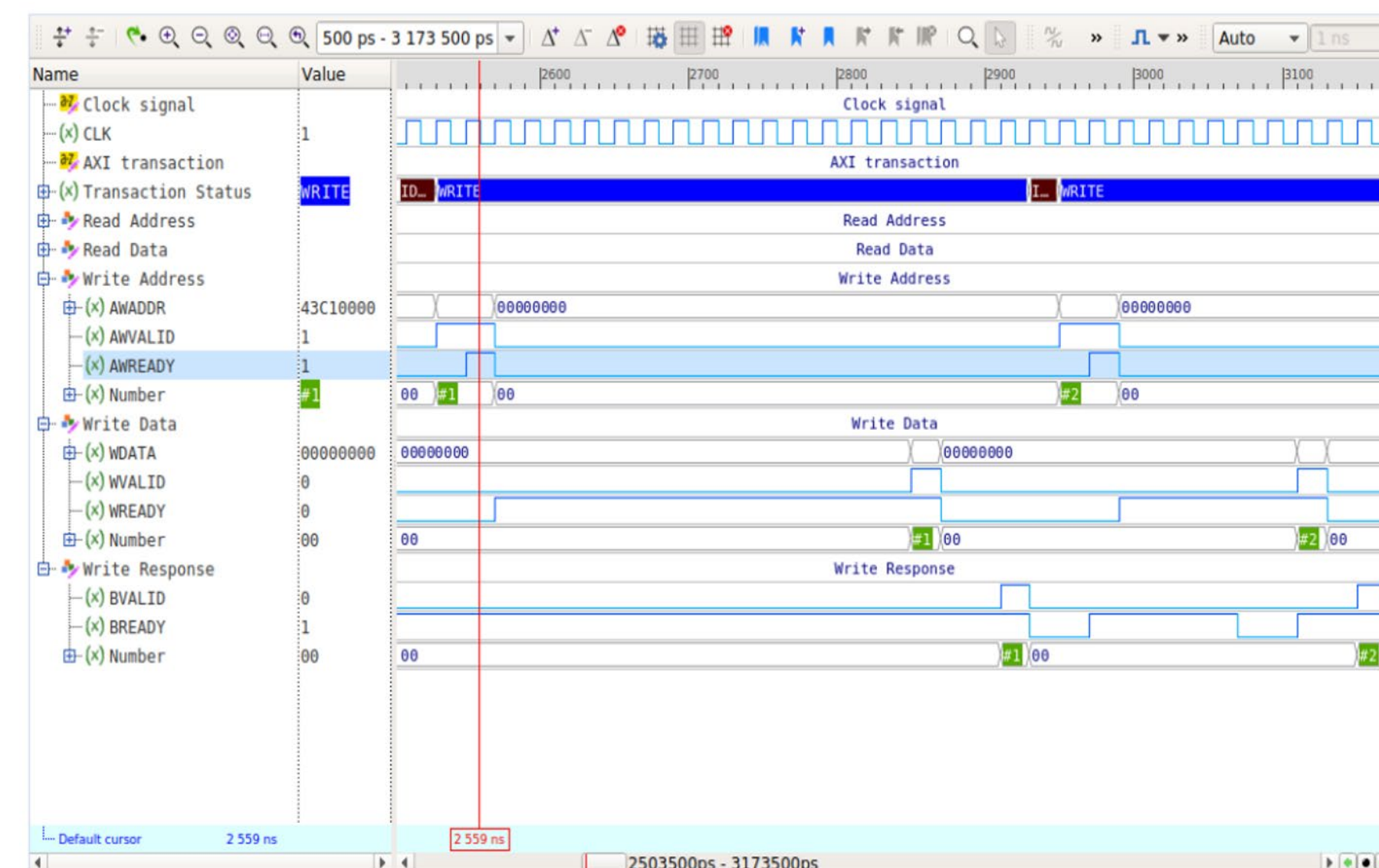
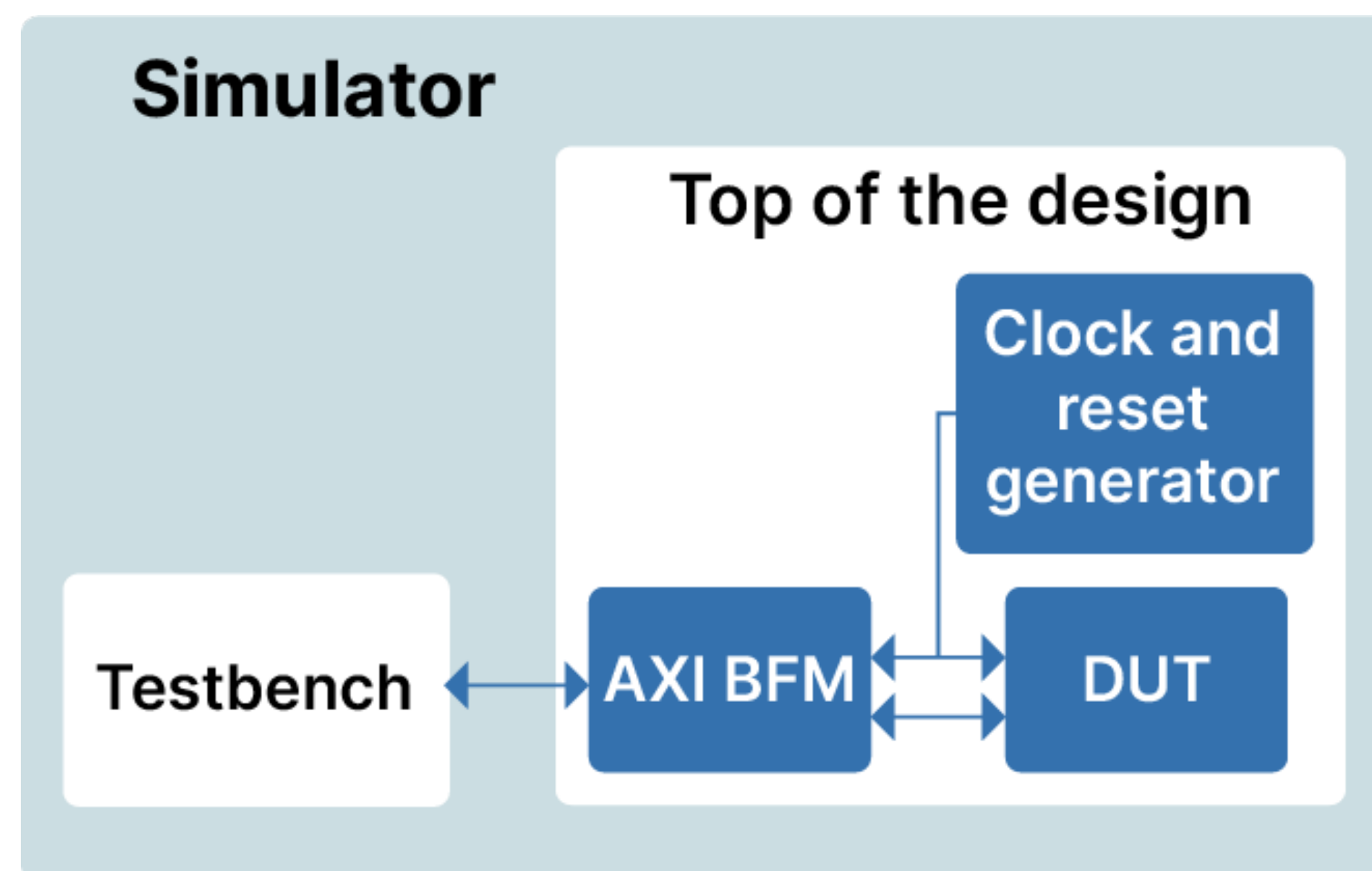
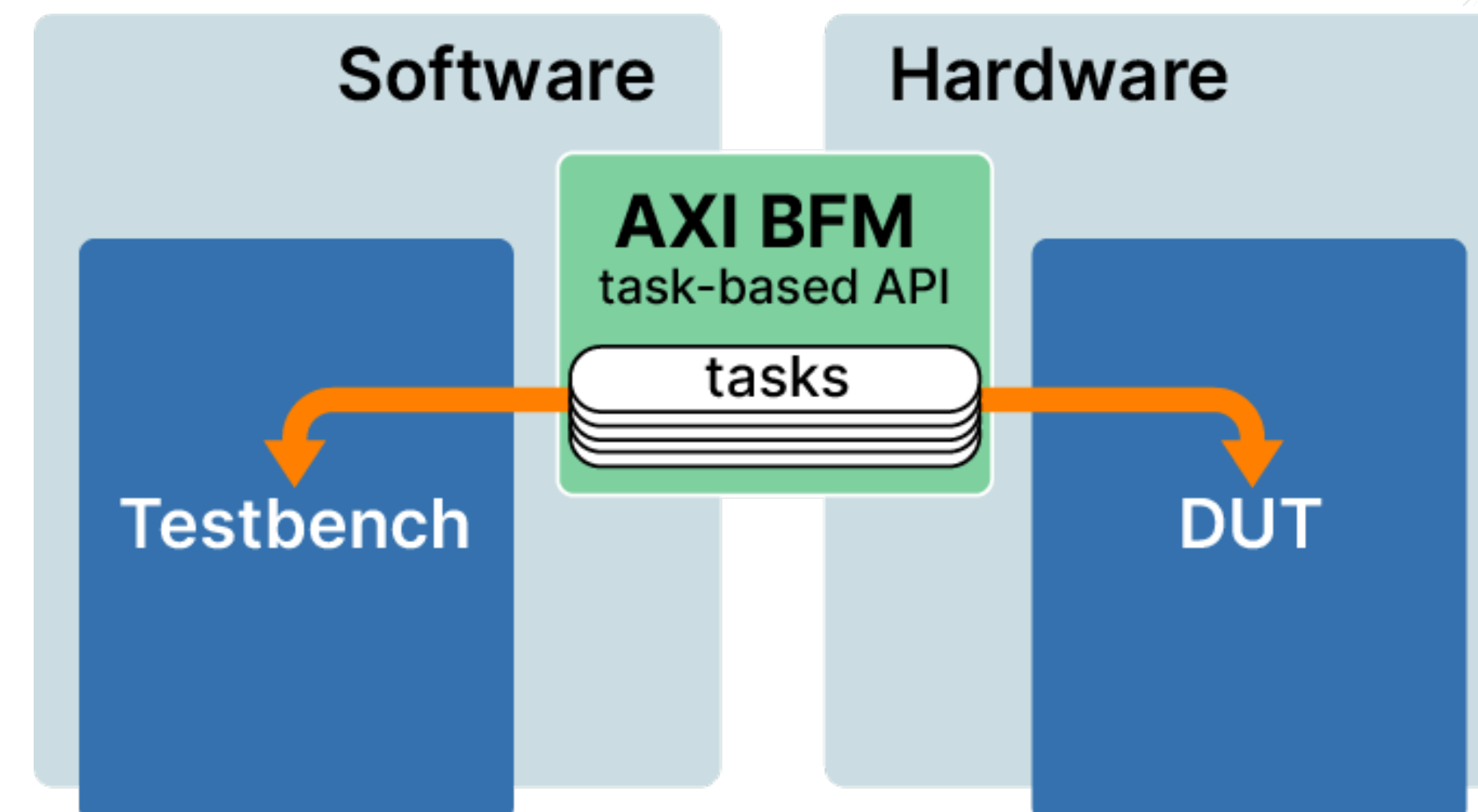
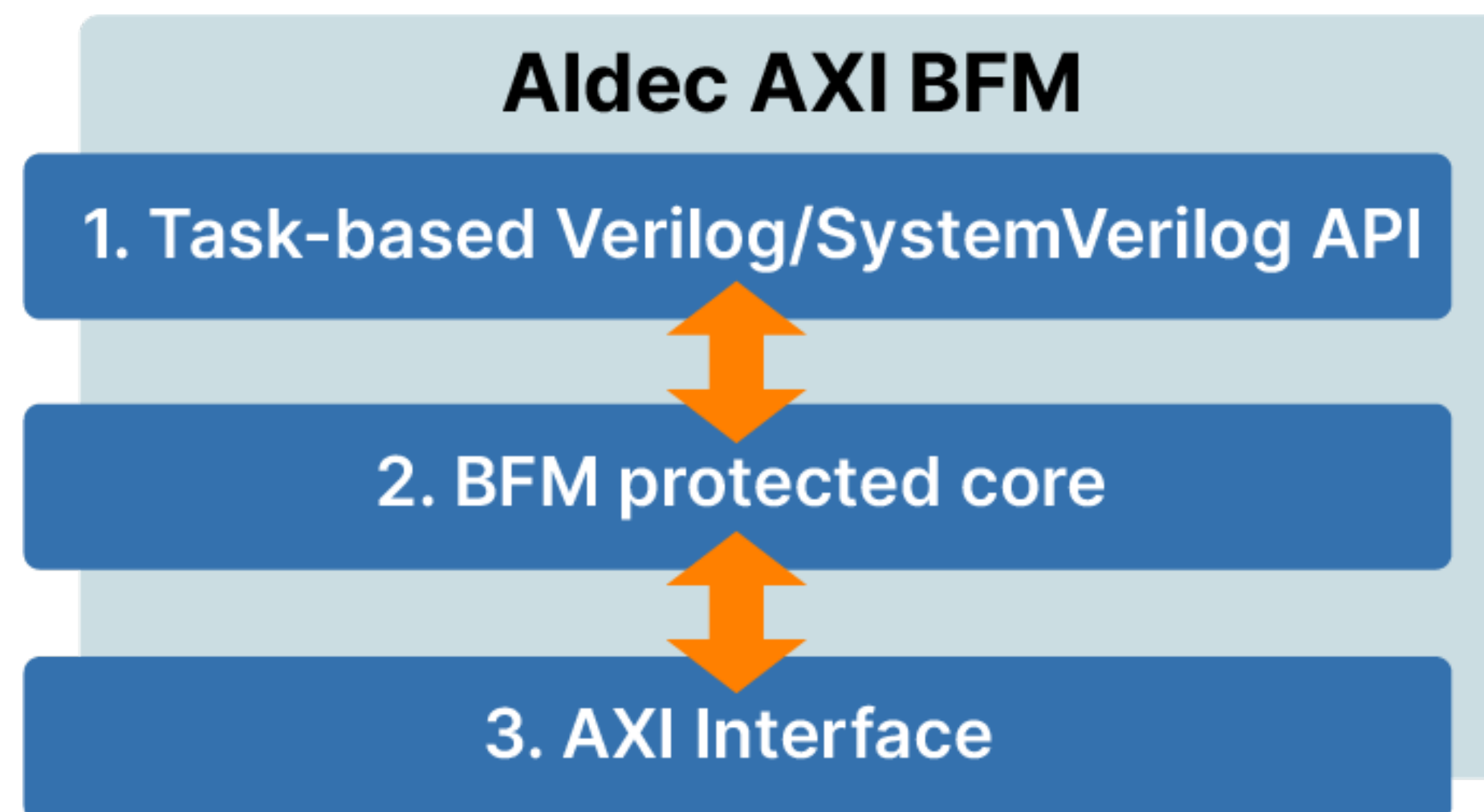


**BFM AMBA AXI**

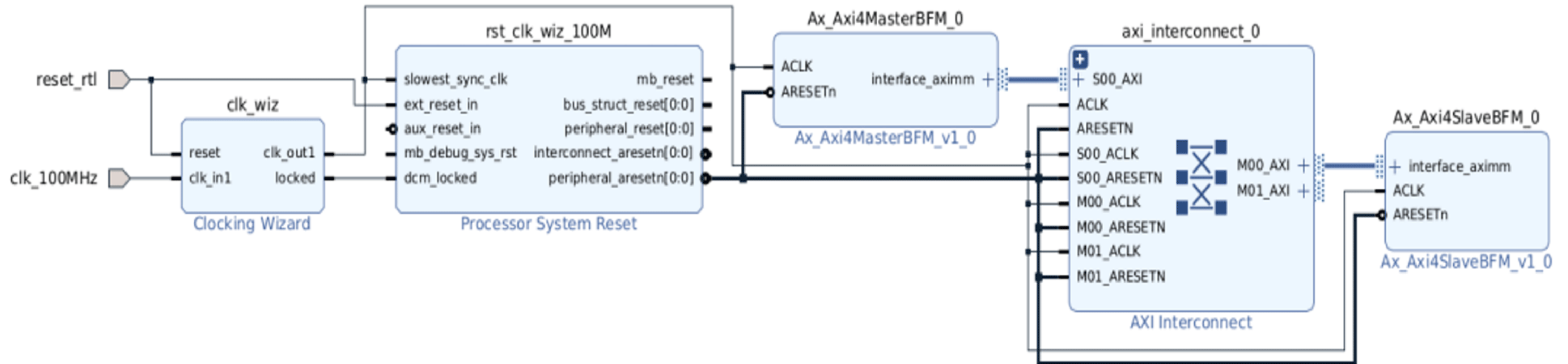




# The Aldec AXI BFM standard usage



# Supported Vendors



Aldec BFM in Vivado





# Supported Vendors

The screenshot displays the Quartus Prime Design Software interface. The IP Catalog on the left lists various components, including the ALDEC AXI4 Master BFM and ALDEC AXI4 Slave BFM. The System View in the center shows a hierarchical structure of components, including the Clock Bridge Intel FPGA IP, Reset Bridge Intel FPGA IP, Clock Source BFM Intel FPGA IP, Reset Source BFM Intel FPGA IP, and the ALDEC AXI4 Master BFM (New BFM) and ALDEC AXI4 Slave BFM (New BFM). The Project Settings on the right show the device family, device, and board, along with the interfaces and parameters for the selected component.

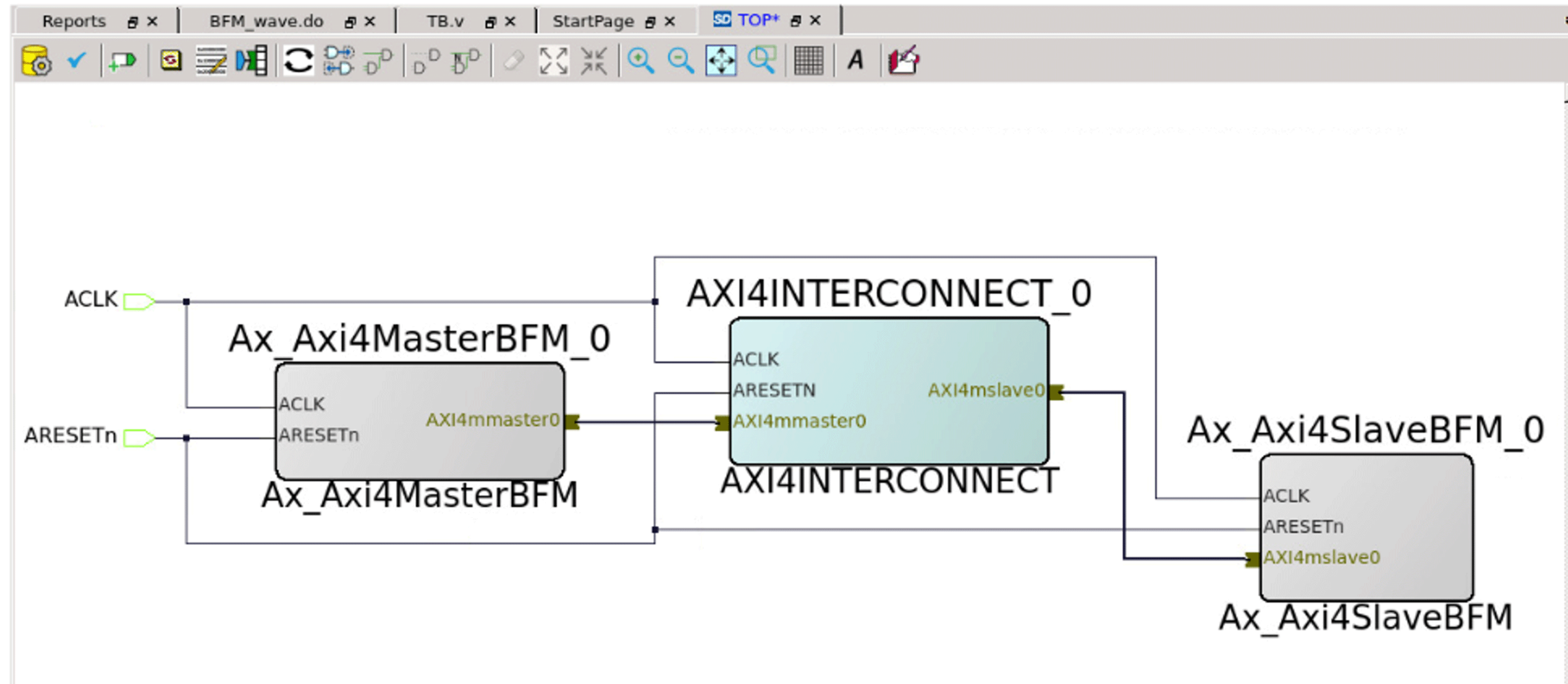
Component	clock_in	IP	Ip/demo_BFM/demo_BFM_c
Project Settings	device family	device	board
Interfaces	in_clk	clock_rate	clock_rate
Legend	missing	different	Sync All
Interface: in_clk	Parameter: clock_rate	Component Instantiation Value	IP File Value
		50000000	50000000



## Aldec BFM in Quartus Prime Design

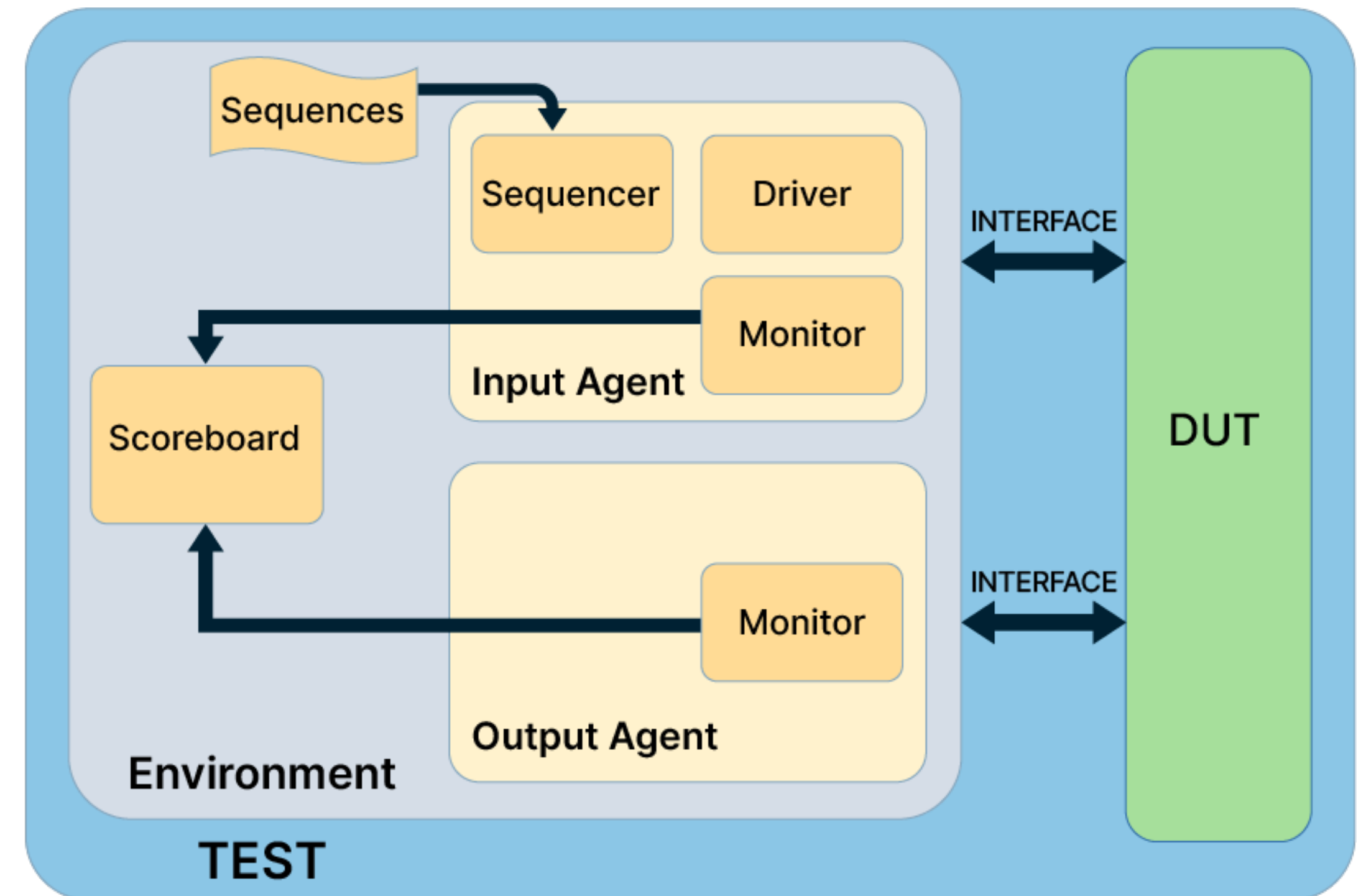
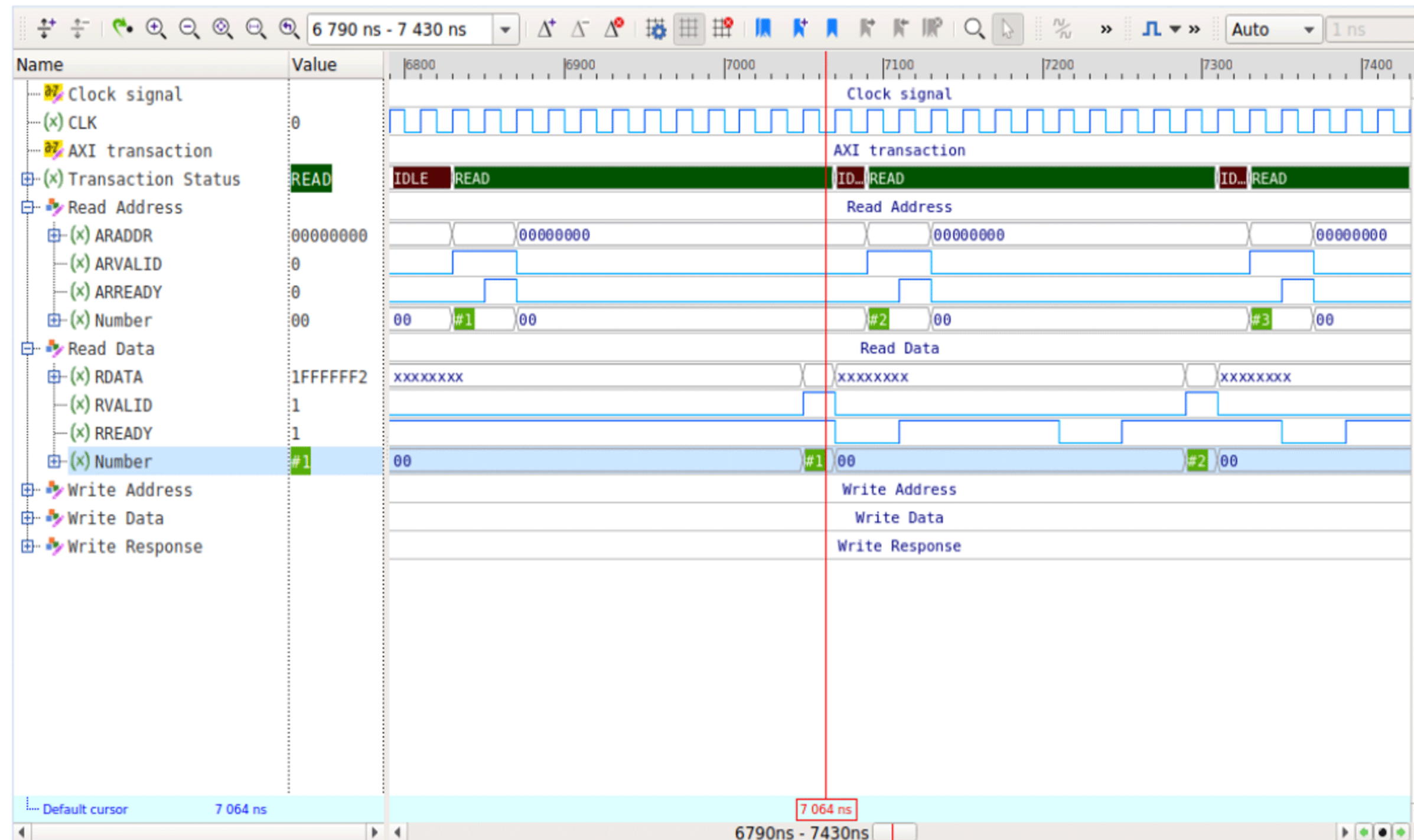


# Supported Vendors



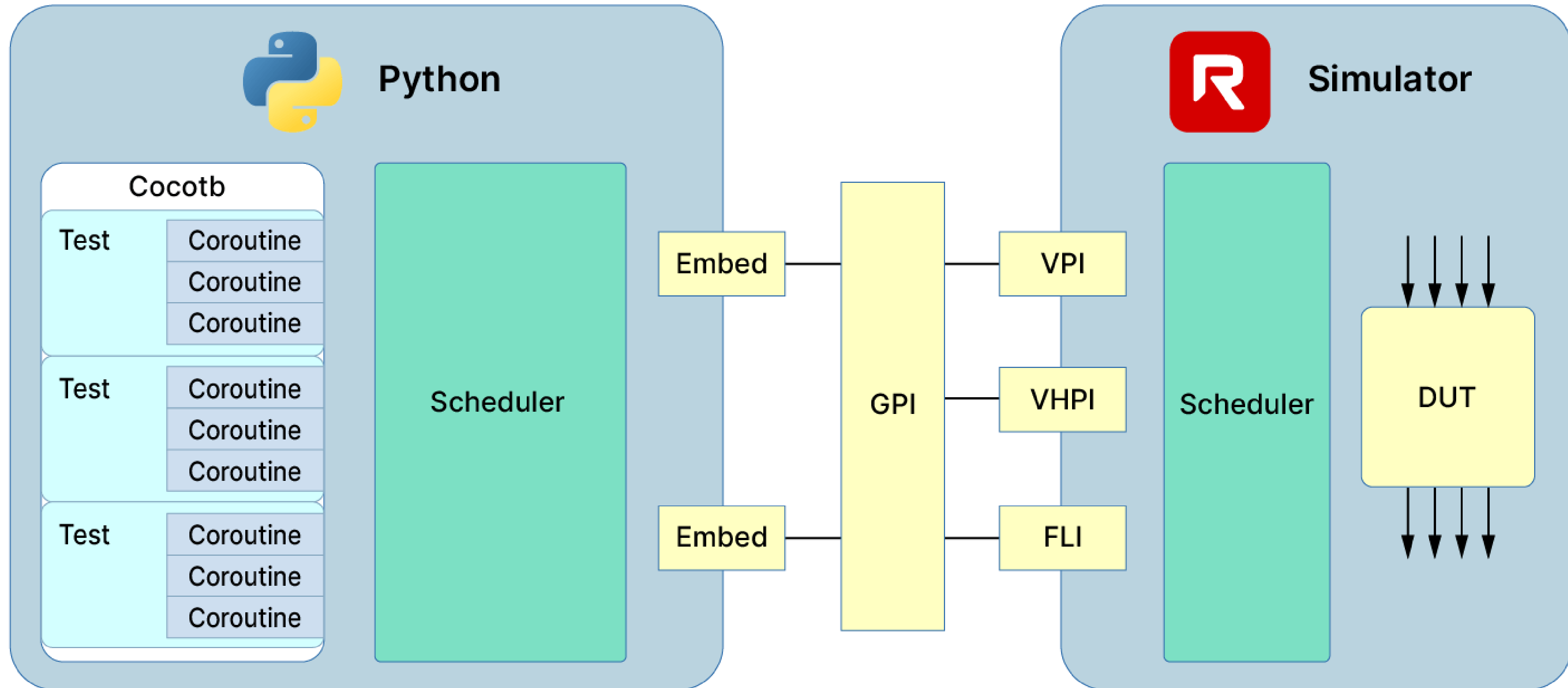
## Aldec BFM in Libero\_SoC

# BFM as UVM\_Driver

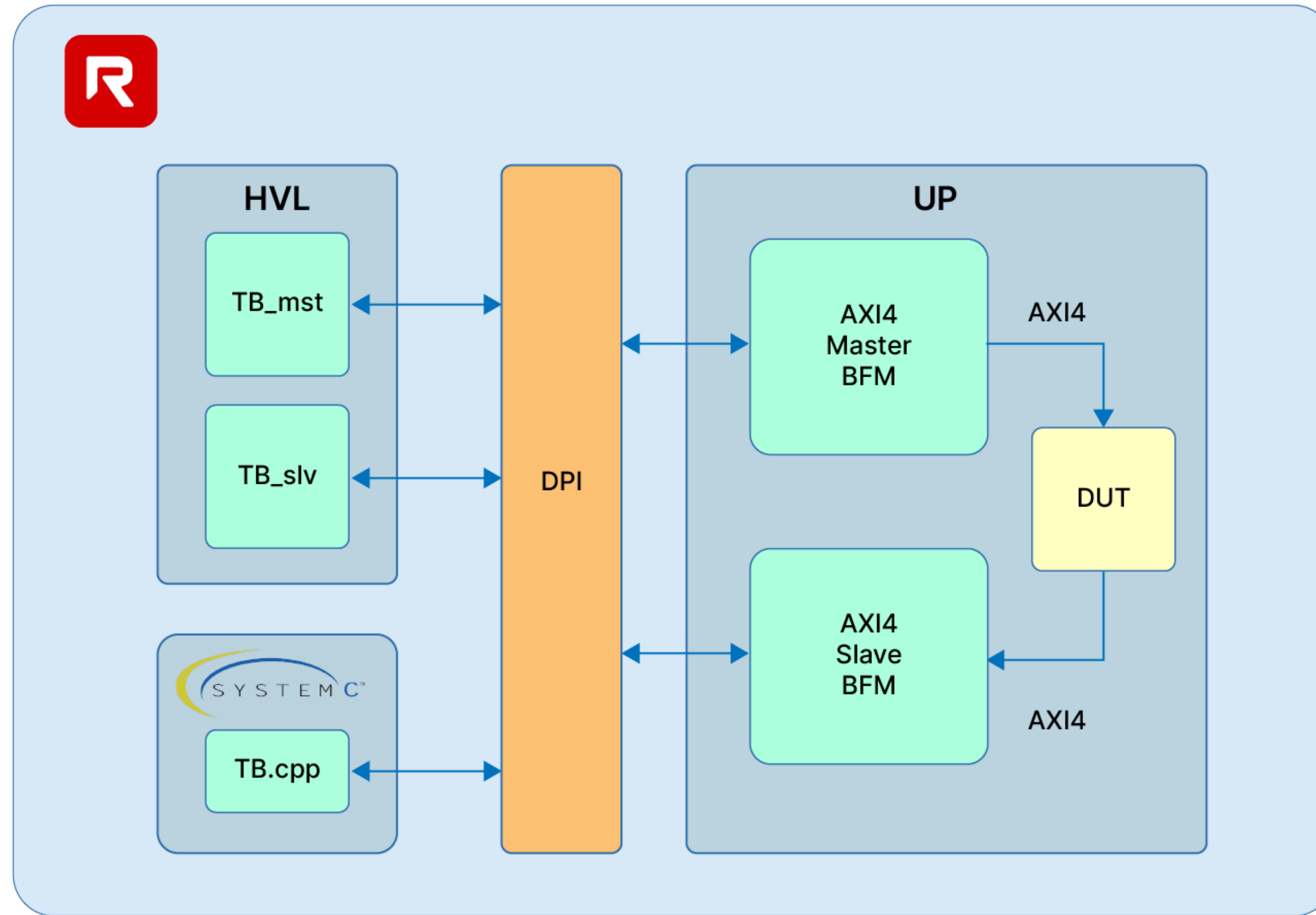




# Cocotb with BFM in AXI simulation

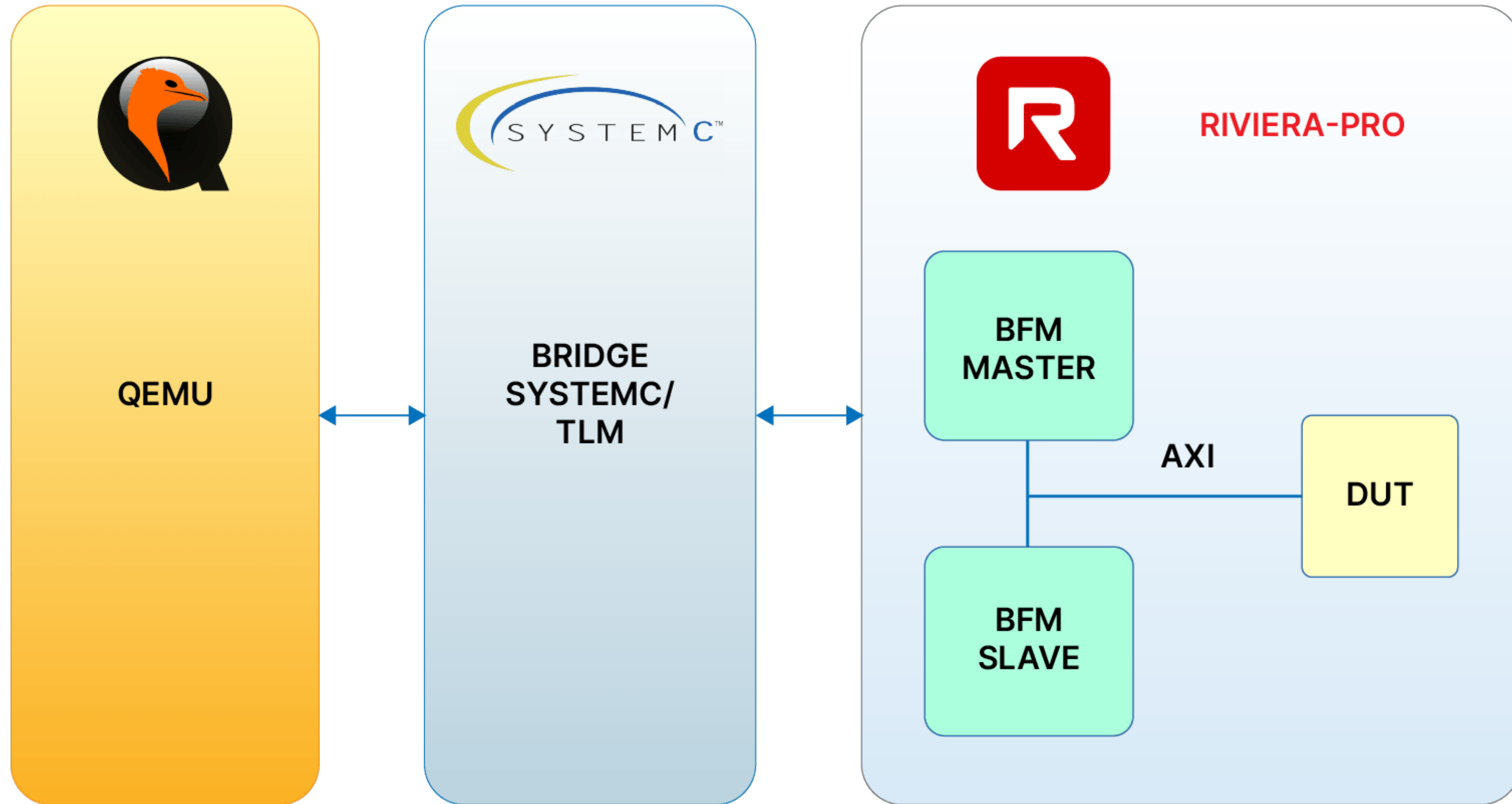


# Using BFM through DPI in simulation



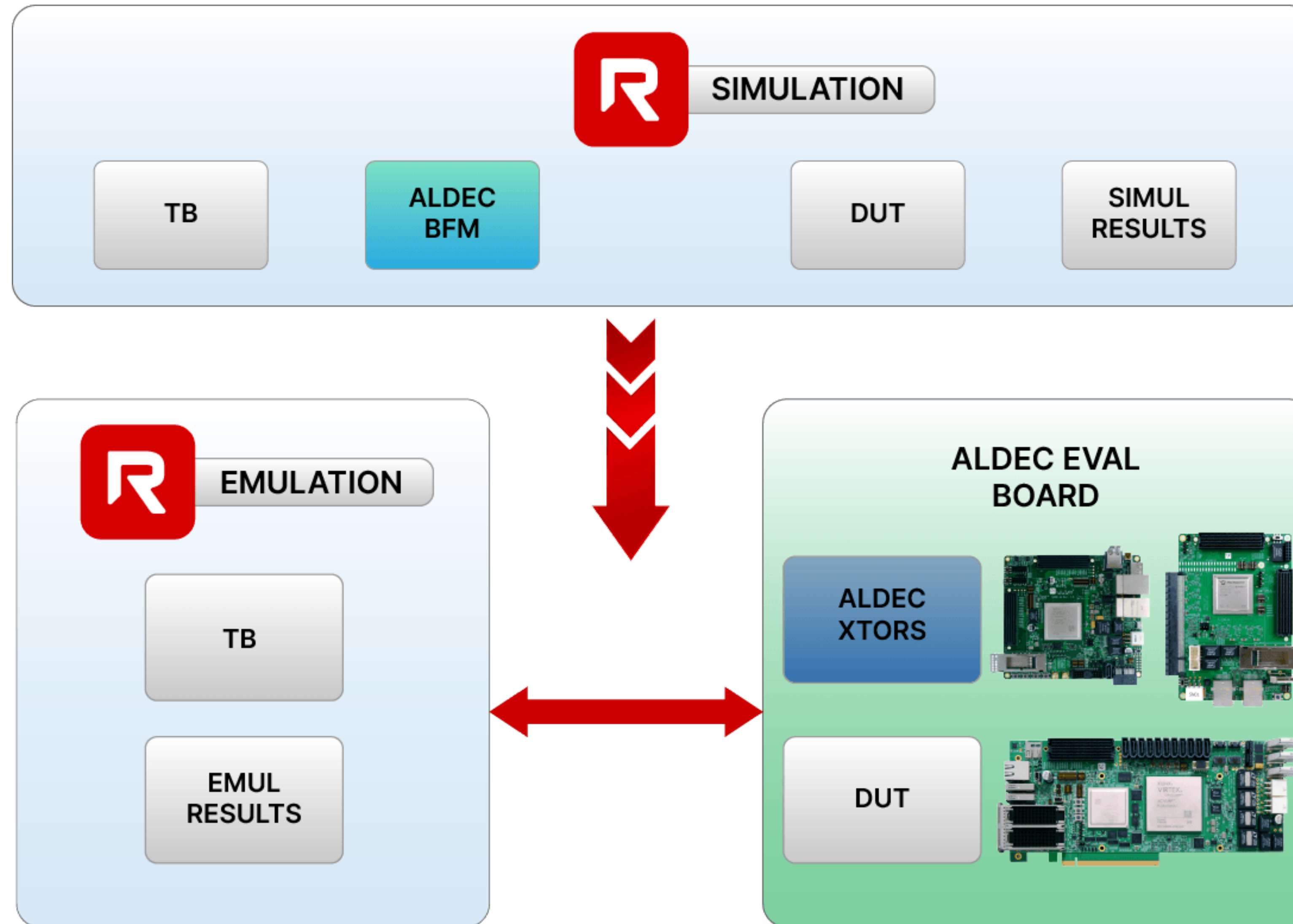


# Using BFM with Qemu





# HW verification base on XTOR Emulation







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