A 5-BIT, 0.08mm^{2}Area Flash Analog to Digital Converter Implemented on Cadence Virtuoso 180nm

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Abstract:

A 5-bit flash analog to digital converter (ADC) is implemented on 180nm CMOS technology. The ADC is operates at 1.2v and employs best comparator to improve performance of ADC. In this paper implemented two types of comparators, latch type comparator and proposed comparator. Dual input single output differential amplifier as latch stage has been used in proposed comparator. The simulation result of ADC is operating at 5GHz sampling frequency and its delay and power dissipation is 419.9ns and 15.2 mw respectively. At 5GHz the average power dissipation of the encoder circuit is 58.5uw and delay 1.29 ns and proposed comparator delay is 1.1ns.

Keywords: Analog to digital converter, latch type comparator, encoder, proposed comparator.

I. INTRODUCTION

The signals in the nature are analog form, such as audio, video and voice etc. in order to convert analog signal to digital signal, we need analog to digital converter. Analog to digital converters are very important in many advanced systems that needs the integration of analog signals with digital systems. In the past decade the researchers are proposed many analog to digital converters using different techniques and power optimization methods to reach low power systems.

In the past years, ADC architectures such as, successive approximation (SAR) and $\Sigma\Delta$modulation have been implemented [1], are used for highly resolution digital conversion because of their compatibility with the CMOS technology. In flash ADC with latch type comparators switched at a time, this may affect the input analog signal and reference voltage of the converter [2].The location of the architectures may alter in some architecture amplifier in each stage may be degraded. So we can say that the flash analog to digital converter is the fastest ADC in comparison with other ADC architectures. In ADCs power dissipation and delay is most important concern used for portable devices used batteries. It is most important to find the trends in ADC power efficiency during the past years [3].

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Power dissipation and speed is most important in ADCs used for portable devices [4].

In this paper implemented latch type comparator and proposed comparator using dual input single output differential latch stage. Compared both the results of comparators. However in this paper to reaches ADC speed and reduces power dissipation implemented encoder with less power dissipation.

This paper described as follows. Section I discussed introduction. Section II can be follows ADC architecture implementation. Section III follows by results and discussion. Conclusion will be discussed in section IV.

II. FLASH ADC ARCHITECTURE

Fig 1 shows the 5 bit flash ADC, it consist resistor ladder, comparators and encoder circuit. For N bit flash ADC required 2^N resistors, $2^N - 1$ comparators and encoder. Flash ADC is faster ADC compared to other ADC. It's used for high frequency applications.

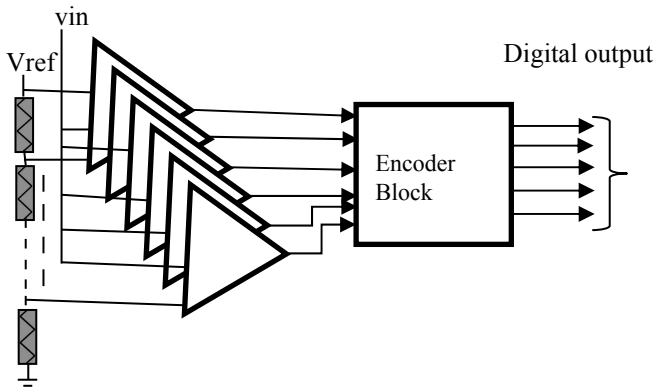


Fig 1 Flash ADC Architecture block diagram

A. Latched type Comparator

In flash ADC comparators are used to find weather a signal is greater than or less than reference voltage. Latched comparator constructed by using preamplifier, latch and

buffer. Comparator. Condition to give digital output of latch comparator as shown below.

$V_+ < V_-$ then Vout = logic 0,
$V_+ > V_-$ then Vout = logic 1.

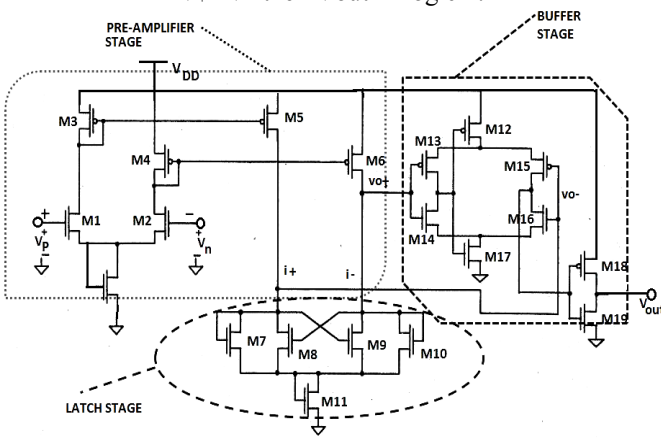


Fig 2 latched type comparator schematic

Fig 2 shows latched type comparator schematic. It has three stages: latch stage, output buffer stage, and input preamplifier stage. It has self-biased differential amplifier followed by an inverter which gives the digital output. The preamplifier stage is a differential amplifier with active load [5]. In this comparator improved the comparator sensitivity by using preamplifier stage and isolates the input of the comparator from switching noise coming from the positive feedback stage [5]. It also reduce reduced input latch offset voltage. The sizes of M1 & M2 are set by considering the differential amplifier transconductance and input capacitance. The transconductance sets the gain of the stage, while the size of M1 & M2 deference the input capacitance of the capacitor [5]. Here $g_{m1} = g_{m2}$.

The positive feedback latch stage is used to determine which of the signals is large and extremely their difference [6]. It takes the positive feedback from the cross gate connection of transistor M8 & M9. Let's take i+ >> i- so that transistor M7 & M9 are ON and M8 & M10 are OFF. The amplifier is basically differential amplifier with active loads [5].the positive feedback latch is used to find out which input signal is large [6].

B. Proposed comparator

In the proposed comparator the back to back latch is replaced with dual input single output differential amplifier is used. The fig 3 shows the proposed comparator schematic. Differential amplifier has many advantages over the latch; it has high CMMR and high immunity to environmental noise. The property of differential signaling is maximum achievable voltage swings.

During the reset phase i.e CLK=0, transistor M4 and M5 turn on and the node N charges to VDD. And hence M17 , M19 transistors turn on, the node N voltage discharge to GND, then the transistors M14, M15 and differential amplifier PMOS transistors M12, M13 turn on, differential amplifier NMOS transistors M8, M9 and M6, M7 turn off. The out nodes are charges to VDD.

Now the clock is set to high, the node N voltage discharge from VDD to GND. the discharging rate is proportional to the input voltage. At certain node N voltage, transistor pairs invert node N voltage in to regenerated voltage. This voltage turn off M14, M12, M13, and M15 transistors. Eventually transistors M6, M7, M20, M21 turn on. The transistors M6, M7 being on, the differential amplifier pairs generate node N voltage. The output of latch stage converted from differential voltage transmitted node N in to a full scale digital output.

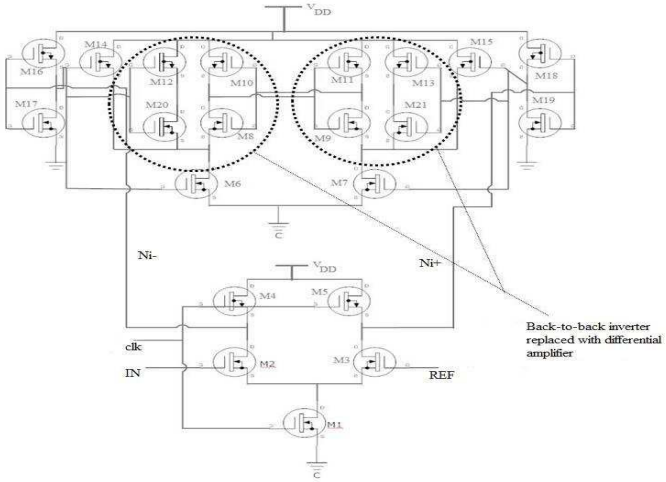


Fig 3 Schematic diagram of proposed comparator

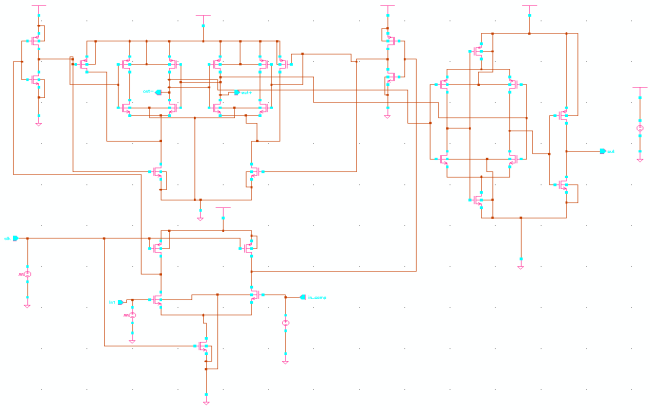


Figure 4 proposed comparator schematic implemented on cadence 180nm

C. Encoder block

Converting thermometer code to binary is main problem in flash ADC [7]. They are many types of thermometer code to binary converters available. In this paper directly converting thermometer code to binary, this method reduces the power dissipation, delay. The tab 1 shows the truth table of thermometer code.

Table 1 Thermometer code truth table

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Thermometer Code
0	0	0	0	0	00000000000000000000000000000000
0	0	0	0	1	00000000000000000000000000000001
0	0	0	1	0	00000000000000000000000000000011
0	0	0	1	1	00000000000000000000000000000111
0	0	1	0	0	00000000000000000000000000001111
0	0	1	0	1	00000000000000000000000000011111
0	0	1	1	0	00000000000000000000000000111111
0	0	1	1	1	00000000000000000000000001111111
0	1	0	0	0	00000000000000000000000011111111
0	1	0	0	1	00000000000000000000000111111111
0	1	0	1	0	00000000000000000000001111111111
0	1	0	1	1	00000000000000000000011111111111
0	1	1	0	0	00000000000000000000111111111111
0	1	1	0	1	00000000000000000001111111111111
0	1	1	1	0	00000000000000000011111111111111
0	1	1	1	1	00000000000000000111111111111111
1	0	0	0	0	00000000000000001111111111111111
1	0	0	0	1	00000000000000011111111111111111
1	0	0	1	0	00000000000000111111111111111111
1	0	0	1	1	00000000000001111111111111111111
1	0	1	0	0	00000000000011111111111111111111
1	0	1	0	1	00000000001111111111111111111111
1	0	1	1	0	00000000011111111111111111111111
1	0	1	1	1	00000000111111111111111111111111
1	1	0	0	0	00000001111111111111111111111111
1	1	0	0	1	00000011111111111111111111111111
1	1	0	1	0	00000111111111111111111111111111
1	1	0	1	1	00001111111111111111111111111111
1	1	1	0	0	00011111111111111111111111111111
1	1	1	0	1	00111111111111111111111111111111
1	1	1	1	0	01111111111111111111111111111111
1	1	1	1	1	11111111111111111111111111111111

From the above truth table we are constructing relation between thermometer codes to binary code. The following shows that from bit4 to bit 0 equivalent thermometer codes.

Bit 4 = K_{15}

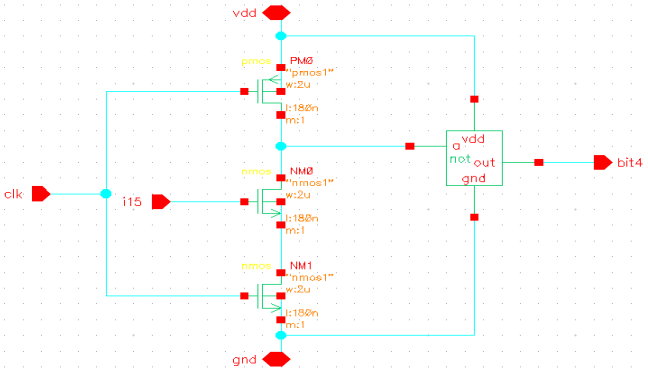
Bit 3 = $K_7.\overline{K_{15}} + K_{23}$

Bit 2 = $K_3.\overline{K_7} + K_{11}.\overline{K_{15}} + K_{23}.\overline{K_{23}} + K_{27}$

Bit 1 = $K_1.\overline{K_3} + K_5.\overline{K_7} + K_9.\overline{K_{11}} + K_{13}.\overline{K_{15}} + K_{17}.\overline{K_{17}} + K_{21}.\overline{K_{23}} + K_{25}.\overline{K_{27}} + K_{29}$

Bit 0 = $K_0.\overline{K_1} + K_2.\overline{K_3} + K_4.\overline{K_5} + K_6.\overline{K_7} + K_8.\overline{K_9} + K_{10}.\overline{K_{11}} + K_{12}.\overline{K_{13}} + K_{14}.\overline{K_{15}} + K_{16}.\overline{K_{17}} + K_{18}.\overline{K_{19}} + K_{20}.\overline{K_{21}} + K_{22}.\overline{K_{23}} + K_{24}.\overline{K_{25}} + K_{26}.\overline{K_{27}} + K_{28}.\overline{K_{29}} + K_{30}$

The fig 5(a), (b), (c) ,(d)& (e) shows the thermometer code to binary converter bit by bit from bit 4 to bit 0 schematic and layout diagrams respectively.



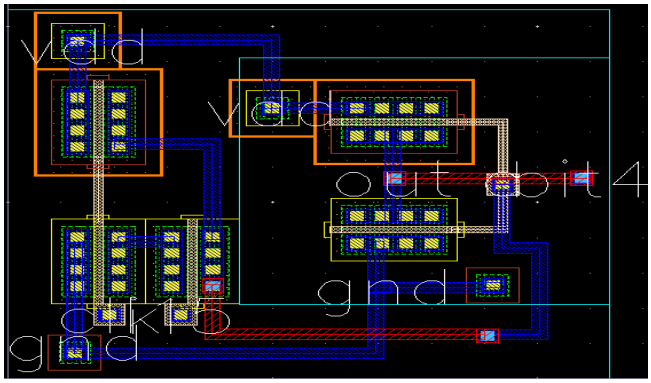
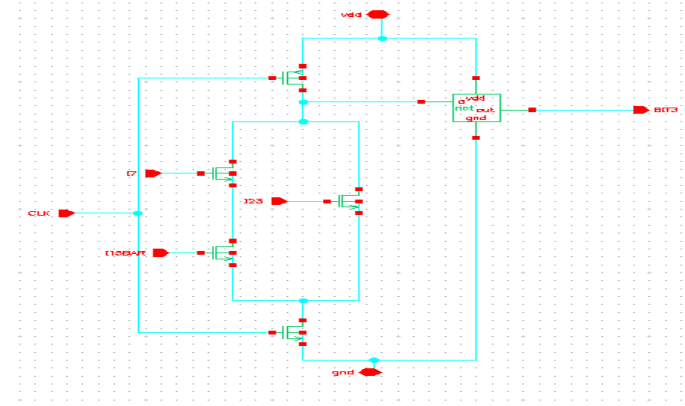


Fig 5.a Bit 4 schematic and layout



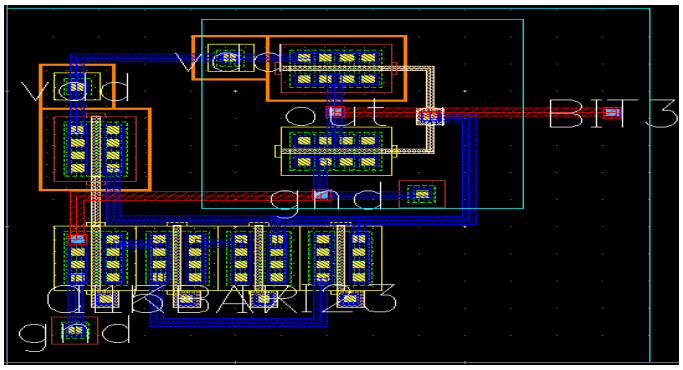
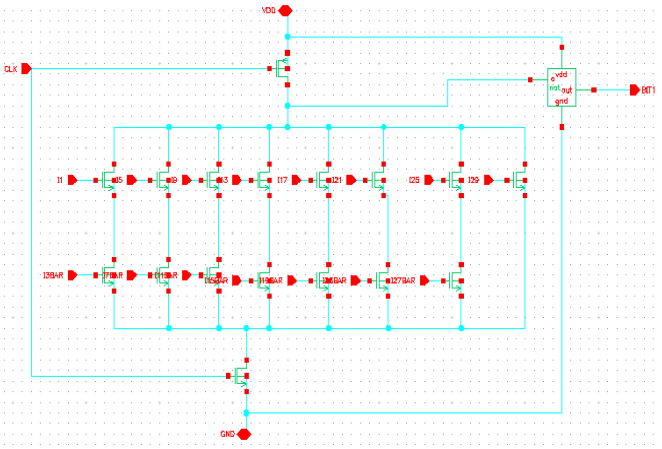


Fig 5.b Bit 3 schematic and layout



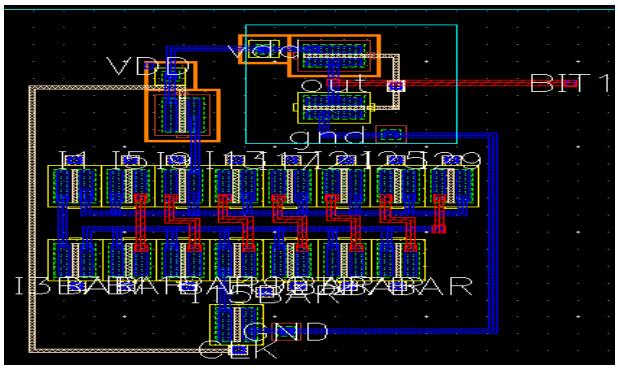
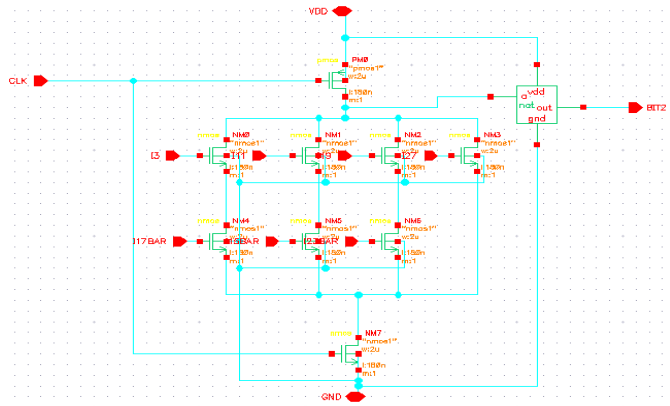


Fig 5.d Bit 1 schematic and layout



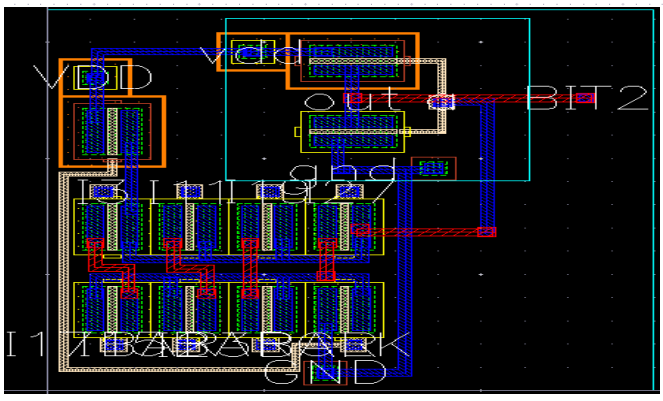
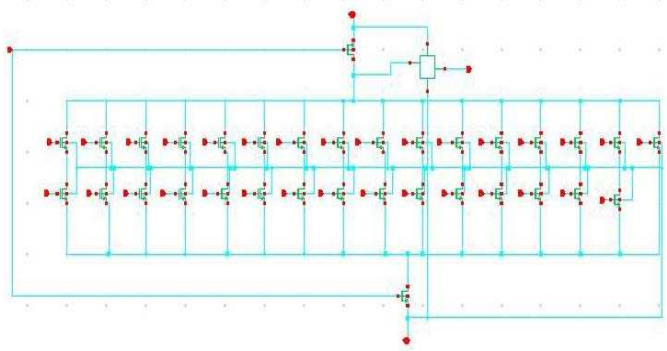


Fig 5.c Bit 2 schematic and layout



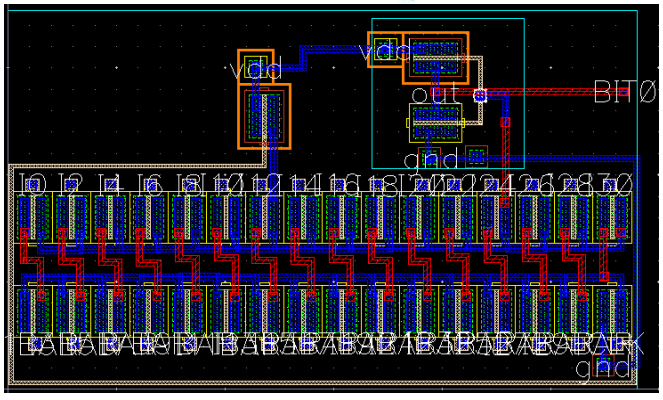


Fig 5.e Bit 0 schematic and layout

III. RESULT

Section II implemented flash ADC implemented by using dynamic comparator to achieve speed of converter. Tab 2 shows Comparison of Transistor values of comparators. Tab 3 shows comparison results of Comparators. Tab 4 shows Comparison results of ADCs.

Table 2 shows Transistor values of comparators

	[1]		[3]		[4]		[5]		PROPOSED COMPARATOR	
TRANSISTOR	W	L	W	L	W	L	W	L	W	L
M1	8	0.1	8	0.1	8	0.1	8	0.1	4	0.1
M2	4	0.1	4	0.1	4	0.1	4	0.1	4	0.1
M3	4	0.1	4	0.1	4	0.1	4	0.1	4	0.1
M4	X	X	2	0.1	2	0.1	2	0.1	2	0.1
M5	X	X	2	0.1	2	0.1	2	0.1	2	0.1
M6	X	X	X	X	2	0.1	2	0.1	2	0.1
M7	X	X	X	X	2	0.1	2	0.1	2	0.1
M8	2	0.1	2	0.1	2	0.1	2	0.1	1	0.1
M9	2	0.1	2	0.1	2	0.1	2	0.1	1	0.1
M10	2	0.1	4	0.1	4	0.1	2	0.1	0.5	0.1
M11	2	0.1	4	0.1	4	0.1	2	0.1	0.5	0.1
M12	2	0.1	2	0.1	2	0.1	4	0.1	0.5	0.1
M13	2	0.1	2	0.1	2	0.1	4	0.1	0.5	0.1
M14	4	0.1	4	0.1	4	0.1	4	0.1	4	0.1
M15	4	0.1	X	X	4	0.1	4	0.1	4	0.1
M16	X	X	0.18	0.1	4	0.1	0.18	0.1	0.18	0.1
M17	X	X	0.18	0.1	4	0.1	0.18	0.1	0.18	0.1
M18	X	X	X	X	X	X	0.18	0.1	0.18	0.1
M19	X	X	X	X	X	X	0.18	0.1	0.18	0.1
M20	X	X	X	X	X	X	X	X	1	0.1
M21	X	X	X	X	X	X	X	X	1	0.1

Table 3 Comparator comparison results

COMPARATORS	***Transistor Count (mV)***	***Offset Voltage (mV)***	***Power Dissipation (nS)***	***Delay(GHz)***	***Speed (V/nS)***	***Slew Rate***
Preamplifier Based Comparator [11]	22	64.35	83.45	0.393	2.54	21.23
Latch Type Voltage Sense Amplifier [2]	19	339.6	14.84	1.247	0.802	11.08
Double Tail Latch Type Voltage SA[3]	22	259.8	127.9	1.745	0.573	39.85
Dynamic Comparator without Calibration [4]	23	300.1	105.33	0.61	1.639	3.09
Double Tail Dual Rail Comp.[5]	27	300	57.37	1.49	0.671	10.77
Proposed Comparator	**29**	**300**	**44**	**1.1**	**0.91**	**10.26**

Table 4 Comparison of ADC results

	Power (um)	Delay(ns)
ADC using latched comparator	18500	781.4
ADC using proposed comparator	15200	419.9
Encoder	58.5	1.29

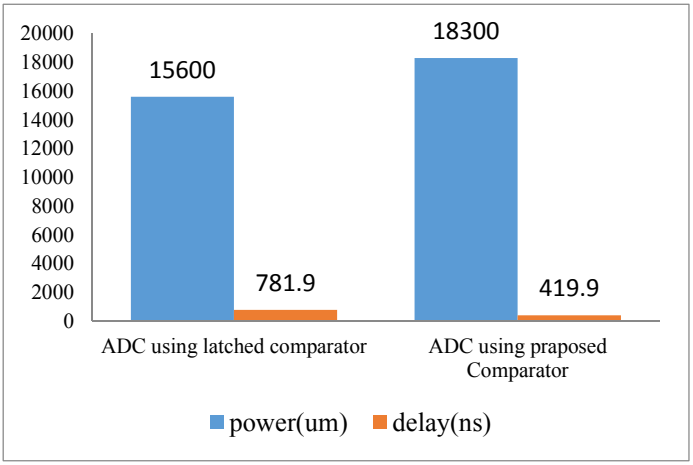


Fig 6 Power and delay graphs of ADCs

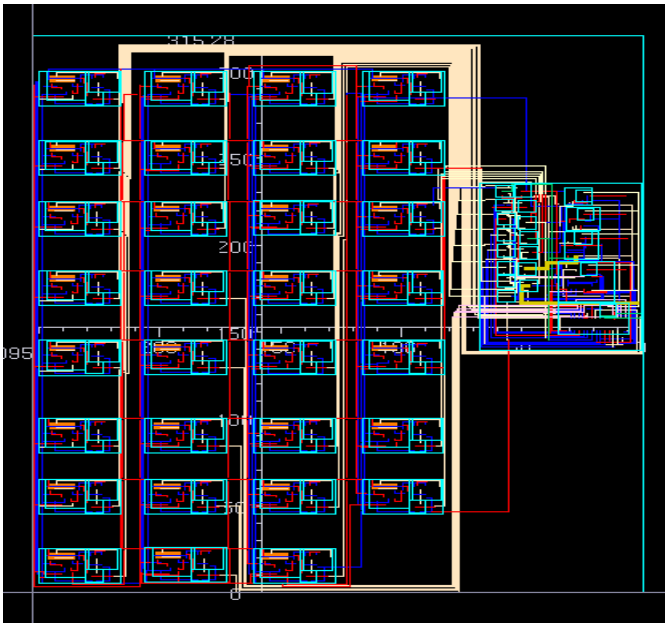


Fig 7 ADC layout

III. CONCLUSION

Two types of comparators implemented those are latched comparator and Proposed comparator. Calculated power, delay and power delay product (PDP). Proposed comparator power and delay is reduced. By using proposed comparator reduced static power dissipation. The encoder power dissipation plays major role designing of flash ADC. Using dynamic CMOS logic designed encoder to reduce static power. The encoder designed and tested using all the input combinations discussed in section II and verified. The proposed encoder which operates at 5 GH_z consumes 58.5uw and delay 1.29 ns. Hence the ADC implemented by proposed comparator having more speed than latched comparator.

V. ACKNOWLEDGEMENT

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