



ASIC Design Subject

**PGS.TS. Hoang Trang
ThS. Pham Dang Lam**



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Synopsys Tools

VCS IC Compiler, Formality, Design Compiler

System-Level Design Digital signal processing design, high-level synthesis, virtual platforms and analog/mixed-signal simulation. MORE ▶	Verification High-performance system, RTL, equivalence checking, mixed-signal verification solutions, and Verification IP MORE ▶	Implementation & Signoff Advanced digital and custom IC and FPGA design solutions, including synthesis, test, physical implementation and verification, and signoff. MORE ▶
Manufacturing Mask synthesis, mask data prep, lithography simulation and verification, and yield management. MORE ▶	TCAD Process and device simulation tools for technology exploration, development and variability analysis. MORE ▶	Optical Design Optical design and analysis software and engineering services. MORE ▶

- ❖ OS: Linux environment (ReadHat 5, Fedora 13 - 14)
- ❖ Mode: Command mode or GUI mode (Command mode)
- ❖ Support tool: DVE (To load the waveform)

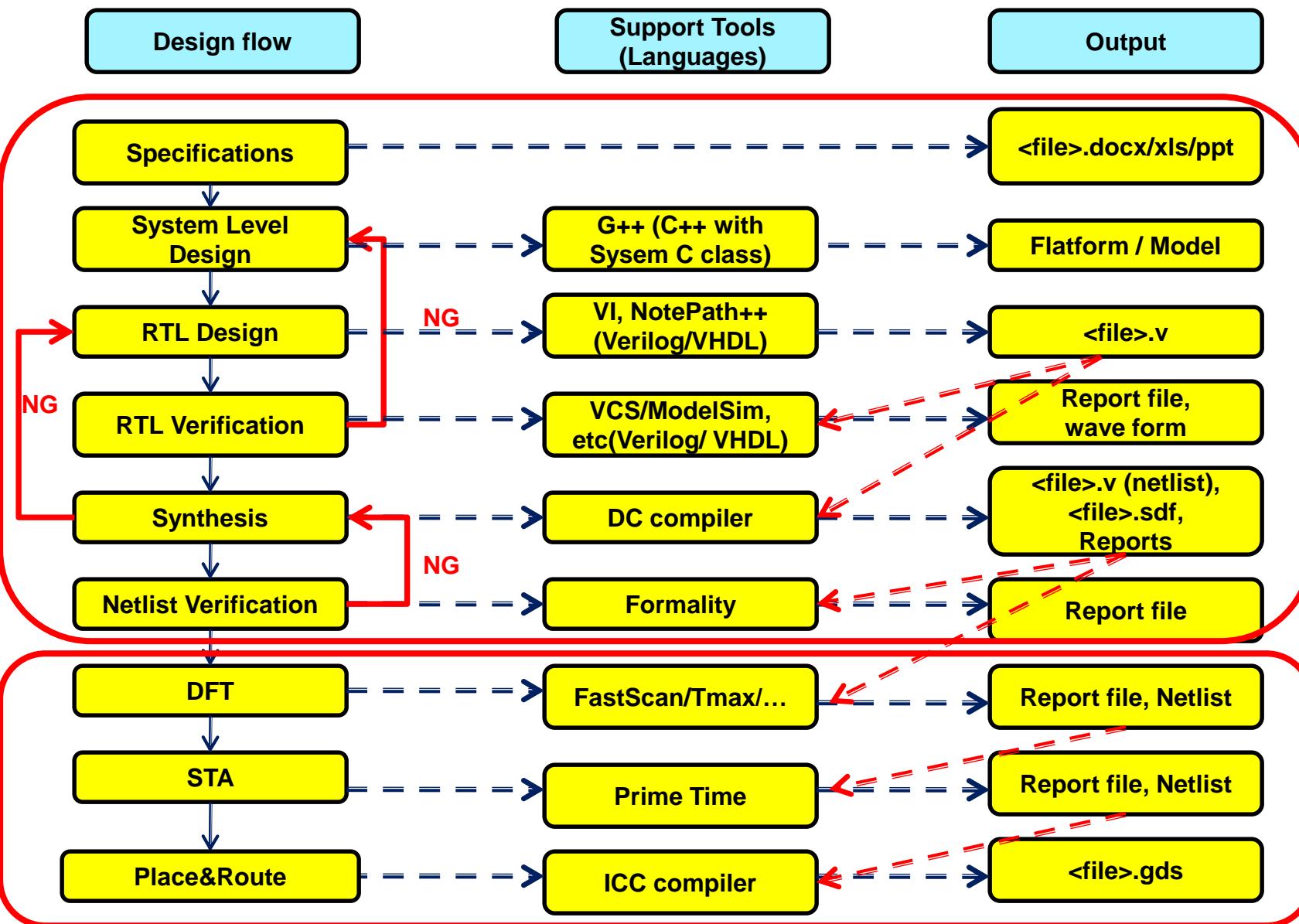
Synopsys Tools

VCS**IC Compiler, Formality, Design Compiler**

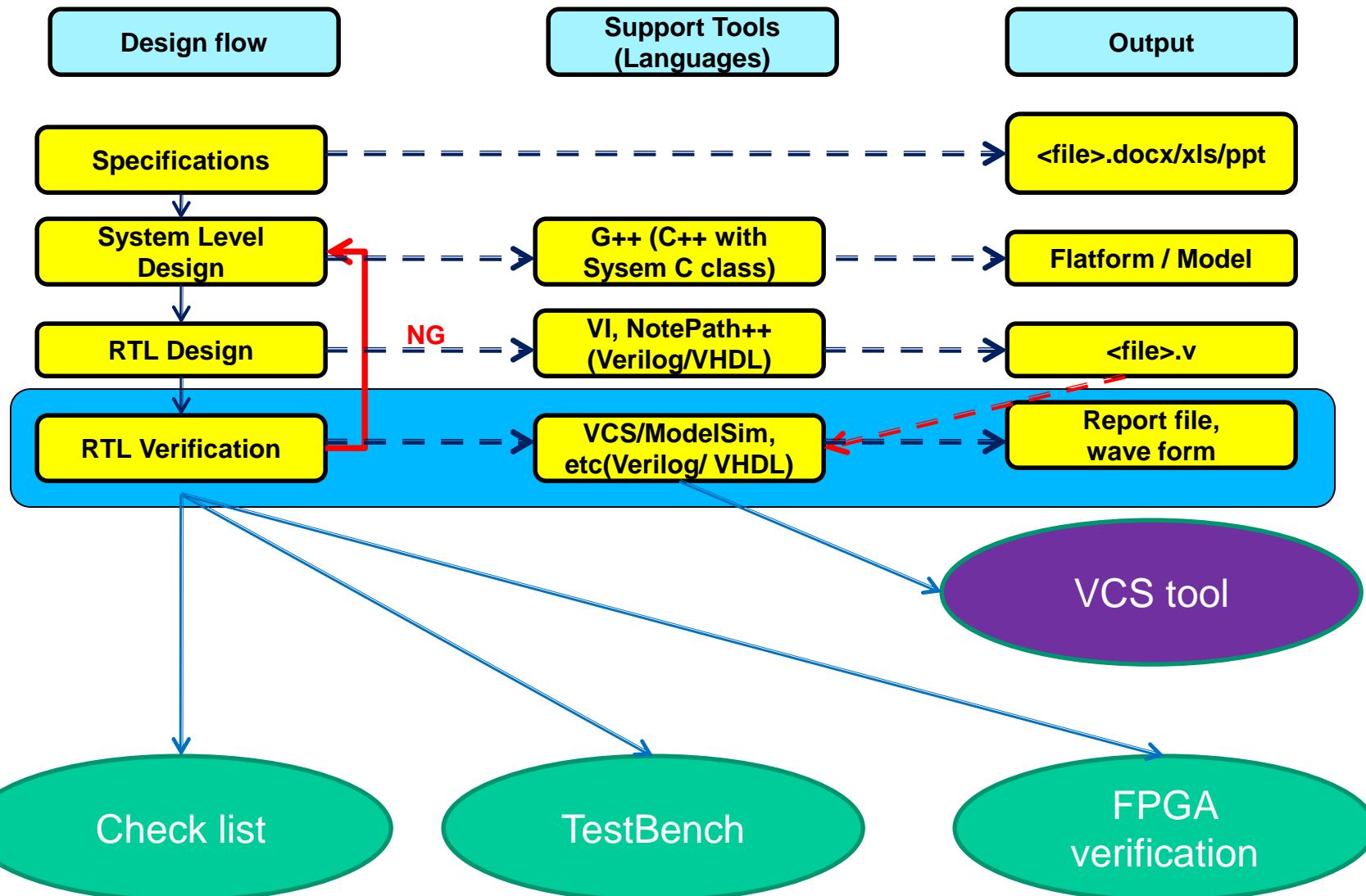
System-Level Design Digital signal processing design, high-level synthesis, virtual platforms and analog/mixed-signal simulation. MORE ▶	Verification High-performance system, RTL, equivalence checking, mixed-signal verification solutions, and Verification IP MORE ▶	Implementation & Signoff Advanced digital and custom IC and FPGA design solutions, including synthesis, test, physical implementation and verification, and signoff. MORE ▶
Manufacturing Mask synthesis, mask data prep, lithography simulation and verification, and yield management. MORE ▶	TCAD Process and device simulation tools for technology exploration, development and variability analysis. MORE ▶	Optical Design Optical design and analysis software and engineering services. MORE ▶

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- ❖ Mode: Command mode or GUI mode (Command mode)
- ❖ Support tool: DVE (To load the waveform)

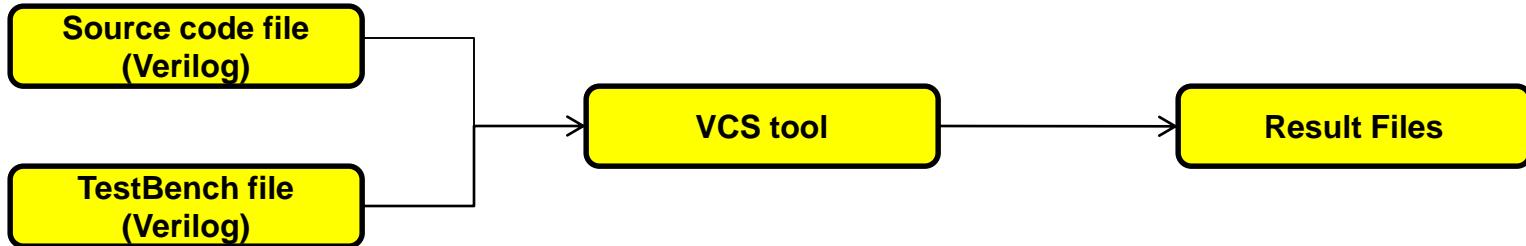
VCS Tool In Design Flow



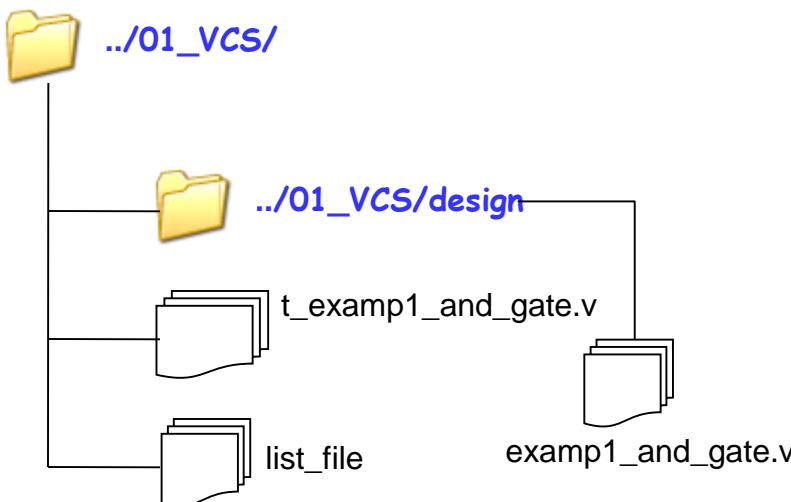
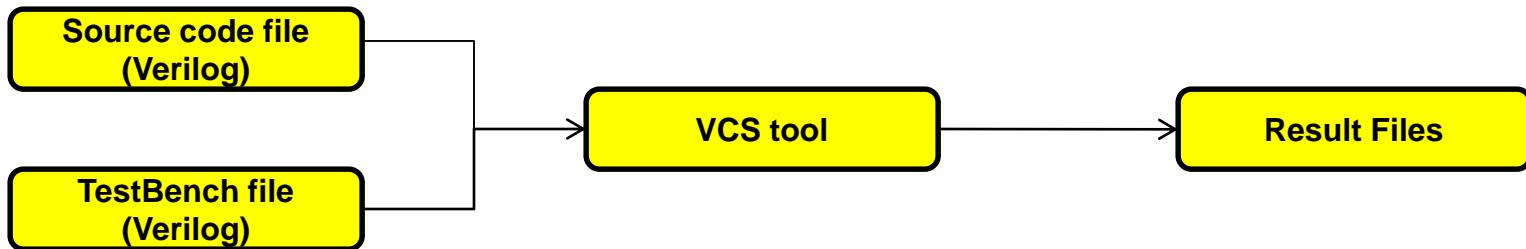
VCS Tool In Design Flow



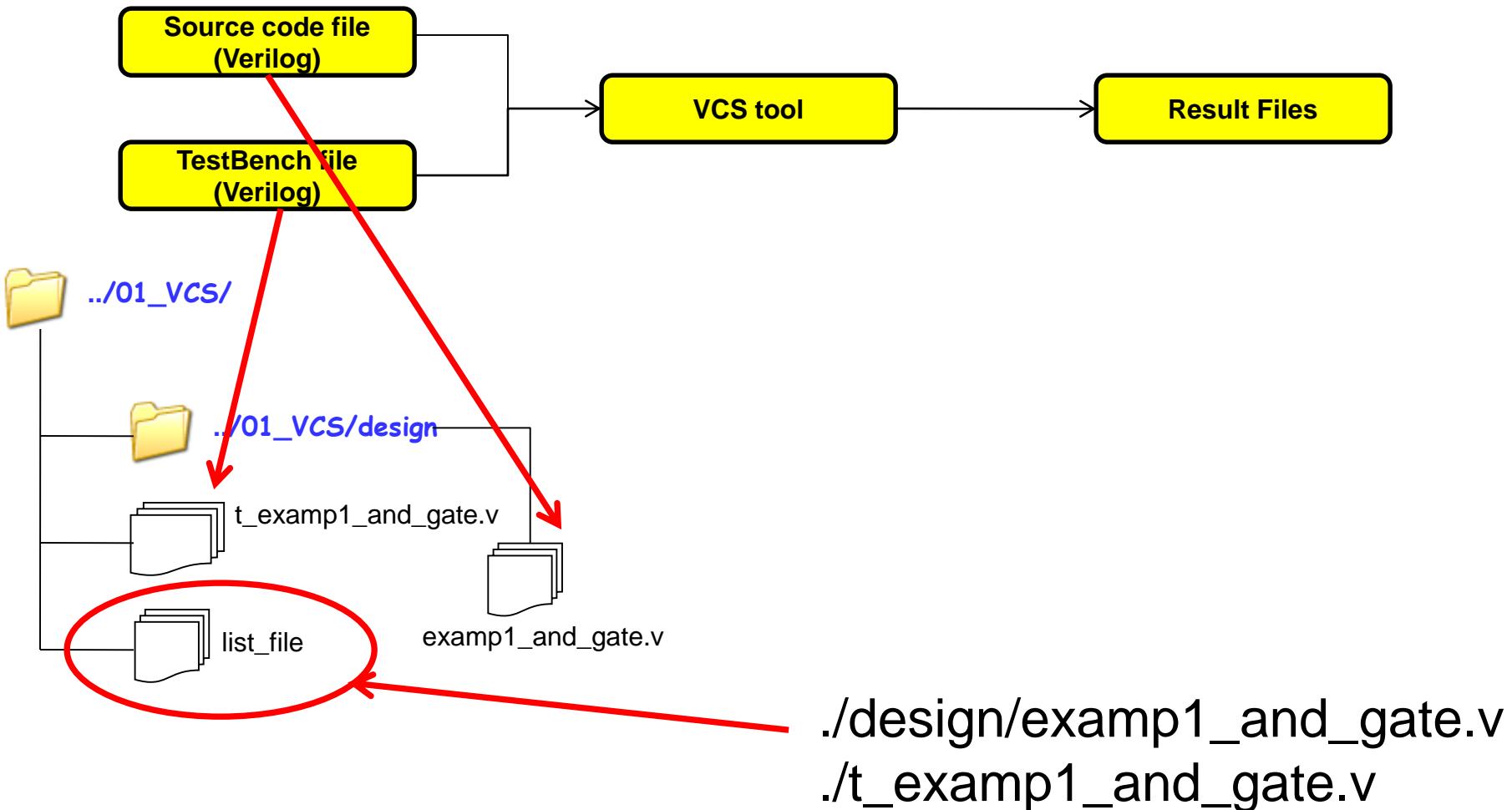
How to run VCS?



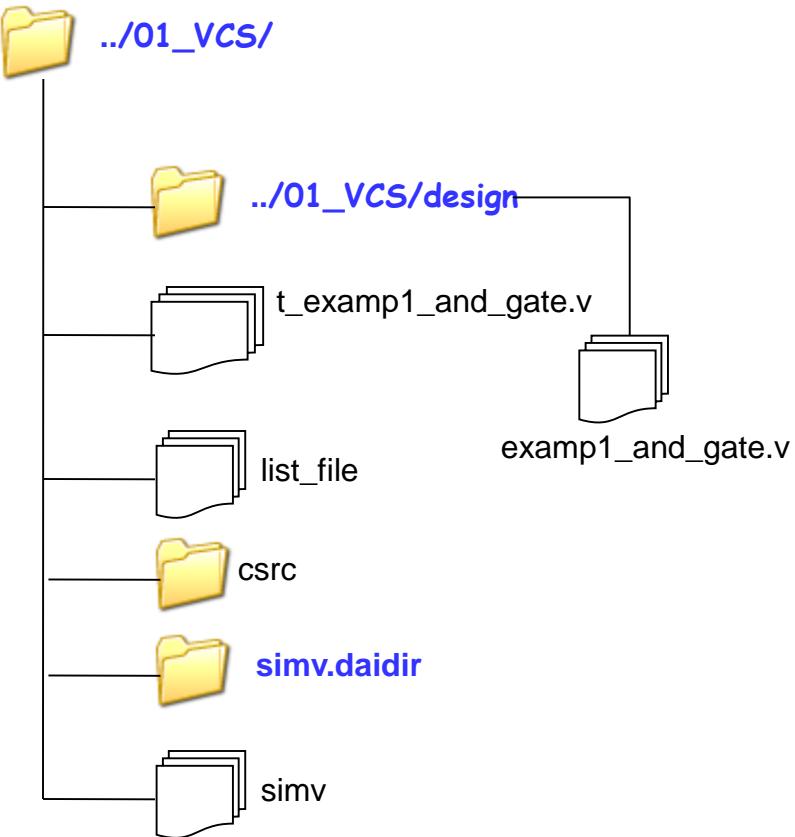
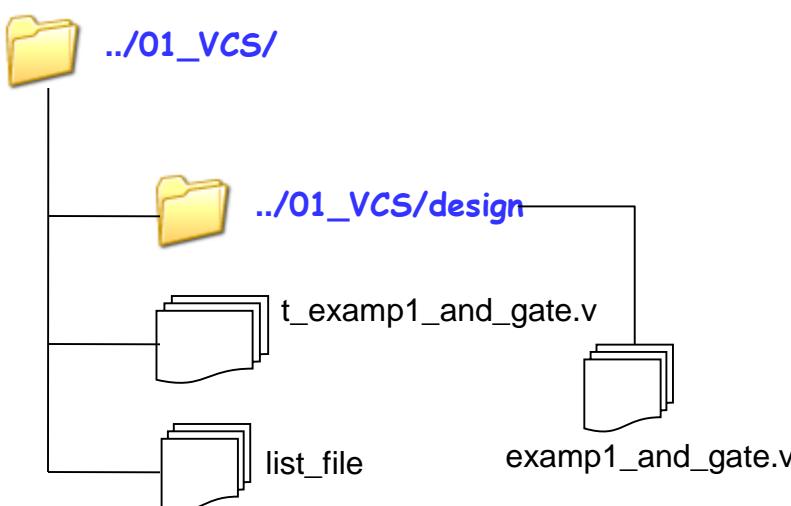
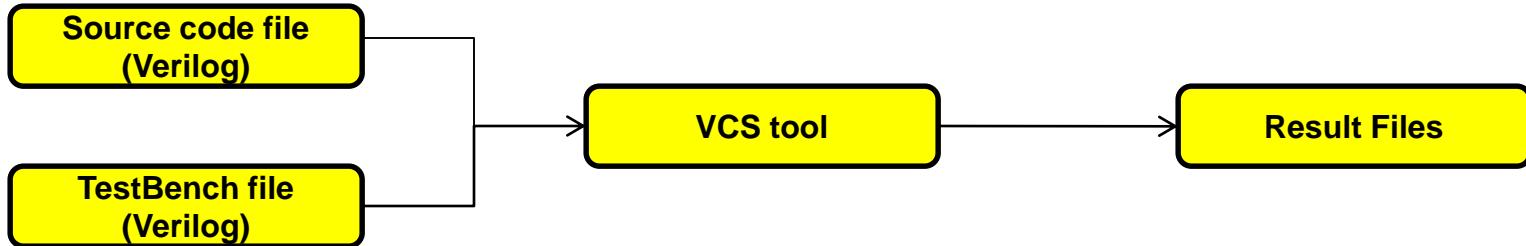
How to run VCS?



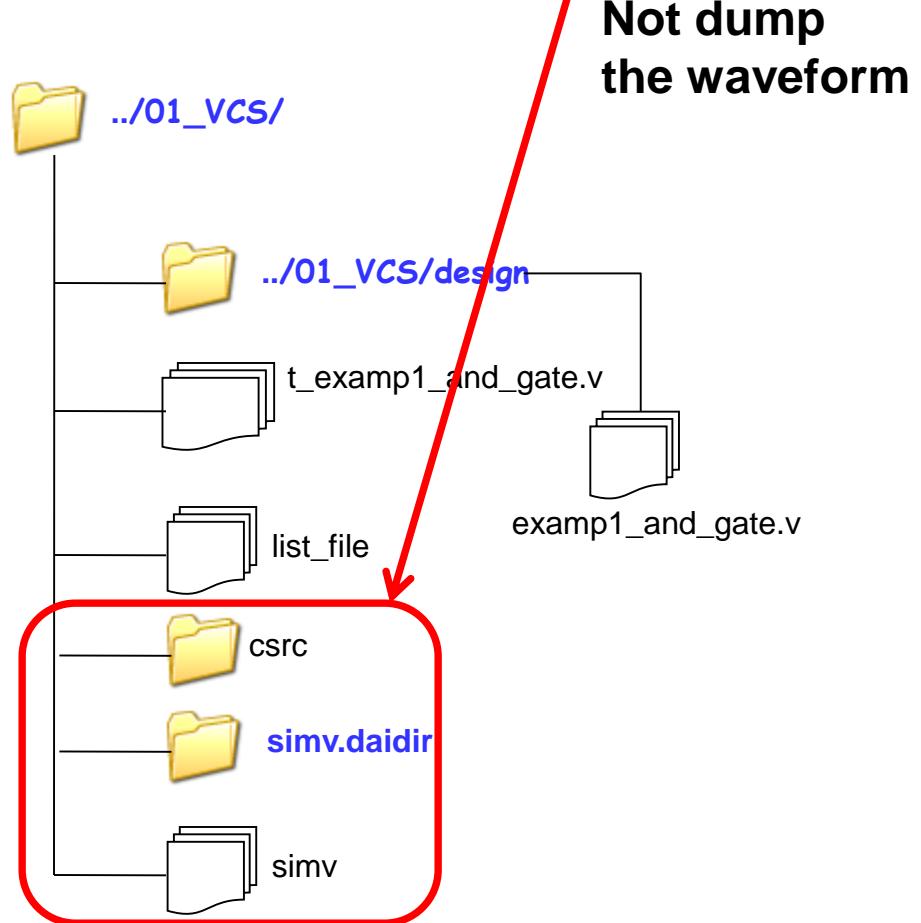
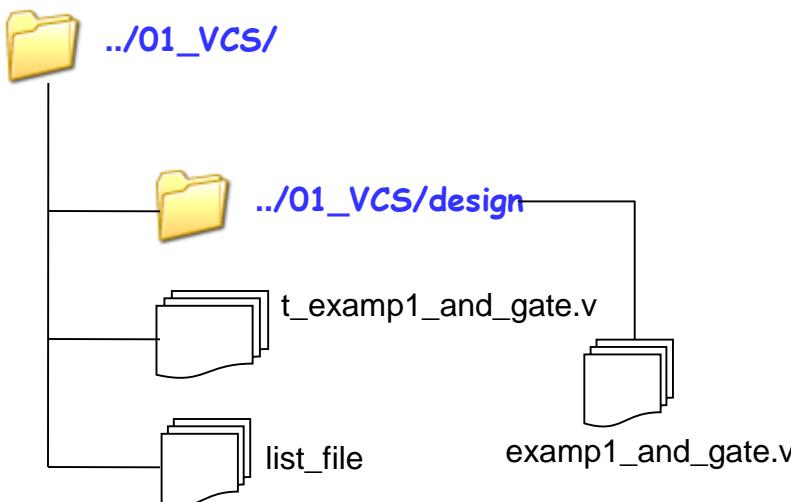
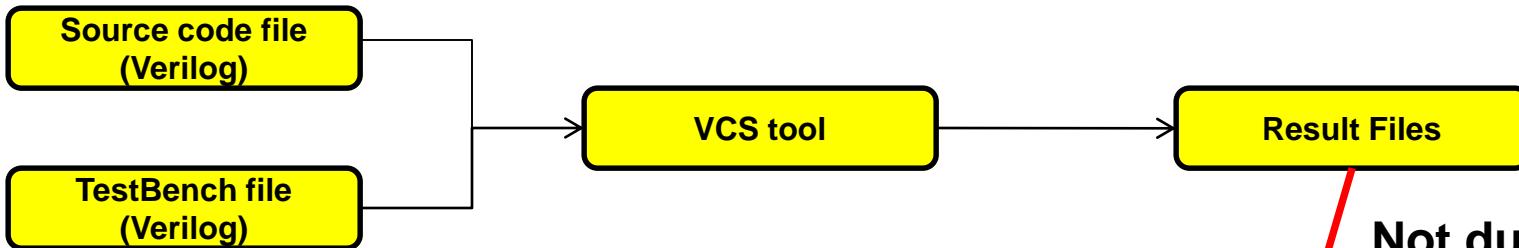
How to run VCS?



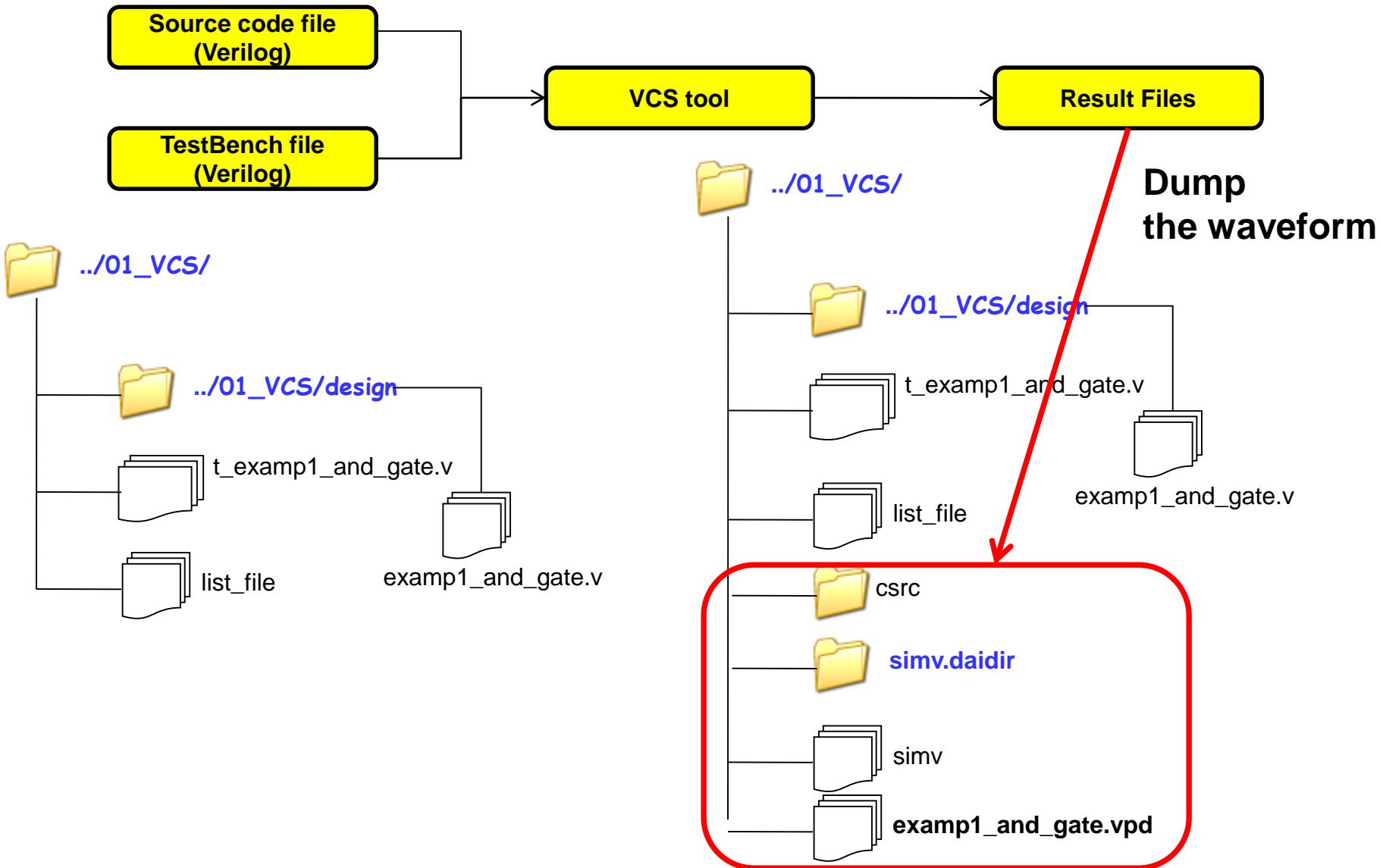
How to run VCS?



How to run VCS?



How to run VCS?





VCS Command

```
source /home/lampham/synopsys/licensen/linux/bin/s
```

```
vcs <mode option> <debug option> <file option> <version option> ...
```

Option Name	Command	Notes
Mode	-R	Command Mode
	-gui	GUI Mode
Debug	-debug	Export the waveform to debug
	-debug_all	Export the waveform to debug, line debug
File	-f <file>	Compile all files listed in the file
	-o <file>	Export the executed file (sim.v is default)
	-l <file>	Export the log file
Version	+v2K	Add the version 2000
Others	-sverilog	Compile the mis_language (Verilog & System Verilog)



How to run VCS?

Applications Places System

Fri Mar 22, 10:53 PM phamdanglam

File Edit View Terminal Help

lampham@lampham:~/Work/06_Lap/01_VCS

```
/home/lampham/Work/06_Lap/01_VCS
design
[lampham@lampham 01_VCS]$ tree
.
`-- design
    '-- example_and_gate.v

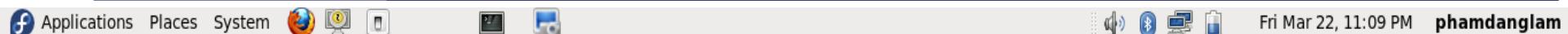
1 directory, 1 file
[lampham@lampham 01_VCS]$
```

A red circle highlights the command "tree" in the terminal window. A red arrow points from the text "Folder/file hierarchy" to the red circle.

Folder/file hierarchy



How to run VCS?



```
File Edit View Terminal Help  
/home/lampham/Work/06_Lap/01_VCS  
design  
[lampham@lampham 01_VCS]$ getlicense
```

A red oval highlights the command 'getlicense' in the terminal window. A red arrow points from this highlighted text to the text 'Get the synopsys license' located below the terminal window.

Get the synopsys license



How to run VCS?



File Edit View Terminal Help

```
Users of AIM_ENCRYPT:  (Uncounted, node-locked)
```

```
Users of aiu_foundation:  (Uncounted, node-locked)
```

```
Users of alien2lig_all:  (Uncounted, node-locked)
```

```
Users of ALTGEN1:  (Uncounted, node-locked)
```

```
Users of ALTGEN2:  (Uncounted, node-locked)
```

```
Users of amat-calib_all:  (Uncounted, node-locked)
```

```
Users of amga:  (Uncounted, node-locked)
```

```
Users of amps:  (Uncounted, node-locked)
```

```
Users of amps/cso:  (Uncounted, node-locked)
```

```
Users of amps/pfx:  (Uncounted, node-locked)
```

```
Users of amps/tr:  (Uncounted, node-locked)
```

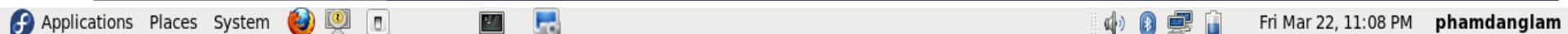
```
Users of AN-Impl3D_all:  (Uncounted, node-locked)
```

```
Users of any_technology:  (Uncounted, node-locked)
```

```
[lampham@lampham 01_VCS]$ █
```



How to run VCS?



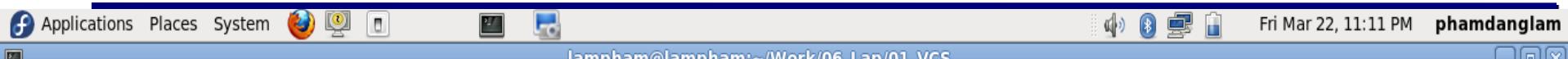
```
File Edit View Terminal Help  
/home/lampham/Work/06_Lap/01_VCS  
design  
[lampham@lampham 01_VCS]$ vcs -R design/examp1_and_gate.v
```

A red oval highlights the command `vcs -R design/examp1_and_gate.v`. A red arrow points from the text "Compile the design" below to this highlighted command.

Compile the design



How to run VCS?



File Edit View Terminal Help

/home/lampham/Work/06_Lap/01_VCS

design

```
[lampham@lampham 01_VCS]$ vcs -R design/examp1_and_gate.v
                                Chronologic VCS (TM)
Version D-2010.06-SP1 -- Fri Mar 22 23:10:55 2013
Copyright (c) 1991-2010 by Synopsys Inc.
ALL RIGHTS RESERVED
```

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controlling such use and disclosure.

Parsing design file 'design/examp1_and_gate.v'

Top Level Modules:

example1_and_gate

No TimeScale specified

The error line in design

```
Error-[ISLHS] Illegal structural left hand side
design/examp1_and_gate.v, 25
```

Following expression cannot be used on the left hand side of this
assignment.

Expression: pre_data_out_and_gate

Source info: assign pre_data_out_and_gate = (fist_data_in & second_data_in);

1 error

CPU time: .076 seconds to compile

```
[lampham@lampham 01_VCS]$
```

Error in design



How to run VCS?



File Edit View Terminal Help

/home/lampham/Work/06_Lap/01_VCS

[design](#)

```
[lampham@lampham 01_VCS]$ vcs -R design/examp1_and_gate.v
Chronologic VCS (TM)
Version D-2010.06-SP1 -- Fri Mar 22 23:10:55 2013
Copyright (c) 1991-2010 by Synopsys Inc.
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```

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Parsing design file 'design/examp1_and_gate.v'

Top Level Modules:

example1_and_gate

No TimeScale specified

Open the design

```
Error-[ISLHS] Illegal structural left hand side
design/examp1_and_gate.v, 25
```

Following expression cannot be used on the left hand side of this
assignment.

Expression: pre_data_out_and_gate

Source info: assign pre_data_out_and_gate = (first_data_in & second_data_in);

1 error

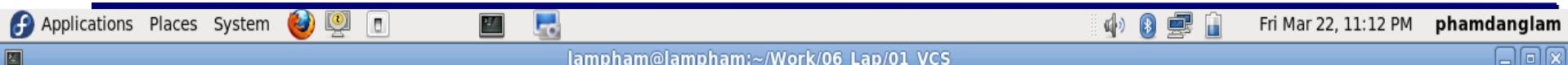
CPU time: .076 seconds to compile

```
[lampham@lampham 01_VCS]$ vi design/examp1_and_gate.v
```





How to run VCS?



```
//===== File name: example1_and_gate.v
//===== Version: 1.0
//===== Update Notes: First Version

module example1_and_gate (system_clock, system_rst_n, fist_data_in, second_data_in, data_out_and_gate);

//parameter define
parameter DATA_WIDTH = 8;

//input define
input system_clock;
input system_rst_n;
input [DATA_WIDTH-1:0] fist_data_in;
input [DATA_WIDTH-1:0] second_data_in;

//output define
output [DATA_WIDTH-1:0] data_out_and_gate;
reg [DATA_WIDTH-1:0] data_out_and_gate;

//internal wire/reg define
reg [DATA_WIDTH-1:0] pre_data_out_and_gate;

//Main functions define
//1.1 Combination logic (and logic) is implemented by "assign" prototype
assign pre_data_out_and_gate = fist_data_in & second_data_in;

//1.2 Combination logic (and logic) is implemented by "always" prototype
```

Look up the error line



How to run VCS?



```
//===== File name: example1_and_gate.v
//===== Version: 1.0
//===== Update Notes: First Version

module example1_and_gate (system_clock, system_rst_n, fist_data_in, second_data_in, data_out_and_gate);

//parameter define
parameter DATA_WIDTH = 8;

//input define
input system_clock;
input system_rst_n;
input [DATA_WIDTH-1:0] fist_data_in;
input [DATA_WIDTH-1:0] second_data_in;

//output define
output [DATA_WIDTH-1:0] data_out_and_gate;
reg [DATA_WIDTH-1:0] data_out_and_gate;

//internal wire/reg define
reg [DATA_WIDTH-1:0] pre_data_out_and_gate;

//Main functions define
//1.1 Combination logic (and logic) is implemented by "assign" prototype
assign pre_data_out_and_gate = fist_data_in & second_data_in;

//1.2 Combination logic (and logic) is implemented by "always" prototype
/pre_data_out_and_gate
```

Conflict the type of variable



How to run VCS?



```
===== File name: example1_and_gate.v
===== Version: 1.0
===== Update Notes: First Version

module example1_and_gate (system_clock, system_rst_n, fist_data_in, second_data_in, data_out_and_gate);

//parameter define
parameter DATA_WIDTH = 8;

//input define
input system_clock;
input system_rst_n;
input [DATA_WIDTH-1:0] fist_data_in;
input [DATA_WIDTH-1:0] second_data_in;

//output define
output [DATA_WIDTH-1:0] data_out_and_gate;
reg [DATA_WIDTH-1:0] data_out_and_gate;

//internal wire/reg define
reg [DATA_WIDTH-1:0] pre_data_out_and_gate;

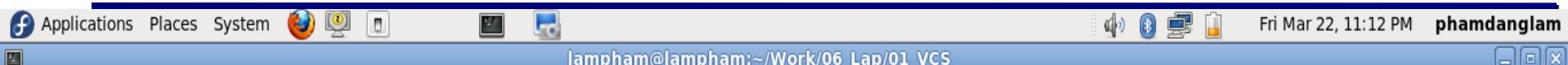
//Main functions define
//1.1 Combination logic (and logic) is implemented by "assign" prototype
assign pre_data_out_and_gate = fist_data_in & second_data_in;

//1.2 Combination logic (and logic) is implemented by "always" prototype
/pre_data_out_and_gate
```

This should be “wire” type



How to run VCS?



```
//===== File name: example1_and_gate.v
//===== Version: 1.0
//===== Update Notes: First Version

module example1_and_gate (system_clock, system_rst_n, fist_data_in, second_data_in, data_out_and_gate);

//parameter define
parameter DATA_WIDTH = 8;

//input define
input system_clock;
input system_rst_n;
input [DATA_WIDTH-1:0] fist_data_in;
input [DATA_WIDTH-1:0] second_data_in;

//output define
output [DATA_WIDTH-1:0] data_out_and_gate;
reg    [DATA_WIDTH-1:0] data_out_and_gate;

//internal wire/reg define
wire    [DATA_WIDTH-1:0] pre_data_out_and_gate;

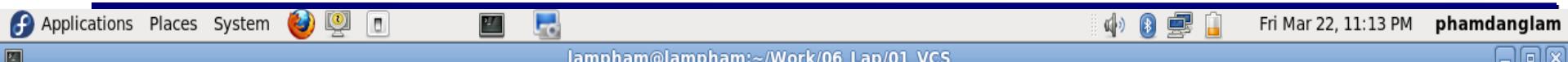
//Main functions define
//1.1 Combination logic (and logic) is implemented by "assign" prototype
assign pre_data_out_and_gate = fist_data_in & second_data_in;

//1.2 Combination logic (and logic) is implemented by "always" prototype
:wq
```

Store and quit



How to run VCS?



File Edit View Terminal Help

/home/lampham/Work/06_Lap/01_VCS

[design](#)

```
[lampham@lampham 01_VCS]$ vcs -R design/examp1_and_gate.v
Chronologic VCS (TM)
Version D-2010.06-SP1 -- Fri Mar 22 23:10:55 2013
Copyright (c) 1991-2010 by Synopsys Inc.
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```

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controlling such use and disclosure.

Parsing design file 'design/examp1_and_gate.v'

Top Level Modules:

example1_and_gate

No TimeScale specified

Error-[ISLHS] Illegal structural left hand side

design/examp1_and_gate.v, 25

Following expression cannot be used on the left hand side of this
assignment.

Expression: pre_data_out_and_gate

Source info: assign pre_data_out_and_gate = (fist_data_in & second_data_in);

1 error

CPU time: .076 seconds to compile

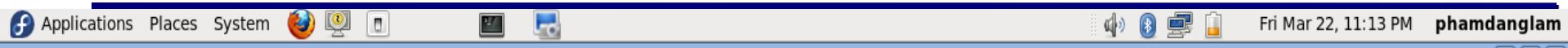
[lampham@lampham 01_VCS]\$ vi design/examp1_and_gate.v

[lampham@lampham 01_VCS]\$ vcs -R design/examp1_and_gate.v

Compile again



How to run VCS?



lampham@lampham:~/Work/06_Lap/01_VCS

File Edit View Terminal Help

```
[lampham@lampham 01_VCS]$ vi design/examp1_and_gate.v
[lampham@lampham 01_VCS]$ vcs -R design/examp1_and_gate.v
    Chronologic VCS (TM)
Version D-2010.06-SP1 -- Fri Mar 22 23:13:12 2013
Copyright (c) 1991-2010 by Synopsys Inc.
ALL RIGHTS RESERVED
```

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Parsing design file 'design/examp1_and_gate.v'

Top Level Modules:
example1_and_gate
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.

```
recompiling module example1_and_gate
if [ -x ..;/simv ]; then chmod -x ..;/simv; fi
g++ -o ..;/simv -melf_i386 _vcsobj_1_1.o 5NrI_d.o 5NrIB_d.o SIM_l.o      rmapats_mop.o rmapats.o      /home/l
ampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libvirsim.so /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libr
terrorinf.so /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libsnpsmalloc.so   /home/lampham/synopsys/VCS_
D-2010.06-SP1/linux/lib/libvcsnew.so      /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/vcs_save_restore_
new.o /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
..;/simv up to date
Chronologic VCS simulator copyright 1991-2010
Contains Synopsys proprietary information.
Compiler version D-2010.06-SP1; Runtime version D-2010.06-SP1; Mar 22 23:13 2013
```

Finish compile

V C S S i m u l a t i o n R e p o r t

Time: 0
CPU Time: 0.030 seconds; Data structure size: 0.0Mb

Fri Mar 22 23:13:17 2013

CPU time: .082 seconds to compile + .061 seconds to elab + .377 seconds to link + .119 seconds in simulation

[lampham@lampham 01_VCS]\$ █

lampham@lampham:~



How to run VCS?



```
File Edit View Terminal Help  
/home/lampham/Work/06_Lap/01_VCS  
csrc design simv simv.daidir  
[lampham@lampham 01_VCS]$ ll  
total 516  
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:13 csrc ←  
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 design ←  
-rwxrwxr-x. 1 lampham lampham 515876 Mar 22 23:13 simv ←  
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 simv.daidir ←  
[lampham@lampham 01_VCS]$ █
```

The output files



How to run VCS?

Applications Places System

Fri Mar 22, 11:15 PM phamdanglam

File Edit View Terminal Help

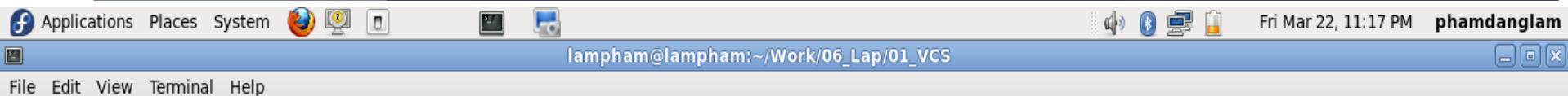
lampham@lampham:~/Work/06_Lap/01_VCS

```
/home/lampham/Work/06_Lap/01_VCS
csrc design simv simv.daidir
[lampham@lampham 01_VCS]$ ll
total 516
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:13 csrc
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 design
-rwxrwxr-x. 1 lampham lampham 515876 Mar 22 23:13 simv
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 simv.daidir
[lampham@lampham 01_VCS]$ vi t_exampl_and_gate.v
[lampham@lampham 01_VCS]$
```

Compose the testbench



How to run VCS?

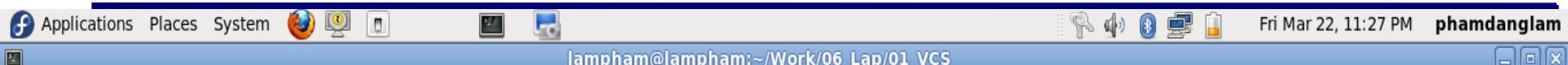


**Copy the same content
from the other file**

```
:r /home/lampham/Work/01_Speech_Reg/02_Developpt/01_Floating_Point_Mul/t_floating_point_muliple.v
```



How to run VCS?



File Edit View Terminal Help

```
/home/lampham/Work/06_Lap/01_VCS
csrc design simv simv.daidir t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ ll
total 520
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:13 csrc
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:19 design
-rwxrwxr-x. 1 lampham lampham 515876 Mar 22 23:13 simv
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 simv.daidir
-rw-rw-r--. 1 lampham lampham 1319 Mar 22 23:27 t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ vi list_file
```

Compose the list file



How to run VCS?

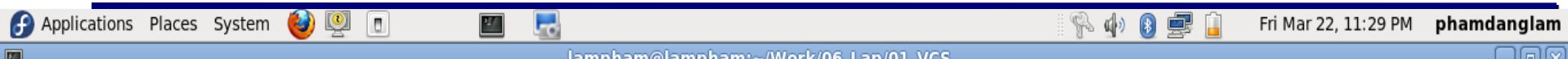
```
Applications Places System lampham@lampham:~/Work/06_Lap/01_VCS
File Edit View Terminal Help
./t_exampl1_and_gate.v
./design/examp1_and_gate.v
~:wq
```

The list file includes :

- + Design file
- + Testbench file



How to run VCS?

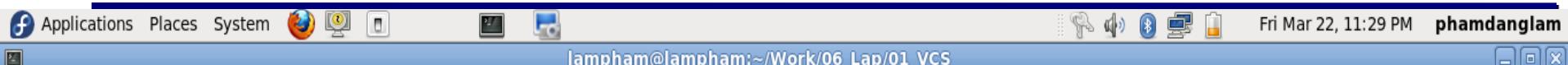


```
/home/lampham/Work/06_Lap/01_VCS
csim design list_file simv simv.daidir t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ ll
total 524
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:13 csrc
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:27 design
-rw-rw-r--. 1 lampham lampham 49 Mar 22 23:29 list_file
-rwxrwxr-x. 1 lampham lampham 515876 Mar 22 23:13 simv
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 simv.daidir
-rw-rw-r--. 1 lampham lampham 1319 Mar 22 23:27 t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ █
```

Finish testbench and list file



How to run VCS?

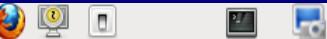


```
/home/lampham/Work/06_Lap/01_VCS
csrc  design  list_file  simv  simv.daidir  t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ ll
total 524
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:13 csrc
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:27 design
-rw-rw-r--. 1 lampham lampham 49 Mar 22 23:29 list_file
-rwxrwxr-x. 1 lampham lampham 515876 Mar 22 23:13 simv
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:13 simv.daidir
-rw-rw-r--. 1 lampham lampham 1319 Mar 22 23:27 t_exampl_and_gate.v
[lampham@lampham 01_VCS]$ vcs -R -debug_all -f list_file
```

Compose the design and testbench



How to run VCS?

Applications Places System  Fri Mar 22, 11:47 PM phamdanglam

```
File Edit View Terminal Help
Parsing design file './design/examp1_and_gate.v'
Top Level Modules:
    t_examp1_and_gate
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module t_examp1_and_gate because:
    This module or some inlined child module(s) has/have been modified.
if [ -x ..simv ]; then chmod -x ..simv; fi
g++ -o ..simv -melf_i386 _vcsobj_1.o 5NrI_d.o 5NrIB_d.o SIM_l.o      rmapats_mop.o rmapats.o      /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libvirsim.so
/home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/librerrorinf.so /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libsnpsmalloc.so      /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libvcsnew.so      /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/vcs_save_restore_new.o /home/lampham/synopsys/VCS_D-2010.06-SP1/linux/lib/libctype-stubs_32.a -ldl -lm -lc -lpthread -ldl
../simv up to date
Chronologic VCS simulator copyright 1991-2010
Contains Synopsys proprietary information.
Compiler version D-2010.06-SP1; Runtime version D-2010.06-SP1; Mar 22 23:47 2013

VCD+ Writer D-2010.06-SP1 Copyright (c) 1991-2010 by Synopsys Inc.
time=      0, system_clock=0, system_rst_n=x, t_first_data_in:xxxxxxxx, t_second_data_in:xxxxxxxx, data_out_and_gate=xxxxxxxx
time=      1, system_clock=0, system_rst_n=0, t_first_data_in:xxxxxxxx, t_second_data_in:xxxxxxxx, data_out_and_gate=00000000
time=     11, system_clock=0, system_rst_n=1, t_first_data_in:xxxxxxxx, t_second_data_in:xxxxxxxx, data_out_and_gate=00000000
time=     21, system_clock=0, system_rst_n=1, t_first_data_in:11010101, t_second_data_in:10101010, data_out_and_gate=00000000
time=     50, system_clock=1, system_rst_n=1, t_first_data_in:11010101, t_second_data_in:10101010, data_out_and_gate=10000000
time=    100, system_clock=0, system_rst_n=1, t_first_data_in:11010101, t_second_data_in:10101010, data_out_and_gate=10000000

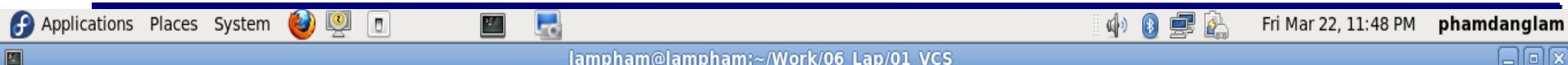
$finish called from file "./t examp1_and_gate.v", line 48.
$finish at simulation time          121
    V C S   S i m u l a t i o n   R e p o r t
Time: 121
CPU Time: 0.030 seconds; Data structure size: 0.0Mb
Fri Mar 22 23:47:28 2013
CPU time: .079 seconds to compile + .041 seconds to elaboration + .164 seconds to link + .089 seconds in simulation
[lampham@lampham 01_VCS]$
```

Simulation result

Finish the compile



How to run VCS?



File Edit View Terminal Help

```
/home/lampham/Work/06_Lap/01_VCS
csrc design exempl_and_gate.vpd list_file simv simv.daidir t_exmpl_and_gate.v
[lampham@lampham 01_VCS]$ ll
total 572
drwxrwxr-x. 3 lampham lampham 4096 Mar 22 23:47 csrc
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:42 design
-rw-rw-r--. 1 lampham lampham 1849 Mar 22 23:47 exempl_and_gate.vpd
-rw-rw-r--. 1 lampham lampham 49 Mar 22 23:37 list_file
-rwxrwxr-x. 1 lampham lampham 558594 Mar 22 23:47 simv
drwxrwxr-x. 2 lampham lampham 4096 Mar 22 23:47 simv.daidir
-rw-rw-r--. 1 lampham lampham 1451 Mar 22 23:47 t_exmpl_and_gate.v
[lampham@lampham 01_VCS]$
```

Use DVE tool to open the wave form



How to load the wave form?

Applications Places System

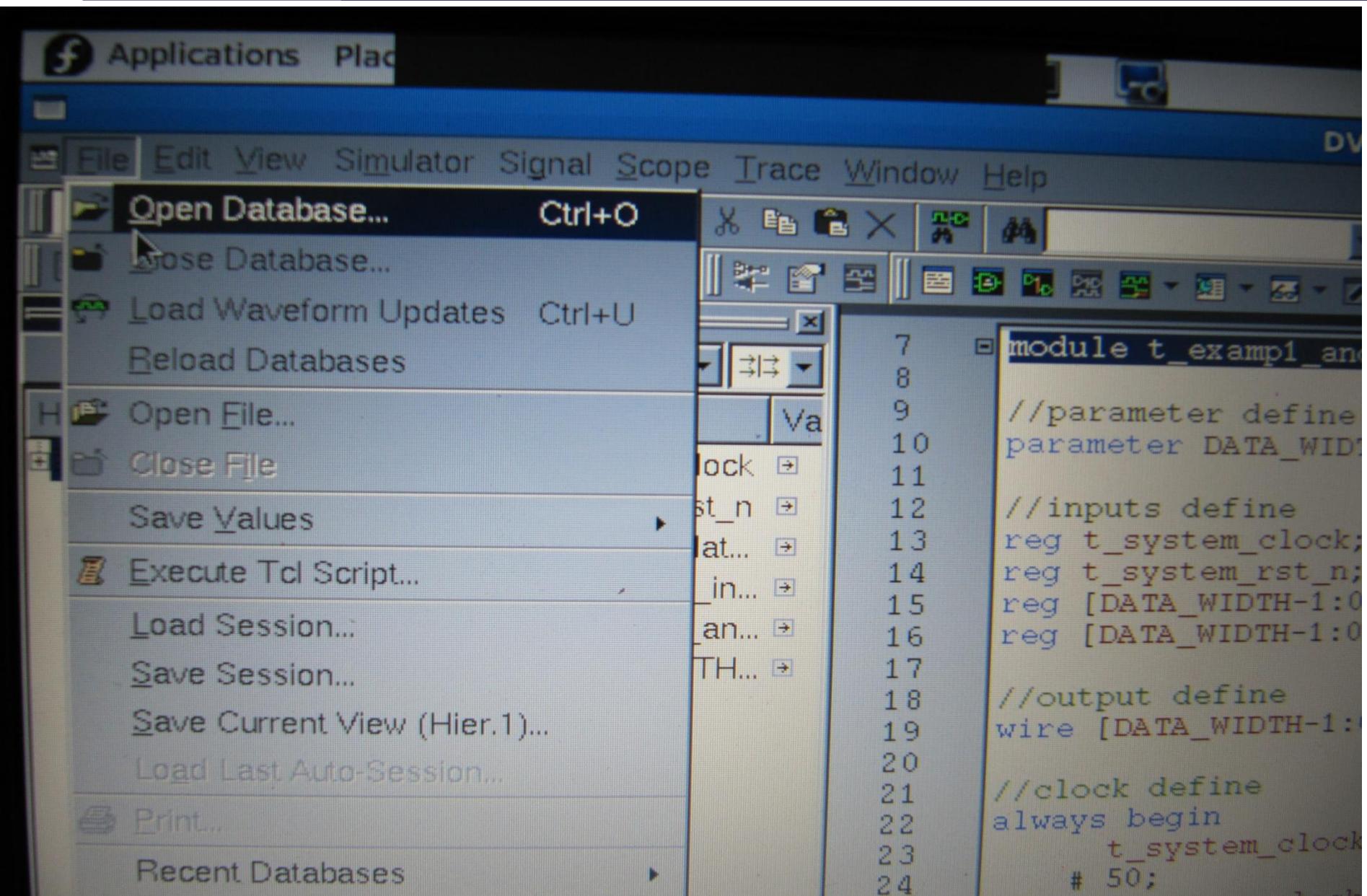
Fri Mar 22, 11:48 PM phamdanglam

File Edit View Terminal Help

```
/home/lampham/Work/06_Lap/01_VCS  
csrc design exempl_and_gate.vpd list_file simv simv.daidir t_exempl_and_gate.v  
[lampham@lampham 01_VCS]$ dve &
```

Use DVE tool to open the wave form

How to load the wave form?





How to load the wave form?

DVE - TopLevel.1 - [Hier.1]

Trace Window Help

File Edit View Insert Options Tools Reports Help

module t_exampl_and_gate;

//parameter define

parameter DATA_WIDTH = 8;

//inputs define

Open Database

Lock in: /home/lampham/Work/06_Lap/01_VCS/

File name: examp1_and_gate.vpd

File type: Database Files (*.vpd; *.vcd; *.dump; *.evcd)

Designator: V2

Time range from: to: Time Range

t_exampl_and_gate.v

.. design

DVEfiles simv.daidir

csrc examp1_and_gate.vpd

Open Cancel

This screenshot shows a software interface for a digital verification environment (DVE). The main window displays Verilog code for a module named 't_exampl_and_gate'. A modal dialog box titled 'Open Database' is open, prompting the user to select a database file. The 'Lock in' field contains the path '/home/lampham/Work/06_Lap/01_VCS/'. The file list shows several directories ('..', 'design', 'DVEfiles', 'simv.daidir', 'csrc') and one database file, 'examp1_and_gate.vpd', which is highlighted with a blue selection bar. Below the list, there are fields for 'File name:' (set to 'examp1_and_gate.vpd'), 'File type:' (set to 'Database Files (*.vpd; *.vcd; *.dump; *.evcd)'), 'Designator:' (set to 'V2'), and time range controls ('Time range from:' and 'to:'). At the bottom right of the dialog are 'Open' and 'Cancel' buttons.



How to load the wave form?

Applications Places System Fri Mar 22, 11:50 PM phamdanglam

DVE - TopLevel.1 - [Source.1 - t_exampl_and_gate: t_exampl_and_gate.v]

File Edit View Simulator Signal Scope Trace Window Help

0 x1s

V1 * Hierarchy t_exampl_and_gate Module Variable Va

```
7 module t_exampl_and_gate;
8
9 //parameter define
10 parameter DATA_WIDTH = 8;
11
12 //inputs define
13 reg t_system_clock;
14 reg t_system_rst_n;
15 reg [DATA_WIDTH-1:0] t_second_data_in;
16 reg [DATA_WIDTH-1:0] t_first_data_in;
17
18 //output define
19 wire [DATA_WIDTH-1:0] t_data_out_and_gate;
20
21 //clock define
22 always begin
23     t_system_clock = 1'b0;
24     # 50;
25     t_system_clock = 1'b1;
26     # 50;
27 end
```

/home/lampham/Work/06_Lap/01_VCS//t_exampl_and_gate.v

7 Reuse

t_exampl_and_gate t_exampl_and_gate.v

Log History

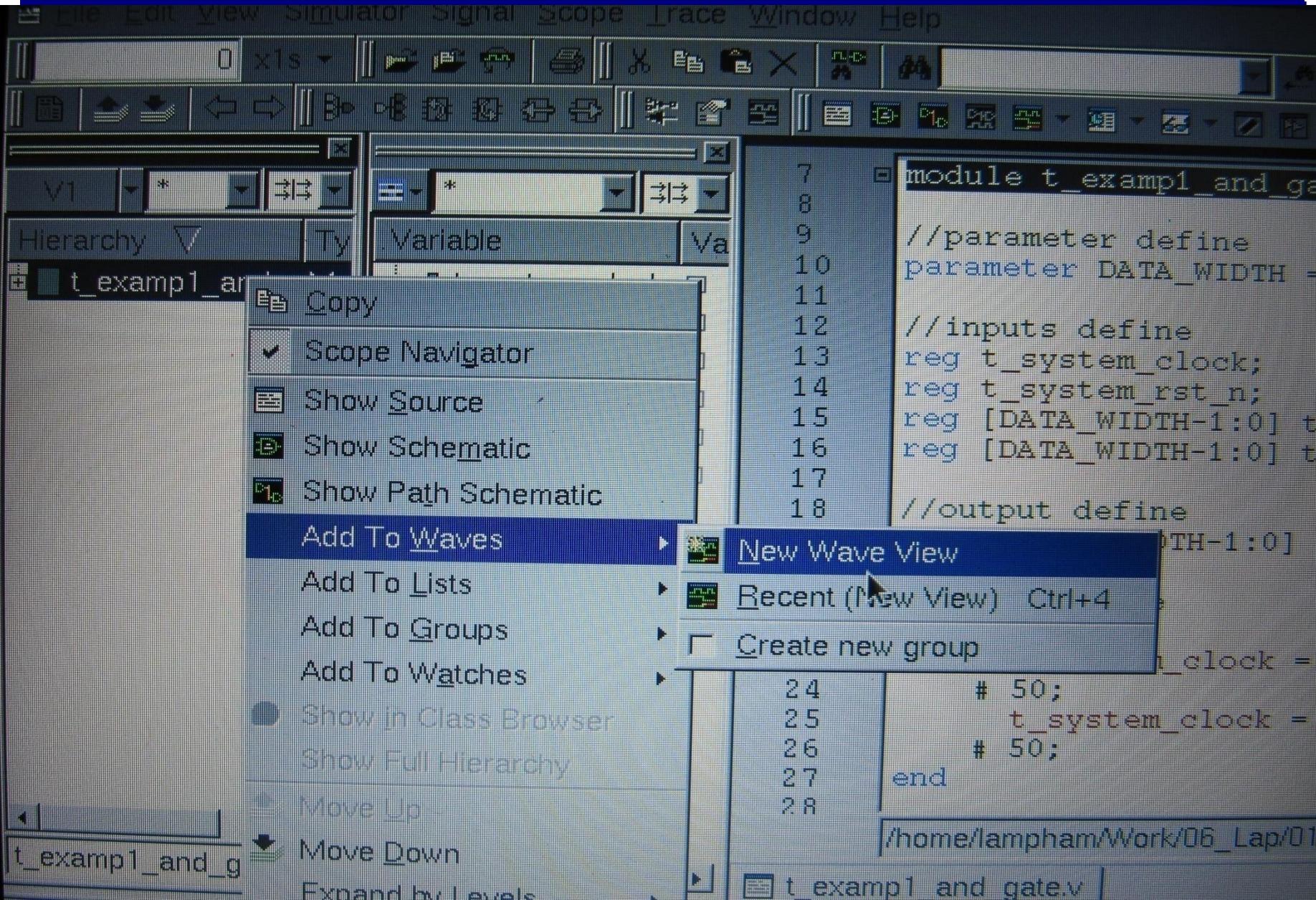
dve>

.v (New Volum...) DVE - TopLevel.1 - [So...]

N/A N/A

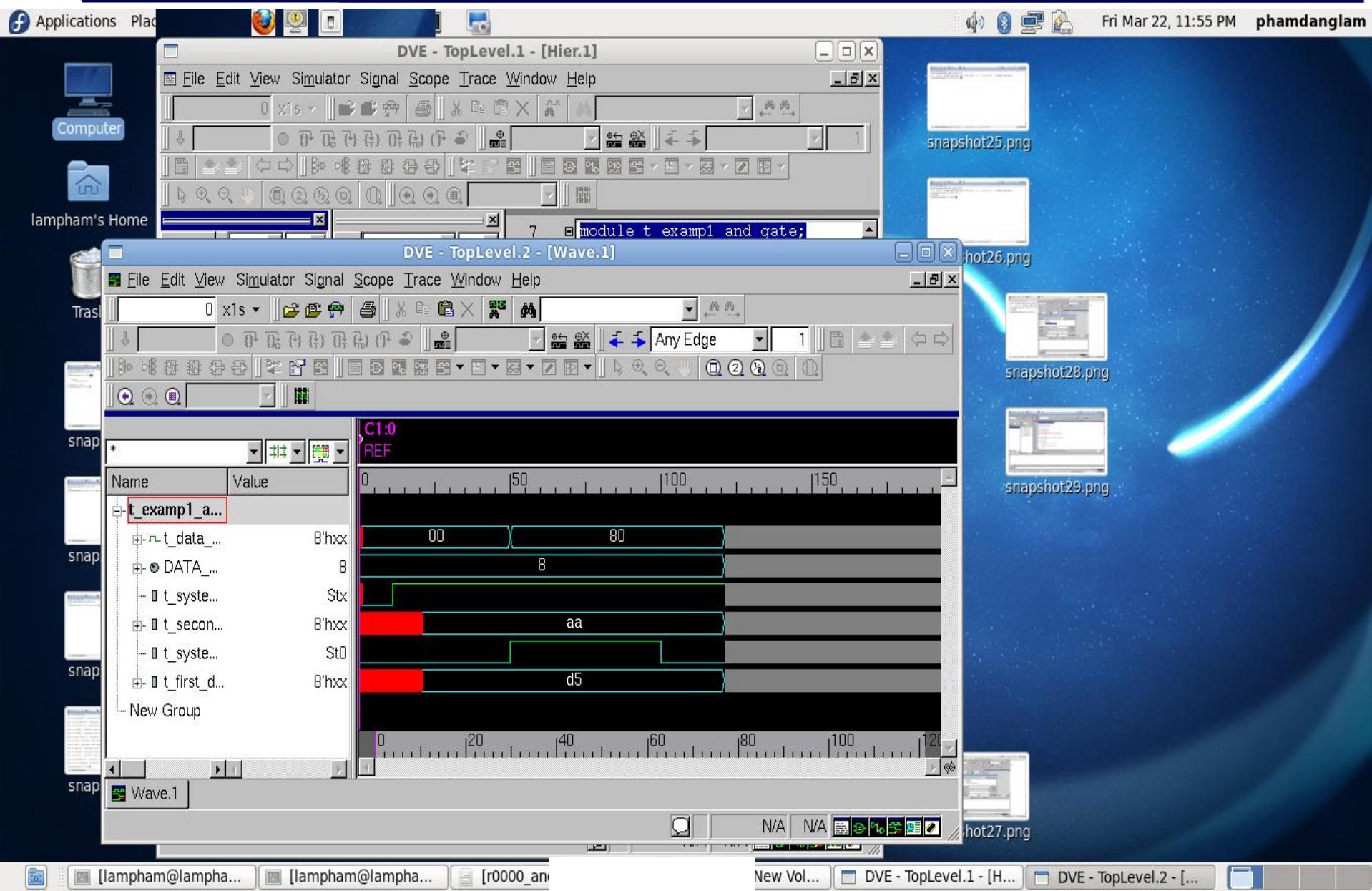


How to load the wave form?



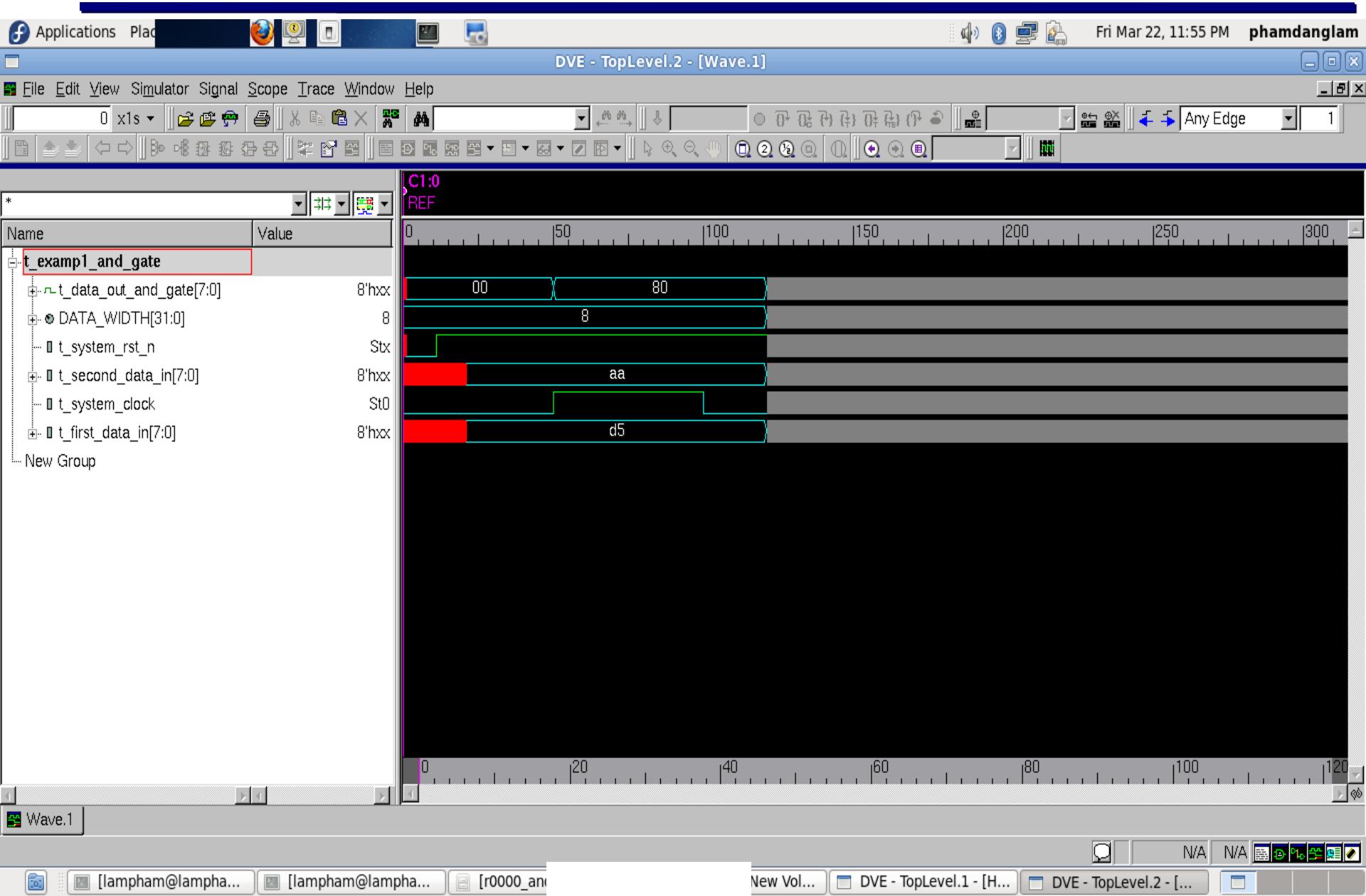


How to load the wave form?



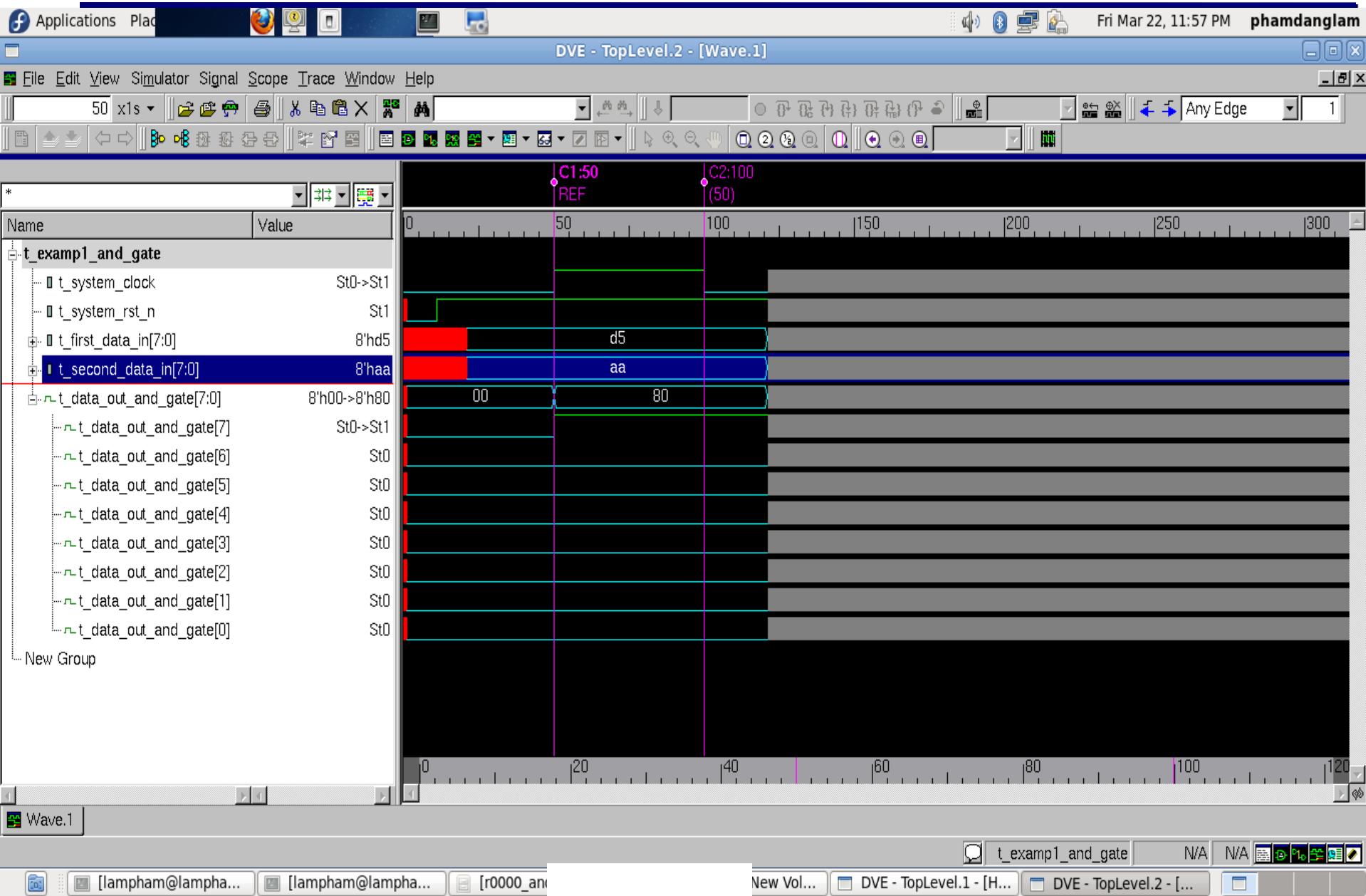


How to load the wave form?

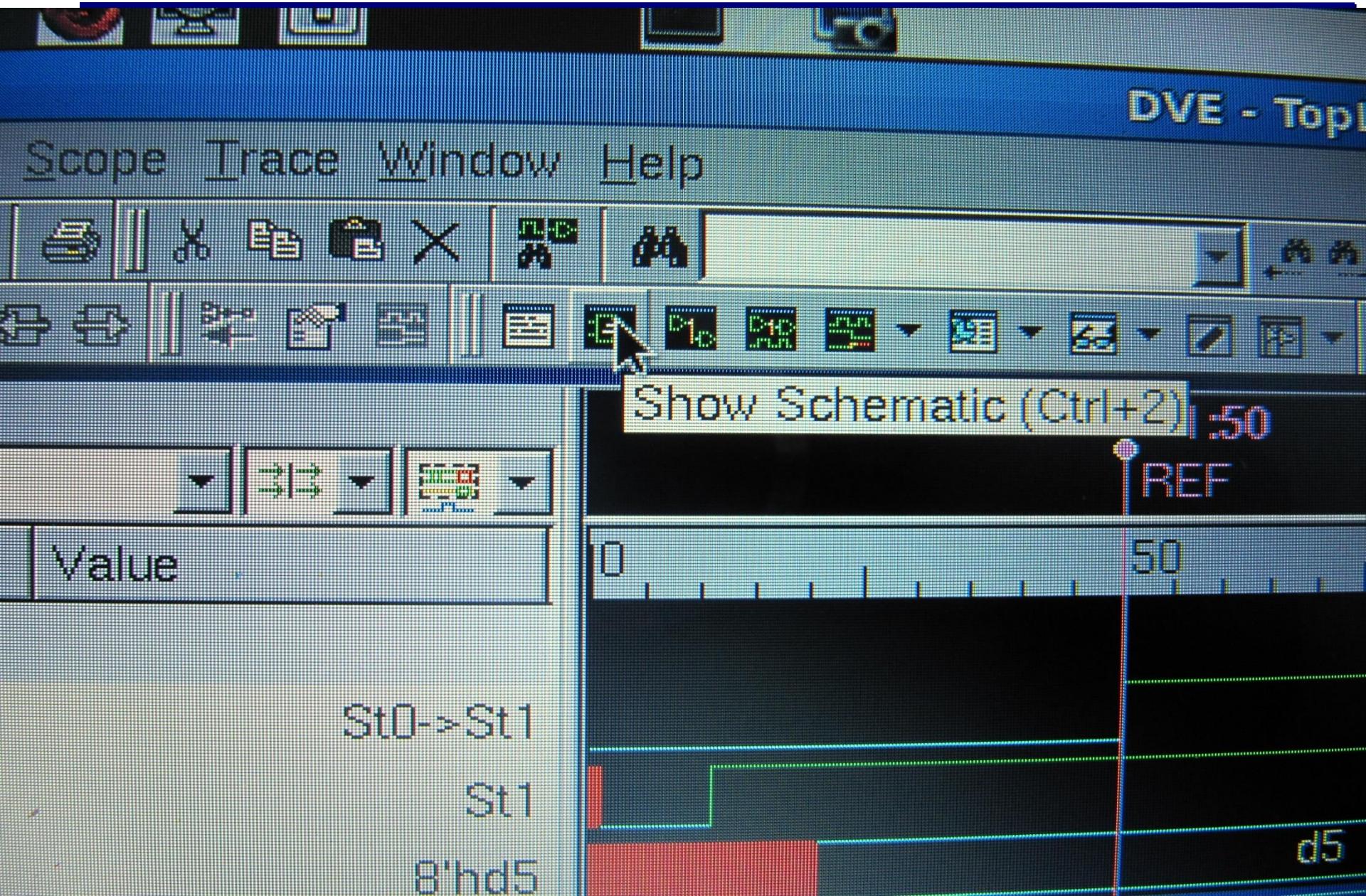




How to load the wave form?



How to load the wave form?





How to load the wave form?

Screenshot of a DVE (Digital Verification Environment) interface showing a schematic diagram of an AND gate circuit.

The schematic diagram shows the following components and connections:

- Inputs: system_clock, system_rst_n, fist_data_in[7:0], second_data_in[7:0], data_out_and_gate.
- Logic: AND gates (~a_out_and_gate), inverter (~nd_data_in), and a clock buffer (*p@25).
- Outputs: system_clock, system_rst_n, fist_data_in[7:0], second_data_in[7:0], ~a_out_and_gate, and data_out_and_gate.

The variable browser on the left lists the following variables:

- system_clock
- system_rst_n
- fist_data_in[7:0]
- second_data_in[7:0]
- data_out_and_gate
- pre_data_out...
- DATA_WIDTH...

The bottom log window shows the following messages:

```
>Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/generic.sdb'
>Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/vcs.sdb'
>Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/vcs.sdb'
>Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/vcs.sdb'
>Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/generic.sdb'
```



How to load the wave form?

Screenshot of the Synopsys Design Environment (DVE) interface showing a schematic diagram and waveform viewer.

The top menu bar includes: Applications, Place, File, Edit, View, Simulator, Signal, Scope, Trace, Window, Help.

The title bar shows: DVE - TopLevel.1 - [Schematic.1 t_exampl_and_gate].

The status bar indicates: Fri Mar 22, 11:58 PM phamdanglam

The left pane displays the Hierarchy and Variable browser. The Variable browser lists:

- system_clock
- system_rst_n
- + fist_data_in[7:0]
- + second_data_...
- > data_out_and...
- +> pre_data_out_...
- > DATA_WIDTH...

The main workspace shows a schematic diagram of a logic circuit. The circuit consists of several components and their connections:

- Inputs: fist_data_in[7:0], second_data_in, ~rst_data_in, t_system_clock.
- Intermediate signals: t_system_rst_n, ~second_data_in, t_first_data_in, ~rst_data_in, t_system_block.
- Logic blocks: ~em_rst_n, ~second_data_in, ~rst_data_in, ~em_clock, ~and_gate, ~data_in.
- Outputs: examp1_and_gate, t_exampl_and_gate.

The waveform viewer on the right shows waveforms for variables: *p@37, *p@51, *p@43, *p@22, and t_exampl_and_gate_01.

The bottom left pane shows the command history:

```
>Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/generic.sdb'  
Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/vcs.sdb'  
Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/vcs.sdb'  
Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/vcs.sdb'  
Loading db file '/home/lampham/synopsys/VCS_D-2010.06-SP1/gui/dve/libraries/syn/generic.sdb'
```

The bottom right pane shows the log history:

```
dve>
```

The bottom navigation bar includes: New Vol..., DVE - TopLevel.1 - [S...], DVE - TopLevel.2 - [...].



Q & A