**Lab1:**

1. **EX01\_a**

#!/bin/bash

#============== SET DIRECTORY =================

set search\_path "./../02\_library"

set osearch\_path [ concat $search\_path \

]

#============== ADD THE LIBRARY ================

set target\_library "pdk180nm\_tt\_1p8v\_25c.db"

set link\_library "\* $target\_library"

set synthesis\_library standard.sldb

#============= ANALYSE DESIGN ==================

analyze -format verilog "./../01\_rtl/ex01.v"

elaborate ex01\_a

current\_design ex01\_a

#============= CONSTRAIN FOR DESIGN ============

#create\_clock -name clk -period 1000 {clk}

#set\_input\_delay -max 10 -clock clk [all\_inputs]

#set\_input\_delay -min 1 -clock clk [all\_inputs]

#set\_output\_delay -max 10 -clock clk [all\_outputs]

#set\_output\_delay -min 1 -clock clk [all\_outputs]

#set\_wire\_load\_model -name "zero-wire-load-model"

set\_wire\_load\_model -name "pdk\_bk\_v1.00"

#set\_wire\_load\_model -name "pdk\_bk\_v1.01"

#set\_wire\_load\_model -name "pdk\_bk\_v1.02"

#set\_wire\_load\_model -name "pdk\_bk\_v1.03"

#set\_wire\_load\_model -name "pdk\_bk\_v1.04"

#set\_wire\_load\_model -name "pdk\_bk\_v1.05"

#============= SYNTHESIZE========================

compile\_ultra

#============= REPORT PERFORMANCE ===============

report\_area >> syn.log

report\_timing >> syn.log

report\_power >> syn.log

report\_constraint >> syn.log

write -f ddc -o ./../04\_gate/ex01.ddc

write -format verilog -hierarchy -output ./../04\_gate/ex01.netlist.v

write\_sdf ./../04\_gate/ex01.sdf

quit

* **Kết quả synthesis**

Error: Current design is not defined. (UID-4)

0

Error: Current design is not defined. (UID-4)

0

Error: Current design is not defined. (UID-4)

0

Error: Current design is not defined. (UID-4)

0

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : area

Design : ex01\_a

Version: G-2012.06-SP2

Date : Fri Jan 4 23:18:41 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Information: Updating design information... (UID-85)

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex01a/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Number of ports: 9

Number of nets: 15

Number of cells: 7

Number of combinational cells: 7

Number of sequential cells: 0

Number of macros: 0

Number of buf/inv: 3

Number of references: 3

Combinational area: 414.375008

Buf/Inv area: 90.873001

Noncombinational area: 0.000000

Net Interconnect area: 269.334697

Total cell area: 414.375008

Total area: 683.709704

1

* Total area của design được tạo nên từ total cell area và net interconnect area. Trong đó thì total cell area chỉ bao gồm các cell combinational logic. Do đó thiết kế này diện tích chỉ bao gồm diện tích của các cell combinational logic and net connection của mạch.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : ex01\_a

Version: G-2012.06-SP2

Date : Fri Jan 4 23:18:41 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: w (input port)

Endpoint: m (output port)

Path Group: (none)

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex01\_a pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 r

w (in) 0.00 0.00 r

U10/Y (AOI22X1) 0.27 0.27 f

U13/Y (AOI22X1) 0.22 0.49 r

U14/Y (AO22X1) 0.17 0.66 r

m (out) 0.00 0.66 r

data arrival time 0.66

-----------------------------------------------------------

(Path is unconstrained)

1

Loading db file '/home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex01a/02\_library/pdk180nm\_tt\_1p8v\_25c.db'

Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)

Warning: There is no defined clock in the design. (PWR-80)

Warning: Design has unannotated primary inputs. (PWR-414)

* Mạch chỉ bao gồm các cell combinational logic nên không có timing constraint. Bên cạnh đó, report timing có thể trích xuất bằng report timing cho loại in to out, nghĩa là timing từ input pin của thiết kế qua các cell combinational logic và output ra output pin mà không qua bất cứ một flipflop nào.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : power

-analysis\_effort low

Design : ex01\_a

Version: G-2012.06-SP2

Date : Fri Jan 4 23:18:41 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex01a/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Design Wire Load Model Library

------------------------------------------------

ex01\_a pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Global Operating Voltage = 1.8

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000pf

Time Units = 1ns

Dynamic Power Units = 1mW (derived from V,C,T units)

Leakage Power Units = 1pW

Cell Internal Power = -126.2200 nW (110%)

Net Switching Power = 11.0838 nW (-9%)

---------

Total Dynamic Power = -115.1362 nW (100%)

Cell Leakage Power = 160.2893 pW

Information: report\_power power group summary does not include estimated clock tree power. (PWR-789)

Internal Switching Leakage Total

Power Group Power Power Power Power ( % ) Attrs

--------------------------------------------------------------------------------------------------

io\_pad 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

memory 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

black\_box 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

clock\_network 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

register 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

sequential 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

combinational -1.2622e-04 1.1084e-05 160.2893 -1.1498e-04

( 100.00%)

--------------------------------------------------------------------------------------------------

Total -1.2622e-04 mW 1.1084e-05 mW 160.2893 pW -1.1498e-04 mW

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : constraint

Design : ex01\_a

Version: G-2012.06-SP2

Date : Fri Jan 4 23:18:41 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Constraint Cost

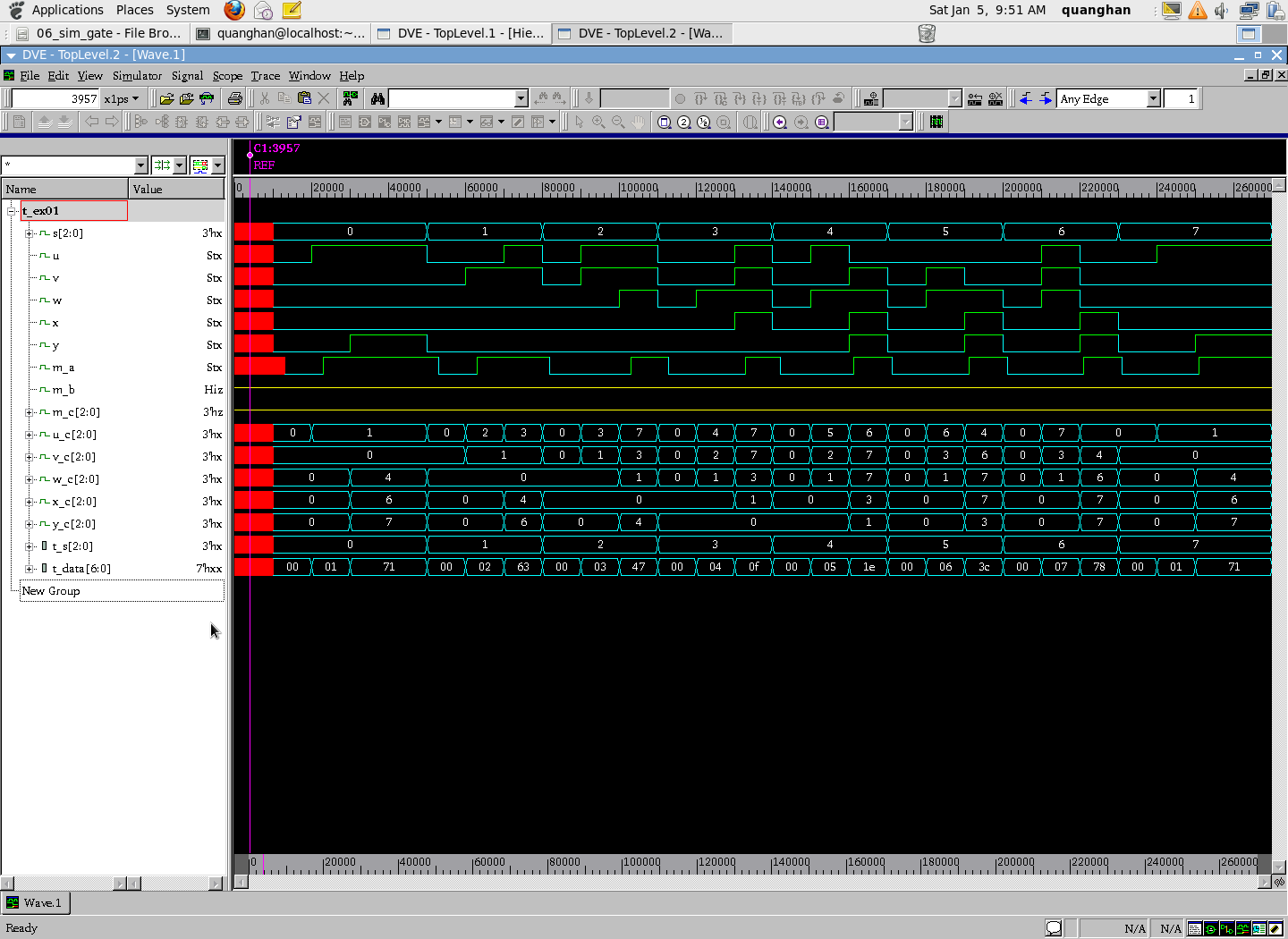
-----------------------------------------------------

max\_transition 0.00 (MET)

max\_capacitance 0.00 (MET)

1

* Power của mạch chỉ rơi trên các cell combinational logic. Song bên cạnh đó có một phần nhỏ power là dynamic power và leakage power (không đáng kể)
* Gate simulation



1. **Ex01\_b**

* **Constrain file:**

#!/bin/bash

#============== SET DIRECTORY =================

set search\_path "./../02\_library"

set osearch\_path [ concat $search\_path \

]

#============== ADD THE LIBRARY ================

set target\_library "pdk180nm\_tt\_1p8v\_25c.db"

set link\_library "\* $target\_library"

set synthesis\_library standard.sldb

#============= ANALYSE DESIGN ==================

analyze -format verilog "./../01\_rtl/ex01.v"

elaborate ex01\_b

current\_design ex01\_b

#============= CONSTRAIN FOR DESIGN ============

#create\_clock -name clk -period 1000 {clk}

#set\_input\_delay -max 10 -clock clk [all\_inputs]

#set\_input\_delay -min 1 -clock clk [all\_inputs]

#set\_output\_delay -max 10 -clock clk [all\_outputs]

#set\_output\_delay -min 1 -clock clk [all\_outputs]

#set\_wire\_load\_model -name "zero-wire-load-model"

set\_wire\_load\_model -name "pdk\_bk\_v1.00"

#set\_wire\_load\_model -name "pdk\_bk\_v1.01"

#set\_wire\_load\_model -name "pdk\_bk\_v1.02"

#set\_wire\_load\_model -name "pdk\_bk\_v1.03"

#set\_wire\_load\_model -name "pdk\_bk\_v1.04"

#set\_wire\_load\_model -name "pdk\_bk\_v1.05"

#============= SYNTHESIZE========================

compile\_ultra

#============= REPORT PERFORMANCE ===============

report\_area >> syn.log

report\_timing >> syn.log

report\_power >> syn.log

report\_constraint >> syn.log

write -f ddc -o ./../04\_gate/ex01.ddc

write -format verilog -hierarchy -output ./../04\_gate/ex01.netlist.v

write\_sdf ./../04\_gate/ex01.sdf

quit

* **Synthesis log file**

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : area

Design : ex01\_b

Version: G-2012.06-SP2

Date : Fri Jan 4 23:26:11 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Information: Updating design information... (UID-85)

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex01b/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Number of ports: 9

Number of nets: 15

Number of cells: 7

Number of combinational cells: 7

Number of sequential cells: 0

Number of macros: 0

Number of buf/inv: 3

Number of references: 3

Combinational area: 414.375008

Buf/Inv area: 90.873001

Noncombinational area: 0.000000

Net Interconnect area: 269.334697

Total cell area: 414.375008

Total area: 683.709704

1

* Total area của design được tạo nên từ total cell area và net interconnect area. Trong đó thì total cell area chỉ bao gồm các cell combinational logic. Do đó thiết kế này diện tích chỉ bao gồm diện tích của các cell combinational logic and net connection của mạch.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : ex01\_b

Version: G-2012.06-SP2

Date: Fri Jan 4 23:26:11 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: w[0] (input port)

Endpoint: m[0] (output port)

Path Group: (none)

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex01\_b pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 r

w[0] (in) 0.00 0.00 r

U10/Y (AOI22X1) 0.27 0.27 f

U13/Y (AOI22X1) 0.22 0.49 r

U14/Y (AO22X1) 0.17 0.66 r

m[0] (out) 0.00 0.66 r

data arrival time 0.66

-----------------------------------------------------------

(Path is unconstrained)

1

Loading db file '/home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex01b/02\_library/pdk180nm\_tt\_1p8v\_25c.db'

Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)

Warning: There is no defined clock in the design. (PWR-80)

Warning: Design has unannotated primary inputs. (PWR-414)

* Mạch chỉ bao gồm các cell combinational logic nên không có timing constraint. Bên cạnh đó, report timing có thể trích xuất bằng report timing cho loại in to out, nghĩa là timing từ input pin của thiết kế qua các cell combinational logic và output ra output pin mà không qua bất cứ một flipflop nào.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : power

-analysis\_effort low

Design : ex01\_b

Version: G-2012.06-SP2

Date : Fri Jan 4 23:26:11 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex01b/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Design Wire Load Model Library

------------------------------------------------

ex01\_b pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Global Operating Voltage = 1.8

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000pf

Time Units = 1ns

Dynamic Power Units = 1mW (derived from V,C,T units)

Leakage Power Units = 1pW

Cell Internal Power = -126.2200 nW (110%)

Net Switching Power = 11.0838 nW (-9%)

---------

Total Dynamic Power = -115.1362 nW (100%)

Cell Leakage Power = 160.2893 pW

Information: report\_power power group summary does not include estimated clock tree power. (PWR-789)

Internal Switching Leakage Total

Power Group Power Power Power Power ( % ) Attrs

--------------------------------------------------------------------------------------------------

io\_pad 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

memory 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

black\_box 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

clock\_network 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

register 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

sequential 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

combinational -1.2622e-04 1.1084e-05 160.2893 -1.1498e-04

( 100.00%)

--------------------------------------------------------------------------------------------------

Total -1.2622e-04 mW 1.1084e-05 mW 160.2893 pW -1.1498e-04 mW

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : constraint

Design : ex01\_b

Version: G-2012.06-SP2

Date : Fri Jan 4 23:26:11 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Constraint Cost

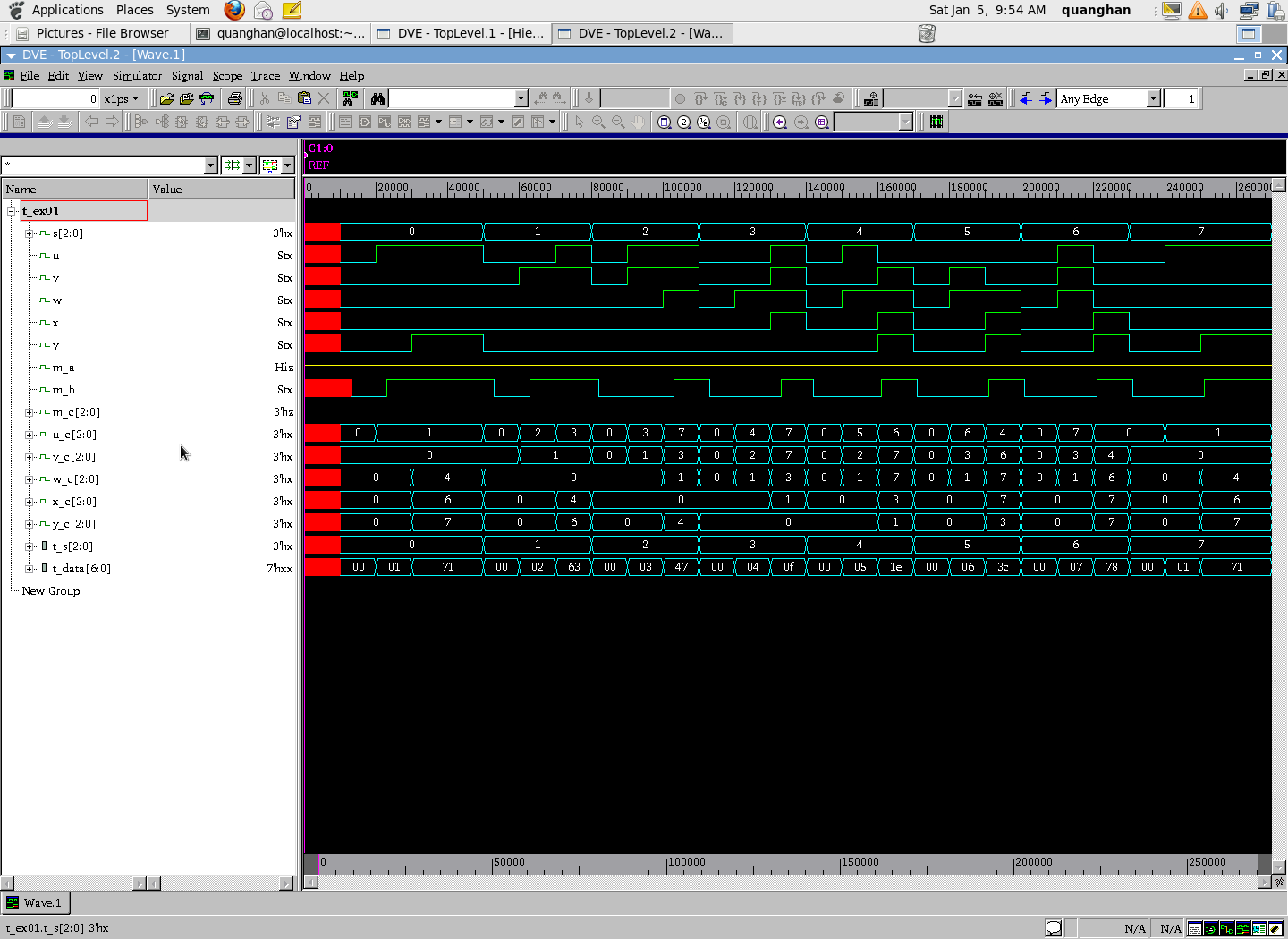
-----------------------------------------------------

max\_transition 0.00 (MET)

max\_capacitance 0.00 (MET)

1

* Power của mạch chỉ rơi trên các cell combinational logic. Song bên cạnh đó có một phần nhỏ power là dynamic power và leakage power (không đáng kể)
* Gate simulation



1. **EX01\_c**

* **Constraint file:**

#!/bin/bash

#============== SET DIRECTORY =================

set search\_path "./../02\_library"

set osearch\_path [ concat $search\_path \

]

#============== ADD THE LIBRARY ================

set target\_library "pdk180nm\_tt\_1p8v\_25c.db"

set link\_library "\* $target\_library"

set synthesis\_library standard.sldb

#============= ANALYSE DESIGN ==================

analyze -format verilog "./../01\_rtl/ex01.v"

elaborate ex01\_c

current\_design ex01\_c

#============= CONSTRAIN FOR DESIGN ============

#create\_clock -name clk -period 1000 {clk}

#set\_input\_delay -max 10 -clock clk [all\_inputs]

#set\_input\_delay -min 1 -clock clk [all\_inputs]

#set\_output\_delay -max 10 -clock clk [all\_outputs]

#set\_output\_delay -min 1 -clock clk [all\_outputs]

#set\_wire\_load\_model -name "zero-wire-load-model"

set\_wire\_load\_model -name "pdk\_bk\_v1.00"

#set\_wire\_load\_model -name "pdk\_bk\_v1.01"

#set\_wire\_load\_model -name "pdk\_bk\_v1.02"

#set\_wire\_load\_model -name "pdk\_bk\_v1.03"

#set\_wire\_load\_model -name "pdk\_bk\_v1.04"

#set\_wire\_load\_model -name "pdk\_bk\_v1.05"

#============= SYNTHESIZE========================

compile\_ultra

#============= REPORT PERFORMANCE ===============

report\_area >> syn.log

report\_timing >> syn.log

report\_power >> syn.log

report\_constraint >> syn.log

write -f ddc -o ./../04\_gate/ex01.ddc

write -format verilog -hierarchy -output ./../04\_gate/ex01.netlist.v

write\_sdf ./../04\_gate/ex01.sdf

quit

* **Synthesis log file**

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : area

Design : ex01\_c

Version: G-2012.06-SP2

Date : Fri Jan 4 23:33:17 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Information: Updating design information... (UID-85)

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex01c/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Number of ports: 21

Number of nets: 36

Number of cells: 18

Number of combinational cells: 18

Number of sequential cells: 0

Number of macros: 0

Number of buf/inv: 2

Number of references: 5

Combinational area: 1117.479019

Buf/Inv area: 60.582001

Noncombinational area: 0.000000

Net Interconnect area: 740.670411

Total cell area: 1117.479019

Total area: 1858.149430

1

* Total area của design được tạo nên từ total cell area và net interconnect area. Trong đó thì total cell area chỉ bao gồm các cell combinational logic. Do đó thiết kế này diện tích chỉ bao gồm diện tích của các cell combinational logic and net connection của mạch.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : ex01\_c

Version: G-2012.06-SP2

Date : Fri Jan 4 23:33:17 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: x[2] (input port)

Endpoint: m[2] (output port)

Path Group: (none)

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex01\_c pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 r

x[2] (in) 0.00 0.00 r

U34/Y (AOI22X1) 0.27 0.27 f

U35/Y (AOI21X1) 0.19 0.45 r

U36/Y (AO21X1) 0.17 0.62 r

m[2] (out) 0.00 0.62 r

data arrival time 0.62

-----------------------------------------------------------

(Path is unconstrained)

1

Loading db file '/home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex01c/02\_library/pdk180nm\_tt\_1p8v\_25c.db'

Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)

Warning: There is no defined clock in the design. (PWR-80)

Warning: Design has unannotated primary inputs. (PWR-414)

* Mạch chỉ bao gồm các cell combinational logic nên không có timing constraint. Bên cạnh đó, report timing có thể trích xuất bằng report timing cho loại in to out, nghĩa là timing từ input pin của thiết kế qua các cell combinational logic và output ra output pin mà không qua bất cứ một flipflop nào.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : power

-analysis\_effort low

Design : ex01\_c

Version: G-2012.06-SP2

Date : Fri Jan 4 23:33:18 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex01c/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Design Wire Load Model Library

------------------------------------------------

ex01\_c pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Global Operating Voltage = 1.8

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000pf

Time Units = 1ns

Dynamic Power Units = 1mW (derived from V,C,T units)

Leakage Power Units = 1pW

Cell Internal Power = -276.8700 nW (112%)

Net Switching Power = 30.6058 nW (-11%)

---------

Total Dynamic Power = -246.2641 nW (100%)

Cell Leakage Power = 530.0533 pW

Information: report\_power power group summary does not include estimated clock tree power. (PWR-789)

Internal Switching Leakage Total

Power Group Power Power Power Power ( % ) Attrs

--------------------------------------------------------------------------------------------------

io\_pad 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

memory 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

black\_box 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

clock\_network 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

register 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

sequential 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

combinational -2.7687e-04 3.0606e-05 530.0533 -2.4573e-04

( 100.00%)

--------------------------------------------------------------------------------------------------

Total -2.7687e-04 mW 3.0606e-05 mW 530.0533 pW -2.4573e-04 mW

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : constraint

Design : ex01\_c

Version: G-2012.06-SP2

Date : Fri Jan 4 23:33:18 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Constraint Cost

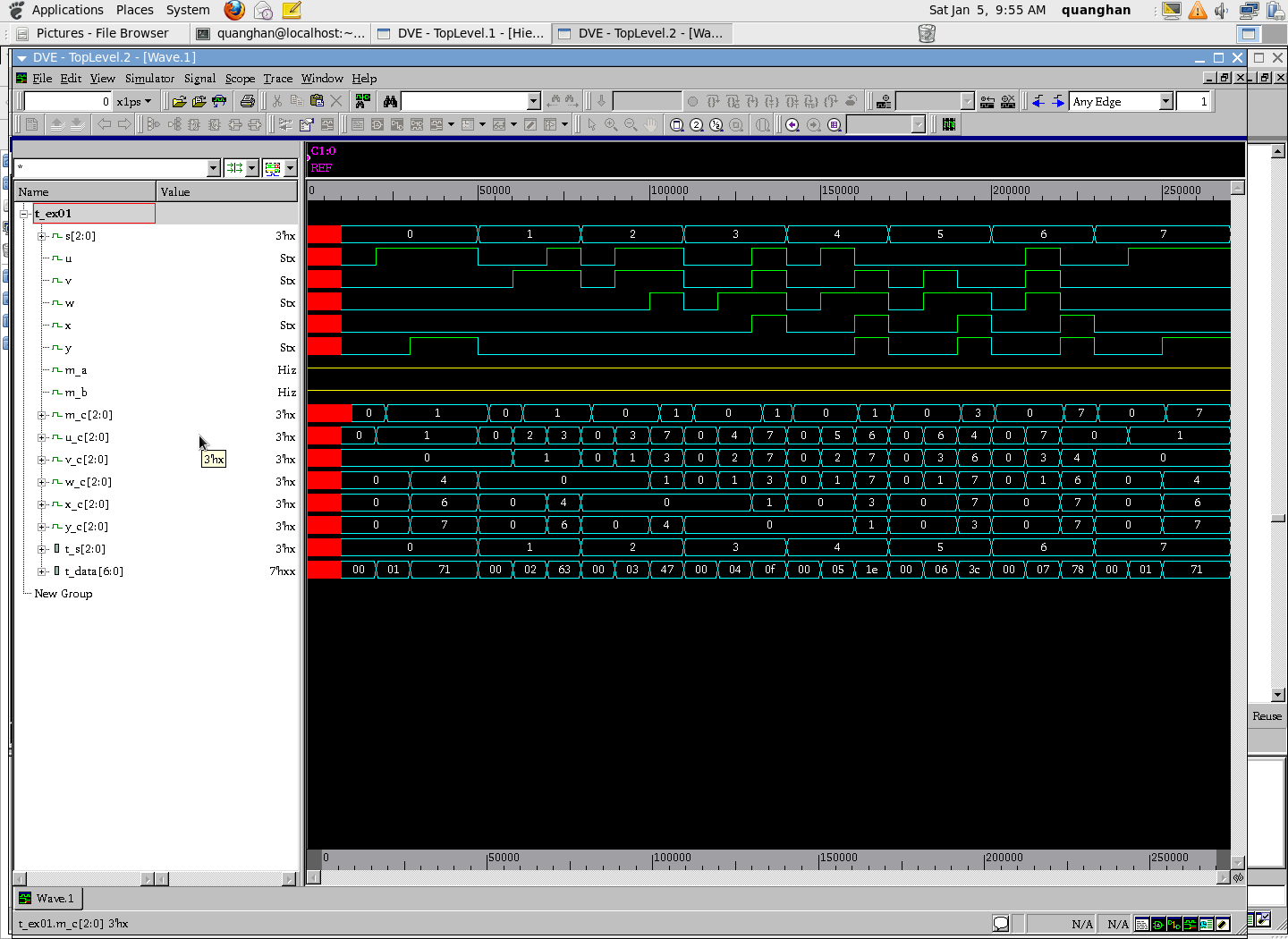
-----------------------------------------------------

max\_transition 0.00 (MET)

max\_capacitance 0.00 (MET)

1

* Power của mạch chỉ rơi trên các cell combinational logic. Song bên cạnh đó có một phần nhỏ power là dynamic power và leakage power (không đáng kể)
* Gate simulation



**Lab2:**

* **Constraint file**

#!/bin/bash

#============== SET DIRECTORY =================

set search\_path "./../02\_library"

set osearch\_path [ concat $search\_path \

]

#============== ADD THE LIBRARY ================

set target\_library "pdk180nm\_tt\_1p8v\_25c.db"

set link\_library "\* $target\_library"

set synthesis\_library standard.sldb

#============= ANALYSE DESIGN ==================

analyze -format verilog "./../01\_rtl/ex02.v"

elaborate ex02

current\_design ex02

#============= CONSTRAIN FOR DESIGN ============

create\_clock -name clk -period 20 {clk}

set\_load 0 [all\_inputs]

set\_load 1 [all\_outputs]

set\_input\_delay -max 1 -clock clk [all\_inputs]

set\_output\_delay -max 0 -clock clk [all\_outputs]

#set\_wire\_load\_model -name "zero-wire-load-model"

set\_wire\_load\_model -name "pdk\_bk\_v1.00"

#set\_wire\_load\_model -name "pdk\_bk\_v1.01"

#set\_wire\_load\_model -name "pdk\_bk\_v1.02"

#set\_wire\_load\_model -name "pdk\_bk\_v1.03"

#set\_wire\_load\_model -name "pdk\_bk\_v1.04"

#set\_wire\_load\_model -name "pdk\_bk\_v1.05"

#============= SYNTHESIZE========================

compile\_ultra

#============= REPORT PERFORMANCE ===============

report\_area >> syn.log

report\_timing -path\_type full -delay min >> syn.log

report\_timing -path\_type full -delay max >> syn.log

report\_power >> syn.log

report\_constraint >> syn.log

write -f ddc -o ./../04\_gate/ex02.ddc

write -format verilog -hierarchy -output ./../04\_gate/ex02.netlist.v

write\_sdf ./../04\_gate/ex02.sdf

quit

* **Synthesis log file**

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : area

Design : ex02

Version: G-2012.06-SP2

Date : Fri Jan 4 23:41:59 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Information: Updating design information... (UID-85)

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex02/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Number of ports: 26

Number of nets: 78

Number of cells: 58

Number of combinational cells: 55

Number of sequential cells: 3

Number of macros: 0

Number of buf/inv: 27

Number of references: 11

Combinational area: 2594.139038

Buf/Inv area: 817.857010

Noncombinational area: 665.039978

Net Interconnect area: 1642.941637

Total cell area: 3259.179016

Total area: 4902.120653

1

* Total area của mạch bao gồm total cell area và net interconnect area. Song bên cạnh đó total cell area bao gồm các cell combination logic và các cell flip – flop. Net connection vẫn chiếm phần lớn diện tích của mạch.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay min

-max\_paths 1

Design : ex02

Version: G-2012.06-SP2

Date : Fri Jan 4 23:41:59 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: signal/qa\_reg[1]/CK

(internal path startpoint clocked by clk)

Endpoint: led7\_out[0]

(output port clocked by clk)

Path Group: (none)

Path Type: min

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex02 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 r

signal/qa\_reg[1]/CK (DFFRHQX1) 0.00 0.00 r

signal/qa\_reg[1]/Q (DFFRHQX1) 0.08 0.08 r

U62/Y (INVX1) 0.04 0.11 f

U36/Y (AND3X1) 0.09 0.21 f

U45/Y (INVX1) 1.92 2.13 r

led7\_out[0] (out) 10.93 13.06 r

data arrival time 13.06

-----------------------------------------------------------

(Path is unconstrained)

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : ex02

Version: G-2012.06-SP2

Date : Fri Jan 4 23:41:59 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: signal/qa\_reg[2]/CK

(internal path startpoint clocked by clk)

Endpoint: led7\_out[0]

(output port clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex02 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.00 0.00 r

signal/qa\_reg[2]/CK (DFFRHQX1) 0.00 0.00 r

signal/qa\_reg[2]/Q (DFFRHQX1) 0.08 0.08 r

U71/Y (OR2X1) 0.10 0.17 r

U36/Y (AND3X1) 0.18 0.35 r

U45/Y (INVX1) 2.87 3.22 f

led7\_out[0] (out) 10.93 14.16 f

data arrival time 14.16

clock clk (rise edge) 20.00 20.00

clock network delay (ideal) 0.00 20.00

output external delay 0.00 20.00

data required time 20.00

-----------------------------------------------------------

data required time 20.00

data arrival time -14.16

-----------------------------------------------------------

slack (MET) 5.84

1

Loading db file '/home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex02/02\_library/pdk180nm\_tt\_1p8v\_25c.db'

Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)

Warning: Design has unannotated primary inputs. (PWR-414)

Warning: Design has unannotated sequential cell outputs. (PWR-415)

* Timing report bao gồm 2 loại timing report là in2out and reg2out. Đối với report in2out không có constraint về timing vì đây là path chỉ toàn những cell combinational logic nên timing không cần constraint vì data truyền sẽ không bao giờ mất mát. Chúng ta thấy report reg2out bắt đầu tại cell signal/qa\_reg[2]/CK (DFFRHQX1) và kết thúc tại điểm led7\_out[0] (out) bên cạnh đó đây là path có critical timing nên report timing sẽ report ra, ta thấy path này met về timing có nghĩa là data truyền trên path này sẽ không bao giờ thất thoát dữ liệu, thông số của clock network delay và input external delay đều lý tưởng bằng 0.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : power

-analysis\_effort low

Design : ex02

Version: G-2012.06-SP2

Date : Fri Jan 4 23:42:00 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex02/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Design Wire Load Model Library

------------------------------------------------

ex02 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Global Operating Voltage = 1.8

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000pf

Time Units = 1ns

Dynamic Power Units = 1mW (derived from V,C,T units)

Leakage Power Units = 1pW

Cell Internal Power = -153.3996 nW (0%)

Net Switching Power = 100.6000 uW (100%)

---------

Total Dynamic Power = 100.4466 uW (100%)

Cell Leakage Power = 689.2457 nW

Internal Switching Leakage Total

Power Group Power Power Power Power ( % ) Attrs

--------------------------------------------------------------------------------------------------

io\_pad 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

memory 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

black\_box 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

clock\_network 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

register -1.9377e-06 1.1996e-06 6.8774e+05 6.8700e-04 ( 0.68%)

sequential 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

combinational -1.5146e-04 0.1006 1.5037e+03 0.1004 ( 99.32%)

--------------------------------------------------------------------------------------------------

Total -1.5340e-04 mW 0.1006 mW 6.8925e+05 pW 0.1011 mW

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : constraint

Design : ex02

Version: G-2012.06-SP2

Date : Fri Jan 4 23:42:00 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Weighted

Group (max\_delay/setup) Cost Weight Cost

-----------------------------------------------------

clk 0.00 1.00 0.00

default 0.00 1.00 0.00

-----------------------------------------------------

max\_delay/setup 0.00

Total Neg Critical

Group (critical\_range) Slack Endpoints Cost

-----------------------------------------------------

clk 0.00 0 0.00

default 0.00 0 0.00

-----------------------------------------------------

critical\_range 0.00

Constraint Cost

-----------------------------------------------------

max\_transition 14.28 (VIOLATED)

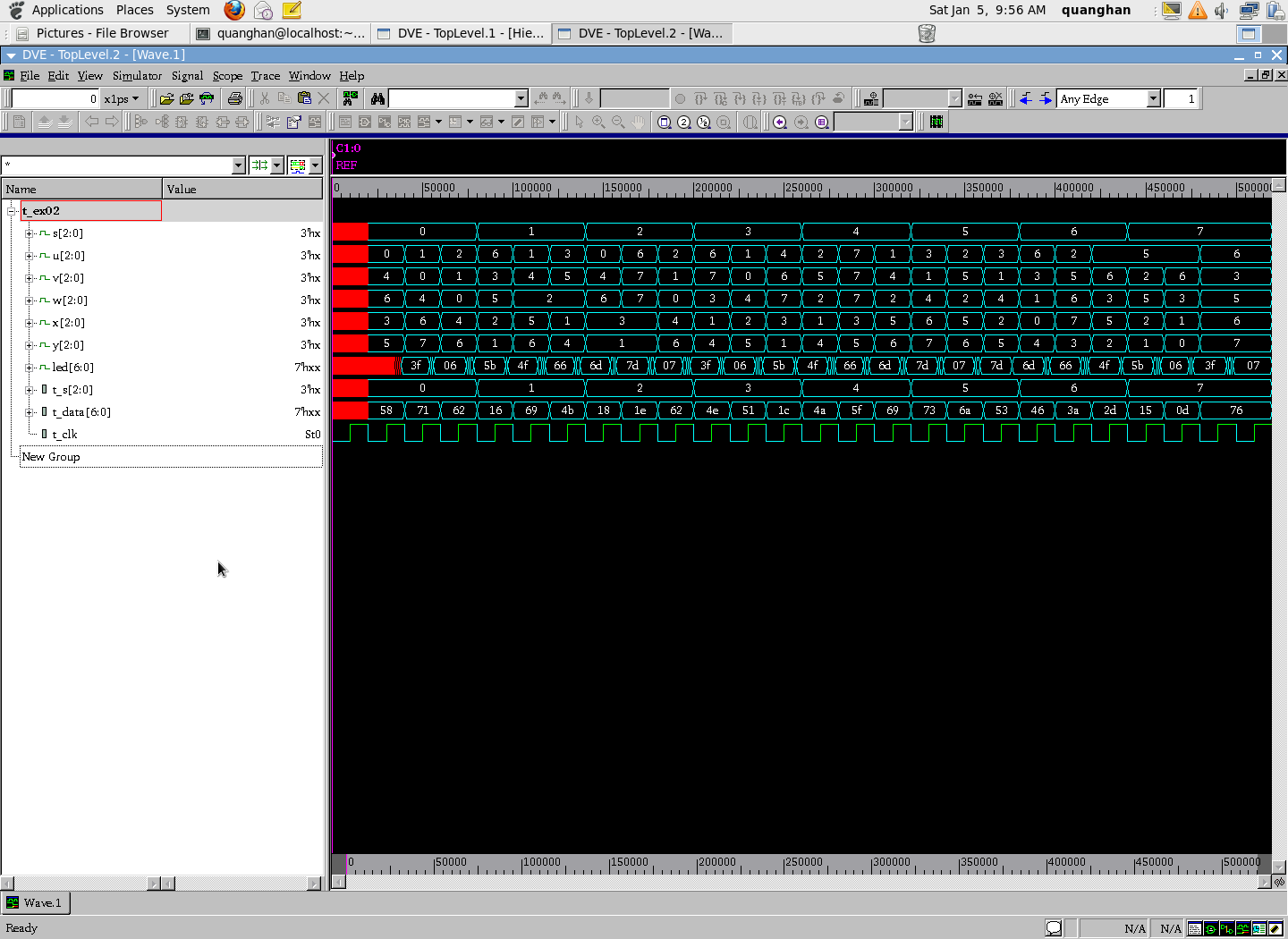
max\_capacitance 6.93 (VIOLATED)

max\_delay/setup 0.00 (MET)

critical\_range 0.00 (MET)

1

* Năng lượng tiêu tán phần lớn trong mode switching và chủ yếu tiêu tán trên các cell combinational logic. Bên cạnh đó, internal power tiêu tán chủ yếu trên các cell combinational logic. Đối với mode leakage power, năng lượng chủ yếu rơi trên các register.
* Gate simulation



**Lab3**

* **Constraint file:**

#!/bin/bash

#============== SET DIRECTORY =================

set search\_path "./../02\_library"

set osearch\_path [ concat $search\_path \

]

#============== ADD THE LIBRARY ================

set target\_library "pdk180nm\_tt\_1p8v\_25c.db"

set link\_library "\* $target\_library"

set synthesis\_library standard.sldb

#============= ANALYSE DESIGN ==================

analyze -format verilog "./../01\_rtl/ex03.v"

elaborate ex03

current\_design ex03

#============= CONSTRAIN FOR DESIGN ============

create\_clock -name clk -period 20 {clk}

set\_load 0 [all\_inputs]

set\_load 1 [all\_outputs]

set\_input\_delay -max 1 -clock clk [all\_inputs]

set\_output\_delay -max 0 -clock clk [all\_outputs]

#set\_wire\_load\_model -name "zero-wire-load-model"

set\_wire\_load\_model -name "pdk\_bk\_v1.00"

#set\_wire\_load\_model -name "pdk\_bk\_v1.01"

#set\_wire\_load\_model -name "pdk\_bk\_v1.02"

#set\_wire\_load\_model -name "pdk\_bk\_v1.03"

#set\_wire\_load\_model -name "pdk\_bk\_v1.04"

#set\_wire\_load\_model -name "pdk\_bk\_v1.05"

#============= SYNTHESIZE========================

compile\_ultra

#============= REPORT PERFORMANCE ===============

report\_area >> syn.log

report\_timing -path\_type full -delay min >> syn.log

report\_timing -path\_type full -delay max >> syn.log

report\_power >> syn.log

report\_constraint >> syn.log

write -f ddc -o ./../04\_gate/ex03.ddc

write -format verilog -hierarchy -output ./../04\_gate/ex03.netlist.v

write\_sdf ./../04\_gate/ex03.sdf

quit

* **Synthesis log file:**

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : area

Design : ex03

Version: G-2012.06-SP2

Date : Fri Jan 4 23:55:16 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Information: Updating design information... (UID-85)

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex03/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Number of ports: 4

Number of nets: 10

Number of cells: 7

Number of combinational cells: 3

Number of sequential cells: 4

Number of macros: 0

Number of buf/inv: 0

Number of references: 2

Combinational area: 183.790798

Buf/Inv area: 0.000000

Noncombinational area: 886.719971

Net Interconnect area: 255.867963

Total cell area: 1070.510769

Total area: 1326.378732

1

* Total area được tạo nên từ diện tích của các cell Non-combinational (Flip – flop) và net connection trong mạch.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay min

-max\_paths 1

Design : ex03

Version: G-2012.06-SP2

Date : Fri Jan 4 23:55:16 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: d\_ff\_04/q\_reg/CK

(internal path startpoint clocked by clk)

Endpoint: trigger (output port clocked by clk)

Path Group: (none)

Path Type: min

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex03 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 r

d\_ff\_04/q\_reg/CK (DFFRHQX1) 0.00 0.00 r

d\_ff\_04/q\_reg/Q (DFFRHQX1) 2.29 2.29 r

trigger (out) 10.93 13.23 r

data arrival time 13.23

-----------------------------------------------------------

(Path is unconstrained)

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : ex03

Version: G-2012.06-SP2

Date : Fri Jan 4 23:55:16 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: d\_ff\_04/q\_reg/CK

(internal path startpoint clocked by clk)

Endpoint: trigger (output port clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex03 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.00 0.00 r

d\_ff\_04/q\_reg/CK (DFFRHQX1) 0.00 0.00 r

d\_ff\_04/q\_reg/Q (DFFRHQX1) 3.04 3.04 f

trigger (out) 10.93 13.98 f

data arrival time 13.98

clock clk (rise edge) 20.00 20.00

clock network delay (ideal) 0.00 20.00

output external delay 0.00 20.00

data required time 20.00

-----------------------------------------------------------

data required time 20.00

data arrival time -13.98

-----------------------------------------------------------

slack (MET) 6.02

1

Loading db file '/home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex03/02\_library/pdk180nm\_tt\_1p8v\_25c.db'

Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)

Warning: Design has unannotated primary inputs. (PWR-414)

Warning: Design has unannotated sequential cell outputs. (PWR-415)

* Timing report bao gồm 2 loại timing report là in2out and reg2out. Đối với report in2out không có constraint về timing vì đây là path chỉ toàn những cell combinational logic nên timing không cần constraint vì data truyền sẽ không bao giờ mất mát. Chúng ta thấy report reg2out bắt đầu tại cell d\_ff\_04/q\_reg/CK và kết thúc tại điểm trigger (out) bên cạnh đó đây là path có critical timing nên report timing sẽ report ra, ta thấy path này met về timing có nghĩa là data truyền trên path này sẽ không bao giờ thất thoát dữ liệu, thông số của clock network delay bằng 20 và input external delay lý tưởng bằng 0.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : power

-analysis\_effort low

Design : ex03

Version: G-2012.06-SP2

Date : Fri Jan 4 23:55:16 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex03/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Design Wire Load Model Library

------------------------------------------------

ex03 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Global Operating Voltage = 1.8

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000pf

Time Units = 1ns

Dynamic Power Units = 1mW (derived from V,C,T units)

Leakage Power Units = 1pW

Cell Internal Power = -10.4863 nW (0%)

Net Switching Power = 3.9925 uW (100%)

---------

Total Dynamic Power = 3.9820 uW (100%)

Cell Leakage Power = 760.9962 nW

Internal Switching Leakage Total

Power Group Power Power Power Power ( % ) Attrs

--------------------------------------------------------------------------------------------------

io\_pad 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

memory 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

black\_box 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

clock\_network 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

register -8.8466e-06 3.9923e-03 7.6087e+05 4.7443e-03 ( 100.03%)

sequential 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

combinational -1.6397e-06 2.3928e-07 125.7993 -1.2746e-06

( -0.03%)

--------------------------------------------------------------------------------------------------

Total -1.0486e-05 mW 3.9925e-03 mW 7.6100e+05 pW 4.7430e-03 mW

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : constraint

Design : ex03

Version: G-2012.06-SP2

Date : Fri Jan 4 23:55:16 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Weighted

Group (max\_delay/setup) Cost Weight Cost

-----------------------------------------------------

clk 0.00 1.00 0.00

default 0.00 1.00 0.00

-----------------------------------------------------

max\_delay/setup 0.00

Total Neg Critical

Group (critical\_range) Slack Endpoints Cost

-----------------------------------------------------

clk 0.00 0 0.00

default 0.00 0 0.00

-----------------------------------------------------

critical\_range 0.00

Constraint Cost

-----------------------------------------------------

max\_transition 1.76 (VIOLATED)

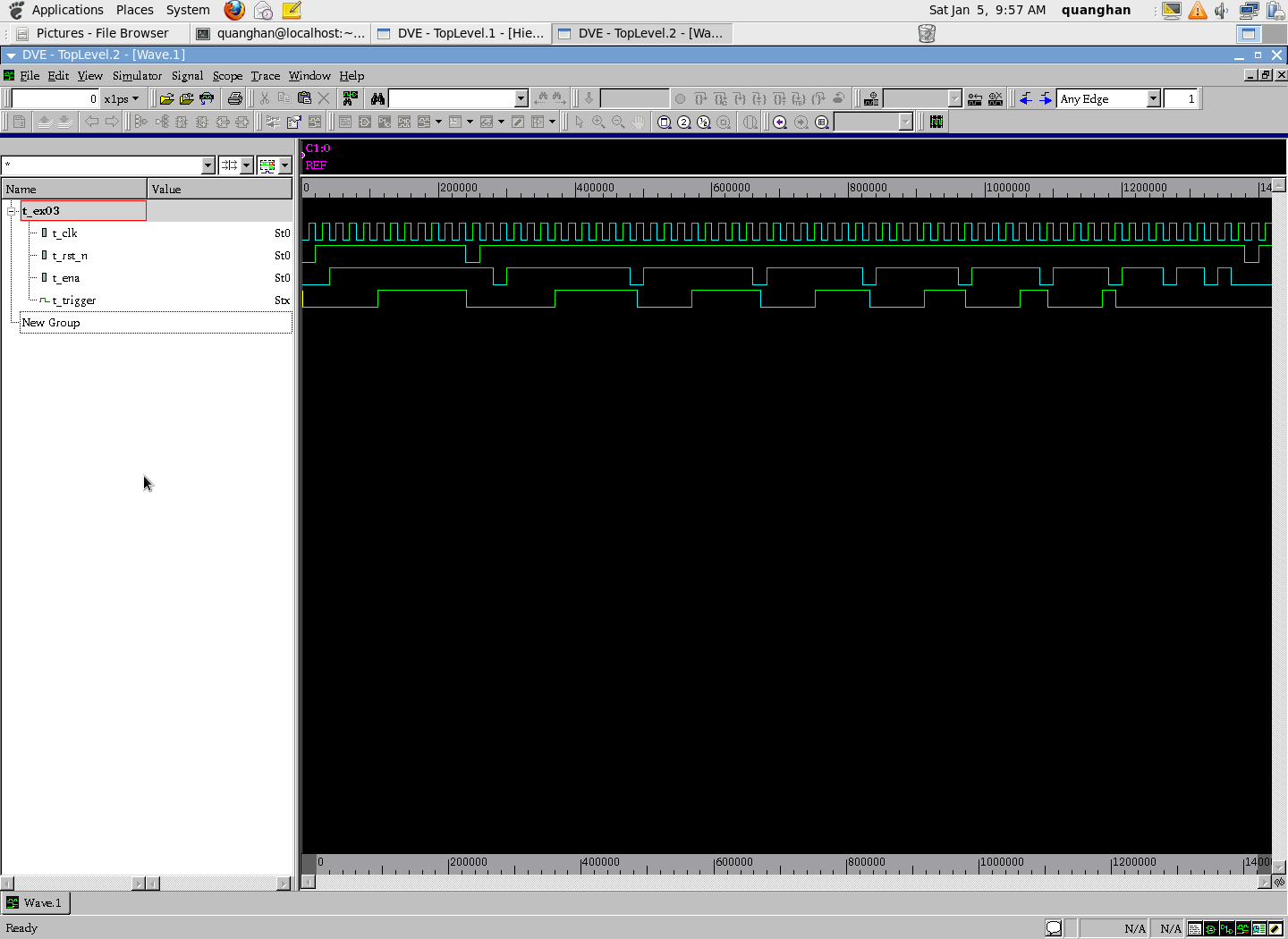
max\_capacitance 0.99 (VIOLATED)

max\_delay/setup 0.00 (MET)

critical\_range 0.00 (MET)

1

* Năng lượng tiêu tán phần lớn trong mode switching và chủ yếu tiêu tán trên các cell combinational logic. Bên cạnh đó, internal power tiêu tán chủ yếu trên các cell combinational logic. Đối với mode leakage power, năng lượng chủ yếu rơi trên các register.
* Gate simulation



**Lab4**

* **Constraint file:**

#!/bin/bash

#============== SET DIRECTORY =================

set search\_path "./../02\_library"

set osearch\_path [ concat $search\_path \

]

#============== ADD THE LIBRARY ================

set target\_library "pdk180nm\_tt\_1p8v\_25c.db"

set link\_library "\* $target\_library"

set synthesis\_library standard.sldb

#============= ANALYSE DESIGN ==================

analyze -format verilog "./../01\_rtl/ex04.v"

elaborate ex04

current\_design ex04

#============= CONSTRAIN FOR DESIGN ============

#create\_clock -name clk -period 1000 {clk}

#set\_input\_delay -max 10 -clock clk [all\_inputs]

#set\_input\_delay -min 1 -clock clk [all\_inputs]

#set\_output\_delay -max 10 -clock clk [all\_outputs]

#set\_output\_delay -min 1 -clock clk [all\_outputs]

#set\_wire\_load\_model -name "zero-wire-load-model"

set\_wire\_load\_model -name "pdk\_bk\_v1.00"

#set\_wire\_load\_model -name "pdk\_bk\_v1.01"

#set\_wire\_load\_model -name "pdk\_bk\_v1.02"

#set\_wire\_load\_model -name "pdk\_bk\_v1.03"

#set\_wire\_load\_model -name "pdk\_bk\_v1.04"

#set\_wire\_load\_model -name "pdk\_bk\_v1.05"

#============= SYNTHESIZE========================

compile\_ultra

#============= REPORT PERFORMANCE ===============

report\_area >> syn.log

report\_timing >> syn.log

report\_power >> syn.log

report\_constraint >> syn.log

write -f ddc -o ./../04\_gate/ex04.ddc

write -format verilog -hierarchy -output ./../04\_gate/ex04.netlist.v

write\_sdf ./../04\_gate/ex04.sdf

quit

* **Synthesis log file**

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : area

Design : ex04

Version: G-2012.06-SP2

Date : Sat Jan 5 00:00:41 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Information: Updating design information... (UID-85)

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex04/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Number of ports: 14

Number of nets: 27

Number of cells: 18

Number of combinational cells: 18

Number of sequential cells: 0

Number of macros: 0

Number of buf/inv: 0

Number of references: 6

Combinational area: 1195.875008

Buf/Inv area: 0.000000

Noncombinational area: 0.000000

Net Interconnect area: 632.936538

Total cell area: 1195.875008

Total area: 1828.811545

1

* Total area được tạo nên từ diện tích của các cell Non-combinational (Flip – flop) và net connection trong mạch.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : ex04

Version: G-2012.06-SP2

Date : Sat Jan 5 00:00:41 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: b[0] (input port)

Endpoint: cout (output port)

Path Group: (none)

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex04 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 r

b[0] (in) 0.00 0.00 r

U13/Y (OR2X1) 0.19 0.19 r

U15/Y (OAI2BB1X1) 0.15 0.34 r

U16/Y (OR2X1) 0.10 0.44 r

U18/Y (OAI2BB1X1) 0.15 0.59 r

U19/Y (OR2X1) 0.10 0.69 r

U21/Y (OAI2BB1X1) 0.15 0.83 r

U22/Y (OAI21X1) 0.13 0.97 f

U23/Y (OAI2BB1X1) 0.13 1.10 r

cout (out) 0.00 1.10 r

data arrival time 1.10

-----------------------------------------------------------

(Path is unconstrained)

1

Loading db file '/home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex04/02\_library/pdk180nm\_tt\_1p8v\_25c.db'

Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)

Warning: There is no defined clock in the design. (PWR-80)

Warning: Design has unannotated primary inputs. (PWR-414)

* Timing report bao gồm 2 loại timing report là in2out and reg2out. Đối với report in2out không có constraint về timing vì đây là path chỉ toàn những cell combinational logic nên timing không cần constraint vì data truyền sẽ không bao giờ mất mát. Chúng ta thấy report reg2out bắt đầu tại cell b[0] và kết thúc tại điểm count (out) bên cạnh đó đây là path có critical timing nên report timing sẽ report ra, ta thấy path này met về timing có nghĩa là data truyền trên path này sẽ không bao giờ thất thoát dữ liệu, thông số của clock network delay bằng 20 và input external delay lý tưởng bằng 0.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : power

-analysis\_effort low

Design : ex04

Version: G-2012.06-SP2

Date : Sat Jan 5 00:00:41 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex04/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Design Wire Load Model Library

------------------------------------------------

ex04 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Global Operating Voltage = 1.8

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000pf

Time Units = 1ns

Dynamic Power Units = 1mW (derived from V,C,T units)

Leakage Power Units = 1pW

Cell Internal Power = -254.8140 nW (125%)

Net Switching Power = 51.2628 nW (-24%)

---------

Total Dynamic Power = -203.5512 nW (100%)

Cell Leakage Power = 247.7916 nW

Information: report\_power power group summary does not include estimated clock tree power. (PWR-789)

Internal Switching Leakage Total

Power Group Power Power Power Power ( % ) Attrs

--------------------------------------------------------------------------------------------------

io\_pad 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

memory 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

black\_box 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

clock\_network 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

register 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

sequential 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

combinational -2.5481e-04 5.1263e-05 2.4779e+05 4.4240e-05 ( 100.00%)

--------------------------------------------------------------------------------------------------

Total -2.5481e-04 mW 5.1263e-05 mW 2.4779e+05 pW 4.4240e-05 mW

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : constraint

Design : ex04

Version: G-2012.06-SP2

Date : Sat Jan 5 00:00:41 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Constraint Cost

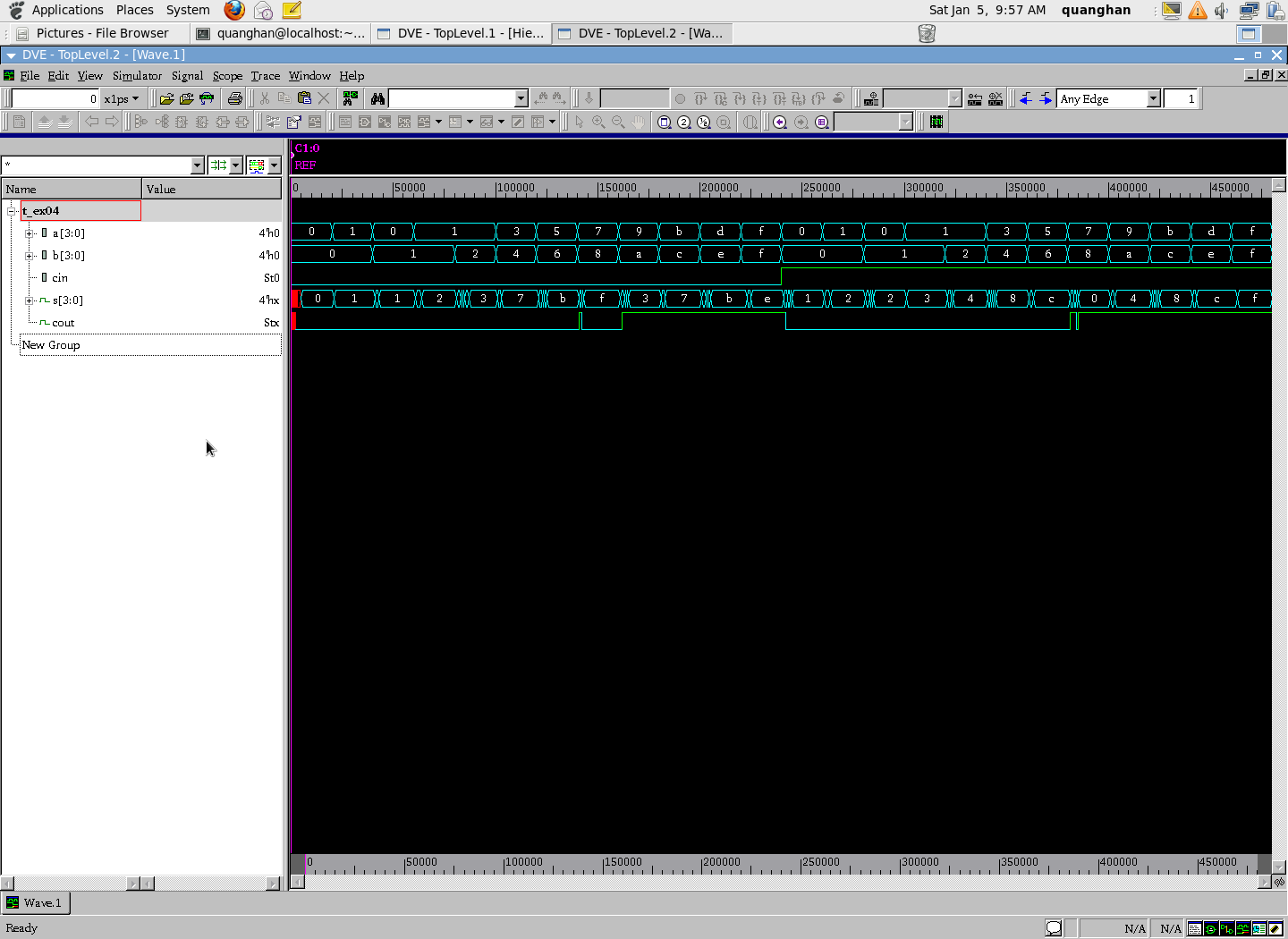
-----------------------------------------------------

max\_transition 0.00 (MET)

max\_capacitance 0.00 (MET)

1

* Toàn bộ power rơi trên các cell combinational logic và phần lớn ở mode switching.
* Gate simulation



**Lab5**

* **Constraint file:**

#!/bin/bash

#============== SET DIRECTORY =================

set search\_path "./../02\_library"

set osearch\_path [ concat $search\_path \

]

#============== ADD THE LIBRARY ================

set target\_library "pdk180nm\_tt\_1p8v\_25c.db"

set link\_library "\* $target\_library"

set synthesis\_library standard.sldb

#============= ANALYSE DESIGN ==================

analyze -format verilog "./../01\_rtl/ex05.v"

elaborate ex05

current\_design ex05

#============= CONSTRAIN FOR DESIGN ============

#create\_clock -name clk -period 1000 {clk}

#set\_input\_delay -max 10 -clock clk [all\_inputs]

#set\_input\_delay -min 1 -clock clk [all\_inputs]

#set\_output\_delay -max 10 -clock clk [all\_outputs]

#set\_output\_delay -min 1 -clock clk [all\_outputs]

#set\_wire\_load\_model -name "zero-wire-load-model"

set\_wire\_load\_model -name "pdk\_bk\_v1.00"

#set\_wire\_load\_model -name "pdk\_bk\_v1.01"

#set\_wire\_load\_model -name "pdk\_bk\_v1.02"

#set\_wire\_load\_model -name "pdk\_bk\_v1.03"

#set\_wire\_load\_model -name "pdk\_bk\_v1.04"

#set\_wire\_load\_model -name "pdk\_bk\_v1.05"

#============= SYNTHESIZE========================

compile\_ultra

#============= REPORT PERFORMANCE ===============

report\_area >> syn.log

report\_timing >> syn.log

report\_power >> syn.log

report\_constraint >> syn.log

write -f ddc -o ./../04\_gate/ex05.ddc

write -format verilog -hierarchy -output ./../04\_gate/ex05.netlist.v

write\_sdf ./../04\_gate/ex05.sdf

quit

* **Synthesis log file**

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : area

Design : ex05

Version: G-2012.06-SP2

Date : Sat Jan 5 00:07:38 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Information: Updating design information... (UID-85)

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex05/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Number of ports: 16

Number of nets: 66

Number of cells: 58

Number of combinational cells: 58

Number of sequential cells: 0

Number of macros: 0

Number of buf/inv: 4

Number of references: 13

Combinational area: 3461.805061

Buf/Inv area: 121.164001

Noncombinational area: 0.000000

Net Interconnect area: 1939.209813

Total cell area: 3461.805061

Total area: 5401.014874

1

* Total area của design được tạo nên từ total cell area và net interconnect area. Trong đó thì total cell area chỉ bao gồm các cell combinational logic. Do đó thiết kế này diện tích chỉ bao gồm diện tích của các cell combinational logic and net connection của mạch.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : ex05

Version: G-2012.06-SP2

Date : Sat Jan 5 00:07:38 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: q[1] (input port)

Endpoint: p[6] (output port)

Path Group: (none)

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex05 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 r

q[1] (in) 0.00 0.00 r

U62/Y (NOR2BX1) 3.21 3.21 r

U75/Y (AOI22X1) 0.15 3.37 f

U77/Y (XOR3X1) 0.31 3.67 f

U89/Y (OAI21X1) 0.32 3.99 r

U101/Y (AOI21X1) 0.15 4.14 f

U103/Y (OAI21X1) 0.16 4.31 r

U57/Y (XOR2X1) 0.22 4.52 f

U59/Y (XNOR2X1) 0.33 4.85 r

U105/Y (AOI21X1) 0.15 5.00 f

U109/Y (XOR3X1) 0.30 5.30 f

p[6] (out) 0.00 5.30 f

data arrival time 5.30

-----------------------------------------------------------

(Path is unconstrained)

1

Loading db file '/home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex05/02\_library/pdk180nm\_tt\_1p8v\_25c.db'

Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)

Warning: There is no defined clock in the design. (PWR-80)

Warning: Design has unannotated primary inputs. (PWR-414)

* Mạch chỉ bao gồm các cell combinational logic nên không có timing constraint. Bên cạnh đó, report timing có thể trích xuất bằng report timing cho loại in to out, nghĩa là timing từ input pin của thiết kế qua các cell combinational logic và output ra output pin mà không qua bất cứ một flipflop nào.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : power

-analysis\_effort low

Design : ex05

Version: G-2012.06-SP2

Date : Sat Jan 5 00:07:39 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex05/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Design Wire Load Model Library

------------------------------------------------

ex05 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Global Operating Voltage = 1.8

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000pf

Time Units = 1ns

Dynamic Power Units = 1mW (derived from V,C,T units)

Leakage Power Units = 1pW

Cell Internal Power = -568.8396 nW (128%)

Net Switching Power = 123.1409 nW (-27%)

---------

Total Dynamic Power = -445.6987 nW (100%)

Cell Leakage Power = 341.9795 nW

Information: report\_power power group summary does not include estimated clock tree power. (PWR-789)

Internal Switching Leakage Total

Power Group Power Power Power Power ( % ) Attrs

--------------------------------------------------------------------------------------------------

io\_pad 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

memory 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

black\_box 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

clock\_network 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

register 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

sequential 0.0000 0.0000 0.0000 0.0000 ( -0.00%)

combinational -5.6884e-04 1.2314e-04 3.4198e+05 -1.0372e-04

( 100.00%)

--------------------------------------------------------------------------------------------------

Total -5.6884e-04 mW 1.2314e-04 mW 3.4198e+05 pW -1.0372e-04 mW

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : constraint

Design : ex05

Version: G-2012.06-SP2

Date : Sat Jan 5 00:07:39 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Constraint Cost

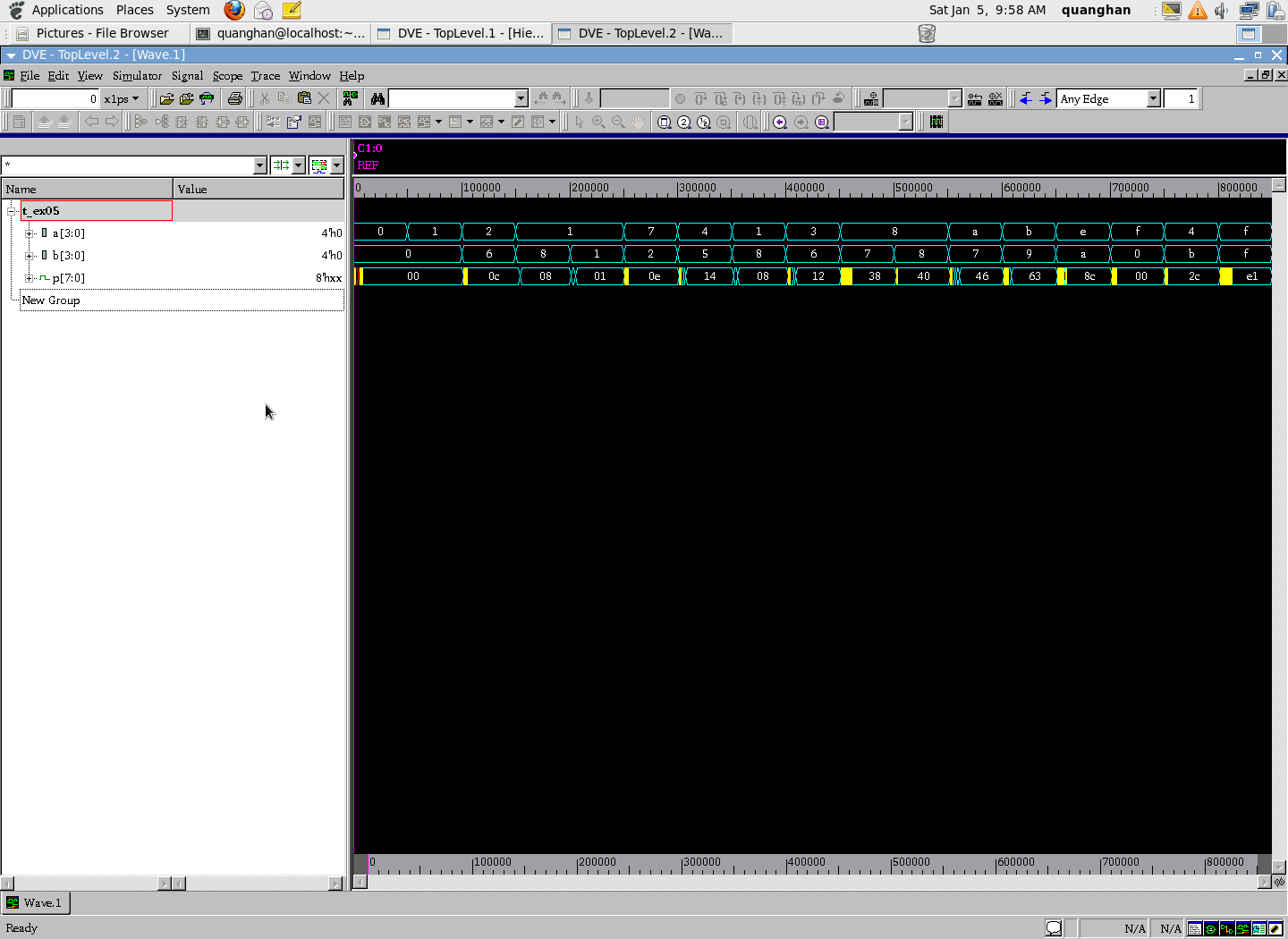
-----------------------------------------------------

max\_transition 0.00 (MET)

max\_capacitance 0.00 (MET)

1

* Toàn bộ power rơi trên các cell combinational logic và phần lớn ở mode switching.
* Gate simulation



**Lab6**

* **Constraint file:**

#!/bin/bash

#============== SET DIRECTORY =================

set search\_path "./../02\_library"

set osearch\_path [ concat $search\_path \

]

#============== ADD THE LIBRARY ================

set target\_library "pdk180nm\_tt\_1p8v\_25c.db"

set link\_library "\* $target\_library"

set synthesis\_library standard.sldb

#============= ANALYSE DESIGN ==================

analyze -format verilog "./../01\_rtl/ex06.v"

elaborate ex06

current\_design ex06

#============= CONSTRAIN FOR DESIGN ============

create\_clock -name clk -period 20 {clk}

set\_load 0 [all\_inputs]

set\_load 1 [all\_outputs]

set\_input\_delay -max 1 -clock clk [all\_inputs]

set\_output\_delay -max 0 -clock clk [all\_outputs]

#set\_wire\_load\_model -name "zero-wire-load-model"

set\_wire\_load\_model -name "pdk\_bk\_v1.00"

#set\_wire\_load\_model -name "pdk\_bk\_v1.01"

#set\_wire\_load\_model -name "pdk\_bk\_v1.02"

#set\_wire\_load\_model -name "pdk\_bk\_v1.03"

#set\_wire\_load\_model -name "pdk\_bk\_v1.04"

#set\_wire\_load\_model -name "pdk\_bk\_v1.05"

#============= SYNTHESIZE========================

compile\_ultra

#============= REPORT PERFORMANCE ===============

report\_area >> syn.log

report\_timing -path\_type full -delay min >> syn.log

report\_timing -path\_type full -delay max >> syn.log

report\_power >> syn.log

report\_constraint >> syn.log

write -f ddc -o ./../04\_gate/ex06.ddc

write -format verilog -hierarchy -output ./../04\_gate/ex06.netlist.v

write\_sdf ./../04\_gate/ex06.sdf

quit

* **Synthesis log file**

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : area

Design : ex06

Version: G-2012.06-SP2

Date : Sat Jan 5 00:13:17 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Information: Updating design information... (UID-85)

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex06/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Number of ports: 4

Number of nets: 8

Number of cells: 5

Number of combinational cells: 3

Number of sequential cells: 2

Number of macros: 0

Number of buf/inv: 0

Number of references: 4

Combinational area: 191.844002

Buf/Inv area: 0.000000

Noncombinational area: 443.359985

Net Interconnect area: 175.067554

Total cell area: 635.203987

Total area: 810.271541

1

* Total area được tạo nên từ diện tích của các cell Non-combinational (Flip – flop) và net connection trong mạch.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay min

-max\_paths 1

Design : ex06

Version: G-2012.06-SP2

Date : Sat Jan 5 00:13:17 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: state\_reg[1]/CK

(internal path startpoint clocked by clk)

Endpoint: out (output port clocked by clk)

Path Group: (none)

Path Type: min

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex06 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 r

state\_reg[1]/CK (DFFRHQX1) 0.00 0.00 r

state\_reg[1]/Q (DFFRHQX1) 2.29 2.29 r

out (out) 10.93 13.23 r

data arrival time 13.23

-----------------------------------------------------------

(Path is unconstrained)

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : ex06

Version: G-2012.06-SP2

Date : Sat Jan 5 00:13:17 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: state\_reg[1]/CK

(internal path startpoint clocked by clk)

Endpoint: out (output port clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex06 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.00 0.00 r

state\_reg[1]/CK (DFFRHQX1) 0.00 0.00 r

state\_reg[1]/Q (DFFRHQX1) 3.04 3.04 f

out (out) 10.93 13.98 f

data arrival time 13.98

clock clk (rise edge) 20.00 20.00

clock network delay (ideal) 0.00 20.00

output external delay 0.00 20.00

data required time 20.00

-----------------------------------------------------------

data required time 20.00

data arrival time -13.98

-----------------------------------------------------------

slack (MET) 6.02

1

Loading db file '/home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex06/02\_library/pdk180nm\_tt\_1p8v\_25c.db'

Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)

Warning: Design has unannotated primary inputs. (PWR-414)

Warning: Design has unannotated sequential cell outputs. (PWR-415)

* Timing report bao gồm 2 loại timing report là in2out and reg2out. Đối với report in2out không có constraint về timing vì đây là path chỉ toàn những cell combinational logic nên timing không cần constraint vì data truyền sẽ không bao giờ mất mát. Chúng ta thấy report reg2out bắt đầu tại cell state\_reg[1]/CK và kết thúc tại điểm out bên cạnh đó đây là path có critical timing nên report timing sẽ report ra, ta thấy path này met về timing có nghĩa là data truyền trên path này sẽ không bao giờ thất thoát dữ liệu, thông số của clock network delay bằng 20 và input external delay lý tưởng bằng 0.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : power

-analysis\_effort low

Design : ex06

Version: G-2012.06-SP2

Date : Sat Jan 5 00:13:17 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex06/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Design Wire Load Model Library

------------------------------------------------

ex06 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Global Operating Voltage = 1.8

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000pf

Time Units = 1ns

Dynamic Power Units = 1mW (derived from V,C,T units)

Leakage Power Units = 1pW

Cell Internal Power = -16.2263 nW (0%)

Net Switching Power = 10.8819 uW (100%)

---------

Total Dynamic Power = 10.8657 uW (100%)

Cell Leakage Power = 682.8129 nW

Internal Switching Leakage Total

Power Group Power Power Power Power ( % ) Attrs

--------------------------------------------------------------------------------------------------

io\_pad 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

memory 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

black\_box 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

clock\_network 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

register -1.5234e-05 1.0882e-02 5.9404e+05 1.1460e-02 ( 99.24%)

sequential 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

combinational -9.9251e-07 2.4728e-07 8.8776e+04 8.8030e-05 ( 0.76%)

--------------------------------------------------------------------------------------------------

Total -1.6226e-05 mW 1.0882e-02 mW 6.8281e+05 pW 1.1549e-02 mW

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : constraint

Design : ex06

Version: G-2012.06-SP2

Date : Sat Jan 5 00:13:17 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Weighted

Group (max\_delay/setup) Cost Weight Cost

-----------------------------------------------------

clk 0.00 1.00 0.00

default 0.00 1.00 0.00

-----------------------------------------------------

max\_delay/setup 0.00

Total Neg Critical

Group (critical\_range) Slack Endpoints Cost

-----------------------------------------------------

clk 0.00 0 0.00

default 0.00 0 0.00

-----------------------------------------------------

critical\_range 0.00

Constraint Cost

-----------------------------------------------------

max\_transition 1.76 (VIOLATED)

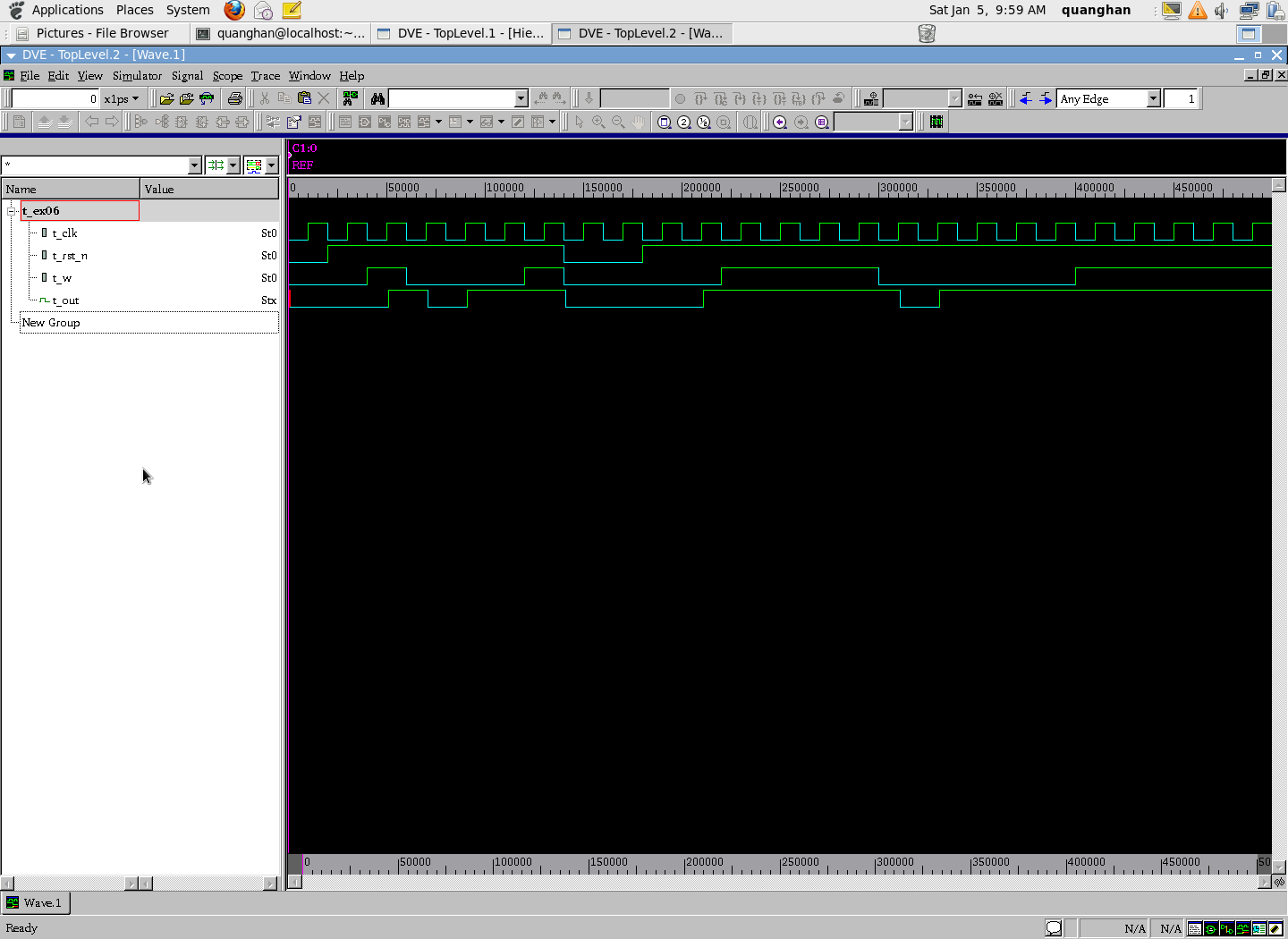
max\_capacitance 0.99 (VIOLATED)

max\_delay/setup 0.00 (MET)

critical\_range 0.00 (MET)

1

* Năng lượng tiêu tán phần lớn trong mode switching và chủ yếu tiêu tán trên các cell combinational logic. Bên cạnh đó, internal power tiêu tán chủ yếu trên các cell combinational logic. Đối với mode leakage power, năng lượng chủ yếu rơi trên các register.
* **Gate simulation**



**Lab7**

* **Constraint file:**

#!/bin/bash

#============== SET DIRECTORY =================

set search\_path "./../02\_library"

set osearch\_path [ concat $search\_path \

]

#============== ADD THE LIBRARY ================

set target\_library "pdk180nm\_tt\_1p8v\_25c.db"

set link\_library "\* $target\_library"

set synthesis\_library standard.sldb

#============= ANALYSE DESIGN ==================

analyze -format verilog "./../01\_rtl/ex07.v"

elaborate ex07

current\_design ex07

#============= CONSTRAIN FOR DESIGN ============

create\_clock -name clk -period 20 {clk}

set\_load 0 [all\_inputs]

set\_load 1 [all\_outputs]

set\_input\_delay -max 1 -clock clk [all\_inputs]

set\_output\_delay -max 0 -clock clk [all\_outputs]

#set\_wire\_load\_model -name "zero-wire-load-model"

set\_wire\_load\_model -name "pdk\_bk\_v1.00"

#set\_wire\_load\_model -name "pdk\_bk\_v1.01"

#set\_wire\_load\_model -name "pdk\_bk\_v1.02"

#set\_wire\_load\_model -name "pdk\_bk\_v1.03"

#set\_wire\_load\_model -name "pdk\_bk\_v1.04"

#set\_wire\_load\_model -name "pdk\_bk\_v1.05"

#============= SYNTHESIZE========================

compile\_ultra

#============= REPORT PERFORMANCE ===============

report\_area >> syn.log

report\_timing -path\_type full -delay min >> syn.log

report\_timing -path\_type full -delay max >> syn.log

report\_power >> syn.log

report\_constraint >> syn.log

write -f ddc -o ./../04\_gate/ex07.ddc

write -format verilog -hierarchy -output ./../04\_gate/ex07.netlist.v

write\_sdf ./../04\_gate/ex07.sdf

quit

* **Synthesis log file:**

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : area

Design : ex07

Version: G-2012.06-SP2

Date : Sat Jan 5 00:19:46 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Information: Updating design information... (UID-85)

Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex07/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Number of ports: 4

Number of nets: 25

Number of cells: 22

Number of combinational cells: 18

Number of sequential cells: 4

Number of macros: 0

Number of buf/inv: 7

Number of references: 10

Combinational area: 893.757011

Buf/Inv area: 212.037003

Noncombinational area: 886.719971

Net Interconnect area: 659.870004

Total cell area: 1780.476982

Total area: 2440.346986

1

* Total area được tạo nên từ diện tích của các cell Non-combinational (Flip – flop), net connection trong mạch và các khối combinational logic

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay min

-max\_paths 1

Design : ex07

Version: G-2012.06-SP2

Date : Sat Jan 5 00:19:46 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: state\_reg[2]/CK

(internal path startpoint clocked by clk)

Endpoint: out (output port clocked by clk)

Path Group: (none)

Path Type: min

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex07 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 r

state\_reg[2]/CK (DFFRHQX1) 0.00 0.00 r

state\_reg[2]/Q (DFFRHQX1) 0.08 0.08 r

U37/Y (INVX1) 0.04 0.11 f

U32/Y (OR2X1) 0.12 0.24 f

U35/Y (INVX1) 0.04 0.27 r

U33/Y (INVX1) 0.04 0.31 f

U34/Y (INVX1) 2.05 2.36 r

out (out) 10.93 13.29 r

data arrival time 13.29

-----------------------------------------------------------

(Path is unconstrained)

1

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : ex07

Version: G-2012.06-SP2

Date : Sat Jan 5 00:19:46 2019

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Startpoint: state\_reg[1]/CK

(internal path startpoint clocked by clk)

Endpoint: out (output port clocked by clk)

Path Group: clk

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

ex07 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.00 0.00

clock network delay (ideal) 0.00 0.00

input external delay 0.00 0.00 r

state\_reg[1]/CK (DFFRHQX1) 0.00 0.00 r

state\_reg[1]/Q (DFFRHQX1) 0.08 0.08 r

U38/Y (NOR2X1) 0.06 0.13 f

U39/Y (INVX1) 0.04 0.17 r

U32/Y (OR2X1) 0.08 0.25 r

U35/Y (INVX1) 0.04 0.29 f

U33/Y (INVX1) 0.03 0.32 r

U34/Y (INVX1) 2.49 2.81 f

out (out) 10.93 13.75 f

data arrival time 13.75

clock clk (rise edge) 20.00 20.00

clock network delay (ideal) 0.00 20.00

output external delay 0.00 20.00

data required time 20.00

-----------------------------------------------------------

data required time 20.00

data arrival time -13.75

-----------------------------------------------------------

slack (MET) 6.25

1

Loading db file '/home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex07/02\_library/pdk180nm\_tt\_1p8v\_25c.db'

Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)

Warning: Design has unannotated primary inputs. (PWR-414)

Warning: Design has unannotated sequential cell outputs. (PWR-415)

* Timing report bao gồm 2 loại timing report là in2out and reg2out. Đối với report in2out không có constraint về timing vì đây là path chỉ toàn những cell combinational logic nên timing không cần constraint vì data truyền sẽ không bao giờ mất mát. Chúng ta thấy report reg2out bắt đầu tại cell state\_reg[1]/CK và kết thúc tại điểm out bên cạnh đó đây là path có critical timing nên report timing sẽ report ra, ta thấy path này met về timing có nghĩa là data truyền trên path này sẽ không bao giờ thất thoát dữ liệu, thông số của clock network delay bằng 20 và input external delay lý tưởng bằng 0.

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Report : power

-analysis\_effort low

Design : ex07

Version: G-2012.06-SP2

Date : Sat Jan 5 00:19:47 2019

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Library(s) Used:

pdk180nm\_tt\_1p8v\_25c (File: /home/quanghan/Work/LamPham/06\_For\_Thinh/synthesis\_ex07/02\_library/pdk180nm\_tt\_1p8v\_25c.db)

Operating Conditions: tt\_1p8v\_25c Library: pdk180nm\_tt\_1p8v\_25c

Wire Load Model Mode: top

Design Wire Load Model Library

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ex07 pdk\_bk\_v1.00 pdk180nm\_tt\_1p8v\_25c

Global Operating Voltage = 1.8

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000pf

Time Units = 1ns

Dynamic Power Units = 1mW (derived from V,C,T units)

Leakage Power Units = 1pW

Cell Internal Power = -27.0824 nW (0%)

Net Switching Power = 7.9130 uW (100%)

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Total Dynamic Power = 7.8859 uW (100%)

Cell Leakage Power = 1.1373 uW

Internal Switching Leakage Total

Power Group Power Power Power Power ( % ) Attrs

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io\_pad 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

memory 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

black\_box 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

clock\_network 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

register -7.4398e-06 1.0382e-06 1.1189e+06 1.1125e-03 ( 12.33%)

sequential 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

combinational -1.9643e-05 7.9119e-03 1.8371e+04 7.9106e-03 ( 87.67%)

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Total -2.7082e-05 mW 7.9130e-03 mW 1.1373e+06 pW 9.0232e-03 mW

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Report : constraint

Design : ex07

Version: G-2012.06-SP2

Date : Sat Jan 5 00:19:47 2019

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Weighted

Group (max\_delay/setup) Cost Weight Cost

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clk 0.00 1.00 0.00

default 0.00 1.00 0.00

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max\_delay/setup 0.00

Total Neg Critical

Group (critical\_range) Slack Endpoints Cost

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clk 0.00 0 0.00

default 0.00 0 0.00

-----------------------------------------------------

critical\_range 0.00

Constraint Cost

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max\_transition 2.23 (VIOLATED)

max\_capacitance 0.99 (VIOLATED)

max\_delay/setup 0.00 (MET)

critical\_range 0.00 (MET)

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* Năng lượng tiêu tán phần lớn trong mode switching và chủ yếu tiêu tán trên các cell combinational logic. Bên cạnh đó, internal power tiêu tán chủ yếu trên các cell combinational logic. Đối với mode leakage power, năng lượng chủ yếu rơi trên các register.
* Gate simulation

