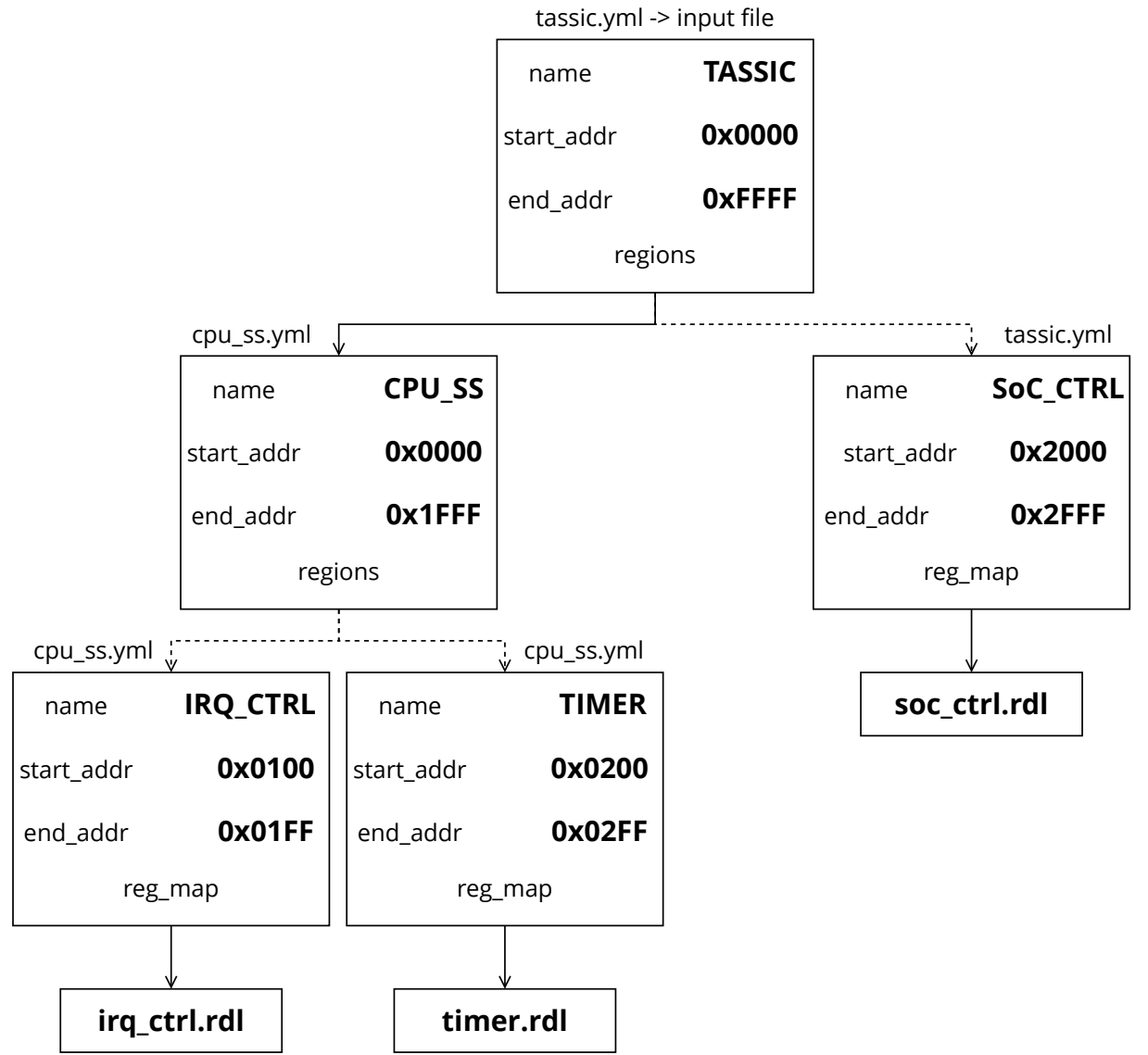
tassic.yml -> input file
name TASSIC
start_addr 0x0000
end_addr 0xFFFF
regions
cpu_ss.yml
name CPU_SS
start_addr 0x0000
end_addr 0x1FFF
regions
tassic.yml
name SoC_CTRL
start_addr 0x2000
end_addr 0x2FFF
reg_map
soc_ctrl.rdl
cpu_ss.yml
name IRQ_CTRL
start_addr 0x0100
end_addr 0x01FF
reg_map
irq_ctrl.rdl
cpu_ss.yml
name TIMER
start_addr 0x0200
end_addr 0x02FF
reg_map
timer.rdl