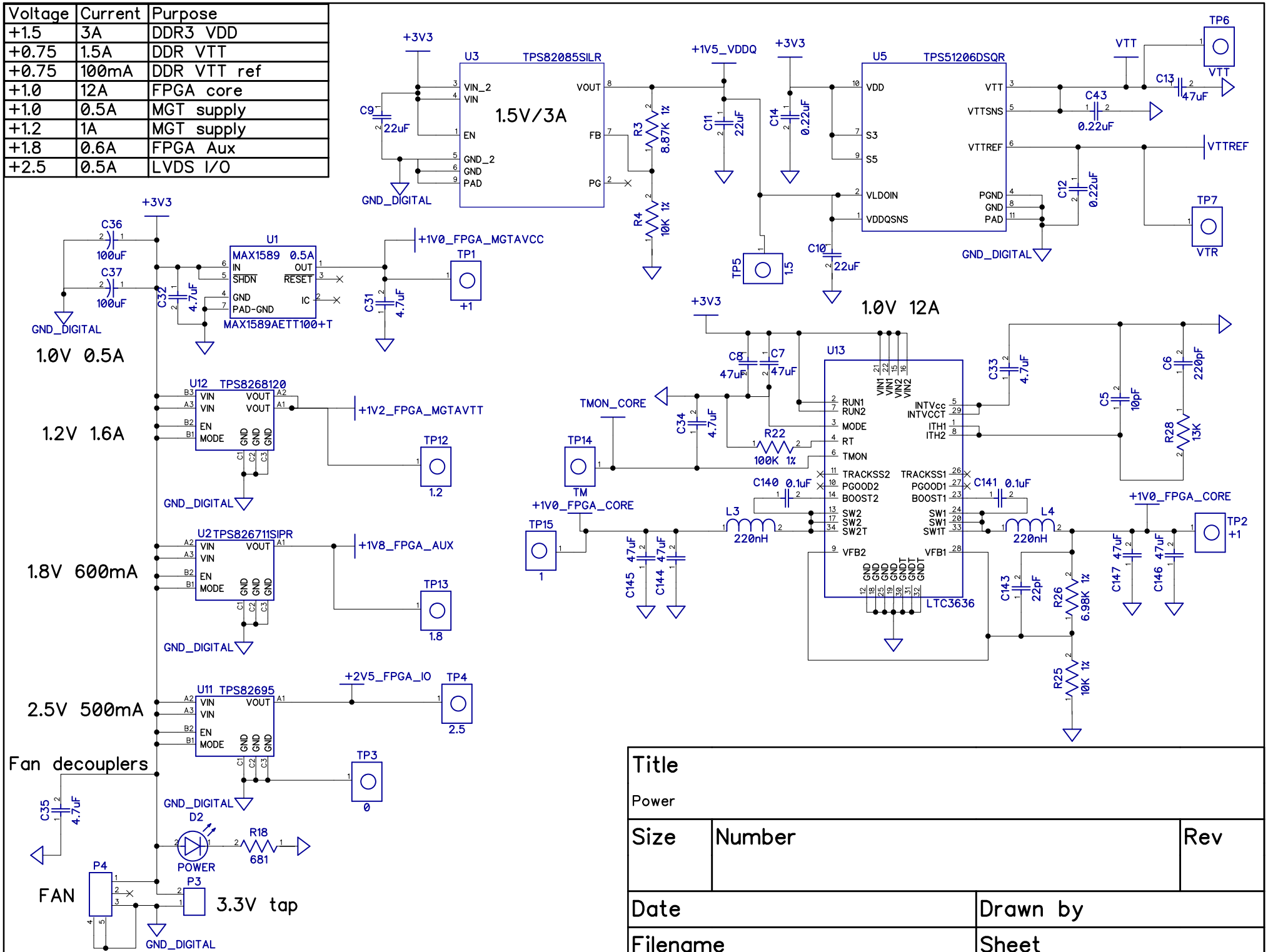
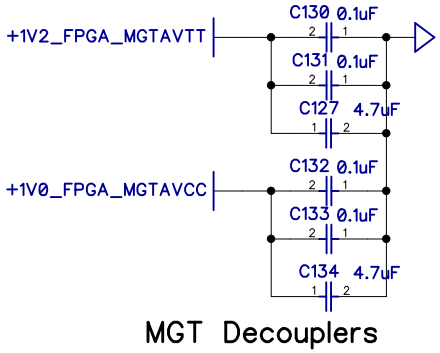
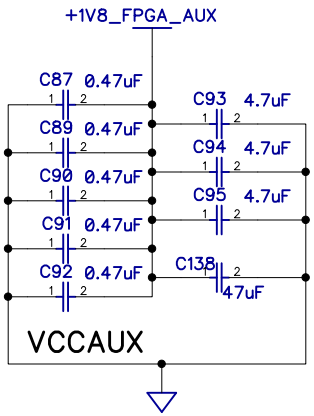
Title Block Diagram		
Size	Number	Rev
Date		Drawn by
Filename		Sheet

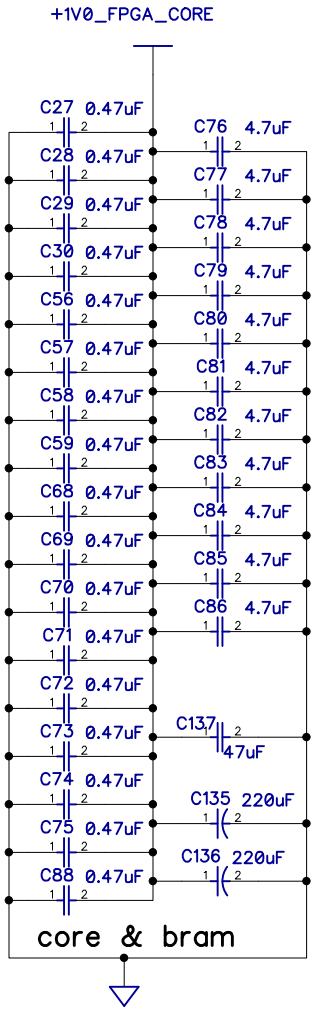
Voltage	Current	Purpose
+1.5	3A	DDR3 VDD
+0.75	1.5A	DDR VTT
+0.75	100mA	DDR VTT ref
+1.0	12A	FPGA core
+1.0	0.5A	MGT supply
+1.2	1A	MGT supply
+1.8	0.6A	FPGA Aux
+2.5	0.5A	LVDS I/O

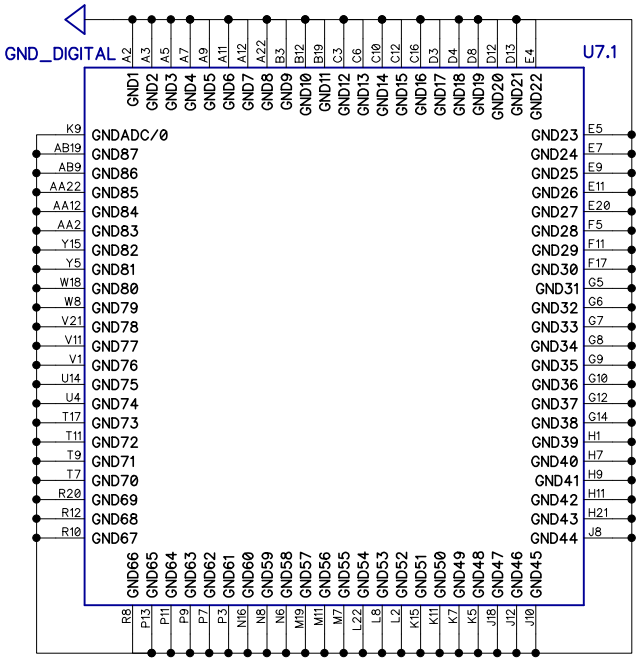


Title		
Power		
Size	Number	Rev
Date		Drawn by
Filename		Sheet



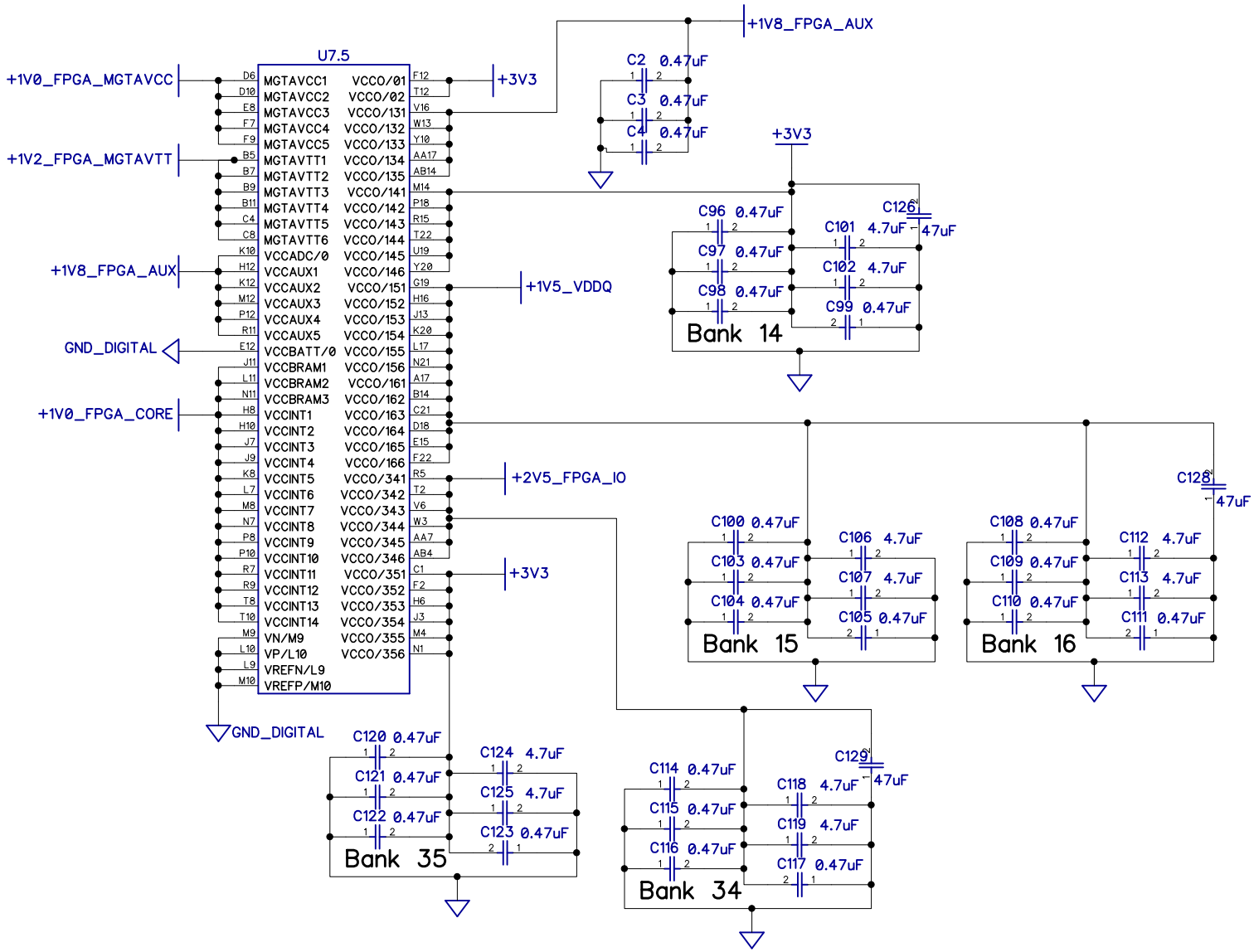






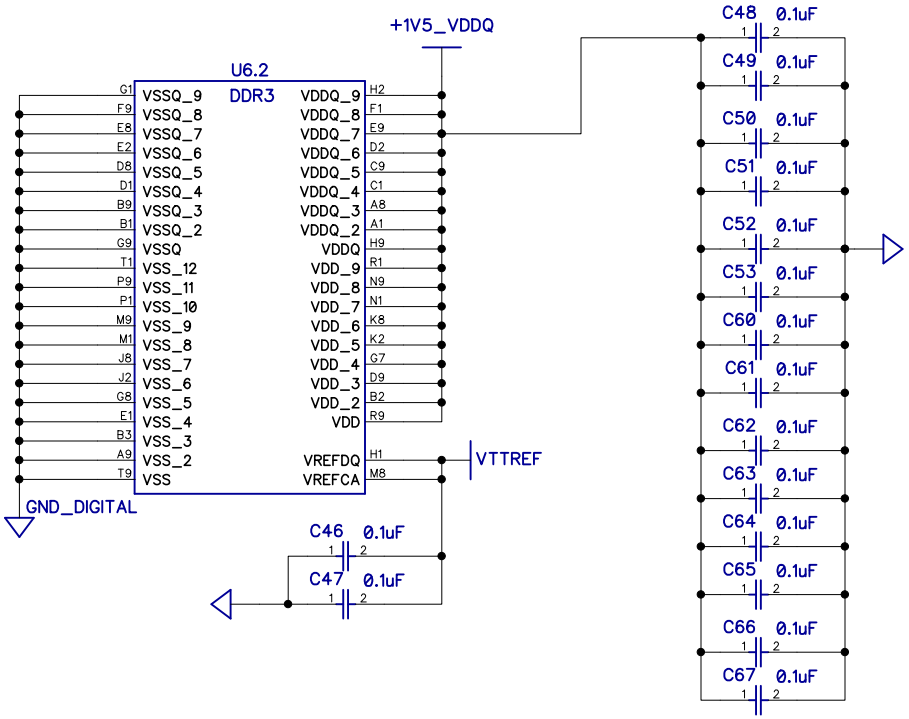
Bars	Value
0	
1 (A)	0.1uF
2 (B)	4.7uF
3 (C)	0.47uF

Title: FPGA power and decoupling		
Size	Number	Rev
Date		Drawn by
Filename		Sheet

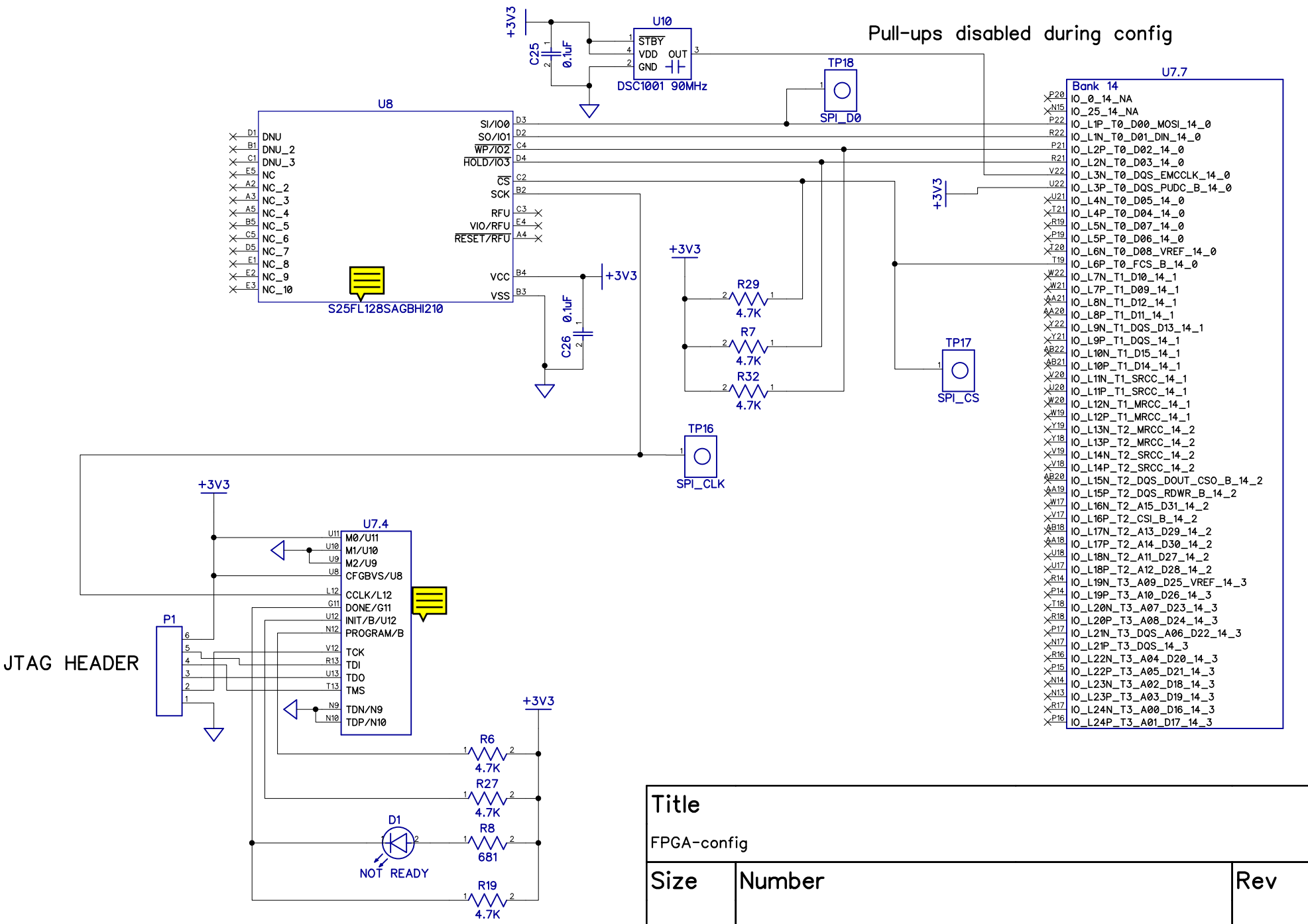


Bank	Voltage	Purpose
0	3.3	SPI, JTAG
13	3.3	Unused (NA on A50)
14	3.3	Config & 3.3V IO
15	1.5	DDR Addr/CTL
16	1.5	DDR data
34	2.5	LVDS I/O
35	3.3	3.3V I/O

Title: FPGA I/O decoupling		
Size	Number	Rev
Date		Drawn by
Filename		Sheet



Title DRAM Power and decoupling		
Size	Number	Rev
Date		Drawn by
Filename		Sheet


Pull-ups disabled during config
U10
STBY
VDD
OUT
GND
DSC1001 90MHz
C25
0.1uF
+3V3
TP18
SPI_D0
U8
DNU
DNU_2
DNU_3
NC
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
NC_9
NC_10
SI/IO0
SO/IO1
WP/IO2
HOLD/IO3
CS
SCK
RFU
VIO/RFU
RESET/RFU
VCC
VSS
S25FL128SAGBHI210
C26
0.1uF
R29
4.7K
R7
4.7K
R32
4.7K
TP17
SPI_CS
TP16
SPI_CLK
U7.7
Bank 14
IO_0_14_NA
IO_25_14_NA
IO_L1P_T0_D00_MOSI_14_0
IO_L1N_T0_D01_DIN_14_0
IO_L2P_T0_D02_14_0
IO_L2N_T0_D03_14_0
IO_L3N_T0_DQS_EMCCLK_14_0
IO_L3P_T0_DQS_PUDC_B_14_0
IO_L4N_T0_D05_14_0
IO_L4P_T0_D04_14_0
IO_L5N_T0_D07_14_0
IO_L5P_T0_D06_14_0
IO_L6N_T0_D08_VREF_14_0
IO_L6P_T0_FCS_B_14_0
IO_L7N_T1_D10_14_1
IO_L7P_T1_D09_14_1
IO_L8N_T1_D12_14_1
IO_L8P_T1_D11_14_1
IO_L9N_T1_DQS_D13_14_1
IO_L9P_T1_DQS_14_1
IO_L10N_T1_D15_14_1
IO_L10P_T1_D14_14_1
IO_L11N_T1_SRCC_14_1
IO_L11P_T1_SRCC_14_1
IO_L12N_T1_MRCC_14_1
IO_L12P_T1_MRCC_14_1
IO_L13N_T2_MRCC_14_2
IO_L13P_T2_MRCC_14_2
IO_L14N_T2_SRCC_14_2
IO_L14P_T2_SRCC_14_2
IO_L15N_T2_DQS_DOUT_CSO_B_14_2
IO_L15P_T2_DQS_RDWR_B_14_2
IO_L16N_T2_A15_D31_14_2
IO_L16P_T2_CSI_B_14_2
IO_L17N_T2_A13_D29_14_2
IO_L17P_T2_A14_D30_14_2
IO_L18N_T2_A11_D27_14_2
IO_L18P_T2_A12_D28_14_2
IO_L19N_T3_A09_D25_VREF_14_3
IO_L19P_T3_A10_D26_14_3
IO_L20N_T3_A07_D23_14_3
IO_L20P_T3_A08_D24_14_3
IO_L21N_T3_DQS_A06_D22_14_3
IO_L21P_T3_DQS_14_3
IO_L22N_T3_A04_D20_14_3
IO_L22P_T3_A05_D21_14_3
IO_L23N_T3_A02_D18_14_3
IO_L23P_T3_A03_D19_14_3
IO_L24N_T3_A00_D16_14_3
IO_L24P_T3_A01_D17_14_3
U7.4
M0/U11
M1/U10
M2/U9
CFGBVS/U8
CCLK/L12
DONE/G11
INIT/B/U12
PROGRAM/B
TCK
TDI
TDO
TMS
TDN/N9
TDP/N10
P1
JTAG HEADER
R6
4.7K
R27
4.7K
D1
NOT READY
R8
681
R19
4.7K
Title
FPGA-config
Size
Number
Rev
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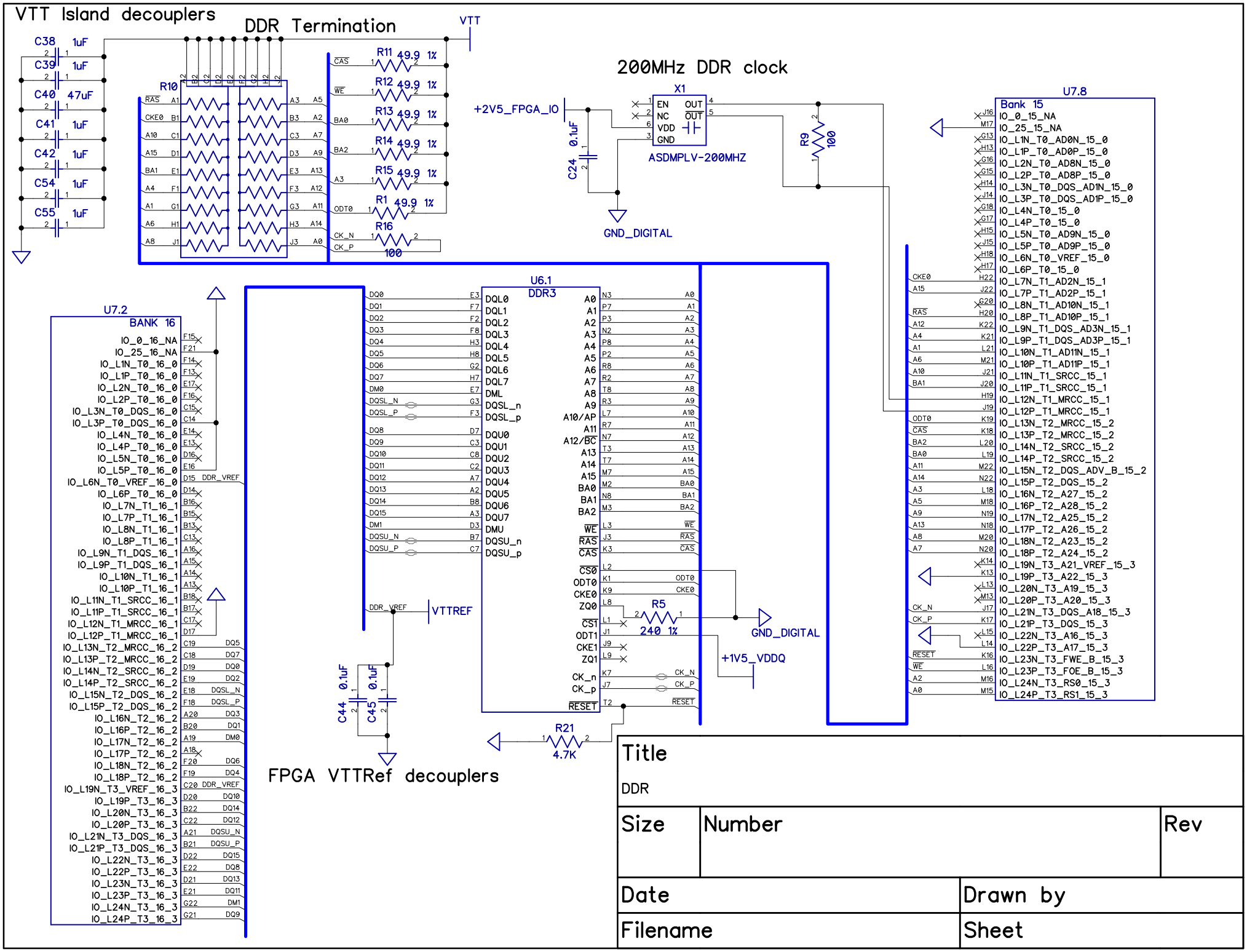
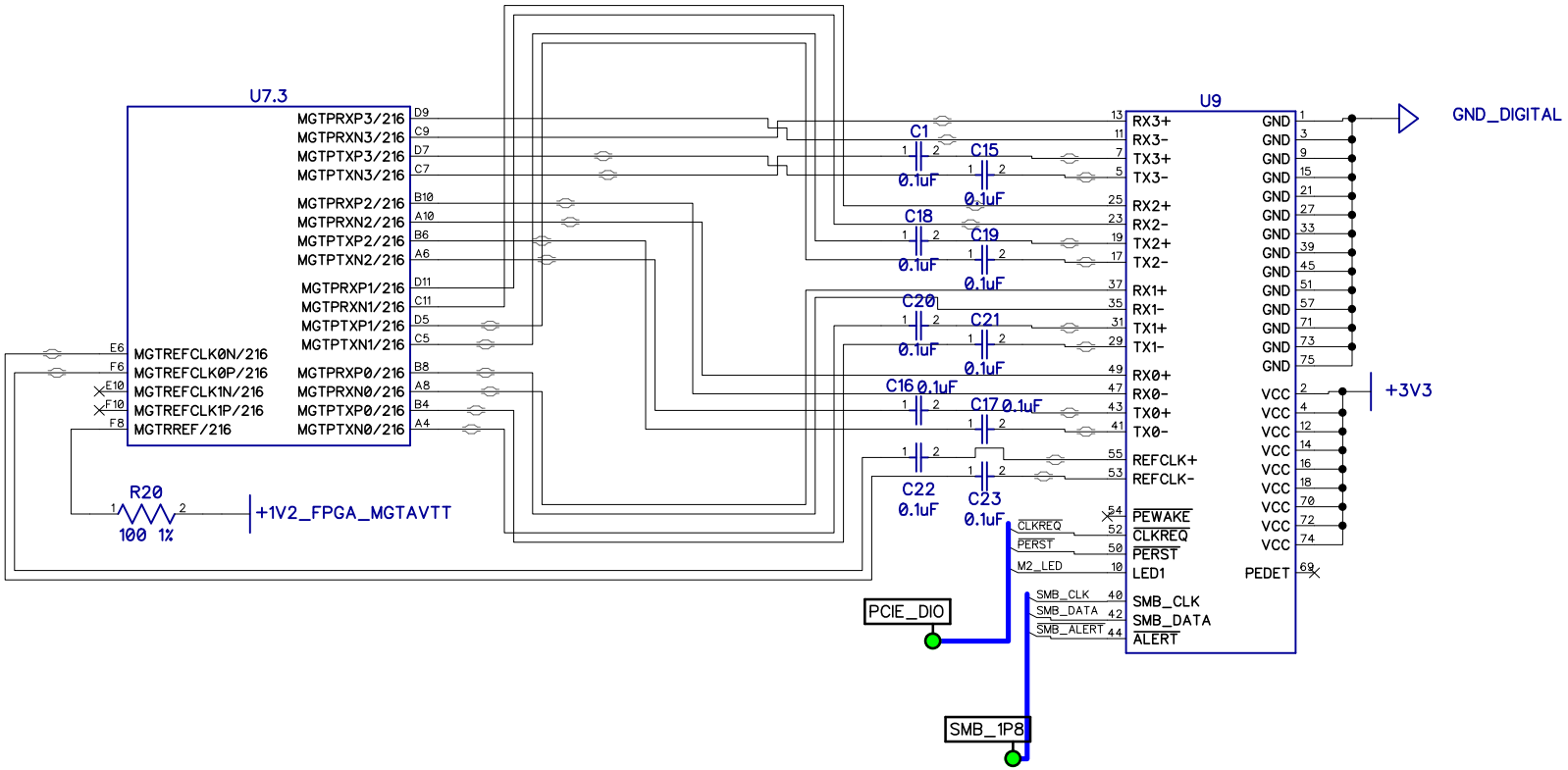
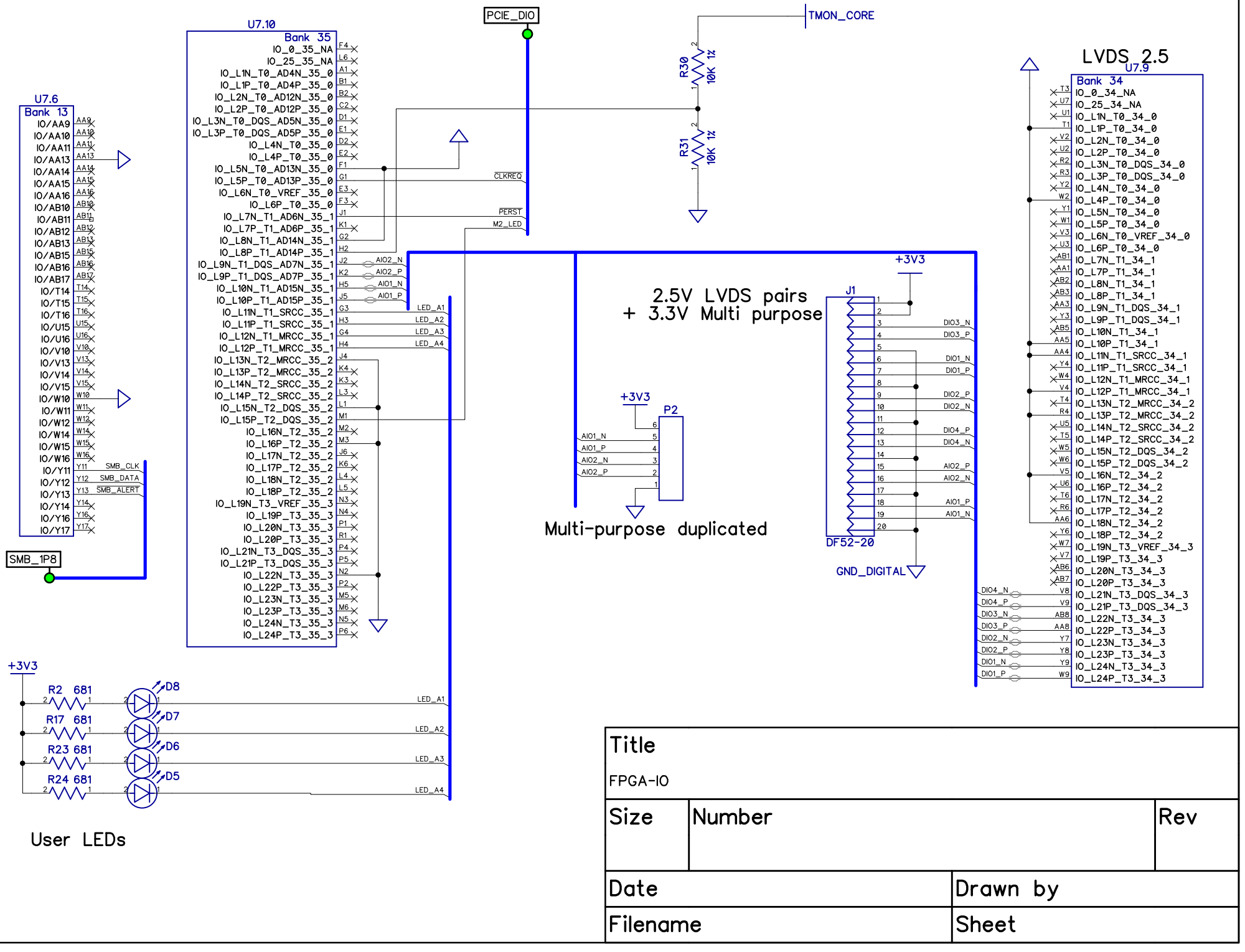
Drawn by
Filename
Sheet

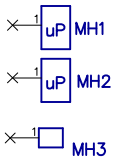

VTT Island decouplers
DDR Termination
VTT
C38 1uF
C39 1uF
C40 47uF
C41 1uF
C42 1uF
C54 1uF
C55 1uF
R10
R11 49.9 1%
R12 49.9 1%
R13 49.9 1%
R14 49.9 1%
R15 49.9 1%
R1 49.9 1%
R16 100
200MHz DDR clock
X1
ASDMPLV-200MHZ
+2V5_FPGA_IO
C24 0.1uF
GND_DIGITAL
R9 100
U7.8
Bank 15
U6.1
DDR3
U7.2
BANK 16
R5 240 1%
+1V5_VDDQ
R21 4.7K
C44 0.1uF
C45 0.1uF
DDR_VREF
VTTREF
FPGA VTTRef decouplers
Title
DDR
Size
Number
Rev
Date
Drawn by
Filename
Sheet



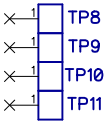
Title FPGA-MGT		
Size	Number	Rev
Date		Drawn by
Filename		Sheet


U7.6
Bank 13
IO/AA9
IO/AA10
IO/AA11
IO/AA13
IO/AA14
IO/AA15
IO/AA16
IO/AB10
IO/AB11
IO/AB12
IO/AB13
IO/AB15
IO/AB16
IO/AB17
IO/T14
IO/T15
IO/T16
IO/U15
IO/U16
IO/V10
IO/V13
IO/V14
IO/V15
IO/W10
IO/W11
IO/W12
IO/W14
IO/W15
IO/W16
IO/Y11
IO/Y12
IO/Y13
IO/Y14
IO/Y16
IO/Y17
SMB_CLK
SMB_DATA
SMB_ALERT
SMB_1P8
U7.10
Bank 35
IO_0_35_NA
IO_25_35_NA
IO_L1N_T0_AD4N_35_0
IO_L1P_T0_AD4P_35_0
IO_L2N_T0_AD12N_35_0
IO_L2P_T0_AD12P_35_0
IO_L3N_T0_DQS_AD5N_35_0
IO_L3P_T0_DQS_AD5P_35_0
IO_L4N_T0_35_0
IO_L4P_T0_35_0
IO_L5N_T0_AD13N_35_0
IO_L5P_T0_AD13P_35_0
IO_L6N_T0_VREF_35_0
IO_L6P_T0_35_0
IO_L7N_T1_AD6N_35_1
IO_L7P_T1_AD6P_35_1
IO_L8N_T1_AD14N_35_1
IO_L8P_T1_AD14P_35_1
IO_L9N_T1_DQS_AD7N_35_1
IO_L9P_T1_DQS_AD7P_35_1
IO_L10N_T1_AD15N_35_1
IO_L10P_T1_AD15P_35_1
IO_L11N_T1_SRCC_35_1
IO_L11P_T1_SRCC_35_1
IO_L12N_T1_MRCC_35_1
IO_L12P_T1_MRCC_35_1
IO_L13N_T2_MRCC_35_2
IO_L13P_T2_MRCC_35_2
IO_L14N_T2_SRCC_35_2
IO_L14P_T2_SRCC_35_2
IO_L15N_T2_DQS_35_2
IO_L15P_T2_DQS_35_2
IO_L16N_T2_35_2
IO_L16P_T2_35_2
IO_L17N_T2_35_2
IO_L17P_T2_35_2
IO_L18N_T2_35_2
IO_L18P_T2_35_2
IO_L19N_T3_VREF_35_3
IO_L19P_T3_35_3
IO_L20N_T3_35_3
IO_L20P_T3_35_3
IO_L21N_T3_DQS_35_3
IO_L21P_T3_DQS_35_3
IO_L22N_T3_35_3
IO_L22P_T3_35_3
IO_L23N_T3_35_3
IO_L23P_T3_35_3
IO_L24N_T3_35_3
IO_L24P_T3_35_3
AIO2_N
AIO2_P
AIO1_N
AIO1_P
CLKREQ
PERST
M2_LED
LED_A1
LED_A2
LED_A3
LED_A4
PCIE_DIO
TMON_CORE
R30
10K 1%
R31
10K 1%
+3V3
2.5V LVDS pairs
+ 3.3V Multi purpose
J1
DIO3_N
DIO3_P
DIO1_N
DIO1_P
DIO2_P
DIO2_N
DIO4_P
DIO4_N
AIO2_P
AIO2_N
AIO1_P
AIO1_N
DF52-20
GND_DIGITAL
P2
Multi-purpose duplicated
LVDS_2.5
U7.9
Bank 34
IO_0_34_NA
IO_25_34_NA
IO_L1N_T0_34_0
IO_L1P_T0_34_0
IO_L2N_T0_34_0
IO_L2P_T0_34_0
IO_L3N_T0_DQS_34_0
IO_L3P_T0_DQS_34_0
IO_L4N_T0_34_0
IO_L4P_T0_34_0
IO_L5N_T0_34_0
IO_L5P_T0_34_0
IO_L6N_T0_VREF_34_0
IO_L6P_T0_34_0
IO_L7N_T1_34_1
IO_L7P_T1_34_1
IO_L8N_T1_34_1
IO_L8P_T1_34_1
IO_L9N_T1_DQS_34_1
IO_L9P_T1_DQS_34_1
IO_L10N_T1_34_1
IO_L10P_T1_34_1
IO_L11N_T1_SRCC_34_1
IO_L11P_T1_SRCC_34_1
IO_L12N_T1_MRCC_34_1
IO_L12P_T1_MRCC_34_1
IO_L13N_T2_MRCC_34_2
IO_L13P_T2_MRCC_34_2
IO_L14N_T2_SRCC_34_2
IO_L14P_T2_SRCC_34_2
IO_L15N_T2_DQS_34_2
IO_L15P_T2_DQS_34_2
IO_L16N_T2_34_2
IO_L16P_T2_34_2
IO_L17N_T2_34_2
IO_L17P_T2_34_2
IO_L18N_T2_34_2
IO_L18P_T2_34_2
IO_L19N_T3_VREF_34_3
IO_L19P_T3_34_3
IO_L20N_T3_34_3
IO_L20P_T3_34_3
IO_L21N_T3_DQS_34_3
IO_L21P_T3_DQS_34_3
IO_L22N_T3_34_3
IO_L22P_T3_34_3
IO_L23N_T3_34_3
IO_L23P_T3_34_3
IO_L24N_T3_34_3
IO_L24P_T3_34_3
+3V3
R2 681
R17 681
R23 681
R24 681
D8
D7
D6
D5
User LEDs
Title
FPGA-IO
Size
Number
Rev
Date
Drawn by
Filename
Sheet

Heatsink mounting holes/standoffs



Stencil Alignment Pads



Title Mechanical		
Size	Number	Rev
Date		Drawn by
Filename		Sheet

REV	Date	DESC
Z2	3/10/2019	Fixed faulty power supply wiring
Z1	10/15/2018	Initial release

Title		
Revision history		
Size	Number	Rev
2018-05-11		DPR
NiteFury		Sheet