Rev. 0.00

Data Sheet

S6B3306X11

Preliminary

MOBILE DISPLAY DRIVER IC

TRADEMARK & COPYRIGHT INFORMATION

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REVISION HISTORY

Rev.#	Date	History
0.00	2008.09.19	Initial release for review

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Preface

About This Data Sheet

This document is to provide a complete Data Sheet of S6B3306 IC design. It also provides useful information to those who works on a panel module or a set.

IMPORTANT NOTICE

Precautions against Light

The conductivity of a semiconductor is strongly influenced by electro-magnetic radiation such as visible light, infrared light, ultraviolet light, or gamma radiation. When light is absorbed, electron-hole pairs are generated raising the conductivity of the material, eventually altering the electrical characteristics of the IC. Therefore, if the packages that expose IC's to external light sources, such as COB, COG, TCP, and COF, are used, effective means to shield the IC from the light coming in all directions – top, bottom, and the sides – must be devised. Full observation of the following precautions is strongly recommended.

1. Make sure that the IC and substrate (board or glass) are protected from a stray light.
2. Always test and inspect products under the environment with no light penetration.

CHAPTER 1

OVERVIEW

1. OVERVIEW

1.1. INTRODUCTION

S6B3306 is a mid-display-size-compatible driver for liquid crystal dot matrix gray-scale graphic systems. With on-chip RC oscillator circuit, the display-timing signal is generated without being sent from MPU. Also, it is capable of using 8bit/16bit data bus alternatively and operating with 68/80-series MPU in asynchronous. Due to the LCD driving signal (132 RGB X 132 output) corresponding to the display data and the internal bit-map display RAM of 132 ×132 ×16-bit, S6B3306 is capable of operating maximum 132 RGB x 132 dot LCD panels in low-power consumption. Being the segment RGB 3-output, one pixel is 16-bit data and S6B3306 can max display 65,536 color.

1.2. PRODUCT OPTIONS

S6B3306 offers more than one option in order to meet customer-specific functions from the customers. Table 1 describes its functions.

Table 1. List of S6B3306 options

Options	Remarks
-X11	Reference design of S6B3306X11

1.3. FEATURES

S6B3306 offers the following key features:

- Driver Output
  - 132 RGB x 132
- Gray Scale Function
  - 65,536 color display of R: 32 gray scale, G: 64 gray scale, B: 32 gray scale
  - 4,096 color display of R: 16 gray scale, G: 16 gray scale, B: 16 gray scale
- On-chip Display Data RAM
  - Capacity: 132 x 16 x 132 = 278,784 bits
- Display Mode
  - Normal display mode: Entire duty displaying
  - Partial display mode: Partial duty displaying
  - Standby mode: Internal display clocks off
- MPU (Microprocessor) Interface
  - 8-bit/16 bit parallel bi-directional interface with 6800-series or 8080-series
  - 3/4 Pin SPI (only write operation)
- On-chip Low Power Analog Circuit
  - On-chip RC oscillator (Internal capacitor & resistor), external clock available
  - Voltage converter / Voltage regulator / Voltage follower
  - On-chip electronic contrast control
- Operating Voltage Range
  - VDD3 = 1.65 to 3.0 [V]
  - VIN1: 2.4 to 3.0 [V], VIN1R: 2.4 to 3.0 [V]
  - Display operating voltage (V1): 2.8 to 4.0 [V]
- Low Power Consumption
  - 900 μA Typ. (Refer to DC CHARACTERISTICS (2))
- Package Type
  - COG (Output Pad Pitch Min. 20 μm)

1.4. BLOCK DIAGRAM

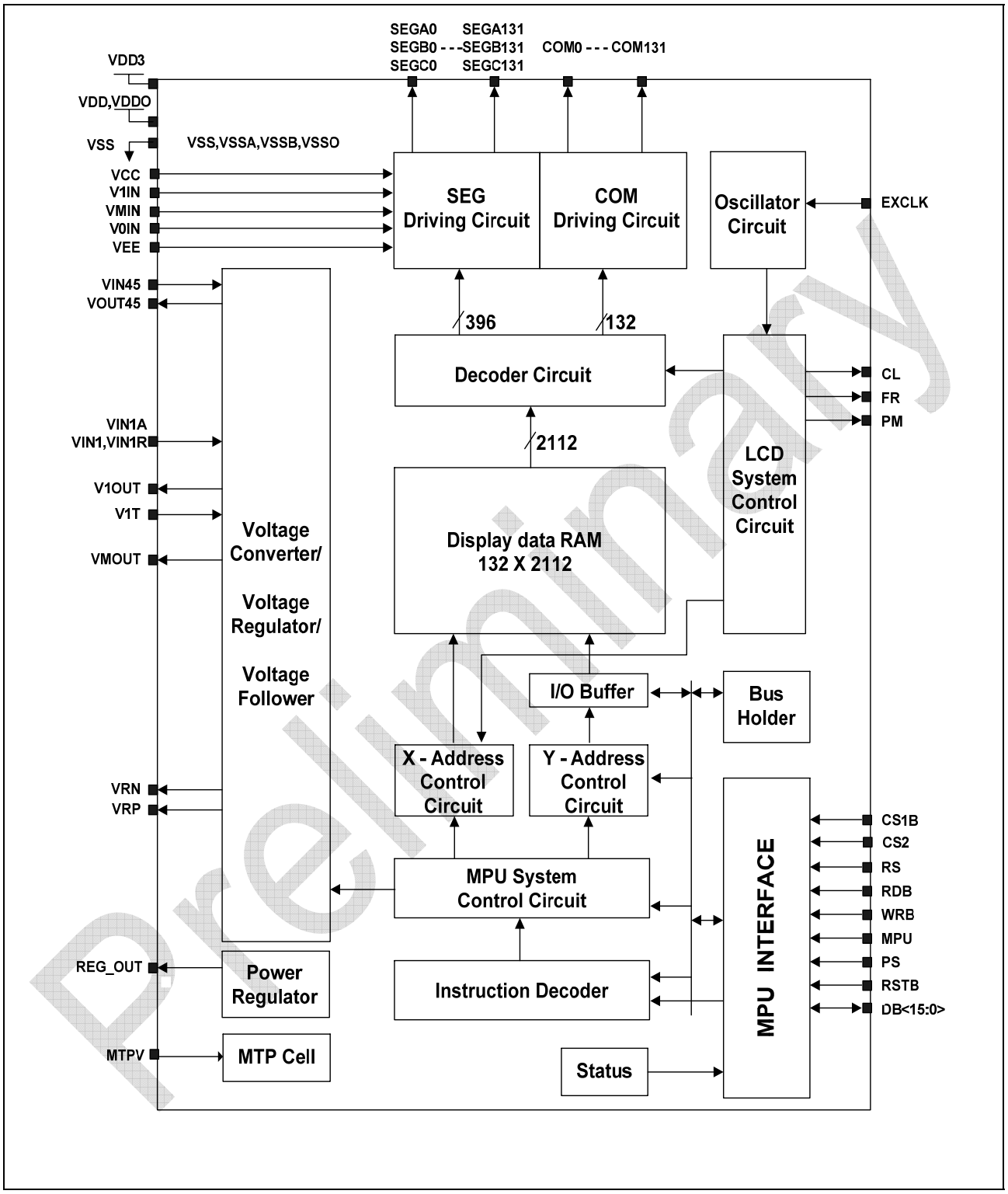


Figure 1. Block Diagram

1.5. PAD INFORMATION

1.5.1. Configuration of Signal Pads

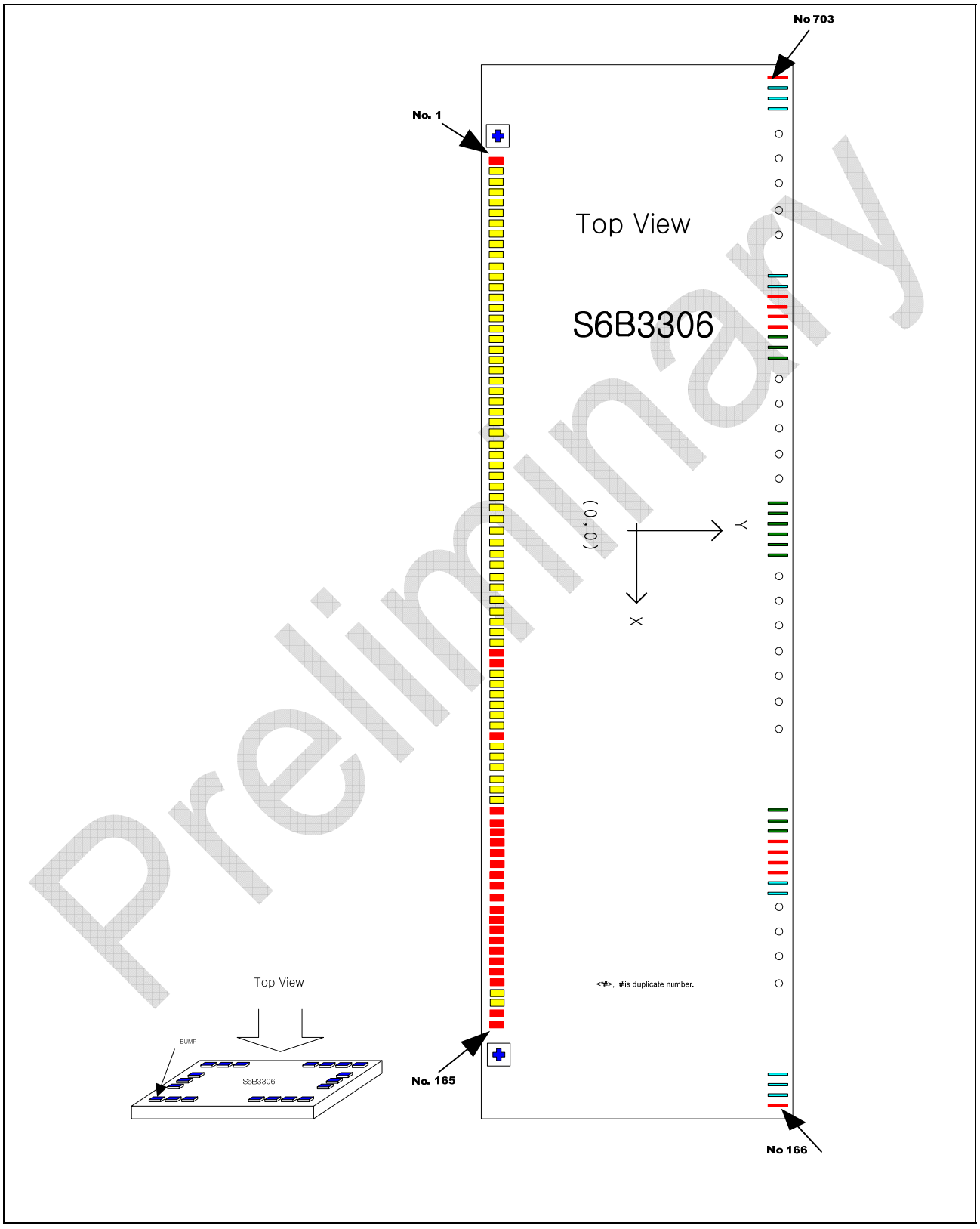


Figure 2. S6B3306 Chip pin configuration

1.5.2. Bump

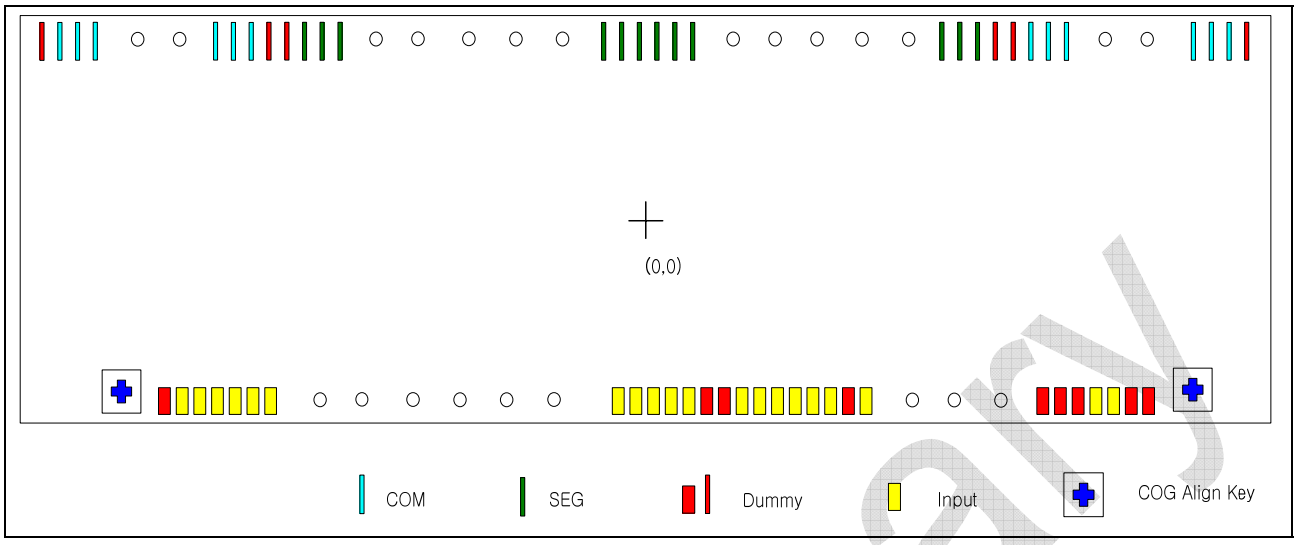


Figure 3. S6B3306 Chip Pad Configuration

Table 2. S6B3306 Pad Dimensions

Item	Pad No.		Size		Unit
			X	Y	
Chip size	-		10970	670	μm
Pad pitch	Input	(1~52,69~165)	60		
		(53~68)	85		
	Output	(166~171,710~715)	30		
		(172~709)	20		
Bumped Pad top size	Input	(1~165)	40 ±2	56 ±2	
	Output	(166~171,710~715)	120 ±2	10 ±2	
		(172~709)	10 ±2	120 ±2	
Bumped pad height	Height In Wafer		15±3		
	Tolerance In Chip		Under 2		
	Dimple Height		1.5		
Chip Thickness	-		Note2		

Note1: Scribe lane 80um included in this die size
Note2: Wafer Thickness can be varies based on the Customer's need.
- S6B3306●●●-●●●C : 300um

1.5.3. Align Key

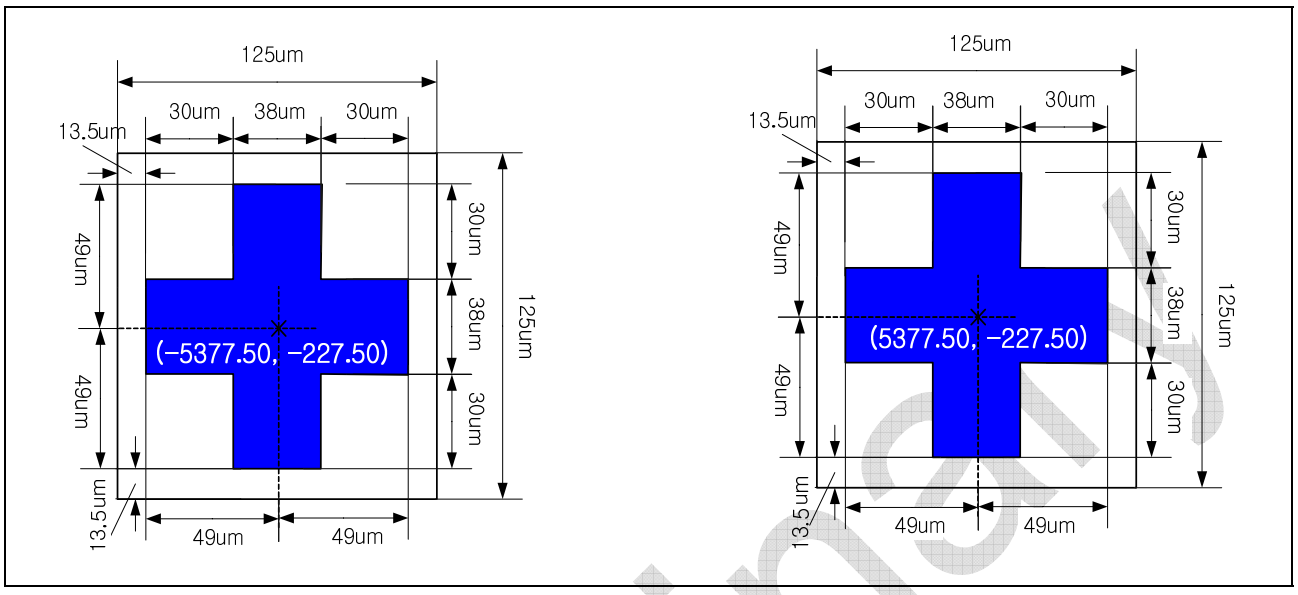


Figure 4. COG Align Key Coordinate

Note: When designing COG pattern, ITO pattern must be prohibited on BUMP, COG Align Keys, DUMMY pads, TEST pads. If ITO pattern is used for routing over these areas, it can be happened pattern-short through bumped pattern on these areas.

1.6. DESCRIPTION OF SIGNAL PADS

1.6.1. Power Supply Pins

Table 3. Power Supply Pins

Name	I/O	Description
VDD3	Supply	I/O power supply.
VIN1R	Supply	Internal regulator power supply This pin is connected to VIN1.
VDD	Supply	Regulated power supply input pin for internal digital and DDRAM block. This pin is connected to REG_OUT outside the chip with stabilization capacitor.
VDDO	Supply	Oscillator Power Supply. Connect to VDD
VSS, VSSO VSSA, VSSB	GND	Ground
VSS3	GND	I/O Ground (This pin is connected to VSS inside the chip and is the assistance pin for adjacent pins.)
V1IN	I	LCD segment high selected driving voltage input pin
V1OUT	O	LCD segment high selected driving voltage output pin
VMIN	I	LCD common non-selected driving voltage input pin
VMOUT	O	LCD common non-selected driving voltage output pin
V0IN	I	LCD segment low selected driving voltage input pin
VCC	I	LCD common high selected driving voltage input pin
VRP	O	LCD common high selected driving voltage output pin
VEE	I	LCD common low selected driving voltage input pin The relationship between VCC, V1, VM, V0 and VEE: VCC > V1 > VM > V0(=VSS) > VEE (V1 - VM = VM – V0, VCC –VM = VM - VEE)
VRN	O	LCD common low selected driving voltage output pin
VIN1, VIN1A	I	Power supply for 1’st booster circuit and VM amp
VOUT45	O	1’st booster output pin
VIN45	I	Power supply for V1 amp. Recommend to connect this pin to VOUT45
V1T	I	V1 voltage adjustment pin. It is valid only when the external temperature compensation circuit is used. Otherwise, the ITO pattern is recommended not to be made for this pin. Note : V1T is recommended to connect the external Cap. with GND if much noise is injected into this pin.

1.6.2. MPU Interface Pins

Table 4. MPU Interface Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin.
When RSTB is “L”, initialization is executed.</td></tr>
<tr><td rowspan="7">PS
MPU</td><td rowspan="7">I</td><td>MPU interface select pin
<table>
<tr><th>PS</th><th>MPU</th><th>Description</th></tr>
<tr><td>H</td><td>L</td><td>8080-parallel interface</td></tr>
<tr><td>H</td><td>H</td><td>6800-parallel interface</td></tr>
<tr><td>L</td><td>L</td><td>3 pin SPI (Write only)</td></tr>
<tr><td>L</td><td>H</td><td>4 pin SPI (Write only)</td></tr>
</table></td></tr>
<tr><td>NOTE: In serial mode, WRB and RDB must be fixed to either VDD3 or VSS3.</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pin.
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. When chip select is non-active, DB0 to DB15 are high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Display Data / Instruction select input pin
– RS = “H”: DB0 to DB15 are display data
– RS = “L”: DB0 to DB7 are instruction data
* When this pin is not used according to mode, these pins must be tied to VSS3. (In the case of 3Pin Serial I/F mode)</td></tr>
<tr><td rowspan="3">WRB
(R/W)</td><td rowspan="3">I</td><td>Read / Write execution control pin
<table>
<tr><th>PS</th><th>MPU</th><th>MPU Type</th><th>WRB</th><th>Description</th></tr>
<tr><td>H</td><td>H</td><td>6800-series</td><td>R/W</td><td>Read / Write control input pin
– R/W = “H”: read
– R/W = “L”: write</td></tr>
<tr><td>H</td><td>L</td><td>8080-series</td><td>WRB</td><td>Write enable clock input pin
The data on DB0 to DB15 are latched at the rising edge of the WRB signal.</td></tr>
</table></td></tr>
<tr><td rowspan="3">RDB
(E)</td><td rowspan="3">I</td><td>Read / Write execution control pin
<table>
<tr><th>PS</th><th>MPU</th><th>MPU Type</th><th>RDB</th><th>Description</th></tr>
<tr><td>H</td><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– R/W = “H”: When E is “H”, DB0 to DB15 are in an output status.
– R/W = “L”: The data on DB0 to DB15 are latched at the falling edge of the E signal.</td></tr>
<tr><td>H</td><td>L</td><td>8080-series</td><td>RDB</td><td>Read enable clock input pin
When RDB is “L”, DB0 to DB15 are in an output status.</td></tr>
</table></td></tr>
<tr><td>DB[15:8]
DB[7]/SDI
DB[6]/SCL
DB[5:0]</td><td>I/O</td><td>-DB[15:0]: 16-bit bi-directional data bus.
-SDI: Serial data input pin. The data is latched at the rising edge of SCL.
-SCL: Serial clock input pin.
* When these pins are not used according to mode, these pins must be connected to VSS3.</td></tr>
</table>

1.6.3. Display Pins

Table 5. Timing signal Pins for monitoring

Name	I/O	Description
CL	O	Shift clock output pin
PM	O	Field delimiter output pin
FR	O	Liquid crystal alternating current output pin

Table 6. LCD driver output pins

Name	I/O	Description
SEGA0 to 131	O	LCD driving segment outputs (Red or Blue)
SEGB0 to 131	O	LCD driving segment outputs (Green)
SEGC0 to131	O	LCD driving segment outputs (Blue or Red)
COM0 to 131	O	LCD common outputs

1.6.4. Miscellaneous Control Pins

Table 7. Oscillator and Power Regulator Pins

Name	I/O	Description
EXCLK	I	External clock input pin When an external input is used, it is input to this pin. But the internal oscillator is used, this pin is connected to VDD3 or VSS3.
REG_OUT	O	Internal voltage regulator output pin This pin is connected to VDD, VDDO, VDDM outside the chip with stabilization capacitor.
CID[1:0]	I	These pins assign ID[1:0] of status-read. This pin must be tied to VDD3 or VSS3.

Table 8. MTP pins

Name	I/O	Description
MTPV	I	Power of writing MTP cell (When this pin is not used, this pin must be floating)

Table 9. Test pins

Name	I/O	Description
TEST[2]	I	Don't use these pins. IC maker's test pins These pins must be tied to VDD3.
FUSE_EN	I	Don't use this pin. IC maker's test pin This pin must be tied to VDD3.
MODE[1:0]	I	Don't use these pins. IC maker's test pins These pins must be tied to VDD3.
ZIGZAG_MODE	I	COM group scan mode select pin. - ZIGZAG_MODE = H : COM group scanning operates in zigzag. In this mode, ZIGZAG_MODE pin is tied to VDD3. - ZIGZAG_MODE = L : COM group scanning operates in sequence. In this mode, ZIGZAG_MODE pin is tied to VSS3.
RTEST	I	Don't use this pin. IC maker's test pin This pin must be tied to VSS3.
DUMMY	-	This pin must be floating.

CHAPTER 2

ELECTRICAL SPECIFICATION

2. ELECTRICAL SPECIFICATION

2.1. ABSOLUTE MAXIMUM RATINGS

Table 10. Absolute maximum rating

Item	Symbol	Rating	Unit
Supply Voltage range	VDD3	-0.3 to +5.0	V
	VIN1	-0.3 to +5.0	V
LCD Supply Voltage range	|VCC – VEE|	25	V
Input Voltage range	Vin	- 0.3 to VDD3 +0.3	V
Operating Temperature range	TOPR	-30 to +70	°C
Storage Temperature range	TSTR	-55 to +150	°C

Note1: Absolute maximum rating is the limit value beyond which the IC may be broken. They do not assure operations.

Note2: Operating temperature is the range of device-operating temperature. They do not guarantee chip performance.

Note3: Absolute maximum rating is guaranteed when our company's package used.

Caution

Stresses above these absolute maximum ratings may cause permanent damage. These are stress ratings only and functional operation at these conditions is not implied. Exposure to maximum rating conditions for extended periods may reduce device reliability.

2.2. DC CHARACTERISTICS

2.2.1. DC Characteristics (1)

Table 11. DC characteristics

(VSS = 0V, VDD3 = 1.65 to 3.0V, Ta = -30 to 70 °C)

Item		Symbol	Condition	Min	Typ.	Max	Unit	Remarks
Operating voltage		VDD3		1.65		3.0	V	VDD3
Operating voltage		VIN1		2.4	2.8	3.0	V	VIN1, VIN1A
Operating voltage		VIN45		2.4	-	6.0	V	VIN45
Operating voltage		2Vr	2Vr = |VRP- VRN|	14	-	20	V	VRP, VRN
Output voltage		REG_OUT	REG_OUT voltage	1.5 ± 0.05			V	REG_OUT
Driving voltage input range (*1)		VM	External power supply mode	1.4		2.0	V	VM
		VCC		7.0		12.0	V	VCC
		VEE		-8.0		-4.5	V	VEE
Input voltage	High	VIH		0.8VDD3	-	VDD3	V	
	Low	VIL		VSS	-	0.2VDD3	V	
Output voltage	High	VOH	IOH = 0.5mA	0.8VDD3	-	VDD3	V	
	Low	VOL	IOL = -0.5mA	VSS	-	0.2VDD3	V	
Input leakage current		IIL	VIN = VDD or VSS	-1.0	-	+1.0	μA	
Output leakage current		IOZ	VIN = VDD or VSS	-3.0	-	+3.0	μA	
Oscillator Frequency Tolerance	Normal or Partial	FOSC1	(fFR=120Hz target), DSG=0, 132 display lines VDDO=1.5V, Temp=25°C	1534.5	1705	1875.5	kHz	
Driving voltage input range (*2)		V1 VM		2.8 1.4	-	4.0 2.0	V	

(*1) The Driving voltage range depend on the operating voltage (VIN1).

V1 < VIN1*2-1.05 (@Iload=250uA, V1 maximum voltage=4V)

VCC < VIN1*M_2-1.0 (@Iload=20uA, VCC maximum voltage=12V)

VEE > VIN1*(M_3) + 1.0 (@Iload=20uA, VEE minimum voltage=-8V)

→ M_2 and M_3 is Booster Boosting Ratio. (See Booster Boosting Set (70H))

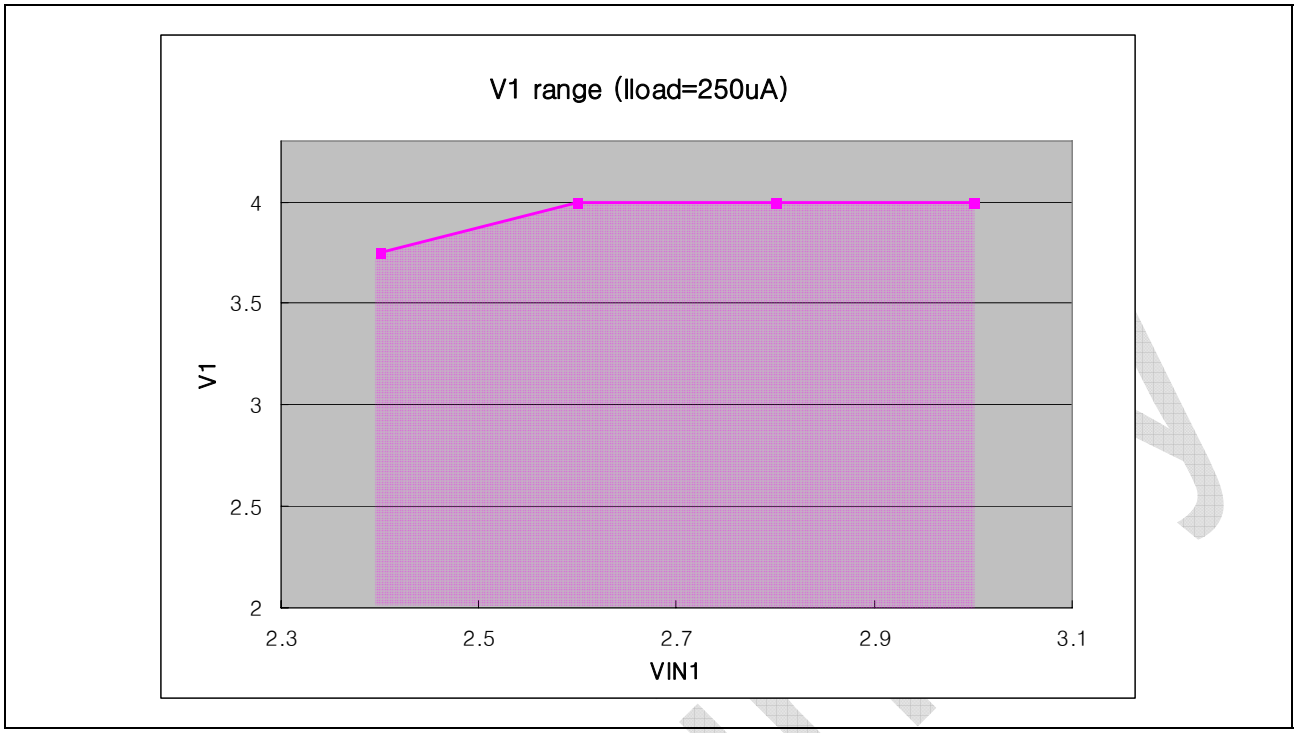


Figure 5. V1 < VIN1*2-1.05 (@Iload=250uA, V1 maximum voltage=4V)

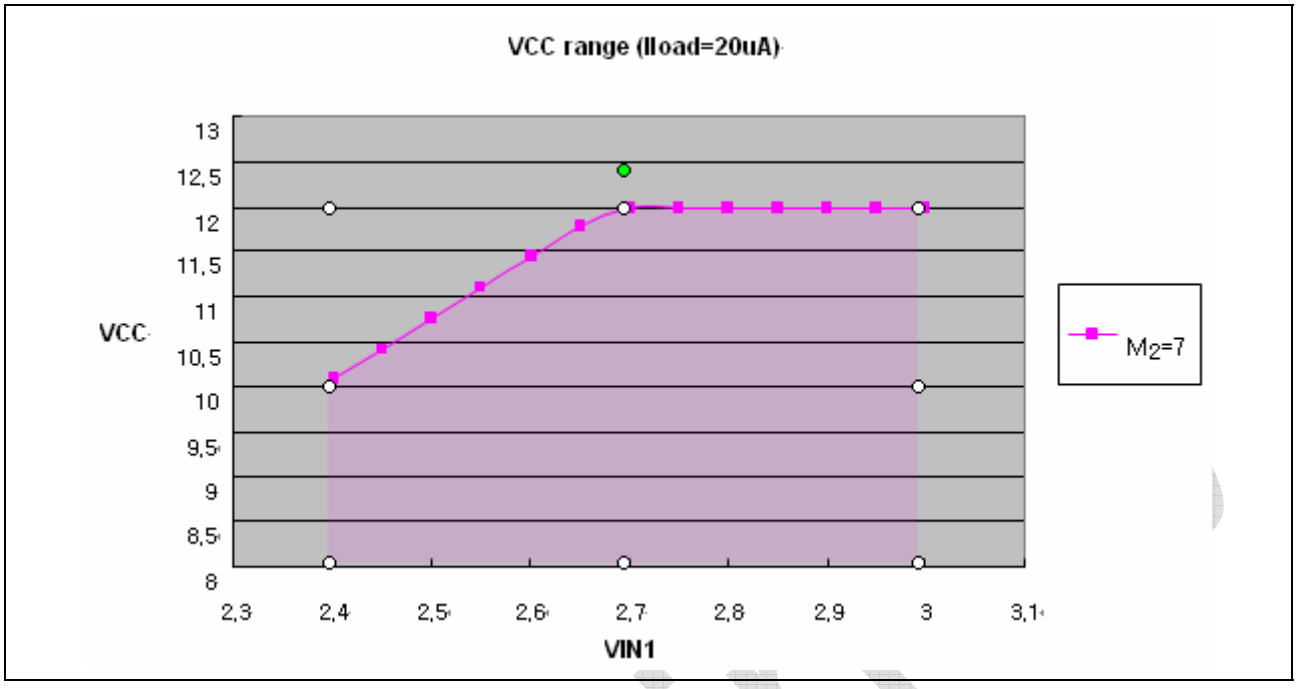


Figure 6. VCC < VIN1*M_2-1.0 (@Iload=20uA, VCC maximum voltage=12V)

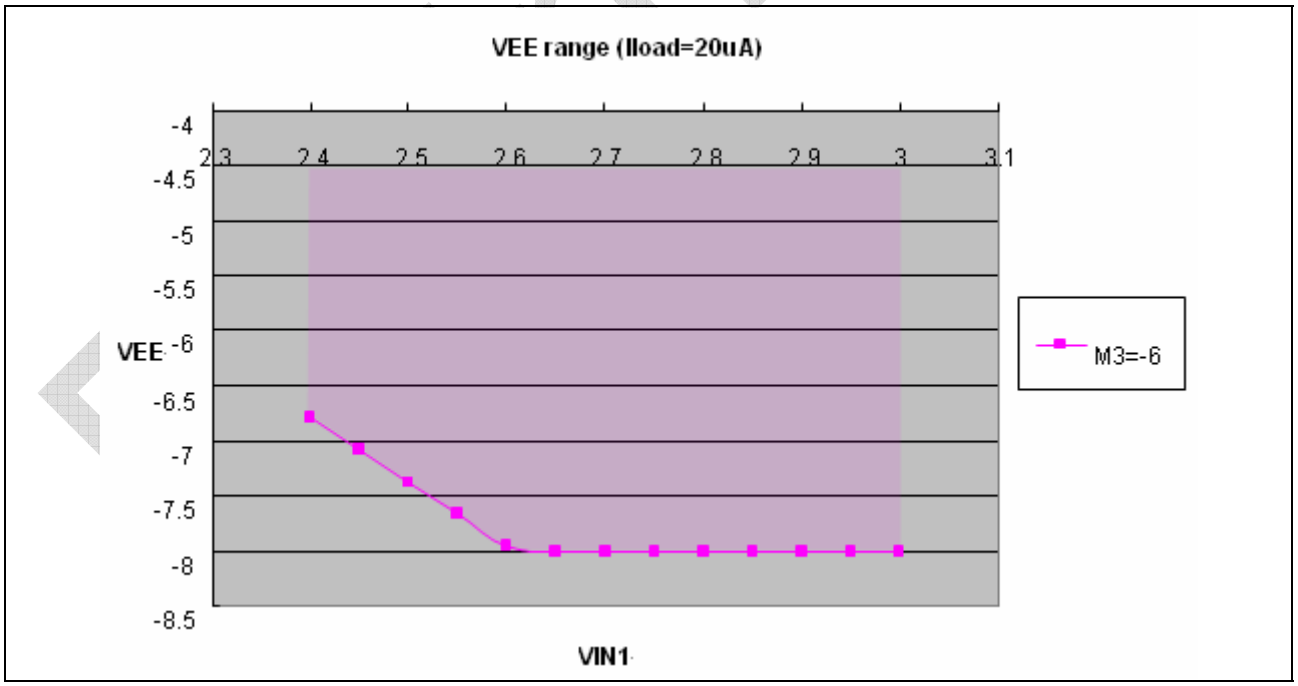


Figure 7. VEE > VIN1*(M3) + 1.0 (@Iload=20uA, VEE minimum voltage=-8V)

2.2.2. DC Characteristics (2)

Table 12. DC characteristics for LCD driver outputs

(VSS = 0V, VDD3 = 1.65 to 3.0V, VIN1=2.4 to 3.0V, Ta = -30 to 70 °C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Remarks
Driver output resistance	SEG	R_{ON-Seg}	V1=3.0 V, V0=0V, Ta = 25°C, Iload=50uA	-	1.5	2.0	kΩ	SEGn
	COM	R_{ON-Com}	VCC=9 V, VEE=-6.0V, Ta = 25°C, Iload=100uA	-	1.5	2.0	kΩ	COMn
Current consumption	Normal Mode	IDD	VDD3=VIN1=3.0V, V1=3.0V, Bias=1/5, DC=x2, Ta=25°C, Display line=132 DSG=0 (1dummy) fOSC=1705kHz (fFR=120Hz) No load, No access, All white pattern	-	900	1100	μA	VDD3 VIN1

* : “IDD” is determined from lowest power consumption for dc-dc converter.

2.2.3. DC Characteristics (3)

Table 13. DC characteristics for voltage shift range

(VSS = 0V, VDD3 = 1.65 to 3.0V, VIN1=2.4 to 3.0V, Ta = -30 to 70 °C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Voltage shift range(*1)	Δ VRP	Low current mode Isource = 20uA	-	-	200	mV	VRP
	Δ V1	Low current mode Isource = 250uA	-	-	50	mV	V1
	Δ VM	Low current mode Isource,sink = 250uA	-	-	50	mV	VM
	ΔVRN	Low current mode Isink = 20uA	-	-	200	mV	VRN

(*1) Voltage shift means output voltage deference between output current = Iload and no-load.
Refer to the following figure. (In case of source current mode)

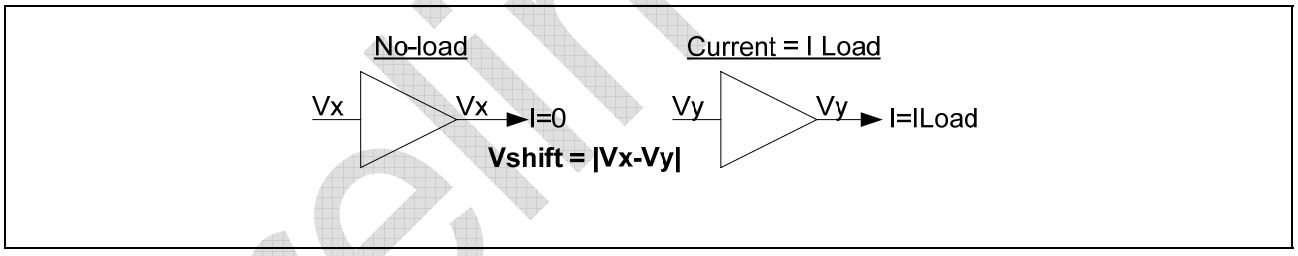


Figure 8. Voltage shift

Table 14. DC characteristics for bias ratio

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks
Tolerance of Bias ratio	Δ VRP_0 Δ VRN_0(*1)	No load	-200	-	+200	mV	VRP VRN

(*1) Tolerance of bias ratio definition

Δ VRP_0 = (VRP - VM) – VM *Bias

Δ VRN_0 = (VM - VRN) – VM *Bias

2.2.4. DC Characteristics (4)

Table 15. DC characteristics for voltage tolerance and offset

(VSS = 0V, VDD3 = 1.65 to 3.0V, VIN1=2.4 to 3.0V, Ta = 25°C)

Item	Symbol	Condition		Min	Typ	Max	Unit	Remarks
Temperature compensation	ΔVt	VDD3=VIN1=3.0V, 25°C to 70 °C		-0.02	-	+0.02	%/°C	V1
Tolerance of Contrast step of V1	ΔVstep			3.13	6.27	9.41	mV	V1
Voltage range	ΔV1 ΔVM	Contrast set = 7Fh	V1	3.95	4.0	4.05	V	V1
			VM	1.95	2.00	2.05	V	VM
		Contrast set = 00h	V1	2.75	2.80	2.85	V	V1
			VM	1.35	1.40	1.45	V	VM

Item			Condition		Max	Unit	Ref
			Load current	Voltage range			
Offset Voltage	‖VRP-VM‖ -‖VM - VRN‖		I Load = +20uA (VRP) I Load = -20uA (VRN)	VRP=7.0~12 V V1=2.8~4.0V VM=1.4~2.0V VRN=-4.5~-8.0 V	100	mV	Fig.1
	‖V1-VM‖ - ‖VM-V0‖	A	I Load = +100uA (V1, VM)		50	mV	Fig.2
		B	I Load = +100uA (VRP) I Load = -100uA (VRN)				

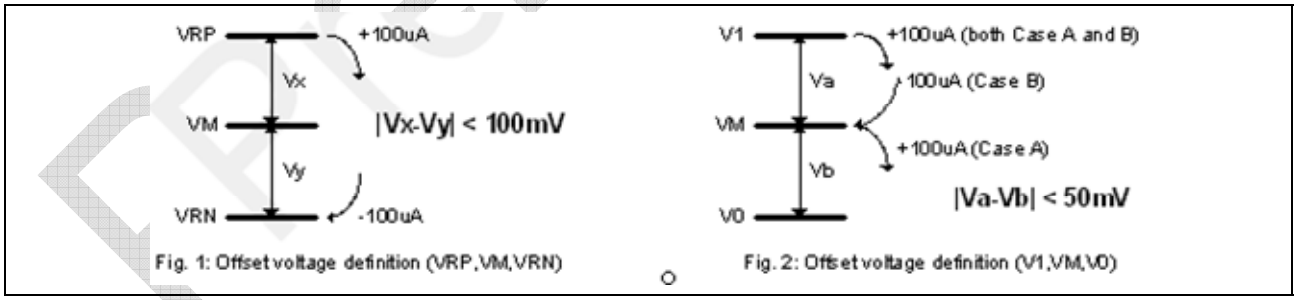


Figure 9. Offset Voltage

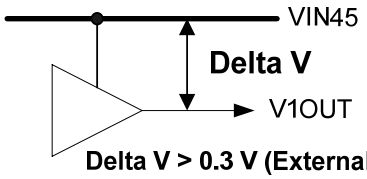
2.2.5. DC Characteristics (5)

Table 16. DC characteristics for voltage level

(VSS = 0V, VDD3 = 1.65 to 3.0V, VIN1=2.4 to 3.0V, Ta = -30 to 70 °C)

Item		Range	
		Min	Max (DC = X2.0)
Voltage Level	V1OUT	2.8 V	4.0 V(*1)
	VMOUT	1.4 V	2.0 V(*2)

(*1) This definition is shown as below



Delta V > 0.3 V (External VIN45)

Delta V > 0.5 V (VIN45 = VOUT45)

If V1OUT input voltage is set over VIN45, V1OUT output voltage must be clipped near VIN45. In this case, V1OUT output level must not be unstable. Refer to Fig.1

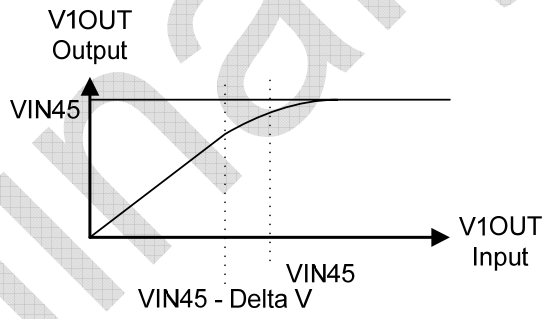
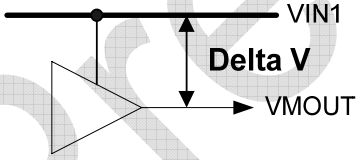


Fig. 1

(*2) This definition is shown as below



Delta V > 0.3 V

If VMOUT input voltage is set over VIN1, VMOUT output voltage must be clipped near VIN1. In this case, VMOUT output level must not be unstable. Refer to Fig.2

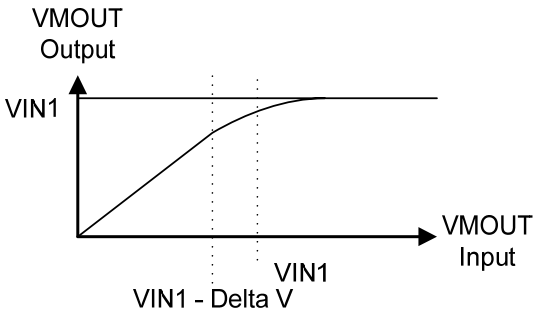


Fig. 2

Figure 10. DC characteristics for voltage level

2.3. AC CHARACTERISTICS

2.3.1. Read / Write Characteristics (8080-series MPU)

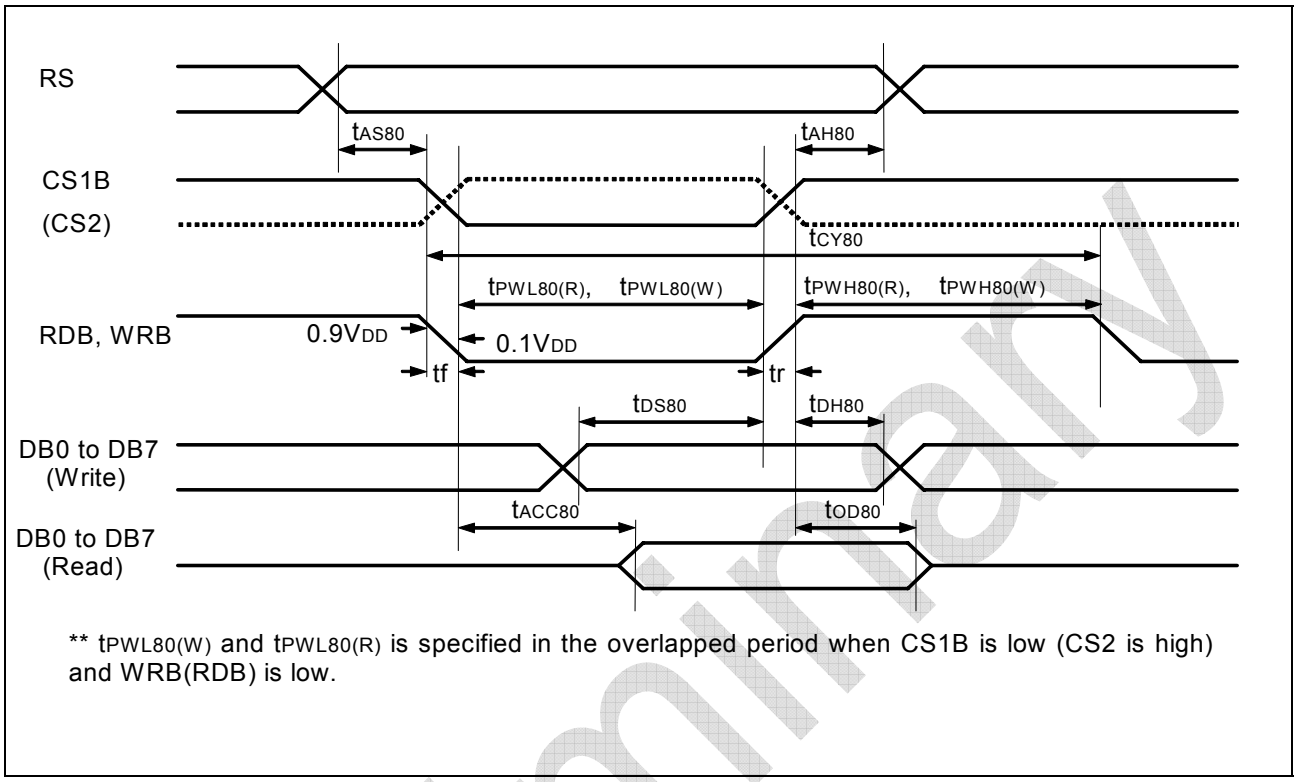


Figure 11. Parallel Interface (8080-series MPU) Timing Diagram

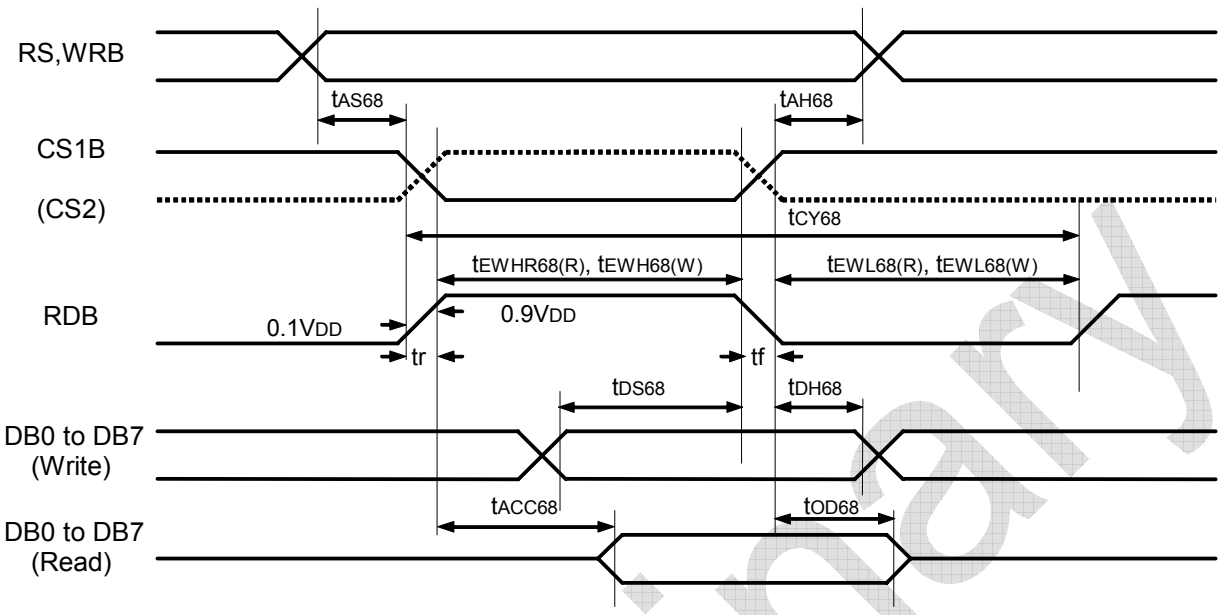
Table 17. AC Characteristics (8080-series Parallel Mode)

(VSS=0V, VDD3 = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Max	Unit
Address setup time Address hold time	RS	t_{AS80} t_{AH80}		0 0		ns
System cycle time(Write)		t_{CY80}		100		Ns
Pulse width low for write Pulse width High for write	WRB	$t_{PWL80(W)}$ $t_{PWH80(W)}$		40 40		Ns
Pulse width low for read Pulse width high for read	RDB	$t_{PWL80(R)}$ $t_{PWH80(R)}$		200 100		Ns
Data setup time Data hold time	DB0 to DB15	t_{DS80} t_{DH80}		10 10		Ns
Read access time		t_{ACC80}	CL = 50 pF		150	Ns
Output disable time		t_{OD80}	no load	20		Ns

NOTE : (tr + tf) < (tCY80 – tPWL80(W) – tPWH80(W)) for write,
(tr + tf) < (tCY80 – tPWLR80 – tPWHR80) for read

2.3.2. Read / Write Characteristics (6800-series MPU)



** $t_{EWH68(W)}$ and $t_{EWH68(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and RDB is high.

Figure 12. Parallel Interface (6800-series MPU) Timing Diagram

Table 18. AC Characteristics (6800-series Parallel Mode)

(VSS=0V, VDD3 = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Max	Unit
Address setup time Address hold time	RS WRB	tAS68 tAH68		0 0		Ns
System cycle time(Write)		tCY68		100		Ns
Enable width high for write Enable width low for write	RDB	tEWH68(W) tEWL68(W)		40 40		Ns
Enable width high for read Enable width low for read	RDB	tEWH68(R) tEWL68(R)		200 100		Ns
Data setup time Data hold time	DB0 to DB15	tDS68 tDH68		10 10		Ns
Read access time		TACC68	CL = 50 pF		150	Ns
Output disable time		tOD68	no load	20		Ns

NOTE: (tr + tf) < (tCY68 – tEWH68(W) – tEWL68(W)) for write,
(tr + tf) < (tCY68 – tEWH68(R) – tEWL68(R)) for read

2.3.3. Serial Data Interface (4 Pin) Timing

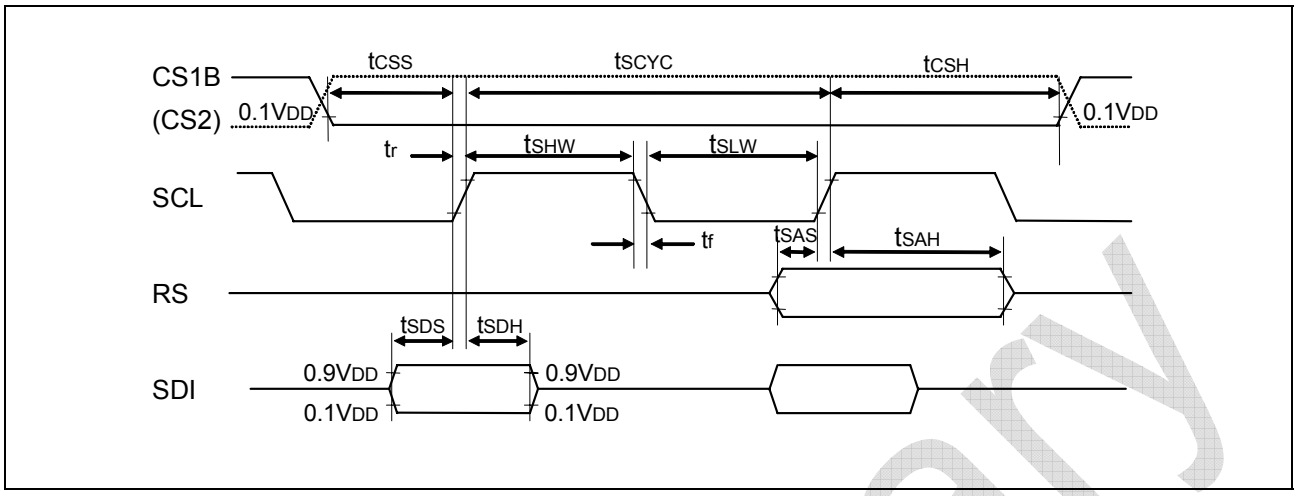


Figure 13. Serial Interface (4 Pin) Timing Diagram

Table 19. Serial Data Interface Timing

(VSS=0V, VDD3 = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Unit
SCL Cycle Time	SCL	tSCYC		75	ns
SCL High Pulse Width	SCL	tSHW		20	ns
SCL Low Pulse Width	SCL	tSLW		20	ns
SDI Setup time	SDI	tSDS		10	ns
SDI Hold time	SDI	tSDH		10	ns
RS Setup time	RS	tSAS		10	ns
RS Hold time	RS	tSAH		10	ns
Chip Select Setup time	CS1B (CS2)	tCSS		10	ns
Chip Select Hold time	CS1B (CS2)	tCSH		0	ns

NOTE: (tr + tf) < (tSCYC – tSHW – tSLW) for write,

2.3.4. Serial Data Interface (3 Pin) Timing

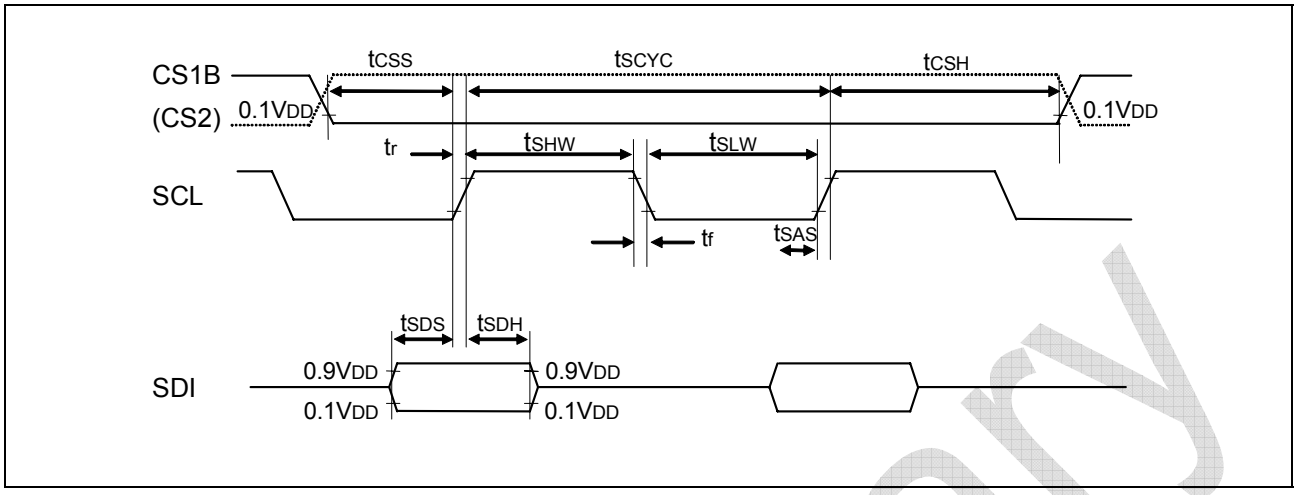


Figure 14. Serial Interface (3 Pin) Timing Diagram

Table 20. Serial Data Interface Timing

(VSS=0V, VDD3 = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min	Unit
SCL Cycle Time	SCL	tSCYC		75	ns
SCL High Pulse Width	SCL	tSHW		20	ns
SCL Low Pulse Width	SCL	tSLW		20	ns
SDI Setup time	SDI	tSDS		10	ns
SDI Hold time	SDI	tSDH		10	ns
Chip Select Setup time	CS1B (CS2)	tCSS		10	ns
Chip Select Hold time	CS1B (CS2)	tCSH		0	ns

NOTE: (tr + tf) < (tSCYC – tsHW – tSLW) for write,

2.3.5. Reset Input Timing

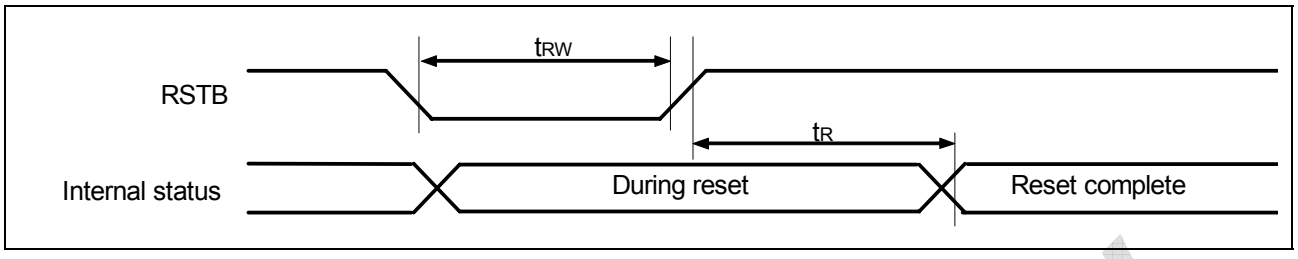


Figure 15. Reset Input Timing Diagram

Table 21. AC Characteristics (Reset mode)

(VSS=0V, VDD3 = 1.8V, Ta = -30 to +70°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RSTB	TRW		1000	-	ns
Reset time	-	tR		-	1000	ns

CHAPTER 3

INTERFACE

3. INTERFACE

3.1. MPU INTERFACE

3.1.1. Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B3306 can interface with an MPU only when CS1B is “L” and CS2 is “H”. When these pins are set to any other combination, RS, RDB, and WRB inputs are disabled and DB0 to DB15 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

3.1.2. Parallel/Serial Interface

The S6B3306 has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in Table 22.

Table 22. Parallel/Serial Interface-Mode.

PS	MPU	CS1B	CS2	MPU bus type
H	L	CS1B	CS2	8080-Series MPU
	H			6800-Series MPU
L	L	CS1B	CS2	3–Pin SPI
	H			4-Pin SPI

3.2. PARALLEL INTERFACE (PS="H")

The 8-bit/16-bit bi-directional data bus is used in parallel interface. The type of MPU is selected by MPU and the mode of data-bus is controlled by 16B register as shown in below. In accessing internal registers (RS = "L"), only DB[7:0] are valid. When 16B is high, DB[15:8] are high impedance.

Table 23. MPU Selection for Parallel Interface

MPU	16B	CS1B	CS2	RDB	WRB	Data Bus	MPU bus type
L	L	CS1B	CS2	RDB	WRB	DB[15:0]	8080-series MPU
	H					DB[7:0]	
H	L	CS1B	CS2	E	R/W	DB[15:0]	6800-series MPU
	H					DB[7:0]	

Table 24. Parallel Data Transfer

RS	6800-series		8080-series		Description
	E	R/W	RDB	WRB	
H	H	H	L	H	Read display data
H	H	L	H	L	Write display data
L	H	H	L	H	Read out internal status register
L	H	L	H	L	Write instruction data

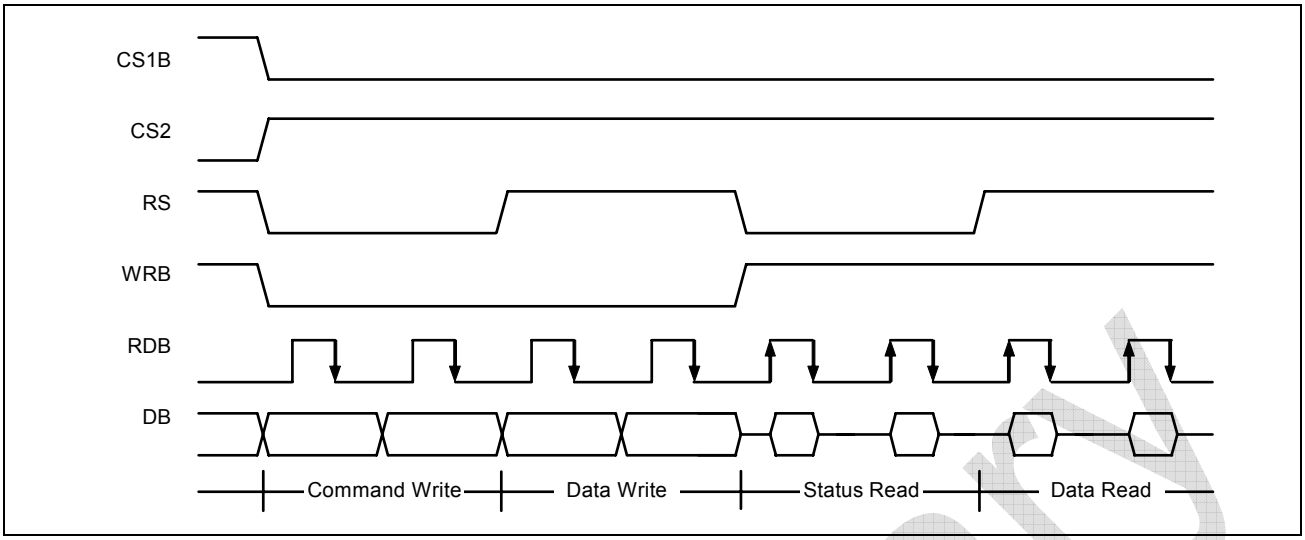


Figure 16. 6800-Series MPU Interface protocol (MPU="H")

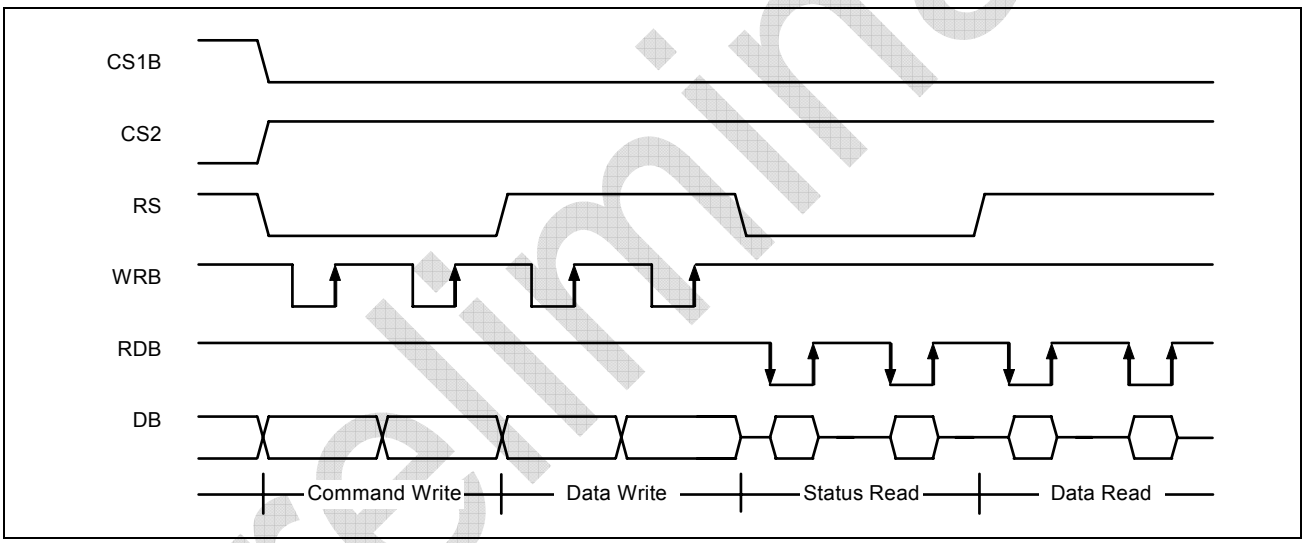


Figure 17. 8080-Series MPU Interface Protocol (MPU="L")

3.3. SERIAL INTERFACE (PS="L")

Communication with the MPU occurs via a clock-synchronized serial peripheral interface when PS is low. When using the serial interface, read operations are not allowed. When the chip select inputs are valid (CS1B = "L" & CS2 = "H"), the serial data is sent most significant bit first on the rising edge of a serial clock going into DB6 and processed as 8 bit parallel data on the eighth clock. Since the clock signal is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended. And Invalid, the internal shift register and the counter are reset.

The serial interface type is selected by setting PS as shown in Table25.

Table 25. MPU Selection for Serial Interface

PS	MPU	CS1B	CS2	RS	Serial Data	Serial Clock	SPI Mode
L	L	CS1B	CS2	By S/W	DB[7]	DB[6]	3-Pin
	H	CS1B	CS2	D/I			4-Pin

3.3.1. 3-Pin SPI Interface (PS = "L" & MPU = "L")

In 3-Pin SPI Interface mode, the first bit of serial 9 bits is used to indicate whether serial data input is display or instruction data instead of D/I pin. The serial data format consists of D/I (1bit) and DATA (8bits). For details, refer the Figure 18.

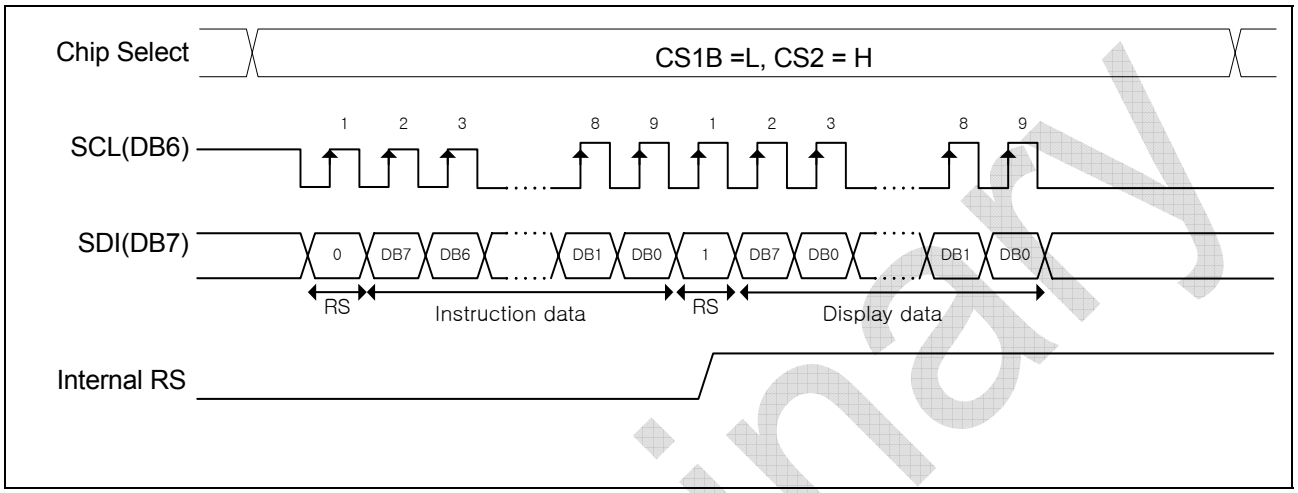


Figure 18. 3-Pin SPI Timing (RS is not used)

3.3.2. 4-Pin Serial Interface (PS="L" & MPU="H")

In 4-pin SPI interface mode, RS pin is used for indicating whether serial data input is display or instruction data. Data is display data when RS is high and instruction data when RS is low. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. For details, refer the Figure 19.

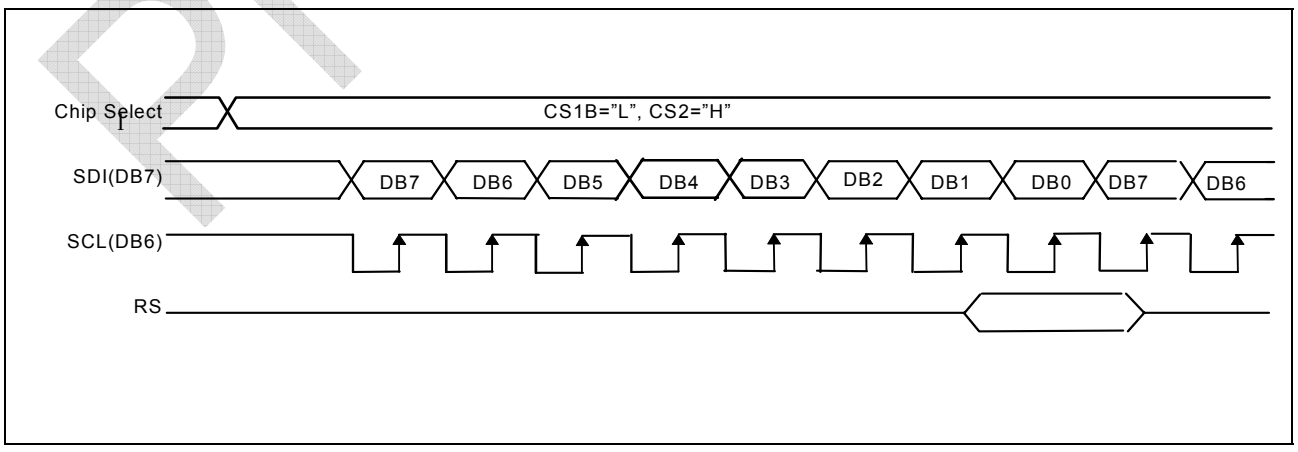


Figure 19. 4-Pin Serial Interface Timing

CHAPTER 4

FUNCTIONAL DESCRIPTION

4. FUNCTIONAL DESCRIPTION

4.1. DISPLAY DATA RAM

The on-chip display data RAM of S6B3306 is a static RAM that is stored the data for the display. It is a 2,112 x 132 structure. It is controlled by 2 addresses, X and Y. And, RAM area selection and automatic address count up functions are accomplished by the internal instructions.

4.1.1. DDRAM Address Area Selection

A part of DDRAM address area of S6B3306 can be accessed by X and Y address area settings. After setting RAM area, the addresses become the start address.

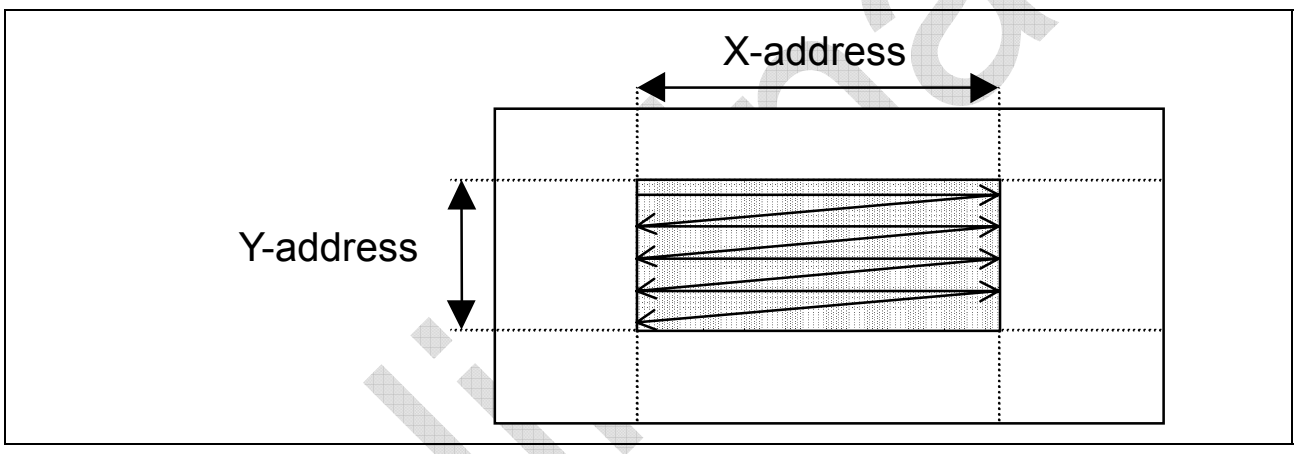


Figure 20. DDRAM Address Area

Table 26. Y address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	0	0	0	1	0
P1	Y start address set(Initial Status = 00H)							
P2	Y end address set(Initial Status = 83H)							

Table 27. X address Control

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	0	0	0	1	1
P1	X start address set (Initial status = 00H)							
P2	X end address set (Initial status = 83H)							

4.1.2. RAM Addressing Count up

By selecting the X address and Y address area by the internal instructions, the address counts up from its start address to end address after data access operation. When one address is equal to the end address, it returns to the start address. At this time, the other address is increased by 1.

4.1.3. X address count mode (X address = 00h to 83h, Y address = 00h to 83h)

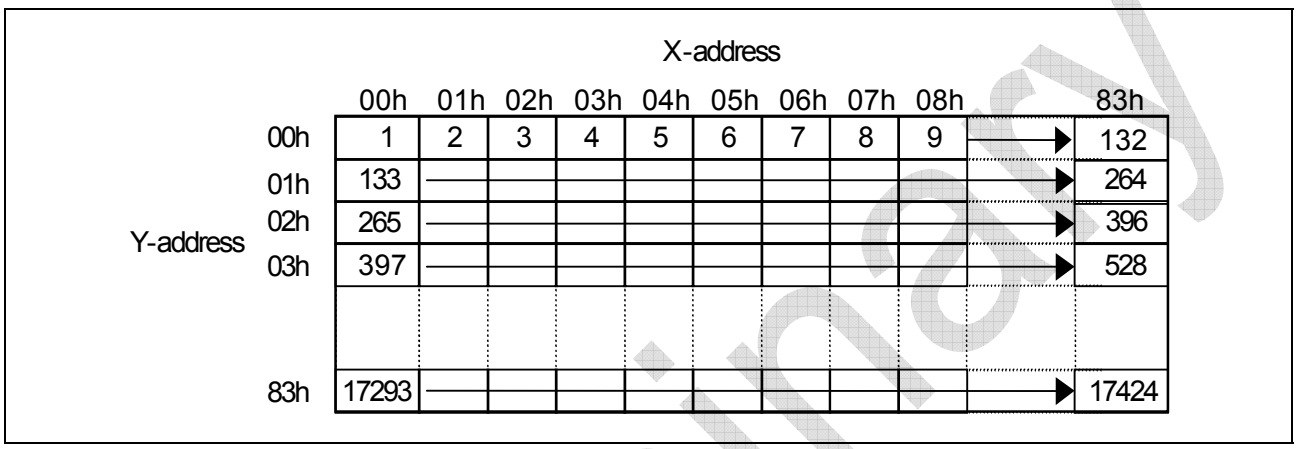


Figure 21. X address count mode

4.1.4. Y address count mode (X address =00h to 83h, Y address = 00h to 83h)

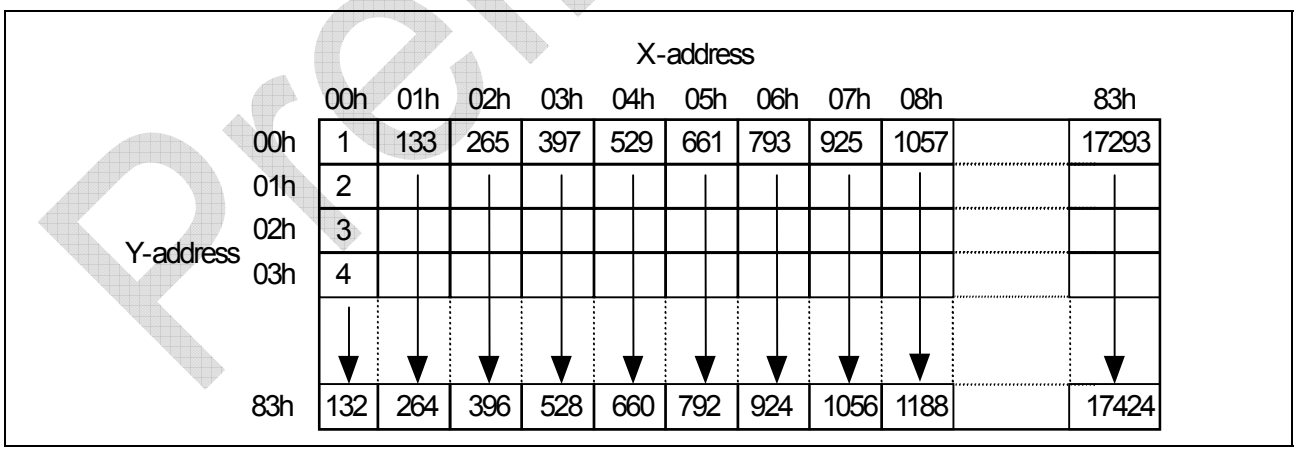


Figure 22. Y address count mode

YA Address	XA Address																
	00H	01H	02H	03H	04H	05H	06H	07H	08H	- - - - - - -	7DH	7EH	7FH	80H	81H	82H	83H
00H										- - - - - - -							
01H										- - - - - - -							
02H										- - - - - - -							
03H										- - - - - - -							
04H										- - - - - - -							
05H										- - - - - - -							
06H										- - - - - - -							
07H										- - - - - - -							
08H										- - - - - - -							
09H										- - - - - - -							
0AH										- - - - - - -							
0BH										- - - - - - -							
0CH										- - - - - - -							
0DH										- - - - - - -							
0EH										- - - - - - -							
0FH										- - - - - - -							
⋮										⋮							
74H										- - - - - - -							
75H										- - - - - - -							
76H										- - - - - - -							
77H										- - - - - - -							
78H										- - - - - - -							
79H										- - - - - - -							
7AH										- - - - - - -							
7BH										- - - - - - -							
7CH										- - - - - - -							
7DH										- - - - - - -							
7EH										- - - - - - -							
7FH										- - - - - - -							
80H										- - - - - - -							
81H										- - - - - - -							
82H										- - - - - - -							
83H										- - - - - - -							

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Red					Green						Blue				

Figure 23. Display Data RAM Map

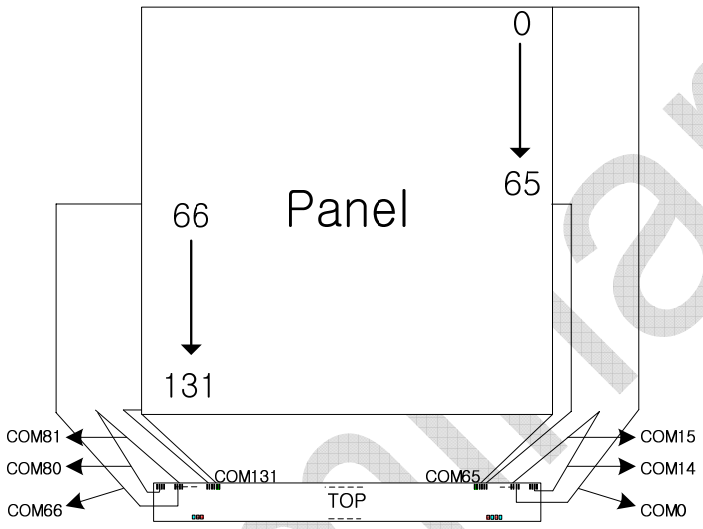
4.2. DISPLAY DIRECTION

4.2.1. COM Group Scan Mode

There is ZIGZAG_MODE pin for COM group scan mode selection.

ZIGZAG_MODE=0

COM group scanning operates in sequence.



ZIGZAG_MODE=1

COM group scanning operates in zigzag.

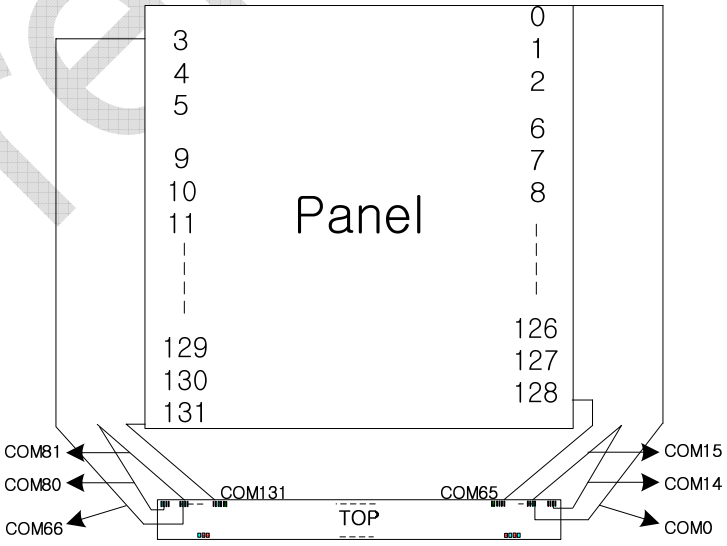


Figure 24. The relationship between COM outputs and Panel

4.2.2. The relationship between COM outputs and display line of panel (CDIR=0)

Table 28. The relationship between COM outputs and display line of panel

Display Line Number	Common Number ZIGZAG_ MODE=0	Common Number ZIGZAG_ MODE=1	Display Line Number	Common Number ZIGZAG_ MODE=0	Common Number ZIGZAG_ MODE=1	Display Line Number	Common Number ZIGZAG_ MODE=0	Common Number ZIGZAG_ MODE=1
Line Number0	COM0	COM0	Line Number45	COM45	COM87	Line Number90	COM90	COM45
Line Number1	COM1	COM1	Line Number46	COM46	COM88	Line Number91	COM91	COM46
Line Number2	COM2	COM2	Line Number47	COM47	COM89	Line Number92	COM92	COM47
Line Number3	COM3	COM66	Line Number48	COM48	COM24	Line Number93	COM93	COM111
Line Number4	COM4	COM67	Line Number49	COM49	COM25	Line Number94	COM94	COM112
Line Number5	COM5	COM68	Line Number50	COM50	COM26	Line Number95	COM95	COM113
Line Number6	COM6	COM3	Line Number51	COM51	COM90	Line Number96	COM96	COM48
Line Number7	COM7	COM4	Line Number52	COM52	COM91	Line Number97	COM97	COM49
Line Number8	COM8	COM5	Line Number53	COM53	COM92	Line Number98	COM98	COM50
Line Number9	COM9	COM69	Line Number54	COM54	COM27	Line Number99	COM99	COM114
Line Number10	COM10	COM70	Line Number55	COM55	COM28	Line Number100	COM100	COM115
Line Number11	COM11	COM71	Line Number56	COM56	COM29	Line Number101	COM101	COM116
Line Number12	COM12	COM6	Line Number57	COM57	COM93	Line Number102	COM102	COM51
Line Number13	COM13	COM7	Line Number58	COM58	COM94	Line Number103	COM103	COM52
Line Number14	COM14	COM8	Line Number59	COM59	COM95	Line Number104	COM104	COM53
Line Number15	COM15	COM72	Line Number60	COM60	COM30	Line Number105	COM105	COM117
Line Number16	COM16	COM73	Line Number61	COM61	COM31	Line Number106	COM106	COM118
Line Number17	COM17	COM74	Line Number62	COM62	COM32	Line Number107	COM107	COM119
Line Number18	COM18	COM9	Line Number63	COM63	COM96	Line Number108	COM108	COM54
Line Number19	COM19	COM10	Line Number64	COM64	COM97	Line Number109	COM109	COM55
Line Number20	COM20	COM11	Line Number65	COM65	COM98	Line Number110	COM110	COM56
Line Number21	COM21	COM75	Line Number66	COM66	COM33	Line Number111	COM111	COM120
Line Number22	COM22	COM76	Line Number67	COM67	COM34	Line Number112	COM112	COM121
Line Number23	COM23	COM77	Line Number68	COM68	COM35	Line Number113	COM113	COM122
Line Number24	COM24	COM12	Line Number69	COM69	COM99	Line Number114	COM114	COM57
Line Number25	COM25	COM13	Line Number70	COM70	COM100	Line Number115	COM115	COM58
Line Number26	COM26	COM14	Line Number71	COM71	COM101	Line Number116	COM116	COM59
Line Number27	COM27	COM78	Line Number72	COM72	COM36	Line Number117	COM117	COM123
Line Number28	COM28	COM79	Line Number73	COM73	COM37	Line Number118	COM118	COM124
Line Number29	COM29	COM80	Line Number74	COM74	COM38	Line Number119	COM119	COM125
Line Number30	COM30	COM15	Line Number75	COM75	COM102	Line Number120	COM120	COM60
Line Number31	COM31	COM16	Line Number76	COM76	COM103	Line Number121	COM121	COM61
Line Number32	COM32	COM17	Line Number77	COM77	COM104	Line Number122	COM122	COM62
Line Number33	COM33	COM81	Line Number78	COM78	COM39	Line Number123	COM123	COM126
Line Number34	COM34	COM82	Line Number79	COM79	COM40	Line Number124	COM124	COM127
Line Number35	COM35	COM83	Line Number80	COM80	COM41	Line Number125	COM125	COM128
Line Number36	COM36	COM18	Line Number81	COM81	COM105	Line Number126	COM126	COM63
Line Number37	COM37	COM19	Line Number82	COM82	COM106	Line Number127	COM127	COM64
Line Number38	COM38	COM20	Line Number83	COM83	COM107	Line Number128	COM128	COM65
Line Number39	COM39	COM84	Line Number84	COM84	COM42	Line Number129	COM129	COM129
Line Number40	COM40	COM85	Line Number85	COM85	COM43	Line Number130	COM130	COM130
Line Number41	COM41	COM86	Line Number86	COM86	COM44	Line Number131	COM131	COM131
Line Number42	COM42	COM21	Line Number87	COM87	COM108			
Line Number43	COM43	COM22	Line Number88	COM88	COM109			
Line Number44	COM44	COM23	Line Number89	COM89	COM110			

4.2.3. Display Direction

4.2.3.1. CDIR (ZIGZAG_MODE=0)

The CDIR flag of driver output mode set instruction selects the direction of common driver scanning. COM group scanning operates in sequence.

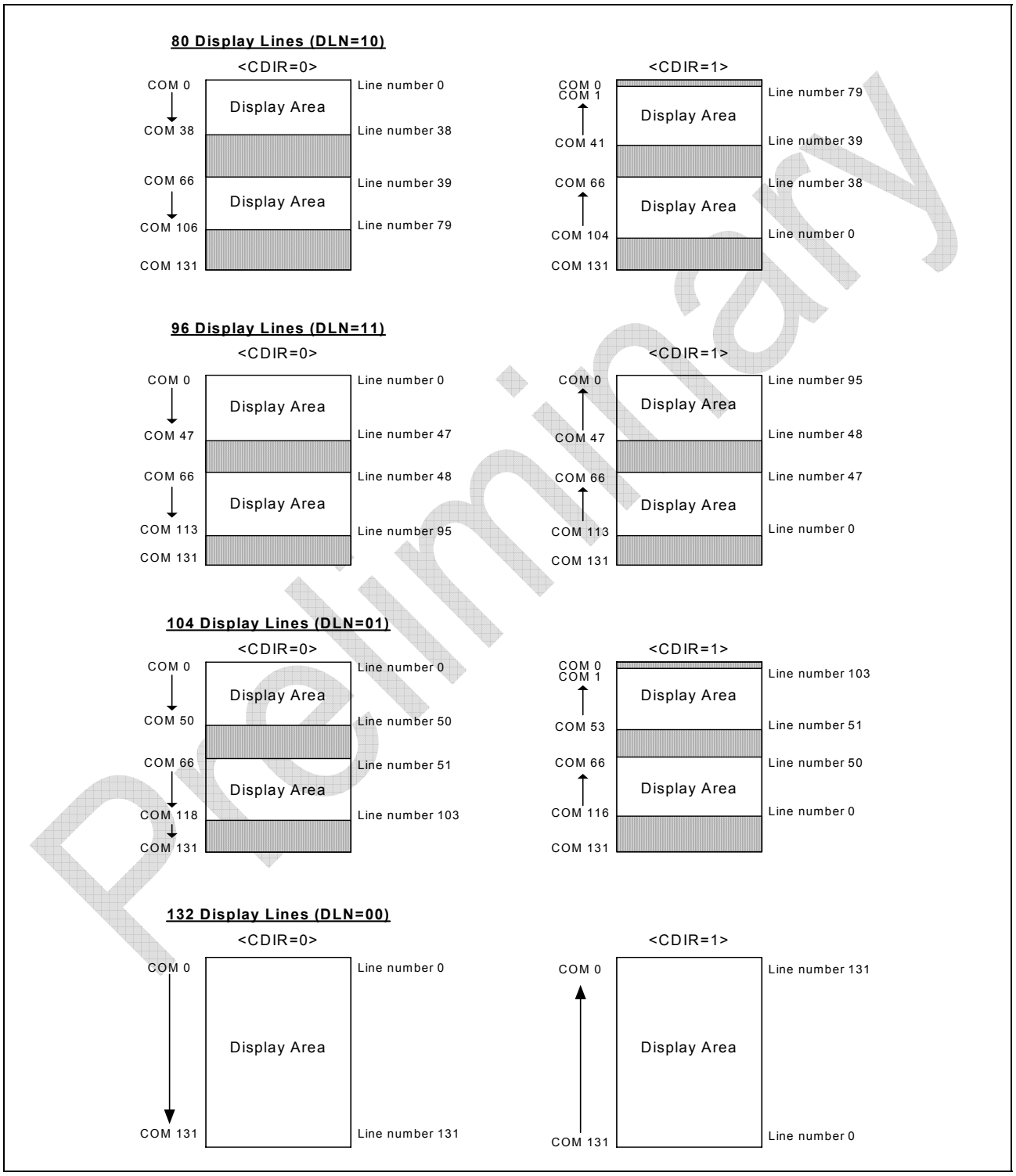


Figure 25. Direction of COM outputs (ZIGZAG_MODE = 0)

4.2.3.2. CDIR (ZIGZAG_MODE=1)

The CDIR flag of driver output mode set instruction selects the direction of common driver scanning.

COM group scanning operates in zigzag

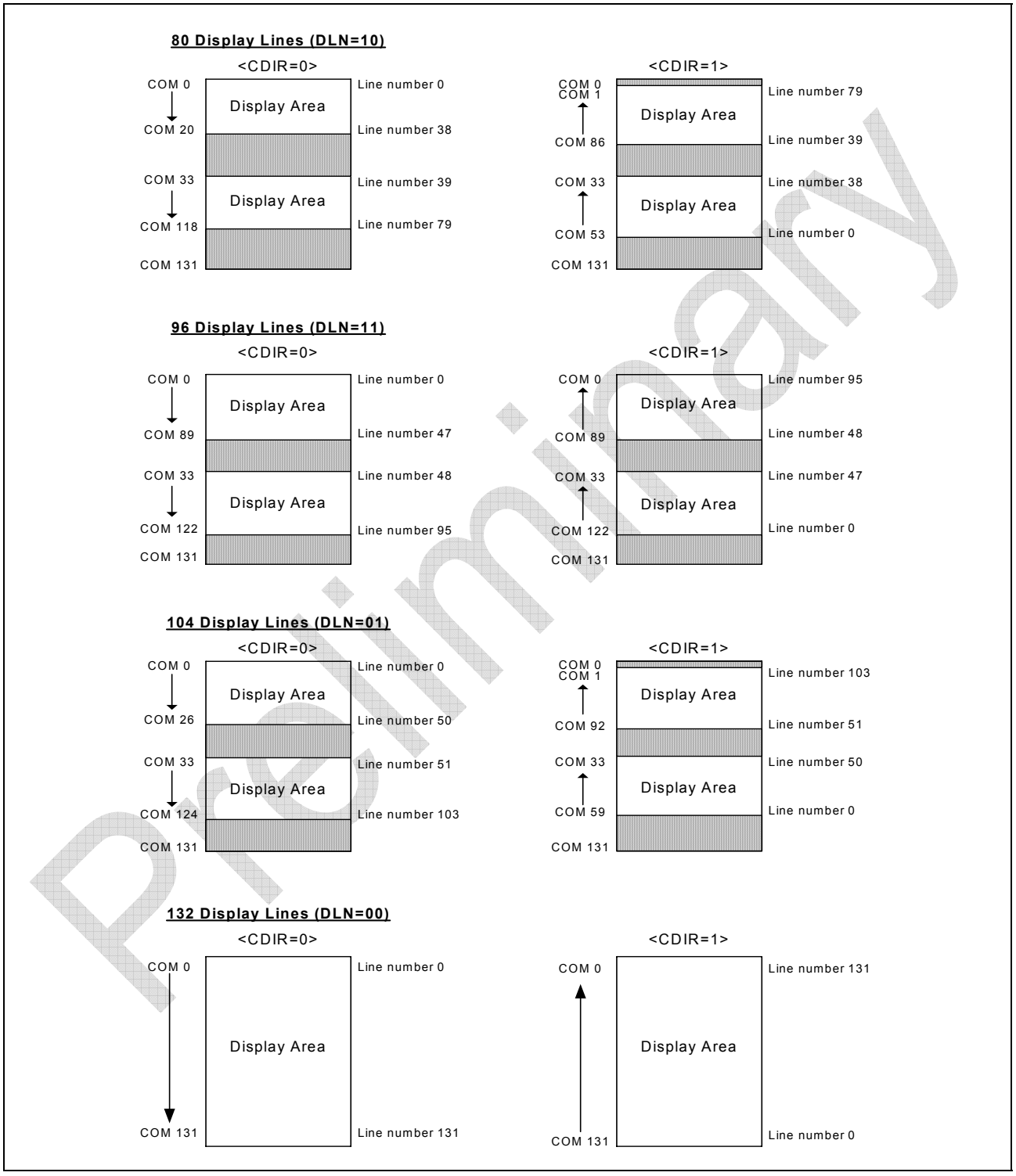
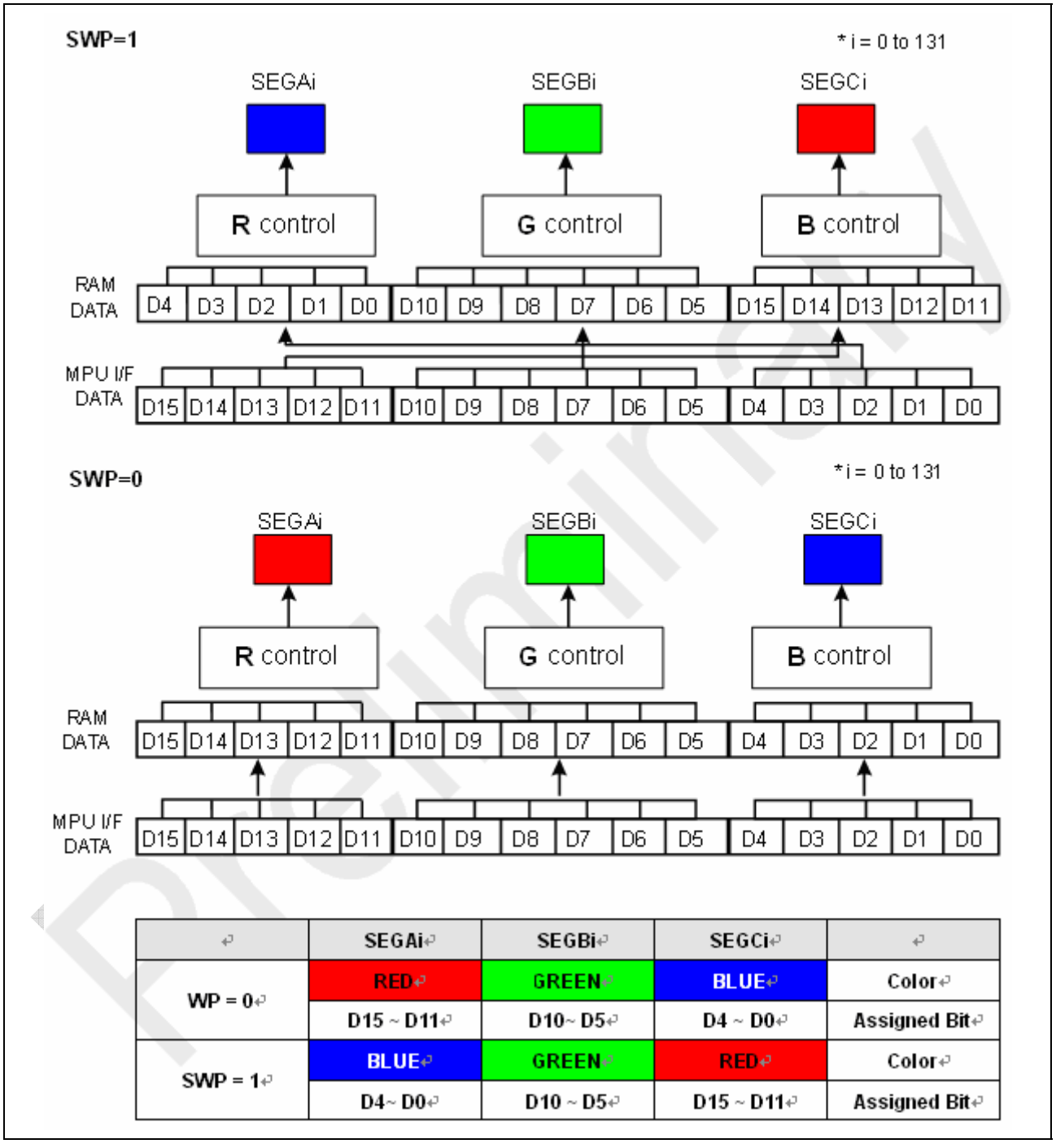


Figure 26. Direction of COM outputs (ZIGZAG_MODE = 1)

4.2.3.3. SWP Function

The SWP flag of Driver Output Mode Set instruction selects the swapping of segment display.



	SEGAi	SEGBi	SEGCi	
WP = 0	RED	GREEN	BLUE	Color
	D15 ~ D11	D10~ D5	D4 ~ D0	Assigned Bit
SWP = 1	BLUE	GREEN	RED	Color
	D4~ D0	D10 ~ D5	D15 ~ D11	Assigned Bit

Figure 27. The relationship between SEG outputs and RGB color

4.3. POWER ON/OFF SEQUENCE

4.3.1. Power On Sequence

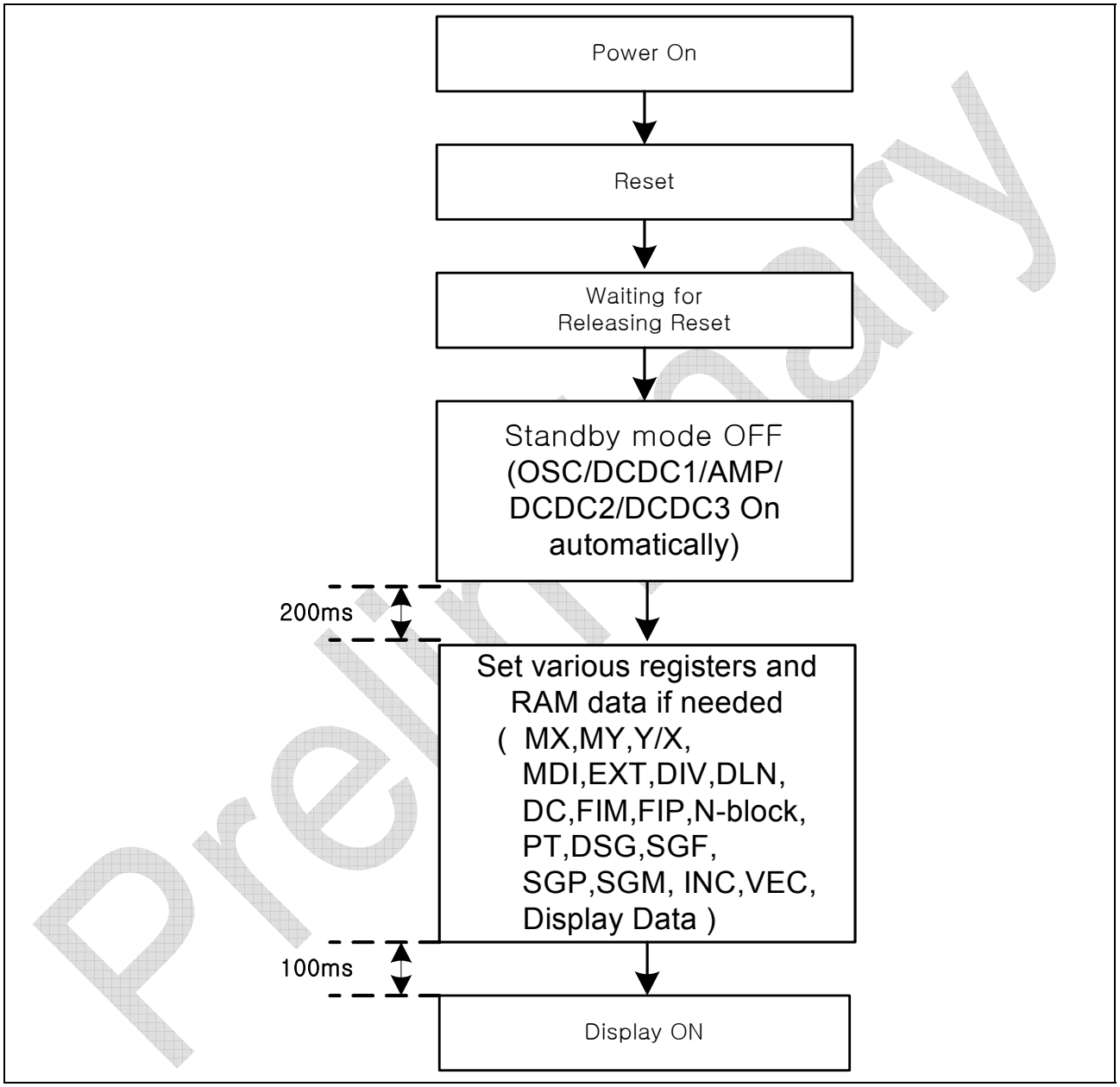


Figure 28. Power on sequence

4.3.2. External Power Input Sequence

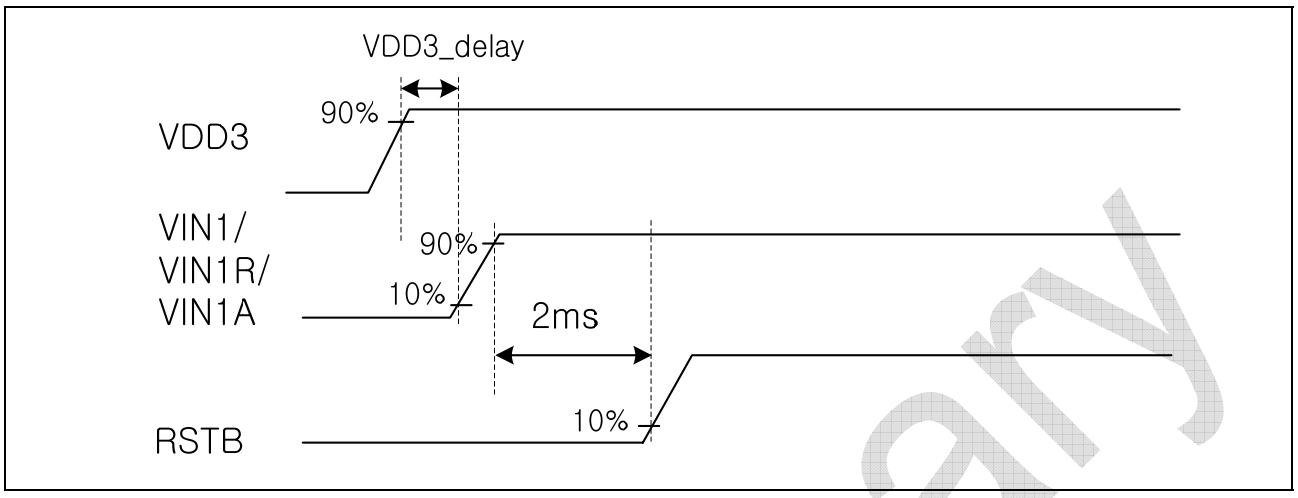
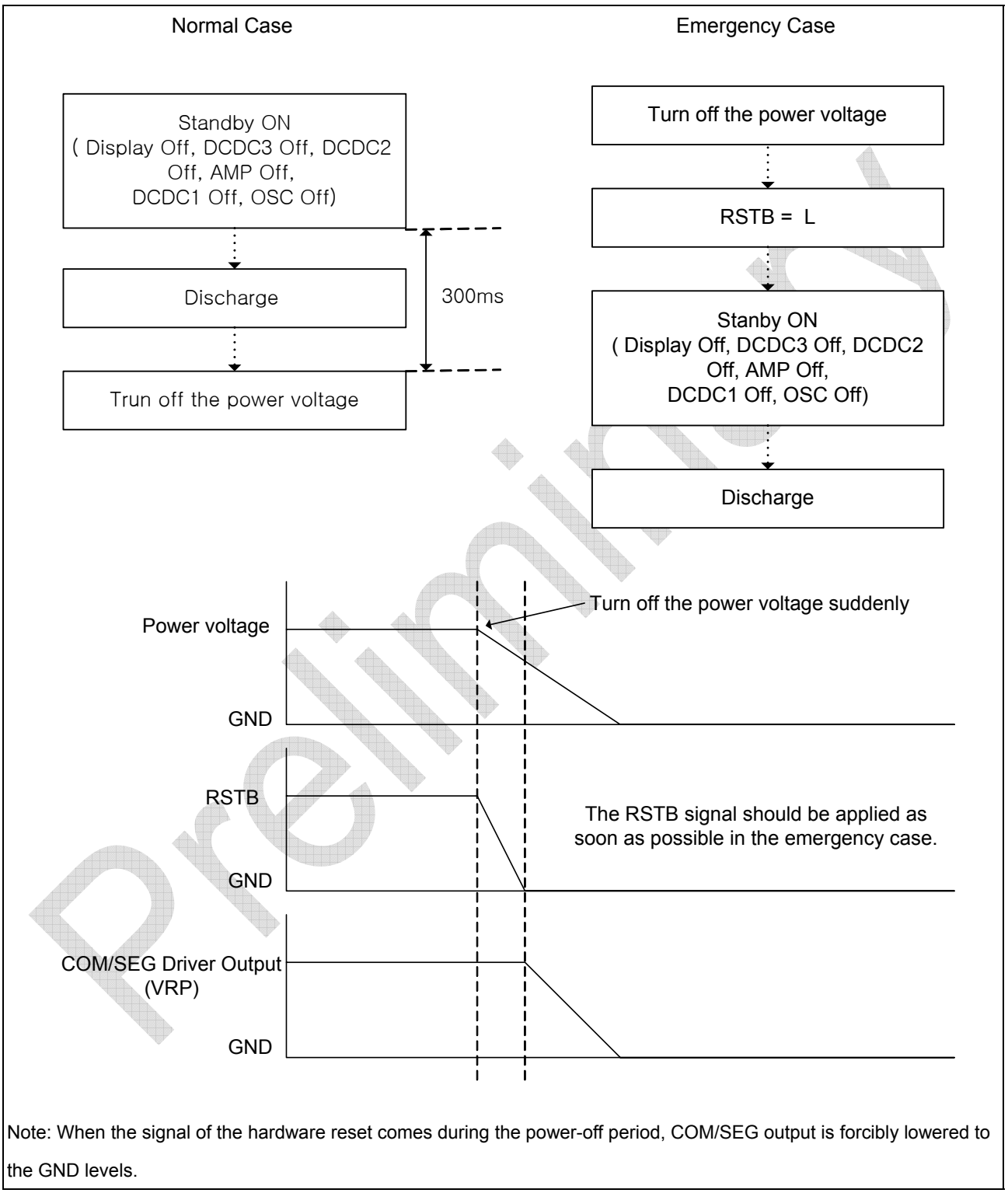


Figure 29. External power input sequence

VDD3 must be applied earlier than VIN1/VIN1R/VIN1A or at least applied simultaneously with these signals. When C1 of table24. External component is 1μF, RSTB must be applied after VIN1/VIN1R/VIN1A have been applied. The applied time gap between VIN1/VIN1R/VIN1A and RSTB is minimum 2ms. As C1 becomes larger, this time gap must be increased. Otherwise function is not guaranteed.

4.3.3. Power Off Sequence



Note: When the signal of the hardware reset comes during the power-off period, COM/SEG output is forcibly lowered to the GND levels.

Figure 30. Power off sequence

4.3.4. External Power Off Sequence

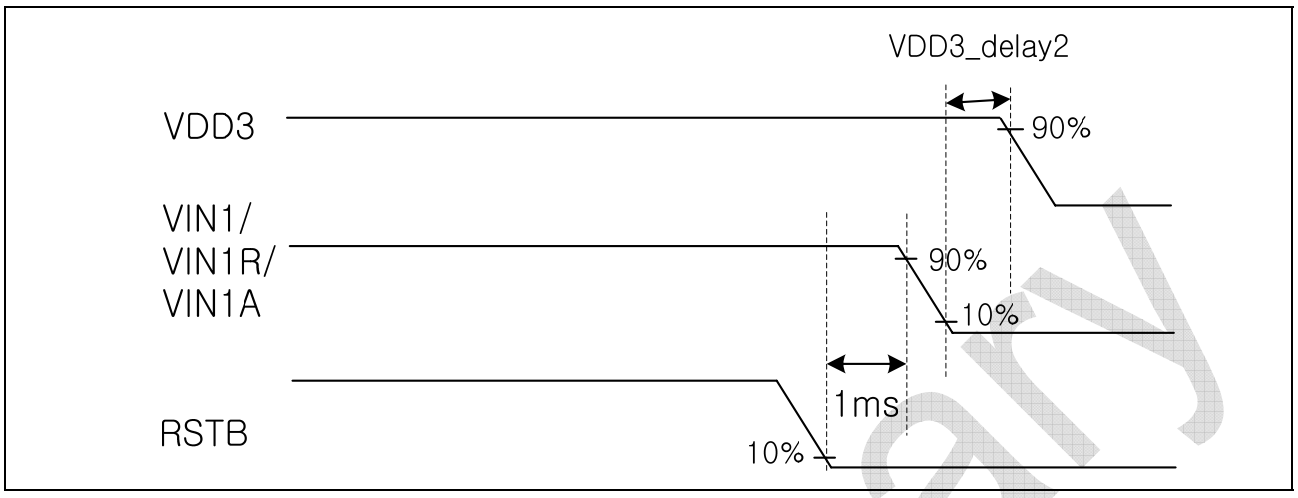


Figure 31. External power off sequence

VDD3 must be powered down later than VIN1/VIN1R/VIN1A or at least powered down simultaneously with these signals. VIN1/VIN1R/VIN1A must be powered down after RSTB have been powered down. The time gap of powered down between RSTB and VIN1/VIN1R/VIN1A is minimum 1ms. Otherwise function is not guaranteed.

4.3.5. Wake up Sequence

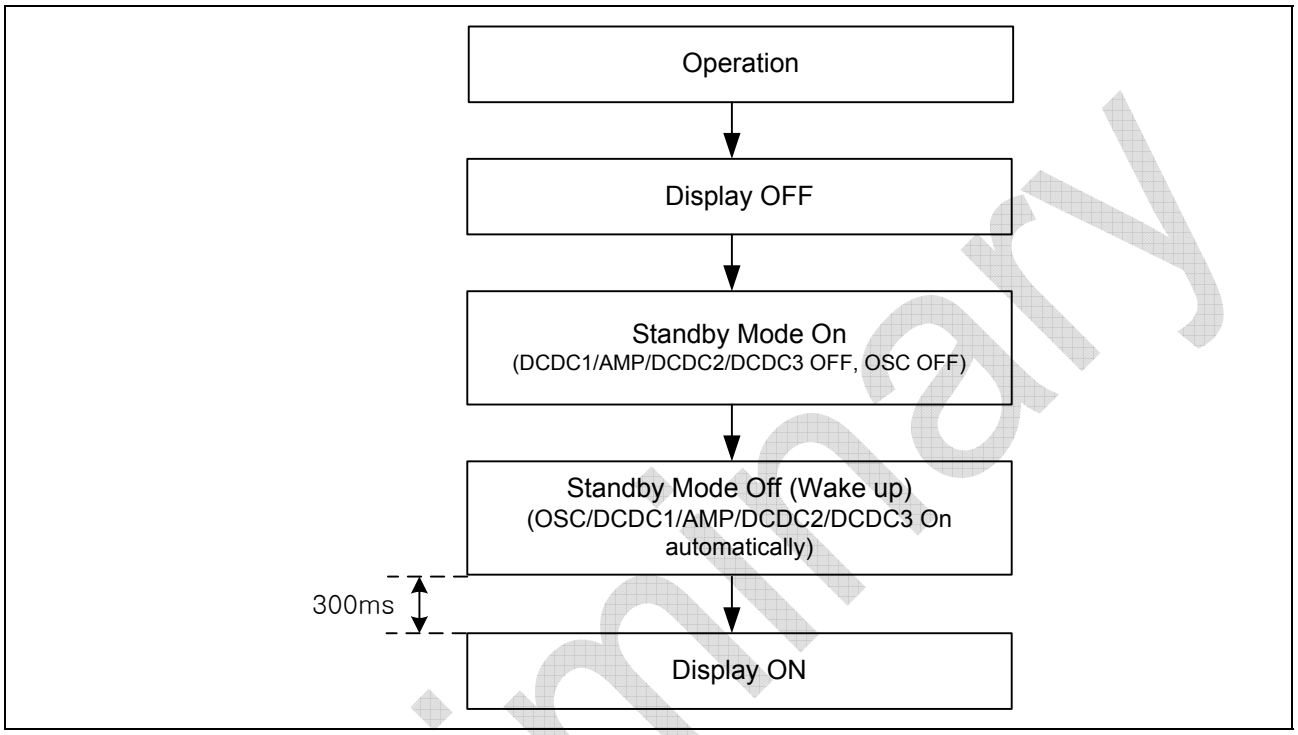


Figure 32. Wake up sequence

4.4. MTP CALIBRATION MODE

4.4.1. Sequence for Setting the Modified Electronic Volume

Next figure is a Block Diagram of Sequence for Setting the Modified Electronic Volume.

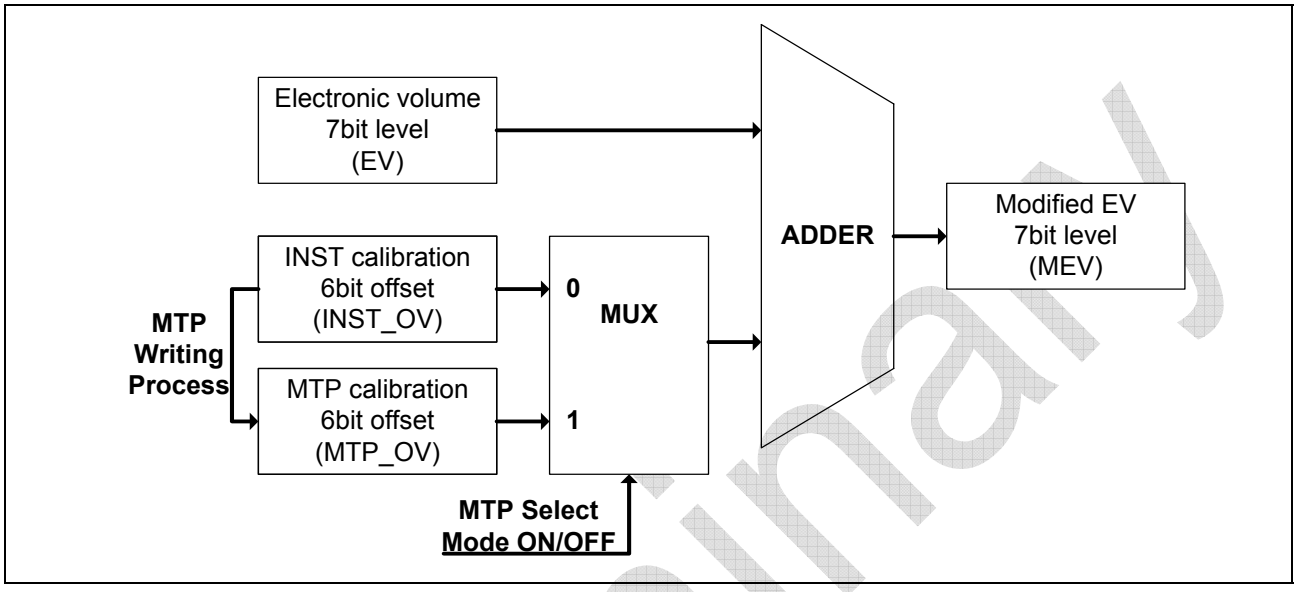


Figure 33. Sequence for Setting the Modified Electronic Volume

Initially, MTP cell is not programmed and has 6'b000000 value. When the external reset is applied, MTP select mode is On. MEV is EV + MTP_OV. Since MTP_OV is 6'b00000, MEV is EV. For V1OUT calibration, the instruction "MTP select mode off" is executed, and then MEV is EV + OV and user can adjust MEV value using the instruction "Set offset volume register". When MEV overflows or underflows, MEV will be saturated. Repeat this step until end of the calibration. If V1OUT calibration is suitable, MTP writing process is executed, and then MTP cell is programmed and MTP_OV is programmed with OV. Finally, V1OUT calibration process is finished. Again, when the external reset is applied, MTP select mode is ON. MEV is EV + MTP_OV. Accordingly MEV is the EV that has always the offset with MTP_OV value. However, if programmed MTP_OV is unlike, the instruction "MTP select mode off" can be executed and then MEV will be EV + OV. Accordingly OV can be adjusted with instructions although MTP cell is programmed.

4.4.2. EEPROM Cell Structure

MTP (Multi Time Programmable) has been implemented on the S6B3306. The EEPROM stores the offset volume for V1OUT calibration after the device has been assembled and calibrated on a LCD module. For MTP programming, MTPV pin is used. These pin should be available to on the module glass by ITO.

The MTP block of the S6B3306 consists of 7 bits. 1 bit is used for MTP mode protection bit (MPRT), and 6 bits are used for V1OUT calibration (MOV5~MOV0). MPRT can be read or written automatically in this LSI.

4.4.2.1. EEPROM block

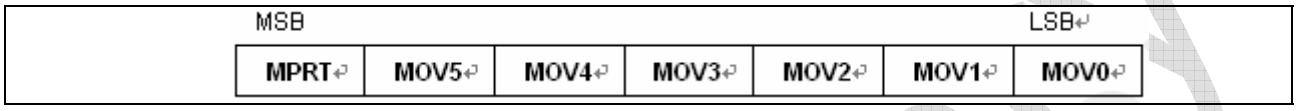


Figure 34. EEPROM block

4.4.2.2. Description

MPRT: The Offset Volume(OV) can be written to EEPROM cells only when MPRT bit = '0'

MOV5~MOV0: The MOV is used for calibrating the V1OUT voltage as an offset to the EV register value.

4.4.3. V1OUT Calibration flow

V1OUT may be calibrated with MTP in the following order.(ex : EV = 32, OV=-3)

Table 29. MTP calibration flow

STEP	RS	RW	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	Description
1.											Execute MTP erase sequence.
2.											Apply external reset. (MTP data load)
3.	0	0	0	0	1	0	1	0	1	0	Set contrast control using instruction.
	0	0	0	0	1	0	0	0	0	0	(EV = 32)
4.	0	0	1	1	1	0	1	0	1	0	MTP select mode off by using the instruction.
5.	0	0	1	1	1	0	1	1	0	1	Set offset volume by using the instruction.
	0	0	0	0	1	1	1	1	0	1	(OV = -3)
6.											Repeat STEP 4. Until the end of the calibration.
7.	0	0	0	0	1	0	1	1	0	1	Standby on by using the instruction.
8.											Apply programming voltages for MTP programming. (MTPV=17V±500mV) Wait 1ms or more.
9.	0	0	1	0	0	0	1	1	0	0	Preliminary Command.(8Ch)
	0	0	0	0	0	0	1	1	1	1	Preliminary parameter. (0Fh)
10.	0	0	1	1	1	0	1	1	1	1	Set MTP write enable. (Only available when MPRT= 0). Wait 100ms ~ 200ms.
11.	0	0	1	1	1	0	1	1	1	0	Set MTP write disable. Wait 1ms or more.
12.											Cut off programming voltages for MTP programming (MTPV)
13.											Apply external reset.

After the external reset, the calibrated data are automatically transferred to the 6-bit reference voltage control register.

*MTP_WRITING PROCESS is available when MPRT is zero (if MPRT = 1, MTP cell could not be programmed).

4.4.4. MTP Erase Sequence

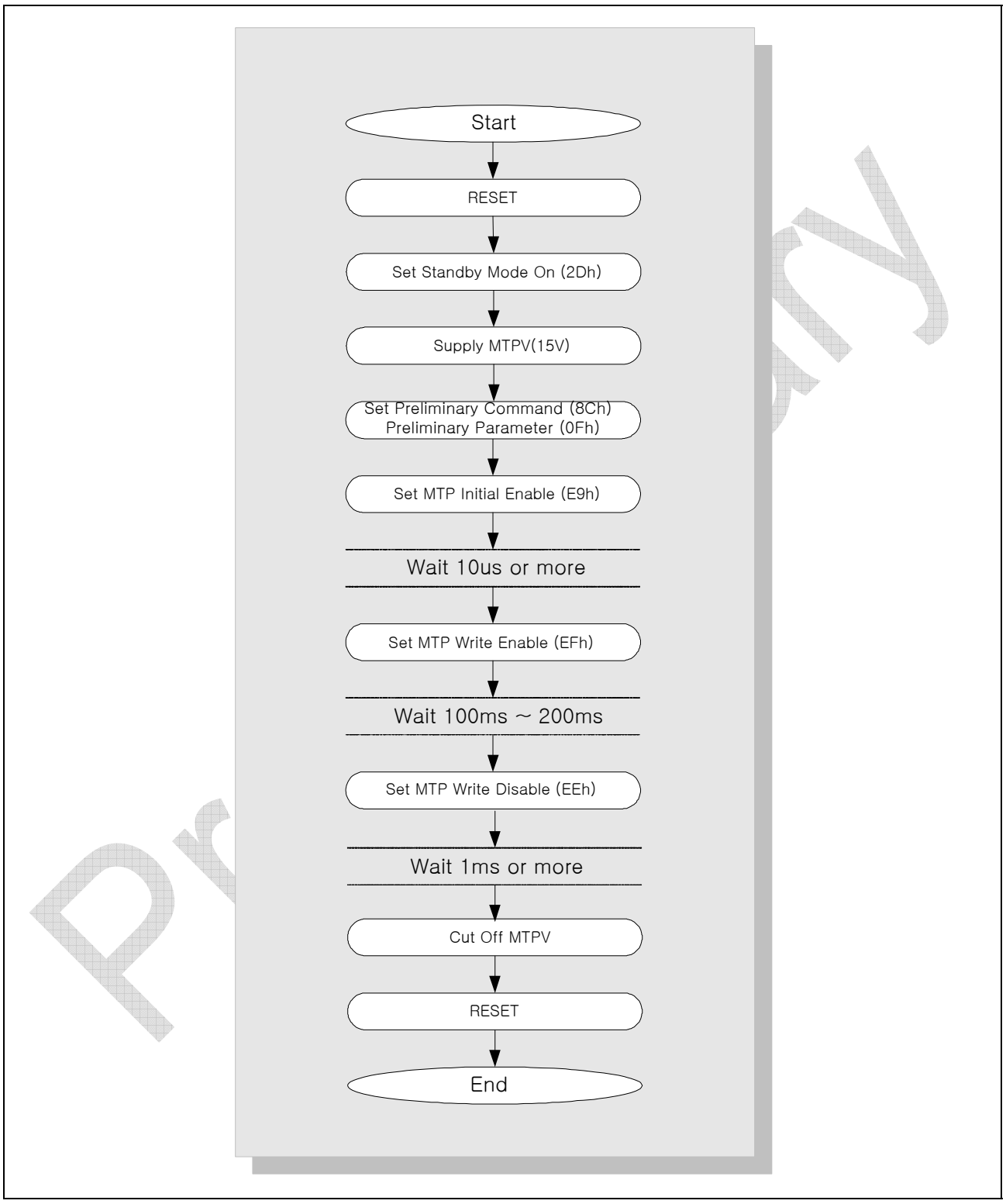


Figure 35. MTP erase sequence

4.4.5. MTP Write Sequence

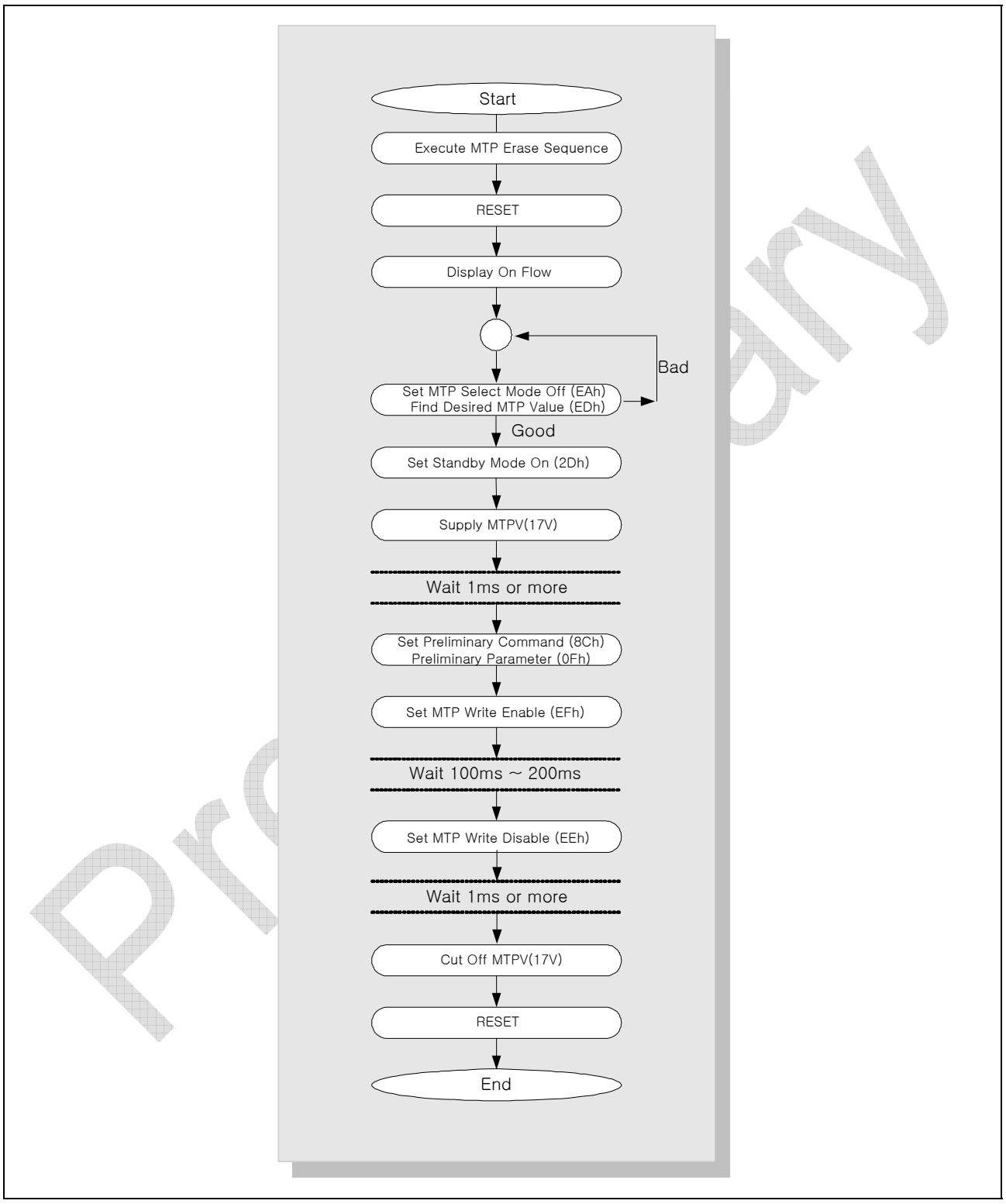


Figure 36. MTP write sequence

4.4.6. Voltages and waveforms for MTP programming

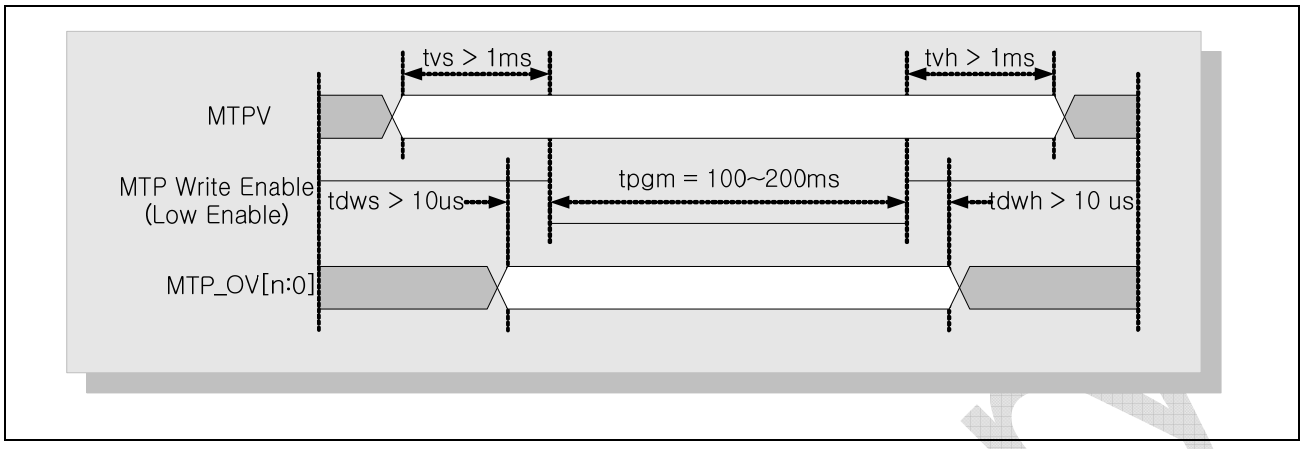


Figure 37. Voltages and waveforms for MTP programming

* Note: MTP_OV is offset volume.

4.4.6.1. Specific timings

Table 30. Specification of MTP programming timings

Timing	Min	Max
Tvs	1ms	-
Tvh	1ms	-
Tdws	10us	-
Tdwh	10us	-
Tpgm	100ms	200ms

4.4.6.2. MTPV Voltage Tolerance

Table 31. Specification of MTP programming voltage

Item	Pgm	Min	Typ	Max	Unit	Remarks
Tolerance of MTPV	Erase		15		V	± 500 mV
	Write		17			

CHAPTER 5

COMMAND

5. COMMAND

5.1. INSTRUCTIONS

Table 32. Instruction Table

Instruction Name	RS	WRB	RDB	DB 15~8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Hex.	Parameter
Non Operation	0	0	1	*	0	0	0	0	0	0	0	0	00	
Oscillation Mode Set	0	0	1	*	0	0	0	0	0	0	1	0	02	1Byte
Driver Output Mode Set	0	0	1	*	0	0	0	1	0	0	0	0	10	1Byte
Monitor Signal Control	0	0	1	*	0	0	0	1	1	0	0	0	18	1Byte
Temperature Compensation Set	0	0	1	*	0	0	1	0	1	0	0	0	28	1Byte
Contrast Control	0	0	1	*	0	0	1	0	1	0	1	0	2A	1Byte
Standby Mode OFF	0	0	1	*	0	0	1	0	1	1	0	0	2C	-
Standby Mode ON	0	0	1	*	0	0	1	0	1	1	0	1	2D	-
Addressing Mode Set	0	0	1	*	0	0	1	1	0	0	0	0	30	1Byte
ROW Vector Mode Set	0	0	1	*	0	0	1	1	0	0	1	0	32	1Byte
N-block Inversion Set	0	0	1	*	0	0	1	1	0	1	0	0	34	1Byte
Driving Mode Set	0	0	1	*	0	0	1	1	0	1	1	0	36	1Byte
Entry Mode Set	0	0	1	*	0	1	0	0	0	0	0	0	40	1Byte
Row address Area Set	0	0	1	*	0	1	0	0	0	0	1	0	42	2Byte
Column address Area Set	0	0	1	*	0	1	0	0	0	0	1	1	43	2Byte
RAM skip Area Set	0	0	1	*	0	1	0	0	0	1	0	1	45	1Byte
Display OFF	0	0	1	*	0	1	0	1	0	0	0	0	50	-
Display ON	0	0	1	*	0	1	0	1	0	0	0	1	51	-
Specified Display Pattern Set	0	0	1	*	0	1	0	1	0	0	1	1	53	1Byte
Partial Display Mode Set	0	0	1	*	0	1	0	1	0	1	0	1	55	1Byte
Partial Display Start Line Set	0	0	1	*	0	1	0	1	0	1	1	0	56	1Byte
Partial Display End Line Set	0	0	1	*	0	1	0	1	0	1	1	1	57	1Byte
Booster Boosting Ratio Set	0	0	1	*	0	1	1	1	0	0	0	0	70	1Byte
Frame Frequency Set	0	0	1	*	0	1	1	1	1	1	1	1	7F	1Byte
Preliminary Instruction	0	0	1	*	1	0	0	0	1	1	0	0	8C	1Byte
CID Read Mode On	0	0	1	*	1	1	0	1	1	0	1	0	DA	-
CID Read Mode Off	0	0	1	*	1	1	0	1	1	0	1	1	DB	-
MTP Load	0	0	1	*	1	1	1	0	0	1	0	1	E5	-
MTP Read Mode	0	0	1	*	1	1	1	0	0	1	1	0	E6	1Byte
MTP Initial Disable	0	0	1	*	1	1	1	0	1	0	0	0	E8	-
MTP Initial Enable	0	0	1	*	1	1	1	0	1	0	0	1	E9	-
MTP Select Mode Off	0	0	1	*	1	1	1	0	1	0	1	0	EA	-
MTP Select Mode On	0	0	1	*	1	1	1	0	1	0	1	1	EB	-
Offset Volume Set	0	0	1	*	1	1	1	0	1	1	0	1	ED	1Byte
MTP Write Disable	0	0	1	*	1	1	1	0	1	1	1	0	EE	-
MTP Write Enable	0	0	1	*	1	1	1	0	1	1	1	1	EF	-
Display Data Write	1	0	1	Display Data Write									-	-
Display Data Read	1	1	0	Display Data Read									-	-
Status Read	0	1	0	0	Status Data Read								-	-

*: Don't care

Parameter: The number of parameter bytes that follows instruction data.

5.2. INSTRUCTION DESCRIPTIONS

5.2.1. Non Operation (00H)

This instruction is non operation.

Table 33. Non operation

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	0	0

5.2.2. Oscillation Mode Set (02H)

Setting of internal function mode

Table 34. Oscillation mode set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1	0
			0	0	0	0	0	0	EXT	0

EXT: External clock selecting

EXT = 0: Internal clock mode (Initial status)

EXT = 1: External clock mode

5.2.3. Driver Output Mode Set (10H)

This instruction sets the display duty and direction.

Table 35. Driver output mode set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	0	0	0	0
			0	0	DLN		MY	MX	SWP	CDIR

DLN: Display Line Number selecting (DLN = 00 initial status)

Table 36. DLN register set

DB5	DB4	Display Duty
0	0	1/132
0	1	1/104
1	0	1/80
1	1	1/96

MY: Selection Row Address Count.

MY = 0 : Row address increment (Initial status)

MY = 1 : Row address decrement

MX: Selection Column Address Count.

MX = 0 : Column address increment (Initial status)

MX = 1 : Column address decrement

SWP: Swap segment output SEGAi and SEGCi This bit is for swapping the output of segment driver.

SWP = 0 (Initial status)

CDIR: Common Direction This bit is for controlling the direction of common driver.

CDIR = 0 (Initial status)

5.2.4. Monitor Signal Control (18H)

This instruction configures the output enable and timing of monitor signal

Table 37. Monitor signal control

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	1	1	0	0	0
			0	0	0	0	0	PM	CL	FR

PM: Enable to transfer field delimiter signal to output pin by active high

PM = 0 (Initial status)

CL: Enable to transfer shift signal to output pin by active high

CL = 0 (Initial status)

FR: Enable to transfer liquid crystal alternating signal to output pin by active high

FR = 0 (Initial status)

5.2.5. Temperature Compensation Set (28H)

This Instruction sets up the driving voltage slope for temperature compensation.

Table 38. Temperature compensation set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	0	0
			0	0	0	0	0	0	TCS	

TCS: Temperature compensation slope set (TCS = 00 initial status)

Table 39. TCS register set

TCS[1:0]	Temp. Coefficient	Note
00	0.00%/°C	(Initial status)
01	-0.05%/°C	
10	-0.10%/°C	
11	-0.15%/°C	

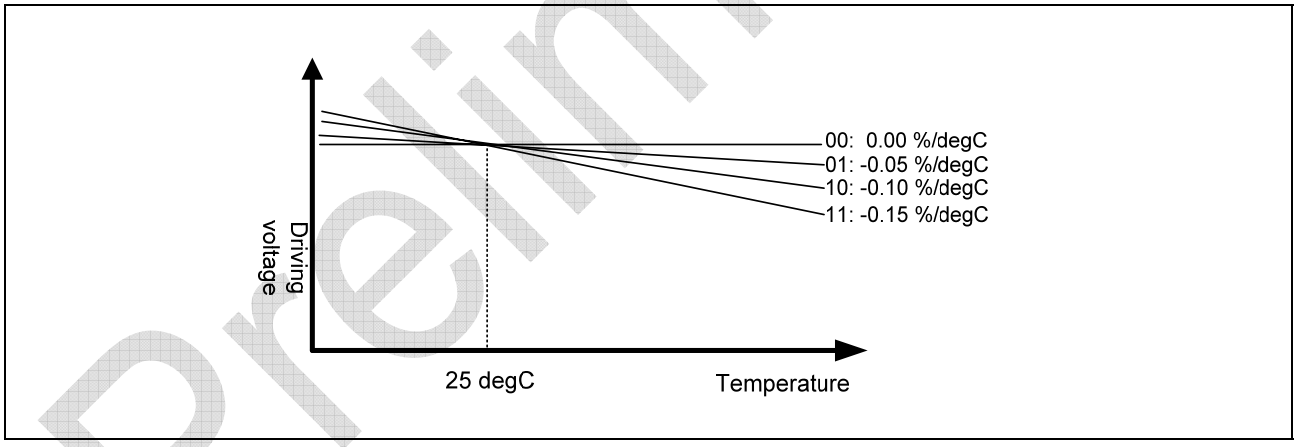


Figure 38. Temperature compensation

5.2.6. Contrast Control (2AH)

This instruction updates the contrast control value in normal display mode and partial display mode.

Table 40. Contrast control

RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	0	1	0
				Contrast control value (0 to 127)						

The relation between V1 voltage (typ.) and Contrast set value (00h initial status)

Table 41. V1 voltage level by contrast setting

Contrast(HEX)	V1 [V]	Contrast(HEX)	V1 [V]	Contrast(HEX)	V1 [V]	Contrast(HEX)	V1 [V]
00h	2.800	20h	3.102	40h	3.405	60h	3.707
01h	2.809	21h	3.112	41h	3.414	61h	3.717
02h	2.819	22h	3.121	42h	3.424	62h	3.726
03h	2.828	23h	3.131	43h	3.433	63h	3.735
04h	2.838	24h	3.140	44h	3.443	64h	3.745
05h	2.847	25h	3.150	45h	3.452	65h	3.754
06h	2.857	26h	3.159	46h	3.461	66h	3.764
07h	2.866	27h	3.169	47h	3.471	67h	3.773
08h	2.876	28h	3.178	48h	3.480	68h	3.783
09h	2.885	29h	3.187	49h	3.490	69h	3.792
0Ah	2.894	2Ah	3.197	4Ah	3.499	6Ah	3.802
0Bh	2.904	2Bh	3.206	4Bh	3.509	6Bh	3.811
0Ch	2.913	2Ch	3.216	4Ch	3.518	6Ch	3.820
0Dh	2.923	2Dh	3.225	4Dh	3.528	6Dh	3.830
0Eh	2.932	2Eh	3.235	4Eh	3.537	6Eh	3.839
0Fh	2.942	2Fh	3.244	4Fh	3.546	6Fh	3.849
10h	2.951	30h	3.254	50h	3.556	70h	3.858
11h	2.961	31h	3.263	51h	3.565	71h	3.868
12h	2.970	32h	3.272	52h	3.575	72h	3.877
13h	2.980	33h	3.282	53h	3.584	73h	3.887
14h	2.989	34h	3.291	54h	3.594	74h	3.896
15h	2.998	35h	3.301	55h	3.603	75h	3.906
16h	3.008	36h	3.310	56h	3.613	76h	3.915
17h	3.017	37h	3.320	57h	3.622	77h	3.924
18h	3.027	38h	3.329	58h	3.631	78h	3.934
19h	3.036	39h	3.339	59h	3.641	79h	3.943
1Ah	3.046	3Ah	3.348	5Ah	3.650	7Ah	3.953
1Bh	3.055	3Bh	3.357	5Bh	3.660	7Bh	3.962
1Ch	3.065	3Ch	3.367	5Ch	3.669	7Ch	3.972
1Dh	3.074	3Dh	3.376	5Dh	3.679	7Dh	3.981
1Eh	3.083	3Eh	3.386	5Eh	3.688	7Eh	3.991
1Fh	3.093	3Fh	3.395	5Fh	3.698	7Fh	4.000

5.2.7. Standby Mode OFF (2CH)

This instruction releases the standby mode.

Table 42. Standby mode off

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	0

The internal statuses during standby off are as following:

All commons output: VRP or –VR or VM

All segments output: VSS or V1

All Analog power is generated automatically. (OSC. , Amp. , Booster(1'st, 2'nd, 3'rd))

Displaying clocks (FR, PM, CL): In operation

Table 43. Function and Pin condition at standby OFF

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	ON (Operate)
COM outputs	VRP or VM or VRN
SEG outputs	V1 or VSS

5.2.8. Standby Mode ON (2DH)

This instruction enters the standby mode to reduce the power consumption to the static power consumption value (Initial status). The following instructions, standby off and display on, cause returning to the normal operation status.

Table 44. Standby mode on

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	1	1	0	1

The internal statuses during standby on are as following:

All common and segment output: VSS

All analog power circuit : OFF (OSC. , Amp. , Booster(1'st,2'nd,3'rd))

Displaying clocks (FR, PM, CL) are held.

Table 45. Function and Pin condition at standby ON

Function/Pin	Condition
DC/DC booster(1'st,2'nd,3'rd)	OFF
COM outputs	VSS
SEG outputs	Floating (discharged)

Table 46. LCD driving power output condition at Standby ON.

level	Condition
VRP	VIN1
V1	VSS
VM	VSS
VRN	VSS

5.2.9. Addressing Mode Set (30H)

Table 47. Addressing mode set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	0	0
			0	0	GSM	DSG	SGF	SGP		SGM

GSM: Gray Scale Mode

- 0: 65,536 color mode(Initial status)
- 1: 4,096 color mode (refer to “Display data Write/Read”)

DSG: Duty Adjust Setting

- 0: Dummy subgroup is one subgroup (Initial status)
- 1: Dummy subgroup is none

SGF: Sub Group Frame Inversion mode setting

- 0: SG Frame inversion OFF (Initial status)
- 1: SG Frame inversion ON

SGM: Sub Group inversion mode setting

- 0: SG inversion OFF (Initial status)
- 1: SG inversion ON

SGP: Sub Group Phase mode setting

- 00: Same phase in all pixels (Initial status)
- 01: Different phase by 1pixel-unit
- 10: Different phase by 2pixel-unit
- 11: Different phase by 4pixel-unit

5.2.10. Row Vector Mode Set (32H)

Setting ROW function

Table 48. Row vector mode set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	0	1	0
			0	0	0	0	INC			VEC

INC: Row Vector Increment Mode. This Parameter set up Row vector increment period

(INC = 000 initial status)

Table 49. VEC register set

DB3	DB2	DB1	Row Vector Increment Period
0	0	0	Every subgroup
0	0	1	Every 2subgroup
0	1	0	Every 4subgroup
0	1	1	Every 8subgroup
1	0	0	Every 16subgroup
1	0	1	Every 16subgroup
1	1	0	Every 16subgroup
1	1	1	Every subframe

VEC: ROW Vector Sequence Mode

- 0: R1->R2->R3->R4 -> R1….. (initial status)
- 1: R1->R3->R2->R4 -> R1…..

5.2.11. N-block Inversion Set (34H)

This instruction set up N block inversion for AC driving.

Table 50. N-block inversion set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	0	0
			FIM	FIP	0	N-block inversion				

FIM: Forcing Inversion Mode

FIM = 0: Forcing Inversion OFF (Initial status)

FIM = 1: Forcing Inversion ON

FIP: Forcing Inversion Period

FIP = 0: Forcing Inversion Period is one frame (Initial status)

FIP = 1: Forcing Inversion Period is two frames

N-block Inversion: This parameter indicates the basic period of polarity inversion.

The whole period of polarity inversion is decided by FIM, FIP and this parameter.

(N-block Inversion = 00h initial status)

Table 51. Polarity inversion set

DB7	DB6	DB5	DB4 – DB0	Polarity Inversion Period
x	X	x	0	Every frame
0	X	x	1	Every 1 block
:	:	:	:	:
0	X	x	31	Every 31 blocks
1	0	x	1	Every 1 block and every frame
:	:	:	:	:
1	0	x	31	Every 31 blocks and every frame
1	1	x	1	Every 1 block and every 2 frames
:	:	:	:	:
1	1	x	31	Every 31 blocks and every 2 frames

5.2.12. Driving Mode Set (36H)

This instruction controls the internal driving mode.

Table 52. Driving mode set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	0	1	1	0
			0	0	0	0	0	0	0	LFS

LFS: Low frame frequency set for low power consumption.

LFS = 0 : Low frequency set OFF (Initial status)

LFS = 1 : Low frequency set ON

note. fFR @(LFS=1) = fFR @(LFS=0) / 2

5.2.13. Entry Mode Set (40H)

Setting internal function mode.

Table 53. Entry mode set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	0	0
			16B	0	0	0	0	MDI	Y/X	RMW

16B: Selection data bus width.

16B = 0: 16bit data bus (Initial status)

16B = 1: 8bit data bus

MDI: Memory data inversion setting for low power consumption.

MDI = 0: Memory data inversion OFF (Initial status)

MDI = 1: Memory data inversion ON

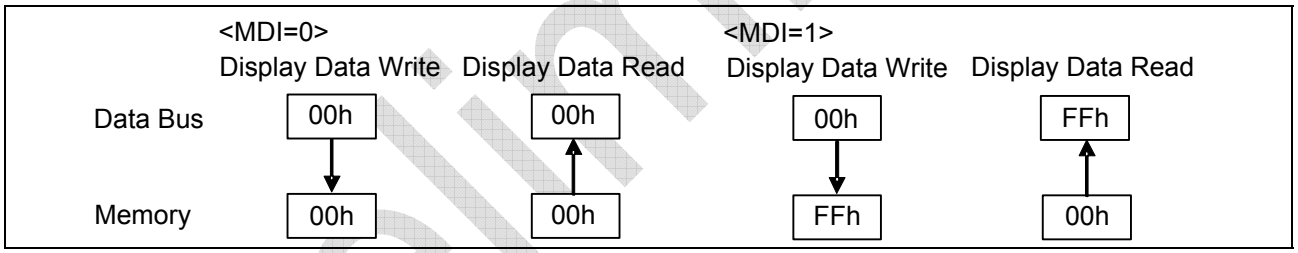


Figure 39. MDI function

Y/X: Selection Address Count.

Y/X = 0 : Column address count first (Initial status)

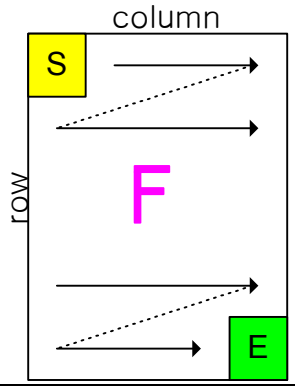
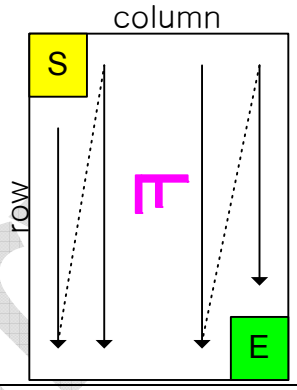
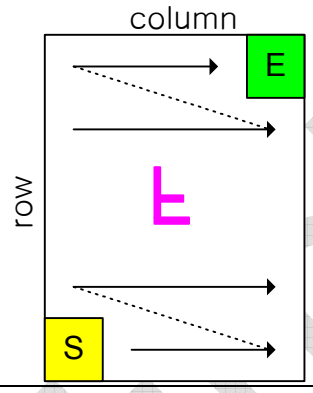
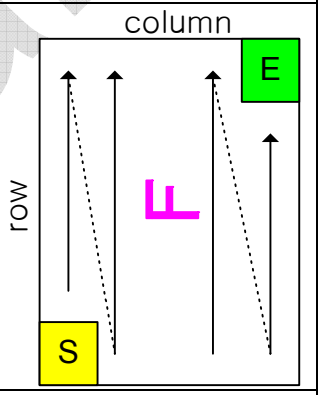
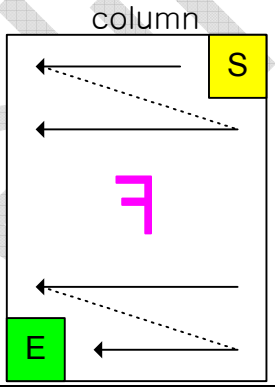
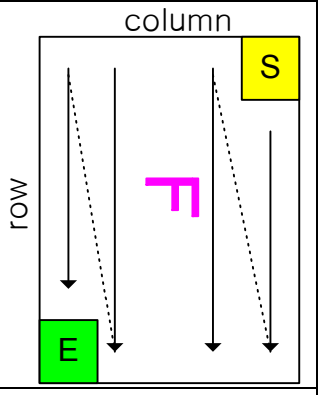
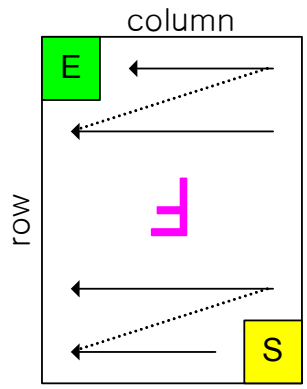
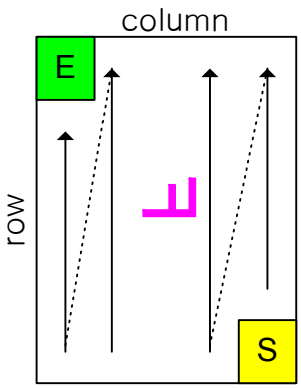
Y/X = 1 : Row address count first

RMW: Read modify write mode ON/OFF select

RMW = 0 : Read modify write OFF (Initial status)

RMW = 1: Read modify write ON. When this mode is on, X(Y) address of on-chip display RAM is not increment in reading display data but in writing display data.

Table 54. Entry Mode Set Table

Display Data Direction	Entry Mode Set			Stored data into DDRAM	Display Data Direction	Entry Mode Set			Stored data into DDRAM
	Y/X	MX	MY			Y/X	MX	MY	
Normal	0	0	0		X-Y Exchange	1	0	0	
Y-Mirror	0	0	1		X-Y Exchange Y-Mirror	1	0	1	
X-Mirror	0	1	0		X-Y Exchange X-Mirror	1	1	0	
X-Mirror Y-Mirror	0	1	1		X-Y Exchange X-Mirror Y-Mirror	1	1	1	

5.2.14. Row Address Area Set (42H)

This instruction and parameter set up the Y address areas of the on-chip display data RAM.

Table 55. Row address area set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	0
			Y start address set (Initial Status = 00H)							
			Y end address set (Initial Status = 83H)							

The current Y address of the on-chip display data RAM is the Y start address by setting this instruction. In Y address count mode (Y/X = “H”), the Y address is increased from Y start address to Y end address. When Y address is equal to the Y end address, the X address is increased by 1 and the Y address returns to Y start address. The Y start and Y end addresses must be set as a pair and Y start address must be less than Y end address.

5.2.15. Column Address Area Set (43H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

Table 56. Column address area set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	1	1
			X start address set (Initial Status = 00H)							
			X end address set (Initial Status = 83H)							

The current X address of the on-chip display data RAM is the X start address by setting this instruction. In X address count mode (Y/X = “L”), the X address is increased from X start address to X end address. When X address is equal to the X end address, the Y address is increased by 1 and the X address returns to X start address. The X start and X end address must be set as a pair and X start address must be less than X end address.

5.2.16. RAM Skip Area Set (45H)

This instruction and parameter set up the X address areas of the on-chip display data RAM.

Table 57. RAM skip area set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	0	1
			0	0	0	0	0	0	RSK	

RSK: RAM Skip function ON/OFF set

RSK = 00: No Skip (initial status)

RSK = 01: X address 34h-4Fh skip (104 RGB)

RSK = 10: X address 3Ch-47h skip (120 RGB)

RSK = 11: X address 30h-53h skip (96RGB)

5.2.16.1. RAM Skip Area Set

RAM Skip Area Set can skip a part of RAM X-address area. After setting RAM skip area, X-address counts skip this area and count. In other words, X address after skip area is changed into X address which added a part for skip area.

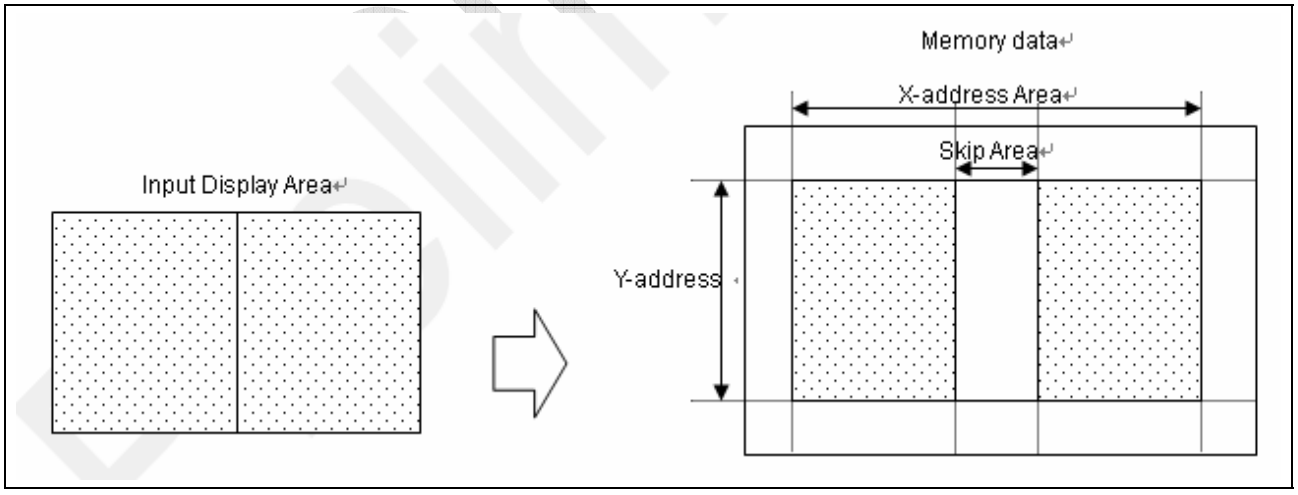


Figure 40. RAM Skip Area

5.2.17. Display OFF (50H)

Turn the display OFF (Initial status).

When display is off, all segment and common output are VSS level.

Table 58. Display off

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	0

Function and Pin condition at Display OFF

Table 59. Booster and Drivers operation in display off

Function/Pin	Condition
DC/DC booster (1'st, 2'nd, 3'rd)	ON (Operate)
SEG and COM outputs	VSS

5.2.18. Display ON (51H)

Turn the display ON.

In case of being standby mode, this instruction does not work. This instruction is executed after Standby mode off

Table 60. Display on

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	1

Function and Pin condition at Display ON

Table 61. Booster and Drivers operation in display on

Function/Pin	Condition
DC/DC booster (1'st, 2'nd, 3'rd)	ON(Operate)
COM outputs	VRP or VM or VRN
SEG outputs	V1 or VSS

5.2.19. Specified Display Pattern Set (53H)

This instruction sets the specified display pattern.

Table 62. Sepecified display pattern set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	1	1
			0	0	0	0	0	0	SDP	

SDP: Specified Display Pattern set

SDP = 00: Normal display (Initial status)

SDP = 01: Reverse display: Display data reversing mode setting without the contents of the display RAM

SDP = 10: Whole display pattern becomes OFF regardless of the RAM data.

SDP = 11: Whole display pattern becomes ON regardless of the RAM data.

5.2.20. Partial Display Mode Set (55H)

Table 63. Partial display mode set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	0	1
			0	0	0	0	0	0	0	PT

PT: Partial Display ON/OFF

PT = 0: Partial display OFF = Normal mode (Initial status)

PT = 1: Partial display ON

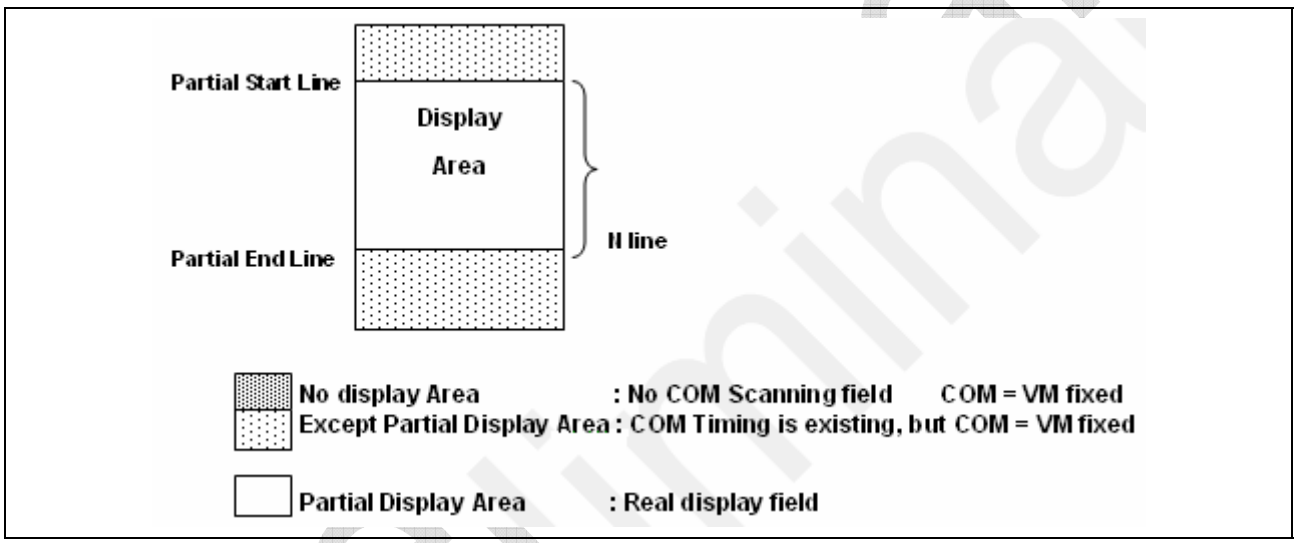


Figure 41. Partial display mode

5.2.20.1. Operation in Partial Display Mode

On scanning except partial display area

- SEG output select V0 or V1 level depend on “FR” value.
- All of COM output is fixed VM level.

On scanning partial display area

- It is equal to be in normal mode

5.2.21. Partial Display Start Line Set (56H), Partial Display End Line Set (57H)

These 2 instructions set the partial display area and it is possible to display a part as 3-lines unit.

5.2.21.1. Partial Display Start Line Set (56H)

Table 64. Partial display start line set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	0
			Partial start line							

EX) Partial start line : 0, 3, 6, 9, …, 126, 129 (3 Lines step)

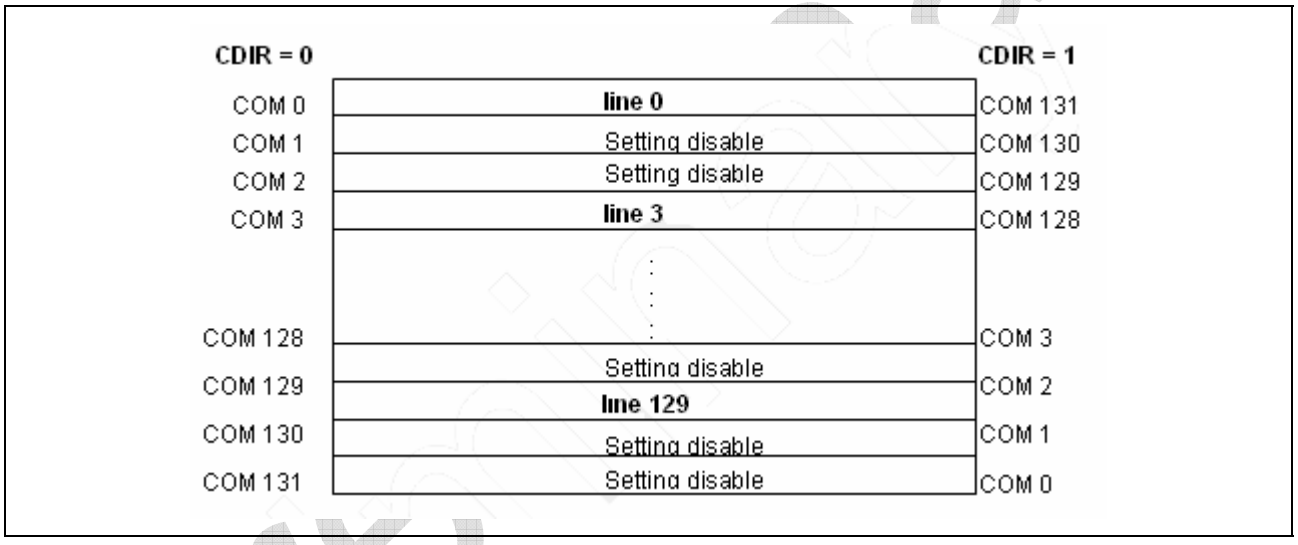


Figure 42. Partial Display Start Line Set

5.2.21.2. Partial Display End Line Set (57H)

Table 65. Partial Display End Line Set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1	1
			Partial end line							

EX) Partial end line : 2, 5, 8, 11, …, 128, 131 (3 Lines step)

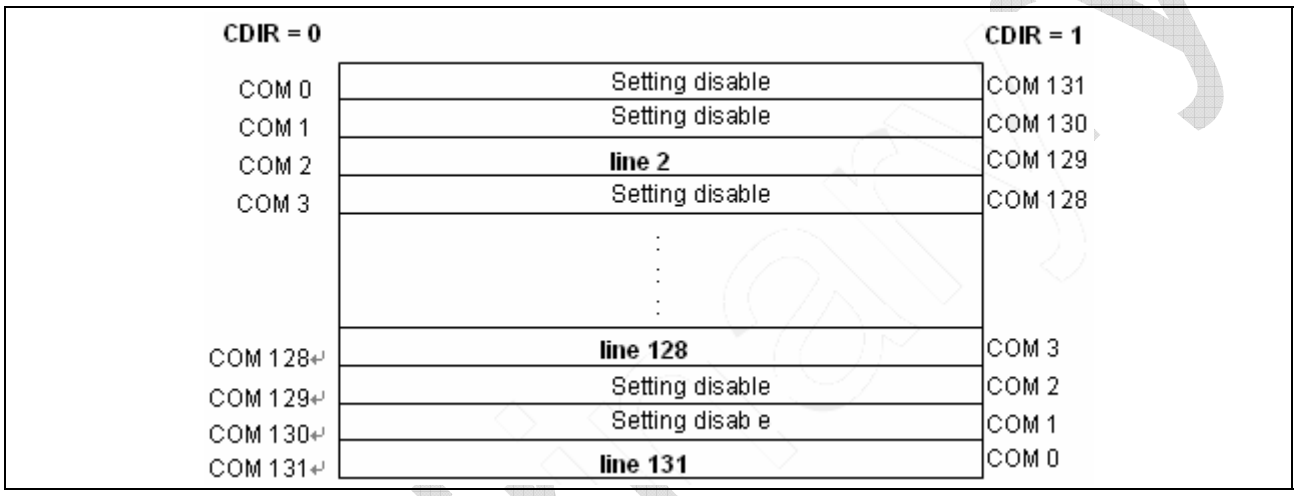


Figure 43. Partial Display End Line Set

Parameter set appoints display line number. Parameter size is able to be set as 3-line unit. Partial end line must set bigger number than Partial start line

5.2.22. Display Data Write/Read

Table 66. Display Data Write/Read

RS	WRB	RDB	DB15 ~ DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	Display RAM write in data								
1	1	0	Display RAM read out data								

5.2.22.1. GSM = 0 (65,536 Color Mode)

Table 67. 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
2'nd cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Table 68. 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	R4	R3	R2	R1	R0	G5	G4	G3
2'nd cycle	G2	G1	G0	B4	B3	B2	B1	B0
3'rd cycle	R4	R3	R2	R1	R0	G5	G4	G3
4'th cycle	G2	G1	G0	B4	B3	B2	B1	B0

5.2.22.2. GSM = 1 (4,096 Color Mode)

Table 69. 16bit access mode

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
2'nd cycle	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0

Table 70. 8bit access mode

	7	6	5	4	3	2	1	0
1'st cycle	X	X	X	X	R3	R2	R1	R0
2'nd cycle	G3	G2	G1	G0	B3	B2	B1	B0
3'rd cycle	X	X	X	X	R3	R2	R1	R0
4'th cycle	G3	G2	G1	G0	B3	B2	B1	B0

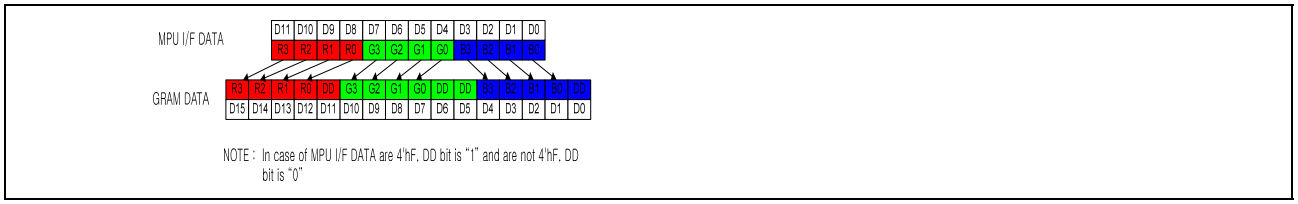


Figure 44. 4,096 Color Mode Data Format

5.2.23. Booster Boosting Set (70H)

This instruction sets the Booster Boosting ratio.

Table 71. Booster Boosting Set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	1	0	0	0
			0	0	NDC[2:0]			DC[2:0]		

NDC[2:0] : Select 3rd Booster Boosting ratio

Table 72. 3rd Booster Boosting Ratio

DB5	DB4	DB3	Boosting ratio (M_3)	Remark
0	0	0	X-3	
0	0	1	X-3	
0	1	0	X-4	
0	1	1	X-4	default
1	0	0	X-4	
1	0	1	X-4	
1	1	0	X-4	
1	1	1	X-4	

DC[2:0] : Select 2rd Booster Boosting ratio

Table 73. 2nd Booster Boosting Ratio

DB2	DB1	DB0	Boosting ratio (M_2)	Remark
0	0	0	X 3	
0	0	1	X 3	
0	1	0	X 4	
0	1	1	X 4	
1	0	0	X 5	default
1	0	1	X 5	
1	1	0	X 5	
1	1	1	X 5	

The 2nd, 3rd Booster efficiency is changed according to M2 and M3. (See DC CHARACTERISTICS(1))

5.2.24. Frame Frequency Set (7FH)

This instruction sets the Frame Frequency.

Table 74. Frame Frequency Set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	1	1	1	1
			0	Frame Frequency (Initial Status = 2H)			0	0	0	0

Table 75. Frame Frequency Control

DB[6]	DB[5]	DB[4]	Frame Frequency[Hz]	Remark
0	0	0	Don't Use	
0	0	1	Don't Use	
0	1	0	198	
0	1	1	148	
1	0	0	119	Default
1	0	1	99	
1	1	0	85	
1	1	1	74	

5.2.25. Status Read

MTP_RD = 0 : Normal Status Read (Initial status)

Table 76. Status Read (MTP_RD=0, ST_RD_MODE=0)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	BUSY	Y/X	MPRT	0	PT	STB	REV	DP

This instruction indicates the internal status of the S6B3306.

DP : (0 : Display OFF Status, 1 : Display ON Status)

REV : (0 : Display Image Non-Reversing, 1 : Display Image Reversing)

STB : (0 : Standby Mode OFF Status, 1 : Standby Mode ON Status)

PT : (0 : Partial Display Mode OFF Status, 1 : Partial Display Mode ON Status)

MPRT: (0: MTP cell non-protection status, 1: MTP cell protection status)

Y/X : (0: X-address Count Mode, 1 : Y-address Count Mode)

BUSY: (0: No Busy, 1: Busy)

MTP_RD = 1: MTP Status Read

Table 77. Status Read (MTP_RD=1, ST_RD_MODE=0)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	MPRT	MOV5	MOV4	MOV3	MOV2	MOV1	MOV0

This instruction indicates the MTP cell values of the S6B3306. (Refer to EEPROM CELL STRUCTURE)

ST_RD_MODE = 1: CID Status Read (refer to DAh command)

Table 78. Status Read (MTP_RD=0, ST_RD_MODE=1)

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	0	0	0	CID[1]	CID[0]

CID[1:0]: This instruction indicates the status of CID[1:0] pins

5.2.26. Preliminary Instruction (8CH)

This instruction is used to write / erase MTP cell.

Table 79. Preliminary Instruction

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	1	1	0	0
			0	0	0	0	1	1	1	1

Parameter default (F0h)

5.2.27. CID Read Mode On (DAH)

CID read mode enable (ST_RD_MODE = 1).

Table 80. CID Read Mode On

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	0	1	0

5.2.28. CID Read Mode Off (DBH)

CID read mode disable (ST_RD_MODE = 0, initial status).

Table 81. CID Read Mode Off

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	0	1	1

5.2.29. MTP Load (E5H)

This command is used to load MTP cell.

Table 82. MTP Load

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	0	1

This command is valid at standby ON.

5.2.30. MTP Read Mode (E6H)

This command is used to read MTP cell.

Table 83. MTP Read Mode

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	0	1	1	0
			0	0	0	0	0	0	0	MTP_RD

MTP_RD: MTP Read Mode

- MTP_RD = 0: Normal Status Mode (Initial status)
- MTP_RD = 1: MTP Status Mode

5.2.31. MTP Initial Disable (E8H)

This command is used to turn MTP initial mode off. (Initial status)

Table 84. MTP Initial Disable

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	0	0

5.2.32. MTP Initial Enable (E9H)

This command is used to turn MTP initial mode on.

Table 85. MTP Initial Enable

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	0	1

5.2.33. MTP Select Mode Off (EAH)

This command is used to turn MTP select mode off.

Table 86. MTP Select Mode

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	1	0

5.2.34. MTP Select Mode On (EBH)

This command is used to turn MTP select mode on. (Initial status)

Table 87. MTP Select Mode On

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	0	1	1

5.2.35. Offset Volume Set (EDH)

This command is used to set offset value x (-32 to +31) to electronic volume by 2s complement.

Table 88. Offset Volume Set

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	1	0	1
			0	0	OV5	OV4	OV3	OV2	OV1	OV0

Table 89. Offset Volume Control

OV5	OV4	OV3	OV2	OV1	OV0	Offset Volume
0	1	1	1	1	1	31
:	:	:	:	:	:	
0	0	0	0	0	1	1
0	0	0	0	0	0	0
1	1	1	1	1	1	-1
	:	:	:	:	:	:
1	0	0	0	0	0	-32

5.2.36. MTP Write Disable (EEH)

This command is used to cut off offset value (OV) from EEPROM cells.

Table 90. MTP Write Disable

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	1	1	0

5.2.37. MTP Write Enable (EFH)

This command is used to write offset value (OV) into EEPROM cells.

Table 91. MTP Write Enable

RS	WRB	RDB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	0	1	1	1	1

5.3. INSTRUCTION PARAMETERS

Table 92. Instruction Parameter

Instruction	Hex	Para	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Oscillation Mode Set	02H	1	0	0	0	0	0	0	EXT	0
			Initial value (00h)							
Driver Output Mode Set	10H	1	0	0	DLN		MY	MX	SWP	CDIR
			Initial value (00h)							
Monitor Signal control	18H	1	0	0	0	0	0	PM	CL	FR
			Initial value (00h)							
Temperature Compensation Set	28H	1	0	0	0	0	0	0	TCS	
			Initial value (00h)							
Contrast Control	2AH	1	0	Contrast control value(0 to 127)						
			Initial value (00h)							
Addressing Mode Set	30H	1	0	0	GSM	DSG	SGF	SGP		SGM
			Initial value (00h)							
ROW Vector Mode Set	32H	1	0	0	0	0	INC			VEC
			Initial value (00h)							
N-block Inversion Set	34H	1	FIM	FIP	0	N-block Inversion				
			Initial value (00h)							
Driving Mode Set	36H	1	0	0	0	0	0	0	0	LFS
			Initial value (00h)							
Entry Mode Set	40H	1	16B	0	0	0	0	MDI	Y/X	RMW
			Initial value (00h)							
Row address Area Set	42H	2	Y Start address set							
			Initial value (00h)							
			Y end address set							
			Initial value (83h)							
RAM Skip Area Set	45H	1	0	0	0	0	0	0	RSK	
			Initial value (00h)							
Column Address Area Set	43H	2	X start address set							
			Initial value (00h)							
			X end address set							
			Initial value (83h)							
Specified Display Pattern Set	53H	1	0	0	0	0	0	0	SDP	
			Initial value (00h)							
Partial Display Mode Set	55H	1	0	0	0	0	0	0	0	PT
			Initial value (00h)							
Partial Display Start Line Set	56H	1	Partial start line							
			Initial value (00h)							
Partial Display End Line Set	57H	1	Partial end line							
			Initial value (00h)							
Booster Boosting Set	70H	1	0	0	NDC[2:0]			DC[2:0]		
			Initial value (1Ch)							
Frame Frequency Set	7FH	1	0	Frame Frequency			0	0	0	0
			Initial value (40h)							
MTP Read Mode	E6H	1	0	0	0	0	0	0	0	MTP_RD
			Initial value (00h)							
Offset Volume Set	EDH	1	0	0	OV5	OV4	OV3	OV2	OV1	OV0
			Initial value (00h)							

Parameter: The number of parameter bytes that follows instruction data.

5.4. RESET OPERATION

When RSTB becomes “L”, following procedure is occurred.

- X start address: 0, X end address: 131
- Y start address: 0, Y end address: 131
- Display OFF
- Read Modify Write Mode OFF
- Function Mode Set
  - EXT = 0: Internal Oscillator Mode
  - LFS = 0: Normal Frequency Mode
  - 16B = 0: Data Bus Width 8bit Mode
  - MDI = 0: Memory Data Inversion OFF
  - MX = 0: Column Address increment
  - MY = 0: Row Address increment
  - Y/X = 0: X-address Count Mode
  - Standby Mode ON
- Duty Set
  - Display Duty : DLN = 00 (132 duty)
- N-block inversion
  - FIM =0: Forcing Inversion OFF
  - N-block inversion = 00H: frame inversion
- Partial Display Mode
  - PT = 0: Partial Display Mode OFF
- Partial Display Area Set
  - Partial start line = 00H
  - Partial end line = 00H
- Addressing Mode Set
  - DSG = 0: Mode 0
  - SGF = 0: SG Frame Inversion OFF
  - SGP = 00: Same phase in all pixels
- Row Vector Mode Set
  - INC =000: Increment every subgroup
  - VEC=0: R1->R2->R3->R4->R1->…
- CID Read Mode Off

CHAPTER 6

APPENDIX

6. APPENDIX

6.1. DISPLAY APPLICATIONS

By combination of DLN, CDIR, RSK bits setting, LCD panel and S6B3306 can be connected in many ways.

6.1.1. 132 Duty Display (ZIGZAG_MODE=0)

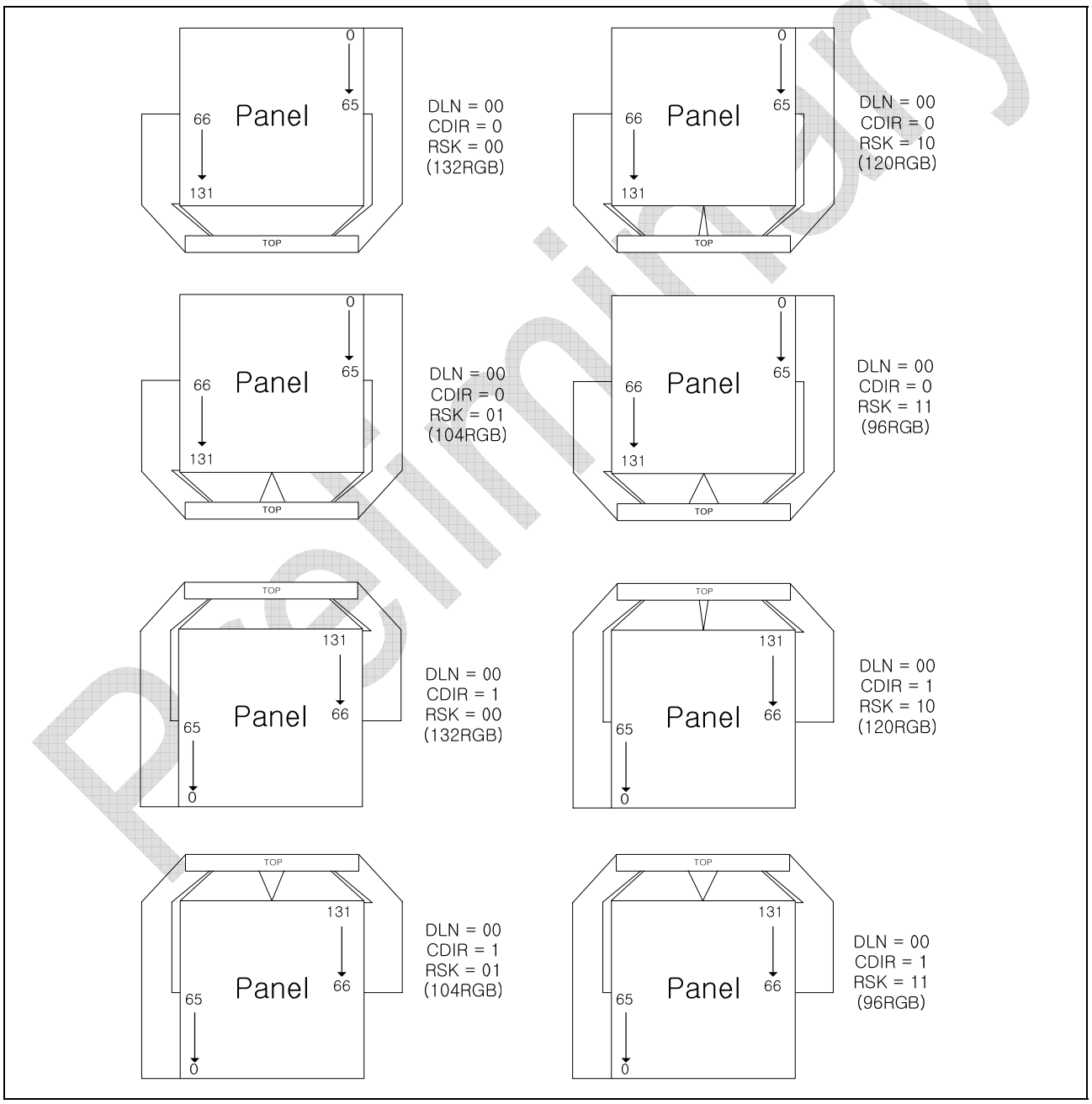


Figure 45. Display application (132 Duty, ZIGZAG_MODE=0)

6.1.2. 104 Duty Display (ZIGZAG_MODE=0)

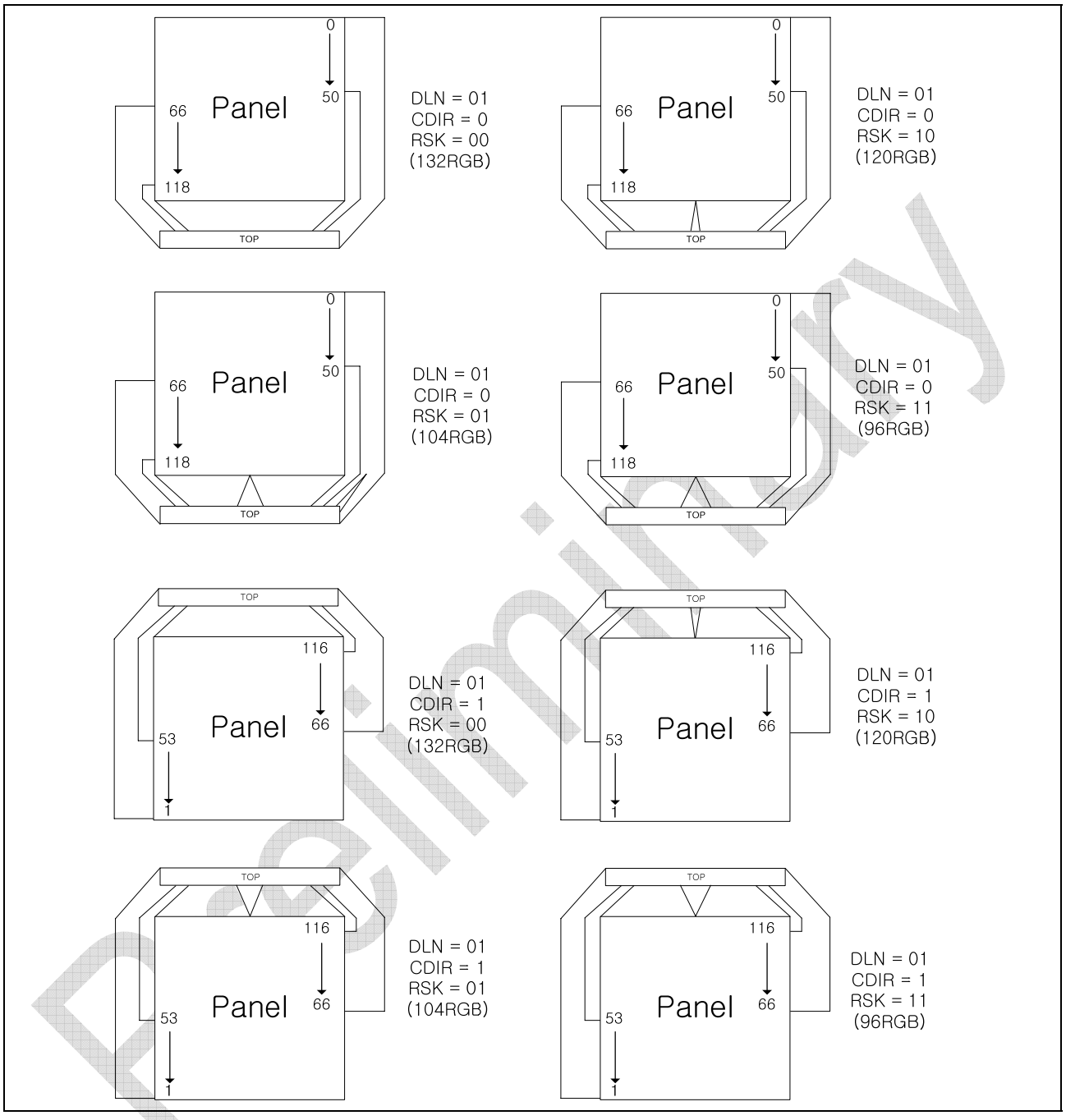


Figure 46. Display application (104 Duty, ZIGZAG_MODE=0)

6.1.3. 96 Duty Display (ZIGZAG_MODE=0)

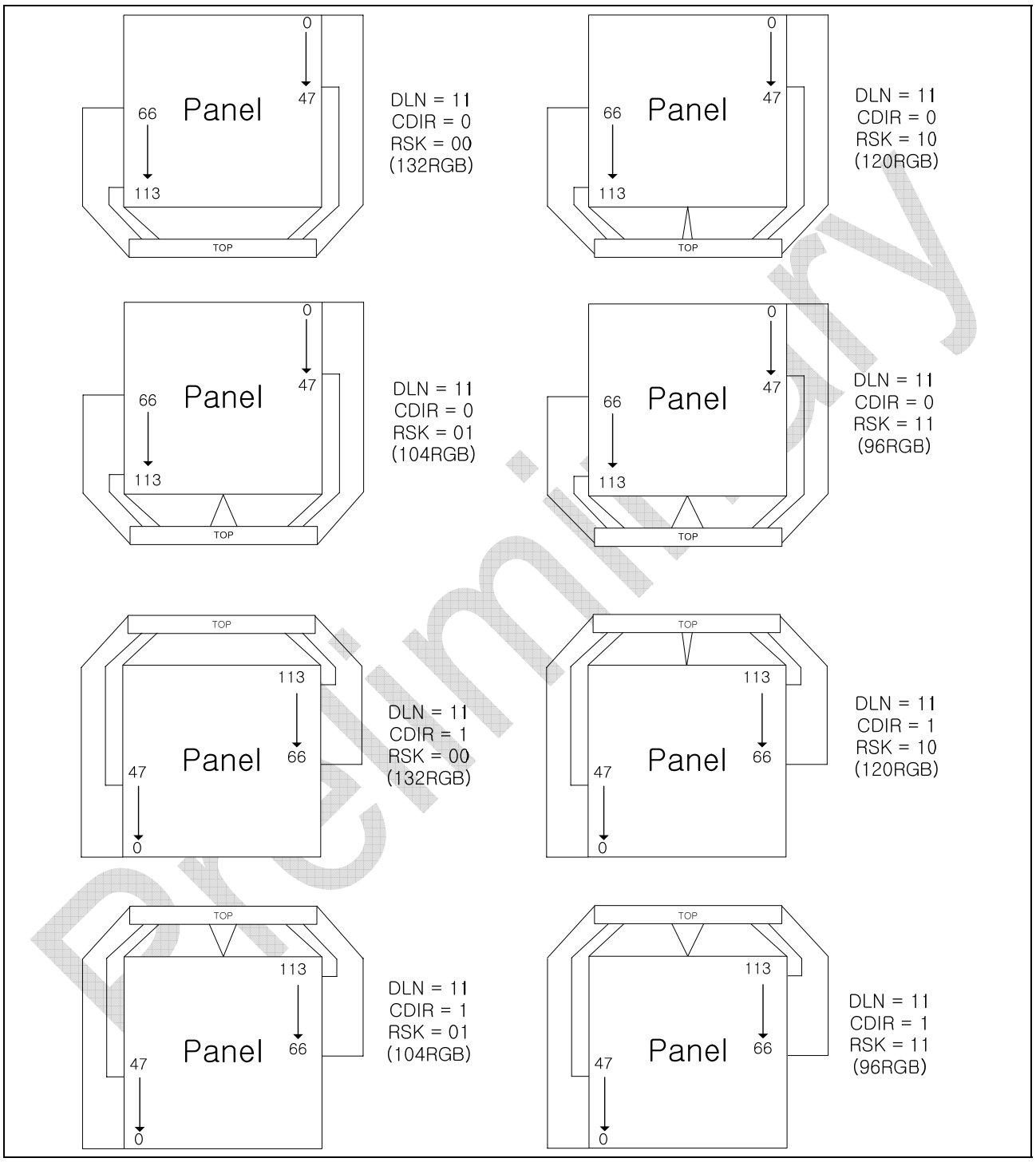


Figure 47. Display application (96 Duty, ZIGZAG_MODE=0)

6.1.4. 80 Duty Display (ZIGZAG_MODE=0)

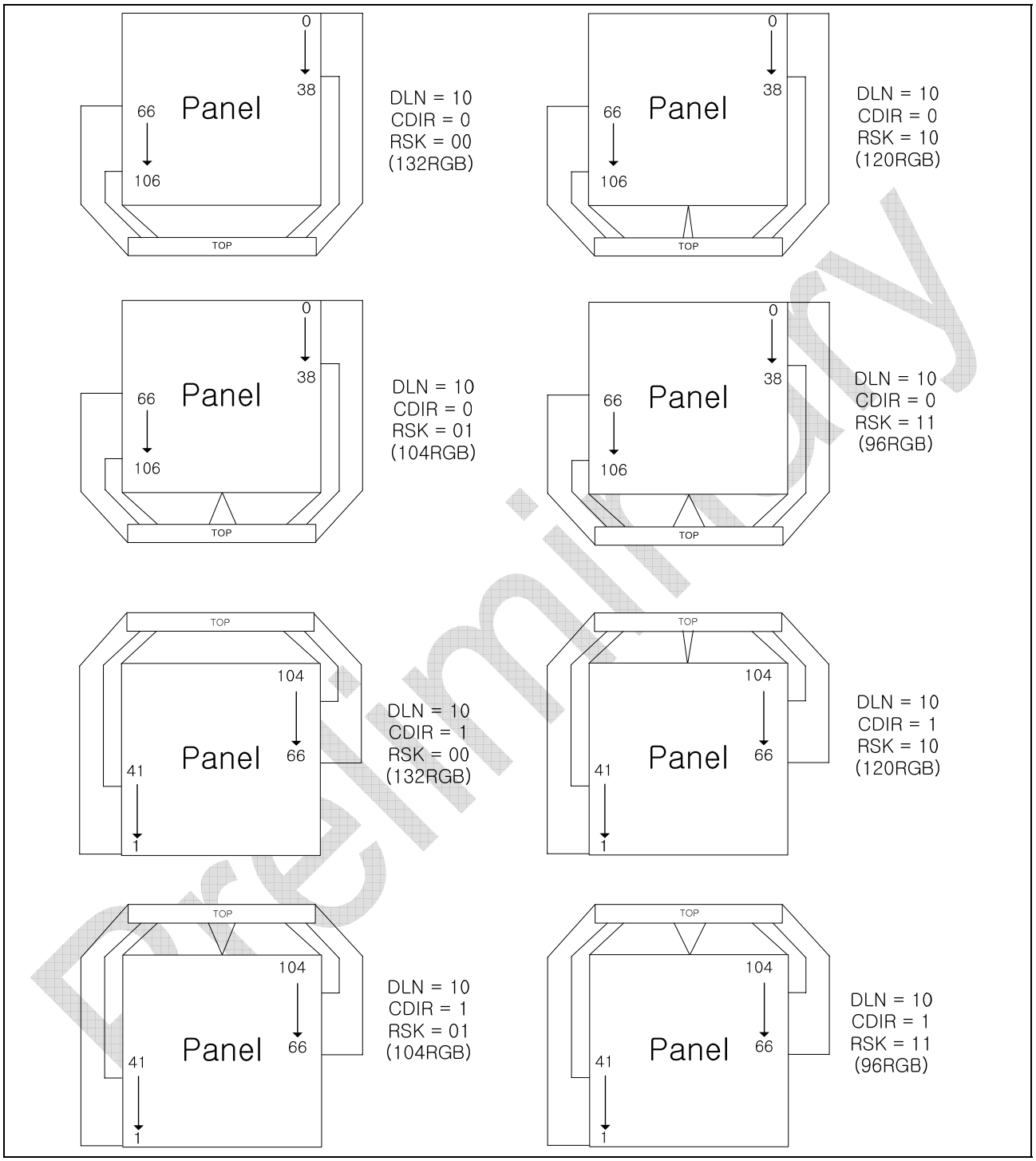


Figure 48. Display application (80 Duty, ZIGZAG_MODE=0)

6.2. APPLICATION CIRCUIT

6.2.1. Internal Power Mode

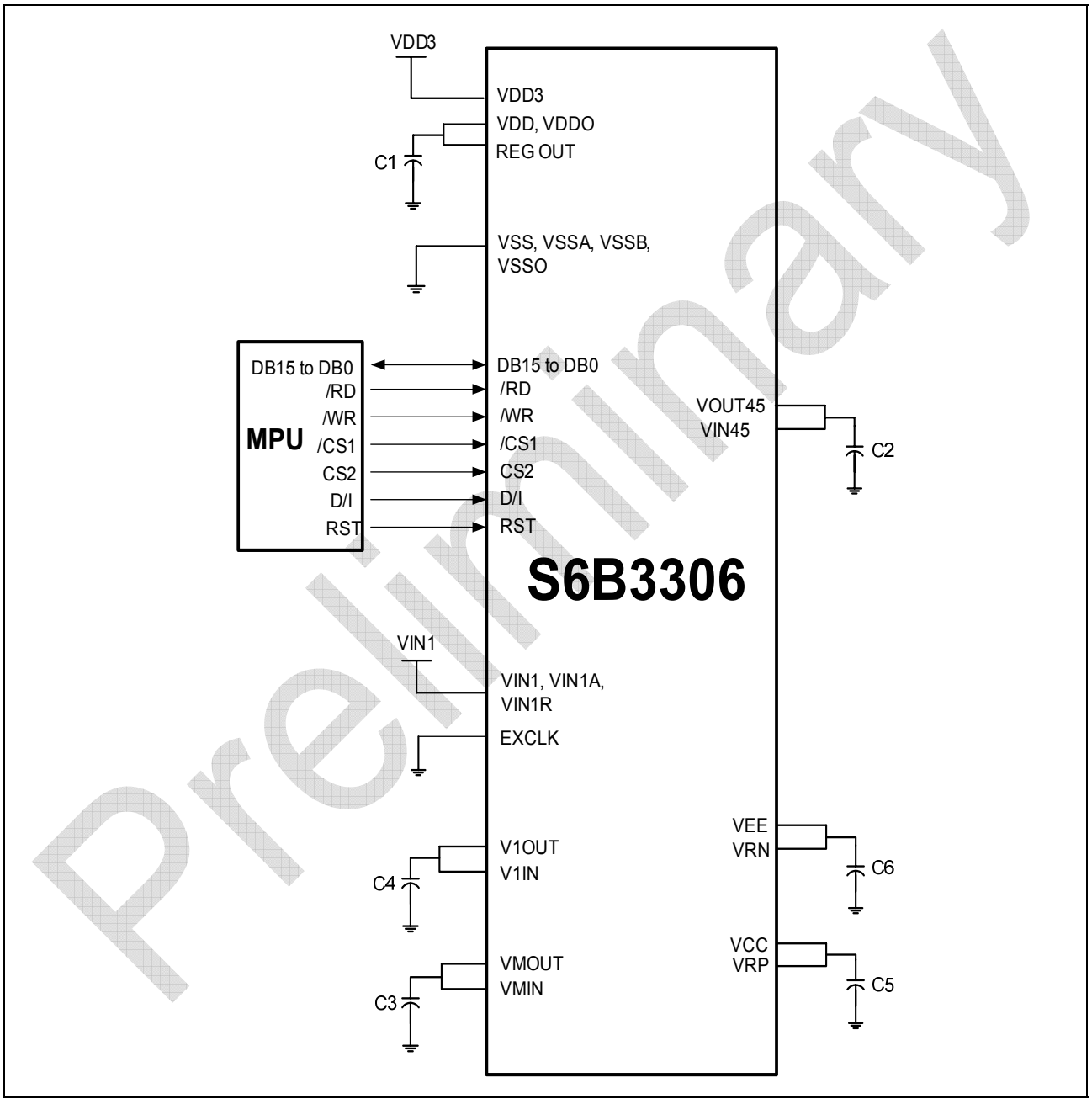


Figure 49. Application Circuit (80 Series MPU, Internal Power Mode)

6.2.2. External Power Mode

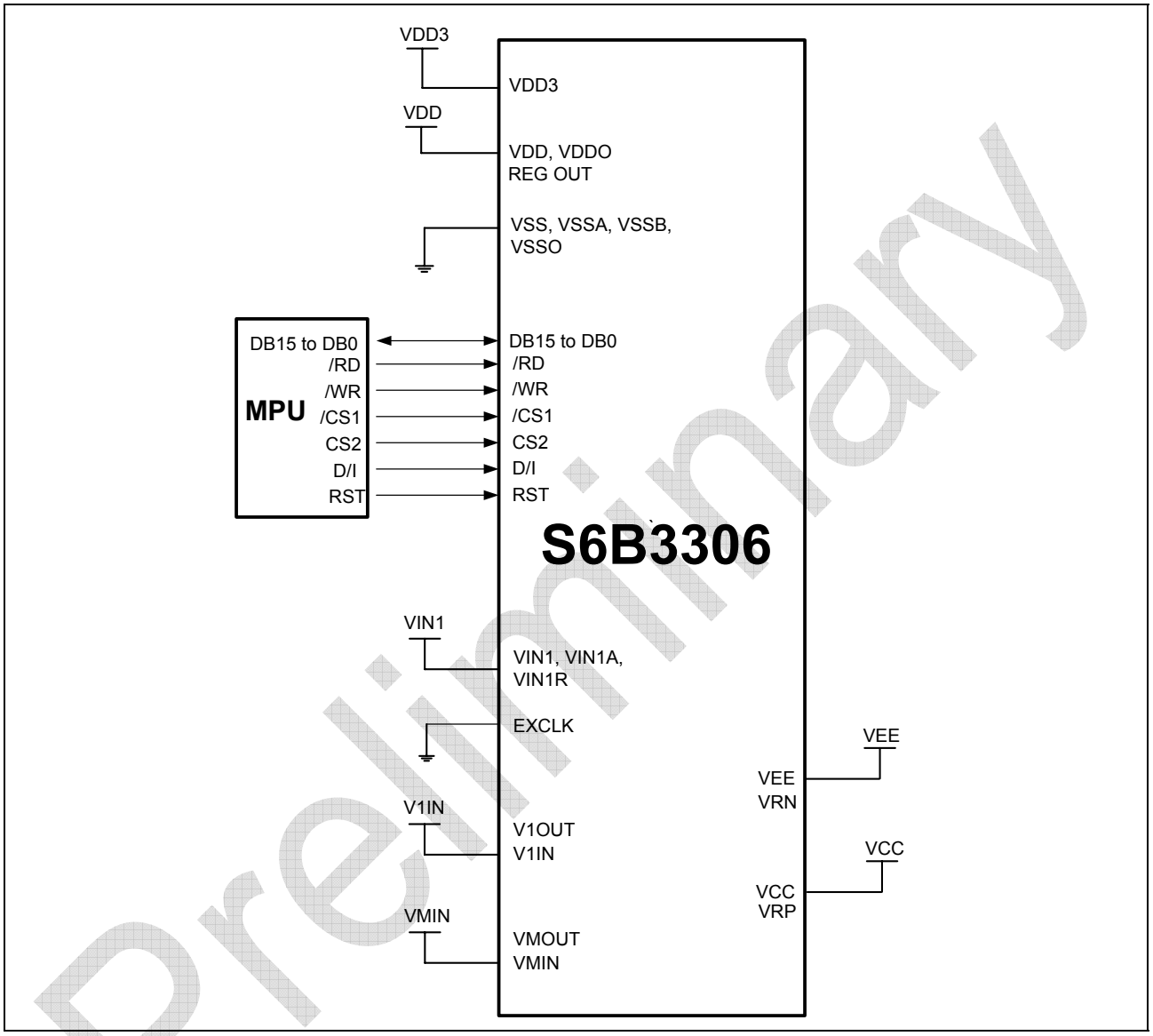


Figure 50. Application Circuit (80 Series MPU, External Power Mode)

6.3. PAD CENTER COORDINATES

Table 93. Pad Center Coordinates(–X11)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	DUMMY<1>	-5157.5	-260	51	CID<1>	-2082.5	-260	101	VIN1R	1317.5	-260
2	DUMMY<2>	-5097.5	-260	52	CID<0>	-2022.5	-260	102	VIN1R	1377.5	-260
3	MTPV	-5037.5	-260	53	DB<0>	-1962.5	-260	103	VIN1R	1437.5	-260
4	MTPV	-4977.5	-260	54	DB<1>	-1877.5	-260	104	VIN1R	1497.5	-260
5	V0IN	-4917.5	-260	55	DB<2>	-1792.5	-260	105	VIN1A	1557.5	-260
6	V0IN	-4857.5	-260	56	DB<3>	-1707.5	-260	106	VIN1A	1617.5	-260
7	RTEST	-4797.5	-260	57	DB<4>	-1622.5	-260	107	VIN1A	1677.5	-260
8	VSS3	-4737.5	-260	58	DB<5>	-1537.5	-260	108	VIN1A	1737.5	-260
9	REGOUT	-4677.5	-260	59	DB<6>	-1452.5	-260	109	VIN1	1797.5	-260
10	REGOUT	-4617.5	-260	60	DB<7>	-1367.5	-260	110	VIN1	1857.5	-260
11	VDDO	-4557.5	-260	61	DB<8>	-1282.5	-260	111	VIN1	1917.5	-260
12	VDDO	-4497.5	-260	62	DB<9>	-1197.5	-260	112	VIN1	1977.5	-260
13	VDD	-4437.5	-260	63	DB<10>	-1112.5	-260	113	VIN1	2037.5	-260
14	VDD	-4377.5	-260	64	DB<11>	-1027.5	-260	114	VIN1	2097.5	-260
15	VDD	-4317.5	-260	65	DB<12>	-942.5	-260	115	VIN1	2157.5	-260
16	VDD	-4257.5	-260	66	DB<13>	-857.5	-260	116	VIN1	2217.5	-260
17	VDD3	-4197.5	-260	67	DB<14>	-772.5	-260	117	VIN1	2277.5	-260
18	VDD3	-4137.5	-260	68	DB<15>	-687.5	-260	118	VIN1	2337.5	-260
19	VDD3	-4077.5	-260	69	VSS3	-602.5	-260	119	VIN45	2397.5	-260
20	VDD3	-4017.5	-260	70	PS	-542.5	-260	120	VIN45	2457.5	-260
21	FUSE_EN	-3957.5	-260	71	VDD3	-482.5	-260	121	VIN45	2517.5	-260
22	V1IN	-3897.5	-260	72	MPU	-422.5	-260	122	VOUT45	2577.5	-260
23	V1IN	-3837.5	-260	73	VSS3	-362.5	-260	123	VOUT45	2637.5	-260
24	V1IN	-3777.5	-260	74	CS2	-302.5	-260	124	VOUT45	2697.5	-260
25	V1IN	-3717.5	-260	75	VDD3	-242.5	-260	125	DUMMY<3>	2757.5	-260
26	V1OUT	-3657.5	-260	76	CS1B	-182.5	-260	126	DUMMY<4>	2817.5	-260
27	V1OUT	-3597.5	-260	77	VSSO	-122.5	-260	127	DUMMY<5>	2877.5	-260
28	V1T	-3537.5	-260	78	VSSO	-62.5	-260	128	DUMMY<6>	2937.5	-260
29	VMOUT	-3477.5	-260	79	VSS	-2.5	-260	129	VRN	2997.5	-260
30	VMOUT	-3417.5	-260	80	VSS	57.5	-260	130	VRN	3057.5	-260
31	VMIN	-3357.5	-260	81	VSS	117.5	-260	131	VRN	3117.5	-260
32	VMIN	-3297.5	-260	82	VSS	177.5	-260	132	VEE	3177.5	-260
33	VMIN	-3237.5	-260	83	VSS	237.5	-260	133	VEE	3237.5	-260
34	VMIN	-3177.5	-260	84	VSS	297.5	-260	134	VEE	3297.5	-260
35	MODE<1>	-3117.5	-260	85	VSS	357.5	-260	135	DUMMY<7>	3357.5	-260
36	MODE<0>	-3057.5	-260	86	VSS	417.5	-260	136	VCC	3417.5	-260
37	EXCLK	-2997.5	-260	87	VSSA	477.5	-260	137	VCC	3477.5	-260
38	VDD3	-2937.5	-260	88	VSSA	537.5	-260	138	VCC	3537.5	-260
39	ZIGZAG_MODE	-2877.5	-260	89	VSSA	597.5	-260	139	VRP	3597.5	-260
40	VSS3	-2817.5	-260	90	VSSA	657.5	-260	140	VRP	3657.5	-260
41	CL	-2757.5	-260	91	VSS3	717.5	-260	141	VRP	3717.5	-260
42	PM	-2672.5	-260	92	VSS3	777.5	-260	142	DUMMY<8>	3777.5	-260
43	FR	-2587.5	-260	93	VSSB	837.5	-260	143	DUMMY<9>	3837.5	-260
44	RSTB	-2502.5	-260	94	VSSB	897.5	-260	144	DUMMY<10>	3897.5	-260
45	RS	-2442.5	-260	95	VSSB	957.5	-260	145	DUMMY<11>	3957.5	-260
46	VSS3	-2382.5	-260	96	VSSB	1017.5	-260	146	DUMMY<12>	4017.5	-260
47	WRB	-2322.5	-260	97	VSSB	1077.5	-260	147	DUMMY<13>	4077.5	-260
48	RDB	-2262.5	-260	98	VSSB	1137.5	-260	148	DUMMY<14>	4137.5	-260
49	VDD3	-2202.5	-260	99	VSSB	1197.5	-260	149	DUMMY<15>	4197.5	-260
50	TEST<2>	-2142.5	-260	100	VSSB	1257.5	-260	150	DUMMY<16>	4257.5	-260

Table 94. Pad Center Coordinates (–X11, Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
151	DUMMY<17>	4317.5	-260	201	COM<34>	4670	228	251	SEGA<4>	3670	228
152	DUMMY<18>	4377.5	-260	202	COM<35>	4650	228	252	SEGC<5>	3650	228
153	DUMMY<19>	4437.5	-260	203	COM<36>	4630	228	253	SEGB<5>	3630	228
154	DUMMY<20>	4497.5	-260	204	COM<37>	4610	228	254	SEGA<5>	3610	228
155	DUMMY<21>	4557.5	-260	205	COM<38>	4590	228	255	SEGC<6>	3590	228
156	DUMMY<22>	4617.5	-260	206	COM<39>	4570	228	256	SEGB<6>	3570	228
157	DUMMY<23>	4677.5	-260	207	COM<40>	4550	228	257	SEGA<6>	3550	228
158	DUMMY<24>	4737.5	-260	208	COM<41>	4530	228	258	SEGC<7>	3530	228
159	DUMMY<25>	4797.5	-260	209	COM<42>	4510	228	259	SEGB<7>	3510	228
160	DUMMY<26>	4857.5	-260	210	COM<43>	4490	228	260	SEGA<7>	3490	228
161	DUMMY<27>	4917.5	-260	211	COM<44>	4470	228	261	SEGC<8>	3470	228
162	V0IN	4977.5	-260	212	COM<45>	4450	228	262	SEGB<8>	3450	228
163	V0IN	5037.5	-260	213	COM<46>	4430	228	263	SEGA<8>	3430	228
164	DUMMY<28>	5097.5	-260	214	COM<47>	4410	228	264	SEGC<9>	3410	228
165	DUMMY<29>	5157.5	-260	215	COM<48>	4390	228	265	SEGB<9>	3390	228
166	DUMMY<30>	5370	228	216	COM<49>	4370	228	266	SEGA<9>	3370	228
167	COM<14>	5350	228	217	COM<50>	4350	228	267	SEGC<10>	3350	228
168	COM<13>	5330	228	218	COM<51>	4330	228	268	SEGB<10>	3330	228
169	COM<12>	5310	228	219	COM<52>	4310	228	269	SEGA<10>	3310	228
170	COM<11>	5290	228	220	COM<53>	4290	228	270	SEGC<11>	3290	228
171	COM<10>	5270	228	221	COM<54>	4270	228	271	SEGB<11>	3270	228
172	COM<9>	5250	228	222	COM<55>	4250	228	272	SEGA<11>	3250	228
173	COM<8>	5230	228	223	COM<56>	4230	228	273	SEGC<12>	3230	228
174	COM<7>	5210	228	224	COM<57>	4210	228	274	SEGB<12>	3210	228
175	COM<6>	5190	228	225	COM<58>	4190	228	275	SEGA<12>	3190	228
176	COM<5>	5170	228	226	COM<59>	4170	228	276	SEGC<13>	3170	228
177	COM<4>	5150	228	227	COM<60>	4150	228	277	SEGB<13>	3150	228
178	COM<3>	5130	228	228	COM<61>	4130	228	278	SEGA<13>	3130	228
179	COM<2>	5110	228	229	COM<62>	4110	228	279	SEGC<14>	3110	228
180	COM<1>	5090	228	230	COM<63>	4090	228	280	SEGB<14>	3090	228
181	COM<0>	5070	228	231	COM<64>	4070	228	281	SEGA<14>	3070	228
182	COM<15>	5050	228	232	COM<65>	4050	228	282	SEGC<15>	3050	228
183	COM<16>	5030	228	233	DUMMY<31>	4030	228	283	SEGB<15>	3030	228
184	COM<17>	5010	228	234	DUMMY<32>	4010	228	284	SEGA<15>	3010	228
185	COM<18>	4990	228	235	DUMMY<33>	3990	228	285	SEGC<16>	2990	228
186	COM<19>	4970	228	236	DUMMY<34>	3970	228	286	SEGB<16>	2970	228
187	COM<20>	4950	228	237	SEGC<0>	3950	228	287	SEGA<16>	2950	228
188	COM<21>	4930	228	238	SEGB<0>	3930	228	288	SEGC<17>	2930	228
189	COM<22>	4910	228	239	SEGA<0>	3910	228	289	SEGB<17>	2910	228
190	COM<23>	4890	228	240	SEGC<1>	3890	228	290	SEGA<17>	2890	228
191	COM<24>	4870	228	241	SEGB<1>	3870	228	291	SEGC<18>	2870	228
192	COM<25>	4850	228	242	SEGA<1>	3850	228	292	SEGB<18>	2850	228
193	COM<26>	4830	228	243	SEGC<2>	3830	228	293	SEGA<18>	2830	228
194	COM<27>	4810	228	244	SEGB<2>	3810	228	294	SEGC<19>	2810	228
195	COM<28>	4790	228	245	SEGA<2>	3790	228	295	SEGB<19>	2790	228
196	COM<29>	4770	228	246	SEGC<3>	3770	228	296	SEGA<19>	2770	228
197	COM<30>	4750	228	247	SEGB<3>	3750	228	297	SEGC<20>	2750	228
198	COM<31>	4730	228	248	SEGA<3>	3730	228	298	SEGB<20>	2730	228
199	COM<32>	4710	228	249	SEGC<4>	3710	228	299	SEGA<20>	2710	228
200	COM<33>	4690	228	250	SEGB<4>	3690	228	300	SEGC<21>	2690	228

Table 95. Pad Center Coordinates (–X11, Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
301	SEGB<21>	2670	228	351	SEGC<38>	1670	228	401	SEGA<54>	670	228
302	SEGA<21>	2650	228	352	SEGB<38>	1650	228	402	SEGC<55>	650	228
303	SEGC<22>	2630	228	353	SEGA<38>	1630	228	403	SEGB<55>	630	228
304	SEGB<22>	2610	228	354	SEGC<39>	1610	228	404	SEGA<55>	610	228
305	SEGA<22>	2590	228	355	SEGB<39>	1590	228	405	SEGC<56>	590	228
306	SEGC<23>	2570	228	356	SEGA<39>	1570	228	406	SEGB<56>	570	228
307	SEGB<23>	2550	228	357	SEGC<40>	1550	228	407	SEGA<56>	550	228
308	SEGA<23>	2530	228	358	SEGB<40>	1530	228	408	SEGC<57>	530	228
309	SEGC<24>	2510	228	359	SEGA<40>	1510	228	409	SEGB<57>	510	228
310	SEGB<24>	2490	228	360	SEGC<41>	1490	228	410	SEGA<57>	490	228
311	SEGA<24>	2470	228	361	SEGB<41>	1470	228	411	SEGC<58>	470	228
312	SEGC<25>	2450	228	362	SEGA<41>	1450	228	412	SEGB<58>	450	228
313	SEGB<25>	2430	228	363	SEGC<42>	1430	228	413	SEGA<58>	430	228
314	SEGA<25>	2410	228	364	SEGB<42>	1410	228	414	SEGC<59>	410	228
315	SEGC<26>	2390	228	365	SEGA<42>	1390	228	415	SEGB<59>	390	228
316	SEGB<26>	2370	228	366	SEGC<43>	1370	228	416	SEGA<59>	370	228
317	SEGA<26>	2350	228	367	SEGB<43>	1350	228	417	SEGC<60>	350	228
318	SEGC<27>	2330	228	368	SEGA<43>	1330	228	418	SEGB<60>	330	228
319	SEGB<27>	2310	228	369	SEGC<44>	1310	228	419	SEGA<60>	310	228
320	SEGA<27>	2290	228	370	SEGB<44>	1290	228	420	SEGC<61>	290	228
321	SEGC<28>	2270	228	371	SEGA<44>	1270	228	421	SEGB<61>	270	228
322	SEGB<28>	2250	228	372	SEGC<45>	1250	228	422	SEGA<61>	250	228
323	SEGA<28>	2230	228	373	SEGB<45>	1230	228	423	SEGC<62>	230	228
324	SEGC<29>	2210	228	374	SEGA<45>	1210	228	424	SEGB<62>	210	228
325	SEGB<29>	2190	228	375	SEGC<46>	1190	228	425	SEGA<62>	190	228
326	SEGA<29>	2170	228	376	SEGB<46>	1170	228	426	SEGC<63>	170	228
327	SEGC<30>	2150	228	377	SEGA<46>	1150	228	427	SEGB<63>	150	228
328	SEGB<30>	2130	228	378	SEGC<47>	1130	228	428	SEGA<63>	130	228
329	SEGA<30>	2110	228	379	SEGB<47>	1110	228	429	SEGC<64>	110	228
330	SEGC<31>	2090	228	380	SEGA<47>	1090	228	430	SEGB<64>	90	228
331	SEGB<31>	2070	228	381	SEGC<48>	1070	228	431	SEGA<64>	70	228
332	SEGA<31>	2050	228	382	SEGB<48>	1050	228	432	SEGC<65>	50	228
333	SEGC<32>	2030	228	383	SEGA<48>	1030	228	433	SEGB<65>	30	228
334	SEGB<32>	2010	228	384	SEGC<49>	1010	228	434	SEGA<65>	10	228
335	SEGA<32>	1990	228	385	SEGB<49>	990	228	435	SEGC<66>	-10	228
336	SEGC<33>	1970	228	386	SEGA<49>	970	228	436	SEGB<66>	-30	228
337	SEGB<33>	1950	228	387	SEGC<50>	950	228	437	SEGA<66>	-50	228
338	SEGA<33>	1930	228	388	SEGB<50>	930	228	438	SEGC<67>	-70	228
339	SEGC<34>	1910	228	389	SEGA<50>	910	228	439	SEGB<67>	-90	228
340	SEGB<34>	1890	228	390	SEGC<51>	890	228	440	SEGA<67>	-110	228
341	SEGA<34>	1870	228	391	SEGB<51>	870	228	441	SEGC<68>	-130	228
342	SEGC<35>	1850	228	392	SEGA<51>	850	228	442	SEGB<68>	-150	228
343	SEGB<35>	1830	228	393	SEGC<52>	830	228	443	SEGA<68>	-170	228
344	SEGA<35>	1810	228	394	SEGB<52>	810	228	444	SEGC<69>	-190	228
345	SEGC<36>	1790	228	395	SEGA<52>	790	228	445	SEGB<69>	-210	228
346	SEGB<36>	1770	228	396	SEGC<53>	770	228	446	SEGA<69>	-230	228
347	SEGA<36>	1750	228	397	SEGB<53>	750	228	447	SEGC<70>	-250	228
348	SEGC<37>	1730	228	398	SEGA<53>	730	228	448	SEGB<70>	-270	228
349	SEGB<37>	1710	228	399	SEGC<54>	710	228	449	SEGA<70>	-290	228
350	SEGA<37>	1690	228	400	SEGB<54>	690	228	450	SEGC<71>	-310	228

Table 96. Pad Center Coordinates (–X11, Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
451	SEGB<71>	-330	228	501	SEGC<88>	-1330	228	551	SEGA<104>	-2330	228
452	SEGA<71>	-350	228	502	SEGB<88>	-1350	228	552	SEGC<105>	-2350	228
453	SEGC<72>	-370	228	503	SEGA<88>	-1370	228	553	SEGB<105>	-2370	228
454	SEGB<72>	-390	228	504	SEGC<89>	-1390	228	554	SEGA<105>	-2390	228
455	SEGA<72>	-410	228	505	SEGB<89>	-1410	228	555	SEGC<106>	-2410	228
456	SEGC<73>	-430	228	506	SEGA<89>	-1430	228	556	SEGB<106>	-2430	228
457	SEGB<73>	-450	228	507	SEGC<90>	-1450	228	557	SEGA<106>	-2450	228
458	SEGA<73>	-470	228	508	SEGB<90>	-1470	228	558	SEGC<107>	-2470	228
459	SEGC<74>	-490	228	509	SEGA<90>	-1490	228	559	SEGB<107>	-2490	228
460	SEGB<74>	-510	228	510	SEGC<91>	-1510	228	560	SEGA<107>	-2510	228
461	SEGA<74>	-530	228	511	SEGB<91>	-1530	228	561	SEGC<108>	-2530	228
462	SEGC<75>	-550	228	512	SEGA<91>	-1550	228	562	SEGB<108>	-2550	228
463	SEGB<75>	-570	228	513	SEGC<92>	-1570	228	563	SEGA<108>	-2570	228
464	SEGA<75>	-590	228	514	SEGB<92>	-1590	228	564	SEGC<109>	-2590	228
465	SEGC<76>	-610	228	515	SEGA<92>	-1610	228	565	SEGB<109>	-2610	228
466	SEGB<76>	-630	228	516	SEGC<93>	-1630	228	566	SEGA<109>	-2630	228
467	SEGA<76>	-650	228	517	SEGB<93>	-1650	228	567	SEGC<110>	-2650	228
468	SEGC<77>	-670	228	518	SEGA<93>	-1670	228	568	SEGB<110>	-2670	228
469	SEGB<77>	-690	228	519	SEGC<94>	-1690	228	569	SEGA<110>	-2690	228
470	SEGA<77>	-710	228	520	SEGB<94>	-1710	228	570	SEGC<111>	-2710	228
471	SEGC<78>	-730	228	521	SEGA<94>	-1730	228	571	SEGB<111>	-2730	228
472	SEGB<78>	-750	228	522	SEGC<95>	-1750	228	572	SEGA<111>	-2750	228
473	SEGA<78>	-770	228	523	SEGB<95>	-1770	228	573	SEGC<112>	-2770	228
474	SEGC<79>	-790	228	524	SEGA<95>	-1790	228	574	SEGB<112>	-2790	228
475	SEGB<79>	-810	228	525	SEGC<96>	-1810	228	575	SEGA<112>	-2810	228
476	SEGA<79>	-830	228	526	SEGB<96>	-1830	228	576	SEGC<113>	-2830	228
477	SEGC<80>	-850	228	527	SEGA<96>	-1850	228	577	SEGB<113>	-2850	228
478	SEGB<80>	-870	228	528	SEGC<97>	-1870	228	578	SEGA<113>	-2870	228
479	SEGA<80>	-890	228	529	SEGB<97>	-1890	228	579	SEGC<114>	-2890	228
480	SEGC<81>	-910	228	530	SEGA<97>	-1910	228	580	SEGB<114>	-2910	228
481	SEGB<81>	-930	228	531	SEGC<98>	-1930	228	581	SEGA<114>	-2930	228
482	SEGA<81>	-950	228	532	SEGB<98>	-1950	228	582	SEGC<115>	-2950	228
483	SEGC<82>	-970	228	533	SEGA<98>	-1970	228	583	SEGB<115>	-2970	228
484	SEGB<82>	-990	228	534	SEGC<99>	-1990	228	584	SEGA<115>	-2990	228
485	SEGA<82>	-1010	228	535	SEGB<99>	-2010	228	585	SEGC<116>	-3010	228
486	SEGC<83>	-1030	228	536	SEGA<99>	-2030	228	586	SEGB<116>	-3030	228
487	SEGB<83>	-1050	228	537	SEGC<100>	-2050	228	587	SEGA<116>	-3050	228
488	SEGA<83>	-1070	228	538	SEGB<100>	-2070	228	588	SEGC<117>	-3070	228
489	SEGC<84>	-1090	228	539	SEGA<100>	-2090	228	589	SEGB<117>	-3090	228
490	SEGB<84>	-1110	228	540	SEGC<101>	-2110	228	590	SEGA<117>	-3110	228
491	SEGA<84>	-1130	228	541	SEGB<101>	-2130	228	591	SEGC<118>	-3130	228
492	SEGC<85>	-1150	228	542	SEGA<101>	-2150	228	592	SEGB<118>	-3150	228
493	SEGB<85>	-1170	228	543	SEGC<102>	-2170	228	593	SEGA<118>	-3170	228
494	SEGA<85>	-1190	228	544	SEGB<102>	-2190	228	594	SEGC<119>	-3190	228
495	SEGC<86>	-1210	228	545	SEGA<102>	-2210	228	595	SEGB<119>	-3210	228
496	SEGB<86>	-1230	228	546	SEGC<103>	-2230	228	596	SEGA<119>	-3230	228
497	SEGA<86>	-1250	228	547	SEGB<103>	-2250	228	597	SEGC<120>	-3250	228
498	SEGC<87>	-1270	228	548	SEGA<103>	-2270	228	598	SEGB<120>	-3270	228
499	SEGB<87>	-1290	228	549	SEGC<104>	-2290	228	599	SEGA<120>	-3290	228
500	SEGA<87>	-1310	228	550	SEGB<104>	-2310	228	600	SEGC<121>	-3310	228

Table 97. Pad Center Coordinates (–X11, Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
601	SEGB<121>	-3330	228	651	COM<117>	-4330	228	701	COM<79>	-5330	228
602	SEGA<121>	-3350	228	652	COM<116>	-4350	228	702	COM<80>	-5350	228
603	SEGC<122>	-3370	228	653	COM<115>	-4370	228	703	DUMMY<39>	-5370	228
604	SEGB<122>	-3390	228	654	COM<114>	-4390	228				
605	SEGA<122>	-3410	228	655	COM<113>	-4410	228				
606	SEGC<123>	-3430	228	656	COM<112>	-4430	228				
607	SEGB<123>	-3450	228	657	COM<111>	-4450	228				
608	SEGA<123>	-3470	228	658	COM<110>	-4470	228				
609	SEGC<124>	-3490	228	659	COM<109>	-4490	228				
610	SEGB<124>	-3510	228	660	COM<108>	-4510	228				
611	SEGA<124>	-3530	228	661	COM<107>	-4530	228				
612	SEGC<125>	-3550	228	662	COM<106>	-4550	228				
613	SEGB<125>	-3570	228	663	COM<105>	-4570	228				
614	SEGA<125>	-3590	228	664	COM<104>	-4590	228				
615	SEGC<126>	-3610	228	665	COM<103>	-4610	228				
616	SEGB<126>	-3630	228	666	COM<102>	-4630	228				
617	SEGA<126>	-3650	228	667	COM<101>	-4650	228				
618	SEGC<127>	-3670	228	668	COM<100>	-4670	228				
619	SEGB<127>	-3690	228	669	COM<99>	-4690	228				
620	SEGA<127>	-3710	228	670	COM<98>	-4710	228				
621	SEGC<128>	-3730	228	671	COM<97>	-4730	228				
622	SEGB<128>	-3750	228	672	COM<96>	-4750	228				
623	SEGA<128>	-3770	228	673	COM<95>	-4770	228				
624	SEGC<129>	-3790	228	674	COM<94>	-4790	228				
625	SEGB<129>	-3810	228	675	COM<93>	-4810	228				
626	SEGA<129>	-3830	228	676	COM<92>	-4830	228				
627	SEGC<130>	-3850	228	677	COM<91>	-4850	228				
628	SEGB<130>	-3870	228	678	COM<90>	-4870	228				
629	SEGA<130>	-3890	228	679	COM<89>	-4890	228				
630	SEGC<131>	-3910	228	680	COM<88>	-4910	228				
631	SEGB<131>	-3930	228	681	COM<87>	-4930	228				
632	SEGA<131>	-3950	228	682	COM<86>	-4950	228				
633	DUMMY<35>	-3970	228	683	COM<85>	-4970	228				
634	DUMMY<36>	-3990	228	684	COM<84>	-4990	228				
635	DUMMY<37>	-4010	228	685	COM<83>	-5010	228				
636	DUMMY<38>	-4030	228	686	COM<82>	-5030	228				
637	COM<131>	-4050	228	687	COM<81>	-5050	228				
638	COM<130>	-4070	228	688	COM<66>	-5070	228				
639	COM<129>	-4090	228	689	COM<67>	-5090	228				
640	COM<128>	-4110	228	690	COM<68>	-5110	228				
641	COM<127>	-4130	228	691	COM<69>	-5130	228				
642	COM<126>	-4150	228	692	COM<70>	-5150	228				
643	COM<125>	-4170	228	693	COM<71>	-5170	228				
644	COM<124>	-4190	228	694	COM<72>	-5190	228				
645	COM<123>	-4210	228	695	COM<73>	-5210	228				
646	COM<122>	-4230	228	696	COM<74>	-5230	228				
647	COM<121>	-4250	228	697	COM<75>	-5250	228				
648	COM<120>	-4270	228	698	COM<76>	-5270	228				
649	COM<119>	-4290	228	699	COM<77>	-5290	228				
650	COM<118>	-4310	228	700	COM<78>	-5310	228				

6.4. EXTERNAL COMPONENT

Table 98. External Component

Name	Device	Value	Item	Maximum Rating Voltage of Capacitors
C1	Capacitors	1.0μF to 4.7μF	REG_OUT – GND	3V
C2	Capacitors	1.0μF	VOUT45 – GND-	10V
C3	Capacitors	1.0μF	Vm – GND	3V
C4	Capacitors	1.0μF	V1 – GND	10V
C5	Capacitors	1.0μF	VRP – GND	18V
C6	Capacitors	1.0μF	VRN – GND	18V

6.5. ABOUT THE POWER ON SEQUENCE

The wait time at Power On Sequence is needed for stabilization wait time of outputs which are VRP, VRN, V1, VM. But, if those outputs are stabilized before Display On, the wait time is changeable.

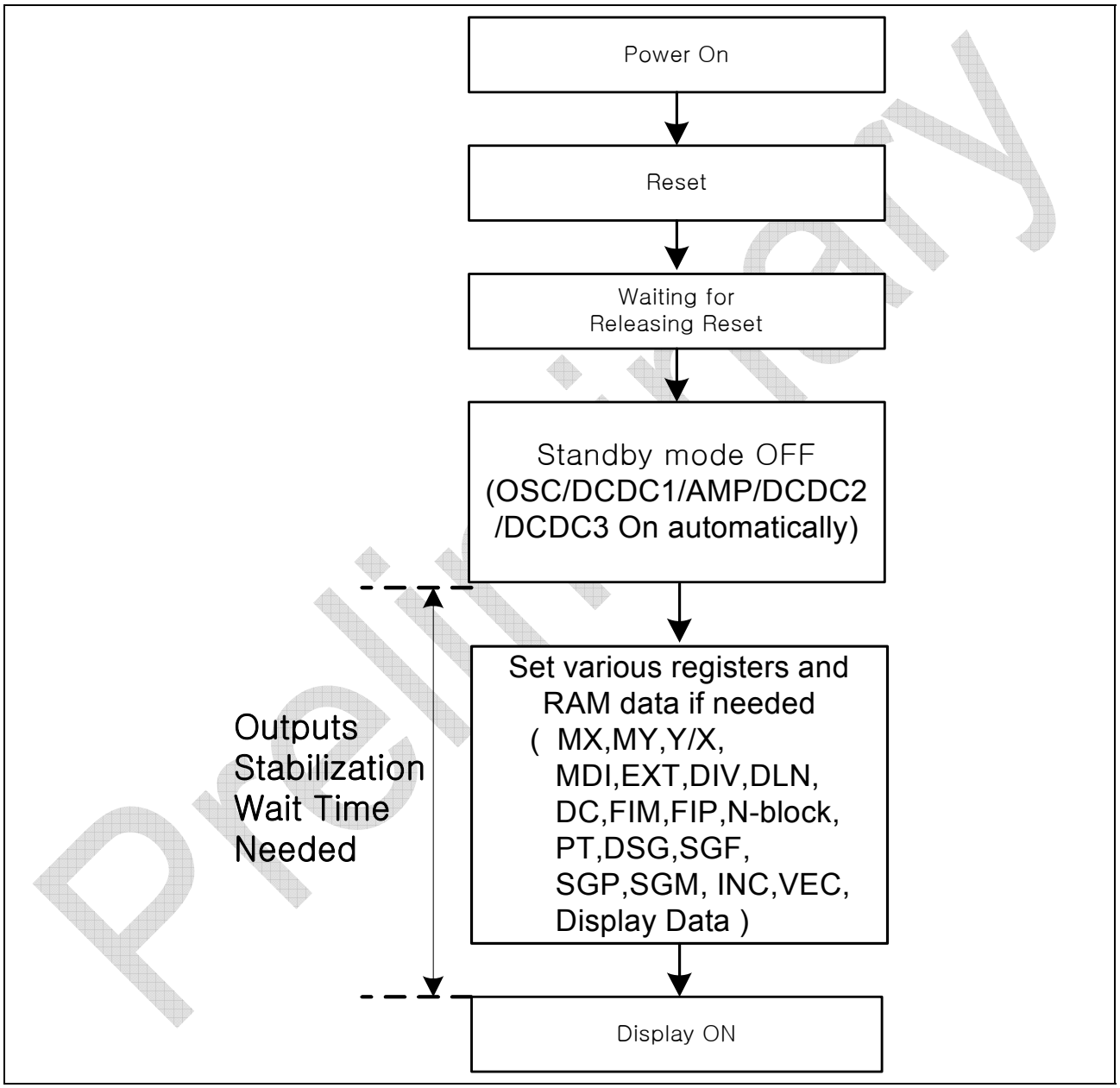


Figure 51. About Power On Sequence

6.6. ABOUT THE WAKE UP SEQUENCE

The wait time at Wake Up Sequence is needed for stabilization wait time of outputs which are VRP, VRN, V1, VM. But, if those outputs are stabilized before Display On, the wait time is changeable.

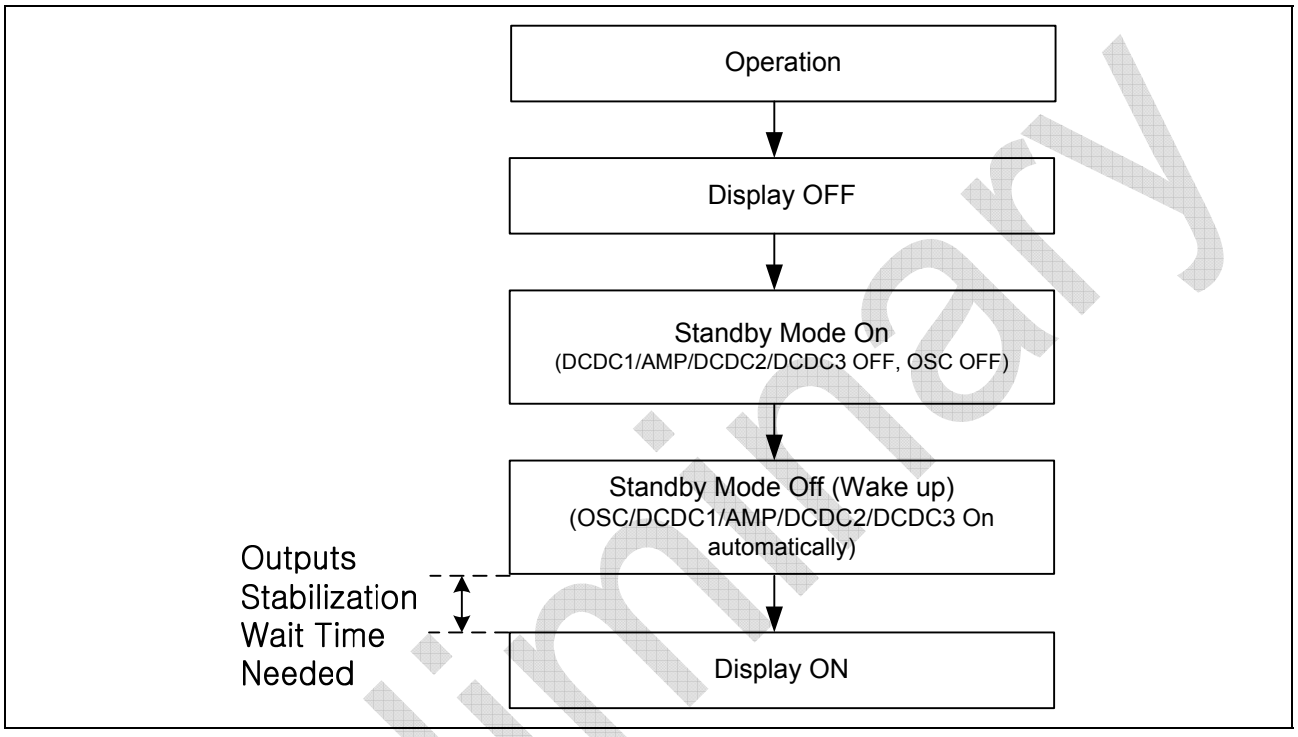


Figure 52. About Wake Up Sequence