EE 3230 Introduction to Integrated Circuit Design Final Project: A 10-bit input and 2-bit output 128*16 bits ROM Macro

Abstract – After 1 semester of learning modern CMOS VLSI design, we have to combine everything we have learned in the class and design a 128*16 bits ROM Macro with access time < 5ns at 5 corners for pre-sim.

Index Terms – access time, ROM

I. INTRODUCTION

In this report, we will explore in detail the design and implementation of the ROM Macro. ROM (Read-Only Memory) is a type of memory in which the data is stored in memory cells, and this data can only be read, not rewritten. In our final project, we have implemented a 128×16-bit ROM Macro using a Contact/Via type ROM. This means that the memory data (1s and 0s) are defined by the presence or absence of contact or via between the BL (bit line) and the source of NMOS transistors.

The ROM Macro consists of the following circuit modules:

1. **Timing Control Module**: This module generates the control signals.
2. **10 D Flip-Flops**: These flip-flops are used to store the input data A[9:0].
3. **7-to-128 X Decoder**: This decoder activates the 128 WL and determines which WL will be turned on.
4. **3-to-8 Y Decoder**: This decoder decides which BL should be read.
5. **Two 8-to-1 MUXs**: These MUXs are used to select the DL (data line).
6. **Two Sense Amplifiers**: read and sense DL.
7. **Two D-latches**: store the output data(SA) until the next clock cycle.

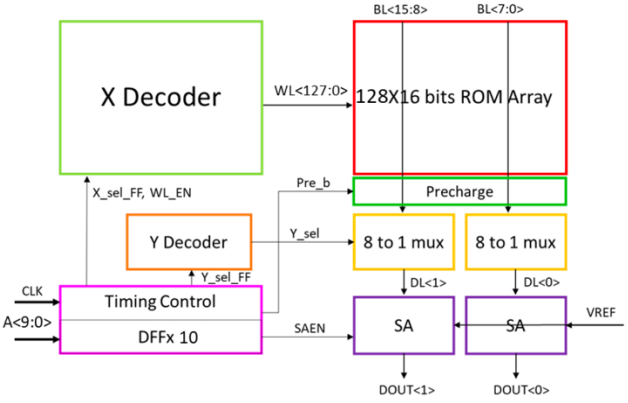

Fig. 1 Schematic of the ROM Macro

II. CIRCUIT MODUAL DESIGN

Since the access time needs to be smaller than 5ns, and the Figure of Merit (FoM) of our circuit is going to compete with the other classmates in class, the sizing of all the MOSFETs in the ROM Macro plays an important role. We have to carefully sizing the transistors for smaller delay and power consumption and make sure they are not too large for layout implementation in the meantime.

Here's our design consideration of the peripheral circuit clocks in the ROM Macro.

A. Overall Input and Output

(1) Inputs Signals:

The ROM Macro has a total of 12 input signals:10 input data signals(A[9:0]) 、1 global clock (clk) 、reference voltage (VREF)used by SA for comparison.

The 10 input signals A[0:9] pass through the D Flip-Flops on the rising edge of clk. These signals are divided into two groups: 7 bits (A[0:6]) and 3 bits (A[7:9]).

(2) X Decoder:

The first 7 bits (A[0:6]) are sent to the 7-to-128 X Decoder.After decoding, only one of the 128 WLs will be activated at a time. The activated WL will turn on the MOSFETs, connecting the BL to the data stored in the memory cells .

The data in the MC is determined by the presence or absence of a via (representing 1 or 0). Each BL will either discharge or remain the same. Before the clock rising edge, the BL will be precharged to a high voltage via a precharge circuit.

(3) Y Decoder:

The last 3 bits (A[7:9]) are sent to the 3-to-8 Y Decoder. According to the ROM macro schematic, the first 8 BLs and the last 8 BLs are passed into two 8-to-1 MUXs. The one-hot signal generated by the Y decoder will determine which BL from each set will be read into the DL.

(4) Reading BL Data:

After selecting the correct BL, the data on the BL is sent to the Sense Amplifier for comparison with the VREF signal. The final VREF value we used is 0.8V.

If the voltage on the DL is greater than VREF, the SA output is high (logic 1); otherwise, it is low (logic 0).

(5) SA Data Latching:

Since many modules in the design require an enable signal to decide whether they should work, and these enable signals typically have a narrow pulse, we connect the SA output to a D-Latch. This ensures that the data is held until the next clock rising edge.

B. D Flip-flop

In our design, the flip-flop is rising edge triggering of the clock. We use 10 DFFs to store the 10 input signals , A[9:0]. This ensures that the input signals are read only on the rising edge of the clock and are held until the next rising edge.

C. X decorder(7to128)

In previous logic designs, decoders were often implemented using AND gates for each output. However, using AND logic would result in an excessive number of transistors. Instead, a more efficient logic implementation is used:

abcdefg=(abc')+(defg')

In this case, we need to connect the 7-bit input data to the decoder. However, the input data will experience a delay due to the DFFs, so we introduce a WLEN (Word Line Enable) signal to ensure that data from the DFFs is correctly passed. When WLEN = 1, the data is valid and passed through; when WLEN = 0, the input is considered 0.To integrate this into the decoder, we AND each of the 10 signals A[9:0] with WLEN, ensuring that only valid data is passed to the decoder.

D. Time Control

The Timing Control circuit is considered the most challenging part of the design.It generates signals that control when other modules should be activated to ensure the correct operation of the ROM macro.

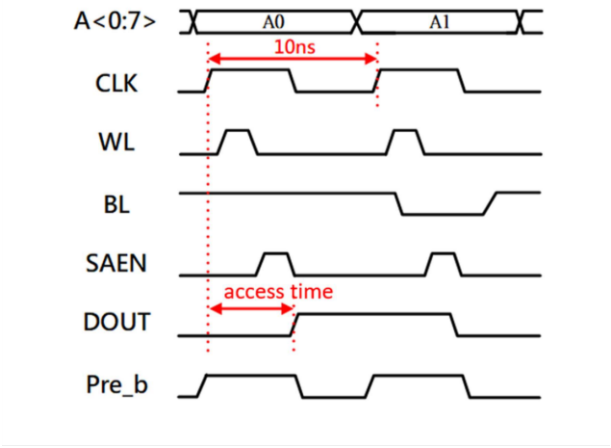

Fig. 2 Time control waveform

Key considerations include:Timing of when each circuit should be turned on or off and Activation sequence: The correct sequence in which different modules should be enabled to ensure the correct functionality of the entire system.

(1) clkb:

The clkb signal is used to provide the input signal for the D Flip-Flops .Since DFFs require an inverted clock signal for their slave part, clkb is generated from the global clock by using an inverter.

(2) Preb:

The Preb signal controls the activation of the precharge circuit. In the ROM macro, we need to precharge each BL to VDD before reading the data.

- On the rising edge of the clock, Preb is pulled low (0) to trigger the PMOS transistors to start charging the BLs to VDD .
- Once the precharging is done, Preb goes high (1), turning off the precharge circuit to stop further charging of the BLs.

(3) WLEN：to enable WL decoding

The WLEN signal is used to activate the 7-to-128 decoder for Word Line (WL) decoding. Once the data from the DFFs is ready, WLEN enables the decoder to select which WL to activate.The width of the WLEN signal directly impacts the discharge time of the BLs. If the width of WLEN is too narrow, the BL may not discharge sufficiently, causing incorrect data at the Data Line (DL).This issue is more pronounced at different process corners, particularly in the SF corner.

- We implement WLEN using a buffer chain with an inverter at the end and a 2-input AND gate.
- The number of buffers affects the width of the WL signal. Adding more buffers increases the duration of the WLEN signal. Additionally, the placement of buffers after the AND gate shifts the signal to the right, ensuring that the timing matches the requirements.
- By adjusting the length and number of buffers, we can achieve the correct delay and duration for the WL signal.

(4) SAEN：for enabling sense amplifier

The SA starts sensing when the Data Line (DL) voltage rises or falls within the reference voltage (VREF) range. The SAEN signal controls the sensing time of the SA. If the SA is highly efficient (strong sensing), SAEN does not need to be wide and output can be captured quickly. However, at corners where the SA performance decreases, SAEN must be wide enough to ensure that the voltage on DL drops/rises adequately for accurate sensing.After the SA successfully differentiates the DL voltage from VREF, SAEN is set to 0, and the data is latched by the D-Latch.The latched data is retained until the next SAEN activation

- We implement SAEN in a similar way as WLEN, using a buffer chain with an inverter at the end and a 2-input AND gate.
- However, in the ROM macro, the SAEN signal needs to be delayed longer than the WLEN signal to ensure proper voltage fluctuation during sensing. Therefore, we add additional buffer stages after the AND gate to introduce a longer delay for the SAEN signal.

E. 128× 16 ROM Array and Precharge Circuit

In this ROM Macro design, the ROM array consists of 128 Word Lines and 16 Bit Lines , so the entire ROM array contains 128 * 16 = 2048 memory cells . Each Bit Line is connected to a PMOS, with the Drain of the PMOS connected to the BL. The precharge circuit ensures that each BL is prepared to a known state before data is read.

The operation of precharge is as follows

- When Preb = 0，PMOS is turned on, allowing current to flow into the BL, charging the BL to VDD (high voltage).This ensures that before any Word Line (WL) discharges, all the BLs are at a known high voltage, preventing interference during reading.
- When Preb returns to 1，PMOS is turned off, ending the prechare.At this point, the BL voltage remains at VDD until discharge occurs based on the activation of the Word Line

(WL)As WL is activated, the specific BL will either discharge or maintain its value depending on the data stored in the memory cell (0 or 1).

F. 8 to 1 MUX

The circuit uses two sets of Bit Lines : BL<7:0> and BL<15:8>. The Y decoder controls which BL to select by activating one of the lines. The selected BL carries the signal that is sent to the Sense Amplifier for comparison with VREF. The Y decoder generates an 8-bit one-hot signal, where only one line is high (1) at a time. This signal is used by the Multiplexer (MUX) to select the corresponding Bit Line (BL) signal as the output.

- Each 8-to-1 Multiplexer (MUX) handles 8 Bit Lines (BL).
- There are two 8-to-1 MUXes:
  - The first MUX handles the first 8 Bit Lines (BL<7:0>).
  - The second MUX handles the last 8 Bit Lines (BL<15:8>).

G. Sense amplifier & D-Latch

Due to the signal voltage drop in the earlier stages, the difference between 0 and 1 may not be clear enough to distinguish. Therefore, a Sense Amplifier is used to amplify the signal (to full swing) and to detect the small difference between the two input signals.

The SA operation is controlled by SAEN. The SA will only begin working when SAEN = 1.

H. D-Latch after SA

Initially, we did not include a D-Latch in the design. Upon observing the waveform, we found that the amplified signal from the SA could not be maintained until the next clock cycle. As soon as SAEN transitions to 0, the signal from SA would disappear. To solve this issue, we realized that we needed a circuit to store the signal and maintain it. Thus, we decided to connect a D-Latch to the SA output. Since a D-Latch is a high-level trigger, we connected the clock of the D-Latch to SAEN. When SAEN falls to 0, the D-Latch will latch the output and retain it until the next cycle. This setup allows the signal to persist and ensures the desired functionality

III. Pre-simulation & Layout

During the pre-simulation, we encountered two common issues: failing at the SF corner and passing in the top-left corner but failing in the bottom-right corner.

(1). SF Corner Issue: During simulation at the SF corner, we often encountered a situation where the Sense Amplifier (SA) did not correctly detect the signal that needed to be sensed. To resolve this, we increased the Buffer chain count to introduce more delay, thereby widening and shifting the SAEN signal. This allowed the SA to sense the signal correctly. However, we later discovered that this approach could cause failures in the FS corner. To fix this, we adjusted the SA size to improve its sensing efficiency. Ultimately, this allowed all the corners to pass the pre-simulation and meet the specifications.

(2). Right-Bottom Corner Issue: The reason for this issue seemed to be the delay in the signal path. The WL signal in the bottom-right corner had to traverse the longest path, leading to the highest delay. If the circuit's setup time was insufficient, this would result in incorrect signal behavior. To address this, we modified the size of the X decoder, which helped speed up the signal propagation, ensuring that the signal reached the required destination at the correct time.

	Access time (ns)	Average Power (uw)
TT 25℃ (pre)	1.42	2403.6
FS 25℃ (pre)	1.36	2453.2
FF 25℃ (pre)	1.17	2815.0
SF 25℃ (pre)	2.08	1827.3
SS 25℃ (pre)	3.93	1507.2
TT 25℃ (post)	2.0175	2565.8

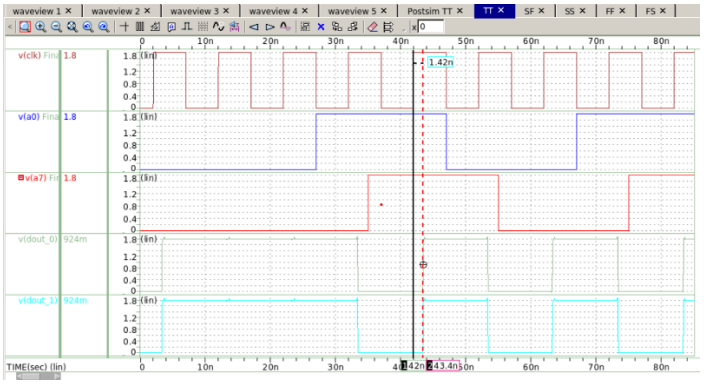

Fig.3 TT 25℃ (presim)

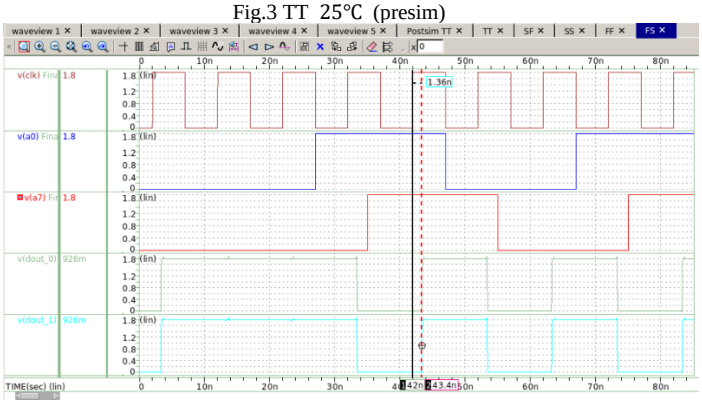

Fig.4 FS 25℃ (presim)

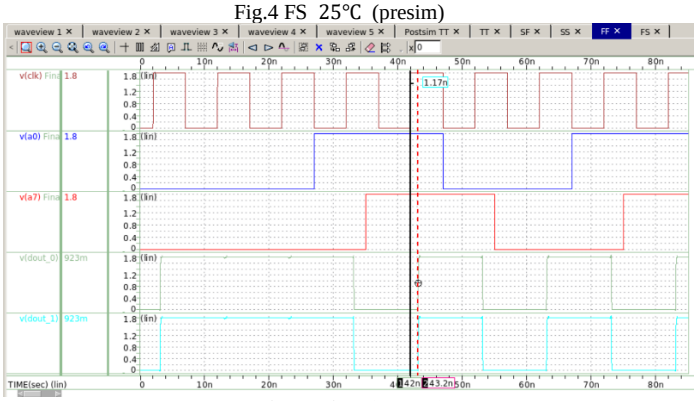

Fig.5 FF 25℃ (presim)

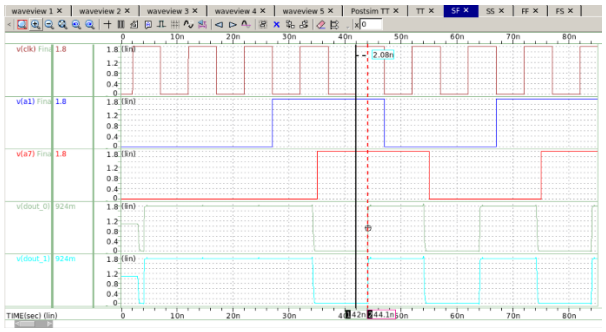

Fig.6 SF 25℃ (presim)

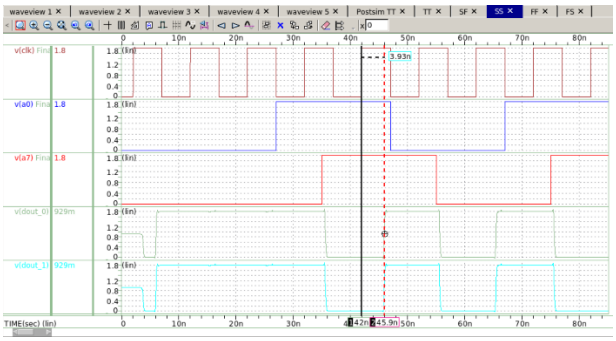

Fig.7 SS 25℃ (presim)

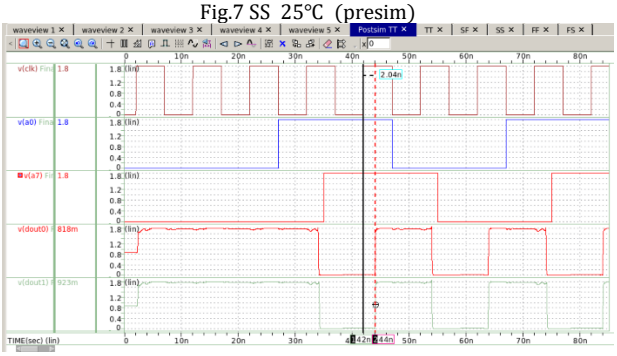

Fig.8 TT 25℃ (postsim)

Layout

(1). During presimulation and postsimulation, we discovered that as the circuit module size increases, sizing issues must be considered. Particularly when taking RC effects into account, maintaining the same sizing can lead to errors. To address this, we analyzed the signal waveforms at each step to identify areas for improvement. The adjustments we made include:

- Changing the decoder size to speed up input signal transmission.
- Increasing the presimulation size to ensure the bitline (BL) can reach 1.8V in a short time.
- Optimizing the placement of circuit modules to reduce delay. For example, placing the input signal A<9:0> and WLEN as close to the decoder as possible.

(2). Since we used larger sizes for the decoder and sense amplifier (SA), the layout area is relatively large, totaling **10956.72 μm²**. During presimulation adjustments, we focused on widening the enable signal but overlooked the fact that making it too wide could result in prolonged template activation time, which in turn increases power consumption.

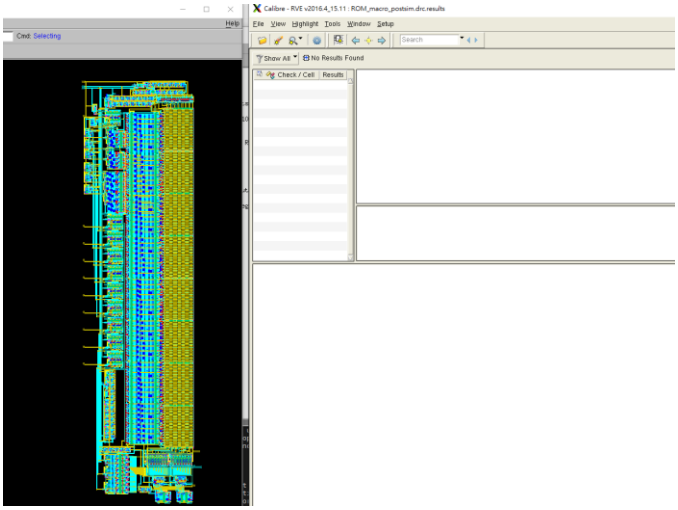

Fig.9 TT Layout DRC clear

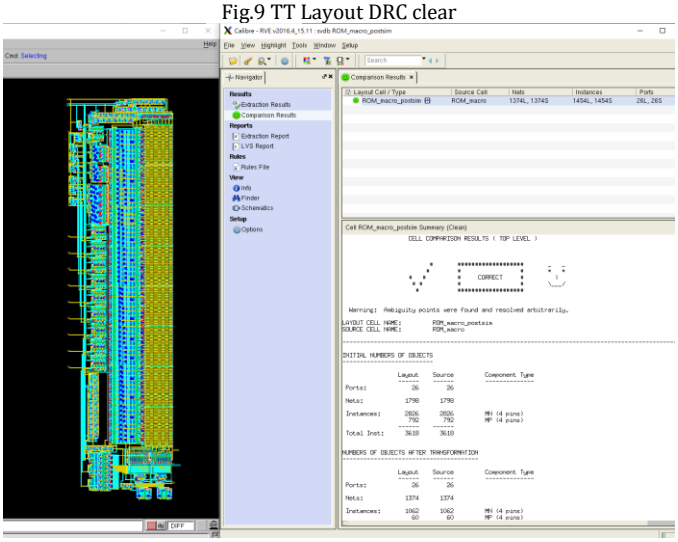

Fig.10 TT Layout LVS clear

IV. Comment Results

We achieve access time < 5ns at 5 corners at pre-sim by carefully sizing the MOSFETs. The access time and average power are shown in the following table.

TABLE I
PERFORMANCE OF EACH CORNER

	Access time (ns)	Average Power (uw)
TT 25℃ (pre)	1.42	2403.6
FS 25℃ (pre)	1.36	2453.2
FF 25℃ (pre)	1.17	2815.0
SF 25℃ (pre)	2.08	1827.3
SS 25℃ (pre)	3.93	1507.2
TT 25℃ (post)	2.0175	2565.8

Access time is the average of four $t_{c\text{-}q}$ delay at 4 corners of the ROM Macro. Also, the average power is power measured from VDD from 10ns to 50ns.

After a semester of rigorous VLSI coursework, we have learned the complete circuit design process—from confirming specifications and using tools to create schematics to designing layouts and finally extracting RC and performing post-simulation. By the end of the semester, we successfully

implemented a ROM macro and gained valuable insights into how to adjust circuits to operate effectively under different conditions.